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Abstract

A common challenge when designing compact fast switching multichip power modules based on wide bandgap semiconductors is imbalanced current sharing between the parallel dies. The issue arises in asymmetric layouts where different parasitic inductance values will be present in the individual power or gate loops for the parallel connected dies. Experimental verification of the current sharing between the dies in a multichip power module is limited by the lack of current sensing strategies suitable for performing accurate drain current measurements of each individual die. This paper proposes a two-stage current sensor consisting of a customizable current transformer and a Pearson current monitor. The current transformer can be embedded into a multichip power module with its core encircling a single die to provide measurements of the die's drain current. The concept is verified with a double pulse test performed at 200 V and 17.7 A of an asymmetric power module with four parallel connected silicon carbide dies. The measured die currents are compared to the total switch current measured with a 30 MHz Rogowski coil where the current imbalance due to the asymmetric layout is clearly seen.

1   Introduction

Power modules based on wide bandgap semiconductors require the designer to keep the parasitics in the module at a minimum for utilizing the full potential brought by wide bandgap as faster switching speed and higher blocking voltage compared to conventional Si. The fast switching speed is obtained through compact integrated packaging of the semiconductor devices where power and gate loops are designed to have an inductance in the nH range [1]. Typically, to reach higher power rating of the power module, multiple dies are connected in parallel which often causes the design to have some asymmetries. Such asymmetries provide a mismatch in the inductance between each individual gate or power loop for the parallel connected dies which leads to imbalanced current sharing and different stress profiles for the dies during operation [2] [3]. Hence it is a necessity to study the current sharing of the dies during the design verification phase. The combination of a compact and fast switching design increases the difficulty of performing accurate local current measurements in

each paralleled device inside the power module. The challenge is due to the high bandwidth that is required of the current sensor and the physical challenge of fitting the sensor into the power module without compromising the performance of the power module [1] [4]. Another issue when measuring the die current is the insertion inductance introduced by the chosen current sensor which has to be less than a few nH in order to not impact the switching transient [5]. As a consequence, designers utilize software as ANSYS Q3D for analyzing the current sharing imbalance and optimizing the layout of the design digitally [6], [7].

For quantifying experimentally that balanced current sharing between the dies in a multichip power module is obtained, the current sensor needs the following attributes; *(1)* galvanic isolation such that it is applicable for measuring both low and high side dies, *(2)* low insertion inductance such that the sensor has a minimum impact on the circuit and *(3)* high bandwidth. Additionally, there is a physical constraint in a power module that also limits the viable current probes. The typical current shunt is not a suitable candidate as it does not provide galvanic isolation. Both [6], [7] utilize a 30 MHz

Rogowski coil for measuring the current in each individual parallel connected die.The Rogowski coil has the advantage of galvanic isolation and it can fit around the source bondwires of a die. However its bandwidth of 30 MHz can be a limiting factor in faster switching designs based on wide bandgap semiconductors. Another limitation is that the Rogowski coil only can be used prior to the power module being encapsulated in gel and thereby not used for monitoring the current sharing after the testing phase. Nor can it be used as a part of a control scheme that ensures current balancing by measuring the current in each die. The Pearson current monitor meets the bandwidth requirement but is limited by its physical size, insertion inductance and potential saturation issue at high current amplitudes [4]. In [8], a two-stage current sensor with a transformer and a Pearson current monitor has been experimentally verified where it shows similar performance as a state of the art SDN-414-025 current shunt. The concept has only been tested for measuring the current in a discrete SiC MOSFET or the busbar current in an IGBT power module as the transformer of the current sensor cannot fit inside a power module. This paper proposes to use the two-stage current sensor concept and adjust the size of the transformer such that the drain current in each parallel connected die in a multichip power module can be measured. The proposed current sensor will be presented in section 2 and its applicability verified by measuring the current in a single die in section 3. In section 4, four current sensors are used to measure the current imbalance in an assymetric four chip power module. Lastly, section 5 includes a quantification of the parasitic winding to winding capacitance for the sensor using both ANSYS Maxwell and experimental verification.

2 Proposed Two-Stage Current Sensor

A sketch of the proposed two-stage current sensor is shown in Fig. 1 and consists of an embedded transformer and a Pearson current monitor model 2877 [9]. The transformer is placed on the drain plane on a power module substrate where its core is encircling the die which serves as the primary winding of the transformer. The secondary winding of the transformer is litz wire which is shorted through a Pearson current monitor. The concept of the proposed sensor is that a current through the die will have a magnetic field that induces a current in the secondary winding of the transformer. The secondary side current will go through the Pearson current monitor and can be read on an oscilloscope. Since the transformer is encircling the die and not its source bondwires, the proposed current sensor enables direct measurements of the drain current. This also applies for designs that do not utilize a kelvin source connection. In such designs the die current measured with a Rogowski coil will consist of both the gate and drain current.
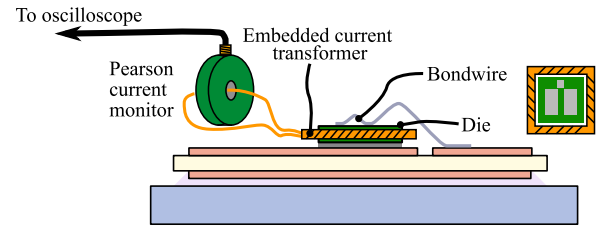
Fig. 1: The concept of the proposed two-stage current sensor.

The transformer core for the proposed sensor is made of silicon steel and can be easily manufactured to fit any semiconductor die. In this paper two different core sizes will be used. In section 3 the transformer core will have the following dimensions 7.1 mm x 4.5 mm x 0.3 mm whereas it will be 4.5 mm x 4.5 mm x 0.3 mm in section 4 such that the sensor can fit in the designed power module. The length of the secondary side winding can be adjusted by the designer such that the Pearson current monitor can be placed outside the power module. The transformer is then seen as an extension of the Pearson current monitor which facilitates local current measurements in compact power modules. The proposed sensor also has the potential to remain around the die after the power module is encapsulated by gel with its secondary windings connected to an outgoing terminal. This can potentially enable online die current measurements during operation of the power module which can be used for condition monitoring of the dies or as part of a current balancing control scheme.

Another advantage of the proposed sensor is that the transformer's turns ratio mitigates the saturation problem that can be an issue when using Pearson current monitors, effectively extending the range of measurable current amplitudes [10]. The Pearson current monitor 2877 however sets a restriction on the measurable rise times for the proposed current sensor which is defined by Eq. (1) [11].

$$t_{r,limit} = [3...5] \cdot \frac{0.35}{200\,\mathrm{MHz}} = [5.25\,\mathrm{ns}...8.75\,\mathrm{ns}] \quad (1)$$

It is chosen for the two initial prototypes to have either 43 and 31 number of turns on the secondary side which is the maximum possible number of windings for the two sizes of core without overlapping turns. This will aid in ensuring that the Pearson current monitor is not saturating. However, by having this many turns the parasitic winding capacitance on the secondary side of the transformer increases which will reduce the maximum obtainable bandwidth of the sensor [12].

3 Validation of the Proposed Current Sensor

The proposed current sensor is tested in a double pulse test (DPT) setup as seen in Fig. 2 where a CPM2-1200-0160B SiC die is used as the low side switch. The die current is measured with both a T&M W-1-005C-2FC 800 MHz current shunt and the proposed current sensor [13]. The two measurement methods will be compared where the current shunt measurement will be used for validating the performance of the proposed current sensor.

(a)
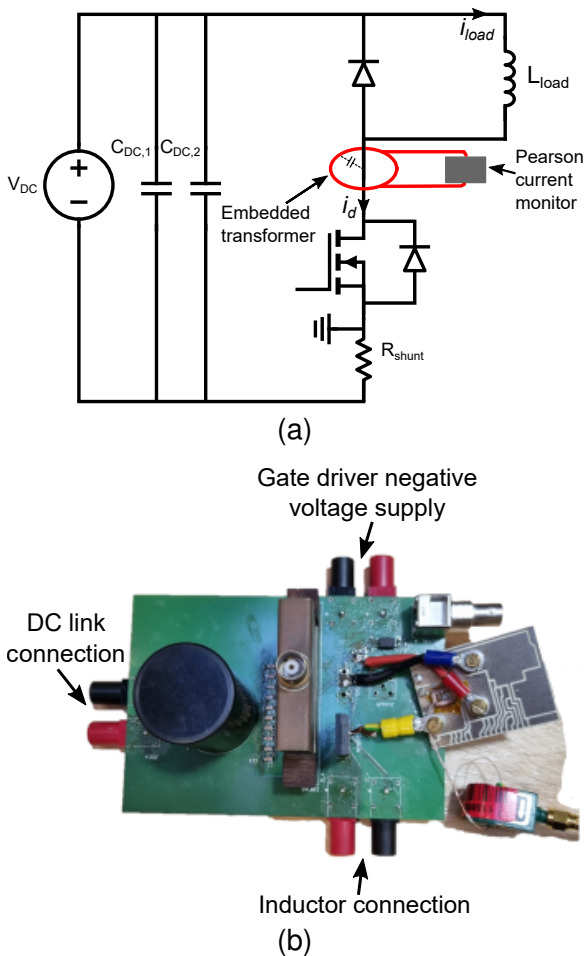
Fig. 2: (a) is a simplified circuit schematic of the DPT setup, (b) is the experimental DPT setup for validating the current sensor.

The DPT is performed at an input voltage of 30 V and a load current of 7 A. The inductance of the load inductor is 103 µH, a 4.7 µF film capacitor and ten 10 nF ceramic capacitors are used as DC link capacitors. The input voltage is 30 V due to the risk of destroying the die as it has not been encapsulated. In order to match the amplitude of the load current measured by the two methods during the DPT test, the current measured with the proposed sensor needs to be scaled according to the turns ratio of the embedded transformer and its magnetic coupling factor. The theory developed in [14] is used for scaling the sensor current where the measurement error due to the transformer's leakage inductance is taken into account by lifting up the waveform. The result of the DPT is seen in Fig. 3.

(a)

(b)
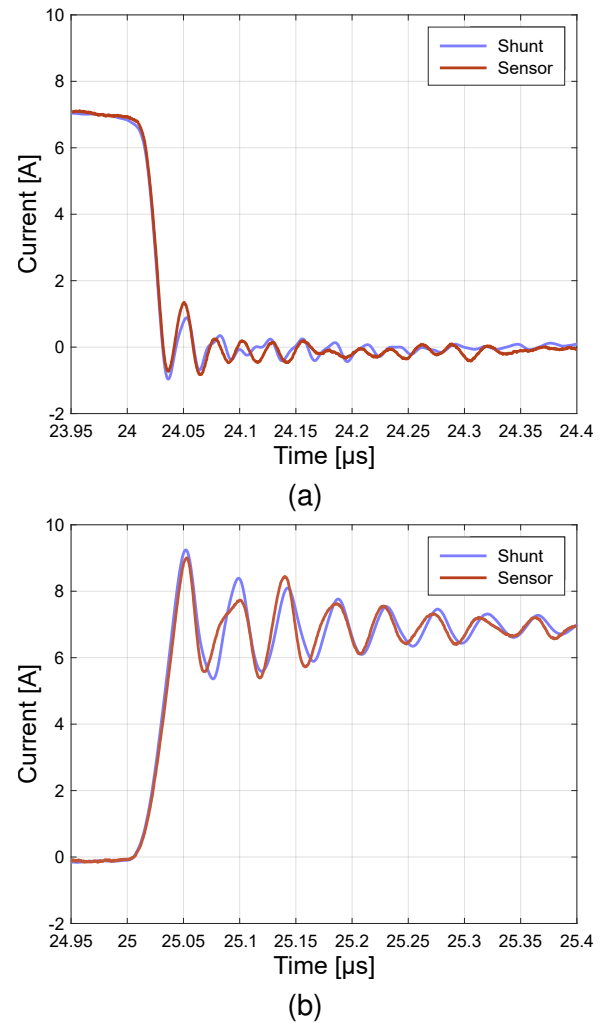
Fig. 3: The current switching transients from a DPT performed at V_{DC} = 30 V and i_{load} = 7 A.

A great resemblance between the two measurement methods is seen during both transients in regards to the 25 ns rise and fall time and also the resonance after both transients. Through an FFT of

both the shunt and sensor measurements after the switching transients, a 27 and 45 MHz resonance is seen after turn-OFF and a 27 MHz component is seen after turn-ON. Both resonance frequencies are ascribed to the high order self resonance of the load inductor. As the amplitudes and timing of the peaks of the resonances on both the shunt and sensor measurements after the switching transients match, it indicates that the bandwidth of the proposed sensor is above 45 MHz. This is further reinforced as the proposed sensor is capable of accurately measuring the 25 ns rising edge of the turn-ON transient, which using Eq. (1) would require a sensor bandwidth between 42 and 70 MHz. As the current sensor can accurately measure the drain current switching transient in a SiC die, it will be used for studying the current imbalance between parallel dies in an asymmetric layout.

4 Current Imbalance Measurements in Multichip Power Module

The designed power module for testing the proposed sensor's ability to measure current sharing is shown in Fig. 4.
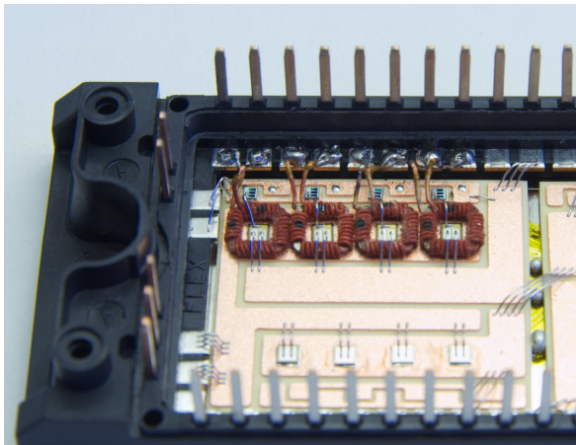

(a)
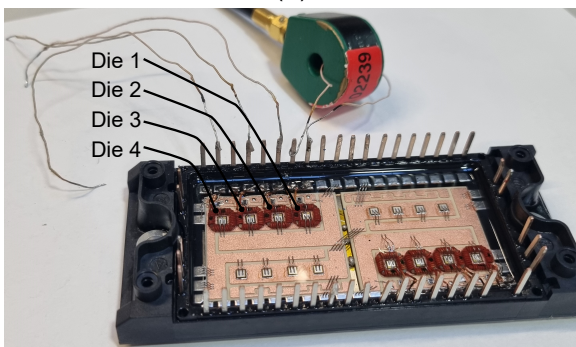
(b)

Fig. 4: (a) is a close up of the transformers encircling the dies and (b) is the designed power module where the circuit to the left is used for the DPT.

As mentioned in section 2 the dimensions of the current transformer core is 4.5 mm x 4.5 mm x 0.3 mm and the secondary side windings of the transformer are 31 turns of litz wire. The ends of a transformer's secondary windings are connected to two separate pins of the power module which are shorted through the Pearson current monitor. The SiC dies (CPM2-1200-0160B) are paralleled in an asymmetric layout which will introduce an imbalance during the switching event due the different parasitic inductances in each specific die's gate loop. A schematic of the gate loops are shown in Fig. 5 where L_b represents the inductance introduced by the source bondwires, L_d is the trace inductance from the load inductor connection to Die 4 and L_{ss} is the source inductance from Die 1 to the negative DC terminal. L_{dn} and L_{nn} are the inductances between each neighbouring die in either the drain plane or the source plane. From the analysis in [2] and [3], Die 1 will experience the smallest impact from the parasitic inductances. Therefore it is expected that Die 1 will switch faster than the three other dies and carry the biggest portion of the load current during the switching transients.
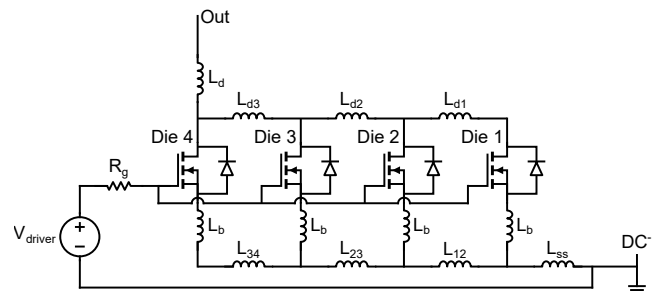
Fig. 5: Simplified schematic of the parasitic inductances in the four gate driver loops causing the current imbalance in the designed power module [2].

The DPT is carried out four times as only one Pearson current monitor was available and the drain source voltage is used as the trigger signal. The current sensor measurements are scaled using the same method as in section 3. The DPT is performed at an input voltage of 200 V and a load current of 17.7 A. The inductance of the load inductor is 103 µH, a 4.7 µF film capacitor and ten 10 nF ceramic capacitors are used as DC link capacitors. A 30 MHz CWT Ultra mini Rogowski coil is used to measure the total switch current which will be compared to the sum of the individual die currents measured with the four current sensors as shown in Fig. 6 [15].
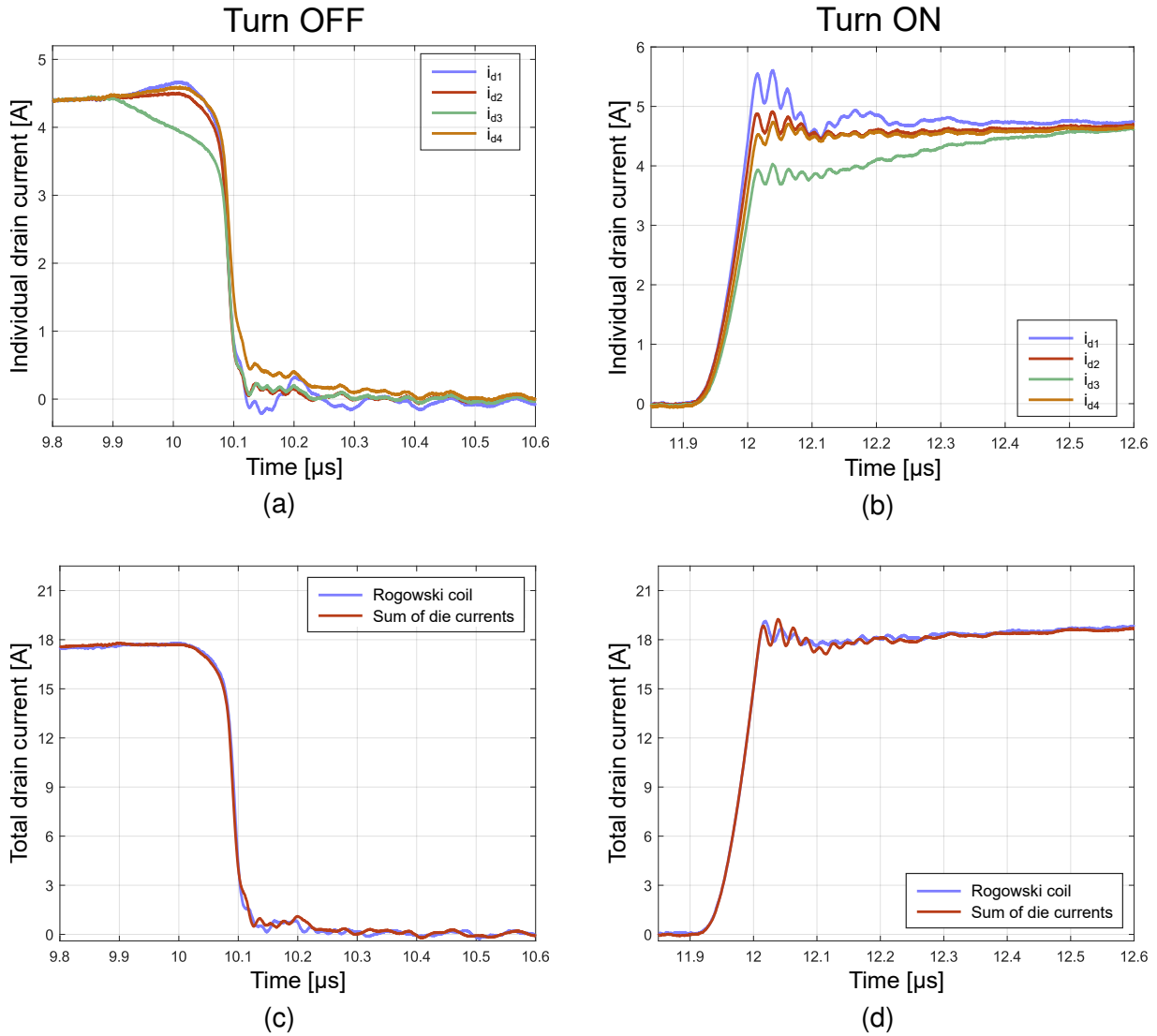
Fig. 6: DPT performed at V_{DC} = 200 V and i_{load} = 17.7 A. (a) and (b) is the OFF and ON current transients of each die measured with the proposed current sensors. (c) and (d) shows the summation of the four die measurements compared to a measurement of the total drain current with the Rogowski coil.

From the experimental results shown in Fig. 6 (a) and (b) a clear current sharing imbalance is seen between the four dies during both switching transients. As predicted Die 1 is turning ON faster than the remaining three and is carrying the biggest portion of the load current during turn-ON whereas Die 3 is carrying the smallest portion. A comparison of the read peak current values and the rise times during the turn-ON transients for the four individual dies is seen in table 1. During the turn-OFF transient, Die 3 is also the one that is diverging the most. The current through it is starting to decrease prior to the other three dies which is forcing Die 1 and 4 to carry more of the load current before actually turning OFF. Figure 6 (c) and (d) show the total switch current which appears close to ideal besides

from the 45 MHz resonance after turn-ON which again is ascribed to a self resonance of the load inductor. By only investigating the total switch current during both switching transients, the designed power module does appear as a good design. But the relevancy of performing local current measurements during testing is clearly emphasised from the individual die current measurements obtained using the proposed current sensor.

Tab. 1: Recorded peak current values and rise times during turn-ON. The rise time is measured from 20 to 80 % of the switched die current.

	Die 1	Die 2	Die 3	Die 4
Peak Current [A]	5.6	4.9	4.0	4.7
Rise time [ns]	39.6	43.5	49.4	45.1

5 Parasitic Common Mode Capacitance Investigation

The transformer of the two-stage current sensor has to encircle either the die or the bondwires connecting the die to the source plane in order to measure the die current. This placement can however introduce a challenge with measurement inaccuracies due to the parasitic common mode capacitance, C_w, between the embedded transformer and the drain plane. The increased blocking voltage and high switching speed provided by WBG yields a rate of change in the voltage potential between the drain plane and the secondary side windings of the sensor that potentially can create a non negligible common mode current in the secondary side windings. The parasitic common mode capacitance depends mainly on the shape of the embedded current transformer, the number of secondary windings, how the windings are configured and the distance between the transformer and the drain plane. The size of C_w for the prototype 31 windings transformer used in section 4 will be determined using a combination of an experimental setup and an LTspice model. Moreover, ANSYS Maxwell will be used to investigate in what extent C_w is influenced by the number of secondary windings and the distance between the sensor and the drain plane.

## 5.1 Experimental Investigation

A schematic of the experimental setup used for determining C_w is seen in Fig. 7 and consists of a function generator, an oscilloscope, the embedded current transformer in the power module and a measurement PCB containing a BNC connector and a $2.1\,\text{k}\Omega$ resistor.
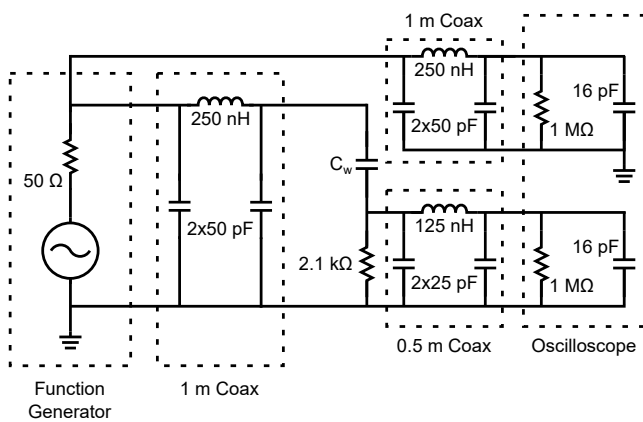
Fig. 7: A circuit schematic of the test used for determining C_w of the embedded transformer.

The output terminal of the function generator is split into two separate 1 m coaxial cables. The first is connected to an oscilloscope for measuring the input voltage to the test setup. The positive end of the second coaxial cable is connected to the drain plane in the power module and its negative end to the ground potential on the measurement PCB. The secondary side winding of the current transformer is shorted and connected to the main pin of the BNC connector on the measurement PCB. A $2.1\,\text{k}\Omega$ resistor is placed in parallel to the BNC connector which is connected to the oscilloscope by a 0.5 m coaxial cable for measuring the output voltage of the setup. All coaxial cables are of the type RG58 and modelled using the π model where the capacitance is 100 pF/m and the characteristic impedance of each cable is $50\,\Omega$. C_w of the embedded transformer is determined by performing a frequency sweep from 10 kHz to 20 MHz of a sine wave at an amplitude of ±10 V. An LTspice model of the experimental setup is created including the parasitics of the different cables and the oscilloscope, due to the high frequencies the sweep is performed at. The in- and output voltages are measured together with the phase between them. The capacitance of C_w is adjusted until the most optimum match at all frequency points are found between the experimental data and the LTspice model. The obtained experimental data together with the fitted simulation data from LTspice is seen in Fig. 8.
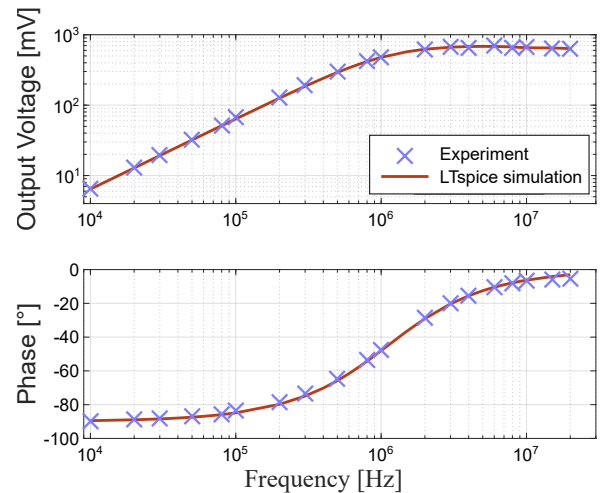

Fig. 8: The measured output voltage and phase of the experimental test together with the fitted simulation data using a C_w of 2.5 pF.

The C_w between the embedded transformer and the drain plane in the power module is found to be approximately 2.5 pF. A parasitic capacitance in this range can introduce unwanted noise on the

measured die current especially if the application for the sensor is medium voltage SiC dies. In the following section the impact on C_w from the number of turns on the secondary side and the distance between the embedded transformer and the drain plane is investigated.

5.2 Ansys Maxwell Investigation

A 3D model of the power module used in section 4 is inserted into ANSYS Maxwell as seen in Fig. 9 where an electrostatic analysis is performed to determine C_w. The distance between the drain plane and the transformer is varied in the y-direction from 0.02 to 0.10 mm in steps of 0.01 mm. The simulation is performed 4 times with 4 different number of secondary windings; 16, 21, 26 and 31. The obtained parasitic capacitances are seen in Fig. 9.

(a)

(b)
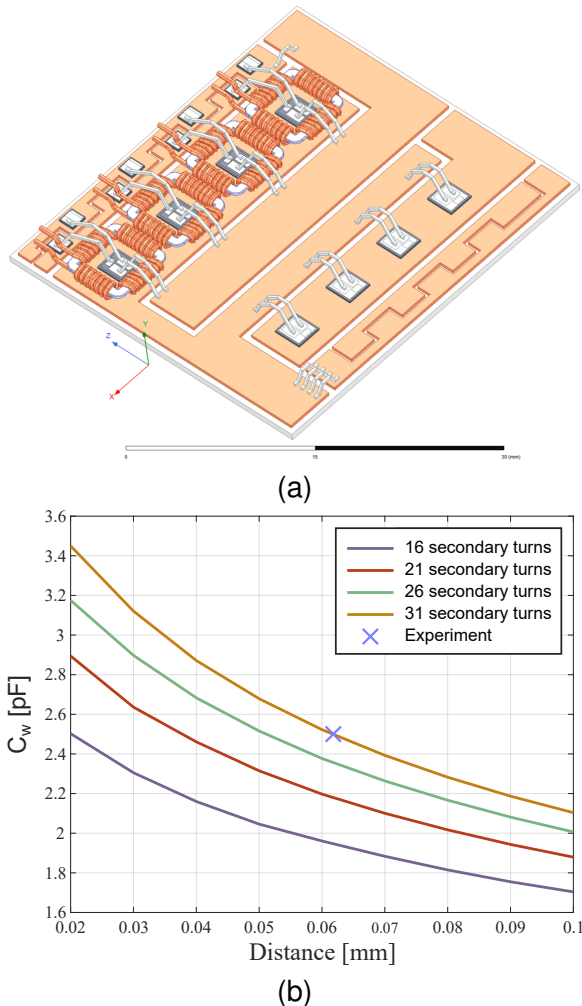
Fig. 9: (a) shows a 3D model of the embedded sensor and power module used in ANSYS Maxwell and (b) is the extracted C_w when the distance between the transformer and drain plane is varied for various number of secondary windings.

From the ANSYS Maxwell analysis it is clearly seen that a designer is incentivized to increase the distance between the transformer and the drain plane using e.g. a small fixture or coating to lift the transformer. But the transformer including its windings already has a height of approximately 1.5 mm and a fixture to increase the distance will force the designer to increase the height of the bondwires which will introduce extra parasitic inductance in the design. By choosing fewer secondary windings of the transformer C_w can also be lowered. The trade off is however that the current through the secondary will increase together with the likelihood of saturating the Pearson current monitor. A lower number of secondary windings can also potentially reduce the magnetic coupling of the transformer which will have a negative effect on the size of the leakage inductance introduced by the transformer into the circuit.

6 Conclusion

This paper proposes a two-stage current sensor concept consisting of a customizable transformer and a Pearson current monitor. The concept has the advantage of being galvanic isolated and has a proven bandwidth above 45 MHz. The sensor is used to study the imbalanced current sharing between four silicon carbide dies in an asymmetric power module during a double pulse test. A mismatch between the currents through the four dies is clearly seen both in rise time and peak current. The total switch current is measured with a Rogowski coil and compared to the summation of the individual die current measurements where a great resemblance is seen. The total switch current of the dies falsely gives the indication that the design of the power module is ideal which emphasizes the value of using the proposed current sensor during testing of parallel connected silicon carbide dies.

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