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Preface

This thesis is written under the Industrial Ph.D. Fellowship EF 682, financially supported by Danfoss Drives A/S and the Danish Academy of Technical Sciences (ATV) and submitted to the Faculty of Engineering and Science at Aalborg University as part of the requirements for obtaining the Ph.D. degree.

Four persons have supervised the project during the project period (November 1997 – November 2000): Prof. Frede Blåbjerg and Assoc. Prof. John K. Pedersen, both from the Institute of Energy Technology, Aalborg University, Paul Thøgersen and Peter Nielsen, both from Danfoss Drives A/S. I want to thank them for their response to my work during the project period. Also I appreciate the support and supervision by NESA A/S in person of Steen M. Munk and Anders E. Petersen.

During the three years, working on this project, I had the opportunity to discuss my work with different people from various countries. All these people have somehow influenced the results presented in this thesis and I want to express my gratitude to you all.

Especially I want to thank Prasad Enjeti for many ideas and discussions during my stay for four month at the Power Quality Laboratory at Texas A&M University. Also I want to express my thanks to Sangsun Kim and Jaehong Hahn for guiding me through the laboratory and College Station.

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Finally, I want to thank all my colleagues at Danfoss Drives A/S. Especially Ejgil Petersen for the newest updates on the European Standards and Johnnie Jensen (Danfoss Electronic Drives in Rockford, USA) for sharing his insight knowledge on the market related aspects of harmonic distortion and rectifier topologies.

Graasten, November 2000

Steffan Hansen

Abstract

This thesis deals with the harmonic distortion of the diode rectifier and a number of alternative rectifier topologies for adjustable speed drives. The main intention of this thesis is to provide models and tools that allow easy prediction of the harmonic distortion of ASD's in a given system and to find reasonable (economical) solutions if the harmonic distortion is exceeding acceptable levels.

To define some acceptable harmonic levels, the international standards IEC 61000-2-2, IEC 61000-2-4, the harmonic limiting standards EN 61000-3-2, EN 61000-3-12 (draft) and IEEE 519-1992 are reviewed.

Models and calculation methods for predicting the harmonic distortion in a given application are discussed. Simple voltage distortion calculation methods are shown and it is pointed out that exact calculation of the resulting harmonic voltage distortion takes the background distortion into account. It is recognized that the harmonic impedance in a given system, which must be known for calculation of the harmonic voltage distortion, can be difficult to determine exactly. This issue is therefore discussed.

Four levels of models for the harmonic current generation of both the single-phase and three-phase diode rectifier are presented. The first level is an ideal model where the diode rectifier basically is treated as an independent (harmonic) current source. The second level is an empirical model, where simulated (or measured) values of the harmonic currents of the diode rectifier for different parameters are stored in tables. The third level is found by analytical calculations and very precise results are obtained. The fourth level is the use of circuit-based simulators, which guarantees high precision even under non-ideal conditions. By use of the numerical circuit-based simulator SABER the phase-angle of the individual harmonic currents of different diode rectifier types is analyzed.

Four selected rectifier topologies with a high input power factor are presented. It is shown that using ac- or dc-coils is a very simple and efficient method to reduce the harmonic currents compared to the basic diode rectifier. Also the 12-pulse topology is analysed and a quite low total harmonic current distortion is shown possible with this topology. However, it is also shown that the 12-pulse topology is sensitive to unbalanced and pre-distorted grid. Furthermore, the basic control strategies of the active rectifier are discussed and the active rectifier is shown capable of near sinusoidal line-current, bi-directional power flow, the possibility to reduce the dc-link capacitor size and a controllable dc-link voltage. Finally, a new integrated single-switch approach for the three-phase rectifier based on the third harmonic injection scheme is proposed. The proposed scheme shows that significant reduction of line-side harmonics is possible.

Also different system level harmonic reduction techniques are presented. It is shown that mixing single- and three-phase diode rectifier loads always reduce the total amount of 5^{th} and often the 7^{th} harmonic current in the system. The quasi 12-pulse topology is shown competitive or even superior to a true 12-pulse rectifier because of a low total harmonic distortion in most of the operating area. It is stated that a reduction of the voltage distortion by a factor of two can be expected compared to a 6-pulse diode rectifier with dc- or ac-

coils. Capacitor banks for displacement power factor correction can be used for passive filtering in applications where displacement power factor correction is needed. Significant harmonic reduction can hereby be achieved. However, these filters have some major drawbacks that are discussed. A lot of the problems arising with the use of passive filters, such as large reactive power generation and resonance conditions can be avoided when using an active filter instead of passive filters. The basic control strategies of the active filter are discussed.

Finally a cost - benefit analysis is presented based on available market information and a general step-by-step approach is proposed to find the cost-optimal rectifier topology that fulfills individual requirements. The applicability of the stepwise method to find the cost-optimal rectifier is demonstrated by a real application example. An easy-to-use calculation tool is developed for doing the required calculations.

Danish summary

Denne Ph.D. rapport omhandler harmonisk forvrængning af diodeensretteren og nogle ensrettertopologier for frekvensomformere til variabel hastighedsstyring af motorer. Formålet med denne rapport er, at frembringe modeller og værktøjer der tillader nem forudbestemmelse af den harmoniske forvrængning forårsaget af frekvensomformere i et givet system, samt at finde fornuftige løsninger hvis den harmoniske forvrængning overstiger et acceptabelt niveau.

Acceptable niveauer er defineret ved at gennemgå de internationale standarder IEC 61000-2-2, IEC 61000-2-4, de harmonisk begrænsende standarder EN 61000-3-2, EN 61000-3-12 (draft) og IEEE 519-1992.

Modeller og beregningsmetoder for forudbestemmelse af den harmoniske forvrængning i en given applikation er diskuteret. Simple spændingsforvrængningsberegninger er vist, og det er fremhævet, at der skal tages højde for baggrundsforvrængning for en præcis beregning af de harmoniske spændinger. Det er erkendt, at impedansværdierne, som er nødvendige for at beregne den harmoniske spænding, kan være svære at bestemme præcist. Dette problem er derfor behandlet.

Modeller for de harmoniske strømme fra både enfasede og trefasede diodeensrettere er vist på fire niveauer. Det første niveau er en ideel model, hvor diodeensretteren er behandlet som en uafhængig (harmonisk) strømkilde. Det andet niveau er en empirisk model, hvor simulerede (eller målte) værdier af de harmoniske strømme er gemt i tabeller for forskellige parametre. Det tredje niveau er bestemt ved analytiske beregninger, der viser sig at være meget præcise. Det fjerde niveau er brugen af numeriske beregningsværktøjer, der garanterer høj præcision selv under ikke-ideelle forhold. Ved brug af det numeriske, kredsløbsbaserede simuleringsværktøj SABER er fasevinklerne på de individuelle harmoniske strømme analyseret for forskellige diodeensrettertyper.

Fire udvalgte ensrettertopologier med en høj indgangseffektfaktor er præsenteret. Det er vist, at brugen af ac- eller dc-spoler er en meget simpel og effektiv metode til at begrænse de harmoniske strømme sammenlignet med den basale diodeensretter. Desuden er 12-puls topologien analyseret, og en lav total harmonisk strømforvrængning er fundet muligt. Det er dog også vist, at 12-puls topologien er følsom overfor spændingsubalance og baggrundsspændingsforvrængning. Endvidere er den grundlæggende kontrolstrategi for den aktive ensretter behandlet og den aktive ensretter er fundet egnet til nær sinusformet strømme, bi-direktionelt effektflow, mulighed for reduceret mellemkredskondensator og kontrollerbar mellemkredsspænding. Til sidst er en ny integreret enkelt-switch topologi præsenteret baseret på ideen om cirkulation af en tredje harmonisk strøm. Den nye topologi viser at en signifikant harmonisk reduktion er mulig.

Endvidere er forskellige topologier til reduktion af harmoniske strømme på systemniveau behandlet. Det er vist at blanding af enfasede og trefasede diodeensrettere altid reducerer den 5. harmoniske og ofte den 7. harmoniske strøm. Quasi 12-puls topologien viser sig konkurrencedygtig eller endda bedre end den ægte 12-puls ensretter med en lav total harmonisk strømforvrængning i det meste af belastningsområdet. En halvering af

spændingsforvrængningen kan forventes sammenlignet med en 6-pulse diodeensretter med dc- eller ac-spoler. Kondensatorbatterier til reaktiv VAr kompensering kan bruges til passiv filtrering i applikationer hvor reaktiv VAr kompensering er nødvendigt. Betydelig harmonisk reduktion kan opnås. Disse filtre har dog nogle enorme ulemper, såsom mulighed for resonance, der er diskuteret. En del af de ulemper der opstår ved brug af passive filtre kan undgås ved at bruge aktive filtre i stedet for. Den grundlæggende kontrolstrategi for aktive filtre er behandlet.

Endelig er en cost-benefit analyse præsenteret baseret på tilgængelig markedsinformation, og en generel anvendelig metode er foreslået til bestemmelse af en omkostningsoptimal ensrettertopologi. Anvendeligheden på den foreslåede metode er demonstreret ved et applikationseksempel fra den virkelige verden. Desuden er et nemt anvendeligt beregningsværktøj udviklet til at hjælpe med de nødvendige beregninger.

List of Content

Abbreviations and Symbols

Abbreviations

CCM	continuous conduction mode
DCM	discontinuous conduction mode
DPWM	discontinuous pulse width modulation
Hc	harmonic constant
HV	high voltage
IPC	in plant point of common coupling
LV	low voltage
MV	medium voltage
PCC	point of common coupling
PWHD	partial weighted harmonic distortion
PWM	pulse width modulation
TDD	total demand distortion
THD	total harmonic distortion
THD_i	total harmonic current distortion
THD_v	total harmonic voltage distortion

Symbols

a, b, c	index of the three-phases in the three-phase system
a', b', c'	index of the three-phases in an alternative system (e.g phase shiftet 15°)
a'', b'', c''	index of the three-phases in an alternative system (e.g phase shiftet -15°)
C_B	capacitor bank for displacement power factor correction
C_{dc}	dc-link capacitance
d	index of voltage oriented coordinate system
e_n	negative sequence voltage vector
e_p	positive sequence voltage vector
e_r	transformer short circuit resistance
e_x	transformer short circuit reactance
e_z	transformer short circuit impedance
f	frequency
h	harmonic order
Hc	harmonic constant
I_{dc}	dc-link current(from rectifier to dc-link capacitor)
I_h	harmonic current of the order h
I_L	maximum demand load current
I_n	negative sequence current
I_o	dc-link current(from dc-link capacitor to load)
I_p	positive sequence current
I_{rms}	rms (root means square) current
I_s	system current
I_{sa}, I_{sb}, I_{sc}	system current phase 'a', phase 'b', phase 'c'
I_0	zero sequence current
I_1	fundamental current

L_B	boost inductance
L_{dc}	dc-link inductance
L_s	system line inductance
q	index of voltage oriented coordinate system
R_{sce}	short circuit ratio
S_{sc}	short circuit power
S_{nom}	nominal (nameplate) apparent power of equipment
S_{xfr}	transformer rated apparent power
sw	Switching function
S_1	fundamental apparent power
u	degree of voltage unbalance
U_{conv}	converter voltage vector
U_h	harmonic voltage of the order h
$U_{h,PCC}$	resulting harmonic voltage of the order h at the PCC
$U_{h,0}$	background harmonic voltage of the order h
U_{ll}	line-line voltage
U_{nom}	nominal (nameplate) voltage of equipment
U_s	system line-neutral voltage
$U_{sa,}$ $U_{sa,}$ U_{sa}	system line-neutral voltage phase ‘a’, phase ‘b’ and phase ‘c’
U_1	fundamental voltage
X_c	capacitor bank reactance
X_d''	subtransient reactance of a synchronous generator
X_h	harmonic reactance of the order h
X_{sc}	system short circuit reactance
X_{xfr}	transformer short circuit reactance of the order h
X_1	reactance at fundamental frequency
Z_b	base impedance
Z_h	harmonic impedance of the order h
Z_{xfr}	transformer short circuit impedance
α	index of the stationary coordinate system
β	index of the stationary coordinate system
μ	commutation angle
ω	angular frequency

Definitions

Hc $$Hc = \frac{\sqrt{\sum_{h=2}^{\infty} h^2 \cdot I_h^2}}{I_1} \cdot 100\%$$

R_{sce} $$R_{sce} = \frac{S_{sc}}{S_1}$$

TDD $$TDD = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_L} \cdot 100\%$$

THD_i $$THD_i = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_1} \cdot 100\%$$

THD_v $$THD_v = \frac{\sqrt{\sum_{h=2}^{\infty} U_h^2}}{U_1} \cdot 100\%$$

PWHD $$PWHD = \frac{\sqrt{\sum_{h=14}^{\infty} h \cdot I_h^2}}{I_1} \cdot 100\%$$

u $$u = \frac{e_n}{e_p}$$

per-unit impedance values are defined by the base impedance (Z_b) in proportion to the impedance at the fundamental frequency, where $Z_b = \frac{U_{nom}^2}{S_{nom}}$.

1. Introduction

Advantages, such as energy optimal control, smaller and cheaper apparatus because of less passive components, have increased the use of electric loads controlled by power electronic converters over the last decades. Today power electronic converters can be found in various applications, e.g. PC's, TV's, stereos, VCR's. Also in the industry adjustable speed drives (ASD) and uninterruptible power supplies (UPS) are commonly used. Without any doubt, power electronic converters are an important and unquestionable part of the modern society.

One area where power electronics is growing in importance is the energy saving of electrical apparatus by more efficient use of electricity. In fact, it has been stated that 15% - 20% of electricity consumption can be saved by extensive application of power electronics [Bose 2000]. This is especially true for ASD's because electrical motors consume 56% of the total consumed electrical energy [Abrahamsen 2000] and power electronic converters control only 10% of these motors [Thøgersen et al. 1999].

Unfortunately, the increasing use of power electronic converters has also led to an increase of harmonic voltage level on the utility grid as shown in Figure 1-1.

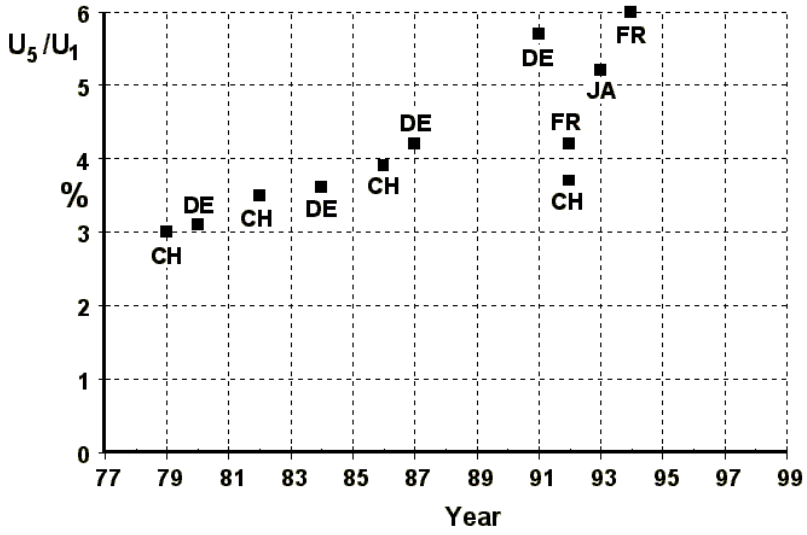


Figure 1-1 Increase of the 5th harmonic voltage levels since 1979 measured in Germany (DE), Switzerland (CH), Japan (JA) and France (FR). [Working document IEC77A/WG1/TF3 07-99, 1999]

In the last decade or so, the focus on harmonic distortion has sharpened. Standards and guidelines have been made to protect the power system and equipment from hazardous levels of harmonics. Unfortunately, these standards and guidelines have some unwanted effects.

In the attempt to limit the harmonic currents generated by certain equipment some standards aim at a level that requires expensive measures and the economical advantage that power electronics gives (e.g. energy savings) are vanishing. For example in the heating, ventilation and air-conditioning (HVAC) market this may result in that the

payback time for using ASD's is too large and the customer prefers a HVAC unit without any ASD control. This results in increased energy consumption compared with if an ASD was used. This was probably not the intention by the harmonic limiting standards.

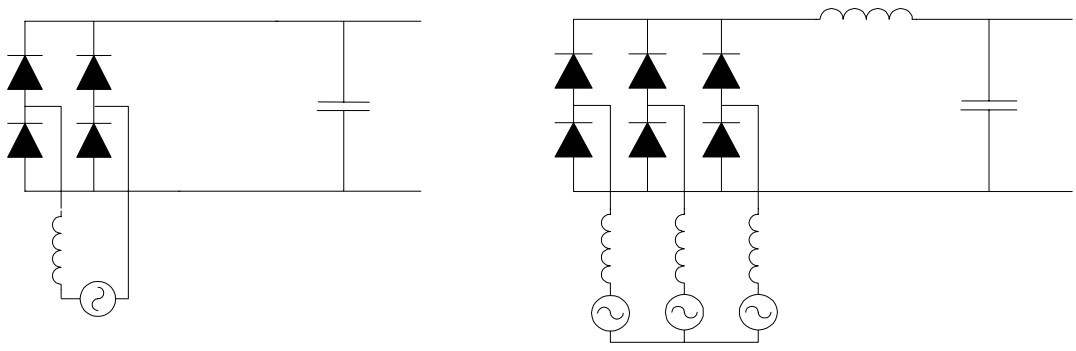
Also engineers not familiar with details on harmonic distortion become uncertain how to handle the various aspects arising with harmonic distortion. Statements, such as "harmonics can result in failure of…" have been the reason why consulting engineers and customers of power electronic equipment now fear harmonic distortion even though they may never have experienced any problems. They specify (or buy) expensive converters or filters where it may not be necessary.

In order to fully use the advantages of power electronics in the future a fair discussion of harmonics is needed, but this requires knowledge. What causes harmonics? What are the effects? And what are the solutions? In this chapter these three questions posed are discussed and different references are reviewed. Based on this, the final objectives of the present thesis are stated.

1.1 What Causes Harmonics?

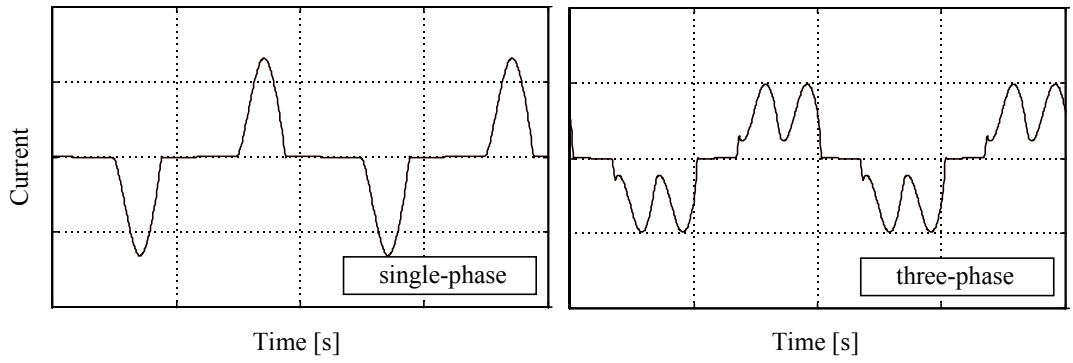
The main cause of harmonics in today's power system is power electronic equipment, namely the diode rectifier, which probably is the most used power electronic converter to interface with the utility grid. The diode rectifier is converting the ac-voltage to dc-voltage. Different kinds of power electronic converters are then controlling the voltage and current to the load.

It is the non-linear characteristics of the diode rectifier that cause harmonic currents. The circuit diagrams of a typical single-phase and three-phase diode rectifier are shown in Figure 1-2, and the typical ac-line current of these rectifier configurations is shown in Figure 1-3. It is clearly seen that the current is not sinusoidal.



(a) (b)

Figure 1-2: (a) Single-phase diode rectifier with a capacitor in the dc-link for smoothing the dc-voltage. (b) Three-phase diode rectifier with dc-link capacitor and a dc-link inductance for smoothing the input current.



(a) (b)

Figure 1-3: Typical line current of (a) single-phase diode rectifier (b) three-phase diode rectifier.

The reason for the wide spread use of the diode rectifier is simple. So far, the diode rectifier is superior to any other possible power electronic converters interfacing to the utility grid because of advantages such as:

- Robustness
- Efficiency
- Price
- Size
- Reliability

It is the large amount of the single-phase diode rectifiers used in consumer electronics that cause the harmonic distortion in the power system today and the problems that are arising with it. Even though the three-phase diode rectifier normally is used in a higher power range than the single-phase rectifier, the number of connected rectifiers is much smaller thus the three-phase rectifier seldom is the cause for harmonic distortion in the Medium (MV) or High Voltage (HV) line. [Kaendler 1995] [Gretsch, Gunselmann 1989], [Gretsch, Gunselmann 1991]

There is other equipment too that causes harmonic currents, but their influence to the overall power system is limited compared to the diode rectifier. However, this equipment may have significant influence to the local power system. The most important harmonic sources, besides the diode rectifier, are:

- Controlled rectifiers such as thyristor controlled 6-pulse rectifiers
- Arc furnaces
- Saturated magnetic devices, such as transformers
- Rotating machines

Normally, the harmonic currents are considered flowing from the non-linear load into the source. Because of the impedance between the equipment and the utility source the harmonic current is generating a voltage drop. This harmonic voltage drop is the reason for that the utility voltage is not sinusoidal but becomes distorted. Basically, the harmonic voltage of the order h (U_h) can be calculated as a product of the harmonic impedance of the order h (Z_h) and the harmonic current of the order h (I_h) as shown in equation 1.1.

$$U_h = Z_h \cdot I_h \tag{1.1}$$

The harmonic impedance, however, is frequency dependent in a non-linear manner due to skin- and proximity effects [Heiß et al. 1994]. Furthermore, predicting the harmonic currents of the diode rectifier is not simple, even though the diode rectifier is a very simple topology. Among other factors, the line impedance has a significant impact on the harmonic currents generated by the diode rectifier as shown in [Grötzbach et al. 1995] [Rice 1994] [Kelley, Yadusky 1992]. A large impedance results in less harmonic current and a small impedance results in larger harmonic currents. Having this in mind, the impedance has a positive effect when calculating harmonic current distortion (resulting in low harmonic current distortion) and negative effect when calculating harmonic voltage distortion (resulting in high harmonic voltage distortion).

There are other factors too complicating the prediction or calculation of harmonic distortion in general: The harmonic current distortion of the diode rectifier may be depending on voltage unbalance [Ray et al. 1988] and pre-distorted grid. Also, the phase-angle of the individual harmonic currents of different rectifier types may differ widely which means that harmonic currents cannot be summed arithmetically [Fender, Dorner 1995].

1.2 What Are the Effects?

The harmonic current and harmonic voltage have different effects on the power system, power system components and on other connected equipment. Therefore, it is important to separate harmonic current and harmonic voltage distortion when discussing the effects of harmonics.

The total harmonic current distortion (THD_i) contributes to the rms current (I_{rms}) as shown in equation 1.2:

$$I_{rms} = I_1 \cdot \sqrt{1 + THD_i^2} \tag{1.2}$$

The increased rms current increases the losses in the power system and series connected power system components, such as transformers and wiring. Also parallel-connected equipment, such as power-factor correction capacitors, can be affected if they provide a low impedance path for the harmonic currents. The increased losses result in increased heating that eventually leads to decreased lifetime or damaging of the affected components.

A high level of harmonic voltage distortion changes the sinusoidal nature of the voltage waveform and thereby also the peak values and zero-crossing characteristics. With some equipment this results in mal-functioning. Also harmonic voltage can generate harmonic currents or harmonic fluxes that again can damage or overheat connected equipment.

A hazardous level of harmonic current or harmonic voltage distortion may affect some equipment as discussed in the following.

Failures have been reported in **transformers** loaded less than the nameplate kVA [Pierce 1996]. The reason for this are the harmonic currents that result in increased heating. Foremost, because the higher frequency components increase the eddy current losses, but also because of the harmonic currents increase the rms current as shown in equation 1.2. The increased rms current results in increased conduction losses. Therefore, a transformer

loaded with some non-linear load must be de-rated [Dugan et al 1996]. The de-rating factor is determined in the north American standard ANSI/IEEE C57.110-1986. The harmonic voltage can also contribute to increased losses, due to increased core losses and harmonic fluxes.

Due to the higher rms current **cables** must also be de-rated and also because of increased losses due to skin- and proximity effects. This is especially true for larger conductors. [IEEE 519]

Another major problem with cables and wiring in general is overheating of the neutral conductor because of the **triplen harmonics** [Lai, Key 1996]. Triplen harmonics are zero-sequence currents, and these sum up in the neutral conductor even under balanced load conditions. However, it is only the single-phase diode rectifier (connected between phase and neutral) that produces triplen zero-sequence harmonics.

Two concerns arise from the use of **capacitors**. One is the possibility of resonance. Resonance imposes harmonic voltages and currents that are considerably higher than without resonance [IEEE 519]. Another problem is overheating of the capacitor. The capacitor acts as a sink for higher frequency harmonics. This increases the heating and dielectrical stress and thereby to reduced lifetime expectations [IEEE 519]. Both harmonic currents and voltages contribute to malfunctioning of capacitors.

Harmonic voltages induce harmonic flux components in **electric machines**. These harmonic fluxes do not contribute significantly to the produced torque and are therefore seldom harmful to the load. However, the harmonic fluxes induce harmonic currents into the rotor, which increases the losses. According to [Dugan et al. 1996] excessive heating problems begin when the voltage distortion reaches $THD_v = 8 – 10$ %.

In general **Electronic equipment** connected to the power system can be divided into two major groups. One group which is insensitive to harmonics (ironically, these are normally powered by the diode rectifier) and another group that is more sensitive to harmonics. The group sensitive to harmonics has normally some special line measuring devices, e.g. zero crossing detection, which makes these devices sensitive to the harmonic voltage distortion. This is especially true when thyristor-controlled rectifier cause the harmonic voltage distortion (notches).

It is important to note that harmonics *can* cause mal-functioning or severe damage on the mentioned equipment, but the subject to discuss is rather: at which level are these problems arising. Unfortunately, this is often neglected when discussing harmonics. Similar to the Radio Frequency Interference (RFI) problem one can discuss whether the problem comes from the emission of harmonics or if some equipment is not immune enough to withstand harmonics.

1.3 What Are the Solutions?

For the single-phase rectifier, which is responsible for the major part of the harmonic distortion in today's power system, there exist several useful rectifier topologies. These rectifiers have been developed through decades and, driven by strict standards for

especially low power single-phase rectifiers, are now becoming standards in most single-phase rectifier applications. However, it may take decades before the effect of these new utility friendly rectifiers is measurable on the power system.

The single-phase diode rectifier followed by a dc-dc converter (Figure 1-4a) is probably the most used power-factor-correction (PFC) method. The dc-dc converter following the diode rectifier can be as various as boost (Figure 1-4b), buck, buck-boost, and others depending on the application. Furthermore, in the recent years the focus has been on zero current switching (ZCS) and zero voltage switching (ZVS) of the used dc-dc converters, in order to reduce the power losses.

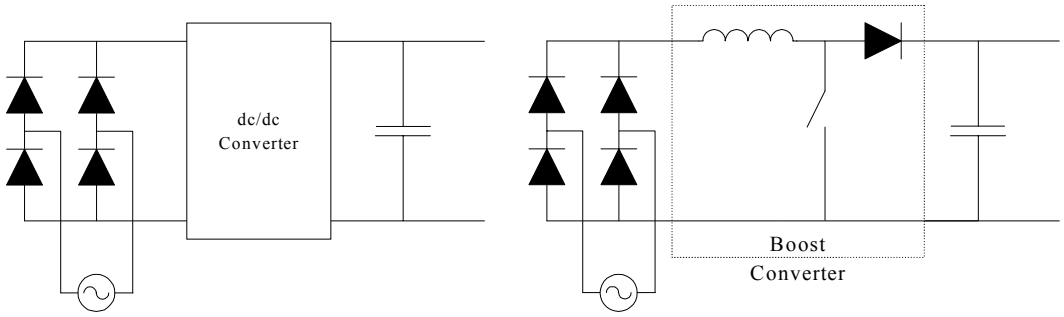


Figure 1-4: (a) Single-phase diode rectifier followed by a dc-dc converter. (b) Single-phase diode rectifier followed by a boost-converter.

The amount of papers concerning different topologies and their control is tremendous and describing all of them is out of the scope of this introduction. [Salmon 1993] and [Sebastian et al. 1994] gives a State-of-the-Art both for the different topologies and for some basic control strategies. Also Appendix C gives a brief introduction to the basic control strategies for the single-phase boost rectifier.

Because of the higher power level, the popular topologies from the single-phase diode rectifier cannot easily be transferred to the three-phase diode rectifier (see also Appendix C). It is therefore significantly more complicated to point-out specific rectifier topologies for three-phase applications.

In the last 5 years or so the interest in the three-phase rectifier has increased. Several articles, that discuses harmonic reduction technique for three-phase diode rectifiers, focus on ASD's that normally use three-phase diode rectifiers to interface the utility grid. The ASD load is believed to increase significantly in the future [Mansoor 1999] and several three-phase rectifier topologies exist, such as those discussed in [Domijan, Embriz-Santander 1992], [Kolar, Ertl 1999] and [Rastrogi et al. 1994]. However, pointing out *the* three-phase rectifier following the three-phase diode rectifier is unfortunately not yet possible.

Interestingly, most papers concerning harmonic distortion of ASD's are focusing on new rectifier topologies, and only few papers are considering using the diode rectifier and reducing the harmonic distortion on a system level. The active filter, however, is an exception and several papers are dealing with improving the power quality in general

including reducing the harmonic distortion. An extensive review can be found in [Akagi 1994] and [Akagi 1996].

1.4 Objective and Scope of the Present Thesis

The main intention of this thesis is to provide models and tools that allow easy prediction of the harmonic distortion of ASD's in a given system and to find reasonable (economical) solutions if the harmonic distortion is exceeding acceptable levels. Based on this and the discussion above, four areas are identified that needs closer investigations.

The effects of harmonics are quite well understood and they are covered in most textbooks treating power quality related problems in general. At which level these effects arise, however, is not very clear. Therefore, some harmonic related standards, guidelines and recommendations are reviewed in this thesis. Even though these standards do not give a definition of at which level harmonic related problems arise, these define which level of harmonic distortion is regarded as acceptable.

The diode rectifier is a simple topology. However, as discussed above the harmonic current of the diode rectifier are not easily calculated. To determine if the acceptable level of harmonic distortion generated by the diode rectifier is exceeded in a given application, useful models for both the diode rectifier and the power system needs to be developed.

In some applications the diode rectifier may not comply with relevant harmonic limiting standards or an acceptable limit of the harmonic distortion may be exceeded with the diode rectifier. Therefore, some alternative rectifier topologies to the diode rectifier needs to be identified and investigated. As discussed above, excellent alternatives exist for the single-phase diode rectifier. Therefore, the focus of this thesis is on three-phase diode rectifiers especially for ASD's. Also topologies that reduce the harmonic distortion on a system level are considered.

Finally, once the different topologies are analyzed, the costs of theses topologies need to be estimated so that a cost-optimal topology can be found in a given ASD application.

The final objectives of this thesis that can be summarized to:

- Determine an acceptable level of harmonic distortion
- Develop models for the diode rectifier and the power system to predict/calculate the harmonic current and voltage distortion in a given application
- Analyze alternative rectifier topologies to the three-phase diode rectifier for ASD's including system-level topologies
- Point out the cost optimal three-phase rectifier topology in a given application

1.4.1 Limitations of the thesis

The analysis performed in this thesis are made under the following limitations:

- The frequency range considered for the used calculation models is limited to 50 Hz – 2000 Hz

- Only voltage and current distortion on the low voltage distribution line are analyzed. I.e. where necessary, only simple models for the medium voltage line are considered
- Because of the above mentioned focus on alternative rectifier topologies for ASD's, these are mainly considered. However, this does not exclude that some of the presented topologies are useful for other applications as well
- The rectifier topologies considered should be useful in the medium power range (1 kVA – 500 kVA). This excludes some three-phase rectifier topologies mainly due to low efficiency. These topologies are therefore not covered in this thesis.

1.5 Outline of the Present Thesis

In accordance with the objectives of this thesis the outline is as follows:

Chapter 2: Harmonic Related Standards

In order to determine an acceptable level for harmonic distortion, the most important standards related to harmonic distortion are reviewed in Chapter 2. The international standards IEC 61000-2-2 and IEC 61000-2-4 are defining the level of harmonic voltages where connected equipment still must operate. Both the harmonic limiting European standards EN 61000-3-2 and EN 61000-3-12 and the North American recommended practice for control of harmonic distortion IEEE 519-1992 are reviewed.

Chapter 3: Harmonic Voltage Distortion

The basic theory for calculation of the voltage distortion is reviewed in this chapter. It is pointed out that exact calculation of the voltage distortion takes the harmonic background voltage distortion into account. Also harmonic impedance models are discussed and measurements are validating the models.

Chapter 4: Harmonic Current Distortion of the Diode Rectifier

In Chapter 4 the harmonic current distortion of the diode rectifier is discussed. Simple empirical models as well as analytical models are presented for the single-phase and three-phase diode rectifier. The importance of the phase-angle of the harmonic currents with respect to the fundamental voltage is pointed out. SABER simulations are made to determine the behavior of the diode rectifier at pre-distorted voltage. Furthermore, experimental measurements are made on a three-phase diode rectifier to verify the developed models.

Chapter 5: High Power Factor Three-Phase Rectifiers

Different high power factor three-phase rectifiers are presented in this chapter. A design procedure for dc-coils and dc-link capacitor of the three-phase diode rectifier to comply with EN 61000-3-12 is presented. The often-used 12-pulse topology in ASD's is also discussed. Furthermore, simulations and experimental results of the active rectifier are presented. Finally, the third harmonic injection scheme is analyzed and a new integrated single-switch approach is presented based on this method.

Chapter 6: System Level Harmonic Reduction Techniques

Chapter 6 presents different system level harmonic reduction techniques. The harmonic cancellation by mixing single- and three-phase diode rectifier is analyzed and a quasi 12-

pulse rectifier topology is presented. Both simulations and experimental results are shown. Finally, advantages and disadvantages of the passive and the active filters are discussed.

Chapter 7: Requirement Based Cost-Optimal Rectifier Topology
In Chapter 7 a cost/benefit analysis for ASD rectifiers is made. The estimated price of the different topologies is compared to the estimated performance of these topologies. Also a step-by-step approach is proposed to determine the cost-optimal rectifier topology in a given application.

Chapter 8: Conclusion
Finally, in Chapter 8 the most important conclusion drawn and the new results obtained in this thesis are summarized.

Appendix A: Measurements at Kyndby
A report of some measurements series made on a medium voltage grid laboratory is found In Appendix A.

Appendix B: Hc and THD_i Values for the Diode Rectifier
In Appendix B some harmonic constant and total harmonic distortion figures for the single- and three-phase diode rectifier are shown.

Appendix C: Single-Switch Boost Rectifier
Appendix C discusses the single-switch boost rectifier.

Appendix D: Publications
Finally, in appendix D some selected publications made during the project period are listed.

2. Harmonic Related Standards

As discussed in the introduction severe harmonic current and voltage distortion may damage various equipments. However, a level of harmonic distortion where these problems occur is not clearly defined. Nevertheless, several harmonic related standards and recommendations exist where limits to the current distortion of apparatus and limits to the system voltage distortion are set.

The two international standards IEC 61000-2-2 and IEC 61000-2-4 are describing the allowable level of harmonic voltage distortion in different systems. The IEC 61000-2-2 applies to the public supply network, whereas the IEC 61000-2-4 applies to industrial plants. These standards are not a definition of which level of harmonic distortion damages some equipment but rather a definition of up to which level there are no problems with harmonic distortion. Basically, it is expected that equipment connected to the described systems work properly up to the defined voltage distortion levels. These standards are therefore a very good indication of what level of harmonic voltage distortion is acceptable and are therefore summarized in this chapter.

To ensure that the voltage distortion levels in IEC 61000-2-2 are not exceeded two European standards, EN 61000-3-2 and the future EN 61000-3-12, exist that limits the emission of harmonic currents from apparatus connected to the public grid. The EN 61000-3-2 limits the current distortion of equipment connected to the public network with rated input (rms) current of less or equal to 16 A whereas the future EN 61000-3-12 will limit the current distortion of equipment with rated input (rms) current between 16 A and 75 A.

Another important recommendation is the IEEE 519-1992. This recommendation includes both limits to the (power) system voltage distortion and current distortion limits. However, the current limits are defined on a system level and not on apparatus level as the EN 61000-3-2 and EN 61000-3-12. The IEEE 519-1992 is mainly a recommendation for the North American area but is also widely used in Asia.

2.1 IEC 61000-2-2

The section 2 of IEC 61000 part 2 defines the “Compatibility levels for low-frequency conducted disturbance and signaling in public low-voltage power supply systems”. The compatibility levels of IEC 61000-2-2 apply for low voltage ac-distribution systems with a nominal voltage up to 240 V, single-phase or 415 V, three-phase and a nominal frequency of 50 Hz or 60 Hz. [IEC 61000-2-2].

Table 2-1 shows the compatibility level for the low-voltage public power supply system. The THD_v-level equals 8%. (In IEC 61000-2-2 the THD_v is calculated up to the 40^{th} harmonic)

Odd harmonics non-multiple of 3		Odd harmonics multiple of 3		Even harmonics	
Harmonic order h	Harmonic voltage %	Harmonic order h	Harmonic voltage %	Harmonic order h	Harmonic voltage %
5	6	3	5	2	2
7	5	9	1.5	4	1
11	3.5	15	0.3	6	0.5
13	3	21	0.2	8	0.5
17	2	>21	0.2	10	0.5
19	1.5			12	0.2
23	1.5			>12	0.2
25	1.5				
>25	0.2+0.5·25/h				

Table 2-1: Compatibility levels for individual harmonic voltages in low voltage networks.

The IEC 61000-2-2 is in use in Europe today. This means that apparatus specific standards, such as the EN 61800 for ASD's, refer to the IEC 61000-2-2. Therefore, all equipment that is intended for connection to the public low-voltage network in Europe must comply with the above compatibility levels. E.g. ASD's or TV-sets must still operate with a voltage distortion level up to $THD_v = 8\%$. Again, this is not a clear definition of at which level of harmonic distortion one can expect problems with the connected equipment, but rather a clear statement of at which minimum level one can assume that there are no problems arising with harmonics (At least the places where IEC 61000-2-2 apply).

2.2 IEC 61000-2-4

The IEC 61000-2-4 defines the compatibility levels in industrial plants for low-frequency conducted disturbances. The compatibility levels of IEC 61000-2-4 applies for low-voltage and medium-voltage ac-power supply at 50 Hz or 60 Hz. [IEC 61000-2-4]

The IEC 61000-2-4 is divided into three classes:

Class 1: This class applies to protected supplies and has compatibility levels lower than public network levels. It relates to the use of equipment very sensitive to disturbance in the power supply, for instance instrumentation of technological laboratories, some automation and protection equipment, some computers etc.

Class 2: This class applies to PCCs and IPCs in the industrial environment in general. The compatibility levels in this class are identical to those of public networks; therefore, components designed for applications in public networks may be used in this class of industrial environment.

Where: PCC = point of common coupling. The point of coupling at the public supply networks to which the system to be studied is, or is to be, connected. Other systems (consumers) may also be connected to or near this

point. IPC = in plant point of common coupling. The point of coupling inside the system or installation to be studied.

Class 3: Class 3 applies only to IPCs in industrial environments. It has higher compatibility levels than those of class 2 for some disturbance phenomena. For instance, this class should be considered when any of the following conditions are met:

- A major part of the load is fed through converters;
- Welding machines are present;
- Large motors are frequently started;
- Loads vary rapidly.

Table 2-2, Table 2-3, Table 2-4 and Table 2-5 shows the compatibility levels in industrial plants. (In IEC 61000-2-4 the THD_v is calculated up to the 40^{th} harmonic)

	Class 1	Class 2	Class 3
THD_v	5%	8%	10%

Table 2-2: Compatibility level for the total harmonic voltage distortion, THD_v.

Order h	Class 1 U_h %	Class 2 U_h %	Class 3 U_h %
5	3	6	8
7	3	5	7
11	3	3.5	5
13	3	3	4.5
17	2	2	4
19	1.5	1.5	4
23	1.5	1.5	3.5
25	1.5	1.5	3.5
>25	0.2+12.5/h	0.2+12.5/h	$5 \cdot \sqrt{}(11/h)$

Table 2-3: Compatibility level for harmonics – Harmonic voltage components (excluding multiples of 3, odd order).

Order h	Class 1 U_h %	Class 2 U_h %	Class 3 U_h %
3	3	5	6
9	1.5	1.5	2.5
15	0.3	0.3	2
21	0.2	0.2	1.75
>21	0.2	0.2	1

Table 2-4: Compatibility level for harmonics – Harmonic voltage components (multiples of 3, odd order).

Order h	Class 1 U_h %	Class 2 U_h %	Class 3 U_h %
2	2	2	4
4	1	1	1.5
6	0.5	0.5	1
8	0.5	0.5	1
10	0.5	0.5	1
>10	0.2	0.2	1

Table 2-5: Compatibility level for harmonics – Harmonic voltage components (even order).

The IEC 61000-2-4 is also used in Europe today and equipment used in industrial or non-public networks must still operate with the defined harmonic levels. Not surprisingly, sensitive equipment as defined in Class 1 must comply with a lower compatibility level than those defined in Class 2 and IEC 61000-2-2. But it should be noted that Class 1 applies only to protected supplies. This normally involves UPS systems, filters or surge suppressors. Again, the defined levels can be used as a reference for up to which level of harmonic distortion one can expect no problems.

2.3 EN 61000-3-2

The EN 61000-3-2 is made to ensure that the harmonic voltage distortion levels of IEC 61000-2-2 are not exceeded in the public power supply. Thus the EN 61000-3-2 limits the current distortion of equipment connected to the public network with rated input (rms) current ≤ 16 [A]. The EN 61000-3-2 will take effect in Europe the 1st January 2001. However, for professional equipment (e.g. ASD's) the EN 61000-3-2 will only take place for a total input power below 1 kW. I.e. there are not harmonic current emission limits to professional equipment with an input power of above 1 kW. [EN 61000-3-2]

The EN 61000-3-2 is divided into four classes:

- Class A: Balanced three-phase equipment, Household equipment expect those specified in Class D, dimming devices for lightning, Audio equipment and all other equipment not stated in Classes B, C and D.
- Class B: Portable tools.
- Class C: Lighting equipment excluding dimming devices.
- Class D: Personal computers, monitors, and television having an input power of less or equal to 600 W.

The current limits for class A, C and D are given in Table 2-6, Table 2-7 and Table 2-8 respectively. For class B equipment the maximum permissible values are given in Table 2-6 multiplied by a factor of 1.5. (In EN 61000-3-2 the THD_i is calculated up to the 40th harmonic.)

Harmonic number h	Maximum permissible harmonic current [A]
odd harmonics	
3	2.3
5	1.14
7	0.77
9	0.4
11	0.33
13	0.21
$15 \le h \le 39$	$0.15 \cdot 15/h$
even harmonics	
2	1.08
4	0.43
6	0.3
$8 \le h \le 40$	$0.23 \cdot 8/h$

Table 2-6: Harmonic current limits for class A equipment.

Harmonic number h	Maximum permissible harmonic current %
2	2
3	$30 \cdot \lambda$
5	10
7	7
9	5
$11 \le h \le 39$ (odd harmonics only)	3
λ is the circuit power factor	

Table 2-7: Harmonic current limits for class C equipment.

Harmonic number h	Maximum permissible harmonic current pr. watt [mA/W]	Maximum permissible harmonic current [A]
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
$15 \le h \le 39$	3.85/h	$0.15 \cdot 15/h$

Table 2-8: Harmonic current limits for class D equipment.

Equipment considered Class D equipment (having an input power of less or equal to 600 W) the harmonic emission limit is a function of the input power. This means that e.g. the 5^{th} harmonic current is limited to 44% (assuming single-phase equipment and 230 V). This is somewhat different for Class A equipment. Here the limit is an absolute current. This results in that for single-phase equipment with an input power of less than 600 W the limits are less stringent in Class A than Class D. And above 600W the limits are more stringent.

Assuming 16A line current for a diode rectifier the relative emission of the 5th harmonic current is limited to 7.125%.

Even though the EN 61000-3-2 only states harmonic current emission limits of equipment, the main objective is to keep the voltage distortion below the levels defined in IEC 61000-2-2. The current harmonic emission levels are theoretically calculated by assuming worst-case impedance with respect to the voltage distortion of levels set in IEC 61000-2-2. The impedance used in these calculations has been and is still widely discussed by the committee members and a total revision of the EN 61000-3-2 is therefore expected in the future.

Also it is important to remember that the EN 61000-3-2 only applies to equipment that is intended for connection to the low-voltage public power supply. It does not apply to a private (industrial) low-voltage network interfacing with the public supply at the medium or high voltage network

2.4 Draft Proposal to EN 61000-3-12 Issue 2000-08-04

The draft proposal of the future EN 61000-3-12 (issue 2000-08-04) limits the current distortion of equipment with input current 16 A - 75 A connected to the public network. The EN 61000-3-12 is a future European standard and is the follow-up of the technical report IEC 61000-3-4. It is not clear yet when the EN 61000-3-12 will take effect. I.e. there are not harmonic current emission limits to equipment with an input current of 16 A - 75 A. [EN 61000-3-12]

The Draft EN 61000-3-12 is divided into three stages.

Stage 1: Simplified connection:
Equipment complying with stage 1 for the emission of harmonic currents can be connected to the supply system without a need to contact the supply authority. The harmonic current limits for stage 1 are listed in Table 2-9. (In EN 61000-3-12 the THD_i is calculated up to the 40th harmonic)

Minimal R_{sce}	Admissible individual harmonic current I_h / I_1 %						Admissible harmonic current distortion factors %	
	I_3	I_5	I_7	I_9	I_{11}	I_{13}	THD_i	PWHD
33	21.6	10.7	7.2	3.8	3.1	2	21	21

Table 2-9: Stage 1 harmonic current limits for simplified connection of equipment.

Stage 1 is based on a worst-case assumption, i.e. a weak grid with a short circuit ratio R_{sce} of 33. The resulting voltage distortion of non-linear equipment is expected to be higher on a weak grid because of the high impedance. Therefore the limits are more stringent to the harmonic current emission on a weak grid. This means equipment complying with the limits stated in stage 1 can be connected at any point of the supply system, providing $R_{sce} \geq 33$.

Stage 2: Connection based on network and equipment data:
For equipment not complying with the emission limits of stage 1, higher values are allowed provided the short-circuit ratio R_{sce} is > 33. For equipment complying with stage 2, the manufacture must state in the instruction manual that the equipment is complying with EN 61000-3-12, provided the necessary minimum short circuit ratio.

The harmonic current limits for single-phase, interphase and unbalanced three-phase equipment is shown in Table 2-10.

Minimal R_{sce}	Admissible individual harmonic current I_h / I_1 %						Admissible harmonic current distortion factors %	
	I_3	I_5	I_7	I_9	I_{11}	I_{13}	THD_i	PWHD
33	21.6	10.7	7.2	3.8	3.1	2	21	21
66	24	13	8	5	4	3	23	23
120	27	15	10	6	5	4	28	28
250	35	20	13	9	8	6	38	38
≥350	41	24	15	12	10	8	46	46

Table 2-10: Harmonic current limits for single-phase, interphase and unbalanced three-phase equipment.

The harmonic current limits for balanced three-phase equipment is shown in Table 2-11.

Minimal R_{sce}	Admissible individual harmonic current I_h / I_1 %				Admissible harmonic current distortion factors %	
	I_5	I_7	I_{11}	I_{13}	THD_i	PWHD
33	10.7	7.2	3.1	2	13	22
66	14	9	5	3	16	25
120	19	12	7	4	22	28
250	31	18	12	7	37	38
≥350	40	25	15	10	48	45

Table 2-11: Harmonic current limits for balanced three-phase equipment.

The harmonic current limits for balanced three-phase equipment with special phase-angle conditions are as shown in the table below.

Minimal R_{sce}	Admissible individual harmonic current I_h / I_1 %				Admissible harmonic current distortion factors %	
	I_5	I_7	I_{11}	I_{13}	THD_i	PWHD
33	10.7	7.2	3.1	2	12	28
≥120	40	25	15	10	48	45

Table 2-12: Harmonic current limits for balanced three-phase equipment with given phase-angle conditions.

Table 2-12 may be used if one of these following conditions are met:

a) The phase-angle of the 5th harmonic current is in the range of 90º to 150º. (Normally fulfilled with a three-phase diode rectifier including a 3% ac-coil or a 4% dc-coil.)
b) The design of the equipment is such that the phase-angle of the 5th harmonic current has no preferential value over time and can take any value in the whole interval [0º, 360º]. (Normally fulfilled by converters with fully controlled bridges)
c) The 5th and 7th harmonic currents are each less than 5% of the reference fundamental current. (Normally fulfilled by 12-pulse equipment.)

For stage 2 the limits for the harmonic current distortion are based on the short circuit ratio. This means it is necessary to know data of the network and of the equipment in order to calculate the short circuit ratio. The limit for each harmonic current increases as the short circuit ratio increases because the resulting voltage distortion is expected to decrease as the impedance decreases. Therefore in Table 2-10 and Table 2-11 relatively high limits are found at a short circuit ratio of ≥350.

However in Table 2-12 these relatively high limits are found at a short circuit ratio of ≥120. The reason for this is that the voltage distortion generated by the equipment mentioned in a) is expected to be in counterphase with the existing voltage distortion of the power system (mainly caused by single-phase diode rectifiers). This issue is more detailed discussed in Chapter 3, Chapter 4 and Chapter 6. The equipment mentioned in b) and c) are believed to have a small impact on the power system as well and are therefore included.

Stage 3: Connection based on consumer's agreed power:
For equipment not complying with the limits stated in stage 1 nor stage 2, stage 3 applies. For stage 3 the supply authorities may accept the connection of the equipment on the basis of the predicted effects of such a connection being within the local supply requirements.

Equipment considered stage 3, the manufacturer must state in the instruction manual and in a document available to a prospective user before purchasing the equipment, that it is necessary for the user to consult the power supply authority for connection of the equipment to the public low-voltage supply. Furthermore, the manufacturer must provide the individual measured harmonics, THD_i and PWHD values.

In stage 3 there are no limits. If the supply authorities agree, this makes is possible to connect equipment that cannot comply with stage 1 or stage 2. However, the harmonic impact to the power supply must be predicted. Therefore in the future there might be an increased need for calculation tools and models to predict the impact of harmonic currents to the system.

As for the EN 61000-3-2 the EN 61000-3-12 states limits to the harmonic current emission of equipment. However, even though the EN 61000-3-12 only states harmonic current emission limits, the main objective is still to keep the voltage distortion below the levels defined in IEC 61000-2-2. Compared to EN 61000-3-2 the EN61000-3-12 takes different impedance levels into account.

Again, it is important to note that the EN 61000-3-12 only applies to equipment that is intended for connection to the low-voltage public power supply. It does not apply to a

private (industrial) low-voltage network interfacing with the public supply at the medium or high voltage network

2.5 IEEE 519-1992

The IEEE 519-1992 "IEEE Recommended Practice and Requirements for Harmonic Control in Electrical Power Systems" [IEEE-519] focuses on the voltage distortion at the point of common coupling (PCC). The objective of this standard is to limit the maximum individual harmonic voltages to 3% and the total harmonic voltage distortion THD_v to 5%. (In IEEE 519-19992 THD_v is calculated up to the 50^{th} harmonic)

To obtain these objectives, the IEEE 519-1992 provides some current distortion limits. These current limits are developed with the following in mind.

1) Limit the harmonic injection from individual customers so that they will not cause unacceptable voltage distortion levels for normal system characteristics.
2) Limit the overall harmonic distortion of the system voltage supplied by the utility.

The current distortion limits developed assume that there will be some diversity between the harmonic currents injected by different customers. This diversity can be in form of different harmonic components being injected, differences in the phase-angle of the individual harmonic currents, or differences in the harmonic injection vs. time profiles. In recognition of this diversity, the current limits are developed so that the maximum individual frequency harmonic voltage caused by a single customer will not exceed the limits in Table 2-13 for systems that can be characterized by the short circuit ratio.

R_{sce} at PCC	Maximum Individual Frequency Voltage Harmonic %
10	2.5-3.0
20	2.0-2.5
50	1.0-1.5
100	0.5-1.0
1000	0.05-0.1

Table 2-13: Basis for current limits of IEEE 519-1992.

The current limits listed in Table 2-14 are applicable to six-pulse rectifiers and general distortion situations for system with voltages below 69 kV. However when phase-shift transformers or converters with pulse numbers (q) higher than six are used the limits for the characteristic harmonic orders are increased by a factor equal to:

$$\sqrt{\frac{q}{6}} \tag{2.1}$$

Provided that the amplitudes of the non-characteristic harmonic orders are less than 25% of the limits specified in the table below (Table 10.3 of [IEEE 519]).

I_{sc} / I_L	<11 [%]	11≤h<17 [%]	17≤h<23 [%]	23≤h<35 [%]	35≤h [%]	TDD [%]
<20	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0
Even harmonic are limited to 25% of the odd harmonic limits above						

Table 2-14: Current distortion limits for voltages below 69 kV

The IEEE 519-1992 is a recommended practice to control the harmonic distortion in an electrical power system hence there are no harmonic current emission limit to equipment. The main objective is to limit the harmonic voltage distortion. Similar to the EN 61000-3-12 stage 2, this results in harmonic current limits depending on the short circuit ratio. However, in the IEEE 519-1992 the harmonic current limits are system limits. To deal with these system harmonic current limits the TDD (Total Demand Distortion) is defined.

The ratio I_{sc} / I_L is the ratio of the short circuit current available and the maximum fundamental load current. It is recommended that the load current I_L is calculated as the average current of the maximum demand for the preceding 12 month.

Also an important aspect of the IEEE 519-1992 is the definition of the PCC. Obviously if one complies with the IEEE 519-1992 can be depending on the choice of the PCC. In general the PCC is defined as the point of the non-linear load and other loads or the point where the consumer meets the utility. For explanation a system as shown in Figure 2-1 is considered.

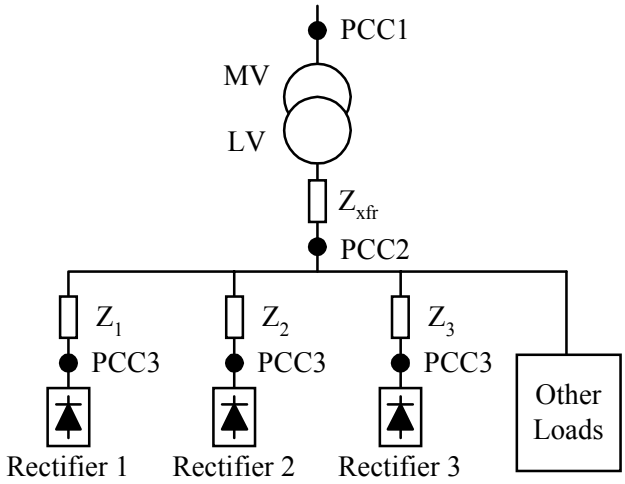


Figure 2-1: Typical industrial distribution system, defining the possible placements of the PCC.

PCC 3 is the point where the non-linear load is connected to the grid. The harmonic distortion at this point only affects the load itself. Therefore, it is not of interest with respect to the IEEE 519-1992. PCC2 is the connection point, which is shared by different loads and maybe by different consumers. The PCC 2 is normally the point of interest and

thereby the PCC at which all harmonic currents and voltages may be measured. Anyway, if only one consumer loads the transformer the PCC1 can be considered to be the PCC.

It should be noted that the IEEE 519-1992 is not a standard, but a recommended practice. Therefore "….., good engineering judgment are required on a case-by-case basis, and this recommendation in no way overrides such judgments" [IEEE 519-1992].

2.6 Conclusion

In the discussion of which level of harmonic distortion is acceptable, the international standards IEC 61000-2-2 and IEC 61000-2-4 play an important role. These two standards influence a significant part of the worldwide market for equipment connected to the grid. Therefore, it is safe to conclude that most equipment eventually (especially equipment produced by international manufacturers) complies with these standards.

The European standards EN 61000-3-2 and the EN 61000-3-12 are defining the current distortion limits for equipment connected to the public supply system. The objective of both standards is to limit the voltage distortion to the level defined in IEC 61000-2-2. Consequently, the harmonic current limits stated are calculated based on a worst-case impedance (EN 61000-3-2) or different impedance scenarios (EN 61000-3-12). However, it is important to note that the focus is on the voltage distortion.

The European standards EN 61000-3-2 and stage 1 in EN 61000-3-12 limits the harmonic distortion of the equipment. In stage 3 and partly in stage 2 of EN 61000-3-12 the focus is moved to the system.

In the IEEE 519-1992 the focus is only on the system. The resulting voltage distortion and harmonic currents are therefore limited at the PCC. Again the objective is to limit the resulting harmonic voltage distortion. The current distortion limits are based on the short circuit ratio and the tolerated voltage distortion. However, the voltage distortion level is somewhat lower in the IEEE 519-1992 as in the IEC 61000-2-2 and IEC 61000-2-4. Interestingly, the stated voltage distortion levels in IEEE 519-1992 are close to those stated in Class 1 of IEC 61000-2-4 which applies for protected power systems. The reason for this may be found in the fact that no standards similar to the IEC 61000-2-2 and IEC 61000-2-4 are found in North America and thus some conservative limits are stated.

It is important to remember that the IEEE 519-1992 is not a standard but only a recommended practice. However, the limits of the IEEE 519-1992 are often specified in new installations of ASD's, even outside North America. Also, it can be expected that some (European) customers of ASD's not connected to the public network will specify that the equipment must respect the limits of the EN 61000-3-12 even-though not limited by this standard.

Based on the presented standards it can be concluded that the harmonic voltage distortion is the most important issue when discussing harmonic distortion in general. Also it is found that a total harmonic voltage distortion level of 5% - 8% and an individual harmonic voltage distortion of 3% - 6% seem to be an acceptable level. On the other hand, acceptable limits for the current distortion are not clearly defined because these are defined with the resulting voltage distortion in mind. The resulting voltage distortion is depending on the

system impedance, thus unambiguous defined current distortion limits valid for all kind of systems is impossible to state if the true objective is to limits the harmonic voltage distortion.

Finally, it can be concluded that there is an increasing need for models and calculation tools to do the required calculations required in IEEE 519-1992 and EN 61000-3-12. In Chapter 3 and Chapter 4 models and easy calculation methods to predict the distortion level in a given system are developed and presented.

3. Harmonic Voltage Distortion

The main purpose of the harmonic limiting standards is to protect the power system from unwanted harmonic voltage distortion. Also parallel-connected equipment (other users) is more likely to be disturbed by voltage distortion (than by current distortion). The harmonic voltage distortion is, therefore, the most important issue when discussing harmonic distortion in general. This chapter discusses the various aspects of calculating the harmonic voltage distortion.

As mentioned in Chapter 1 the harmonic currents are considered flowing from the non-linear load into the source. Because of the impedance between the equipment and the utility source the harmonic current is generating a voltage drop. This harmonic voltage drop is the reason for that the utility voltage becomes distorted. Basically, the individual harmonic voltage of the order h (U_h) equals the product of the harmonic current of the order h (I_h) and the harmonic impedance of the order h (Z_h). If the harmonic impedance and the harmonic currents are known, the harmonic voltages can easily be calculated by equation 3.1.

$$\overrightarrow{U_h} = \overrightarrow{I_h} \cdot \overrightarrow{Z_h} \tag{3.1}$$

This chapter presents a simple method to calculate the total harmonic voltage distortion (THD_v) at the transformer or at any given point where the short circuit power is known. Unfortunately, normally neither the harmonic impedance nor the harmonic currents are easy to determine exactly in a given system. Therefore, the issue of determining the harmonic impedance is discussed in this chapter and it is shown that simple, linear impedance models can be sufficient in most cases. Methods to calculate the harmonic currents of the diode rectifier are presented in Chapter 4.

Another problem in calculating the harmonic voltage distortion is that the harmonic voltages is influenced by resonance and pre-distorted grid. These subjects are considered by a series of measurements and simulations. Finally, the special case where standby generators are used instead of supply transformers is discussed.

3.1 Simple Voltage Distortion Calculations

A typical industrial distribution system with different loads connected, as shown in Figure 3-1, is considered in the following.

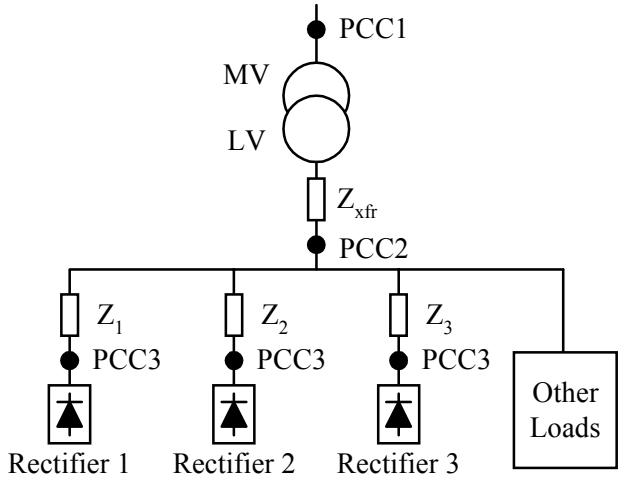


Figure 3-1: Typical industrial distribution line with different loads.

As discussed in Chapter 2 the PCC2 is often defined at the point of common coupling, because this is the point where other loads are affected. For calculation of the voltage distortion at PCC2 the impedance of the MV-line is normally neglected, because the impedance on the LV-line generally is at least 90% of the total impedance and commonly more [Dugan et al.1996]. For calculation of the harmonic voltage distortion at PCC1, knowledge about the MV-line impedance (short circuit power at the PCC1) is required. Capacitive effects are also frequently neglected in order to simplify the calculations. Therefore, it is possible to calculate the voltage distortion at the transformer (PCC2) only knowing the short circuit impedance of the transformer and the harmonic currents. It is important to note, that the transformer impedance is mainly inductive so that equation 3.1 can be rewritten to: (For more detailed information about the harmonic impedance see section 3.3.)

$$\overrightarrow{U_h} = \overrightarrow{I_h} \cdot h\overrightarrow{X_{xfr,1}} \tag{3.2}$$

In a system where more rectifiers are present, as in Figure 3-1, it is convenient to reduce the system under investigation as shown in Figure 3-2. Here the shown rectifier represents the sum of all non-linear loads. I.e. the individual harmonic currents of the order h are summed into one harmonic current of the order h, which is represented by one rectifier. Now the individual harmonic voltages can be calculated by equation 3.2.

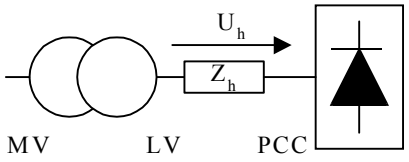


Figure 3-2: Reduced system under consideration. The total rectifier load is summed to one virtual rectifier load.

As shown in Chapter 2 the THD_v is a key index for specifying the level of harmonic distortion. Often the THD_v is the only indication used to comply with some standards such as the IEEE 519-1992. This simplifies the calculations significantly as shown in the following.

Remembering that the voltage THD_v is defined as:

$$THD_v = \sqrt{\sum_{h=2}^{\infty}\left(\frac{U_h}{U_1}\right)^2} \cdot 100\% \tag{3.3}$$

The harmonic voltage U_h is depending of the harmonic currents and the harmonic impedance. Still assuming that the impedance is purely inductive equation 3.3 can be rewritten as:

$$THD_v = \sqrt{\sum_{h=2}^{\infty}\left(\frac{hX_1 I_h}{U_1}\right)^2} \cdot 100\% = \frac{1}{I_{sc}}\sqrt{\sum_{h=2}^{\infty}(hI_h)^2} \cdot 100\% \tag{3.4}$$

For calculation of the total harmonic voltage distortion it is convenient to define the so-called harmonic constant Hc [Paice 1996]:

$$Hc = \sqrt{\sum_{h=2}^{\infty}\left(h\frac{I_h}{I_1}\right)^2} \cdot 100\% \tag{3.5}$$

The definition of Hc reminds somewhat of the definition of the THD_i. But in the Hc definition the harmonic currents are weighted by its order. The harmonic constant relates to the THD_v like:

$$THD_v = Hc \cdot \frac{I_1}{I_{sc}} = Hc \cdot \frac{S_1}{S_{sc}} \tag{3.6}$$

The total harmonic voltage distortion can now be calculated by the ratio of the fundamental apparent load power to the system short circuit power multiplied by Hc. Table 3-1 shows some typical values for Hc for different rectifier types. For more detailed information about the Hc values see Chapter 4.2 for the diode rectifier and Chapter 5 for alternative three rectifier topologies.

Rectifier type	Hc [%]
Basic 6-pulse rectifier	250 – 1000
6-pulse rectifier with ac or dc reactors	150 – 400
12-pulse rectifier	125 – 175

Table 3-1: Hc values for different rectifier types.

3.1.1 Calculation example

To illustrate the simplicity of the above-mentioned calculation method an example is shown here. A system where a 6-pulse non-linear load of 300 kW is connected to a 1 MVA transformer is considered. The non-linear load is a basic 6-pulse rectifier with built-in dc-link inductance. Because the displacement power factor of a diode rectifier is close to one the fundamental apparent power $S_1 \approx 300$ kVA. The Hc value is estimated to be 250% (see also Chapter 4.2). To be sure that the system complies with IEEE-519-1992 it is necessary to determine the resulting voltage distortion at the PCC. (In this case the PCC is the secondary side of the transformer.) The transformer short circuit impedance e_x equals 5%. Neglecting the MV-line impedance, the short circuit power on the secondary side of the

transformer equals 20 MVA. The resulting voltage distortion can now be calculated by the use of equation 3.6.

$$THD_v = Hc \cdot \frac{S_1}{S_{sc}} = 250 \cdot \frac{300\ KVA}{20000\ KVA} = 3.75\% \qquad (3.7)$$

For comparison the same system is simulated in the numeric circuit-based simulator SABER and the resulting voltage distortion is calculated to 3.85%. The difference of 0.1% is due to that the value of Hc = 250% is an estimate, while the true Hc value in this particular system determined by SABER equals 257%. However, it is shown that with this simple calculation method it is possible to estimate if the system complies with IEEE 519-1992 by means of very simple calculations.

3.2 Background Voltage Distortion

The calculation of the harmonic voltage distortion is complicated by the fact that the voltage on the LV distribution line in most cases is distorted even at no load. This is due to the background distortion on the medium voltage (MV) and high voltage (HV) line. Ref. [Kaendler 1995] and [Gretsch, Gunselmann 1991] have pointed out that the harmonic current distortion in the LV distribution system is caused by a large number of switch mode power supplies used in PC's, television sets, VCRs and stereos. These current distortions add up in the MV and HV networks. This means that the large number of small single-phase diode rectifiers is the main cause for the harmonic background voltage distortion. The resulting voltage with this kind of load is shown in Figure 3-3 and can be seen/measured almost everywhere across Europe. The shown voltage is actually measured in the laboratory of Danfoss Drives A/S on a Sunday, i.e. the supply transformer is (almost) unloaded. As seen the dominant harmonic voltage is the 5th and partly the 7th harmonic.

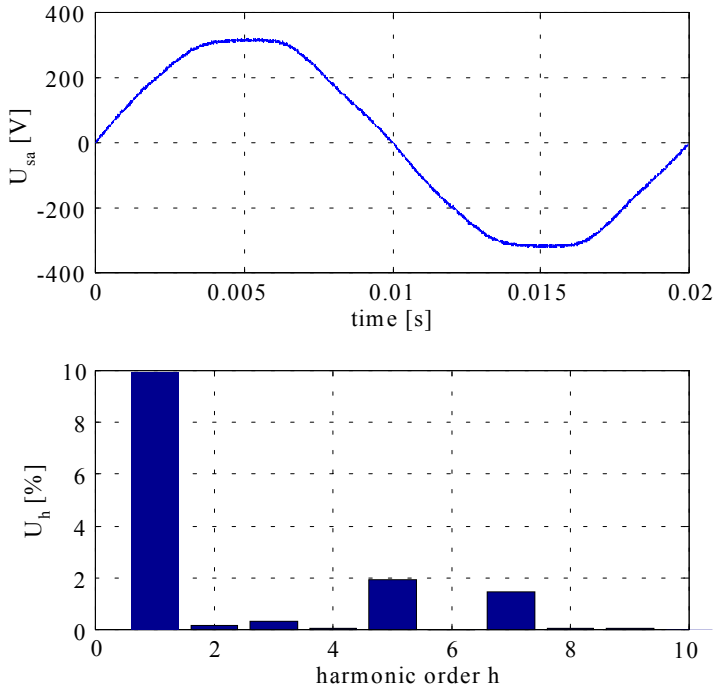


Figure 3-3: Measured line-neutral voltage and the Fourier spectrum. Typical distortion on the LV-distribution line.

To give another example of the background voltage distortion a measurement on a MV-line is done. These measurements are shown in Figure 3-4 and Figure 3-5. The voltages are measured at the secondary side of a 50/10 kV transformer. The 10 kV distribution line is supplying 16 MV/LV substations where three substations are supplying industry, eight substations are supplying domestic area and five substations are supplying miscellaneous. As expected the dominant harmonic voltage is the 5th harmonic. However, the 5th harmonic current is below 1% when the voltages were measured. This means that the 5th harmonic voltage originates from the 50 kV line and thereby conforming that the background distortion originates from the MV and HV line.

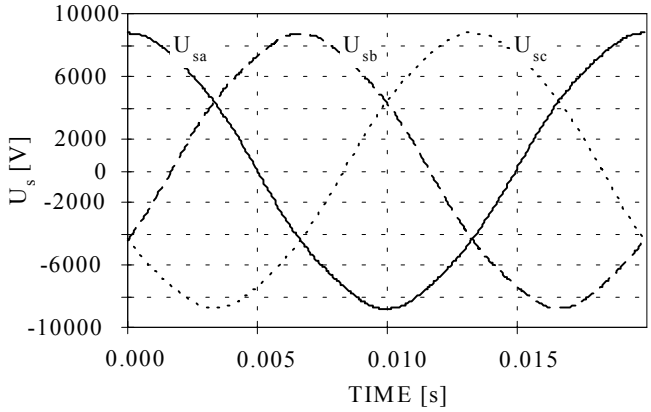


Figure 3-4: Measured line-neutral voltage on a 10 kV MV-distribution line.

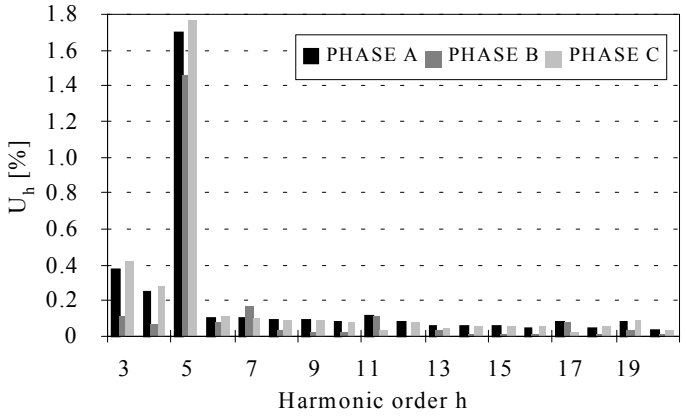


Figure 3-5: Harmonic analysis of the measured voltages of a10 kV distribution line.

If applying non-linear load on the secondary side of the supply transformer then the resulting harmonic voltage distortion measured at the transformer secondary side equals the complex (geometrical) sum of the background voltage distortion and the load distortion. This is illustrated in Figure 3-6 and equation 3.8.

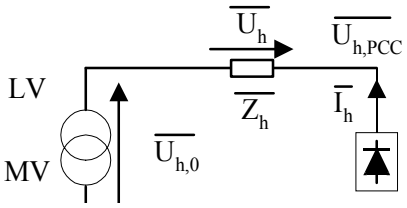


Figure 3-6: Harmonic voltage on the PCC as a sum of voltage drop at the transformer and background distortion

$$\overrightarrow{U_{h,PCC}} = \overrightarrow{U_{h,0}} + \overrightarrow{U_h} = \overrightarrow{U_{h,0}} + \overrightarrow{I_h} \cdot \overrightarrow{Z_h} \tag{3.8}$$

Basically, this means that phase-angle of the background distortion must be known in order to calculate the resulting harmonic distortion.

To illustrate the impact of the background distortion to the simple calculations shown in section 3.1 a simulation example is shown here. A DYn5 coupled 10/04 kV 800 kVA distribution transformer is simulated. The MV side is assumed distorted with the amplitude and phase-angle of 5th harmonic voltage of the measured MV-line voltages of Figure 3-4. The transformer is loaded with a three-phase diode rectifier with a 3% dc-link inductance and varying nominal load from 0 to 650 kW. The three-phase rectifier is located near to the transformer. This is shown in Figure 3-7.

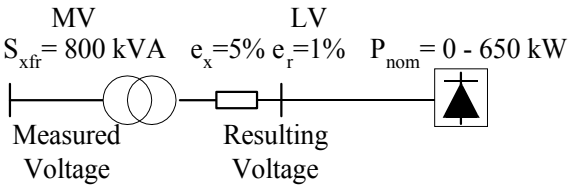


Figure 3-7: Circuit diagram for simulation of rectifier influence on the resulting voltage distortion taking the voltage background distortion into account.

The impact of the rectifier load on the transformer for the 5th harmonic voltage is shown in Figure 3-8.

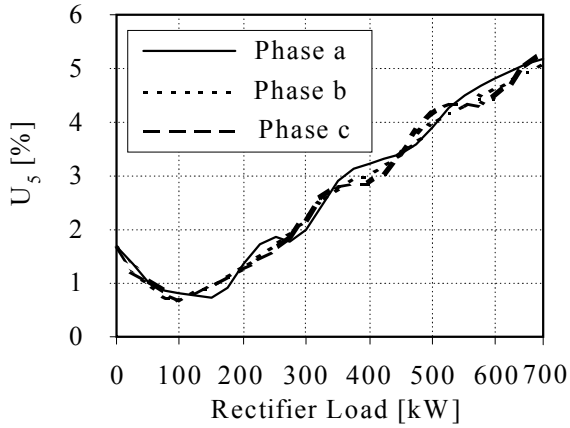


Figure 3-8: The 5th harmonic voltage as a function of the rectifier load at the transformer.

Because differences in the phase-angle of the 5th harmonic background distortion and the generated 5th harmonic voltage distortion an increase in the three-phase non-linear load results actually in a decrease of the resulting 5th harmonic voltage distortion. At approximately 12% of the nominal transformer power the minimum distortion below 1% is reached. At approximately 25% rectifier load of nominal transformer power the resulting 5th harmonic voltage distortion has reached the same level as under no-load conditions (background distortion). Above 25% the resulting 5th harmonic voltage distortion is higher than the background 5th harmonic voltage distortion.

It is important to note that the background voltage distortion is fixed and will not change as a function of the load on the secondary side of the transformer. This is because the background distortion comes from the MV side and thereby has a high short circuit power. Also, one should note that a pre-distorted grid not necessarily comes from background distortion alone. Parallel-connected non-linear loads contribute to the voltage distortion as well. The harmonic voltage distortion generated by the parallel-connected loads might, however, be influenced by other loads, which complicates the calculations.

Before doing some voltage distortion analysis of some non-linear equipment, it is therefore a good idea to measure the pre-existing harmonic voltage distortion and the corresponding phase-angles over a longer period of time before the equipment is connected. The measured values might then be averaged. The theoretical calculated value should then be corrected by the measured pre-existing value (geometrical).

3.3 Harmonic Impedance

Another factor complicating harmonic voltage distortion calculations is the harmonic impedance. Often, only the nominal power, frequency and voltage of the transformer and square diameter of the cable is known, while the necessary parameters such as the short circuit impedance of the transformer or reactance of the cable are not available in a given application. Therefore, some typical transformer data can be found in Table 3-2 and some typical cable data can be found in Table 3-3.

S_{xfr} [kVA]	e_r [%]	e_x [%]
10	3.5	2.5
100	1.3	3
1000	0.9	5
10000	0.5	8
100000	0.35	12

Table 3-2: Typical Transformer data [Vørts 1990].

Cobber cable square [mm^2]	R [Ω/km]	X_1 [Ω/km]
4	4.61	0.104
10	1.83	0.097
25	0.727	0.075
50	0.387	0.072
150	0.124	0.068
Aluminum cable square [mm^2]	R [Ω/km]	X_1 [Ω/km]
4	7.41	0.104
10	3.08	0.097
25	1.20	0.075
50	0.641	0.072
150	0.206	0.068

Table 3-3: Typical cable data [NKT].

In the table above the resistance, inductance and capacitance are considered constant, thus the harmonic impedance is considered linear. However, it is well known that at least the resistance and inductance changes as a function of the frequency due to skin and proximity effect [Hantel & Funk 1987], [Heiß et al. 1994] while the capacitance is considered constant in the frequency range of interest (50 - 2000 Hz). Table 3-4 gives an overview of resistance, inductance and capacitance behavior with increasing frequency depending on their connection.

Series resistance	Series inductance	Series capacitance
Increasing due to skin effect	Decreasing, due to proximity effect	Constant
Parallel Resistance (Equivalent resistance for hysteresis and eddy current losses)	Parallel inductance (Magnetizing inductance)	Parallel Capacitance
Decreasing, due to increased hysteresis and eddy current losses	Constant	Constant

Table 3-4: Behavior of resistance, inductance and capacitance with increasing frequency.

There is no doubt about that the resistance and inductance changes as a function of the frequency. The question however is, how much these changes affect the calculation of the harmonic voltage? Below some simple calculations are compared to measurements to determine if the linear impedance model ($r + j \cdot h \cdot X_1$) is useful for harmonic voltage calculations for both cables and transformer.

3.3.1 Verification of the linear impedance model

The main purpose of exact knowledge of the harmonic impedance is to calculate the harmonic voltage. Therefore, the usefulness of the linear impedance model is evaluated by comparing measured voltages with calculated voltages based on measured currents and the linear impedance model. A detailed description on the measurements can be found in Appendix A. Two sets of measurements are used, one with almost no cable (10 m) and one with a long cable (440 m). The measurement with almost no cable is used to verify the

transformer model, because here the dominating impedance is the transformer impedance while the measurements with the long cable is used to verify the cable model. The measurement system is illustrated in Figure 3-9.

A 200 kVA transformer and a Danfoss frequency converter VLT® 3052 loaded with a motor/generator set-up is used. (The fundamental nominal power of the three-phase diode rectifier equals approximately 50 kVA.) The two combinations of cables are:

1) 10 meter four wire 50 mm^2 Al.
2) 240 meter four wire 50 mm^2 Al. + 200 meter four wire 25 mm^2 Al.

The cable impedance is estimated by the use of Table 3-3 while the transformer nameplate data are known. The impedance of theMV-line is neglected. Thus the fundamental impedance and short circuit power for the 2 combinations, including the impedance of the transformer is estimated to:

1) $Z_1 = 0.01441 + j0.03592 = 0.0387\ \Omega\ \angle 68º$, $S_{sc} = 4.13$ MVA
2) $Z_4 = 0.40184 + j0.06748 = 0.4075\ \Omega\ \angle 9.5º$, $S_{sc} = 0.39$ MVA

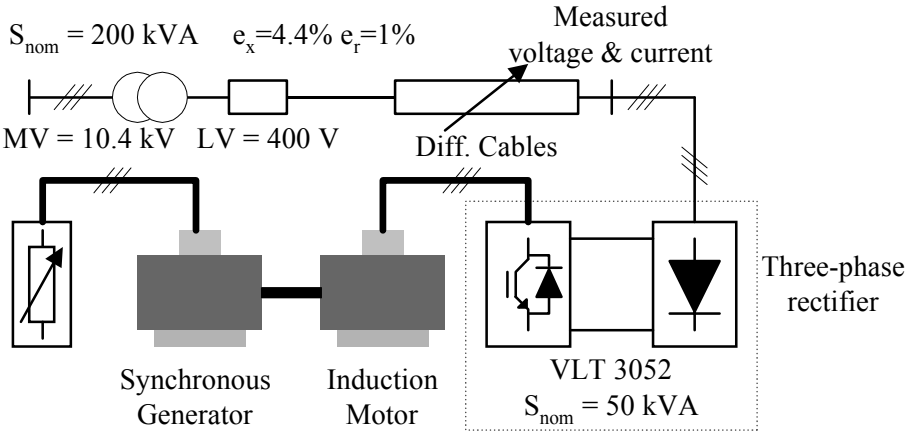


Figure 3-9: A sketch of the system used for measurement series 1

Theoretically, if the harmonic impedance is known exactly, the calculated harmonic voltage matches the measured harmonic voltage. As mentioned in section 3.4 it is important to correct for the background distortion, which in this case is measured at no-load. The measured background distortion is added (geometrical) to the calculated voltage.

In a perfect balanced three-phase system, it is only necessary to calculate for one of the three phases. Of course this saves some calculation time. However, to eliminate calculation error made on the account of unbalance the theory of symmetrical components is used. Equation 3.9 shows the transformation from three-phase currents to positive (I_p), negative (I_n) and zero sequence (I_0) currents.

$$\begin{aligned} I_p &= \tfrac{1}{3}\left(I_a + a\ I_b + a^2 I_c\right) \\ I_n &= \tfrac{1}{3}\left(I_a + a^2 I_b + a\ I_c\right) \\ I_0 &= \tfrac{1}{3}\left(I_a + I_b + I_c\right) \end{aligned} \qquad (3.9)$$

where:

$$a = -0.5 + \tfrac{\sqrt{3}}{2}j$$

The equations to transform back to the three-phase system are:

$$\begin{aligned} I_a &= I_p + I_n + I_0 \\ I_b &= a^2 I_p + a\ I_n + I_0 \\ I_c &= a\ I_p + a^2 I_n + I_0 \end{aligned} \tag{3.10}$$

The zero sequence is not used in the following calculations, because the zero conductor of the cable is unused, hence the zero sequence current is negligible.

Figure 3-10 shows the calculated and the measured harmonic voltage amplitude and the corresponding phase-angles for combination 1). Also the calculated voltage corrected for the pre-measured background distortion is shown. The voltages and currents were measured close to the transformer and the dominating impedance is the transformer impedance. In general the measured harmonic voltages and phase-angles are close to the calculated values and the differences, as shown in Figure 3-11, are less than 0.5 V. The larger differences found at the 31st and 37th harmonic are due to an increased background distortion at these frequencies at the moment of the measurements. This increased background distortion was not measured when the voltage was measured at no-load.

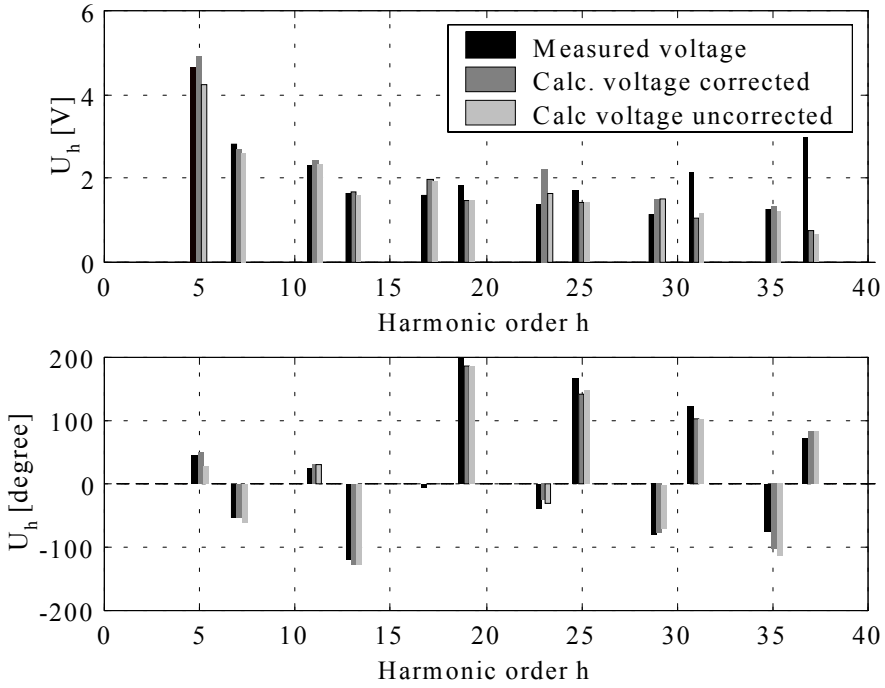


Figure 3-10: Measured and calculated harmonic voltage amplitude and corresponding phase-angle both with and without correcting for the background voltage distortion for combination 1).

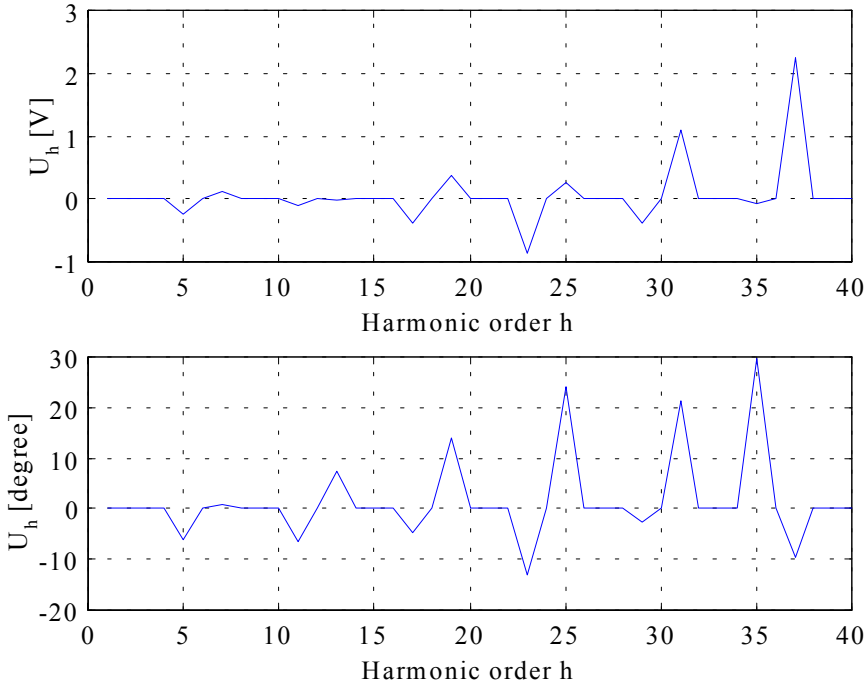


Figure 3-11: Difference between the measured and the corrected calculated harmonic voltage amplitude and phase-angle.

In Figure 3-12 the voltages and currents were measured with a 440 m cable connected to between the transformer and the load. Here, the dominating impedance is the cable impedance, and as shown in Figure 3-12, the measured harmonic voltage amplitude and phase-angles are close to the calculated values.

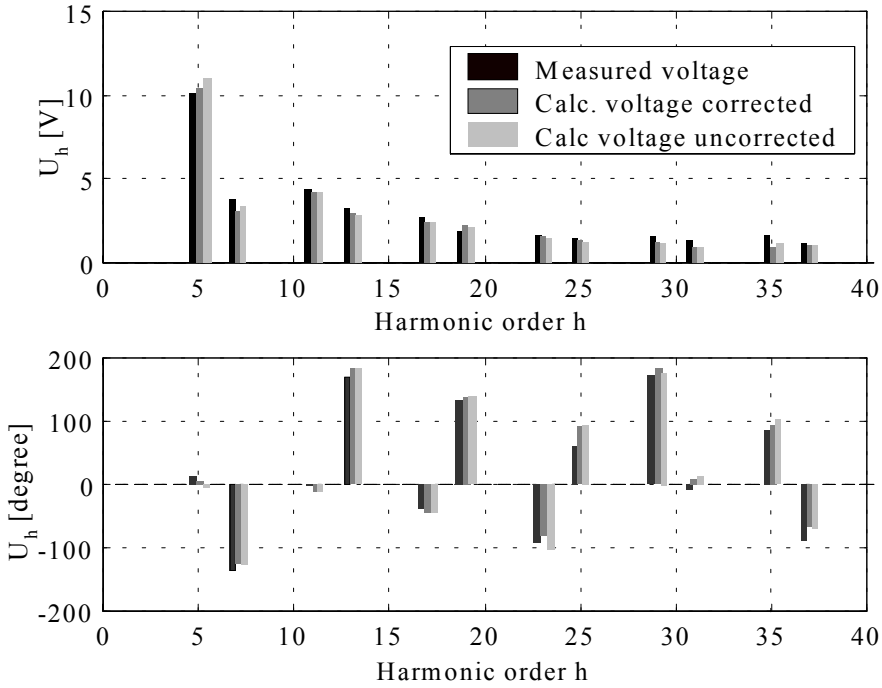


Figure 3-12: Measured and calculated harmonic voltage amplitude and phase both with and without correcting for the background voltage distortion for combination 2).

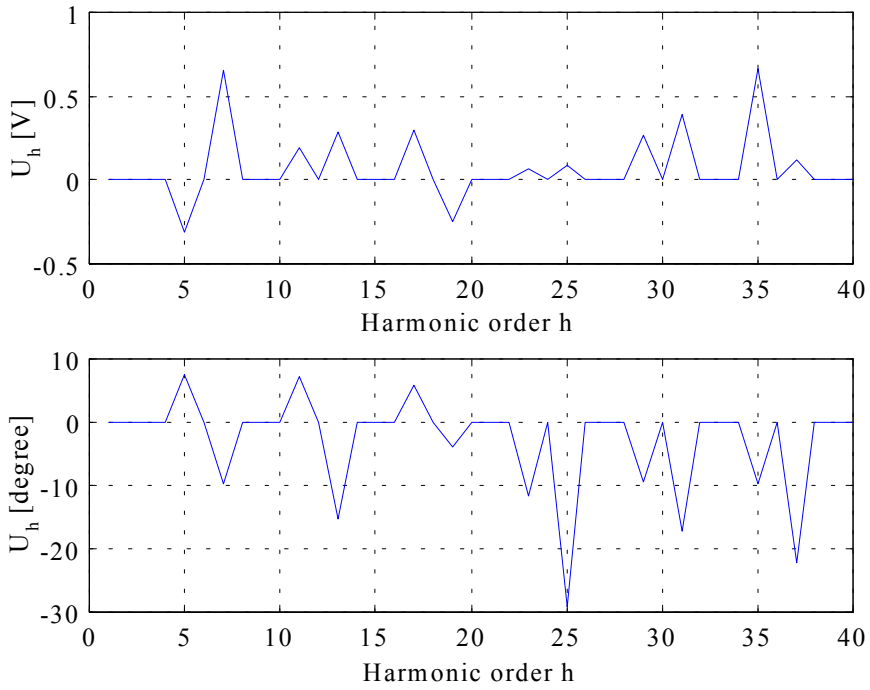


Figure 3-13: Difference between the measured and the corrected calculated harmonic voltage amplitude and phase-angles.

In the calculations above the length and the square of the conductors of the cables are well known. Also the nominal power and voltage rating of the transformer are known. However, the reactance and resistance of the cable and transformer are more or less approximations (data sheets). These are quite realistic circumstances in the "real world". Under these circumstances the simple impedance model shows a fairly good approximation. Therefore, it can be concluded that the simple impedance model can be used for calculation of the harmonic voltage. Errors in the basic data, such as length of the cable, size of the transformer or not taking the background distortion into account, are by far more important than a more precise impedance model. It should be noted, that the skin and proximity effects become more significant for larger conductors (> 240 mm^2) than used here [NKT]. However, conductors of this size are rarely used in an industrial ASD application because they become difficult to handle. Normally, smaller conductors (e.g. 120 mm^2) are used in parallel.

In applications where the data are precisely known and a more accurate calculation is desired, these models must be extended to include skin effect and proximity effect especially when large conductors are used. Also capacitive effects of the cables must then be included. However, high frequency modeling of cables and distribution line is outside the scope of this thesis.

3.4 Capacitor Banks

When power factor correction capacitors are present the system impedance becomes different than described above and resonance conditions become a very important issue.

So far, the harmonic currents are assumed to flow from the non-linear load into the source. This is due to that the source impedance normally is lower than the impedance offered by

parallel loads. However, especially if capacitor banks are present, the harmonic current split depending on the impedance ratio as shown in Figure 3-14. Higher harmonics flow to capacitors that are low impedance to high frequencies.

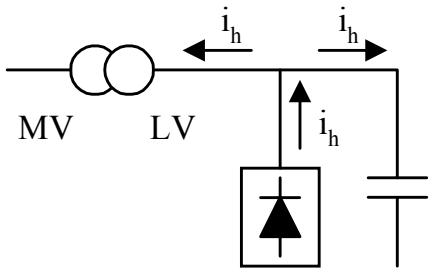


Figure 3-14: Flow of the harmonic currents when capacitor banks are present.

The total impedance of the system shown in Figure 3-14 seen from the non-linear load can be expressed as a parallel connection between the transformer impedance that is mainly inductive and the capacitor as illustrated in Figure 3-15.

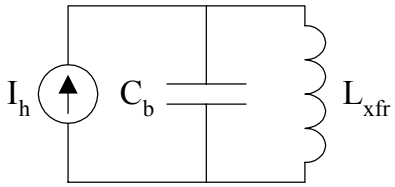


Figure 3-15: Parallel connection of the source inductance and the capacitor banks as seen from the non-linear load.

The total harmonic impedance including the transformer resistance becomes then:

$$Z_h = \frac{R_{xfr} + j\omega L_{xfr}}{-\omega^2 L_{xfr} \cdot C_b + R_{xf} r \cdot j\omega C_b + 1} \tag{3.11}$$

Assuming an industrial distribution system with a 50 Hz 1 MVA 10/0.4 kV transformer (e_x = 5%, e_r = 1%) and a reactive VAr compensation of 300 kVAr the impedance as a function of the frequency could look like in Figure 3-16.

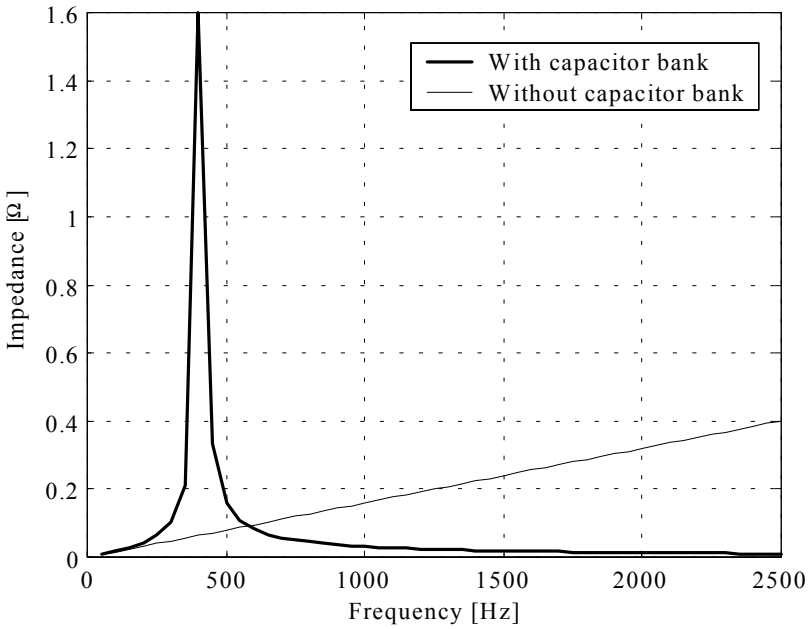


Figure 3-16: Impedance of a given system seen from the non-linear load with and without capacitor banks.

It can be seen that the impedance with capacitor banks differs significantly from the impedance without capacitor banks. The peak of the impedance curve with the capacitor bank indicates the resonance point. Below the resonance point the impedance becomes higher and above the resonance point the impedance becomes lower.

Resonance is one of the most dangerous factors affecting the system harmonic levels. Resonance occurs when the reactive impedance of the capacitor equals the reactance of the system inductance (e.g. transformer) at some frequency. Parallel resonance as shown here is high impedance to the harmonic currents and leads to high harmonic voltage distortion if triggered by harmonic currents. Therefore, it is important to check for resonance.

Another type of resonance is the series resonance which provides a low impedance path for the harmonic currents. This is typical the case when a capacitor bank is connected on the secondary side of the transformer. Due to the impedance of the transformer, the capacitor bank becomes a tuned filter seen from the MV line as shown in Figure 3-17.

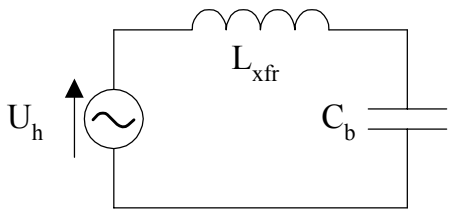


Figure 3-17: Serial connection of the source inductance and the capacitor bank as seen from the MV-line.

In combination with a pre-existing harmonic voltage at the resonance frequency, this can result in a high harmonic current overheating or damaging the capacitor bank. Figure 3-18 shows the impedance of the system described above seen from the MV side.

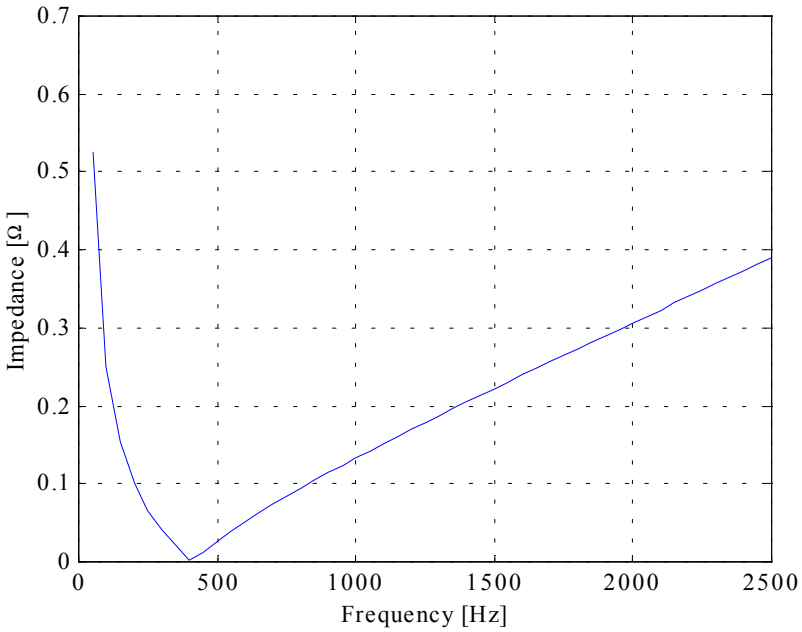


Figure 3-18: Impedance of a given system seen from the MV-line.

Other loads connected to the same bus complicate the calculations of the impedance. E.g. linear loads could provide some damping of the resonance and motors can increase the short circuit power and thereby move the resonant point. But for most systems simple calculations can unveil the resonance point.

Knowing the system reactance and the reactance of the capacitor banks the resonance frequency can easily be calculated by equation 3.12.

$$h_r = \sqrt{\frac{X_c}{X_{sc}}} = \sqrt{\frac{MVA_{sc}}{MVA_{cap}}} \tag{3.12}$$

where:

h_r is the resonant frequency at h_r times the fundamental frequency.

If the calculated resonance is near one of the characteristic harmonics of the non-linear load problems can occur, and a more detailed analysis is necessary, e.g. by numerical analysis.

It should be noted, that it is recommended that power factor correction capacitors should not be used without an additional (tuning) reactance in front of the capacitor bank when non-linear loads are a significant percentage of the total plant load eg. 10% [Mc Granaghan, Müller 1999], Using a tuned capacitor normally solves the problem of resonance. Furthermore, using a tuned capacitor bank can reduce the harmonic voltage distortion since the tuned capacitor bank works as a passive shunt filter (se also Chapter 6.3).

3.5 Standby Generators

It has become quite common to use UPS in combination with computers to ensure safe operation where loss of data is unacceptable. The same is true for large loads, such as ASD's used in wastewater treatment plants or hospitals where it is mandatory that the ASD's are operable on standby generators. However, there are some special considerations when standby generators are used together with large non-linear loads.

As described earlier in this chapter, the harmonic voltage distortion is highly depending on the system impedance and especially the transformer impedance, since this is the point where the voltage distortion normally is of interest. In standby generators the impedance to use for the harmonic voltage distortion calculations is the subtransient reactance X_d'' as shown in Figure 3-19 [P519 1998], [Osman 1994], [Swamy], [Fender et al 1999].

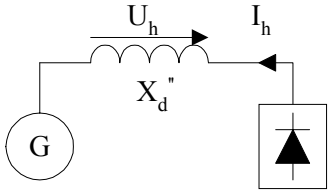


Figure 3-19: harmonic voltage distortion on a standby generator.

In the case where a standby generators is used instead of a supply transformer equation 3.2 can be rewritten as:

$$U_h = I_h \cdot h \cdot X_d'' \tag{3.13}$$

The typical value for the impedance of a distribution transformer varies from 3% - 7%. The subtransient reactance for a standby generator varies from 10% – 20% hence the expected voltage distortion will be larger using a standby generator than on a similar sized transformer.The increased voltage distortion compared to operation on the supply transformer can result in several difficulties.

1) Disturbance or increased losses of the connected equipment.
2) Increased losses on the generator.
3) Generator instability

There are several ways to overcome these potential problems. The easiest way (and probably the most expensive) is to design the system for $THD_v = 5\%$ as recommended by [IEEE 519] and [P519 1998]. THD_v less than 5% should guarantee no disturbance of sensitive equipment, keep the increased losses on both the connected equipment and generator within reasonable values and ensure safe operation of the standby generator. The design goal could be achieved with oversizing the standby generator or/and moving unnecessary non-linear loads to a different bus, which is not powered by the standby generator.

However, [Osman 1994], [Swamy] and [Fender et al 1999] states that higher voltage distortion level is acceptable if no sensitive equipment is connected to the generator bus (e.g. moved to a UPS). The acceptable voltage distortion level is then only limited by generator stability and thermal considerations of the generator.

The increased generator losses due to harmonics are normally not considered as a problem, while the generator stability can become troublesome when non-linear loads are involved. When thyristor converters are used the voltage notches confuse the frequency controller of the standby generator [Osman 1994] while the resulting flat-topped line-line voltage of the three-phase diode rectifier can result in erroneous exciting level of the dc-field and eventually cause saturation [Swamy]. Therefore [Swamy] recommends to limit the ASD load to less or equal to 60% of the total kVA rating of the standby generator, while [Osman 1994] recommends no to exceed 50%. Both limits are based on their own experience.

[Fender et al. 1999] have chosen a different approach to determine how large the non-linear load is allowed to be on a standby generator. [Fender et al. 1999] have actually measured the harmonic voltages on different generators sizes with different loads and compared the result with the allowed voltage distortion levels of the IEC 61000-2-2 as presented in chapter 2. Here they recommend that the three-phase diode rectifier load with additional ac-coils should not exceed 40% of the standby generator.

3.6 Conclusion

In this chapter the various aspects of harmonic voltage distortion calculations are discussed. Calculation of the harmonic voltage distortion seems trivial as indicated by equation 3.1 and some simplified voltage distortion calculations were presented based on ideal conditions. This simple method allows fast and easy estimation of the total harmonic distortion level in a given system. However, it was also shown that several parameters complicate the harmonic voltage distortion calculations.

It is shown that the supply voltage often is distorted even if the supply transformer is un-loaded. This is due to the background distortion. This complicates the harmonic voltage distortion calculation because the resulting voltage distortion is a geometrical sum of the background distortion and the harmonic voltage drop of the non-linear load. This is a very important point, because depending on the phase-angle between the harmonic background distortion and the generated harmonic voltage distortion, this can actually result in decreasing harmonic voltage distortion compared to the background distortion.

It is well known that the harmonic impedance is frequency depending in a non-linear manner, due to proximity and skin effects. Therefore, the exact harmonic impedance can be difficult to determine in a given system. However, it is shown that a simple linear impedance model is sufficient for most harmonic voltage calculations. This is also an important point because this simplifies the calculations significantly.

It is shown that if capacitor banks are used these have a significant influence on the harmonic system impedance and these must therefore be included in the calculations. Furthermore, capacitor banks can result in resonance, which makes it difficult to predict the resulting voltage distortion.

Finally, the special case where standby generators are used instead of supply transformers was discussed and different recommendations were summarized.

4. Harmonic Current Distortion of the Diode Rectifier

For calculation of the harmonic voltage distortion knowledge about the harmonic current distortion is essential. For easy calculation of the resulting harmonic distortion, it is of great importance to find a simple model for the diode rectifier. Unfortunately, even though the diode rectifier has a very simple circuit diagram, calculation of the (harmonic) currents is not a trivial task. Four levels of modeling, as shown in Figure 4-1, are discussed in this chapter.

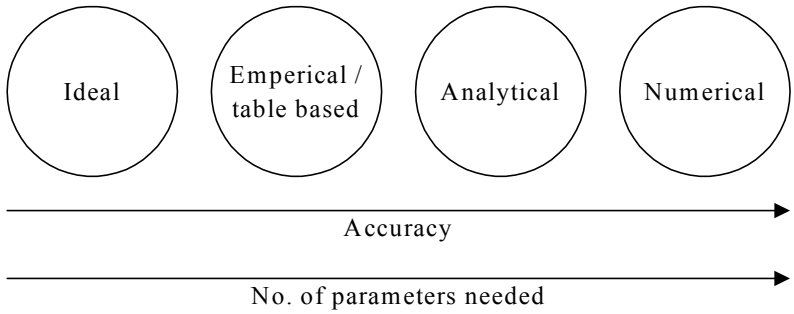


Figure 4-1: Different levels of modelling the diode rectifier.

The first level is the ideal model of the diode rectifier. This model has very limited accuracy, but on the other hand almost no parameters are needed as input. The ideal model is often cited when modeling the diode rectifier and is therefore reviewed in this chapter.

The second level is a table-based model of diode rectifier. This method may be suitable to calculate the harmonic distortion in some applications. The error obtained by using this very simple model is justified by the fact that not all parameters need to be known. Also, in practical applications all system parameters are normally not known. Therefore, one can claim that the very simple model is acceptable to estimate the harmonic distortion. In this chapter a table-based model for the both the three-phase and single-phase diode rectifier is presented.

The third level of the diode rectifier model presented in this chapter is based on an analytical model. The analytical model shows to be quite accurate assuming sinusoidal and balanced voltages.

The harmonic currents are heavily depending on the input voltage (pre-distortion and unbalance). So far, there are no accurate analytical models of the diode rectifier taking all these parameters into account. Therefore, the fourth level of the diode rectifier model is the use of a numerical based circuit simulator. The advantages of circuit-based simulators are that non-linear components, such as diodes, are easily incorporated in the circuit and that circuit topologies easily can be changed. Furthermore, pre-distorted and unbalanced supply voltages can be simulated quite simple compared to other methods. The disadvantage can be long calculation times, and, since it is a circuit-based simulator, all parameters for the system must be known. In this chapter it is chosen to use the circuit simulator SABER to describe the currents of the diode rectifier.

4.1 Ideal Model of the Diode Rectifier

The idealized diode rectifier as shown in Figure 4-2 obtains the simplest analytical model. The current of the idealized diode rectifier is assumed to be smooth on the dc side ($L_{dc} \Rightarrow \infty$) and commutation effects are neglected ($L_s = 0$), i.e. the current is changing instantaneously from zero to some finite magnitude.

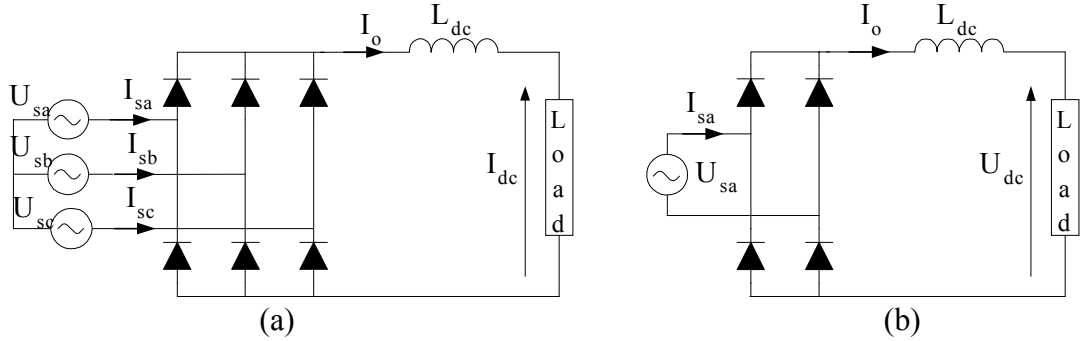


Figure 4-2: The ideal (a) three-phase and (b) single-phase diode rectifier with $L_{dc} \Rightarrow \infty$ and no line impedance ($L_s = 0$).

This results in that the current appears as a symmetrical square wave with a conducting interval of 120° for the three-phase and 180° for the single-phase diode rectifier as shown in Figure 4-3.

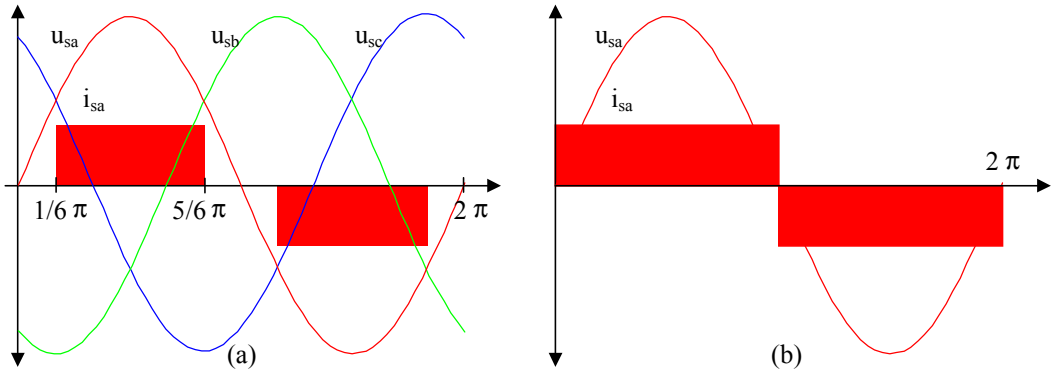


Figure 4-3: The voltages and currents of an idealized (a) three-phase diode rectifier and (b) single-phase diode rectifier.

It should be noted, that in a practical single-phase diode rectifier application the conducting interval is significant less than 180° because the dc-link capacitor for smoothing the voltage can be considered as a voltage source (the rectifier conducts only when the line voltage is higher than the dc-link voltage, see also Figure 4-12). Therefore, an analysis of the idealized single-phase rectifier is only useful to illustrate some basic calculations, while the idealized three-phase diode rectifier can be sufficient for some analysis.

4.1.1 Idealized model for the single-phase diode rectifier

For determining the characteristics of the idealized diode rectifier a Fourier analysis is necessary. The idealized line current in phase 'a' (I_{sa}) can be expressed as:

$$i_{sa}(t) = \begin{cases} -I_o & -\pi < \omega t < 0 \\ I_o & \pi < \omega t < 0 \end{cases} \tag{4.1}$$

The line current is an "odd" function in the sense of Fourier series [Kreyzig, 1988]. Therefore, the current can be expressed as:

$$i_{sa}(t) = f(x) = \sum_{h=1}^{\infty} b_h \sin(h \cdot \omega t) \quad b_h = \frac{2}{\pi} \int_0^{\pi} f(x) \sin(h \cdot \omega t) dt \tag{4.2}$$

Calculating the Fourier coefficients gives:

$$b_h = \frac{2I_o}{h\pi}(1 - \cos(h\pi)) \tag{4.3}$$

There are no even harmonics, since cos (2π) = 1, cos (4π) = 1 etc. Thus, the current of an idealized single-phase diode rectifier can be expressed as:

$$i_{sa}(t) = \frac{4I_o}{\pi}\left(\sin \omega t + \tfrac{1}{3}\sin 3\omega t + \tfrac{1}{5}\sin 5\omega t + \tfrac{1}{7}\sin 7\omega t + ...\right) \tag{4.4}$$

The current THD_i of the idealized single-phase diode rectifier is $THD_i = 48.3\%$.

4.1.2 Idealized model for the three-phase diode rectifier

As shown in Figure 4-3, one phase of the three-phase diode rectifier is only conducting 2/3 of one period and not the total period as the single-phase diode rectifier. This results in a different Fourier series. The current can be expressed as:

$$i_{sa}(t) = \begin{cases} 0 & -\pi < \omega t < -\frac{5}{6}\pi \\ -I_o & -\frac{5}{6}\pi < \omega t < -\frac{1}{6}\pi \\ 0 & -\frac{1}{6}\pi < \omega t < \frac{1}{6}\pi \\ I_o & \frac{1}{6}\pi < \omega t < \frac{5}{6}\pi \\ 0 & \frac{5}{6}\pi < \omega t < \pi \end{cases} \tag{4.5}$$

Calculating the Fourier coefficients gives:

$$b_h = \frac{4I_o}{h\pi}\left(\sin\left(\tfrac{h\cdot\pi}{2}\right) \cdot \sin\left(\tfrac{h\pi}{3}\right)\right) \tag{4.6}$$

Since sin (hπ) = 0, there are no even or triplen harmonics. Thus, the current of an idealized three-phase diode rectifier can be expressed as:

$$i_{sa}(t) = \frac{\sqrt{3}}{2}\frac{4I_o}{\pi}\left(\sin \omega t - \tfrac{1}{5}\sin 5\omega t - \tfrac{1}{7}\sin 7\omega t + \tfrac{1}{11}\sin 11\omega t + \tfrac{1}{13}\sin 13\omega t + ...\right) \tag{4.7}$$

The current THD_i of the idealized three-phase diode rectifier equals $THD_i = 31.1\%$. Note, the fifth, seventh and seventeenth etc. harmonic currents of the idealized three-phase diode rectifier are in counter phase with the corresponding harmonics of the single-phase diode rectifier.

When not taking the phase-angle of the harmonics into account it is possible to obtain a simple equation describing the currents of the single- and three-phase diode rectifier. Equation 4.4 and equation 4.7 can for the characteristic harmonics be rewritten to:

$$\frac{I_h}{I_1} = \frac{1}{h} \qquad h = p \cdot k \pm 1 \tag{4.8}$$

where k = 1, 2, 3 etc. and p is the pulse number. The pulse number is the total number of non-simultaneous commutations pr. period. The three-phase diode rectifier is a six-pulse rectifier and the single-phase diode rectifier is a two-pulse rectifier. The harmonic orders calculated by this equation are called the characteristic harmonics.

Equation 4.8 is often cited when modeling diode rectifiers, but as shown later in this chapter the real current of a diode rectifier differs somewhat from the idealized current. The simplest model beside equation 4.8 is obtained by taking the influence of the commutation angle into account.

4.1.3 The effect of commutation

It is clear that a perfect square wave is never encountered in an actual power system. The first step of modifying the values obtained from equation 4.8 is the recognition that a current wave cannot instantaneously change from zero to some finite magnitude as shown in Figure 4-3. In a three-phase diode rectifier there is a period of time in where the current commutates from one diode to another. The length of this commutation period μ is a function of the magnitude of the dc-current and the ac system inductance L_s. Figure 4-4 shows the current of a three-phase rectifier with the characteristic double humps and commutation.

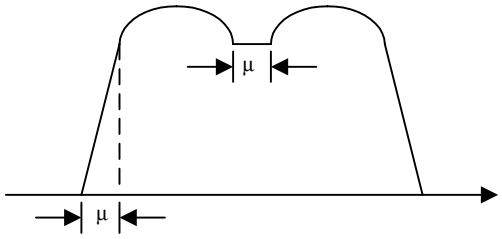


Figure 4-4: Current of a three-phase rectifier with current ripple and commutation.

[Rice, 1994] and [IEEE 519, 1992] describe a method to calculate the influence of the commutation reactance. With this method it is possible to calculate the amplitude of the harmonic currents, but not the phase-angle of the harmonic currents.

$$\frac{I_h}{I_1} = \frac{\sqrt{a^2 + b^2 - 2 \cdot a \cdot b \cdot \cos(2\alpha + \mu)}}{h \cdot (\cos\alpha - \cos(\alpha + \mu))} \tag{4.9}$$

where:

μ is the commutation angle.
α is the firing angle i.e. zero for diode rectifier.

$$a = \frac{\sin((h-1)\frac{\mu}{2})}{h-1}$$

$$b = \frac{\sin((h+1)\frac{\mu}{2})}{h+1}$$

μ is depending on the system impedance and can be calculated as [Mohan et al, 1995]:

$$\mu = \cos^{-1}\left(1 - \frac{2\omega L_s}{\sqrt{2}U_{LL}} I_o\right) \tag{4.10}$$

Equation (15) can be rewritten in terms of the short circuit ratio R_{sce}.

$$\mu = \cos^{-1}(1 - \frac{2\omega L_s}{\sqrt{2}U_{LL}} I_o) = \cos^{-1}(1 - \frac{\omega L_s S_{nom}}{U_{LL}^2}) = \cos^{-1}(1 - \frac{1}{R_{sce}}) \tag{4.11}$$

The effect of the commutation reactance results in that the harmonics are less than described by the 1/h model (especially the higher harmonics 11th, 13th etc.). This is shown in Figure 4-5:

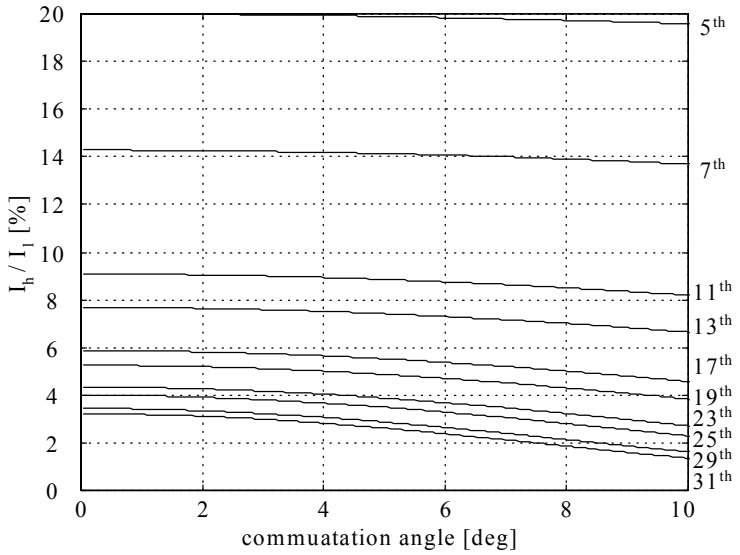


Figure 4-5: The effect of the commutation reactance to the harmonic current generation of a three-phase diode rectifier.

This model takes the ac-inductance into account, and it clearly shows that especially the higher harmonic currents are influenced by the ac-inductance. This is worth noting because this tendency has been experienced in several measurements and simulations of real diode rectifier applications. On the other hand this model is less useful for voltage stiff type rectifiers since a large smoothing inductance is assumed, which is typical used in current stiff rectifiers. Furthermore, the phase-angle of the harmonic currents is not included.

Several other models on the same level exist, but these models are influenced by the wide spread use of the dc-motor and high voltage direct current (HVDC) transmission in the seventies and early eighties which basically means that the rectifier where used for current stiff applications instead of voltage stiff applications. Therefore these models are not shown here. Some of these models can be found in [Rice 1994].

4.2 Table-Based Harmonic Model of the Diode Rectifier

Recognizing the limits of the ideal model of the diode rectifier, the next level is to measure or simulate (by use of numerical circuit simulators) a series of the line current of the diode rectifier for varying parameters such as the line impedance. The results are stored in a look-up table and the actual values for a given application are then found by interpolation.

The disadvantage of using measurements of the line current for generating the table is that this becomes very time consuming. In this section the tables are generated by the SABER simulator. Only values for Hc and THD_i for different short circuit ratios are presented in this section but the tables can be extended to contain the individual harmonic currents. The Hc values found in this section may very well be used to calculate the total harmonic voltage distortion as described in Chapter 3.1.

Even though Hc is denoted the harmonic constant, Hc (and the THD_i) is not constant at all. The line impedance has a significant influence. Making some assumptions it is possible to calculate the currents of the diode rectifier and identify Hc as a function of the short circuit ratio. The assumptions made for the simulations are:

- The line voltage is balanced and sinusoidal
- The diode rectifier operates at rated load
- The grid is primary inductive
- All passive components are linear. I.e. the resistance and inductance are constant at all frequencies

Furthermore, it is assumed that the diode rectifier is of the voltage stiff type. This means that the dc-link capacitor is sufficient large to maintain a constant dc-link voltage. This is a fair assumption since most of the diode rectifiers used in today's power electronic converters are of this type. This is especially true for the single-phase diode rectifier.

Some three-phase diode rectifiers have an additional inductance in the dc-link to suppress harmonic currents and to ensure continuously current into the dc-link of the diode rectifier. This has also the advantage of higher lifetime expectations of the capacitors used in the dc-link. However, some manufacturers choose to omit the dc-link inductance and offer additional ac-reactance. Single-phase diode rectifiers tend to be low cost and low power. Therefore, a dc-link inductance is normally not used. So, three diode rectifier topologies are investigated:

- The basic three-phase diode rectifier without any dc-link inductance (Figure 4-6a)
- The three-phase diode rectifier with a 3% dc-link inductance (Figure 4-6b)
- The basic single-phase diode rectifier without any dc-link inductance (Figure 4-7)

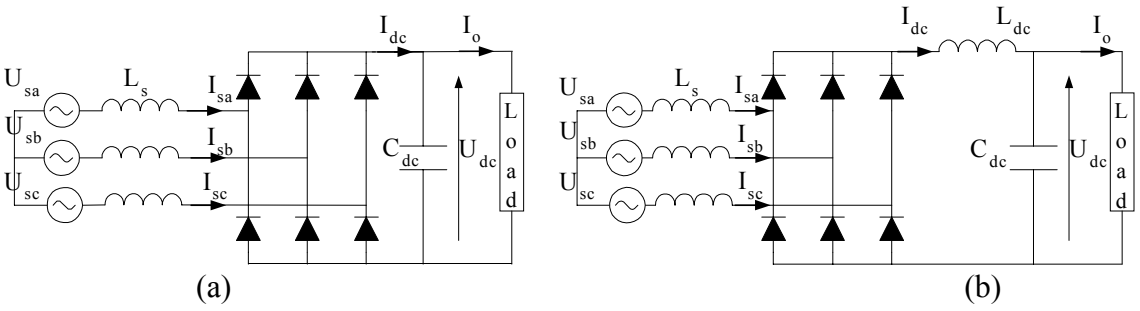


Figure 4-6: The simulated three-phase diode rectifier (a) without any additional inductance and (b) with a 3% dc-link inductance.

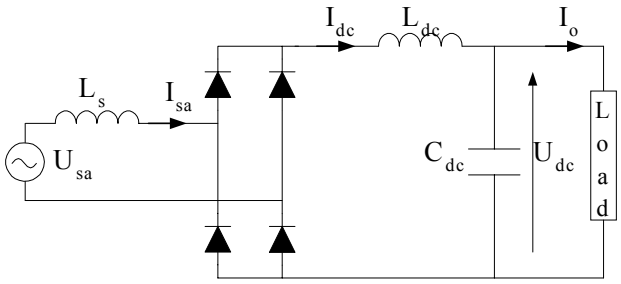
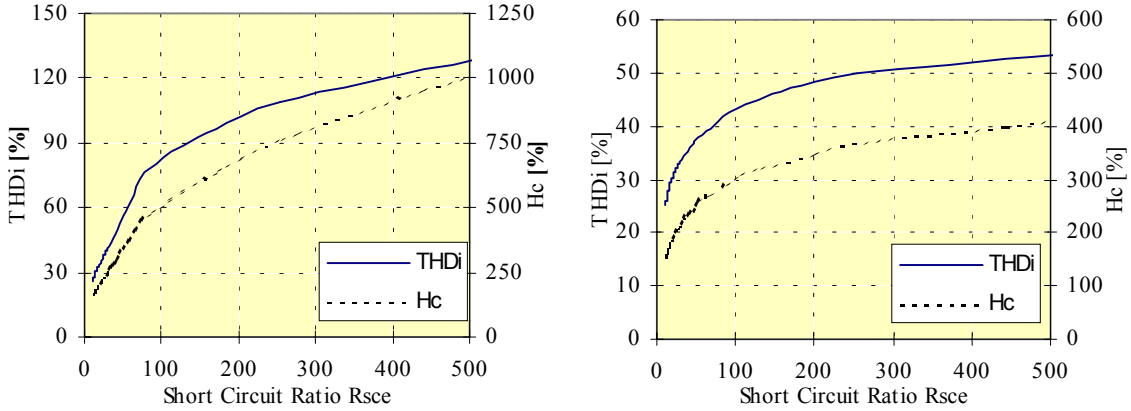


Figure 4-7: The simulated basic single-phase diode rectifier.

Note, that L_{dc} = 3% is in the lower end of the average value used in the industry (usually 3-5%). Figure 4-8 shows the Hc and THD_i values of the three-phase diode rectifier with and without a 3% dc-link inductance and varying short circuit ratio. The lowest THD_i value of both rectifiers is close to 25%, while the lowest Hc value equals 150%.



(a) (b)

Figure 4-8: Hc and THD_i values for the three-phase diode rectifier as a function of the short circuit ratio without (a) and with (b) 3% dc-link inductance.

Note, that a diode rectifier connected to a grid with a short circuit ratio of 20 equals a diode rectifier connected to a stiff grid with a 5% ac-reactance (here the 5% are related to the rectifier p.u. notation).

In Figure 4-8 (a) the THDi and Hc is increasing more rapidly from R_{sce} = 20 – 80 than above. This is due to the different conduction modes of the basic diode rectifier. Below a short circuit ratio of approximately 80 the current of the basic three-phase diode rectifier is discontinuous (DCM) as shown in Figure 4-9. Above a short circuit ratio of approximately 80 the current becomes continuous (CCM). In between these conduction modes (in a very limited short circuit ratio range) there is another discontinuous mode, where the commutation is started between the diodes, but the current still becomes discontinuous (DCCM II). For the three-phase diode rectifier with some 3% dc-link inductance the current is continuous independent of the short circuit ratio.

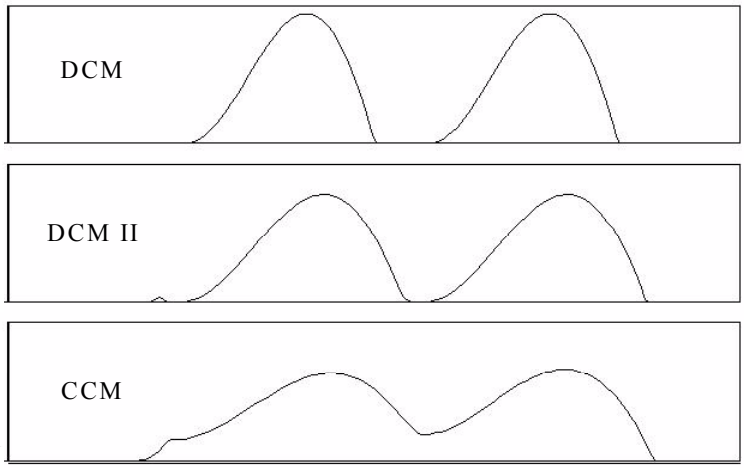


Figure 4-9: The three modes of the basic three-phase diode rectifier. Discontinuous conduction mode (DCM), discontinuous conduction mode II (DCM II), continuous conduction mode (CCM).

Figure 4-10 shows the Hc and THD_i values of the single-phase diode rectifier for varying short circuit ratio. The lowest THD_i value of the single-phase diode rectifier is 61%. While the lowest Hc value equals 225%.

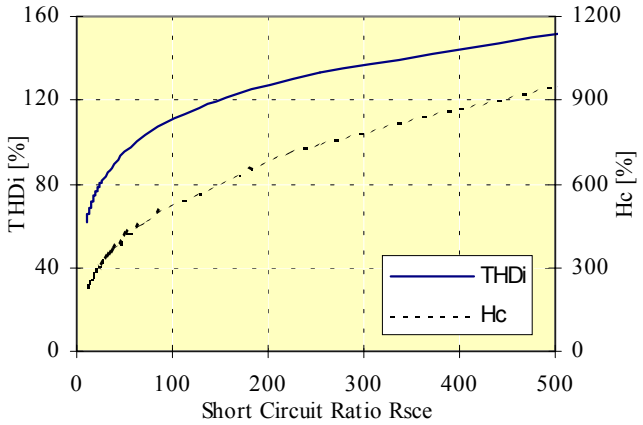


Figure 4-10: Hc and THD_i values for the single-phase diode rectifier with varying short circuit ratio.

Figure 4-8 and Figure 4-10 show clearly that the Hc and THD_i values are very depending on the ac-impedance. Therefore, it is important to know some basic system parameters such as the short circuit power at the connection point and the nominal load of the diode rectifier before it is possible to estimate the harmonic current distortion of the diode rectifier. If the short circuit ratio is fairly known the values above may be used to calculate the harmonic voltage distortion as shown in Chapter 3.1. For this purpose a one-page diagram of Figure 4-8 and Figure 4-10 can be found in Appendix B.

This is a very simple approach, and experience shows that in most cases this gives an acceptable result. Especially when taking into account, that for more accurate calculations more detailed knowledge of the system parameters is essential.

4.3 Analytical Models

If the more detailed system parameters are known, such as the capacitance of the dc-link capacitor, dc-link inductance, load etc., analytical models can be used.

4.3.1 Accurate model for the single-phase diode rectifier

Ref. [Mohan et al., 1995] describes an analytical model of the single-phase diode rectifier. The model is based on the assumption of discontinuous current. This assumption is normally met in a practical single-phase diode rectifier. The described analytical model is summarized here. Figure 4-11 shows the rectifier circuit with the state variables.

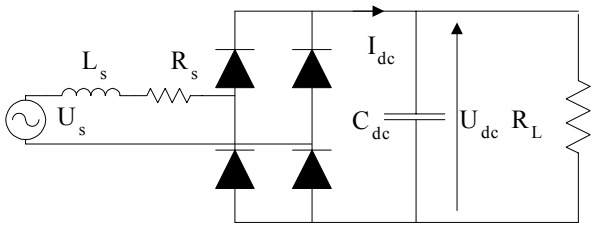


Figure 4-11: The single-phase diode rectifier circuit diagram used for the analytical model including line impedance and a dc-link capacitor.

For each half-cycle of the line frequency there are two intervals. A) The diodes are conducting and the capacitor is charged and B) the diodes are not conducting. Following equations describe state A:

$$u_s = R_s i_{dc} + L_s \frac{di_{dc}}{dt} + u_{dc} \tag{4.12}$$

and

$$i_{dc} = C_{dc} \frac{du_{dc}}{dt} + \frac{u_{dc}}{R_L} \tag{4.13}$$

Rearranging equation 4.12 and 4.13 gives:

$$\begin{bmatrix} \frac{di_{dc}}{dt} \\ \frac{du_{dc}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_s}{L_s} & -\frac{1}{L_s} \\ \frac{1}{C_{dc}} & -\frac{1}{C_{dc} R_L} \end{bmatrix} \begin{bmatrix} i_{dc} \\ u_{dc} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_s} \\ 0 \end{bmatrix} u_s \tag{4.14}$$

Using numerical integration methods such as the trapezoidal method of integration this state equation can be solved. Since these equation solvers often are a part of software packages e.g. MATLAB this is not shown here.

During the interval where the diode is not conducting following equations describe the state B:

$$i_{dc} = 0 \tag{4.15}$$

and

$$\frac{du_{dc}}{dt} = -\frac{1}{C_{dc} R_L} u_{dc} \tag{4.16}$$

For the correct solution of the equations an exact value of the start time for conduction and the initial value of the dc-link voltage is needed. This value can be calculated iterative. When the starting time for conduction of the diodes is the same in two following half cycles the correct initial value is found. Figure 4-12 shows a period with correct initial values.

Using DFT (Discrete Fourier Transformation) the harmonic currents can be determined including the phase-angle information. The disadvantage of this method is that the correct initial values have to be found iteratively.

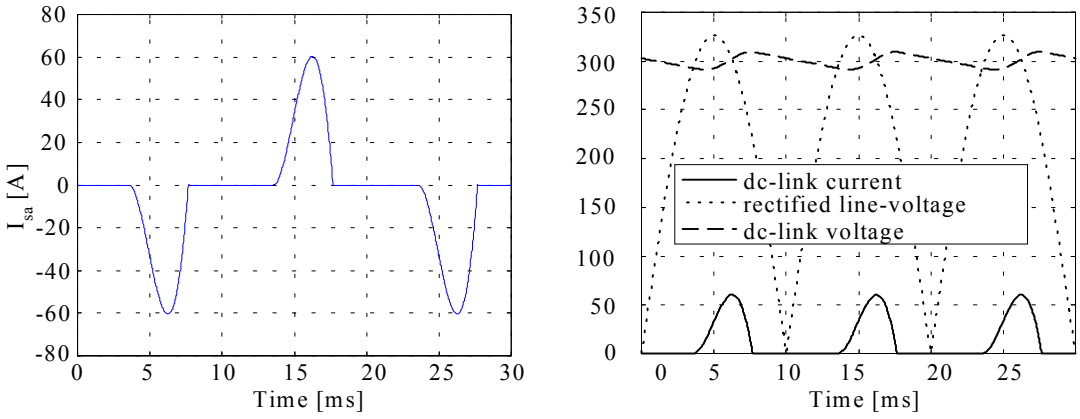


Figure 4-12: Matlab simulation of the single-phase diode rectifier. (a) Line current. (b) dc-link current and voltages.

The presented single-phase diode rectifier model is evaluated by comparing the results with some SABER simulations. The same values for the dc-link capacitor C_{dc} and line inductance L_s are used as in the SABER simulations of the single-phase diode rectifier in section 4.2. The calculated values for Hc and THD_i are compared with those simulated in SABER and presented in Section 4.2. Figure 4-13 shows both the values simulated in SABER and the values calculated by the method presented above. It can be seen that the THD_i and Hc values are nearly identical.

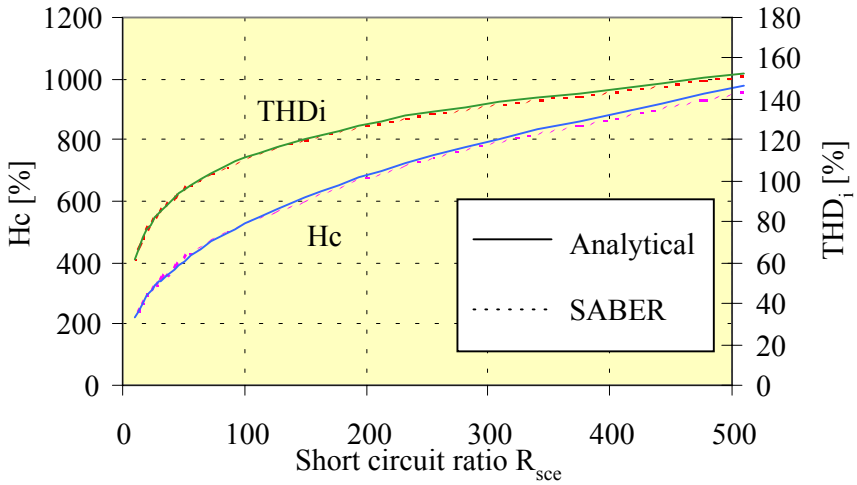


Figure 4-13: Evaluation of the analytical model for the single-phase diode rectifier by comparing the THDi and Hc value with those simulated in SABER.

Figure 4-14 shows the values of the 3rd, 5th, 7th, 9th, 11th and 13th harmonic currents simulated in SABER and the values calculated analytical. Again the calculated and simulated values are nearly identical.

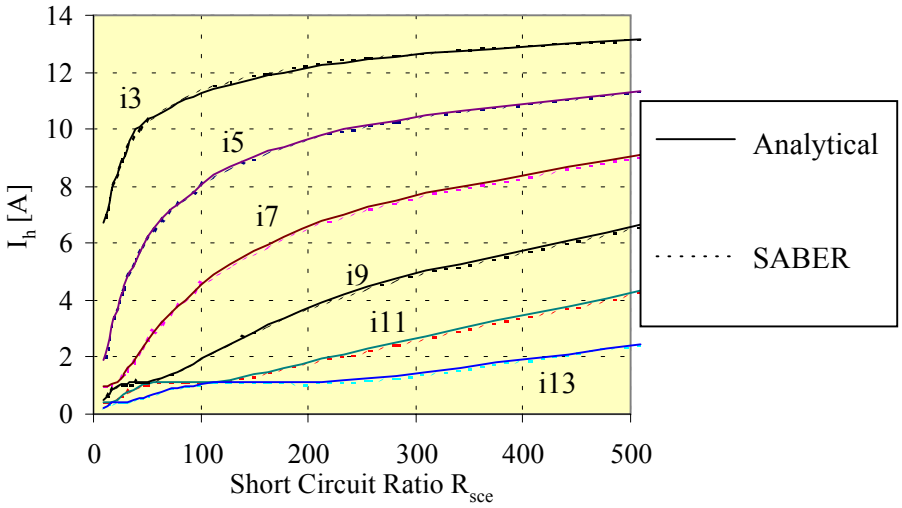


Figure 4-14: Evaluation of the analytical model for the single-phase diode rectifier by comparing the 3rd, 5th, 7th, 9th, 11th and 13th harmonic current with those simulated in SABER.

As shown above it is possible for sinusoidal and balanced voltage to describe the single-phase diode rectifier analytical. In the next section analytical models for the three-phase diode rectifier are described.

4.3.2 Accurate model for the three-phase diode rectifier

In the continuous mode the analytical model for the three-phase rectifier is somewhat more complicated than for the single-phase rectifier because the continuous dc-current is shared by different phases. Several papers on this subject exist [Sakui & Fujita, 1994], [Baghzouz, 1993], [Grötzbach, 1989] and some of the ideas are used here for deriving an accurate analytical model for the three-phase diode rectifier (as shown in Figure 4-15) in continuous mode.

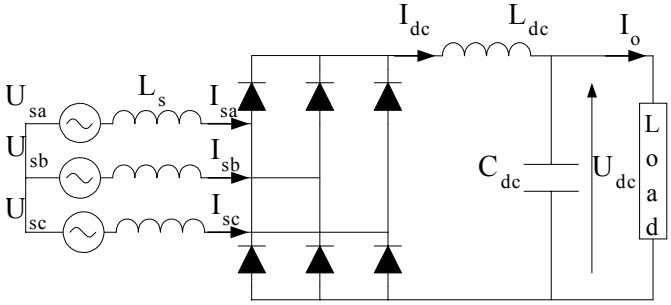


Figure 4-15: The Three-phase diode rectifier circuit diagram used for the analytical model.

The basic idea is to multiply the switching functions of the diode rectifier with the dc-link current i_{dc}. The i_{dc} consists basically of a dc-component I_o and a harmonic component Δi_{dc}.

$$i_{dc} = I_o + \Delta i_{dc} \tag{4.17}$$

The switching functions sw_1, sw_2 and sw_3 describe the characteristic 120° square-wave and for phase a this switching function is given by the well known Fourier series:

$$sw1 = \sum_{h=1}^{\infty} b_n \sin(h \cdot \omega t) \quad b_n = \frac{4}{h\pi}\left(\sin\frac{h\pi}{2}\sin\frac{h\pi}{3}\right) \tag{4.18}$$

The line current of phase 'a' then becomes:

$$i_{sa} = sw1 \cdot i_{dc} \tag{4.19}$$

The problem by this method is that deriving the ripple part of the dc-link current is not an easy task. Also, the switching function defined above is not taking the commutation into account.

Including the commutation, results in a different switching function as above. The switching function is "non-symmetrical" and the Fourier series become:

$$sw1 = \sum_{h=1}^{\infty} (a_{sh} \cos(h \cdot \omega t) + b_{sh} \sin(h \cdot \omega t)) \tag{4.20}$$

The coefficients a_{sh} and b_{sh} calculated by the method of jumps [Kreyzig, 1988]:

$$\begin{aligned} a_{sh} &= \frac{4}{\pi \cdot \mu \cdot h^2}\left[\sin\left(\frac{h\pi}{2}\right)\cdot\sin\left(-\frac{h\pi}{3}\right)+\sin\left(\frac{h\pi}{2}+h\mu\right)\cdot\sin\left(\frac{h\pi}{3}\right)\right] \\ b_{sh} &= \frac{4}{\pi \cdot \mu \cdot h^2}\left[\cos\left(\frac{h\pi}{2}\right)\cdot\sin\left(\frac{h\pi}{3}\right)+\cos\left(\frac{h\pi}{2}+h\mu\right)\cdot\sin\left(-\frac{h\pi}{3}\right)\right] \end{aligned} \tag{4.21}$$

The dc-ripple current is calculated as described in [Sakui & Fujita, 1994], where the m^{th} harmonic dc-ripple current i_{dm} equals:

$$i_{dm} = \sqrt{2} \cdot I_{dm} \cdot \cos(m\omega t - \lambda) \tag{4.22}$$

where: I_{dm} is the amplitude of the m^{th} harmonic dc-ripple current,
λ is the angle between dc-link voltage and current ($\pi/2$)

I_{dm} is calculated as function of the individual harmonic amplitudes of the dc-link voltage and the total impedance. Where the dc-link voltage can be described as:

$$u_{dc} = U_{dc} + \sum_{m=6}^{\infty} (a_{dm} \cos m\omega t + b_{dm} \sin m\omega t) \tag{4.23}$$

where U_{dc} is the dc-part of the dc-link voltage and a_{dm} and b_{dm} are given by:

$$\begin{aligned} a_{dm} &= \frac{3\sqrt{3} \cdot U_{LL} \cdot (-1)^k}{2\pi}\left[\frac{\cos((m+1)\cdot\mu)}{m+1} - \frac{\cos((m-1)\cdot\mu)+1}{m-1}\right] \\ b_{dm} &= \frac{3\sqrt{3} \cdot U_{LL} \cdot (-1)^k}{2\pi}\left[\frac{\sin((m+1)\cdot\mu)}{m+1} - \frac{\sin((m-1)\cdot\mu)}{m-1}\right] \end{aligned} \tag{4.24}$$

The derived switching function and the described dc-ripple current equations of above are implemented in a MATLAB program. Figure 4-16 shows an example of a MATLAB simulation of a three-phase diode rectifier.

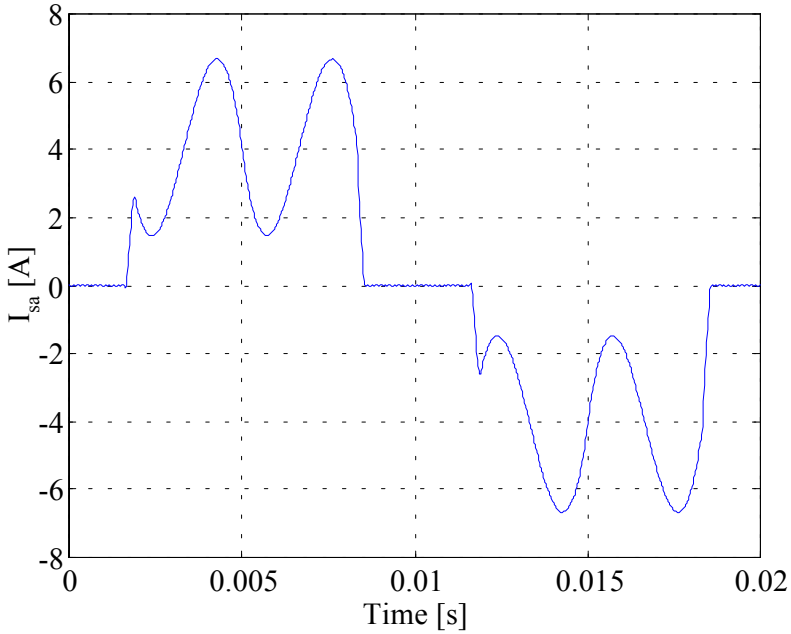


Figure 4-16: MATLAB simulation of a three-phase diode rectifier.

As with the analytical model for the single-phase diode rectifier the presented model is evaluated by comparing the results with some SABER simulations. Again the same values for the dc-link capacitor, L_s and L_{dc} are used as in the SABER simulations of the three-phase diode rectifier with a 3% dc-link inductance in section 4.2. The calculated values for Hc and current THD_i are compared with those simulated in SABER and presented in Section 4.2. Figure 4-17 shows both the values simulated in SABER and the values calculated by the method presented above.

It can be seen that the calculated and simulated THD_i values are almost identical, while there is a small difference in the Hc values. This indicates a difference in especially the higher harmonics since these have a higher weight factor in the Hc definition than in the THD definition.

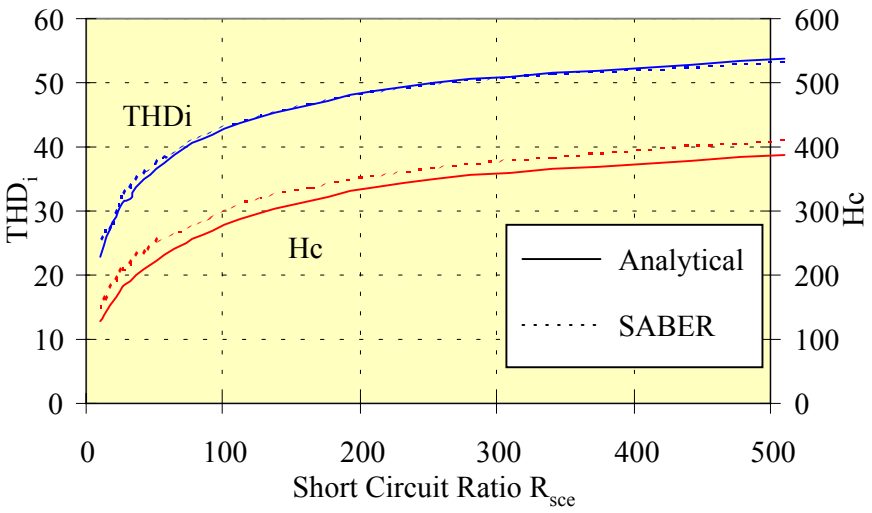


Figure 4-17: Evaluating the analytical model for the three-phase diode rectifier by comparing the THDi and Hc value with those simulated in SABER.

Figure 4-18 shows the values of the 5th, 7th, 11th and 13th harmonic currents simulated in SABER and the values calculated by the method presented above. Again the difference is very small between the calculated and simulated values. Below a short circuit ratio of 100 especially the 13th harmonic current shows some differences.

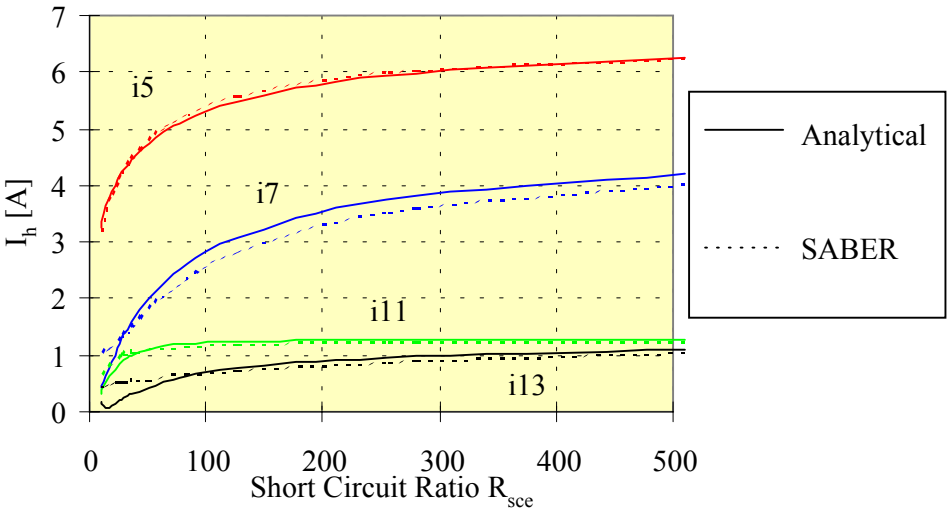


Figure 4-18: Evaluating the analytical model for the three-phase diode rectifier by comparing the 5th, 7th, 11th and 13th harmonic current with those simulated in SABER.

The presented analytical models for both the single- and three-phase diode rectifier can be used as medium level models. I.e. they are more accurate than the ideal and table-based models. However, all parameters for the diode rectifier must be known for the analytical model. Furthermore, the analytical model is only valid at sinusoidal and balanced grid. If these conditions are not met, numerical calculations tools should be used.

4.4 Numerical Models of the Diode Rectifier

Numerical circuit based simulators, such as PSPICE, SABER and EMTP, are commonly used to simulate the diode rectifier [Grötzbach et al, 1995], [Ray et al, 1988]. In this

section the numerical circuit simulator SABER is used to determine the phase-angle of the individual harmonic currents as a function of the line impedance. This is a very important issue, because knowledge of the phase-angle is necessary to calculate the sum of harmonic currents of several diode rectifiers. Also knowledge on the phase-angle is necessary to understand how the harmonic currents of the diode rectifier influences the overall power system (see also Appendix D.1). Both an analysis of the phase-angle of different harmonics with respect to the short circuit ratio as well as the practical importance is discussed.

The circuit diagrams of Figure 4-19 are used to simulate the harmonic current phase-angles of the different diode rectifier topologies.

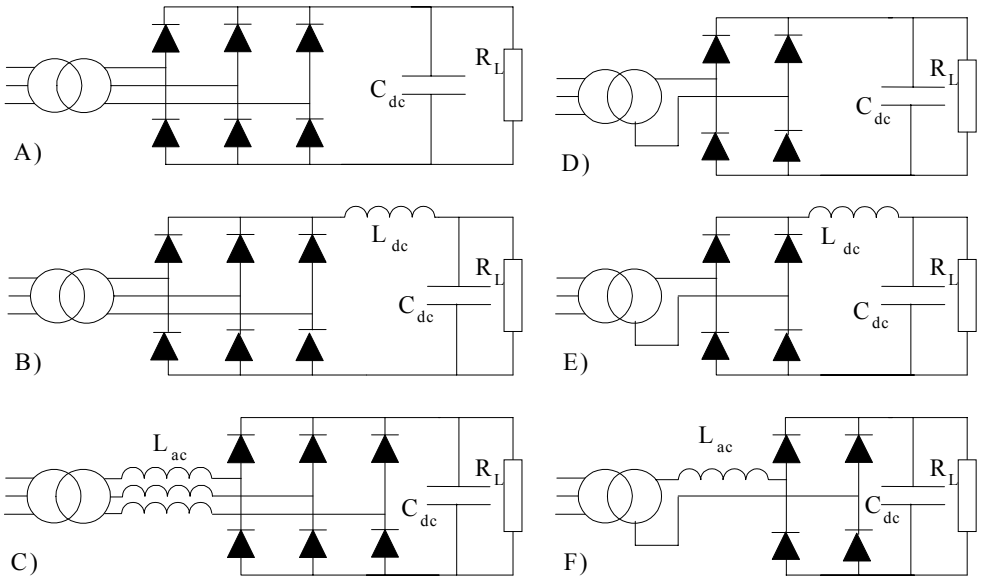


Figure 4-19: Circuit diagrams of the simulations (S_{xfr} = 200 kVA - 6 MVA, ex = 10%, er = 2%).
A) Basic three-phase diode rectifier
B) Three-phase rectifier with dc-link inductance (L_{dc})
C) Three-phase rectifier with ac inductance (L_{ac})
D) Basic single-phase rectifier
E) Single-phase rectifier with dc-link inductance (L_{dc})
F) Single-phase rectifier with ac inductance (L_{ac})

A transformer with e_x = 10% and e_r = 2% is connected to a basic three-phase diode rectifier without any dc-link or additional ac-inductance (Figure 4-19 A). The fundamental apparent input power of the three-phase rectifier is S_1 = 100 kVA. The transformer size S_{xfr} is varied from 200 kVA to 6 MVA which gives a varying ac-side impedance on the secondary side of the transformer. The short circuit power on the secondary side of the transformer is thereby varied from 2 MVA - 60 MVA which gives a short circuit ratio $R_{sce} = S_{sc} / S_1$ = 20 - 600.

A similar simulation is also made with a three-phase diode rectifier with a dc-link inductance (Figure 4-19 B) and with an additional ac-inductance (Figure 4-19 C). Also similar simulations are made for the basic single-phase rectifier (Figure 4-19 D), the single-phase diode rectifier with a dc-link inductance (Figure 4-19 E) and the single-phase diode

rectifier with an additional ac-inductance (Figure 4-19 F). The fundamental input power of the single-phase rectifiers is S_1 = 33 kVA each. This gives a total three-phase load of 100 kVA.

The dc-link capacitor used in case A, B, C, D, E and F is C_d = 20% related to the rectifier per-unit notation. The inductance used in case B, C, E and F equals 3% and it is also related to the rectifier per-unit notation. The harmonic currents are simulated with a step of R_{sce} = 20. The results of the simulations are shown in the polar plots in Figure 4-20, Figure 4-21, Figure 4-22 and Figure 4-23. The line-neutral voltage of phase 'a' forms the reference vector (cosine representation) and all phase-angles are measured with respect to this reference vector.

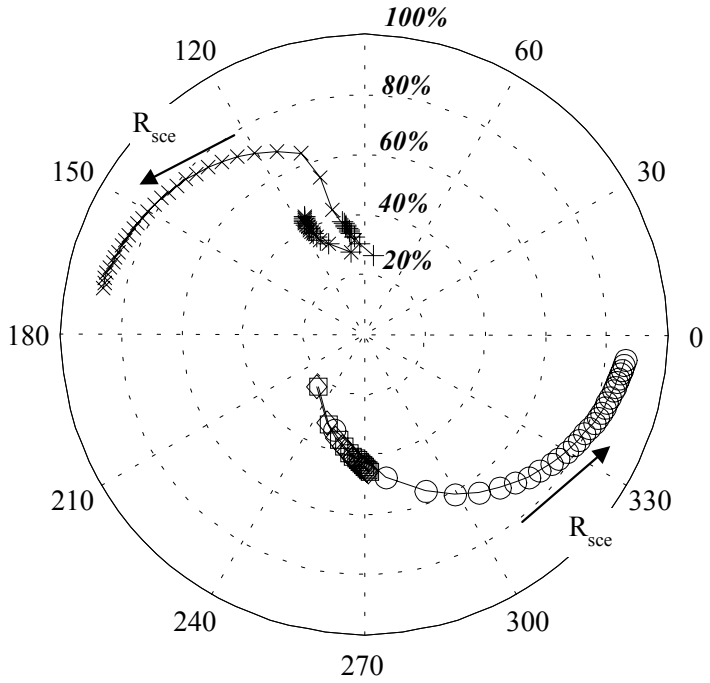


*Figure 4-20: Polar plot of the 5th harmonic current as a function of R_{sce}. R_{sce} = 20 - 600 with a step of 20. x : Basic three-phase (A), * : three-phase with L_{dc} (B), + : three-phase with L_{ac} (C), o : Basic single-phase (D), □ : single-phase with L_{dc} (E), ◊ : single-phase with L_{ac} (F).*

The 5th harmonic current of the three-phase rectifier is within the range of 90° and 170°, while the 5th harmonic current of the single-phase rectifier is within the range of 220° and 350°. The phase-angles of the 5th harmonic current for the single- and three-phase rectifier differs widely and they are often in counter phase. This means the geometrical sum of the 5th harmonic current of the three- and single-phase rectifier is always significantly less than the arithmetical sum and often a total cancellation can be obtained. Furthermore, if the only load is a large single- or three-phase rectifier load there is no cancellation of the 5th harmonic current because they are in phase.

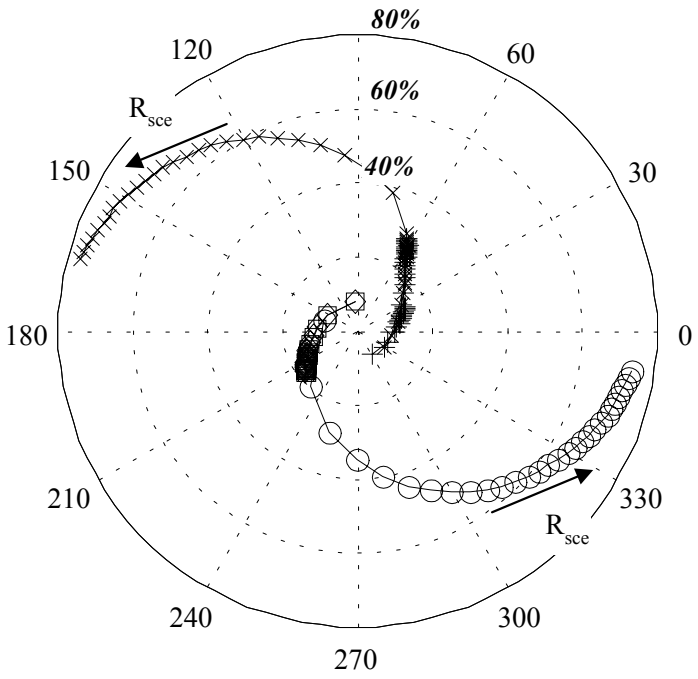


*Figure 4-21: Polar plot of the 7th harmonic current as a function of R_{sce}. R_{sce} = 20 - 600 with a step of 20. x : Basic three-phase (A), * : three-phase with L_{dc} (B), + : three-phase with L_{ac} (C), o : Basic single-phase (D), □ : single-phase with L_{dc} (E), ◊ : single-phase with L_{ac} (F).*

The 7th harmonic current of the three-phase rectifier is in the range of 300° and 170° while it is in the range of 90° and 350° for a single-phase diode rectifier. Both cancellation and summation can therefore be obtained when mixing single- and three-phase diode rectifiers depending on the short-circuit ratio. If a three-phase diode rectifier with dc-link inductance is connected to the same strong distribution line as a single-phase diode rectifier without any additional inductance, an arithmetical summation of the 7th harmonic is obtained. However, in the typical case a large number of single-phase rectifiers are without any dc-link inductance and they are connected to a weak line (long cables) and a few three-phase rectifiers with dc-link inductance are connected to a strong line (near the transformer) then the 7th harmonic currents are in counter phase.

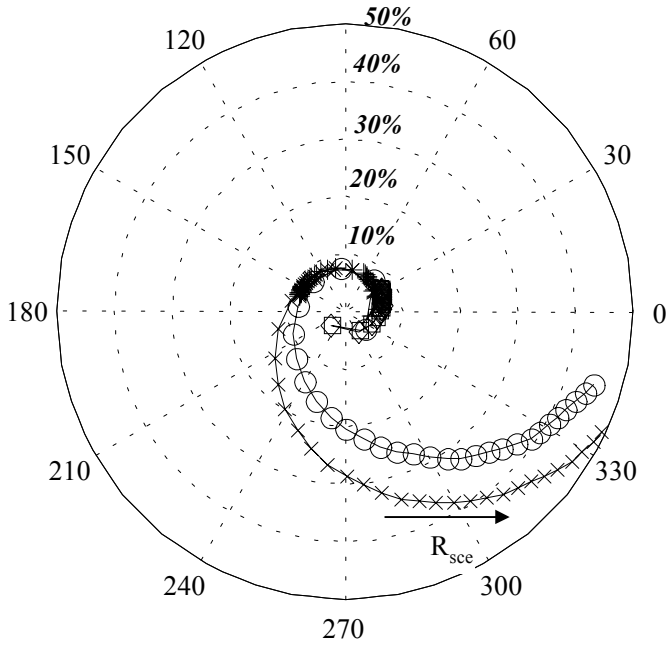


*Figure 4-22: Polar plot of the 11th harmonic current as a function of R_{sce}. R_{sce} = 20 - 600 with a step of 20. x : Basic three-phase (A), * : three-phase with L_{dc} (B), + : three-phase with L_{ac} (C), o : Basic single-phase (D), □ : single-phase with L_{dc} (E), ◊ : single-phase with* L_{ac} (F).

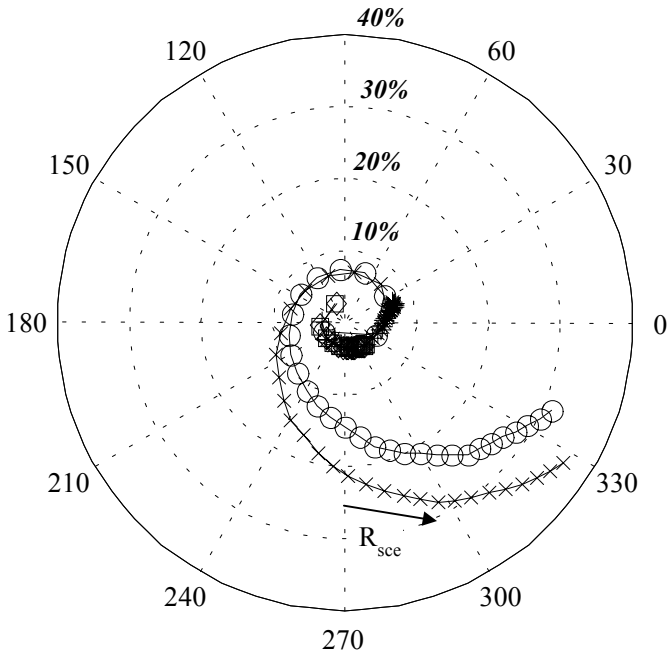


*Figure 4-23: Polar plot of the 13th harmonic current as a function of R_{sce}. R_{sce} = 20 - 600 with a step of 20. x : Basic three-phase (A), * : three-phase with L_{dc} (B), + : three-phase with L_{ac} (C), o : Basic single-phase (D), □ : single-phase with L_{dc} (E), ◊ : single-phase with L_{ac} (F).*

The 11^{th} and 13^{th} harmonic currents for both the single- and three-phase rectifiers are in the range of a complete cycle and they are therefore very dependent on the transformer impedance (and cable).

One interesting conclusion that can be made by the above simulations is that, due to the small differences of the 5^{th} harmonic phase-angle of the single-phase diode rectifier compared to the higher harmonics and the large amount of single-phase non-linear loads on the LV-line the 5^{th} harmonic voltage is the most dominating harmonic distortion on the MV-line. The phase-angle of the 7^{th} harmonic current for the single-phase rectifier differs almost 180°. This means that there is some cancellation of the 7^{th} harmonic current of single-phase rectifiers and thus the 7^{th} harmonic distortion is less dominating. The phase-angle of the 11^{th} and 13^{th} harmonic current differs so much, that there is a high possibility that there is a cancellation in the distribution line.

Also, if single-phase non-linear load is connected to a weak grid and the three-phase diode rectifier has some dc-link or additional ac-inductance the 5^{th} harmonic current is in counterphase. Since single-phase diode rectifiers are the most dominating non-linear loads in the power system, 5^{th} harmonic cancellation is expected in the power system when a three-phase diode rectifier with some dc-link or additional ac-inductance is connected to the grid. This is also recognized by the working group of the EN 61000-3-12 and therefore there are less stringent harmonic current limits to this type of equipment as shown in Chapter 2.4

Another interesting conclusion is that using an additional ac or dc-link inductance makes the amplitude and phase-angle of the harmonic current less dependent of the ac-line impedance. And the dc-link inductance of the single-phase rectifier behaves like an ac-line impedance.

4.5 Verification of the Diode Rectifier Models

So far, most simulations have been made by use of SABER. Also the analytical models are verified by the use of SABER with different short circuit ratios. To verify that the used SABER models are correct measurements are compared with some simulations in the following. The same parameters such as line-impedance, dc-link impedance etc are used for the measurements and simulations.

The measurements are made with a three-phase diode rectifier with a nominal power of 2.2 kW. The dc-link inductance is equal to 7.2 mH (3%) and the dc-link capacitor is 165 µF (26.5%). The rectifier is connected to a Static Power Generator of the type California Instrument with a nominal three-phase power of 15 kVA. The line-line voltage is 400 V and the frequency is set to 50 Hz. The Static Power Generator can be seen as a stiff voltage supply, i.e. no supply impedance (L_s= 0 µH).

Figure 4-24 shows the measured and simulated currents. Both currents of the circuit-based model simulated in SABER and the analytical model simulated in MATLAB are shown together with the measured current. Figure 4-25 shows the Fourier analysis of the currents.

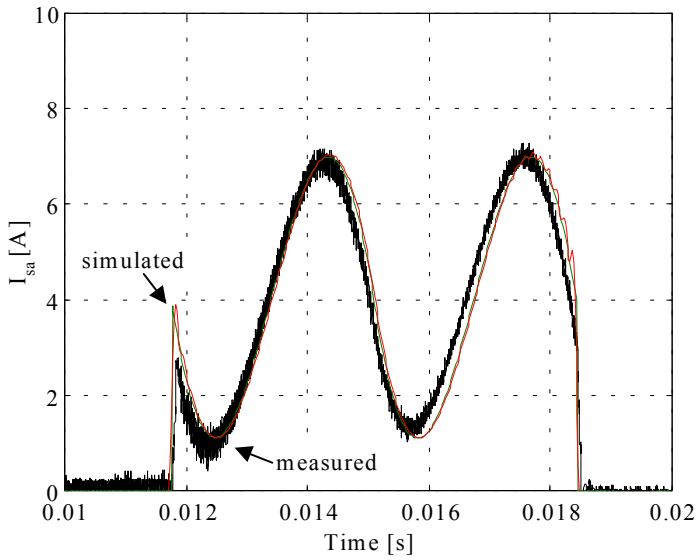


Figure 4-24: Measured and simulated line-current of the three-phase diode rectifier. Both current of SABER and the analytical-based simulations are shown together with the measured current.

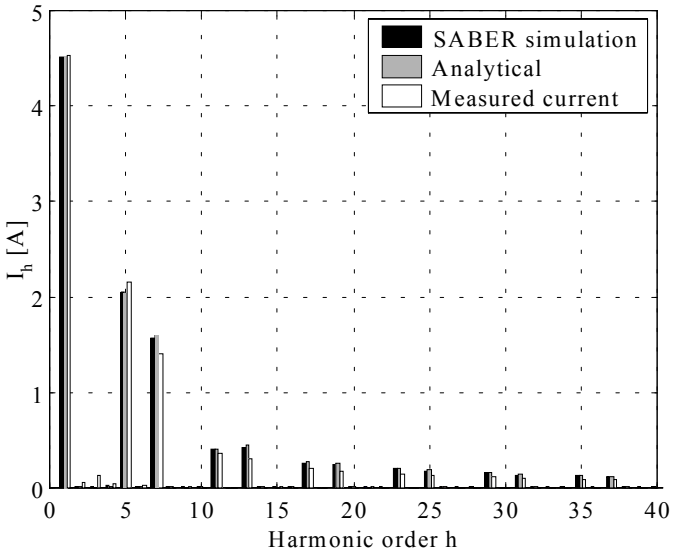


Figure 4-25: Fourier series of the measured and simulated currents.

Harmonic order h	Measured current	SABER current	Analytical current
1	4.53 A (peak)	4.52 A (peak)	4.53 A (peak)
5	2.15 A (peak)	2.05 A (peak)	2.04 A (peak)
7	1.41 A (peak)	1.57 A (peak)	1.60 A (peak)
11	0.37 A (peak)	0.41 A (peak)	0.41 A (peak)
13	0.31 A (peak)	0.43 A (peak)	0.45 A (peak)
THD_i	58.4%	59.9%	60.1%

Table 4-1: Comparison between the measured and simulated harmonic currents as well as the THD_i for a three-phase diode rectifier.

As it can be seen from Figure 4-24, there is a difference between the edges of the measured and simulated current. This indicates that the assumption that the voltage generator is a stiff voltage supply is not correct. Actually the commutation angle μ is measured to be 1.44°, which ideally should be zero as in the simulation. Knowing the commutation angle μ, L_s can be calculated by equation 4.10.

Using equation 4.10, L_s is calculated to 73 μH. Figure 4-26 shows the measured and simulated current with L_s=73 μH. Figure 4-27 shows the Fourier series belonging to Figure 4-26. It is clearly shown that the edges of both currents are almost identical. This results in that the simulated higher harmonics are closer to the measured harmonics.

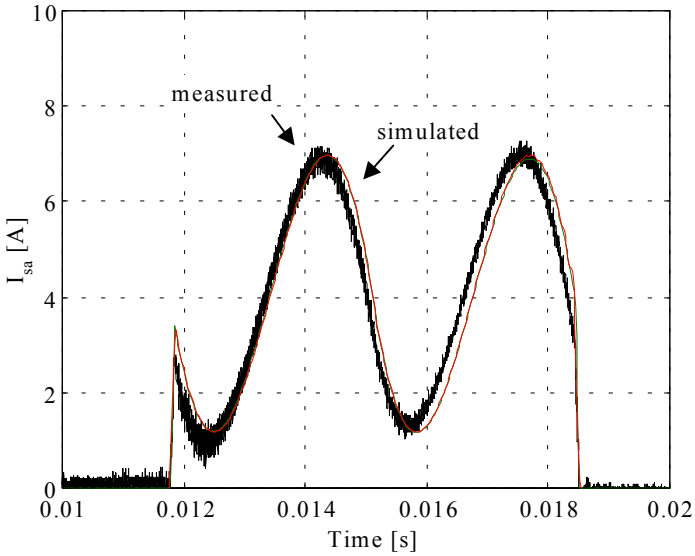


Figure 4-26: Measured and simulated line-current of the three-phase diode rectifier with L_s=73uH. Both simulations with SABER and analytical-based simulations are shown.

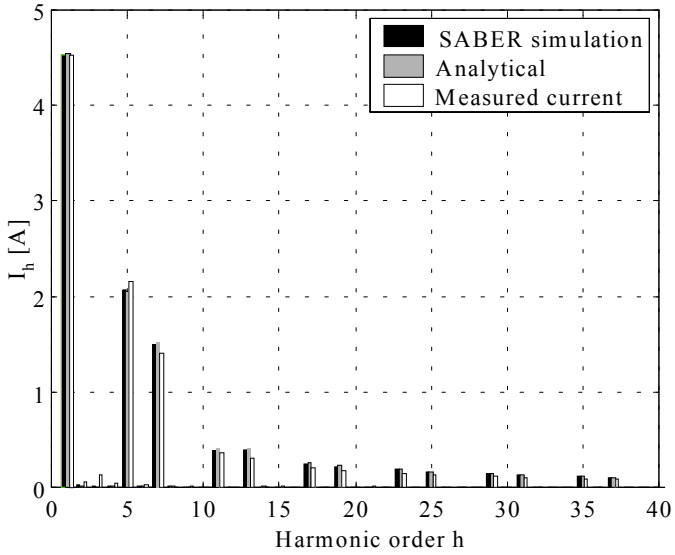


Figure 4-27: Fourier series of the measured and simulated currents.

Harmonic order h	Measured current	SABER current	Analytical current
1	4.53 A (peak)	4.52 A (peak)	4.54 A (peak)
5	2.15 A (peak)	2.06 A (peak)	2.06 A (peak)
7	1.41 A (peak)	1.50 A (peak)	1.52 A (peak)
11	0.37 A (peak)	0.40 A (peak)	0.41 A (peak)
13	0.31 A (peak)	0.40 A (peak)	0.41 A (peak)
THD_i	58.4%	58.7%	58.9

Table 4-2: Comparison between the measured and simulated harmonic currents as well as the THD_i.

The three-phase SABER diode model is now verified and it is shown that the simulated current is very close to the measured current. The three-phase SABER diode rectifier is only validated in one working point (stiff grid, nominal load). However, it is claimed here that if the three-phase SABER diode rectifier model is validated at a very strong grid, as shown above, the model will also be correct at other working points. A strong grid is assumed to be worst-case for validation of the diode rectifier, because here the dc-link voltage ripple will be worst, and the diode rectifier parameters have most influence. Also measurements of a single-phase diode rectifier seem unnecessary, because of the commutation between the phases the three-phase diode rectifier is more complicated to model correctly. On a weak grid, the line impedance becomes very important. It should be noted here, that modelling the line impedance could become difficult because the exact harmonic impedance normally is unknown.

4.6 The Diode Rectifier at Non-Ideal Conditions

As mentioned in the start of this chapter, the harmonic currents of the diode rectifier are also depending on other parameters than the short circuit power, such as the load and supply voltage quality. How does the diode rectifier behave under unbalanced and pre-distorted grid? To simulate all variations of unbalance and pre-distortion on the supply voltage would be a boundless task. However, it is important to determine how much the harmonic currents differ from the harmonic current with sinusoidal voltage. This gives an idea on what level of accuracy one can expect when comparing calculations/simulations based on ideal conditions with measured values. (Here ideal conditions are very unlikely!)

4.6.1 The three-phase diode rectifier with pre-distorted voltage

Figure 4-28 shows six measured line currents from the same three-phase diode rectifier, connected to a static voltage generator supplying sinusoidal voltage distorted with 3% 5^{th} harmonic voltage. The conditions such as load etc. for the measured currents were the same, the only difference is the phase-angle of the 5^{th} harmonic voltage.

In the shown measurements the phase-angle of the 5^{th} harmonic voltage is varied with 60° (0° - 360°). The result is quite surprising. As shown in Table 4-3 the THD_i is actually varying from 40% to 80%.

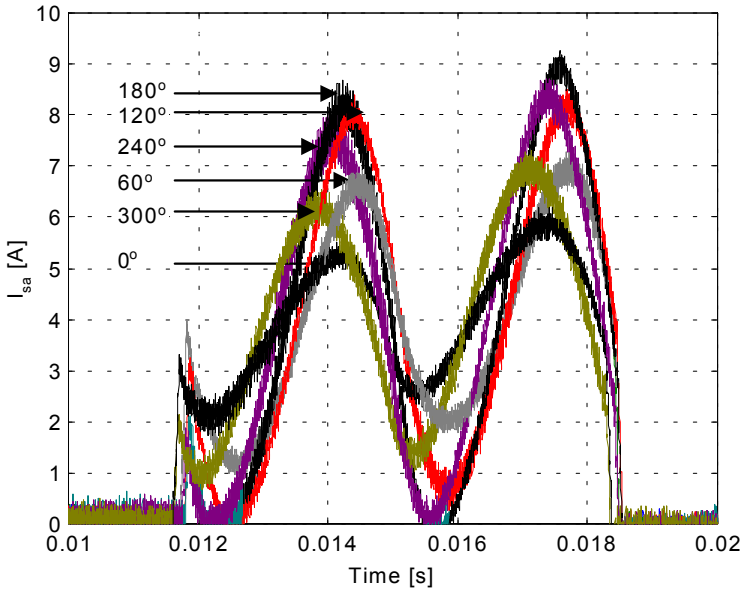


Figure 4-28: The line current of a diode rectifier with 5th harmonic pre-distorted voltage with varying phase-angle.

	0°	60°	120°	180°	240°	300°
THDi [%]	40	55	73	80	73	55
I_5 [%]	33	39	56	65	61	48
I_7 [%]	17	33	44	45	39	24
I_{11} [%]	8	11	11	9	6	5
I_{13} [%]	6	9	9	7	6	5

Table 4-3: The THD_i, 5th, 7th, 11th and 13th harmonic current of a diode rectifier with 5th harmonic pre-distorted voltage with varying phase-angle.

As shown above the harmonic current is very depending of the phase-angle of the 5th harmonic voltage. This gives an indication of how sensitive the diode rectifier is with respect to pre-distorted voltage and it can therefore be difficult to predict the harmonic current of a diode rectifier even in a well-known system in general.

4.6.2 The three-phase diode rectifier with different loads

Another important aspect is the harmonic current distortion as a function of the load. Figure 4-29 shows the THD_i, the relative and absolute values for the 5th and 7th harmonic current as a function of the load.

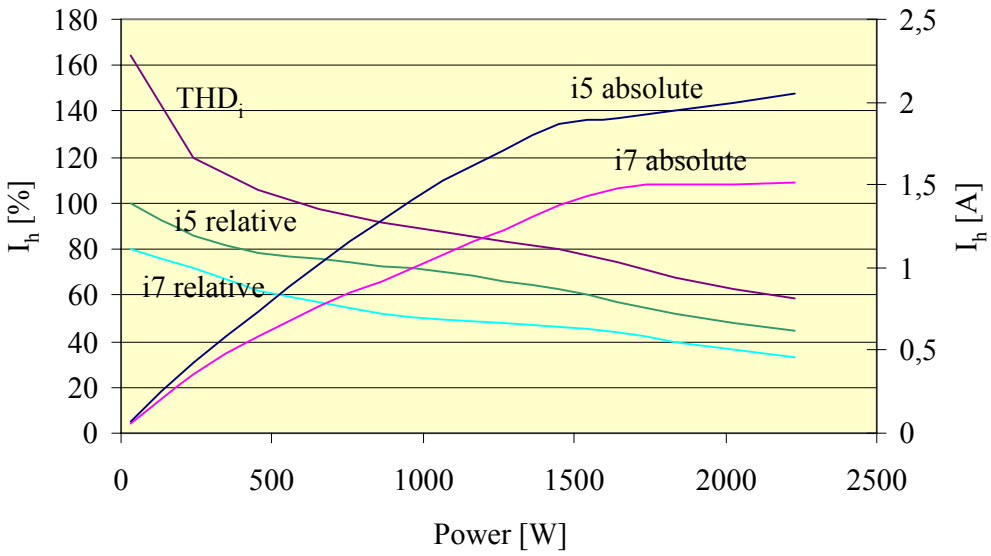


Figure 4-29: THD_i, the relative and absolute values for the 5^{th} and 7^{th} harmonic current as a function of the load.

As expected the absolute values for the 5th and 7th harmonic are decreasing as a function of the load. The interesting thing to be noted is that the THD_i and the relative values for the 5th and 7th harmonic currents are increasing. Thus, the harmonic currents of the diode rectifier are decreasing less as a function of the load than the fundamental current. The fundamental current is decreasing linear with the load (of course). Also it is interesting to note that above 1500 W, where the line-current is continuous, the 5th and 7th harmonic current are decreasing less than in the discontinuous mode (below 1500 W). The 5th and 7th harmonic is actually almost constant in the continuous mode.

4.7 Conclusion

In this chapter four levels of the diode rectifier models have been presented. Furthermore, the behavior of the diode rectifier at some different basic parameters such as the line-impedance and line voltage has been documented.

The ideal model of the diode rectifier has been reviewed and it is shown that the ideal model only is useful for some basic calculations. Also a table based diode rectifier models is presented and it was shown that the harmonic currents are highly depending of the line impedance. Only the short circuit ratio is needed as input to find the total harmonic current distortion (THD_i) and the harmonic constant (Hc) that very well can be used to determine the total harmonic voltage distortion (THD_v) as described in chapter 3.1. Furthermore, an analytical model for both the single- and three-phase diode rectifier was presented and very good accuracy was achieved.

By use of the numerical circuit simulator SABER it is shown that the phase-angle of the 5th harmonic current is mostly depending on the rectifier type (i.e. single-phase or three-phase) and almost independent of the line impedance. Due to the small differences of the 5th harmonic phase-angle of the single-phase diode rectifier compared to the higher harmonics and the large amount of single-phase non-linear loads on the LV-line the 5th harmonic voltage is the most dominating harmonic distortion on the MV-line. The phase-angle of the 7th harmonic current for the single-phase rectifier differs almost 180°. This means that there

is some cancellation of the 7th harmonic current of single-phase rectifiers and thus the 7th harmonic distortion is less dominating. The phase-angle of the 11th and 13th harmonic current differs so much, that there is a high possibility that there is a cancellation in the distribution line.

It is also shown that the 5th harmonic current of the three-phase diode rectifier often is in counterphase with the 5th harmonic current of the single-phase diode rectifier. And because the single-phase didoe re4ctifier is the dominating nonlinear load 5th harmonic cancellation is expected in the power system when a three-phase diode rectifier is connected to the grid. This is also recognized by the working group of the EN 61000-3-12 and therefore there are less stringent harmonic current limits to this type of equipment.

From the discussed diode rectifier models it can be concluded that even though circuit based simulators are best suited for simulation of harmonic currents especial under non-ideal voltage conditions, the analytical models have an advantages with respect to required CPU power. The analytical models may therefore be well suited for calculations where parameters such as voltage background distortion are not exactly known, e.g. in a general harmonic calculation toolbox.

Finally, it was shown that the current of a diode rectifier is depending on several other parameters besides as the supply impedance and dc-link impedance. The voltage quality and the load of the rectifier are shown to have a significant impact on the harmonic currents generated. This is important to know because this shows the limitations of the analytical and table-based models of the diode rectifier. It is recommended to use numerical simulators to predict the harmonic current distortion of the diode rectifier at non-ideal conditions. However, this requires detailed knowledge of all system parameters such as phase-angel of background distortion dc-link inductance etc.

Table 4-4 shows a comparison of the different models presented in this chapter.

Diode rectifier Models	No. of Parameters	CPU	Precision	Comments
Ideal	+	++	-	Only useful for basic calculations
Ideal with Commutation	o	+	-	Not for single-phase diode rectifiers
Table based	o	+	o	The number of parameters and the precision is depending on the effort put into the table.
Accurate Analytical	-	o	+	Analytical expressions for the diode rectifiers are not used so far for harmonic analysis, but can be the future tool, because of good precision/simulation-speed ratio.
Circuit based	-	-	++	Circuit based simulators are the “State of the Art tool” for precise harmonic analysis. Also useful for analysis under non-ideal voltage conditions

Table 4-4: Comparison of different diode rectifier models.

5. High Power Factor Three-Phase Rectifiers

A large number of rectifier topologies are known to reduce the line-side harmonic currents compared to the basic diode rectifier and the amount of papers dedicated to the different harmonic reduction techniques is enormous for both single- and three-phase rectifiers. All these topologies cannot be covered in this thesis. As mentioned in Chapter 1, the focus of this thesis is on medium power (1-500 kW) three-phase rectifiers especially for use in ASD's. However, some recommendable reviews on single-phase rectifiers can be found in [Sebastian et al. 1994], [Salmon 1993] and on low-power three-phase rectifier in [Kolar, Ertl 1999] [Mao et al. 1997].

Some requirements that must be fulfilled to qualify for a three-phase rectifier used for ASD's are:

- No significant increase in the dc-link voltage compared to the diode rectifier, because higher dc-link voltage warrants redesign of the PWM inverter
- The operation of the rectifier should be independent of the line impedance
- No additional components in series with the power flow path should be used, due to increased losses
- Bi-directional power flow is normally not necessary. However, in some applications (high performance with frequent acceleration and deceleration) this may be an advantage
- Electrical isolation between the utility input and the output of the power electronic converter is not needed

The most popular harmonic reduction techniques for the three-phase rectifier can be classified as shown in Figure 5-1. The classification presented is divided into system level harmonic reduction technique and equipment level harmonic reduction.

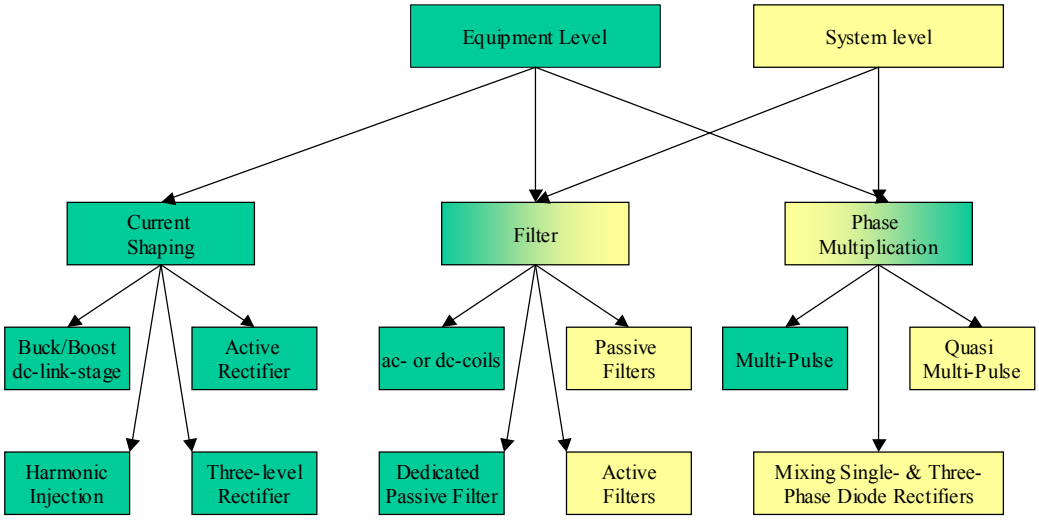


Figure 5-1: Classification of three-phase diode rectifiers for harmonic reduction techniques.

The most useful topologies for ASD's are presented in this chapter along with simulations and some experimental results. The main purpose of this chapter is to estimate the performance of these topologies with respect to harmonic currents. Also advantages and

disadvantages need to be revealed in order to find a realistic alternative for the diode rectifier in applications where the harmonic distortion is critical.

Following topologies are selected to qualify for three-phase apparatus level rectifier for ASD's and they are covered in this chapter. Some selected system level topologies are covered in Chapter 6.

- *Built-in dc-coils:* Built-in dc-coils or additional ac-inductance is probably the most used harmonic reduction technique for ASD's. Therefore, this topology is reviewed in this chapter. That additional inductance reduces the harmonic current distortion is proven in Chapter 4. However, in Chapter 4 no numbers for the optimal inductance is given. Therefore, a guide for designing the dc-link of an ASD for adequate harmonic performance is presented in this chapter. However, since this is a well-known topology the harmonic performance is only discussed by simulations.
- *Multi-pulse rectifiers:* Multi-pulse rectifiers are also a well-known topology and are well documented in textbooks [Paice 1996] and technical papers [Choi et al. 1996 (a)], [Rendusara et al. 1996]. Furthermore, the multi-pulse rectifiers are often used in ASD's. The basic multi-pulse theory is therefore reviewed and two different topologies are discussed. Finally, to estimate the harmonic performance of this topology some simulations are presented.
- *Active rectifier:* The active rectifier is by many, especially by academia, considered to be the most obvious alternative to the diode rectifier in the near future and there is a lot research activity going on in this field, Therefore a more in-depth analysis of the active rectifier is presented in this chapter compared to the analysis of the topologies described above. Basic control strategies are reviewed and a novel line-voltage estimator is presented. Both simulations and experimental results are used to determine the harmonic performance. Furthermore, future perspectives and necessary future work are discussed.
- *Third harmonic injection scheme:* A new integrated single-switch approach to improve the harmonic performance of a standard ASD based on the idea of circulating a third harmonic current is proposed. Since this is a new topology some basic analysis are presented and both simulations and experimental results are shown.

There are other high power factor rectifier topologies that do not qualify for ASD applications in the medium power range. These topologies are not discussed here.

5.1 Built-In dc-Link Inductance

Adding ac- or a dc-link inductance seems like an obvious method to reduce the harmonic currents compared to a basic three-phase diode rectifier without any additional inductance. In Chapter 4 it is proven that the line impedance L_s, an additional ac-inductance L_{ac} or a built-in dc-link inductance L_{dc} as shown in Figure 5-2 reduces the harmonic currents of the diode rectifier significantly. This section focuses therefore on the design of the three-phase diode rectifier to achieve adequate harmonic performance with respect to the future European norm EN 61000-3-12.

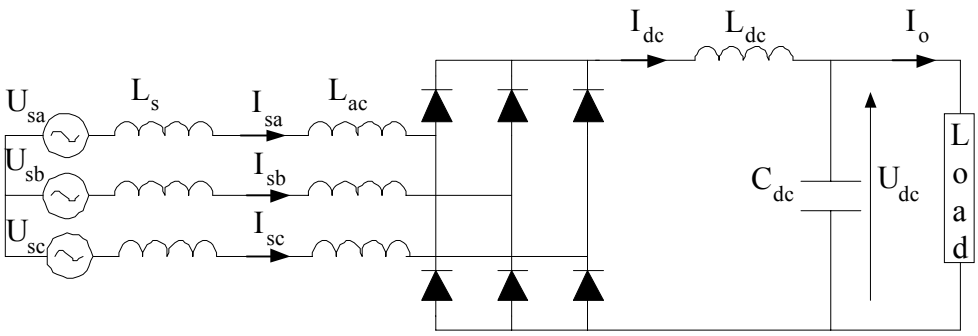


Figure 5-2: The three-phase diode rectifier with a (built-in) dc-link inductance and additional ac-inductance.

Basically, the ac- and dc-inductance work the same way. The additional inductance limits the peak currents and this results eventually in continuous current in the dc-link and, hereby, lowers the harmonic content in the line current. However, the dc-link inductance exhibits a number of advantages compared to the ac-inductance and should therefore be preferred:

- Lower losses due to less hysteresis losses
- Higher dc-link voltage due to no commutation voltage drop
- More compact design compared to the ac-inductance

[Kelley, Yadusky 1992] have investigated the effect of a dc-link inductance of both the three-phase and single-phase diode rectifier with respect to different harmonic related factors. However, [Kelley, Yadusky 1992] assumed a near infinite dc-link capacitor and no ac-line impedance. Also the importance of PWHD with respect to the future European norm EN 61000-3-12 was not yet recognized. In this section a guide similar to [Kelley, Yadusky 1992] is presented for designing the dc-link inductance for a three-phase diode rectifier with respect to the harmonic line currents. Furthermore, the influence of the dc-link capacitor is investigated which results in a design with different combinations of dc-link inductance and capacitor values to comply with the EN 61000-3-12.

5.1.1 Design of the dc-link inductance

In the following a near infinite dc-link capacitor and no line impedance is assumed. Also the capacitor and inductors are linear and loss-less. Under these circumstances the harmonic line currents are determined only by the dc-link inductance. Figure 5-3 and Figure 5-4 shows the individual harmonic currents and the harmonic distortion factors as a function of the dc-link inductance.

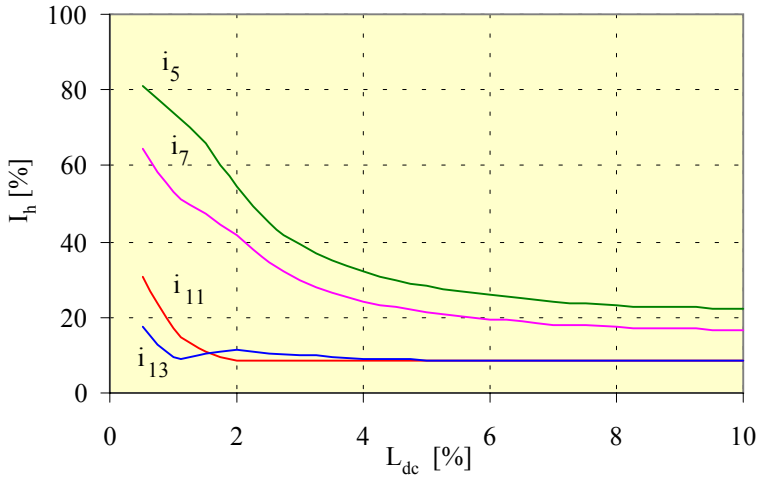


Figure 5-3: The individual harmonic currents as a function of the dc-link inductance.

As expected Figure 5-3 shows that increasing the dc-link inductance decreases the harmonic currents. From 0.5% to 3% the harmonic currents decreases rapidly, while the harmonic currents decrease less in the range from 3% to 6%. If the dc-link inductance is above 6%, the harmonics are almost constant. From the results given in Figure 5-3 one could argue that the optimal value for the dc-link inductance is in the area of 3% – 6%. Here the most harmonic reduction is gained with the least effort (read value of dc-link inductance).

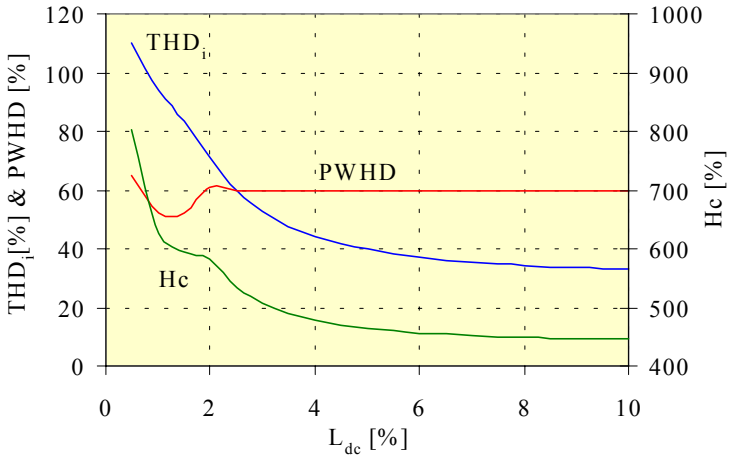


Figure 5-4: The harmonic distortion factors as a function of the dc-link inductance.

While the picture is the same for the THD_i as for the individual harmonic currents it is somewhat different for the partial weighted distortion factor and the harmonic constant as shown in Figure 5-4. The PWHD has a local minima at L_{dc} = 1.5% and the Hc is more or less constant at L_{dc} = 1% to 2%. The reason for this is the transition from discontinuous (DCM) to continuous mode (CCM) as described in Chapter 4.2. In this particular range of L_{dc}, (DCM II), the commutation between the diodes starts, while the current is still discontinuous. Since there is no ac-impedance the current commutates instantaneously and the rapidly rise in the line current results in increased higher harmonics. Therefore the PWHD is increasing in this range of L_{dc} and becomes constant in the CCM where the commutation is not changing.

One possible design goal is to be within the limits set by the EN 61000-3-12 for balanced three-phase equipment with given phase-angle conditions as shown in Table 5-1. The design presented here is made for a short circuit ratio of 120 or more.

Minimal R_{sc}	Admissible individual harmonic current I_h / I_1%				Admissible harmonic current distortion factors%	
	I_5	I_7	I_{11}	I_{13}	THD	PWHD
33	10.7	7.2	3.1	2	12	28
≥120	40	25	15	10	48	45

Table 5-1: Harmonic current limits for balanced three-phase equipment with given phase-angle conditions of EN 61000-3-12 stage 2.

As seen by Figure 5-3, Figure 5-4 and Table 5-1 the individual harmonic currents and the THD_i are within the limits at L_{dc} larger than 4%. Actually with I_7 = 25% this is the design giving factor. However, even the lowest PWHD is above the limit of 45% and a further increase of L_{dc} will not result in a lower PWHD, since the commutation is not affected. So for designing the three-phase diode rectifier within the harmonic current limits of EN 61000-3-12 it is necessary to limit the rise of the current at the commutation by adding an additional ac-inductance or to determine the maximum short circuit ratio at which the rectifier is allowed to be connected.

Recognizing that the PWHD is only limited by the ac-impedance, this becomes the design giving parameter. Adding an additional ac-impedance of 0.3% limits the PWHD to 45% as required by EN 61000-3-12. An ac-impedance of 0.3% corresponds to a short circuit ratio of 333. However, the increased ac-impedance has also influence on the other harmonics, therefore a smaller dc-link inductance can be used instead of 4%. Simulations with an ac-impedance of 0.3% and a dc-link inductance of 3% results in:

R_{sc}	I_5	I_7	I_{11}	I_{13}	THD	PWHD
333	38.8	23.2	8.8%	6.7%	47.6%	43.8%

So using a 3% dc-link inductance and additional 0.3% ac-inductance the three-phase diode rectifier is within the limits of EN 61000 - 3 – 12 (assuming a short circuit ratio above 120). Unfortunately, this is only true when a near infinite dc-link capacitor is used.

5.1.2 Influence of dc-link capacitor

When designing the three-phase diode rectifier into certain harmonic limits such as the EN 61000-3-12 as shown above, the dc-link capacitor needs special attention. As shown in Figure 5-5 and Figure 5-6 the size of the dc-link capacitor becomes important. The smaller the dc-link capacitor becomes, the higher the harmonic currents. Here the simulation is made with a 3% dc-link inductance and a short circuit ratio of 333 (thus no additional ac-inductance is needed).

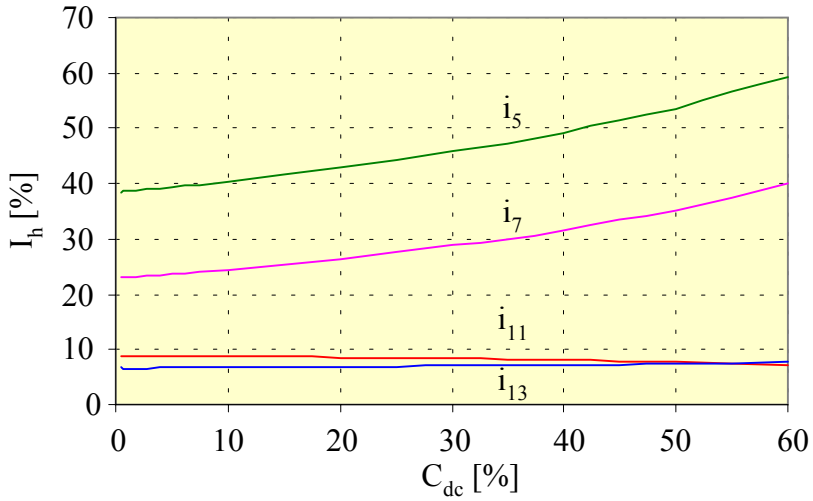


Figure 5-5: The individual harmonic currents as a function of the dc-link capacitance with R_{sce} = 333 and L_{dc} = 3%.

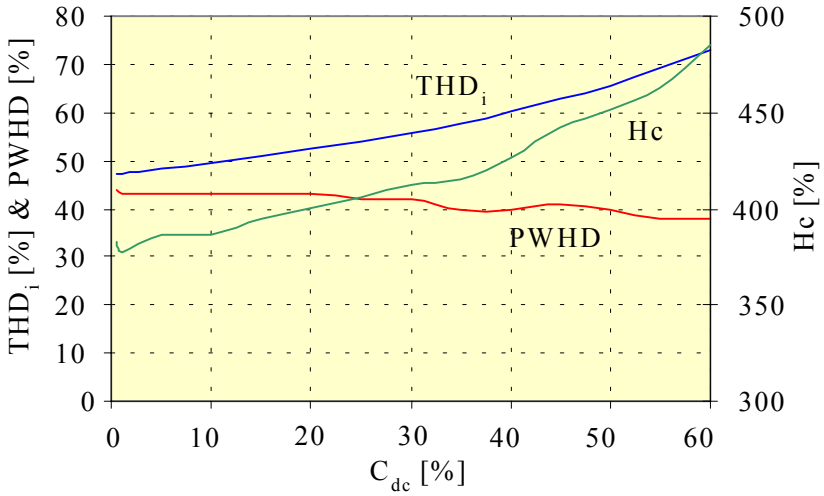


Figure 5-6: The harmonic distortion factors as a function of the dc-link capacitance with R_{sce} = 333 and L_{dc} = 3%.

It becomes clear that for complying with EN 61000-3-12 a realistic value for the dc-link capacitor needs to be found, before the optimal value for the dc-link inductance can be determined. However, mechanical aspects such as space, cooling etc. are quite critical in apparatus design, therefore it is necessary to find a number of possible combinations that will comply with EN 61000-3-12. Assuming a short circuit ratio of 333, the design giving parameters becomes the THD_i. Figure 5-7 shows the THD_i as function of both the dc-link capacitor and the dc-link inductance at a short circuit ratio of 333.

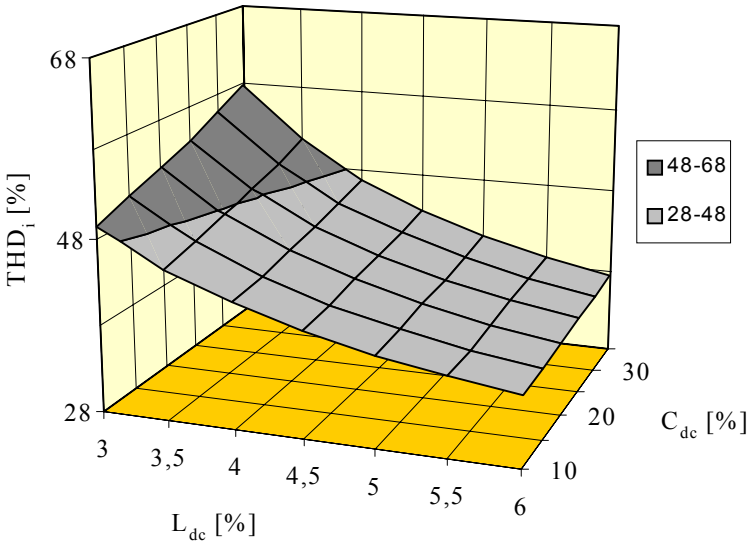


Figure 5-7: The THDi as a function of the dc-link capacitor and dc-link inductance with R_{sce} = 333.

Selecting a dc-link inductance of more than 4% always ensures a THD_i less than 48% for a capacitor size less than 35%. Selecting a dc-link inductance of 3.5% the dc-link capacitor needs to be less than 20%, while it is not possible to be within the limits with a dc-link inductance of 3% and a reasonable sized dc-link capacitor.

5.1.3 Conclusion

Compared to the basic diode rectifier a significant reduction of the harmonic currents can be obtained by introducing a 3% - 6% dc-link inductance. The final size of the dc-link inductance should be considered as a function of the dc-link capacitor value and the required harmonic performance. Above, a design example is shown to comply with the EN 61000-3-12. It was also shown that a maximum short circuit ratio of 333 is required to comply with the PWHD limit of the EN 61000-3-12. The ac line-impedance or an additional 0.3% ac inductance attenuates especially the higher harmonics because the line-impedance limits the rise of the current during the commutation. It should be noted, that the PWHD and Hc-value is highly depending on the line impedance.

Based on the analysis of above a THD_i = 30% - 50% and Hc = 150% - 400% is considered as a realistic harmonic performance of the 6-pulse rectifier with built in dc-link inductance.

5.2 Multi-Pulse Converters

Multi-pulse (especially 12-pulse) rectifiers are frequently used today to reduce the harmonic line currents of ASD's. This section has the intention to estimate the harmonic performance of the multi-pulse topology and to reveal the advantages and disadvantages. Therefore, some simulations are presented both for sinusoidal voltage and pre-distorted grid.

Several converter topologies suited for multi-pulse exists and there exist even more transformer arrangements to supply the necessary phase-shifts [Paice 1996]. However, not all known topologies are considered here. The main focus in this section is on the converter topologies in order to give a short and precise description on existing multi-pulse

topologies. Where it is appropriate, the transformer arrangement is mentioned. Also most multi-pulse topologies operate similar and the only difference is the winding arrangement of the transformer(s) used. For the matter of the transformer this is normally a question of kVA-rating and price rather than performance.

5.2.1 General multi-pulse theory

In general the line current harmonics of the diode rectifier can in general be expressed as:

$$h = (np \pm 1), \qquad n = 1, 2, 3, \ldots\ldots \qquad p = \text{Pulse number} \tag{5.1}$$

Where the pulse number is defined as the number of non-simultaneous commutations per period.

The input current of a 6-pulse diode rectifier has therefore 5^{th}, 7^{th}, 11^{th}, 13^{th} etc. harmonic components, while the harmonic components of a 12-pulse diode rectifier are: 11^{th}, 13^{th}, 23^{rd}, 25^{th} etc. Normally, the 5^{th} and 7^{th} harmonic currents of a 6-pulse rectifier are the most dominating ones. Because the 12-pulse topology ideally eliminates the 5^{th} and 7^{th} harmonic components the harmonic current distortion is significantly reduced compared to a 6-pulse rectifier. The input current harmonics of a 18-pulse rectifier have ideally 17^{th}, 19^{th}, 35^{th}, 37^{th} etc. components. These rectifiers are normally considered as clean power converters, because the THD_i is less than 5% under normal operating conditions.

To obtain multi-pulse performance a minimum of two 6-pulse converters (12-pulse) must be supplied from voltages with different phase-shifts. A possible 12-pulse configuration with one phase-shifting transformer is shown in Figure 5-8.

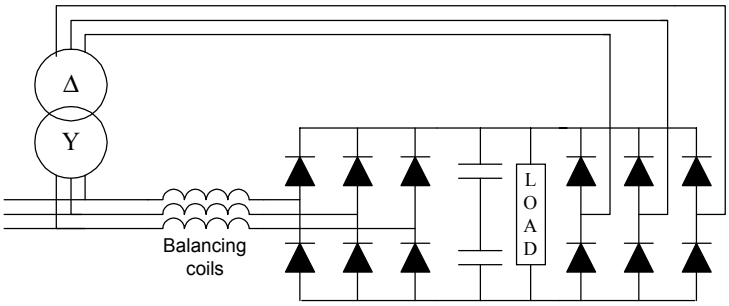


Figure 5-8: 12-pulse configuration with one transformer.

A 12-pulse configuration requires a phase-shift of 30°. The reason for this is easiest explained by Figure 5-9. Considering two voltages with a phase-shift of 0° ($u_{1,0}$) and -30° ($u_{1,-30}$) respectively. For our convenience the 5^{th} harmonic currents ($i_{5,-30}$, $i_{5,0}$) are in phase with the respective voltages. This leads to that the phase-shift between the 5^{th} harmonic currents is -150° as shown in Figure 5-9. If $u_{1,-30}$ is shifted to 0°, 30° must be added. However, the 5^{th} harmonic is a negative sequence current, therefore the 5^{th} harmonic current is phase-shifted -30° and the total phase-shift between the two 5^{th} harmonic currents becomes -180° and total cancellation can be obtained.

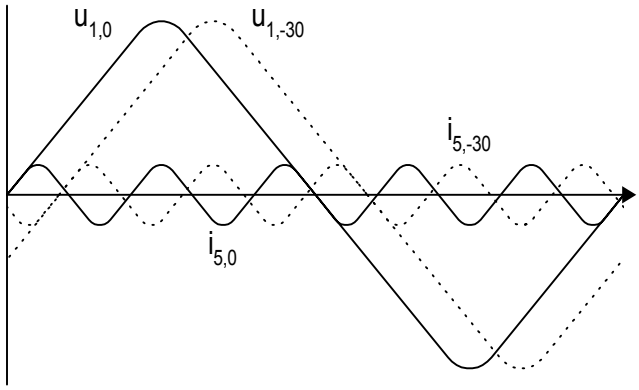


Figure 5-9: A phase-shift of 30° on the fundamental results in a 150° phase-shift on the 5th harmonic.

The same considerations can be made for the 7th harmonic current. The phase-shift between the currents is -210°. The 7th harmonic is a positive sequence current and a phase-shift of 30° results in a total phase-shift of 180°.

The required phase-shift can be calculated as a function of number of six-pulse converters used.

$$phaseshift° = \frac{60}{number\ of\ converters} \tag{5.2}$$

According to equation 5.2 a 12-pulse configuration requires a phase-shift of 30°, a 18-pulse configuration 20° and 24-pulse configuration requires a phase-shift = 15°.

5.2.2 Serial multi-pulse

One possible multi-pulse rectifier is the serial multi-pulse rectifier. The serial multi-pulse rectifier works independent of the pulse number and therefore only the 12-pulse serial multi-pulse rectifier is considered in the description below.

The serial 12-pulse topology consists of a series coupling of two 6-pulse converters and thus galvanic isolation is required for these two converters. It should be noted that this requirement makes it impossible to use an auto-transformer and therefore limits the number of possible transformer arrangements. The three winding arrangement shown in Figure 5-10 with a star/star and star/delta is an obvious arrangement. In the case of the three-winding transformer the total kVA-rating of the transformer is 100%.

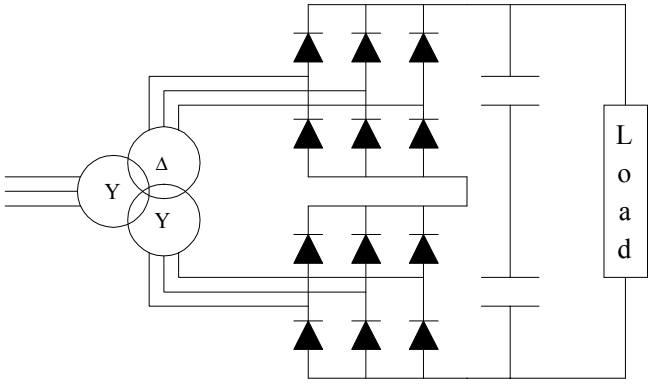


Figure 5-10: Serial 12-pulse rectifier with a star/star and star/delta three winding transformer.

The biggest advantage of the serial 12-pulse topology is that the series connection is not sensitive to pre-existing voltage distortion and voltage unbalance [Paice 1996]. Furthermore, the voltage across the two 6-pulse converters is half of the dc-link voltage. Besides the large transformer kVA-rating the disadvantage is that the diodes of both converters are rated for full current. And because all the output current is flowing through both converters the efficiency is less than for a 6-pulse diode rectifier.

The serial 12-pulse rectifier is seldom used for ASD's in the medium power range (up to 500 kW) because of the bulky transformer and that the diodes of both converters are rated for full current. However, in medium voltage and high voltage applications the serial 12-pulse rectifier is quite popular because the voltage across the two 6-pulse converters is half of the dc-link voltage.

5.2.3 Parallel multi-pulse

Basically, the parallel multi-pulse topology is just as simple as the serial multi-pulse. Unfortunately, there are some design considerations, which makes a proper and easy design a challenge. These considerations have a major impact on the harmonic currents generated and are therefore addressed in this section. The description of the parallel multi-pulse topology is limited to the 12-pulse parallel rectifier because the principle of operation is similar to 18- or 24- pulse parallel rectifiers.

The parallel 12-pulse topology can ideally be build like sketched in Figure 5-11 with the use of only one transformer. Because each 6-pulse converter only conducts half the load current the current rating of each 6-pulse converter is only half the current rating compared to a 6-pulse rectifier or each converter of a serial 12-pulse rectifier. Therefore, the efficiency may be expected higher than in a 12-pulse serial connection.

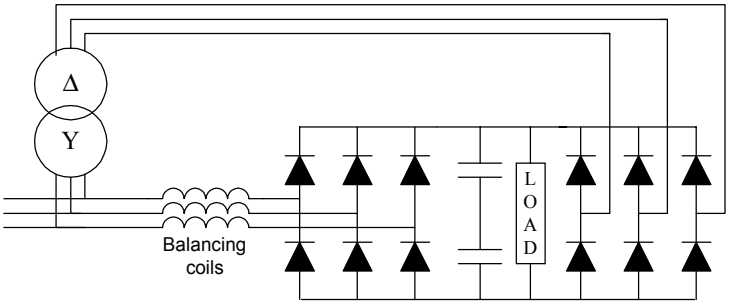
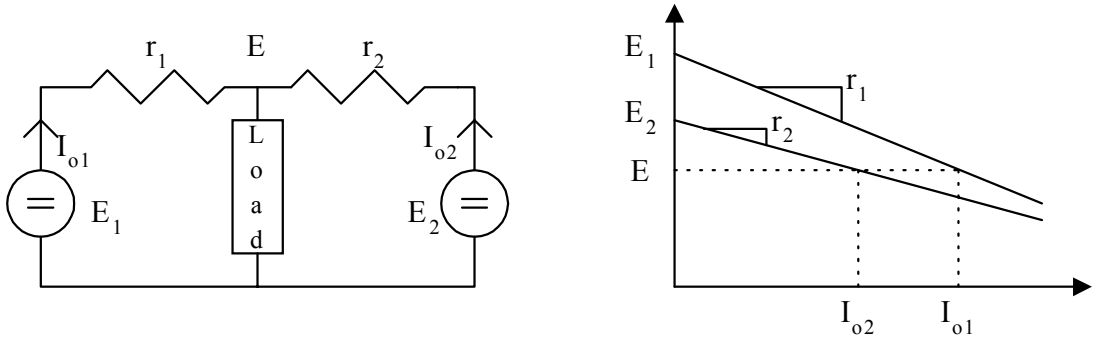


Figure 5-11: The 12-pulse parallel topology with only one transformer.

The main problem of the parallel 12-pulse rectifier is that for optimal performance the two converters must share the current equally. Only when the current is shared equally true 12-pulse performance can be achieved (i.e. no 5^{th}, 7^{th} etc harmonics). The problem is illustrated in Figure 5-12.

Two dc-voltage supplies are feeding a common load. If I_{o1} and I_{o2} have to be equal, E_1 and E_2 as well as the resistors r_1 and r_2 have to be equal. In Figure 5-12 E_1 is higher than E_2, which results in a large difference between the 2 currents.



(a) (b)

Figure 5-12: (a) Schematic diagram of two parallel dc-voltage sources feeding a common load. (b) unequal current sharing caused by unequal dc-voltage.

In the case of Figure 5-11, with only one transformer, there should be added extra reactance to the 6-pulse rectifier without a transformer. This extra reactance (balancing coils) should equal the leakage reactance of the transformer. However, only adding balancing coils to ensure equal current sharing is not recommended. To ensure some degree of equal current sharing even under non-ideal conditions a center tapped current transformer, the so-called inter-phase transformer (IPT), is put into the dc-link as explained in the following.

Inter-phase transformer

The inter-phase transformer is a center tapped current transformer where the primary and secondary side have equal number of windings. Ideally, for the flux to be zero, both currents have to be equal.

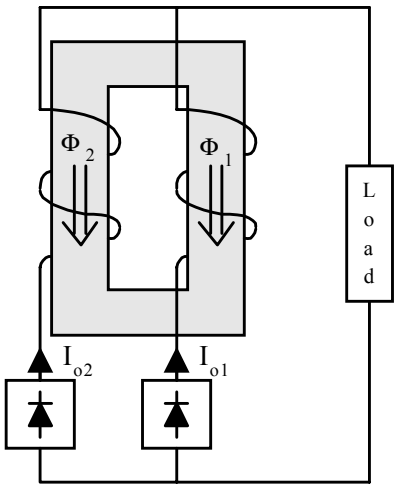


Figure 5-13: Simple sketch of an IPT for two parallel converters.

The terms inter-phase reactors, spanning reactors and current balancing transformers have also been used to describe the device. But the term transformer gives a better idea of the difficulties of designing this device. E.g. the magnetizing current of the transformer influences the rectifier input current resulting in an increased input current distortion. Also the dc-load current tends to saturate the core, resulting in an increased magnetizing current [Paice 1996].

By introducing the IPT some of the current sharing problems can be solved, but because the inter-phase transformer is an ac-device unequal current sharing caused by unequal dc-voltage output of the two rectifiers cannot be solved. Basically the IPT is only ensuring equal ripple current of both converters. Therefore, the voltage drop of both rectifiers needs still to be equal. This includes the voltage drop of the diodes as well as the voltage drop of the transformer/balancing coils.

One of the biggest advantages of the parallel multi-pulse topology is the possibility to use autotransformers. The advantage of using an autotransformer is a significant lower transformer kVA-rating. The number of possible configurations is almost endless and describing all of them is out of the scope of this thesis. Some auto-transformers especially designed for 12-pulse applications have the same amount of leakage inductance for both converters for obvious reasons. An example of such an often used 12-pulse autotransformer is shown in Figure 5-14. The transformer kVA-rating is only 18% [Choi et al. 1996 (a)].

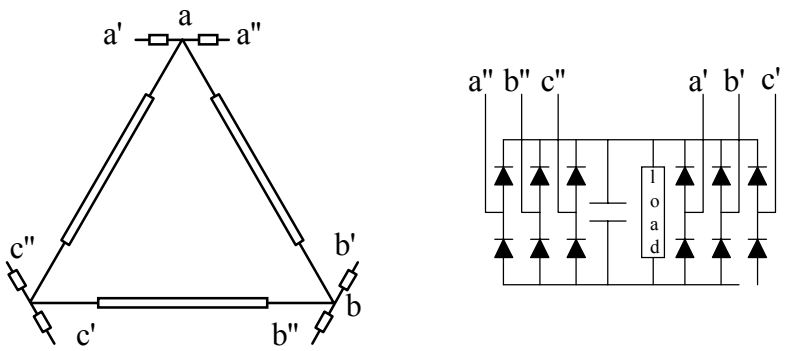


Figure 5-14: Example of an auto-transformer 12-pulse configuration.

Because there is no galvanic isolation there are some additional problems arising with the use of an autotransformer that needs to be addressed.

Zero sequence blocking transformer

In the case of an autotransformer, the two rectifiers are not galvanic isolated. Therefore, unwanted conduction passes can occur so that the independent operation of the two rectifiers is not ensured.

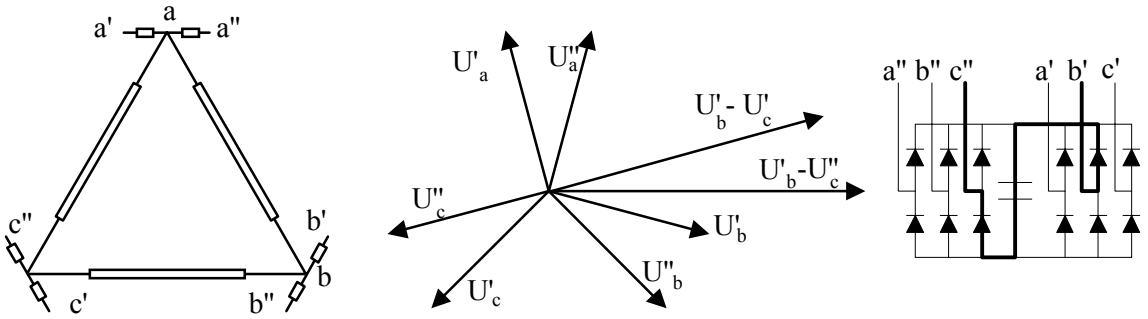


Figure 5-15: The vector diagram of a two-voltage system of a autotransformer with a 30° displacement.

Figure 5-15 shows a vector diagram for two voltage systems with 30° displacement. Here the voltage U'_a - U''_b is higher than the line-line voltage U'_a - U'_b. These voltages force an unwanted conduction path, where the diodes conduct for a period of 60° and the line current is determined to that of a six-pulse rectifier [Paice 1996]. To prevent this two IPT's can be used. One connected on the positive voltage dc-bus and one on the negative voltage dc-bus. Alternatively, because the current of each converter contains a significant amount of 3rd harmonic currents, a zero sequence blocking transformer (ZSBT) can be used.

In a balanced system the 3rd harmonic and other triplen currents are zero sequence currents. Because the zero sequence currents are in phase, they cannot sum to zero as it is the case for the positive and negative sequence currents. A ZSBT exhibits high impedance to zero sequence currents. The most effective ZSBT is the shell-type structure as shown in Figure 5-16.

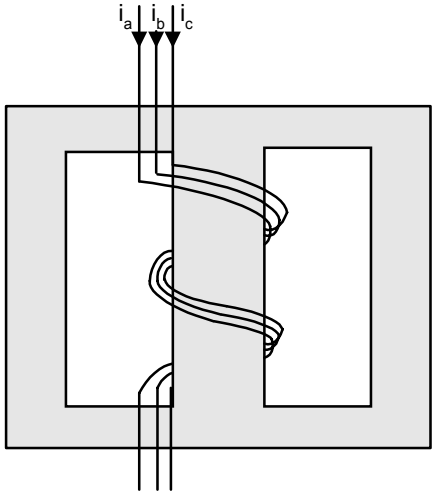


Figure 5-16: Simple sketch of a ZSBT.

The sum of the positive and negative sequence fluxes is zero. These currents will only see some form of leakage inductance. The zero sequence flux cannot sum to zero, but will return inside the core. The produced flux Φ results in the following impedance X:

$$X = \frac{\omega N \Phi}{\sum i_0} \tag{5.3}$$

The necessity of adding some extra measures such as IPT's and ZSBT's is diminishing the advantages of the parallel multi-pulse topology heavily. Especially with regards to enclosure and interconnection of the transformers. However, the parallel 12-pulse rectifier is the most used multi-pulse rectifier topology for ASD's in the medium power range. The reason for this is the possibility of smaller autotransformer compared to a three-winding transformer of the serial 12-pulse rectifier.

5.2.4 Simulation results of the 12-pulse rectifier

To determine the harmonic performance of the parallel 12-pulse rectifier some SABER simulations are discussed here. The parallel 12-pulse rectifier is simulated here instead of the serial 12-pulse rectifier, because this is the topology normally used for ASD's.

A 10 kVA parallel 12-pulse rectifier including an IPT as shown in Figure 5-17 is simulated in SABER. The phase-shifting transformer is assumed ideal (no impedance) and the line voltage is balanced and sinusoidal. The harmonic performance of the parallel 12-pulse rectifier is, just as the 6-pulse diode rectifier, highly depending on the line impedance and the inductance value of the IPT. A short circuit ratio of 100 is considered quite realistic in a real ASD application. However, the inductance value of the phase-shifting transformer and (depending on the transformer arrangement) balancing coils needs to be included. Therefore the simulations are made with R_{sce} = 20. (This means that the transformer and balancing coils have approximately 5% reactance). Figure 5-18 shows the line-current and the Fourier series of the line current. The THD_i = 10.5% and Hc = 138%. Note that there are no 5th and 7th harmonic.

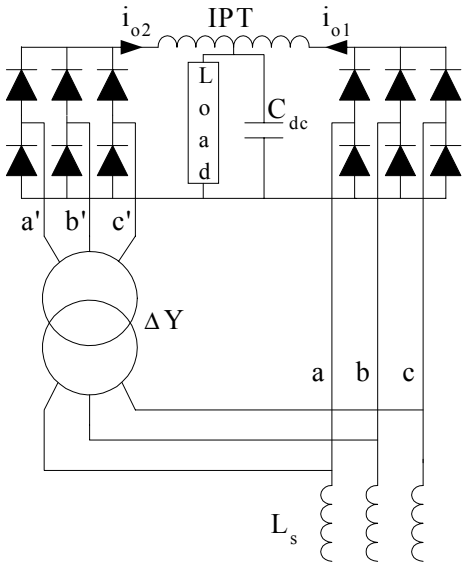


Figure 5-17: Circuit diagram of the simulated parallel 12-pulse rectifier with R_{sce} =20.

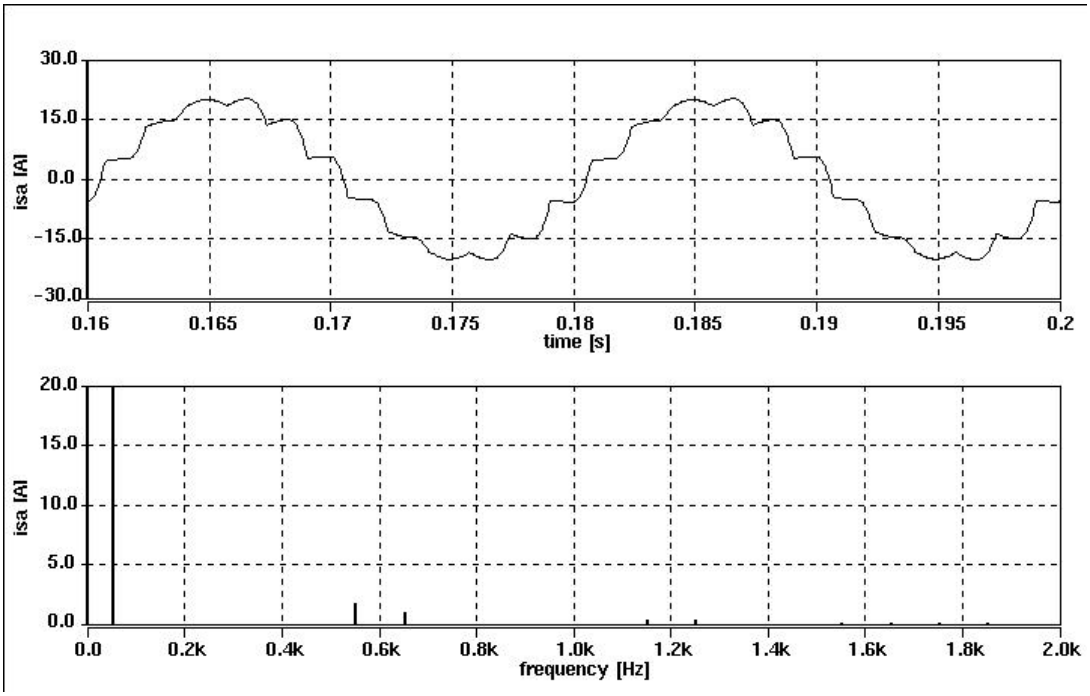


Figure 5-18: Line-current and Fourier series of the simulated parallel 12-pulse rectifier with R_{sce} = 20. THD_i = 10.5% and Hc = 138%.

As mentioned above the IPT ensures equal ripple current of both converters while differences in the average dc-link voltage cannot be equalized with an IPT only. This is shown in Figure 5-19, where the parallel 12-pulse rectifier is simulated with a pre-distorted grid (3% 5^{th} harmonic). In this case the THD_i = 16% and Hc = 150%. Note that a significant amount of 5^{th} harmonic current is present.

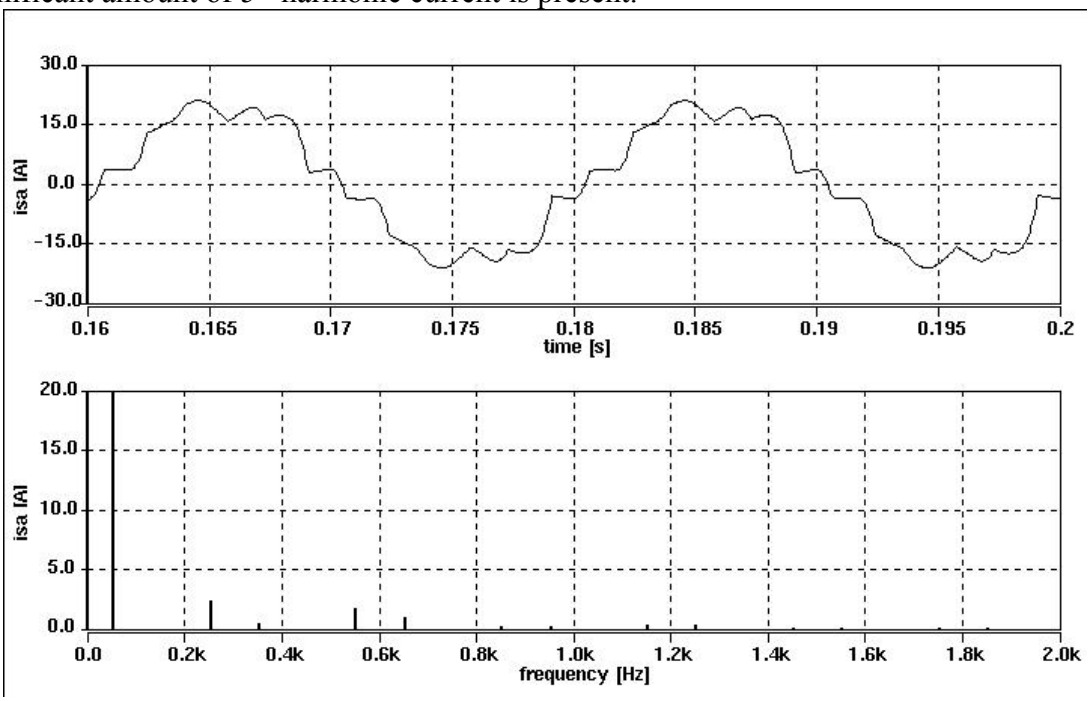


Figure 5-19: Line-current and Fourier series of the simulated parallel 12-pulse rectifier with R_{sce} = 20 and 3% 5^{th} harmonic supply voltage. THDi = 16% Hc =150%.

This difference is only caused by the pre-distorted grid with a 3% 5th harmonic voltage and shows clearly how sensitive the parallel 12-pulse rectifier is with respect to equal current sharing of the paralleled converters. Note, that 3% is a quite realistic value as shown in Chapter 3. The main reason for this is shown in Figure 5-20, where the dc-output current of both converters are shown. Even though the ripple current almost is identical of both converters due to the IPT, there is a big difference in the average output current of both converters.

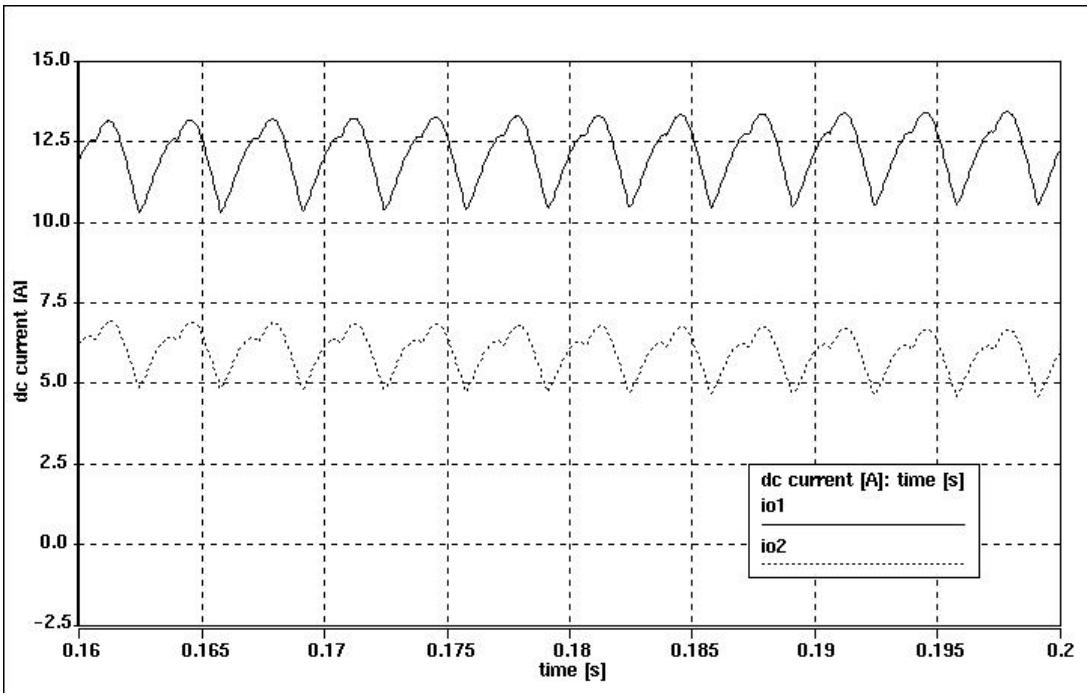


Figure 5-20: The output dc-link current of the two parallel 6-pulse rectifiers with R_{sce} = 20 and 3% 5th harmonic supply voltage.

The here simulated results are also obtained by [Rendusara et al. 1996]. [Rendusara et al. 1996] proposed to use additional line inter-phase transformer (LIT). Basically, these are current transformers as the IPT and they are used on the line-side instead. The disadvantages are that the complexity and total magnetic components are increased. On the other hand [Rendusara et al. 1996] has achieved equal current sharing even under non-ideal input voltages and thereby achieved low input current distortion.

5.2.5 Conclusion

The parallel 12-pulse rectifier is often used for ASD's in the medium power range. And as shown a THD_i = 10%, Hc = 135% can be expected. However, as for the 6-pulse rectifier, the parallel multi-pulse rectifier is highly depending on the line impedance and input voltage quality. It was shown that pre-distorted grid results in unequal current sharing of the two parallel rectifier bridges. At pre-distorted grid some 5th and 7th harmonic distortion must therefore be expected. Alternatively, additional use of LIT should be considered as done in [Rendusara et al. 1996].

Based on the analysis of above a THD_i = 10% - 20% and Hc = 125% - 175% is considered as a realistic harmonic performance of the parallel 12-pulse rectifier scheme.

5.3 Active Rectifier

Because of the capabilities to regenerate power, near sinusoidal input current and controllable dc-link voltage the active rectifier, as shown in Figure 5-21, is popular in high performance ASD's where frequent acceleration and de-acceleration are needed. Because of the harmonic limiting standards and the increased focus on harmonic currents and voltages in general, the active rectifier is by many believed to replace the diode rectifier in other applications too. A lot of research activity is going on in this field and this section reviews some of the recent developments. The main focus is on the harmonic performance of the active rectifier. Simulations and experimental results both at sinusoidal and pre-distorted grid are verifying the analysis.

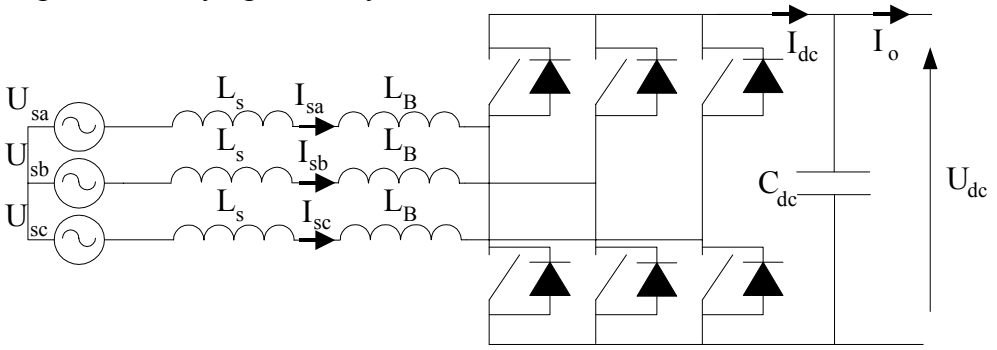


Figure 5-21: The active rectifier.

The active rectifier topology is basically identical to the PWM – Voltage Source Inverter (VSI) and is often called Voltage Source Converter (VSC). Most papers dealing with the active rectifiers focus on the control of the rectifier e.g. [Blaabjerg, Pedersen 1993], [Svensson, Lindgren 1998] and [Lee 1997]. Furthermore, a lot of work has been done to integrate the active rectifier with the PWM VSI inverter and thereby achieving very good dc-link voltage control even with a significant reduced dc-link capacitor [Kim, Sul 1993]. Lately, the influence of voltage unbalance and pre-distorted grid has gained a lot of attention [Blasko 1998], [Kim et al. 1998]. Also some sensorless control schemes have been presented recently [Noguchi et al. 1998] [Kwon et al. 1999].

Because the control strategy has a significant impact on the harmonic currents generated the basic control strategy is discussed in the following.

5.3.1 Basic control strategy

The basic control of the active PWM rectifier is easiest explained by Figure 5-22, where the line current I_s is controlled by the voltage drop across an inductance L_B interconnecting the two voltage supplies (source and converter). The inductance voltage (U_{LB}) equals the difference between the line voltage (U_s) and the converter voltage (U_{conv}). It can also be seen in Figure 5-22 and Figure 5-23 that it is possible to control both the active as well as the reactive power flow.

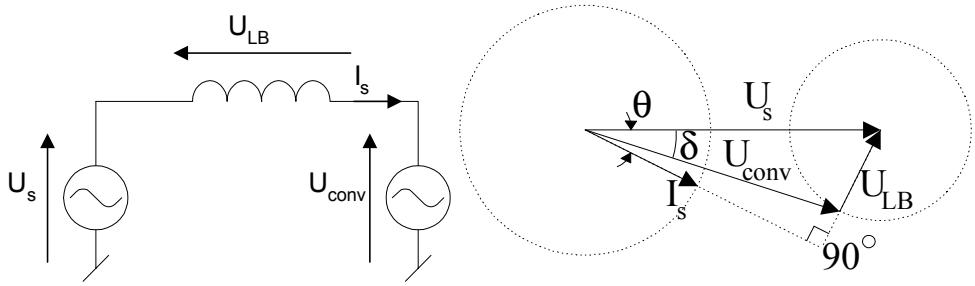


Figure 5-22: (a) Simple diagram of two voltage sources connected via an inductance L_B. (b) General vector diagram of the active rectifier.

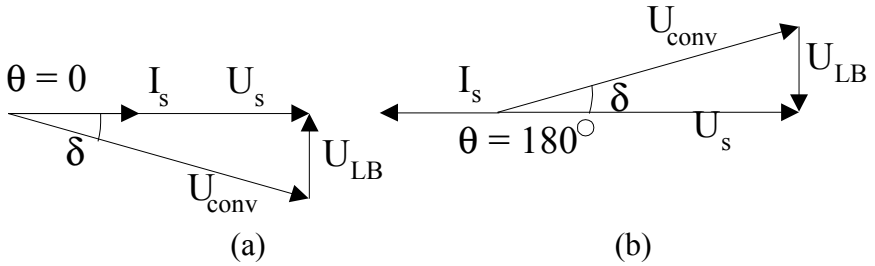


Figure 5-23: (a) Vector diagram for unity power factor for both rectification mode and (b) inversion mode.

One of the most popular control strategies for active rectifiers is the conventional voltage oriented control strategy (VOC) [Blaabjerg, Pedersen 1993] [Kwon et al. 1999] in the rotating d-q axis reference frame as shown in Figure 5-24. The advantage of the rotating d-q axis frame is that the controlled quantities such as voltages and currents become dc-values. This simplifies the expressions for control purpose and simple linear controllers can be used.

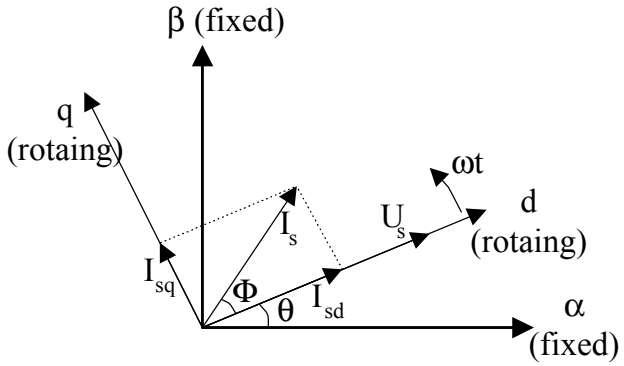


Figure 5-24: Co-ordinate transformation of line and rectifier voltage and current from fixed α–β co-ordinates to rotating d-q co-ordinates

By placing the d-axis of the rotating frame on the line voltage vector a simplified dynamic model can be obtained in the rotating frame. The q-voltage equals zero per definition and hence in order to have a unity displacement power factor the q-current has to be controlled to zero as well. The equations for the utility grid and the converter can in the rotating dq-axis frame be expressed as:

$$u_{sd} = R_B i_{sd} + L_B \frac{di_{sd}}{dt} + u_{d,conv} - \omega_s L_B i_{sq}$$
$$u_{sq} = 0 = R_B i_{sq} + L_B \frac{di_{sq}}{dt} + u_{q,conv} + \omega_s L_B i_{sd} \quad (5.4)$$

A simple way to decouple the d- and q-axis is obtained by measuring the currents and add the resulting voltage to the output of the current controller as in equation 5.5:

$$u_{d,conv} = u_{d,ref} + \omega L_B i_{sq} + u_{sd}$$
$$u_{q,conv} = u_{q,ref} - \omega L_B i_{sd} \quad (5.5)$$

The dc-voltage of the active rectifier is controlled by the active power into the rectifier. This means by controlling the d-current the dc-voltage can be controlled. This leads to the control block-diagram as shown in Figure 5-25.

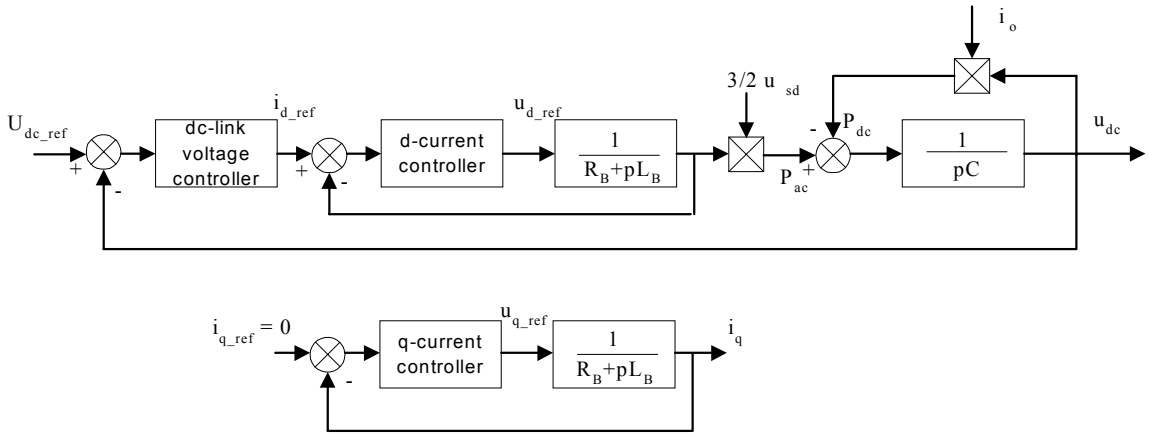


Figure 5-25: Control block diagram of the active rectifier assuming decoupling.

The inner loop current controller can be a simple PI-controller as in [Blaabjerg, Pedersen 1993] or a dead-beat controller as in [Kim et al. 1998] and [Svensson, Lindgren 1998]. The outer loop dc-link voltage controller is not a crucial controller regarding the harmonic performance. The only demand to the controller is that the dc link voltage has to be above the natural dc-link voltage, which is defined as the dc-link voltage of the diode rectifier. Often a simple proportional controller is used.

5.3.2 Line voltage estimator

Reducing the cost of the active rectifier is vital for the competitiveness compared to other high power factor rectifiers. Therefore some different sensorless control schemes have been presented recently. [Noguchi et al. 1998] [Kwon et al. 1999]. To determine if the sensorless control scheme influences the line-side currents a novel sensorless scheme is presented in the following. Simulations and experimental results verify this scheme.

It is clear that some sensors must be used for control of the active rectifier. Normally three kind of sensors are used:

- dc-voltage sensor
- ac-line current sensors
- ac-line voltage sensors

The dc-voltage and the ac-line current sensors are an important part of the over-voltage and over-current protection, while the ac-line voltage sensors can be omitted [Noguchi et al. 1998] [Kwon et al. 1999].

One important feature the line voltage estimator must fulfill is to estimate the voltage correct even under unbalanced conditions and pre-existing harmonic voltage distortion. Not only the fundamental component must be estimated correct, but also the harmonic components and voltage unbalance must be estimated. This is an important point, so it is possible to either compensate for this error to obtain sinusoidal line currents [Blasko 1998], [Kim et al. 1998] or let the current follow the voltage for a higher total power factor [Noguchi et al. 1998].

It is possible to calculate the voltage across the inductance by differentiating the current flowing through it. The line voltage can then be estimated by adding the rectifier voltage reference to the calculated voltage drop across the inductor. However, this approach has the disadvantage that the current is differentiated and noise in the current signal is gained through the differentiation. To prevent this an extension of the voltage estimator described in [Noguchi et al. 1998] is presented.

In traditional vector modulation for three-phase voltage source inverters the currents are sampled in the zero-vector states because no switching noise is present and a filter in the current feedback for the current control loops can be avoided [Leonhard 1996] [Leonhard 1991]. In this case the instantaneous active and reactive power in the inductance can be calculated by measuring only the currents:

$$\begin{aligned} p &= L_B\left(\frac{di_{sa}}{dt}i_{sa}+\frac{di_{sb}}{dt}i_{sb}+\frac{di_{sc}}{dt}i_{sc}\right) \\ q &= \frac{3L_B}{\sqrt{3}}\left(\frac{di_{sa}}{dt}i_{sc}-\frac{di_{sc}}{dt}i_{sa}\right) \end{aligned} \tag{5.6}$$

Since p and q are dc-values it is possible to prevent that noise of the differentiated current has influence on the estimated active and reactive power by the use of a simple (digital) low pass filter. This ensures a robust and noise insensitive performance of the instantaneous power estimator.

The estimated voltage across the inductance can then be calculated by:

$$\begin{bmatrix} u_{L\alpha} \\ u_{L\beta} \end{bmatrix} = \frac{1}{i_{s\alpha}^2+i_{s\beta}^2}\begin{bmatrix} i_{s\alpha} & -i_{s\beta} \\ i_{s\beta} & i_{s\alpha} \end{bmatrix}\begin{bmatrix} p \\ q \end{bmatrix} \tag{5.7}$$

where:

$u_{L\alpha}$, $u_{L\beta}$ are the estimated values of the three-phase voltages across the boost inductance L_B in the fixed α-β reference frame.

The estimated line voltage u_{est} can now be found by adding the voltage reference of the active rectifier to the estimated inductor voltage.

$$\vec{u}_{est} = \vec{u}_{conv} + \vec{u}_{LB} \tag{5.8}$$

The control structure of the VOC scheme including the line-voltage estimator is shown in Figure 5-26

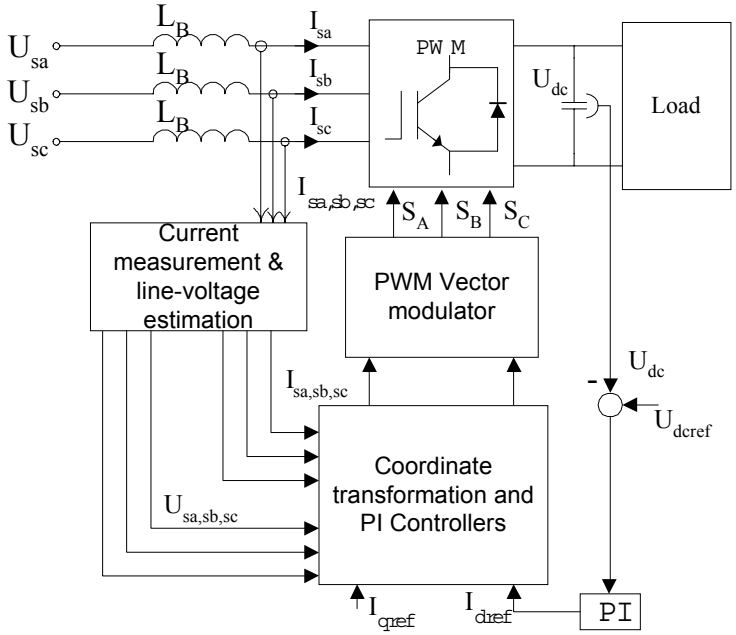


Figure 5-26: Control structure of the conventional VOC with line voltage estimation.

5.3.3 Simulation results

A full model of the active rectifier is implemented in SABER. The active rectifier is connected to a 200 kVA transformer (50 Hz, 400 V) with $e_x = 5\%$ and $e_r = 1\%$ as shown in Figure 5-27.

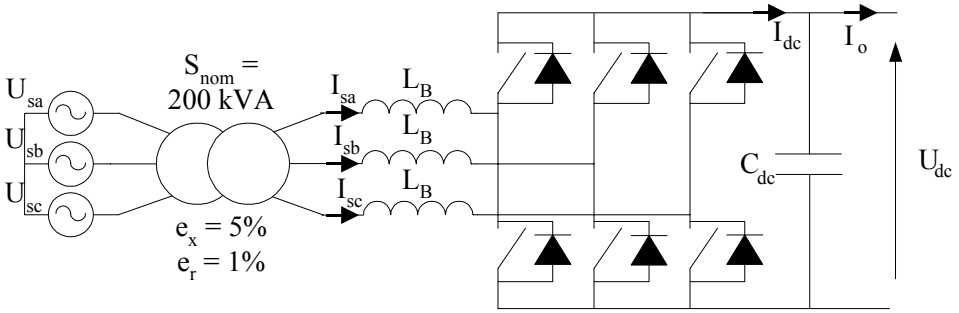


Figure 5-27: Circuit diagram of the simulated active rectifier.

The fundamental input power of the active rectifier equals 5 kVA. The boost inductance (L_B) is normally in the range of 5% - 10% (related to the active rectifier per unit notation). The simulations are made with a 10% (10 mH) boost inductance L_B. The resistance of the boost inductance is 80 mΩ. The dc-link capacitor bank equals 1 mF. The dc-link voltage reference is 600 V. The switching frequency and sampling frequency is 5 kHz.

Simulations on a perfectly balanced and sinusoidal grid as well as simulations with a distorted grid are presented. The distorted grid has 4.5% voltage unbalance and 5% 5^{th} harmonic voltage.

Figure 5-28 shows the simulations of the VOC with sinusoidal line voltage. The simulated current THD_i equals 4.5%. As shown the line-voltage estimator works very well, since the estimated line voltage is very close to the real line voltage.

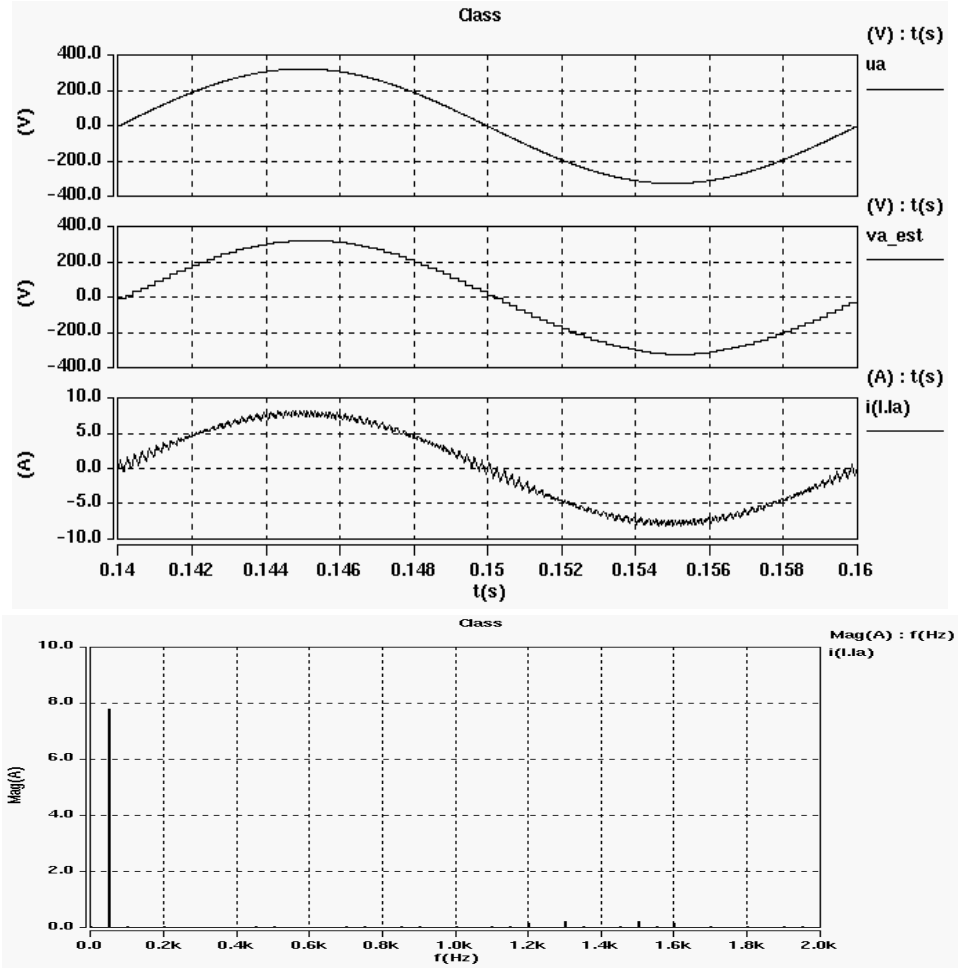


Figure 5-28: Line voltage, estimated line voltage and input current, together with the harmonic spectrum of the input current of the VOC. The current THD_i = 4.5%.

Figure 5-29 shows the simulation results for the VOC with pre-distorted and unbalanced line voltage. The THD_i equals 9.2%. The estimated line voltage is still very close to the real line voltage and the current follows the voltage well.

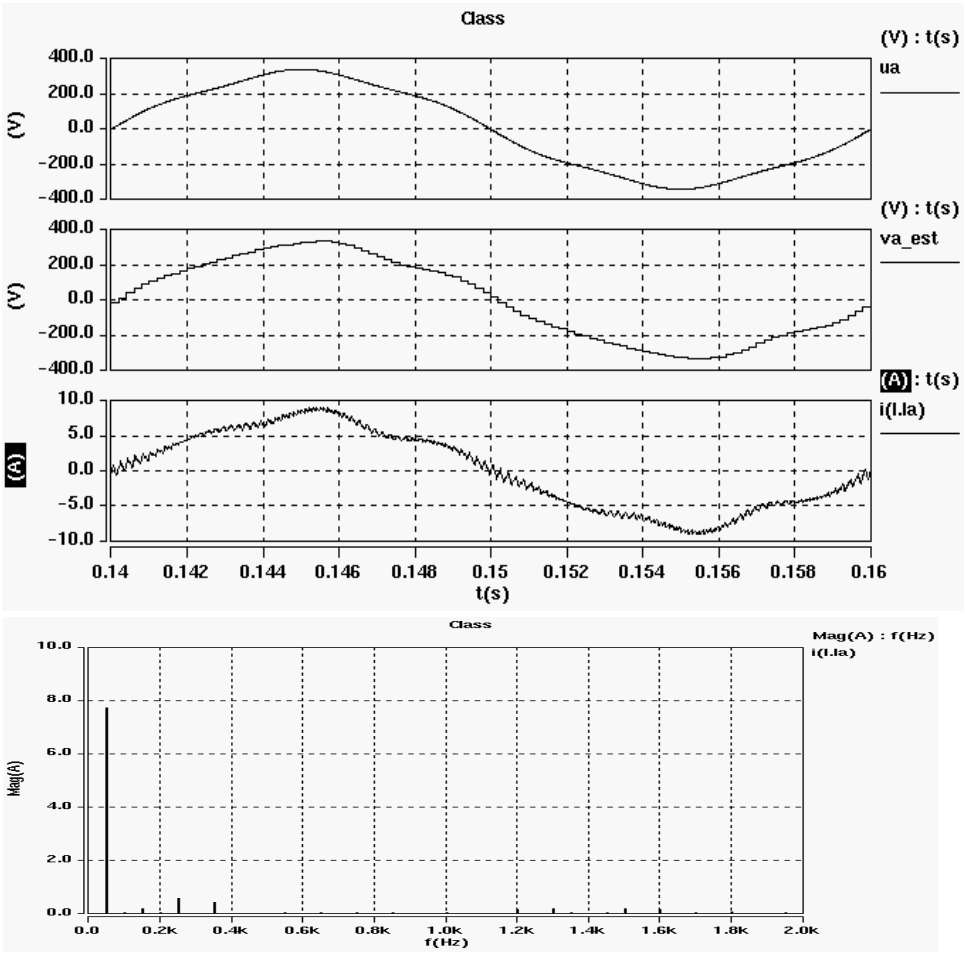


Figure 5-29: Line voltage, estimated line voltage and input current, together with the harmonic spectrum of the input current of the VOC with 4.5% voltage unbalance and 5% 5th harmonic voltage. The current THD_i = 9.2%.

5.3.4 Experimental results

An experimental setup is used in the laboratory of the Institute of Energy Technology at Aalborg University. The laboratory setup consists of a three-phase 30 kVA programmable power supply of the type California Instrument, two commercially available inverters (Danfoss VLT® 3008) controlled by two DSP's (ADSP 21062) and a motor-generator setup as load. The fundamental input power of the active rectifier equals 5 kVA. The boost inductance (L_B) is 10% (10 mH). The dc-link capacitor bank equals 1 mF. The dc-link voltage reference is 600 V and the switching frequency and sampling frequency equals 5 kHz.

The experimental results for the VOC strategy with no ac-line voltage sensor are shown in Figure 5-30, Figure 5-31, Figure 5-32 and Figure 5-33 The experimental results are very close to the simulated results of Figure 5-28 and Figure 5-29. Again it is shown that the line-voltage estimator works very well even under pre-distorted and unbalanced conditions. The measured current THD_i = 6.1% with sinusoidal and balanced input voltage and THD_i = 11.8% under unbalanced and pre-distorted input voltage.

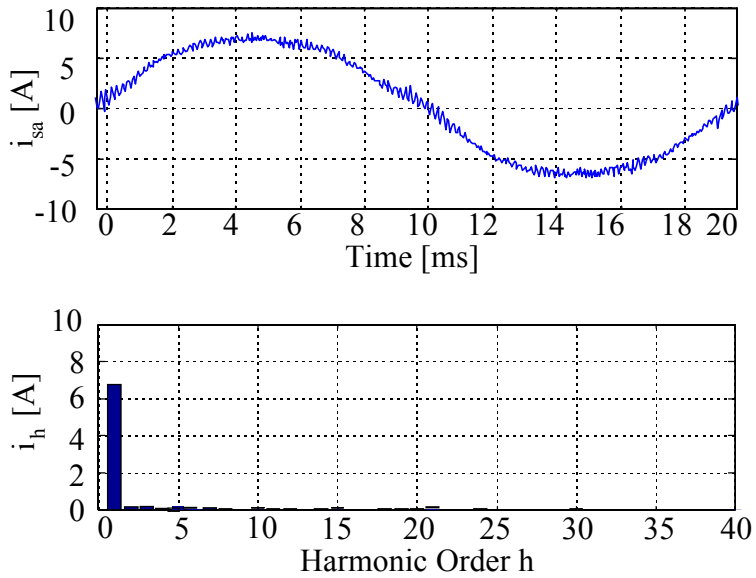


Figure 5-30: Line current, together with the Fourier spectrum of the input current of the VOC. The current THD_i = 6.1%.

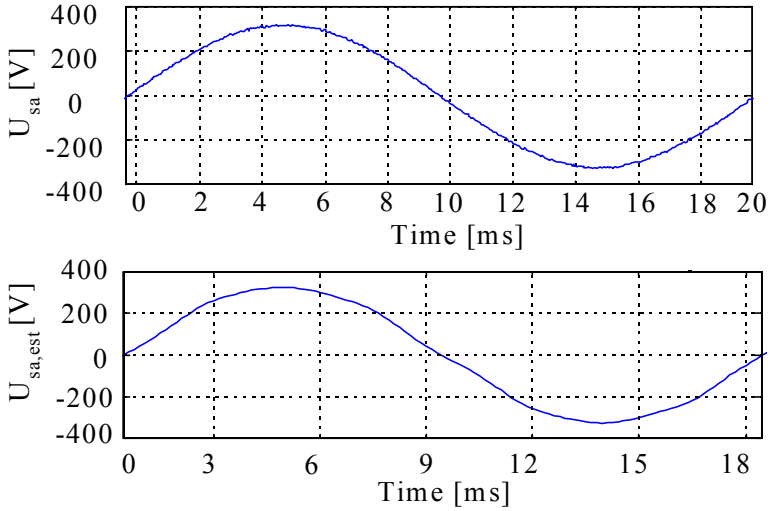


Figure 5-31: Line voltage and estimated line voltage at sinusoidal and balanced grid.

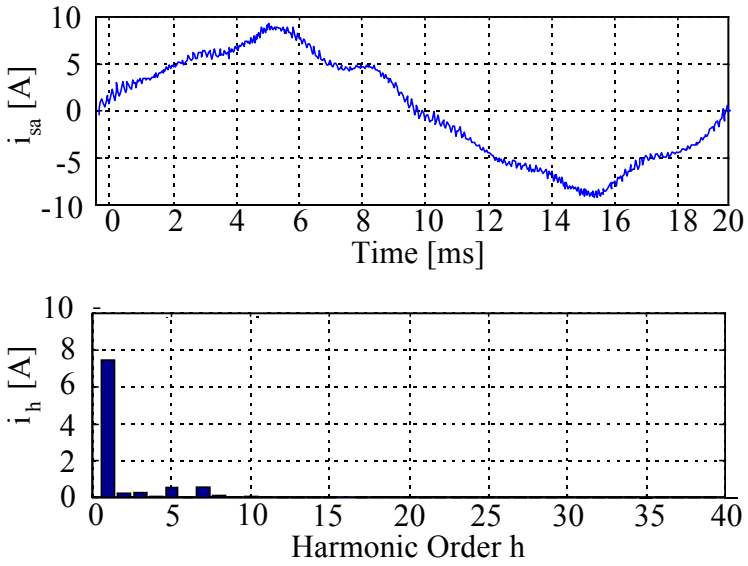


Figure 5-32: Line current, together with the Fourier spectrum of the input current of the VOC at 4.5% voltage unbalance and 5% 5th harmonic voltage. The current THD_i = 11.8%.

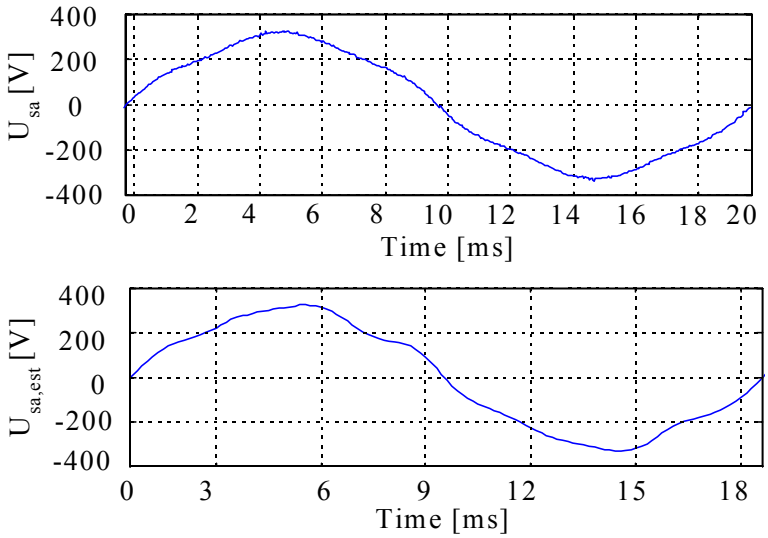


Figure 5-33: Line voltage and estimated line voltage at 4.5% voltage unbalance and 5% 5th harmonic voltage.

As shown above the line voltage estimation is close to the actual line voltage. Therefore it can be concluded that line current is not significantly affected by if the line voltage is measured or estimated. It should be noted, that in the simulation and experimental results of above it is chosen to let the current follow the distorted voltage for a higher total power factor. Therefore some 5th harmonic is seen in the line current at pre-distorted and unbalanced grid. However, it is possible to compensate for this and to obtain sinusoidal line currents. This is shown among others by [Blasko 1998] and [Kim et al. 1998].

5.3.5 Future perspective

As shown above the harmonic current of the active rectifier can almost be controlled to zero so that sinusoidal line current can be obtained. However, the active rectifier is switching directly on the grid and LCL filters should therefore be used instead of only a boost inductance as done in the simulations and experimental results above. Problems with switching noise without LCL filters have been reported by [Hill, Kapoor 1998]. Compared to the above investigated issues only few papers have been working with the design of the filter and the influence of the filter on the control of the active rectifier. However, [Walsh et al. 1997] has shown that using discontinuous modulation (DPWM) can reduce the size of the LCL filter. Some simulations and experimental results of the active filter with DPWM can be found in appendix D.3. Also very few papers have been working with EMI-related problems of the active rectifier, such as the increased common mode and differential mode noise compared to the diode rectifier.

It is believed that future work should focus on one of these areas if the active rectifier should become and alternative to the diode rectifier also in low performance applications.

5.3.6 Conclusion

Because of the advantages listed below, the active PWM rectifier is probably *the* most elegant rectifier topology for ASD's.

- Almost sinusoidal input current is achievable
- Bi-directional power flow
- Possibility for reduced capacitor size due to control of the power flow [Kim, Sul 1993]
- Controllable dc-link voltage, which enhances the speed range of the ASD

All these features are favorable in especially high performance ASD's where frequent acceleration and deceleration or power regeneration are needed. However, the active rectifier has a number of disadvantages, as listed below, which makes that this topology is not seen in a large number of industrial applications (so far).

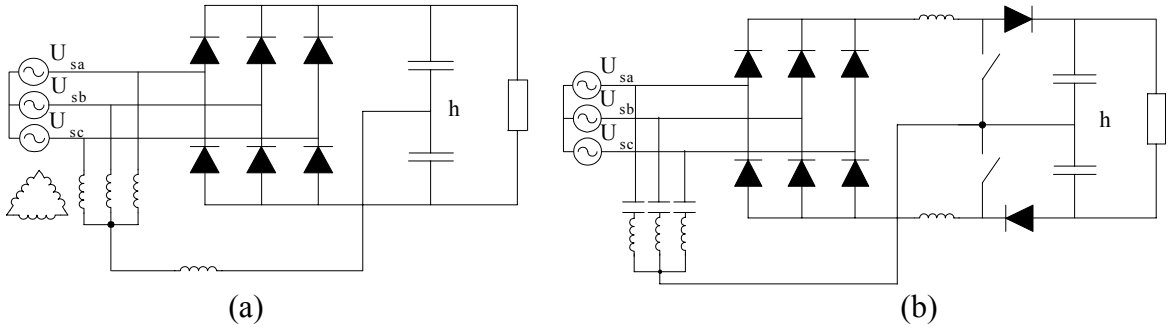
- The need for LCL filters and the number of switches makes this solution about twice as expensive compared to the ASD with a diode rectifier
- A complex control strategy compared to other topologies
- Lower efficiency than the diode rectifier due to extra switching losses and higher conducting losses of the IGBT's compared to power diodes. Furthermore, the losses of the ASD inverter increases too because of a higher dc-link voltage
- EMI can be a significant problem and EMI filters are necessary

Based on the analysis of above a THD_i = 5% - 10% is considered as a realistic harmonic performance of the active rectifier. It is difficult to predict a realistic Hc value because the Hc value is highly depending on the amount of higher harmonics. The higher harmonics of the active rectifier depends on the switching frequency and the type of line-filter used (e.g. LCL or L filter).

5.4 Third Harmonic Injection Scheme

The third harmonic injection scheme presented by [Bird et al. 1969] was one of the first harmonic reduction techniques based on current shaping. Bird et al. stated that harmonic currents of a three-phase rectifier might be significant reduced by injecting third harmonic

currents. Injection of the third harmonic current with an external triplen harmonic current source is later generalized by [Ametani 1972]. In the early nineties the injection of the third harmonic current has been rediscovered by [Kim et al. 1994] and [Mohan 1992], where the third harmonic current is produced by connecting a transformer or a tuned filter from the capacitor neutral point 'h' to the line as shown in Figure 5-34.



(a) (b)

Figure 5-34 Third harmonic injection schemes. (a) Circuit presented in [Kim et al. 1994]. (b) Circuit presented in [Mohan 1992].

The advantages of the circuits presented in [Mohan 1992] are:

- Controllable dc-link voltage
- Current THD_i less than 5% can be obtained (according to [Mohan 1992])

Disadvantages of the circuits presented in [Mohan 1992] are:

- Two power switching devices.
- Two additional diodes in series with the power flow giving extra losses.
- Complex control.

The scheme presented in [Kim et al. 1994] is a passive topology with a non-controllable circulating current and a THD_i of 5% is achievable. However, the scheme of [Kim et al. 1994] is most suitable for a rectifier with a high dc-link inductance. Therefore, the novel scheme presented in the following (see also Appendix D.2) is modified to suit for a standard ASD with small dc-link inductance and large dc-link capacitor. Furthermore, the circulating third harmonic current is controlled and the optimum THD_i can be found at different operating points.

5.4.1 Principle of harmonic reduction with the third harmonic injection scheme

For description of the third harmonic injection scheme the simplified diagram of Figure 5-35 is used.

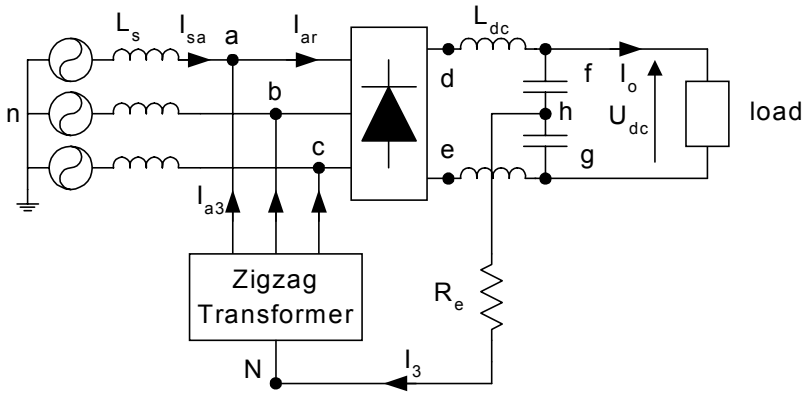


Figure 5-35: Simplified diagram of the proposed scheme showing the basic idea.

As shown in Figure 5-36 the shape of the voltage U_{hN} between the dc-link midpoint 'h' and the neutral of the zigzag transformer 'N' is triangular in nature due to the 120° conduction mode of the 6-pulse diode rectifier. Interconnection between point 'h' and point 'N' via a resistor R_e results in a circulating current I_3, in shape and phase with the voltage U_{hN}. This circulating current is essentially a third harmonic current and it is injected into the three phases 'a', 'b' and 'c' via a zigzag transformer.

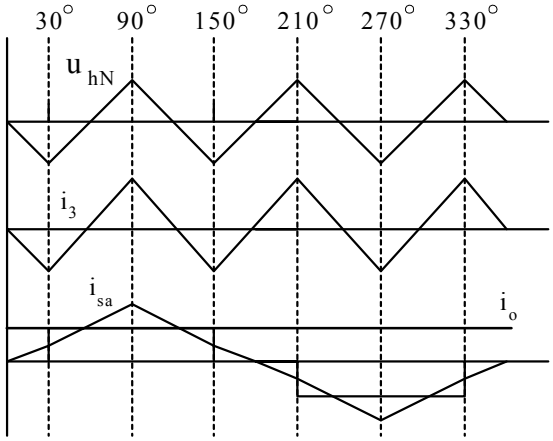


Figure 5-36: The voltage U_{hN} between the dc-link midpoint 'h' and the neutral 'N'. The current I_3 is in phase and shape with the voltage. The line current i_{sa} can be reconstructed as a function of the dc-link output current I_o and the circulating third harmonic current I_3.

In each phase a third of the circulating current is injected. Depending of the conduction mode of the 6-pulse diode rectifier three different modes are considered for each phase. For phase 'a' these three modes are described below.

Mode 1: Phase 'a' is not conducting.

In this case a third of the circulating current I_3 is injected into the source. The source current of phase 'a', I_{sa}, equals:

$$I_{sa} = -\frac{I_3}{3} \tag{5.9}$$

Mode 2: Positive conduction mode.

The upper diode of phase 'a' in the 6-pulse diode rectifier conducts. Half of the circulating current flows into the rectifier. The other half flows into the rectifier via the lower diode of phase 'b' or 'c'. The upper diode of phase 'a' conducts also the load current into the rectifier. Therefore, the source current of phase 'a', I_{sa}, equals:

$$I_{sa} = I_o + \frac{I_3}{2} - \frac{I_3}{3} = I_o + \frac{I_3}{6} \tag{5.10}$$

Mode 3: Negative conduction mode.

The lower diode of phase 'a' in the 6-pulse diode rectifier conducts. Half of the circulating current flows into the rectifier. The other half flows into the rectifier via the upper diode of phase 'b' or 'c'. The lower diode of phase 'a' conducts also the load current back to the source. Therefore, the source current of phase 'a', I_{sa}, equals:

$$I_{sa} = -I_o + \frac{I_3}{2} - \frac{I_3}{3} = -I_o + \frac{I_3}{6} \tag{5.11}$$

The source current can now be reconstructed as shown in Figure 5-36. A detailed description of the principles of the third harmonic injection scheme can be found in [Kim et al. 1994].

In a standard ASD the harmonic content of the input current depends both on the dc-link inductance and the ac-line reactance as shown in Chapter 4. And the input current is seldom a square-wave form as assumed in the description above. In some cases the input current can even be discontinuous. Therefore, finding the optimal amplitude of the circulating current that results in the lowest THD_i in an analytical way is quite cumbersome. Here SABER is used for the analysis part.

The scheme of Figure 5-35 is implemented in SABER. The ASD capacitor banks in the dc-link equal 10.5%. The simulations are done with and without a 2.6% dc-link inductance. The frequency is 60 Hz and the ac- impedance is varied, i.e. the short circuit ratio R_{sce} is varied from 20 to 500. After a total of 90 simulations to analyze the input current THD_i the results are shown in Figure 5-37 and Figure 5-38.

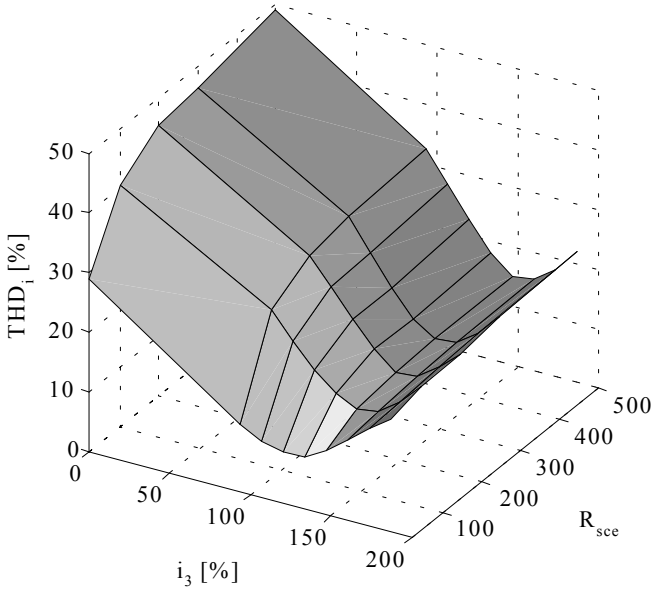


Figure 5-37: The THD_i of the input power as a function of the circulating current in percentage of the output current and the short circuit power. The dc-link inductance of the 6-pulse diode rectifier equals 2.6%.

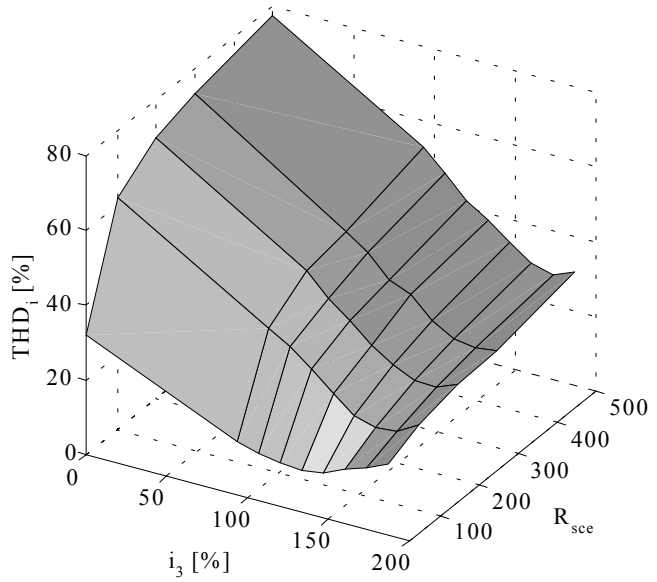


Figure 5-38: The THD_i of the input power as a function of the circulating current in percentage of the output current and the short circuit power. There is no dc-link inductance in the 6-pulse diode rectifier.

It can be seen from Figure 5-37 that using a dc-link inductance of 2.6% and a circulating current (I_3) of approximately 150% of the output current (I_o) results in an input current THD_i of less than 15% and is independent of the line reactance. On a weak utility grid (R_{sce}=20) a circulating current of 120% gives a minimum THD_i of 9%.

Figure 5-38 shows that the circulating current has to be somewhat higher (180%) when no dc-link inductance is used. Only at a weak grid (R_{sce}=20) an input current THD_i of 15% can be achieved. Here, the circulating current (I_3) has only to be 140% of the output current (I_o).

The power dissipated in the resistor equals the circulating current times the voltage U_{hN}. The voltage U_{hN} and the current can be presented as [Kim et al. 1994]:

$$U_{hN} = U_{ab}\frac{-3\sqrt{2}}{8\pi}\sin(3\omega t)$$
$$i_3(t) = -\sqrt{2}\cdot I_3\sin(3\omega t) \qquad (5.12)$$

The instantaneous power losses in the resistor R_e can be calculated as:

$$P_{3,inst} = U_{ab}\hat{i}_3\frac{3\sqrt{2}}{16\pi}\left(1-\cos(6\omega t)\right) \qquad (5.13)$$

To avoid the power losses a single-phase boost converter is employed instead of the resistor. Thus, the only power loss equals the switching and conduction losses in the converter.

5.4.2 The single-switch third harmonic injection scheme

The single-switch third harmonic injection scheme presented in the following is an extension of the scheme presented in [Kim et al. 1994]. Figure 5-39 shows the circuit topology of the proposed scheme.

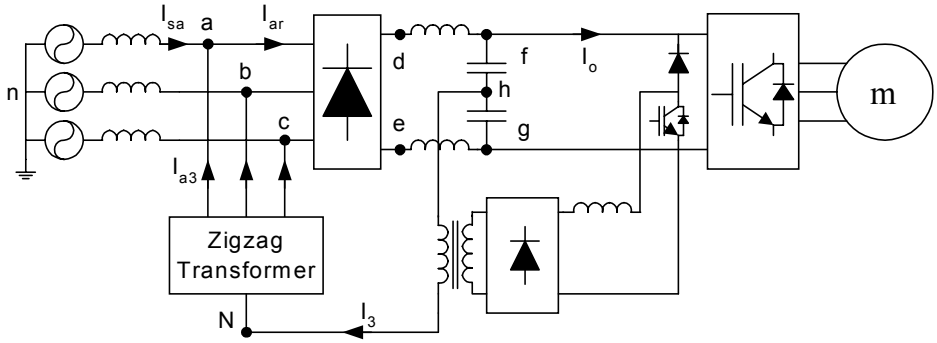


Figure 5-39: Proposed integrated single-switch approach to improve harmonic performance of standard adjustable speed drives.

In this approach a zigzag transformer is employed to create a neutral 'N'. Further, a single-phase transformer is connected between 'N' and the dc-link mid-point 'h'. On the secondary side of the single-phase transformer a single-phase boost power factor correction circuit is implemented as shown Figure 5-39. Since the voltage between 'N' and 'h' is predominantly 3rd harmonic, the single-phase boost converter action results in 3rd harmonic injected current I_3 and drastically improves the ASD utility power quality performance.

For galvanic isolation of the boost converter a single-phase transformer is required. The output of the boost converter is connected to the dc-link capacitor bank of the ASD, and therefore the boost converter need no outer voltage loop control. For integration of the

boost converter in the ASD the diode and the IGBT of the braking chopper circuit of the standard ASD is used. It should be noted that dc-link capacitor midpoint and a dynamic braking chopper (IGBT and diode) exist in most standard ASD's.

To evaluate the proposed scheme some simulations are made using the SABER simulator. The simulated system consists of a 10 kW three-phase rectifier, 480 V line to line voltage and the frequency is 60 Hz. The utility grid is modeled by some line inductance. The total capacitance of the dc-link capacitor banks equals 10.5%. The transformers are ideal with no leakage inductance and a high magnetizing inductance. The transformer ratio of the single-phase transformer is 1:4. The switching frequency of the boost converter is about 8 kHz. The short circuit ratio R_{sce} is varied from 20 to 500. Again simulations are made with and without a 2.6% dc-link inductance.

With dc-link inductance

As expected varying the ac-line impedance and thereby the short circuit ratio has shown that there is small difference of the behavior of the proposed system between a weak and a strong utility grid. The current and the corresponding Fourier spectrum are shown in Figure 5-40 and Figure 5-41.

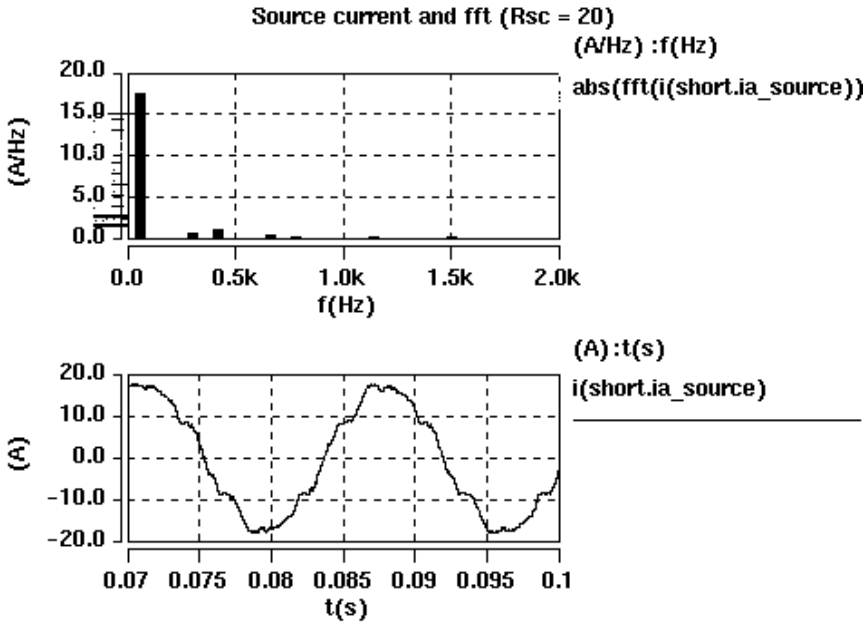


Figure 5-40: The line current and the Fourier spectrum. The short circuit ratio R_{sce} = 20 and the THD_i of the line current is 9%.

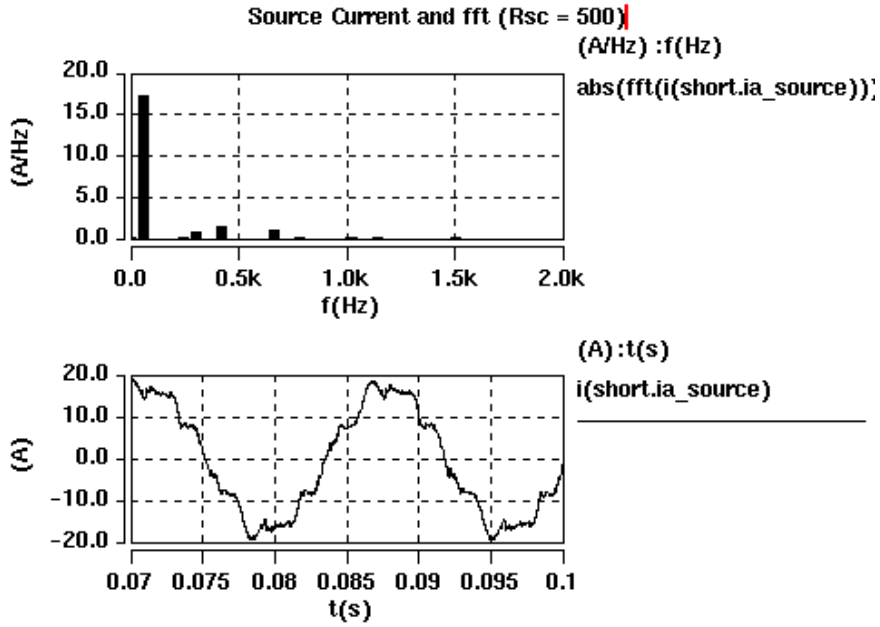


Figure 5-41: The line current and the Fourier spectrum. The short circuit ratio R_{sce} = 500 and the THD_i *of the line current is 13%.*

The THD_i of the current is 9% with a short circuit ratio of 20 while the THD_i is 13% with a short circuit ratio of 500. The amplitude of the circulating current on the primary side of the single-phase transformer is 17.7 A (rms). The output current I_o equals 15 A.

Without dc-link inductance

As expected without the dc-link inductance the harmonic distortion of the input current is increased at a high short circuit ratio. This is shown in Figure 5-42. The THD_i of the current is 23.6% while the short circuit ratio equals 500. The amplitude of the circulating current on the primary side of the single-phase transformer is 21.1 A (rms). The output current I_o equals 15 A.

In a system with a weak utility grid the performance of the proposed solution is almost as good as with the dc-link inductance. This is shown in Figure 5-43. The THD_i of the current is 10% with a short circuit ratio of 20. The amplitude of the circulating current on the primary side of the single-phase transformer is the same as for with dc-link inductance, 17.7 A (rms). The output current I_o equals 15 A.

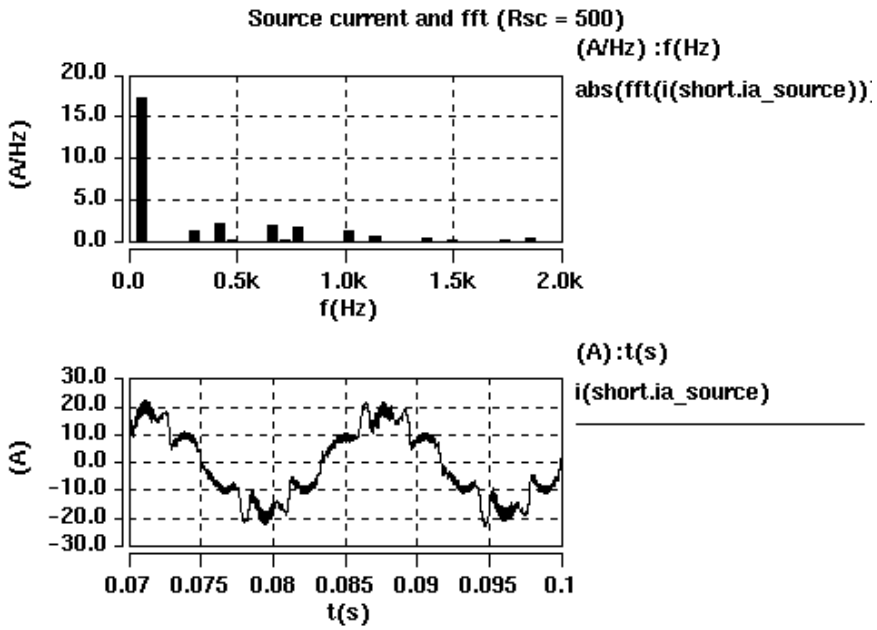


Figure 5-42: The line current and the Fourier spectrum. The short circuit ratio R_{sce} = 500 and the THD_i *of the line current is 23.6%.*

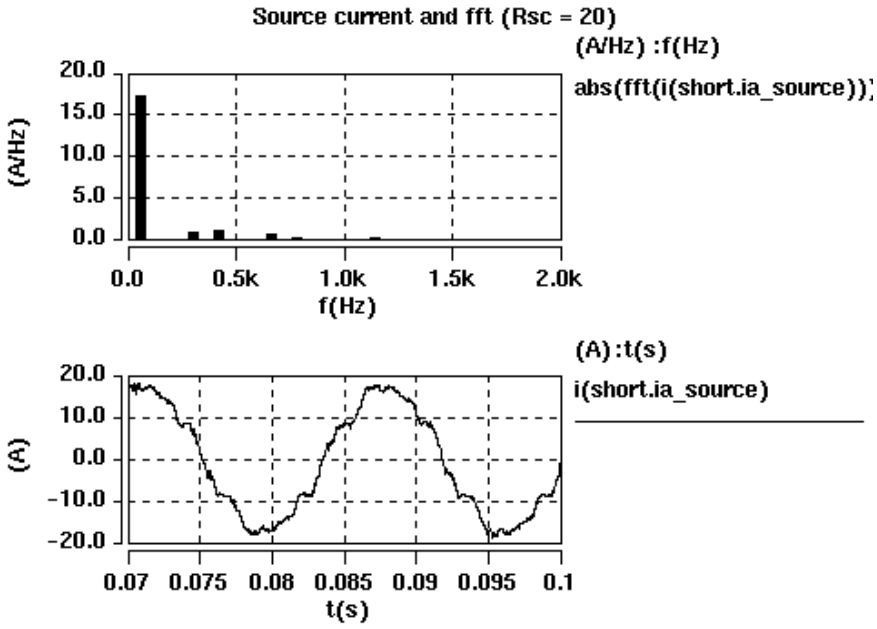


Figure 5-43: The line current and the Fourier spectrum. The short circuit ratio R_{sce} = 20 and the THD_i *of the line current is 10%.*

Adaptation of the proposed scheme for multiple drives

Interconnection of multiple drives is also possible. Two 10 kW ASD's are connected in parallel as shown in Fig. 5-44. By interconnection of the dc-link it is assured that both diode rectifiers are equally loaded, even when one of the ASD's is braking. The connection is made on the line side of the dc-link inductance. The midpoints of the dc-link capacitors in the ASD's are connected together to ensure that the circulating current is divided equally between both rectifiers.

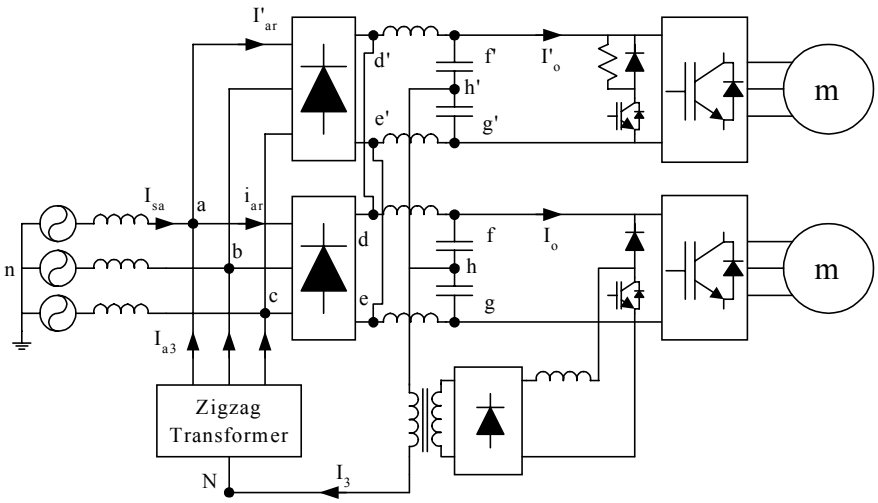


Fig. 5-44: Interconnection of two ASD's, one which uses dynamic breaking chopper for the proposed scheme, while the other uses the dynamic breaking chopper for braking resistor.

Figure 5-45 shows the result when both drives are operating under full load condition. The simulations are made with a short circuit ratio R_{sce} = 100. Figure 5-46 shows the result when one of the drives operates at half load and the other drive operates at full load conditions.

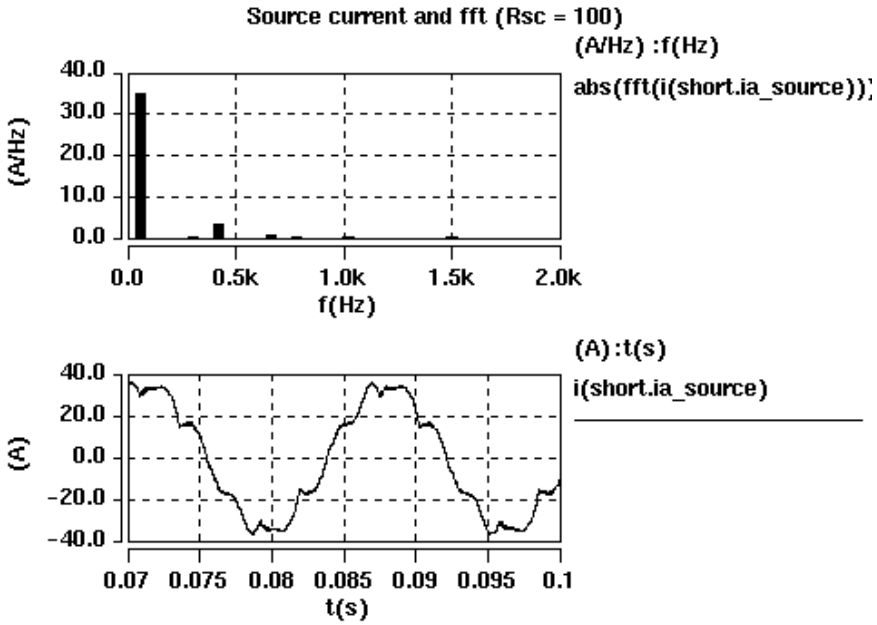


Figure 5-45: The line current and the Fourier spectrum with interconnection of two ASD's. The THD_i of the line current is 11.6%. Both ASD's operates at full load.

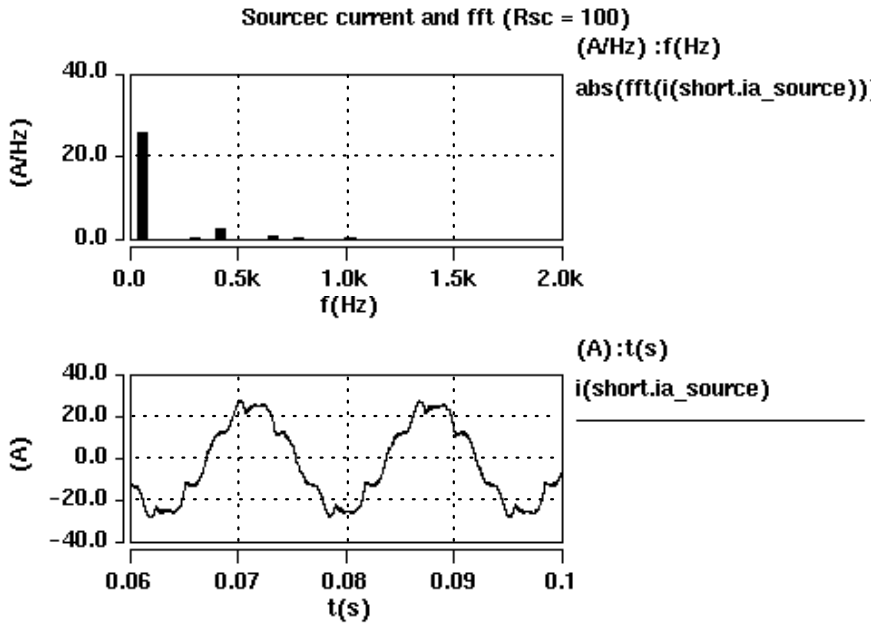


Figure 5-46: The line current and the Fourier spectrum with interconnection of two ASD's. The THD_i of the line current is 12.5%. One ASD operates at full load while the other operates at half load.

It is demonstrated that for a low short circuit ratio a single digit THD_i can be achieved, and when series inductance (either dc- or ac-inductance) is used as in the case with the dc-link inductance a THD_i well below 15% can be achieved even for a (very) high short circuit ratio. Only in the case of no series inductance and high short circuit ratio, the result is not satisfying. Also, the circulating current becomes somewhat higher in this case. To fulfill the demands of independent operation of the line impedance, which is stated in the introduction of this chapter, one should use an additional inductance. Either an ac-inductance or as presented in this section a split dc-link inductance can be used.

5.4.3 Design example

Prior to some experimental results, the additional components used compared to the three-phase diode rectifier needs to be designed. In this section the design of the zigzag transformer, the single-phase transformer and the boost converter is presented in per unit quantities.

Ratings of various components are calculated based on a rectifier using a dc-link inductance, hence $I_3 = 1.2 \cdot I_o$.

The voltage across the zigzag transformer is illustrated in Figure 5-47. The voltage on the primary (and secondary) winding U_{wd} of the transformer is:

$$U_{wd} = \frac{U_{an}}{\sqrt{3}} = \frac{U_{ab}}{3} \tag{5.14}$$

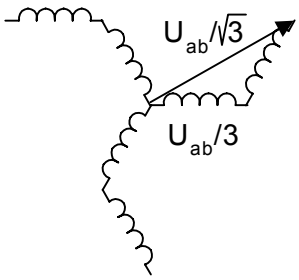


Figure 5-47: The voltage across the windings on a zigzag transformer.

The current in the phase windings (I_{a3}) is $1.2 \cdot I_o/3$. Thus the VA-rating of the transformer is:

$$VA_{zigzag} = \frac{1.2 \cdot I_o \cdot U_{ab}}{3} = 0.296\,pu \qquad (5.15)$$

The transformer ratio of the single-phase transformer should be chosen with care. Since no outer voltage control loop is necessary the output of the boost rectifier is connected directly to the capacitor banks of the ASD. In a boost converter the dc-link voltage must always be somewhat higher than the amplitude of the input voltage. In [Kim et al. 1994] it is shown that U_{hN} basically is given by $U_{hN} = 0.169\ U_{ab}$. Since the output voltage is $1.35\ U_{ab}$ and a boost factor of 1.5 is normal for a boost converter the transformer ratio 'k' can be calculated.

$$k = \frac{1.35 \cdot U_{ab}}{1.5 \cdot 0.169 \cdot \sqrt{2} \cdot U_{ab}} = 3.77 \qquad (5.16)$$

The VA rating of the single-phase transformer is then given by:

$$VA_{\text{sin}\,gle-phase} = 0.169 \cdot U_{ab} \cdot 1.2 \cdot I_o = 0.15\,pu \qquad (5.17)$$

The VA rating of the boost converter is the same as the VA rating of the single-phase rectifier. Also the single-phase transformer is designed to operate at 3 times the fundamental frequency.

5.4.4 Experimental results

An experimental set-up is built in the Power Quality and Power Electronics Laboratory at Texas A&M University. The rectifier of a 480V, 10kW commercially available adjustable speed drive (Danfoss VLT® 5016) is used to retrofit with the proposed approach.

The value of the dc-link inductance is 1.6 mH (2.6%) and the value of the two dc-link capacitors is 2.2 mF (total 10.5%). The rectifier is connected close to a 480 V, 60 Hz, 75 kVA transformer with 6% short circuit impedance. Thus the short circuit ratio is approximately 125. The rectifier is loaded with a 77 Ω power resistor. This equals approximately 5.5 kW. The boost converter is of the continuous conduction mode (CCM) type. The control is performed by two integrated circuits (current controller and multiplier). The reference to the current controller is given by multiplying the rectified voltage U_{hN} and a rms-current reference. The rms-current reference is in this set-up given manually. The switching frequency is about 6 kHz.

Figure 5-48 shows the line current and the Fourier spectrum without the proposed approach. The power is about 5.8 kW. The current THD_i equals 60%. Also a small amount of a third harmonic current can be seen, which indicates some degree of unbalance on the utility grid.

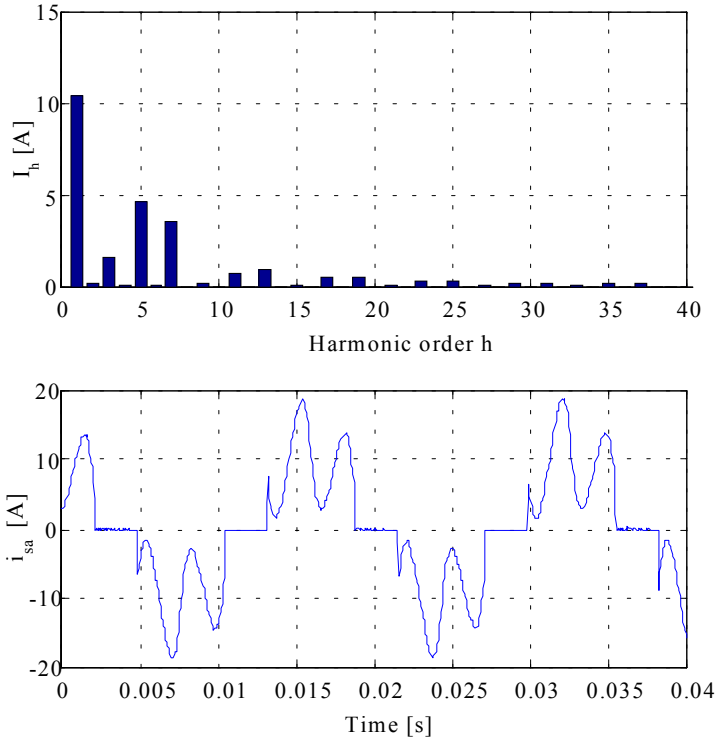


Figure 5-48: The Fourier spectrum and a time plot of the line current without use of the proposed scheme: The THD_i = 60%. The load is approximately 5.8 kW.

Figure 5-49 shows the line current and the Fourier spectrum with the proposed approach. The THD_i equals 19%. It is clearly shown that the amount of the 5^{th} and 7^{th} harmonic current is significantly reduced. The lower plot of Figure 5-49 shows the phase current of the zigzag transformer I_{a3} and the current of the rectifier I_{ar}. It should be noted that the peak current of the rectifier is not higher with the new proposed approach than without, so no derating of the diodes is necessary.

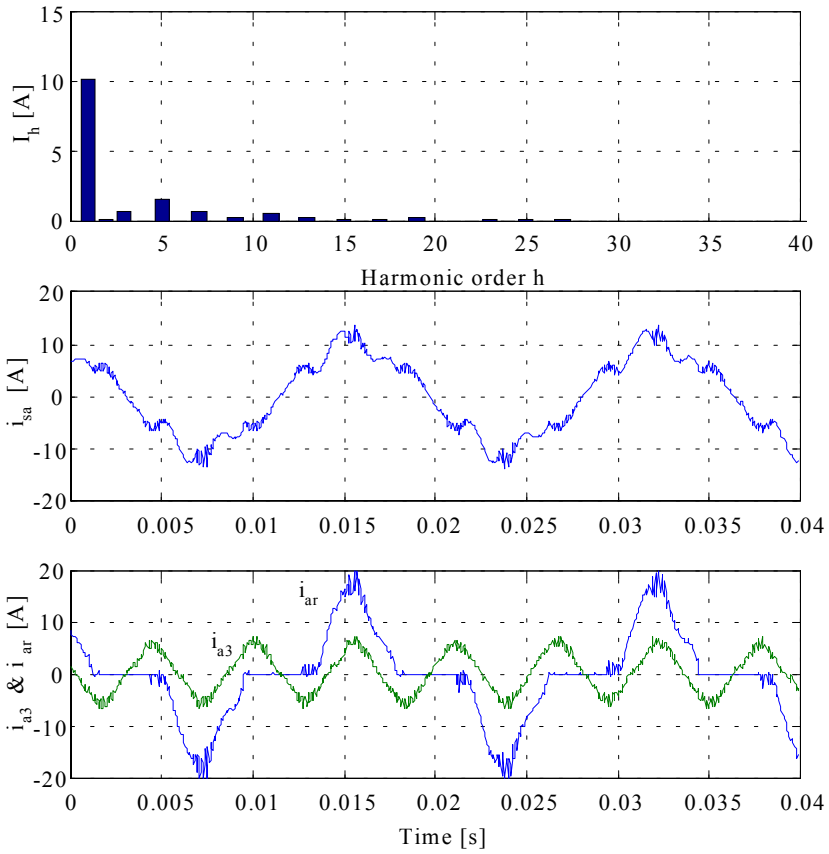


Figure 5-49: The Fourier spectrum and a time plot of the line current with the use of the proposed scheme: The THD_i = 19% and Hc = 190%. The load is approximately 5.8 kW. The lower plot shows the third harmonic current of one transformer phase as well as the phase current in the diode rectifier itself.

Figure 5-50 shows the current and the voltage on the primary side of the single-phase transformer U_{hN}. The lower plot of Figure 5-50 shows the voltage while the converter is not switching. It can be seen that the current i_3 is in shape and phase with the voltage U_{hN}.

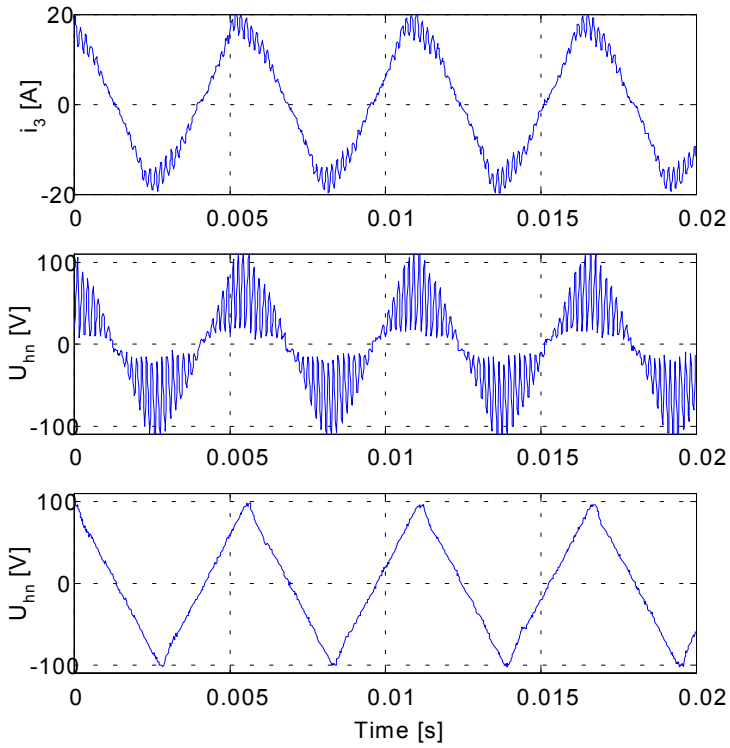


Figure 5-50: The current and voltage of the primary side of the single-phase transformer. The lower plot shows the voltage U_{hN} while the converter is not switching.

5.4.5 Conclusion

In this chapter a new integrated single-switch approach based on the third harmonic injection scheme to improve harmonic performance of standard PWM-ASD's has been presented. The single-switch approach is essentially an add-on solution to standard ASD's. The proposed scheme has shown that a significant reduction of ASD generated harmonics is possible.

The advantages of the proposed scheme are:

- No additional components in the power flow path
- The dc-link voltage has the same level as with a diode rectifier
- The operation of the new scheme is independent of the line impedance
- The approach is an add-on solution. (Once the ASD is modified for the presented scheme, the ASD can easily be sold without the proposal if required
- High reliability because the diode rectifier still works even when the boost rectifier is down
- Using the diode and the IGBT of the dynamic braking circuit, low-cost can be achieved
- Multiple drive connection is possible

One major disadvantage, however, of the presented scheme is that the third harmonic current is circulated through the dc-link capacitor. Compared to a standard diode rectifier decreased lifetime of the dc-link capacitor can therefore be expected.

Based on the analysis of above a THD_i = 10% - 20% and Hc = 125% - 200% is considered as a realistic harmonic performance of the integrated single-switch third harmonic injection scheme.

5.5 Conclusions

In this chapter four selected apparatus level harmonic reduction techniques useful for three-phase rectifiers used in ASD's were presented. Three of the presented rectifier topologies are well known and used in today's ASD's, while the integrated single-switch third harmonic injection scheme is a potential candidate to become a useful rectifier topology in tomorrows ASD's.

Table 5-2 shows the performance indexes such as THD_i, Hc and THD_v. The voltage THD_v is based on the assumption that an ASD with an input power of 300 kW is connected directly to an 1 MVA transformer with a short circuit impedance of 5% (S_{sc}=20 MVA, R_{sce} = 67).

	THD_i [%]	Hc [%]	rms current [%]	THD_v [%]	Comments
Basic diode	35–120	200 - 1000	110 – 150	7.5	Hc = 500% assumed for the THD_v calculation
With ac-coils	30–50	150 – 400	105 - 110	3.8	Hc = 250% assumed for the THD_v calculation
With dc-coils	30–50	150 – 400	105 – 110	3.8	Hc = 250% assumed for the THD_v calculation
12-pulse	10–20	125 – 175	101 – 102	1.9	Hc = 125% assumed for the THD_v calculation
Active Rectifier	5-10	Design depending	100 – 101	Design depending	LCL filters are necessary. Hc and THD_i are depending on the filter design
Third Harmonic	10-20	125 - 200	101 – 102	1.9	Hc = 125% assumed for the THD_v calculation

Table 5-2: Performance index of the high power factor rectifier topologies compared to the basic diode rectifier.

Basically the ac-coil has the same effect as a dc-link inductance. However, the dc-link inductance exhibits some advantages compared to the ac-coils, such as lower losses and compact design. It was shown that adding a 3% - 6% dc-link inductance to the basic diode rectifier a significant reduction of the harmonic currents could be obtained. The final size of the dc-link inductance should be considered as a function of the dc-link capacitor value and the required harmonic performance. However, it was also shown that a maximum short circuit ratio of 333 or an additional 0.3% ac-reactance is required to comply with the PWHD limit of the EN 61000-3-12. The additional line-impedance attenuates especially the higher harmonics because the line-impedance limits the rise of the current during the commutation.

Some simulations of the parallel 12-pulse rectifier were presented and a THD_i of 10.5 % was shown possible. However, it was also shown that the performance of the 12-pulse rectifier is depending on the input voltage quality. Pre-distorted grid results in unequal current sharing of the two parallel rectifier bridges. Therefore, at pre-distorted grid some 5^{th} and 7^{th} harmonic distortion may be expected.

The active rectifier is one of the most elegant solutions for ASD's due to bi-directional power flow, a THD_i of less than 5% is achievable, possible reduced capacitor size and a controllable dc-link voltage, which enhances the speed range of the ASD. However, this is not a low-cost solution. The superior performance comes on the expense of a complex control strategy compared to other solutions, lower efficiency than the diode rectifier and extra switching losses in the inverter. Also EMI becomes a significant issue and EMI filters are necessary to comply with European standards. Furthermore a novel line voltage estimator was presented and it was found that estimator works well even under pre-distorted and unbalanced grid. Thus the estimator has no influence to the overall harmonic performance of the active rectifier.

A novel integrated single-switch approach based on the idea of third harmonic injection is presented in this chapter. The new scheme is essentially an add-on solution to a standard ASD. The proposed scheme has shown that significant reduction of line-side harmonics is possible with the proposed approach. The advantages compared to other solutions, such as no extra components (extra losses) in series with the power flow and independence of the line impedance, makes this approach a potential solution for ASD's. However, the injected current is circulating through the dc-link capacitors, which can result in deceased lifetime of the capacitors compared to a three-phase diode rectifier.

6. System Level Harmonic Reduction Techniques

As mentioned in chapter 1 the diode rectifier exhibits several advantages compared to other known rectifier topologies. Therefore, it is relevant to find competitive harmonic reduction techniques that can reduce the harmonic distortion on a system level and at the same time allow the use of the diode rectifier.

The main purpose of this chapter is to estimate the performance of some selected topologies for reducing the harmonic distortion on a system level. Following topologies are selected are covered in this chapter:

- *Harmonic cancellation by mixing single- and three-phase diode rectifier:* It was proven in Chapter 4 that the 5^{th} harmonic current of the single-phase diode rectifier normally is in counter-phase with the 5^{th} harmonic current of three-phase diode rectifier. Therefore, an analysis is presented that shows significant harmonic cancellation is obtainable by mixing single- and three-phase diode rectifiers. Both simulations and experimental results are verifying the analysis.
- *Quasi 12-pulse rectifier:* In applications where more than two three-phase rectifiers are used it is possible to obtain harmonic cancellation by connecting phase-shifting transformers between the grid and half of the rectifiers. This scheme is often called a quasi 12-pulse topology. Even though this scheme is well known it is not very well documented. Therefore, the harmonic performance of the quasi 12-pulse scheme under various load conditions of the different rectifiers is analyzed and near true multi-pulse performance is shown. Both simulations and experimental results are verifying the analysis.
- *Passive shunt filters:* The passive shunt filter is a well-known topology and often used for especially high power applications. However, the passive filter has some significant drawbacks that need to be addressed. Therefore, the advantages and disadvantages of the passive filter topology are briefly discussed.
- *Active Filters:* Active shunt filters are an emerging technology and an increasing number manufacturer of active filters can be found. The control of the active filter has a significant impact on the harmonic currents cancelled and is therefore discussed. Also some simulations of the active filter are made to estimate the performance of this scheme.

6.1 Mixing Single-Phase and Three-Phase Diode Rectifiers

In Chapter 4 it is shown that the 5^{th} and 7^{th} harmonic current of single-phase and three-phase diode rectifiers often are in counter phase. This knowledge can be used to reduce the system harmonic current distortion by mixing single- and three-phase diode rectifiers. However, in general it can be difficult to predict the cancellation effect, especially when taking the impedance and load dependency of the harmonic currents into account. In this section some simulations as well as experimental results are shown to estimate the harmonic performance when mixing single-phase and three-phase diode rectifiers.

6.1.1 Load and impedance variations

As shown in chapter 4, the harmonic currents of the diode rectifier are influenced by several parameters. Therefore, before a general analysis of the harmonic cancellation effect can be made, some considerations needs to be explained first:

1. In a typical application the three-phase diode rectifier load consists of a few large loads, e.g. ASD's for HVAC units, connected close to the transformer (connected to a strong grid). Typically this kind of load varies as a function of time e.g. with the room temperature. Also this kind of equipment may have a built-in dc-link inductance to reduce the harmonic currents.
2. The single-phase diode rectifier load consists normally of many small loads, e.g. PC's, distributed far away from the supply transformer (connected to a weak grid). Typically, this kind of load is constant e.g. the computers are turned on all day. Also single-phase rectifier tends to be of low cost and therefore these have no input filter.

Considering the above a series of simulations are presented, where a 100 kW three-phase diode rectifier is connected to the grid at a fixed short circuit ratio of 100. The three-phase diode rectifier has a 3% built-in dc-link inductance. The load is varied from 0 – 100%. At nominal load the harmonic currents are as shown in Table 6-1

i_5 [A]	i_7 [A]	i_{11} [A]	i_{13} [A]	THD_i [%]
53.8	25.5	11.8	7.0	43

Table 6-1: Harmonic currents of a 100 kW three-phase diode rectifier with a 3% dc-link inductance at nominal load (Rsce = 100).)

A single-phase diode rectifier of 11 kW (or several PC's with a total load of 11 kW) is connected to each phase. This means that the single-phase load equals a third of the three-phase load per phase. The load is kept constant and the short circuit ratio is varied from 10 to 100.

As shown in Chapter 4 the cancellation effect is most significant on the 5th harmonic current. Figure 6-1 shows a contour plot of the 5th harmonic current when mixing single-phase and three-phase diode rectifier load as a function of the three-phase load and the short-circuit ratio of the single-phase rectifier load.

As expected, when the three-phase load is zero the 5th harmonic of the single-phase rectifier load is highest at a high short circuit ratio. Increasing the load of the three-phase rectifier reduces the 5th harmonic current and the lowest value is obtained when the three-phase load equals the per-phase load of the single-phase rectifier (i.e. the three-phase load = 33%). Surprisingly, even when the three-phase (per-phase) load is three times higher the single-phase load, the 5th harmonic current is still the same or less than the 5th harmonic current of the single-phase rectifier alone.

However, the picture is somewhat different when the single-phase diode rectifier is connected at low short circuit ratio. Here the 5th harmonic current of the single-phase diode rectifier is reduced significantly due to the grid impedance. Therefore, the resulting 5th

harmonic current equals basically the 5th harmonic current from the three-phase diode rectifier only.

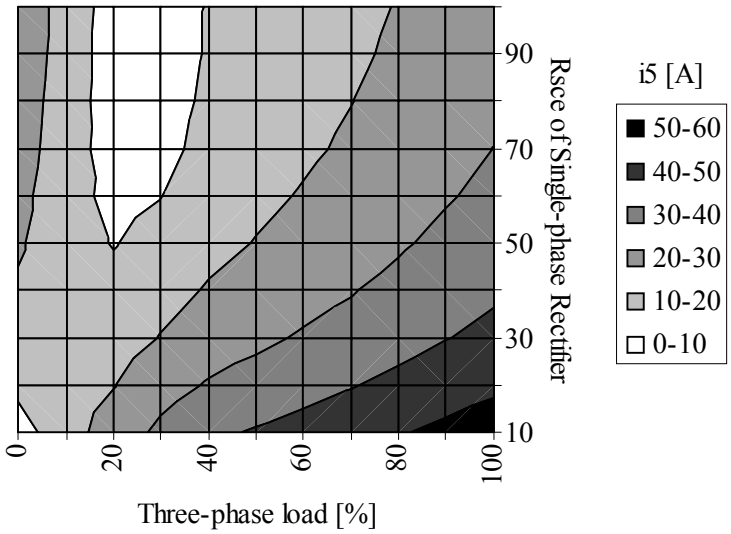


Figure 6-1: Contour plot of 5th harmonic current in absolute values when mixing single-phase and three-phase diode rectifier load as a function of the three-phase load and the short-circuit ratio of the single-phase load.

Figure 6-2 shows the resulting THD_i and again it can be seen that the most significant reduction is obtained, when the single-phase rectifier is connected to a strong grid. As mentioned this is caused by the fact that here the harmonic distortion and especially the 5th harmonic current of the single-phase diode rectifier is largest at a strong grid. It is also shown in Figure 6-2 that the THD_i is reduced even when the three-phase load is three times higher than the single-phase diode rectifier load, and this effect is in general independent of the short circuit ratio of the single-phase diode rectifier. However, this effect is mainly caused by the fact that the harmonic currents are increasing less than the fundamental load.

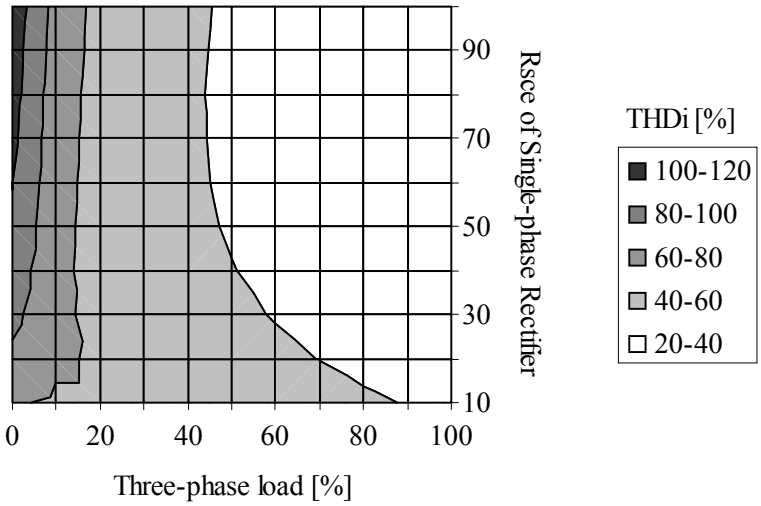


Figure 6-2: Contour plot of the total harmonic current distortion when mixing single-phase and three-phase diode rectifier load as a function of the three-phase load and the short-circuit ratio of the single-phase load.

From Figure 6-1 and Figure 6-2 it can be concluded that the effect of 5th harmonic current cancellation in general is independent of the impedance and load variations. It is also shown that the amount of the 5th harmonic cancellation is very depending on the varying parameters because the amount of the generated 5th harmonic current of the rectifiers is depending on these parameters. Thus, no easy prediction of the harmonic cancellation is possible and this scheme requires case-by-case examination.

6.1.2 Mixing single-phase and 12-pulse rectifiers

Some three-phase rectifier types, such as the 12-pulse rectifier has (ideally) no 5th and 7th harmonic current, therefore no harmonic cancellation by mixing this type of rectifiers with single-phase rectifiers is possible and the distortion of the 5th and 7th harmonic currents remains constant (equal to the single-phase 5th and 7th harmonic currents). To determine if the investment in a 12-pulse rectifier is justified when single-phase diode rectifier load is present in the same system, some SABER simulations are made with the same parameters as above. In this case the short circuit ratio for the single-phase diode rectifier load is fixed at R_{sce} =50.

Figure 6-3 shows the absolute values of the 5th harmonic current and the THD_i when mixing single-phase diode rectifier load with a 12-pulse rectifier. The results are compared to when a 6-pulse diode rectifier is used instead of a 12-pulse rectifier. Obviously, when mixing single-phase diode rectifiers and 12-pulse rectifiers, the 5th harmonic current remains constant and the THD_i is decreasing as the load of the 12-pulse rectifier is increasing (i.e. the fundamental current is increasing more than the harmonic currents). Comparing this result with that of mixing single-phase diode rectifiers with a 6-pulse diode rectifiers it is shown that the 5th harmonic current is actually less up to 50% of the nominal load of the three-phase rectifier (this equals 150% per phase load compared to the single-phase rectifier load.) Also THD_i is less up to 40% load. Finally, a 100% load the THD_i is 30% compared to 25% when using a 12-pulse rectifier.

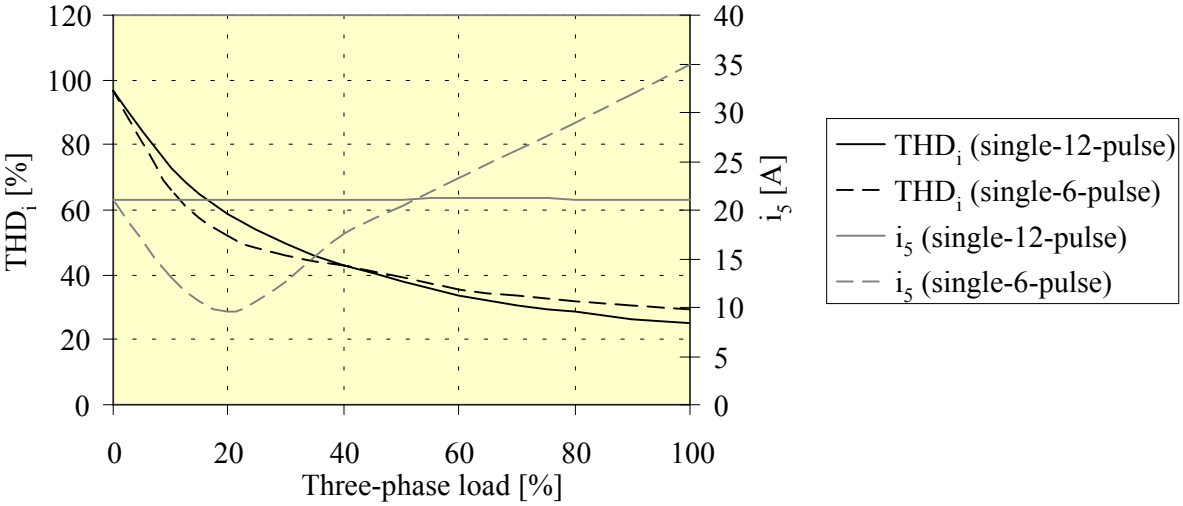


Figure 6-3: Absolute values of the 5th harmonic current and THD_i when mixing single-phase diode rectifier load with 12-pulse rectifier or 6-pulse diode rectifier load.

As mentioned the cancellation is in general difficult to predict. But this example shows that the cancellation effect must be included when considering alternative rectifier topologies to

the three-phase diode rectifier when single-phase diode rectifier loads are present in the same system. In this particular case choosing a more expensive 12-pulse rectifier instead of a 6-pulse diode rectifier shows a worse harmonic performance than the three-phase diode rectifier up to a certain amount of load.

6.1.3 Simulation example of the harmonic current distortion when mixing single- and three-phase diode rectifiers

A plant with an 1 MVA distribution transformer is simulated. The MV line is assumed sinusoidal and balanced. The transformer is loaded with some single-phase diode rectifiers (the total load is 170 kW) and a 170 kW three-phase diode rectifier. The three-phase rectifier is located near the transformer with a 50 m, 90 mm^2 copper cable. The single-phase rectifier loads are evenly distributed on the three-phases with a 200 m, 50 mm^2 copper cable. It is assumed that the single-phase rectifiers are plugged in the wall sockets and therefore a long cable is used for the single-phase rectifiers. Figure 6-4 shows the simulated system.

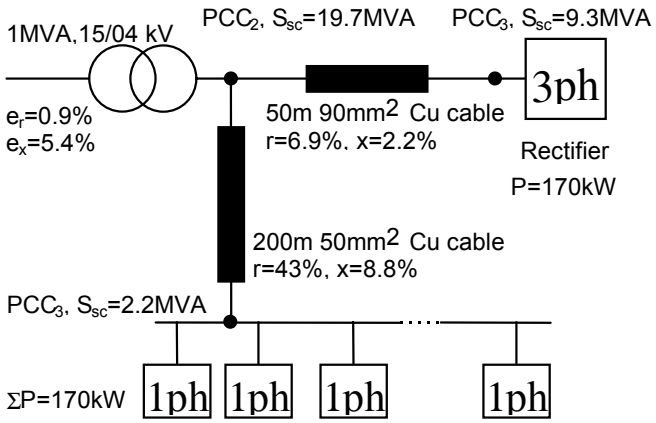


Figure 6-4: Simulated system with transformer, cable and load. The impedance of the cables are shown by their per-unit values related to the transformer

The reactance of the cable is 0.07 Ω/km and the capacitive effects are ignored. The impedance of the cables is shown by their per-unit values related to the transformer. The fundamental voltage drop across the long cable is about 7% at 170 kW single-phase rectifier load. The impedance of the cable is the dominant short circuit impedance as seen from the single-phase rectifiers.

Figure 6-5a shows a simulation result of the currents drawn by the two rectifier groups. The currents add up in the secondary winding of the transformer, which is shown in Figure 6-5b.

Intuitively, it is seen that the two waveforms are supporting each other well. The single-phase current has a "valley filling" effect to the three-phase current, and the resulting waveform looks more sinusoidal than each of the two individual currents.

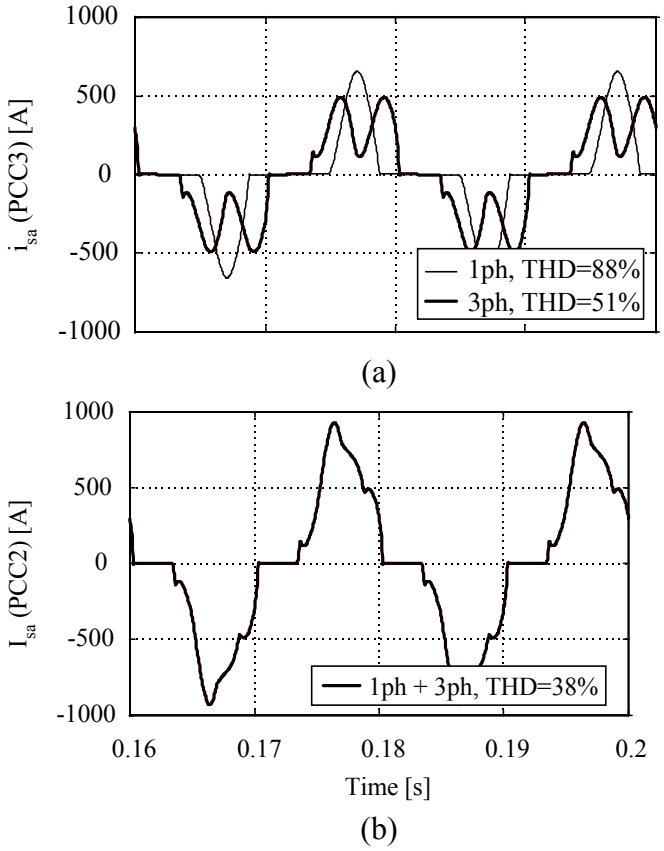


Figure 6-5: Simulated currents drawn in the system (a) Rectifier currents drawn at the PCC 3. (b) Total current in the secondary windings of the transformer (PCC2).

The total harmonic current distortion of the three-phase current is 51% and 88% for the single-phase. When the currents are added in the transformer the resulting distortion is only 38%. This reduction in the distortion is mainly due to 5^{th} harmonic cancellation as it can be seen more clearly from Figure 6-6. Figure 6-6 shows the harmonic spectrum of the three currents of Figure 6-5

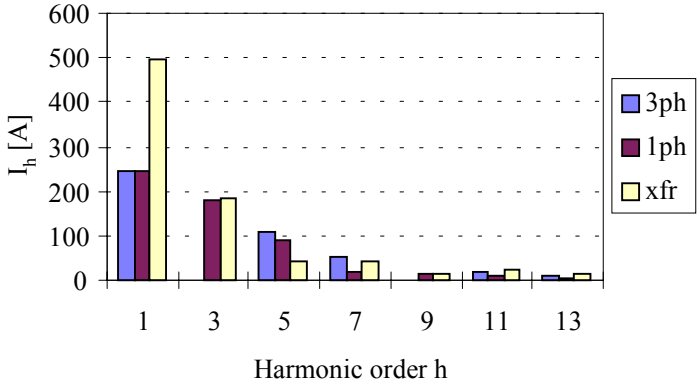


Figure 6-6: Harmonic spectrum of rectifier(1ph and 3ph) and transformer currents (xfr).

The fundamental components of the two rectifier loads add up arithmetically in the transformer. This means that the fundamental components are in phase. The third harmonic is not present in the spectrum of the three-phase load and therefore the third harmonic

component of the single-phase rectifier is seen directly in the transformer. The interesting part is to observe what happens with the 5th harmonic current. In this case a 110 A current from the three-phase rectifier is seen and 90 A from the single-phase rectifier. On the transformer only about 45 A is seen. This is only about 20% of the arithmetical sum of the two rectifier contributions. The 7th harmonic component in the transformer equals less than 60% of the arithmetical sum.

Again it can be concluded that adding a three-phase rectifier to an existing single-phase load will not increase the current THD_i at the transformer but actually lower the THD_i and thereby lower the losses in the transformer. A similar effect can be obtained on the MV-line even if the single-phase non-linear load is fed by a different transformer than the three-phase non-linear load. This is of course provided that the transformers have the same winding arrangement.

6.1.4 Experimental results

On a MV distribution line some measurements were made. The advantage using this setup is that all parameters are known and no other users are disturbing the LV and MV line (see also Appendix A). The system shown in Figure 6-7 is the only load on the distribution system. A three-phase ASD ($S_{nom,1}$ = 50 kVA) with a 5.4% dc-link inductance and a 43% smoothing capacitor is connected to a 200 kVA transformer by a 10 meter cable. The short circuit power at the end of the cable is 3.7 MVA. A single-phase rectifier with a resistive load and no dc-link inductance is connected to phase 'a'.

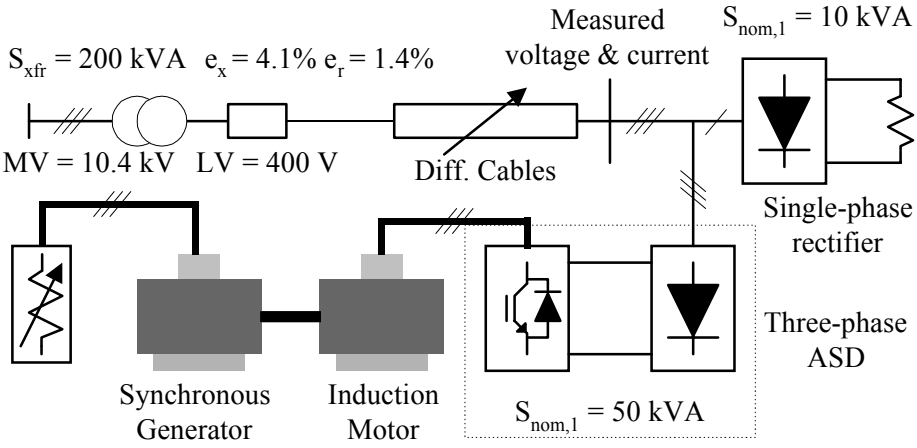
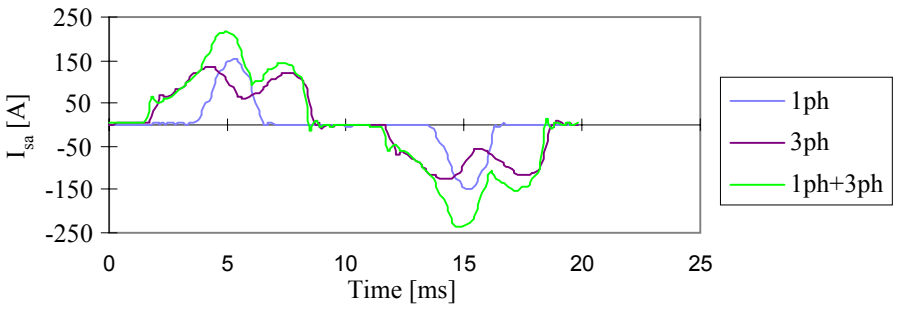
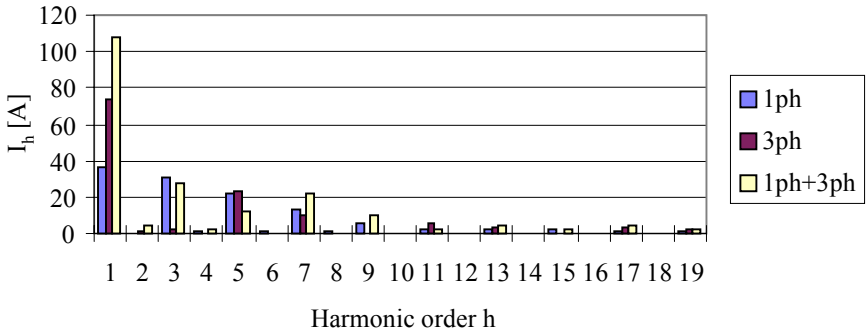


Figure 6-7: Circuit diagram of the load system on the MV distribution line.

The current of the three-phase, single-phase and the sum of both currents are shown in Figure 6-8a. The harmonic currents are shown in Figure 6-8b. It is shown that 5th harmonic current is significantly reduced. The 5th harmonic current of the three-phase load is 22.5 A and the 5th harmonic current of the single-phase load is 23.5 A while the sum only is 12.5 A. This is only 27% of the arithmetical sum of both rectifiers. This is in good agreement with the simulations shown in Figure 6-6 and Figure 6-5. The THD_i of the sum of both currents is 36.5% compared to 113.5% of the single-phase rectifier and 37% of the three-phase rectifier.



(a)



(b)

Figure 6-8: (a) Current of the single-phase and three-phase diode rectifier with the sum of both currents. (b) Harmonic currents of the single-phase and three-phase diode rectifier with the sum of both currents.

Figure 6-9 shows the 5th harmonic voltage as a function of the input power of the ASD. The load of the single-phase rectifier is fixed. At no load of the ASD the 5th harmonic voltage is 1.7%, only generated by the single-phase rectifier. At approximately 11 kW load of the ASD the 5th harmonic voltage has a minimum of 0.06%.

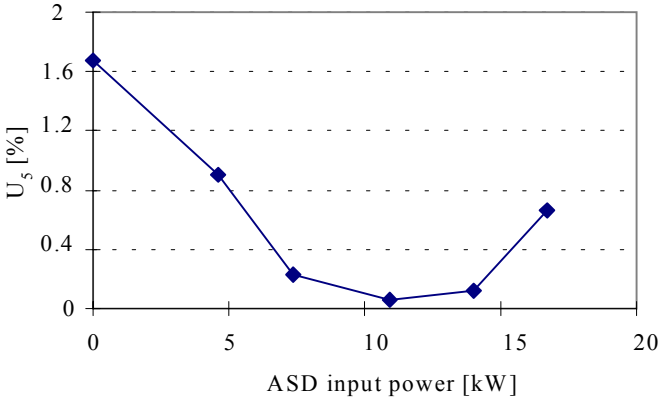


Figure 6-9: 5th harmonic voltage as a function of the drive input power.

These interesting results have also been observed on-site in several applications. Some measurements have been made at an office building. They have been made on a three-phase 32 kVA ASD with a 4.3% dc-link inductance and a 28% smoothing capacitor. The ASD is connected to a 1.5 MVA transformer via a cable. The short circuit power at the end of the cable is 5.4 MVA. A circuit diagram of the system is shown in Figure 6-10. The resulting harmonic voltages are measured as a function of the drive input power.

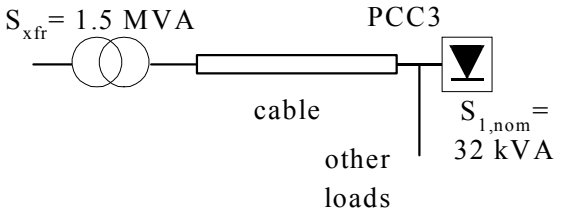
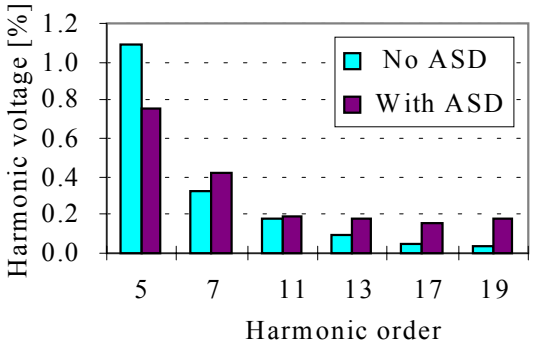


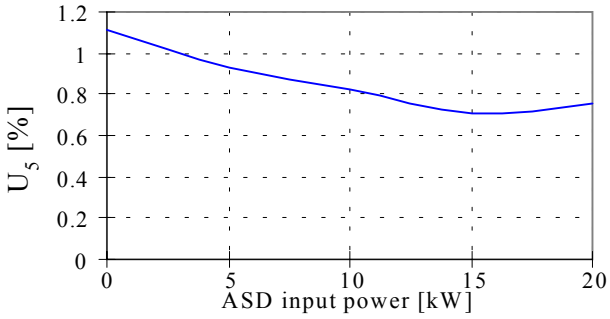
Figure 6-10: Circuit diagram of an office building where the on-site measurements are done.

Figure 6-11a shows the harmonic voltages both without ASD (background voltage distortion) and with the full loaded ASD. The 5th harmonic voltage is lower with the ASD as without. Figure 6-11b shows the 5th harmonic voltage as a function of the drive input power. There is a good agreement to the simulated result shown in Chapter 3 where the background voltage distortion approximately has the same level.

The 7th harmonic voltage is slightly increased. The 11th is remained constant and the 13th is increased. Actually, in this measurement the THD_v was decreased from 1.33% to 1.19% when the ASD was operating.



(a)



(b)

Figure 6-11: (a) Measurements of the resulting voltage distortion with and without a three-phase ASD at the PCC3. (b) 5th harmonic voltage as a function of the drive input power.

6.1.5 Conclusions

Based on the analysis presented above, it can be concluded that a significant amount of 5th harmonic current cancellation can be expected when mixing single- and three-phase diode

rectifiers. However, it is also shown that no easy prediction of the harmonic cancellation is possible and that this scheme requires case-by-case examination. Nevertheless, as shown by an example, the cancellation effect must be included when considering alternative rectifier topologies to the three-phase diode rectifier when single-phase diode rectifier loads are present in the same system. In the presented case choosing a 12-pulse rectifier instead of a 6-pulse diode rectifier showed actually a worse harmonic performance because the 12-pulse rectifier is unable to cancel existing 5^{th} harmonic currents.

The same was shown to be true for the 5^{th} harmonic voltage distortion. Because the harmonic background distortion mainly is caused by a large number of single-phase non-linear loads it is clearly shown that three-phase rectifiers to some level actually can reduce the 5^{th} harmonic voltage and thereby the total harmonic voltage distortion. This is a very important point also, because even clean power converters can result in worse voltage distortion than a three-phase diode rectifier without any extra measures.

6.2 Quasi Multi-Pulse

In applications with multiple converters, solutions combining several separated standard 6-pulse diode rectifier, the so-called quasi 12-pulse topology, can be interesting. The quasi multi-pulse topology is well known. However, the quasi 12-pulse rectifier has the reputation of being sensitive to load variations. The reason for this may be that the quasi multi-pulse rectifier is not very well documented in the literature and very few papers have exploited the possibilities of this very simple scheme. Most papers concerning multi-pulse topologies discuss mainly true multi-pulse configurations i.e. where the converter dc-outputs are connected.

[Hahn et al. 1999] have shown that a significant harmonic reduction can be obtained by the use of a quasi 12-pulse topology on the LV-line. The topology proposed by [Hahn et al. 1999] (harmonic subtractor) is shown Figure 6-12. This approach includes an auto-transformer configuration that often can be found in parallel 12- or 18-pulse topologies (se also Chapter 5.2).

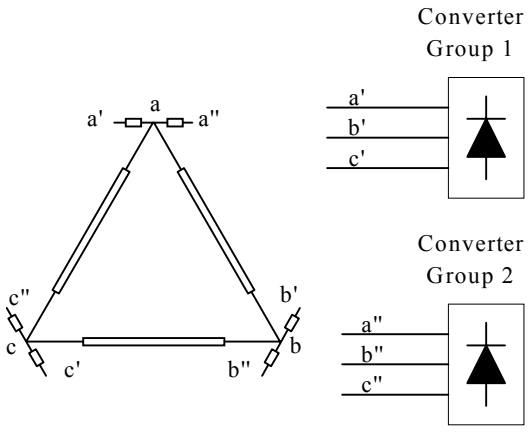


Figure 6-12: The "harmonic subtractor" as proposed in [Hahn et al. 1999].

The harmonic performance under various load conditions was analyzed, while the performance under pre-distorted grid was not investigated. The main advantage of the

"harmonic subtractor" is the low kVA-rating = 18% of the auto-transformer. However, both converter groups must be connected to the transformer.

Dividing the converters on several distribution transformers with different winding arrangement has by [Phipps, Nelson 1993] shown that significant cancellation of the 5th and 7th harmonic can be obtained on the medium voltage line in a large industrial plant. However, the analysis presented is based on controlled rectifiers and the performance with respect to the turn–on angle was investigated. Modern ASD's use 6-pulse (uncontrolled) diode rectifiers of the capacitor load type, where the harmonic profile is somewhat different than for controlled rectifier usually of the inductance load type.

In this section the harmonic performance of the quasi 12-pulse rectifier is analyzed both on the low- and medium-voltage line. Simulations the harmonic currents at various load conditions of the LV- and MV-line topology are presented both with sinusoidal and pre-distorted voltage supply. For the LV-line topology experimental results are verifying the analysis

6.2.1 The LV quasi 12-pulse topologies

In the following a quasi 12-pulse topology is proposed as shown in Figure 6-13 with a 30º phase-shifting auto-transformer with kVA-rating of 23.7%. Only one converter group needs to be connected.

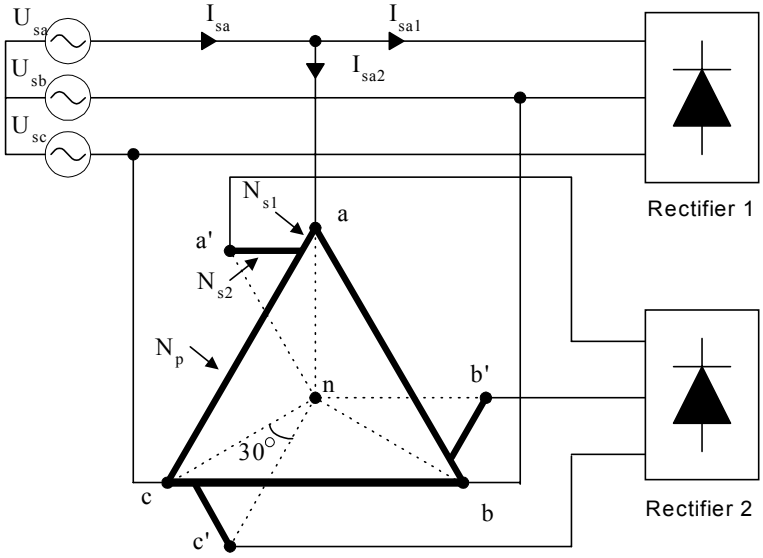


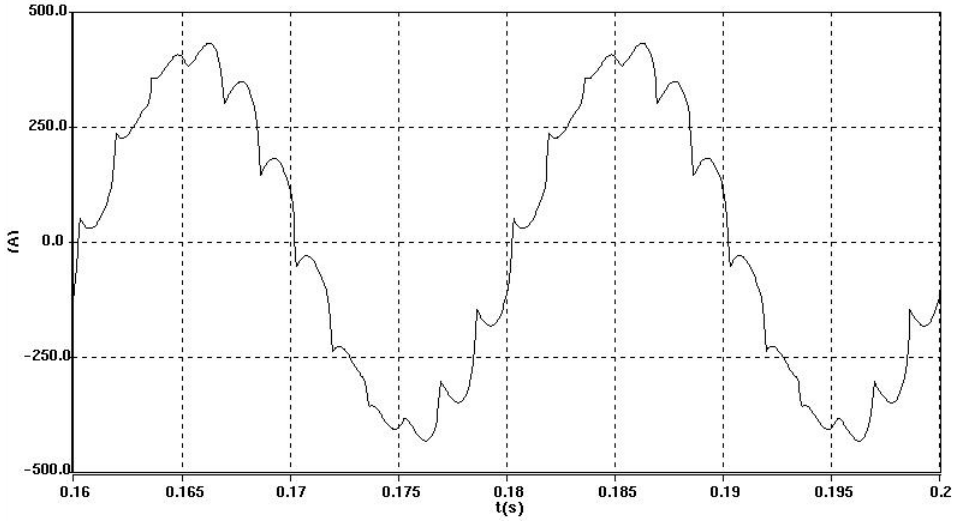
Figure 6-13: Quasi 12-pulse scheme with one auto phase-shifting transformer.

On a 1 MVA 10/0.4 kV supply transformer (e_x = 5% and e_r = 1%) two 100 kW (input power) ASD's are connected with a standard 6-pulse diode rectifier. Rectifier 1 and rectifier 2 have a built-in dc-link inductance of 3%. Without any further measures the total harmonic current distortion THD_i = 38% and the total harmonic voltage distortion THD_v = 3.6% measured at the secondary side of the supply transformer.

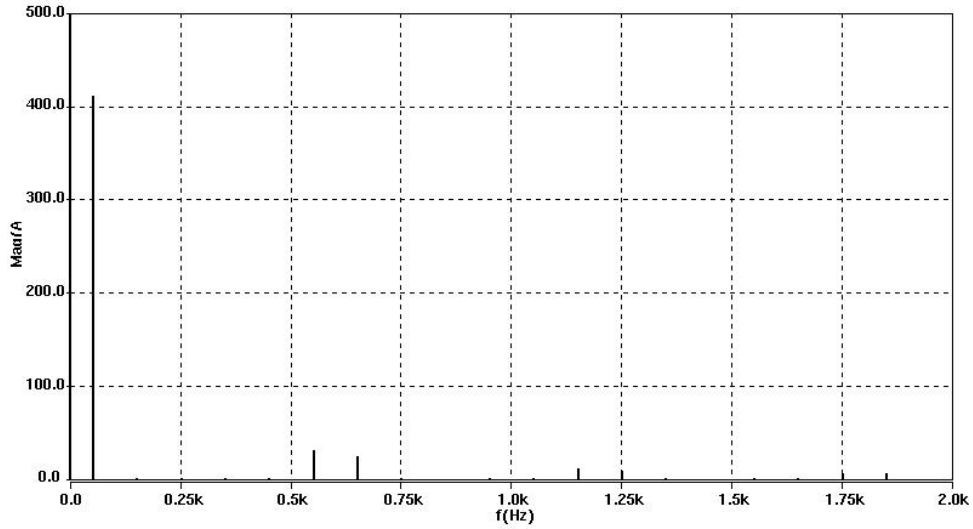
To reduce the harmonic distortion further, rectifier 2 is phase shifted by 30° by means of the auto-transformer connection as shown in Figure 6-13. In the simulations the impedance of the auto-transformer is neglected.

Sinusoidal Grid:

Figure 6-14 shows the simulated system current (i_{sa}) and the corresponding Fourier spectrum when both rectifiers are fully loaded, THD_i = 10.5 %.



(a)



(b)

Figure 6-14: (a) Simulated system current, i_{sa}. (b) Fourier spectrum of i_{sa}. Both rectifier 1 and rectifier 2 are fully loaded.

Figure 6-15 shows the current THD_i as a function of the load of both converter groups. As shown in Figure 6-15 the current THD_i is less than 20% in the main operating area, namely between 40% and 100% of both converter groups. A THD_i of close to 10% is achieved in the operating area between 60% and 100%.

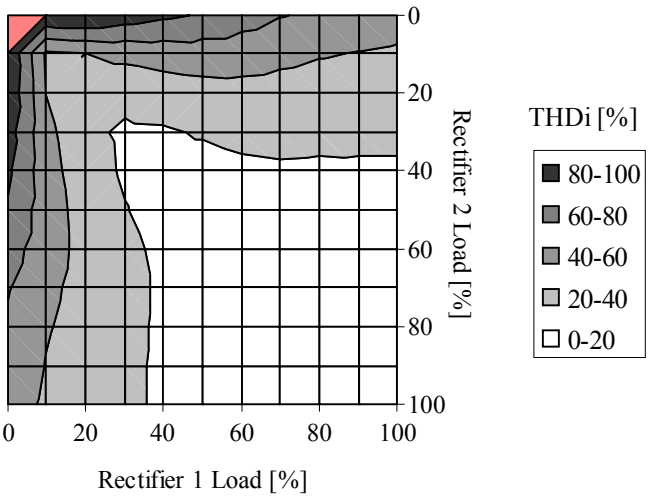


Figure 6-15: Contour plot of the current THD_i as a function of the load of both rectifiers.

Intuitively, one would assume that both the voltage and current THD is smallest when both transformers are equally loaded. But Figure 6-16 shows this is not necessary true. The current THD_i is smallest when both converter groups are fully loaded, while the lowest voltage THD_v is achieved at low load. The maximum voltage distortion is achieved when either both converter groups are fully loaded or only one converter group is fully loaded and the other converter group is unloaded. It should be noted that the maximum voltage distortion is cut by almost a factor of 2 compared with the voltage distortion obtained without the phase shifting transformer (THD_v=3.6%).

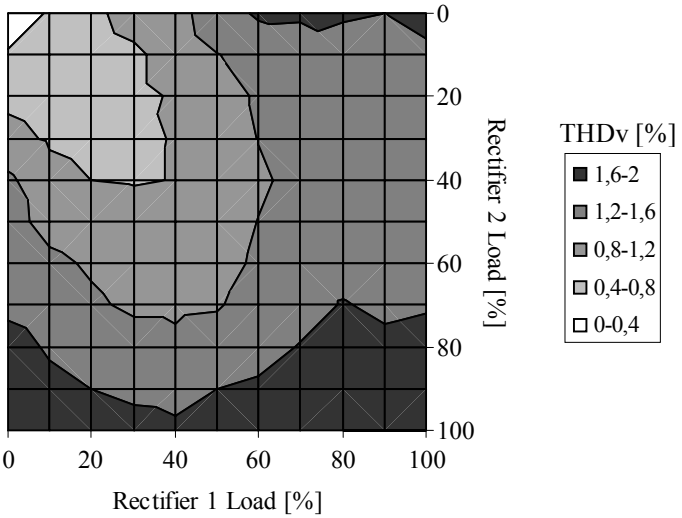


Figure 6-16: Contour plot of the voltage THD_v as a function of the load of both rectifiers.

For a detailed analysis the current for the 5th and 11th harmonics are shown in Figure 6-17 and Figure 6-18. The 7th harmonic current has a similar profile as the 5th harmonic current, while the 13th harmonic current has a similar profile as the 11th harmonic current. Also the resulting voltages are proportional to the currents why these not are shown here.

As expected the 5th harmonic current is smallest when both transformers are equally loaded. The 11th harmonic is increasing with total load. This is also the reason for that the

voltage THD_v is not smallest when both transformers are equally loaded; the 11^{th} and 13^{th} harmonic voltage are highest at high load.

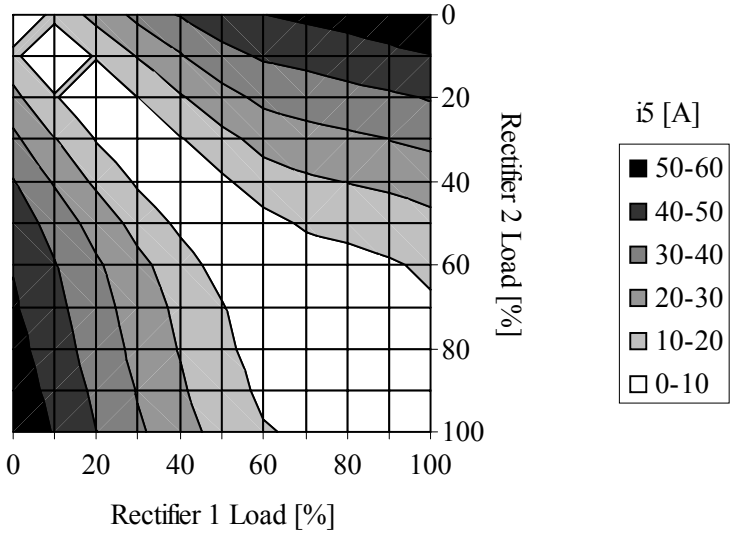


Figure 6-17: Contour plot of the 5^{th} harmonic current as a function of the load of both converter groups.

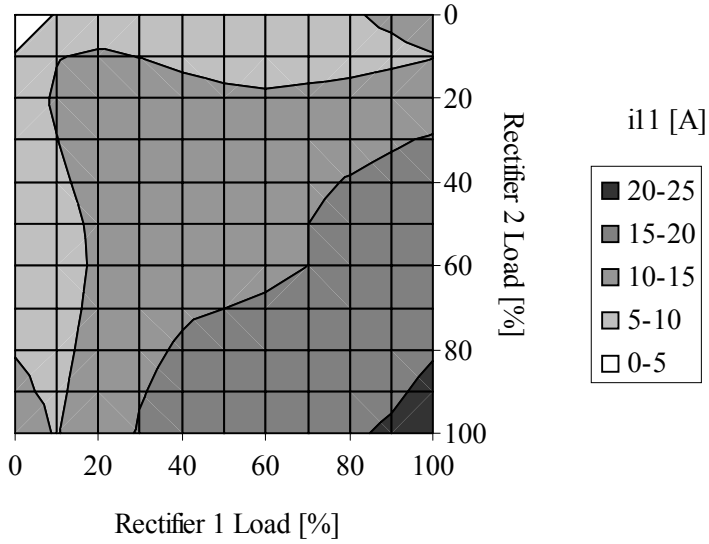


Figure 6-18: Contour plot of the 11^{th} harmonic current as a function of the load of both converter groups.

As shown the quasi 12-pulse has an excellent performance even under wide load variations. The reason for this is that the harmonic currents of the three-phase diode rectifier mainly are almost constant in the CCM as shown in Chapter 4.6.

Pre-distorted grid

To determine if the quasi 12-pulse scheme also is suitable at pre-distorted grid some simulations are made where a 3% 5^{th} harmonic voltage is added to the supply voltage. The phase angle of the 5^{th} harmonic is 180°. This results in a flat-topped line-neutral voltage. The line-neutral voltage on the secondary side of the phase-shift auto-transformer, however, will become triangular.

The harmonic current of a 6-pulse rectifier increases when the pre-distorted voltage is flat-topped, while the harmonic current decreases when the voltage is triangular. In other words, the harmonic currents of rectifier 1 increases, while the harmonic current of rectifier 2 decreases. Therefore, the lowest system harmonic current distortion is not achieved when both rectifiers are equally loaded, but when the rectifier 1 is loaded less.

This is also shown in Figure 6-19. Again the THD_i is plotted as a function of both rectifier loads. The lowest distortion is found when rectifier 1 is loaded 40 % while rectifier 2 is loaded 100%. The THD_i in this case equals 15.6 %. However, the THD_i is still less than 20 % in a wide load range.

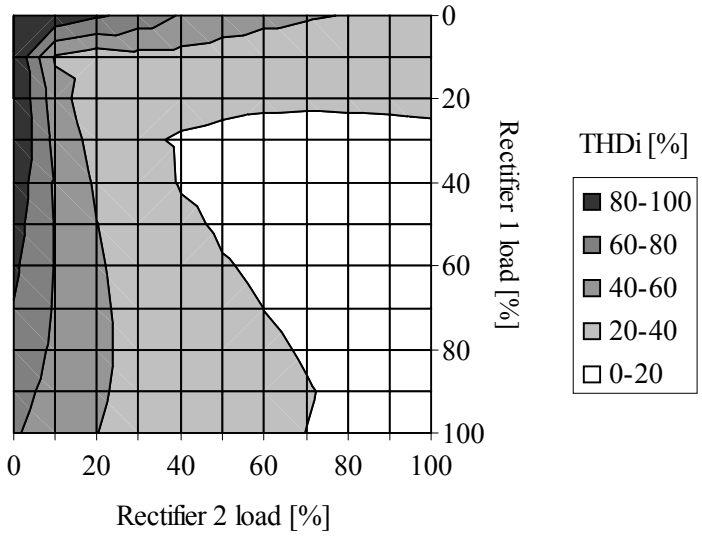


Figure 6-19: Contour plot of the simulated THD_i as a function of t he load of both rectifiers at pre-distorted grid.

Figure 6-20 shows the total harmonic voltage distortion as a function of the load of both rectifiers. The lowest distortion is actually found when rectifier 1 is fully loaded and rectifier 2 is unloaded. The reason for this is shown in Figure 6-21. The generated 5^{th} harmonic voltage of rectifier 1 cancels the pre-existing 5th harmonic voltage, while the generated 5^{th} harmonic voltage of rectifier 2 is in phase with the pre-existing 5^{th} harmonic voltage and is therefore contributing to the voltage distortion.

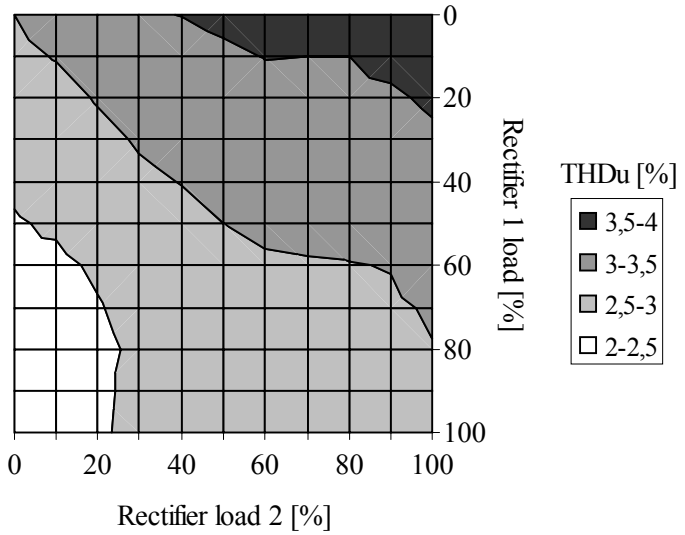


Figure 6-20: Contour plot of the simulated THD_v as a function of the load of both rectifiers at pre-distorted grid.

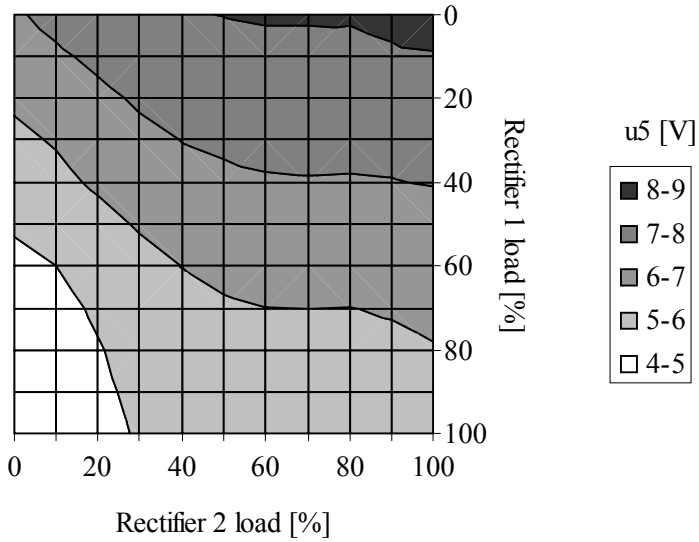


Figure 6-21: Contour plot of the 5th harmonic voltage as a function of the load of both rectifiers at pre-distorted grid.

6.2.2 Comparison of quasi 12-pulse with true 12-pulse rectifier

At sinusoidal voltage a 200 kW true 12-pulse rectifier is simulated on the same grid as the above simulations. The THD_i at full load equals 11 % and the maximum voltage distortion THD_v is 2.0 %. So for a sinusoidal grid the quasi and true 12-pulse rectifier schemes are comparable with respect to maximum voltage distortion generated and low THD_i at full load.

A major difference of these two approaches shows at pre-distorted grid. At pre-distorted grid, the true 12-pulse rectifier has the same problems as the quasi 12-pulse rectifier with respect to different harmonics generated by the two 6-pulse rectifiers and no complete cancellation of the 5th and 7th harmonic current which is also shown in Chapter 5.2. However, using the true 12-pulse rectifier the load-factor between both 6-pulse rectifiers

remains the same and the lowest simulated THD_i = 16 % at full load. The simulated voltage distortion THD_v equals 2.8 %. In a quasi 12-pusle rectifier the load factor between the individual rectifiers can easily be changed. I.e. instead of having the same amount of rectifiers connected to the grid and phase shifting transformers. A larger amount can be connected to the transformer instead of the grid or visa-verse depending on the phase angle of the pre-distorted grid.

Roughly spoken, it is possible to correct for the effects caused by a pre-distorted grid, by connecting twice the amount of rectifier on the auto-transformer as to the grid, when the pre-distorted line-neutral voltage is flat-topped. If the pre-distorted grid is triangular twice the rectifiers can be connected directly to the grid than to the transformer. This is a major advantage compared to the true 12-pulse rectifier, where a low harmonic current distortion not easily can be achieved at a pre-distorted grid.

As shown in Chapter 2 the harmonic voltage distortion is the main objective of the harmonic limiting standards and a THD_v of less than 5 % is often required. Considering this, it should be noted that pre-existing voltage distortion can be cancelled by the quasi 12-pulse rectifier scheme as shown in Figure 6-20 and Figure 6-21. Depending on the phase-angle of the existing voltage distortion a larger amount of rectifiers can be connected to the phase-shifting transformer as to the grid or vice-versa (Ironically, a increased current distortion gives the lowest voltage distortion). In severe cases all rectifiers can be connected directly to the line for maximum current distortion but with the lowest resulting voltage distortion. This feature makes the quasi 12-pulse rectifier scheme unique and superior to the true 12-pulse rectifier scheme.

6.2.3 Experimental results

For the experimental results a 10 kVA autotransformer as shown in Figure 6-13 and two three-phase diode rectifiers with a nominal power of 2.2 kW was used. One rectifier was directly connected to the voltage supply while the other was connected through the phase-shifting transformer. As voltage supply a 15 kVA static Power Generator of the type California Instrument was used. The static Power supply can be seen as a stiff voltage source, therefore no voltage distortion measurements are possible. The frequency was set to 50 Hz and the line-line voltage was 400 V on the power supply.

Sinusoidal Grid:

Figure 6-22 shows the measured current THD_i while Figure 6-23 and Figure 6-24 shows the measured 5^{th} and 11^{th} harmonic current respectively as a function of the load of both rectifiers. Very good agreement to the simulations shown in Figure 6-15, Figure 6-17 and Figure 6-18 can be found.

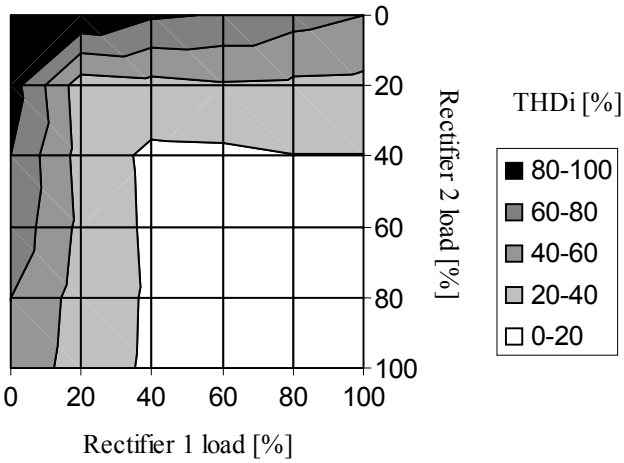


Figure 6-22: Contour plot of the measured current THD_i as a function of the load of both rectifiers.

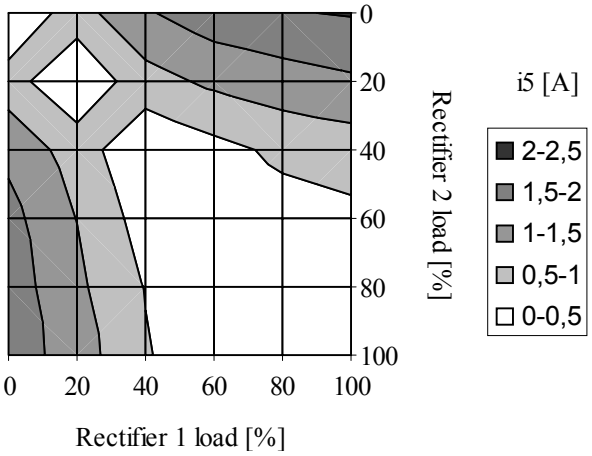


Figure 6-23: Contour plot of the measured 5^{th} harmonic current as a function of the load of both rectifiers.

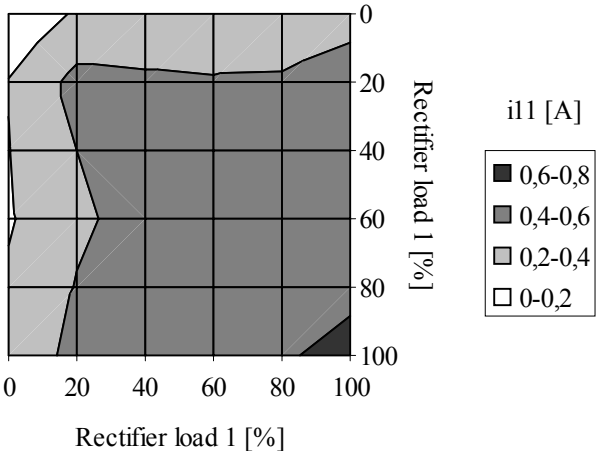


Figure 6-24: Contour plot of the measured 11^{th} harmonic current as a function of the load of both rectifiers.

A total of 36 measurements have been made to verify the simulations. Figure 6-25 shows the measured system current when both rectifiers are fully loaded. Figure 6-26 shows the Fourier spectrum of the measured current.

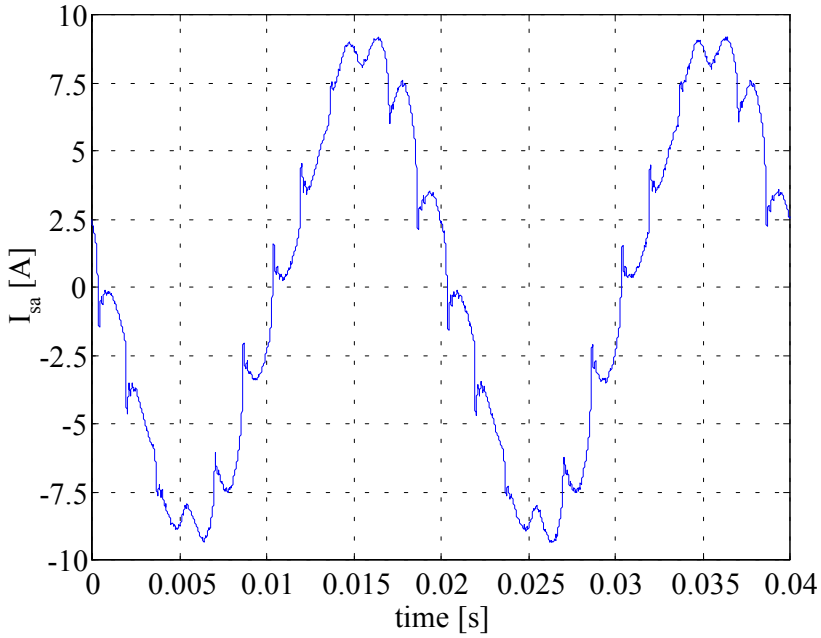


Figure 6-25: The measured system current when both rectifiers are fully loaded.

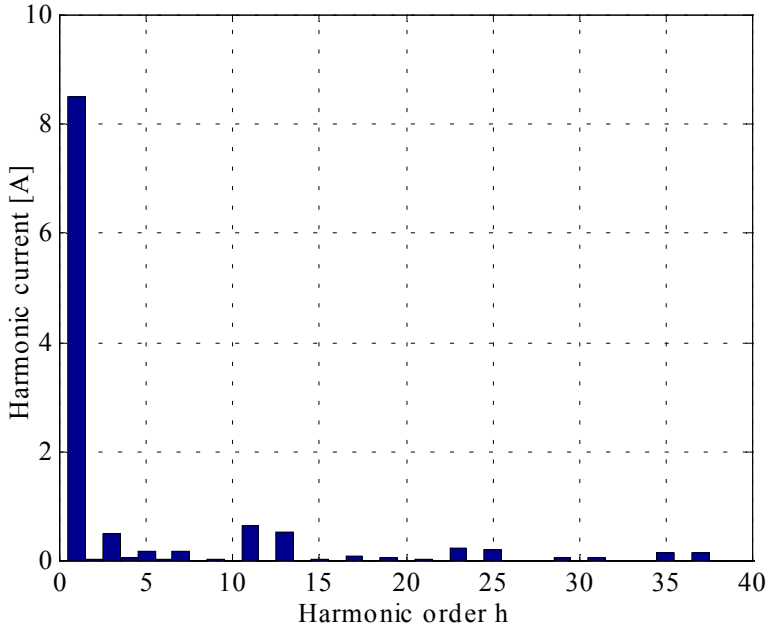


Figure 6-26: The Fourier spectrum of the measured system current when both rectifiers are fully loaded.

The measured THD_i equals 12.5% and Hc = 173%. Recognizing that the mains impedance mainly reduces the higher harmonics and remembering that the present measurements were made on a stiff voltage supply, it is safe to state that the expected Hc and thereby the expected voltage distortion will be somewhat lower in a real application. Basically, a true 12-pulse performance is achieved for a wide load range and a reduction of the voltage

distortion by a factor of two can be expected compared to a 6-pulse diode rectifier with dc- or ac-coils.

Pre-distorted grid

Some extra measurements were made where a 3% 5th harmonic voltage was added to the supply voltage. The phase-angle of the 5th harmonic was 180° as in the simulations of above.

As for the simulations the lowest distortion is found when the rectifier connected directly to grid is loaded 40% while the rectifier connected to the auto-transformer is loaded 100%. This is in very good agreement with the simulations of above.

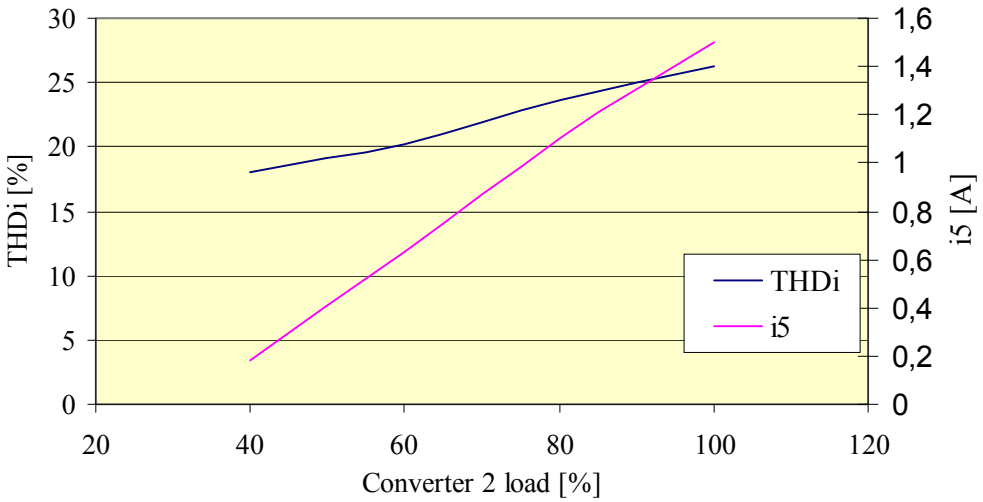


Figure 6-27: The THD_i and 5th harmonic current as a function of the load of the rectifier connected directly to grid, while the rectifier connected to the auto-transformer is loaded 100%.

Figure 6-28 shows the system current when the rectifier connected directly to grid is loaded 40% while the rectifier connected to the auto-transformer is loaded 100%. Figure 6-29 shows the Fourier series of the system current.

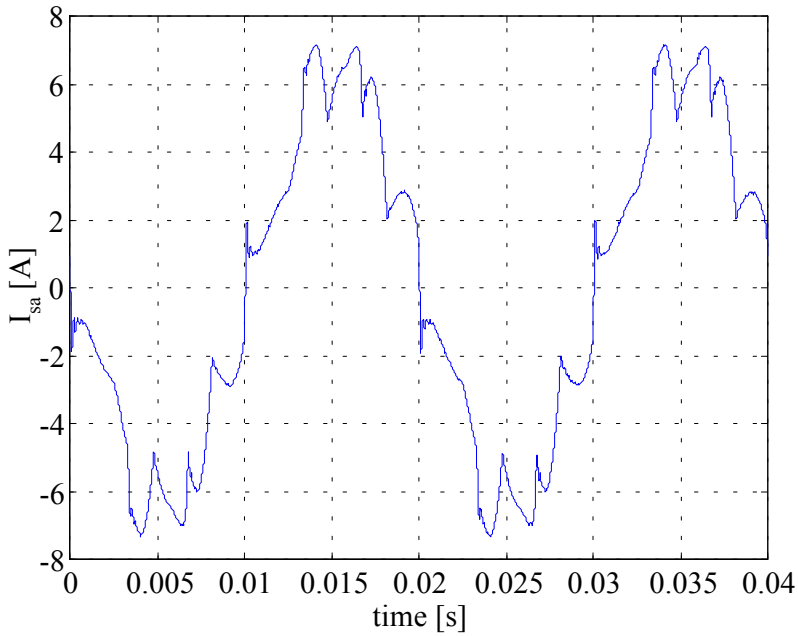


Figure 6-28: The measured system current when the rectifiers rectifier connected directly to grid is loaded 40% while the rectifier connected to the auto-transformer is loaded 100%.

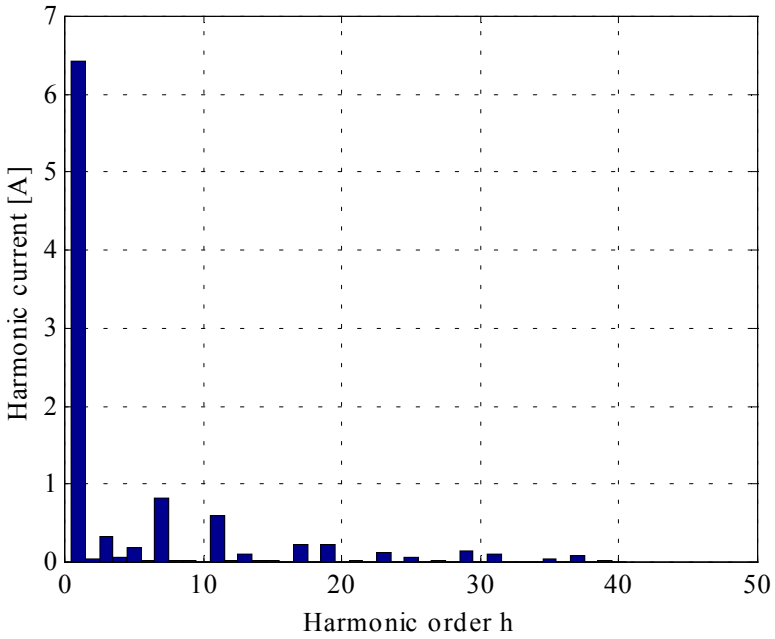


Figure 6-29: The Fourier spectrum of the measured system current when the rectifier connected directly to grid is loaded 40% while the rectifier connected to the auto-transformer is loaded 100%.

6.2.4 MV quasi multi-pulse topology

Dividing the converters on several distribution transformers with different winding arrangement, multi-pulse performance on the medium voltage (MV) line can be assured. A 12-pulse solution for several converters is shown in Figure 6-30. This scheme has in

[Phipps, Nelson 1993] shown to be a cost effective measure to limit the harmonic distortion in large industrial plants.

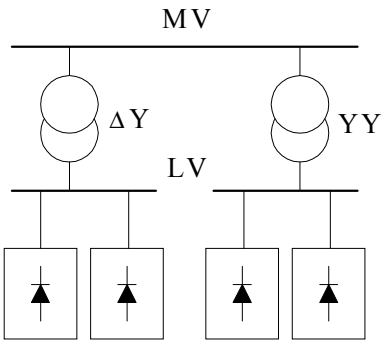


Figure 6-30: 12-pulse solution for several converters.

Again the harmonic performance of this scheme is depending on the load profile of each transformer/converter. This is analyzed in the following.

The performance analysis is made with two supply transformers with different winding arrangement on the primary side (star/star and delta/star). Both transformers have the same size (1 MVA) and impedance (e_x = 5%, e_r = 1%). The primary line-line voltage equals 10 kV, and the secondary line-line voltage equals 400 V. The simulations are made for three-phase diode rectifiers with a 3% dc-link inductance. Each transformer is loaded with 80% rectifier load.

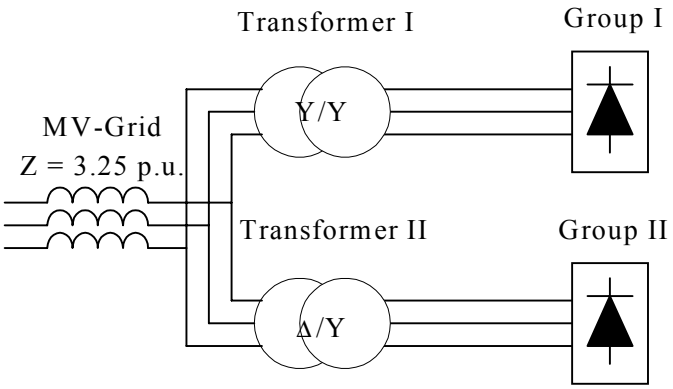


Figure 6-31: The simulated system with the per unit notation with respect to the transformer secondary side.

The next step is to simulate the expected voltage and current distortion on the MV-line as a function of the load profile of the two transformers and of the MV-line impedance. Furthermore the influence of a pre-distorted grid is investigated. The measured data from an actual MV-line (see also chapter 3) are used.

It should be noted that the voltage distortion is a function of the MV-line impedance. The system shown in Figure 6-31 is simplified and the impedance is a linear inductance. Normally, this is not the case and parallel loads such as power factor correction capacitors, generators and motors can be expected to be connected on the MV-line. It is out of the scope of this section to analyze the performance on the presented approach for all these MV-line configurations. However, if the current harmonics are known it is possible to

calculate the harmonic voltage if the system parameters are known. In the presented simulations the MV-line is assumed to be linear with short circuit power of 200 MVA. The current harmonics generated are expected to be independent of the MV-line configuration.

Sinusoidal Grid

Again it can be seen that the current THD_i is smallest when both transformers are fully loaded and the THD_i is less than 20% in a large area. The voltage THD_v is decreasing when the total load is decreasing and the maximum distortion is achieved when either both transformers are fully loaded or one transformer is fully loaded and the second transformer is unloaded.

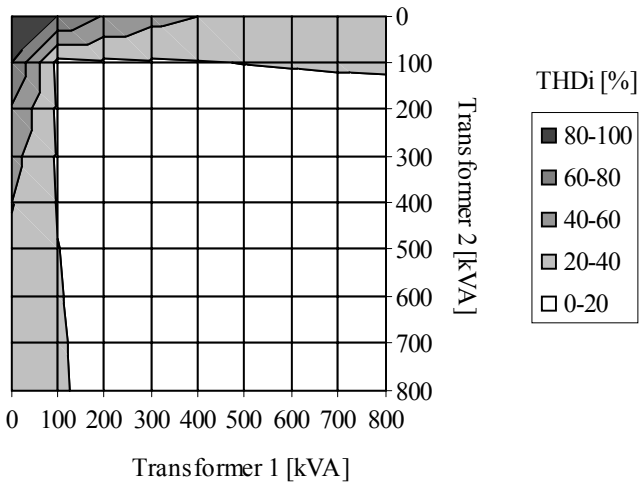


Figure 6-32: Contour plot of the current THD_i as a function of the load of the star/star and delta/star transformer.

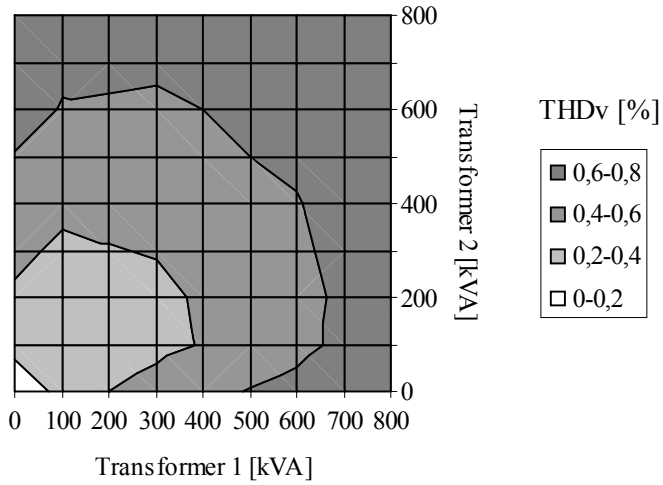


Figure 6-33: Contour plot of the voltage THD_v as a function of the load of the star/star and delta/star transformer.

The current for the 5th and 11th harmonics are shown in Figure 6-34 and Figure 6-35. As expected the 5th harmonic current is smallest when both transformers are equally loaded. The 11th harmonic is increasing with the total load.

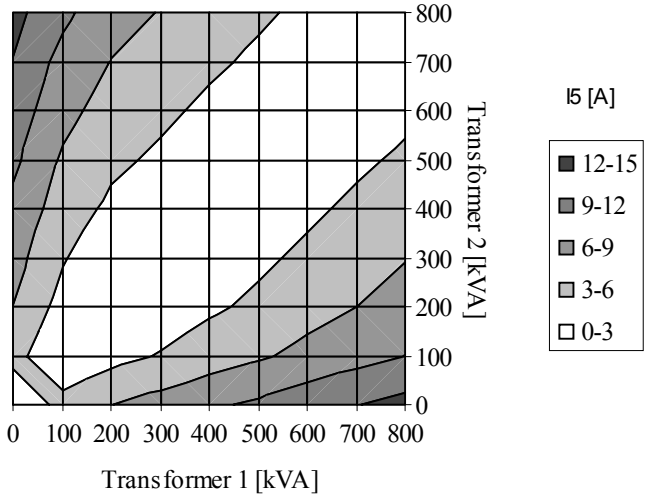


Figure 6-34: Contour plot of the 5th harmonic current as a function of the load of the star/star and delta/star transformer.

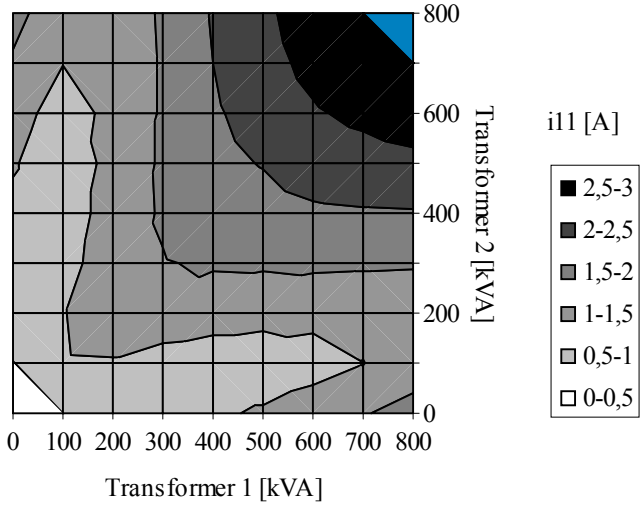


Figure 6-35: Contour plot of the 11th harmonic current as a function of the load of the star/star and delta/star transformer.

Pre-distorted grid

As shown in Figure 6-36 and Figure 6-38 the harmonic currents are hardly affected by the pre-distorted grid. However, the minimum 5th and 7th (7th is not shown) harmonic currents are not exactly obtained when both transformers are equally loaded any more. Also the harmonic 7th, 11th and 13th harmonic voltages are not affected (not shown). The interesting part takes place with the 5th harmonic voltage and the voltage THD_v as shown in Figure 6-37 and Figure 6-39. Both the 5th harmonic voltage and the voltage THD_v have their minimum when the star/star transformer is unloaded and the delta/star is fully loaded. This is because the 5th harmonic voltage generated by the 5th harmonic current of the star/delta transformer is in counter-phase with background harmonic distortion (mainly caused by single-phase diode rectifiers connected to a delta/star transformer). The 5th harmonic voltage distortion caused by the star/star transformer is in phase with the background harmonic distortion.

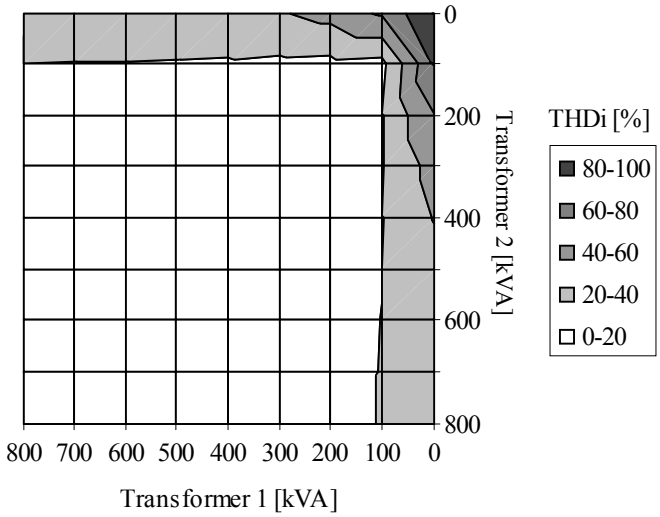


Figure 6-36: Contour plot of the current THD_i as a function of the load of the star/star and delta/star transformer on a pre-distorted MV-grid.

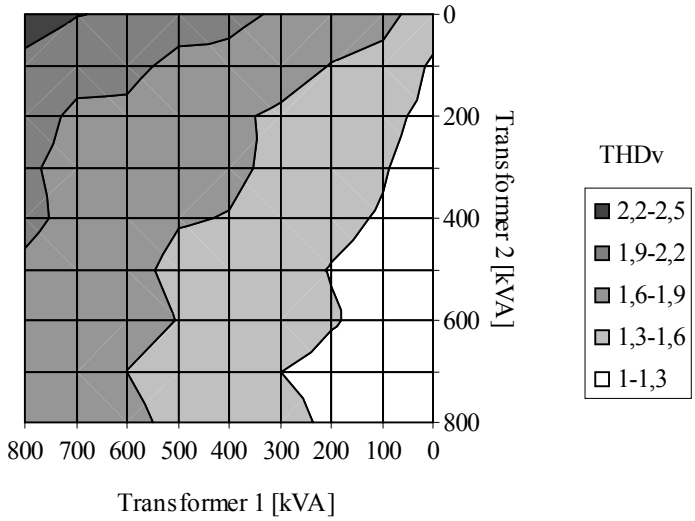


Figure 6-37: Contour plot of the voltage THD_v as a function of the load of the star/star and delta/star transformer on a pre-distorted MV-grid. MV-grid.

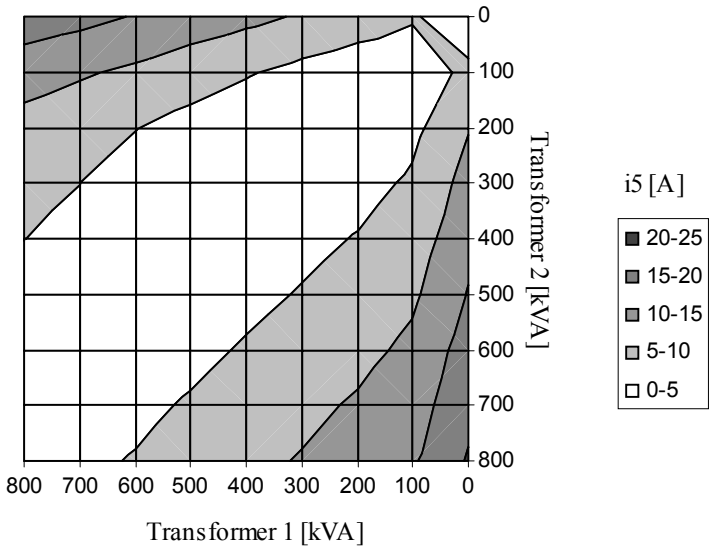


Figure 6-38: Contour plot of the 5th harmonic current as a function of the load of the star/star and delta/star transformer on a pre-distorted MV-grid.

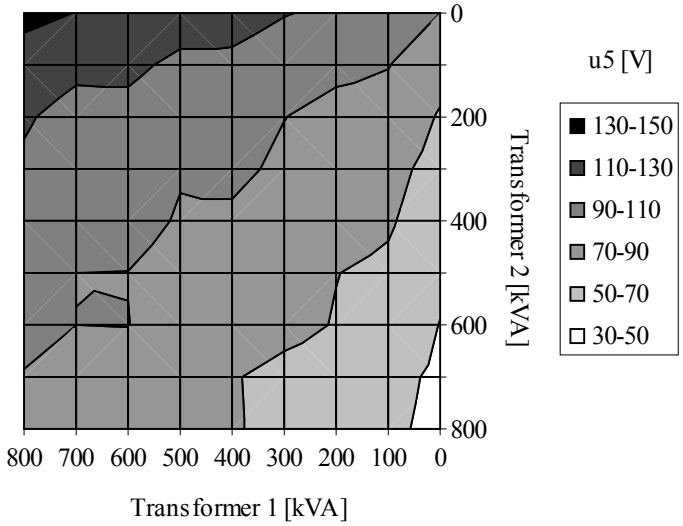


Figure 6-39: Contour plot of the 5th voltage as a function of the load of the star/star and delta/star transformer on a pre-distorted MV-grid.

6.2.5 Conclusion

Based on the analysis presented above it can be concluded that both the quasi 12-pulse rectifier for the LV- and MV-line shows excellent harmonic performance. With a THD_i of less than 20% in most of the operating area, the quasi 12-pulse topology is shown to be competitive to a true 12-pulse rectifier. (e.g. a THD_i = 10% – 20% and Hc = 100% - 200% is considered a realistic harmonic performance of this scheme.) It is stated that a reduction of the voltage distortion by a factor of two can be expected compared to a 6-pulse diode rectifier with dc- or ac-coils.

Also the quasi 12-pulse topology shows possibilities to compensate for effects caused by pre-distorted grid. This is not possible for a true 12-pulse rectifier. Furthermore, the quasi 12-pulse topology can easily be achieved with the use of different transformer arrangements. E.g. a standard star/delta isolation transformer can be used instead of the presented 30° phase shifting auto-transformer or the harmonic subtractor.

For large new plants quasi multi-pulse performance on the MV-line should be considered. However, as shown the performance is very depending on the amount of background distortion. If there is some amount of background distortion on the MV-line, and assuming that this distortion comes from single-phase diode rectifiers, the best result is obtained by just connecting the converters to a delta/star transformer.

6.3 Passive Filter

Often large industrial plants have shunt capacitor banks for displacement power factor correction and since capacitors have low impedance to currents with higher frequencies it is obvious to use these capacitor banks for filtering of harmonic currents. The power source impedance can often be represented by a simple inductive reactance and the simplest filter approach is to just connect the shunt capacitor bank directly to the grid. However, this can be very dangerous due to parallel resonance as explained in chapter 3. Also this may not be satisfactory because a large capacitor rating would be required to provide low impedance at the 5th harmonic. And using a capacitor bank with more VAr compensation than used in the plant would result in leading power factor and possible over-voltage.

6.3.1 Basic design issues

The usual strategy is to divide the capacitors into several banks, add series reactors and series tune each bank for different harmonic frequencies [Cameron 1993]. By providing a low impedance path to the harmonic currents the resulting harmonic voltage is reduced. A general arrangement of multiple parallel path filters is shown in Figure 6-40. Low impedance path for specific harmonics are obtained by series-tuned inductor/capacitor elements connected across the supply bus. One of the filters can include a resistor parallel to the inductor to attenuate higher order harmonics.

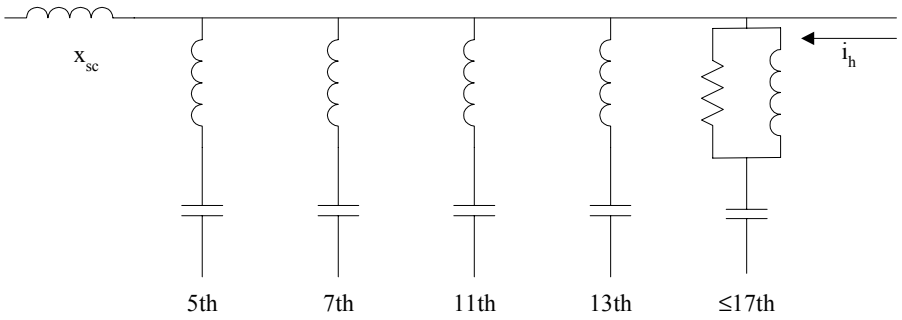


Figure 6-40: Arrangement of multiple parallel path filters using series tuned harmonic filters.

Parallel resonance will still occur but at a lower frequency than the frequency of the lowest tuned capacitor. This is also the reason why it is not advisable to apply filters tuned for higher order harmonics and not the lower orders. For example, if a 12-pulse rectifier is used one could be tempted to apply a shunt filter for the 11th and 13th harmonic current

only. This can have fatal consequences because the parallel resonance frequency will be below the 11th harmonic order and probably close to the 5th or 7th harmonic order. Even though the 5th and 7th harmonic currents of the (non-ideal) 12-pulse rectifier are small, if they are injected at the resonance frequency this will result in very high harmonic voltages and possible damage of other equipment.

If a filter is tuned exactly to the harmonic frequency, e.g. the 5th harmonic, it will offer low impedance at that frequency. This is helpful for filtering, but the tuned circuit will also accept 5th harmonic currents from throughout the utility system and may become overloaded. Therefore the filters for the 5th harmonic are normally detuned to resonate at a frequency below the 5th harmonic e.g. 4.7 or 4.8 times the fundamental frequency. This reduces the filtering effect but also reduces the possibility of overloading. Also this is a guard against the tuned frequency and the associated parallel resonance frequency to shift upwards due to loss of capacitance (blown fusses, manufacturing tolerances etc.) or an increased power system short circuit capacity. However, even if the filter is detuned to a slightly lower frequency, the amount of harmonic currents coming from the power system must be included in the rating of the filter, i.e. the background voltage distortion must be know to estimate the harmonic current coming from the power system.

Taking the above problems into account a general approach to design passive filters for a given plant is as follows [McGranaghan, Mueller 1999]:

1. Characterize the harmonic producing loads
2. Characterize the power system background voltage distortion
3. Design of the filters tuned to individual harmonics (slightly less), starting with the 5th harmonic
4. Calculate harmonic distortion. If the distortion level is above the required levels repeat step 3 and 4 with the next harmonic frequency, e.g. the 7th harmonic

If filter stages above the 5th harmonic frequency is required, the major challenges in designing the passive filter seems to be that low impedance must be provide at one frequency without having unwanted high impedance at another frequency and at the same time ensure that the VAr compensation of the capacitors is small enough to avoid leading power factor. Figure 6-41 shows an example of the impedance as seen by the harmonic current source for a four stage passive filter.

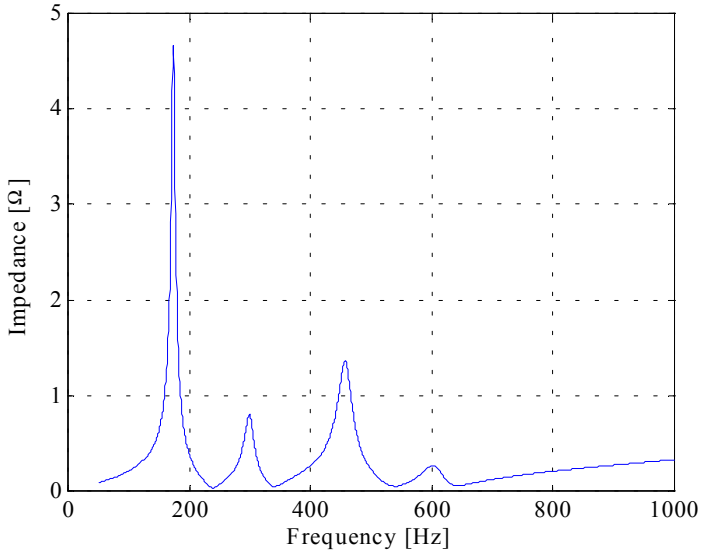


Figure 6-41: Impedance Z_h versus frequency for a four stage passive filter.

It should be noted that the source impedance has a significant influence on the harmonic filtering characteristic of the filter. Basically the harmonic current is split between the filter and the source depending on the impedance ratio between the filter and the source at the specific frequency. Besides the source impedance, also the resistance of the components used of the filter has significant influence on the amount of the harmonic currents absorbed. Therefore a passive filter needs case-by-case considerations and design.

6.3.2 Conclusion

Based on the review presented above it can be concluded that the harmonic filtering of the passive filter is system depending and it is therefore difficult in general to predict the harmonic filtering effect.

The disadvantage of passive shunt filters is that each installation (source impedance) is different and the size and placement of the filters varies accordingly. This means filters cannot be designed generally but must be designed to each application. Another disadvantage is the space required for the shunt passive filters and the high (reactive) fundamental current resulting in power losses. On the other hand the capacitors of the filters can be used as VAr compensation and thereby, if required, saving some extra costs.

Because of the complex nature of the passive filter design, passive filters are normally only used in large industrial plants (in the MVA range) or on the utility side to attenuate harmonic distortion.

6.4 Active Filter

One way to overcome the disadvantages of the passive shunt filter is to use an active filter. The active filter is an emerging technology and several manufacturers are offering active filter for harmonic current reduction in ASD applications. This section reviews some of the most important features. Also some basic control strategies are reviewed because these have significant influence on the harmonic currents.

The active filter is controlled to draw a compensating current i_{af} from the utility, so that it cancels current harmonics on the ac side of the diode rectifier as shown in Figure 6-42.

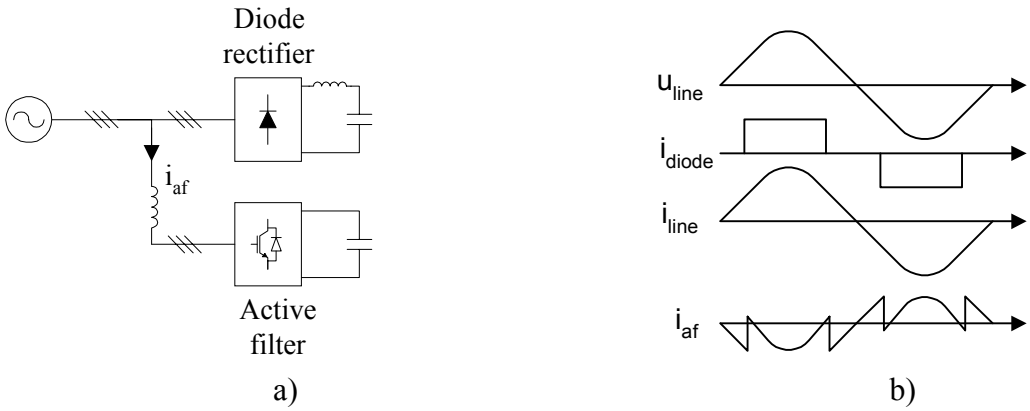


Figure 6-42: a) Shunt active filter. b) The theoretical current of an active filter for achieving a sinusoidal line current.

The most used topology is the shunt active filter with a circuit diagram as shown in Figure 6-43 consisting of six active switches, e.g. IGBT's. The circuit diagram of the active filter is basically the same circuit diagram as the active rectifier. Lately also active series filters and hybrid systems combining active and passive filters have been considered. These topologies are not covered here. But a review can be found in [Akagi 1996].

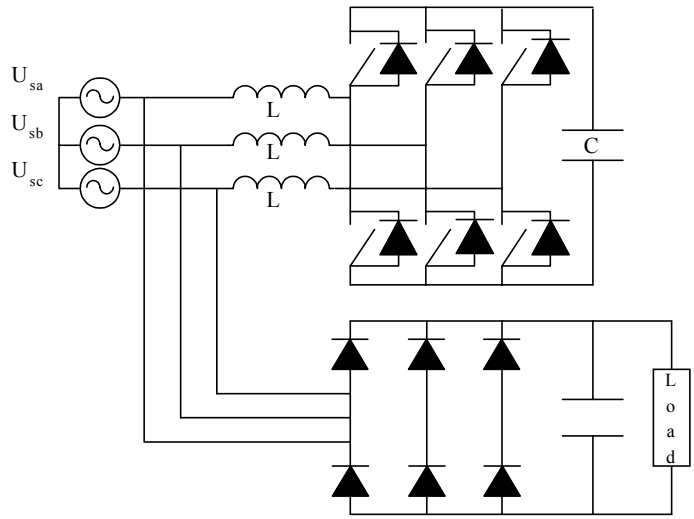


Figure 6-43: Circuit diagram of the active shunt filter and a three-phase diode rectifier load.

Obviously, the chosen control strategy for the active filter has a significant impact on the remaining system harmonic distortion level. Therefore, the basic principles of two different control strategies are reviewed in this section.

6.4.1 Control strategies

Several different control strategies exists depending on the application the active filter is intended to be used for.

One of the first control strategies that made active filters interesting in real applications and out of the laboratory stage was the p-q theory by [Akagi et al. 1984]. The basic principles of this control strategy are still widely used. Therefore this strategy is briefly explained in the following.

Transforming the three-phase voltages, U_{sa},U_{sb} and U_{sc} and the three-phase load currents i_{La}, i_{Lb} and i_{Lc} into the stationary α-β reference frame the instantaneous active power p_L and reactive power q_L of the load can be calculated as:

$$\begin{bmatrix} p_L \\ q_L \end{bmatrix} = \begin{bmatrix} u_\alpha & u_\beta \\ -u_\beta & u_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{6.1}$$

The instantaneous power p_L and q_L are normally divided into three components:

$$\begin{aligned} p_L &= p_{L,dc} + p_{L,lf} + p_{L,hf} \\ q_L &= q_{L,dc} + q_{L,lf} + q_{L,hf} \end{aligned} \tag{6.2}$$

where:

$p_{L,dc}$, $q_{L,dc}$: dc components
$p_{L,lf}$, $q_{L,lf}$: low-frequency components
$p_{L,hf}$, $q_{L,hf}$: high-frequency components

The fundamental active and reactive power is the dc-components, while the negative sequence current is a low frequency component (2 · fundamental frequency). The harmonics are to be found in the higher frequency components. The different components are extracted by the use of high-pass filters. The command currents $i_{ca,ref}$, i_{cb_ref} and $i_{cc,ref}$ can now be found by the following:

$$\begin{bmatrix} i_{ca,ref} \\ i_{cb,ref} \\ i_{cc,ref} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} u_\alpha & u_\beta \\ -u_\beta & u_\alpha \end{bmatrix}^{-1} \begin{bmatrix} p_{ref} \\ q_{ref} \end{bmatrix} \tag{6.3}$$

The active and reactive power references p_{ref} and q_{ref} are depending on what the filter must compensate for. If only harmonics are compensated, p_{ref} and q_{ref} are equal to the high frequency components of the instantaneous active power p_L and reactive power q_L.

The p-q theory control of an active filter is highly depending on the fast response of the current controller Normally this problem is overcome by the use of a high switching and sample frequency (20 kHz – 40 kHz) which results in high bandwidth of the current controller. However, this also leads to high switching losses.

If the harmonic currents are considered stationary (which is a fair assumption for an ASD application) it is possible to overcome this problem by the use of selective harmonic control strategies. Two different approaches, the FFT approach and the Transformation approach, are frequently used for selective harmonic control. The FFT approach [Abrahamsen, David 1995] basically determines the harmonics of the previous period by

Fourier series and injects the detected harmonics with an opposite phase-angle. In the Transformation approach [Jeong, Woo 1997] the harmonic currents are transformed into individual rotating reference frames where the individual harmonics become dc-quantities. The dc-signal errors are easy controlled to zero with linear controllers such as the PI-controller. In [Svensson, Ottersen 1999] these two control strategies are compared along with the p-q control strategy. Both strategies are found to be superior to the p-q control with respect to performance at low switching frequencies (6 kHz). In the following the Transformation approach is described more closely.

The harmonics of interest are the characteristic harmonics of a three-phase diode rectifier i.e. the 5^{th}, 7^{th}, 11^{th}, 13^{th} etc. The control strategy is here explained by the example of the 5^{th} harmonic current. The 5^{th} harmonic current is controlled to zero by transforming the line current from the fundamental rotating reference frame into the 5^{th} harmonic rotating reference frame. After lowpass filtering the transformed current is a dc value and can be controlled to zero by a simple PI controller. The output of the current controller is transformed back to the (fundamental) synchronously rotating reference frame. Figure 6-44 shows a block diagram of the control strategy.

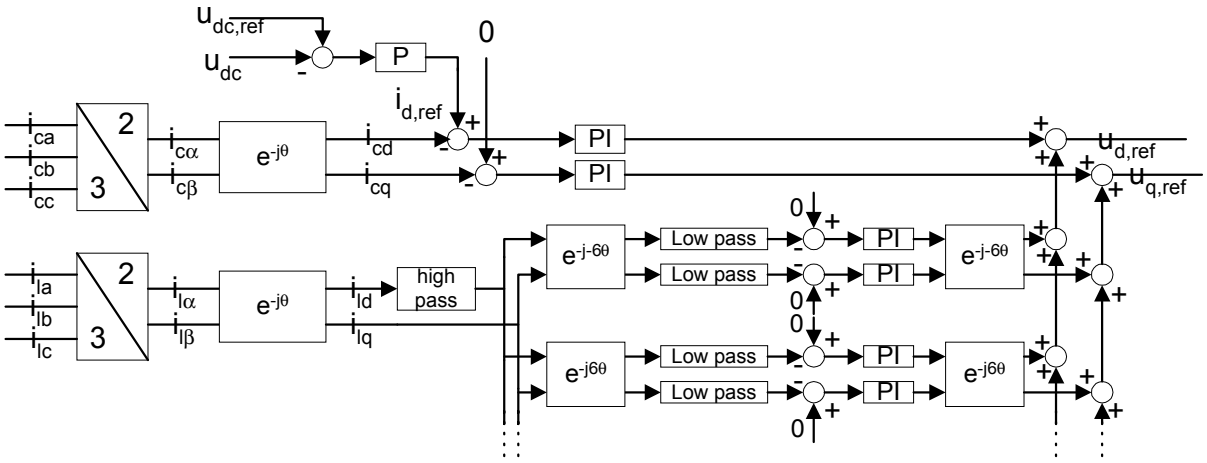


Figure 6-44: Overall control scheme for the shunt active filter.

Because the 5^{th} harmonic current is a negative sequence rotating current the current has to be transformed with an angle of $-6*\theta$ (compared to the synchronously rotating reference frame which is transformed with θ) while the 7^{th} harmonic current has to be transformed with $6*\theta$ because the 7^{th} harmonic current is a positive sequence rotating current.

6.4.2 Simulation results

The above mentioned control strategy is implemented in SABER. The harmonic control is implemented to the 25^{th} harmonic. The switching frequency is 5 kHz. Figure 6-46 shows the result of a SABER simulation with above described control strategy. The low pass filters cutoff frequency is 20 Hz and the integration time of the PI controller in the harmonic reference frame is set to 1 s.

Figure 6-45 shows the current of the three-phase diode rectifier with a 3% dc-link inductance. The load is 100 kW and the short circuit ratio at the connection point is 100. The THD_i of the diode rectifier current is 56.3% and Hc= 412%.

Figure 6-46 shows the line current. As it can be seen the control works very well up to the 25^{th} harmonic current (1250 Hz) while the harmonic currents above not are influenced. The THD_i of the line current (up to the 40^{th} harmonic) is 8.8%.

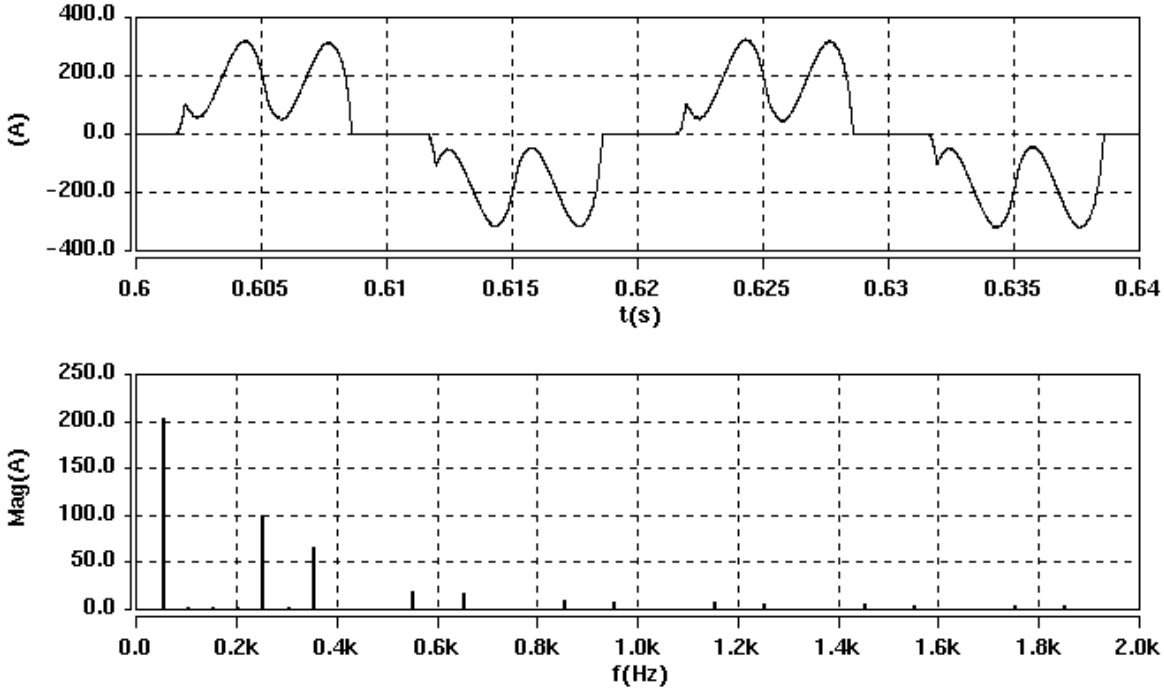


Figure 6-45: The current and Fourier spectrum of the diode rectifier. THD_i = 56,3% Hc = 412%.

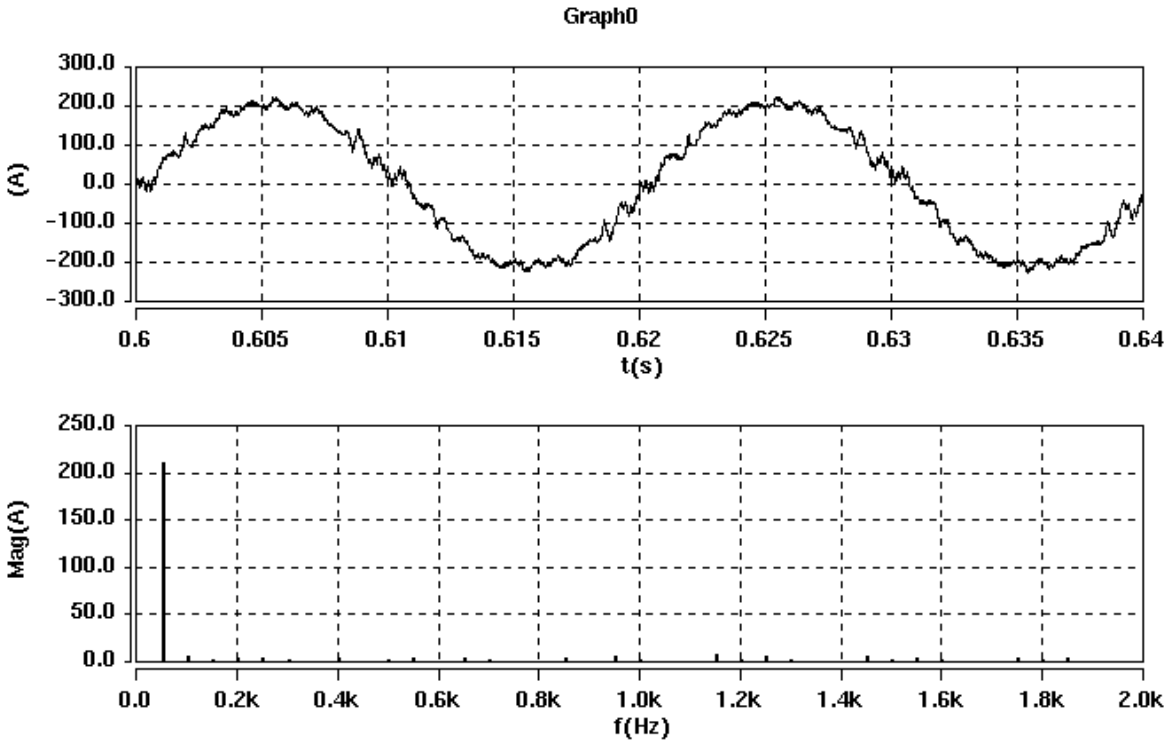


Figure 6-46: The current and fourier spectrum of the line current, THD_i = 8.8% Hc = 242%.

It should be noted, that the active filter is only rated for the harmonic currents of the load. Since the THD_i of the diode rectifier current is 56.3% the current rating of the active filter is only 56.3% of the fundamental current or 49% of the total rms current of the diode rectifier.

6.4.3 Conclusion

Based on the review presented above it can be concluded that the active filter have many advantages for ASD's:

- Current THD_i of below 10% is achievable
- Lower kVA rating than the load current, as long the THD_i of the load is less than 100%
- High reliability: The diode rectifier can continue even if the active filter breaks down

The main disadvantages are:

- Expensive circuit topology (six switching devices, e.g. IGBT's, are required)
- A complex control strategy and a DSP is therefore required
- Significant contribution to system losses
- EMC can become a significant problem and EMC filters are therefore necessary
- Measurements of both converter- and line-currents are necessary

In general a THD_i of 5% - 15% depending on the chosen control strategy is considered as a realistic harmonic performance of the active rectifier. It is difficult to predict the Hc value because the Hc value is depending in the higher harmonics and thereby on the control strategy, switching frequency and chosen filter type (LCL or L)

6.5 Conclusion

In this chapter four selected system level harmonic reduction techniques useful for three-phase rectifiers used in ASD's were presented.

It is shown that a significant amount of 5^{th} harmonic current cancellation can be expected when mixing single- and three-phase diode rectifiers. However, it is also shown that no easy prediction of the harmonic cancellation is possible and that this scheme requires case-by-case examination. Nevertheless, as shown by an example, the cancellation effect must be included when considering alternative rectifier topologies to the three-phase diode rectifier when single-phase diode rectifier loads are present in the same system. In the presented case choosing a 12-pulse rectifier instead of a 6-pulse diode rectifier showed actually a worse harmonic performance because the 12-pulse rectifier is unable to cancel existing 5^{th} harmonic currents.

The same was shown to be true for the 5^{th} harmonic voltage distortion. Because the harmonic background distortion mainly is caused by a large number of single-phase non-linear loads it is clearly shown that three-phase rectifiers to some level actually can reduce the 5^{th} harmonic voltage and thereby the total harmonic voltage distortion. This is a very important point also, because even clean power converters can result in worse voltage distortion than a three-phase diode rectifier without any extra measures.

It is shown that with a THD_i of less than 20% in most of the operating area, the quasi 12-pulse topology is competitive to a true 12-pulse rectifier. It is stated that a reduction of the voltage distortion by a factor of two can be expected compared to a 6-pulse diode rectifier with dc- or ac-coils. Also the quasi 12-pulse topology shows possibilities to compensate for effects caused by pre-distorted grid. This is not possible for a true 12-pulse rectifier

For large new plants quasi multi-pulse performance on the MV-line should be considered. However, as shown the performance is very depending on the amount of background distortion. If there is some amount of background distortion on the MV-line, and assuming that this distortion comes from single-phase diode rectifiers, the best result is obtained by just connecting the converters to the distribution transformer.

Capacitor banks for displacement power factor correction can be used for passive filtering in applications where displacement power factor correction. Significant harmonic reduction can be achieved. However, these filters need careful system design and are therefore only useful in large plants.

A lot of the problems arising with the use of passive filters, such as large reactive power generation resonance conditions can be avoided when using an active filter instead of passive filters. The active filter has many advantages, such as low (system) current THD_i (less than 10% is achievable), lower kVA rating than the load current and high reliability (the apparatus connected can continue even if the active filter breaks down).

Table 6-2 shows the performance indexes such as THD_i, Hc and THD_v. The voltage THD_v is based on the assumption that several ASD's with a total fundamental input power of 300 kW is connected to a 1 MVA transformer with a short circuit impedance of 5%.

	THD_i [%]	Hc [%]	rms curren [%]	THD_v [%]	Comments
Mixing single-phase and three-phase	System depending	System depending	System depending	System depending	
Quasi 12-pulse	15–25	100 – 200	101 – 103	2.25	Hc = 150% assumed for THD_v calculation
Passive Filter	System depending	System depending	System depending	System depending	
Active Filter	5-15	Design depending	100 - 101	Design depending	LCL filters are necessary. Hc and THD_i are depending on the filter design and control strategy

Table 6-2: Performance index of the high power factor rectifier topologies compared to the basic diode rectifier.

7. Requirement Based Cost-Optimal Rectifier Topology

In Chapter 5 and Chapter 6 several harmonic reduction techniques for ASD's have been discussed. By simulations and partly by experimental results an estimate of the harmonic performance of these schemes has shown possible. Also, there is found a big difference in complexity and performance of the presented schemes.

To find a cost-optimal solution, it is necessary to find the estimated cost of the different topologies. In this chapter a cost - benefit analysis is presented based on available market information and the harmonic performance estimates of the previous chapters.

The requirements set to the rectifier equipment can differ widely depending on the application and location, e.g. different standards may be applicable. In this chapter it is therefore found that it is impossible to determine one specific harmonic reduction technique for ASD's that is *the* cost-optimal solution in all applications. Instead, a general step-by-step approach to find the cost-optimal rectifier topology that fulfills individual requirements is proposed.

Finally, an easy-to-use calculation tool is developed for doing the required calculations. The step-by-step approach to find the cost-optimal rectifier topology and the calculation tool are used in a real application example to illustrate their applicability.

7.1 Cost - Benefit Analysis

Besides the cost for the ASD's including one of the presented rectifier topologies other costs become quite significant in an overall cost analysis. The most important cost drivers are:

- Protection, cables, transformer etc. (rms current)
- Lifetime of equipment and components
- Installation (number of extra components e.g. filters)
- Pre-engineering

These cost drivers are briefly discussed in the following.

The harmonic currents contributes to the rms current as shown in equation 7.1:

$$I_{rms} = I_1 \cdot \sqrt{1 + THD_i^2} \tag{7.1}$$

Assuming a basic three-phase diode rectifier with a THD_i = 80% the rms current is 1.28 times higher than the active current I_1. As a comparison, a three-phase diode rectifier with dc-coils and a THD_i = 40% increases the rms current by 1.08 times the active I_1. Here is a significant cost factor. Reducing the rms current compared to the basic rectifier results in that smaller cable cross-section and protection gear may be used, which can contribute to some cost savings. Also the supply transformer can be utilized better.

Furthermore, using dc-coils (or ac-coils) guarantees continuous current into the dc-link, which increases the lifetime of the dc-link capacitors. This could be a second order cost factor.

Another important cost driver is the installation cost for extra components, such as additional ac-coils, passive or active filters. In general, it can be difficult to estimate the costs for the installation, because different installation practices and requirements may be used in different countries and applications, e.g. installations can be more expensive in an explosion safe application than in an office building.

Some of the presented harmonic reduction techniques, such as the quasi 12-pulse topology, passive filters and the harmonic cancellation when mixing single- and three-phase diode rectifiers, require some kind of pre-engineering. Again, the costs for that can differ widely. The experience of the engineer with respect to harmonics and the tools used will have a significant impact of the expected costs. Therefore, it is important to make easy-to-use tools available that can handle this kind of system level harmonic reduction techniques.

Because the mentioned cost-drivers can be difficult to determine, the presented estimated costs for the different harmonic reduction techniques are based on the rectifier and ASD costs only. Figure 7-1 shows the harmonic performance of the harmonic reduction techniques presented in the previous chapters versus the estimated costs of an ASD including the individual harmonic reduction techniques. The estimated costs are based on a USA market survey made by Danfoss Drives A/S (see also Appendix D.4).

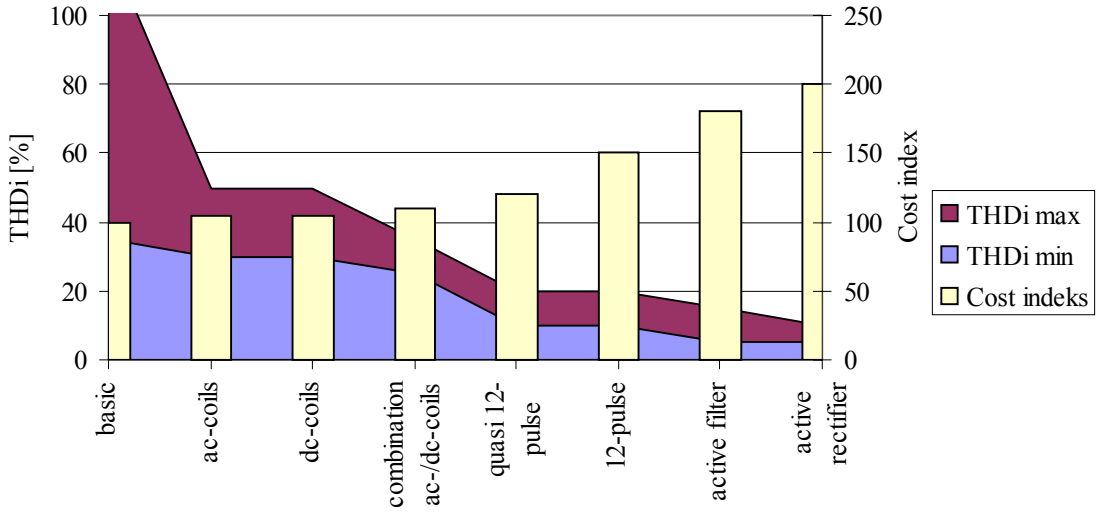


Figure 7-1 Cost – benefit of harmonic reduction techniques for three-phase ASD's.

As shown in Figure 7-1 an ASD with a basic three-phase diode rectifier has a cost index of 100. The expected total harmonic current distortion can vary between 35% to over 100% depending on the line impedance. However, ASD's are normally connected to a quite strong grid and a THD_i of more than 60% is realistic. Therefore, adding ac-coils or using ASD's with built-in dc-coils makes sense. The harmonic current distortion is significantly reduced, and the maximum current distortion on a strong grid will not exceed 50%. The cost index is slightly increased to 105. As mentioned, other advantages are reduced rms

current and the continuous dc-link current obtained increases the lifetime of the dc-link capacitors.

Harmonic performance wise both techniques are comparable. However, built-in dc-coils are a compact, space saving design with higher efficiency than rectifiers with ac-coils. Also, since built-in, no extra installation costs have to be taken into account as with ac-coils. On the other hand, the inductance of dc-coils cannot easily be changed to another value. If a larger inductance is needed, a combination of built-in dc-coil and ac-coils is possible. This reduces the harmonic current distortion even further to 25% – 35% and the cost index equals 110.

If several ASD's are used, and further harmonic current reduction is required, the quasi 12-pulse rectifier is an obvious choice. Harmonic current distortion of 10% - 20% is expected for the quasi 12-pulse rectifier topology with a cost index = 120. While the same harmonic current distortion factors are expected with a true 12-pulse rectifier topology the cost index for the true 12-pulse rectifier = 150. However, the quasi 12-pulse rectifier topology requires some pre-engineering that needs to be taken into account in a total cost analysis.

Active filters are an emerging technology for harmonic reduction on a system level. A harmonic system current distortion of 5% - 15% is expected, depending on the rating of the active filter and the used control strategy. The cost index of existing products equals approximately 180.

Looking at the cost of the rectifier only, the active rectifier is the most expensive topology. A cost factor of approximately 200 is found. The total harmonic current distortion is in the range of 5% - 10%. However, in some applications where power regeneration is required, the savings in energy and cost for dynamical braking resistor must be considered in a total cost analysis. This savings can be significant, and measured in total costs the active rectifier can become cheaper than e.g. the 12-pulse rectifier.

It should be mentioned that topologies, such as the passive filter and mixing single-phase and three-phase diode rectifier are not considered in the cost-benefit analyses because these topologies are highly system dependent both with respect to the harmonic performance and the expected cost. However, in applications where (displacement-) power-factor-correction capacitors are connected to the system the passive filter should be considered. Also were single-phase diode rectifiers are connected to the same line as the ASD, for a cost optimal harmonic reduction the cancellation effect when mixing these two rectifier types should not be neglected.

7.2 Stepwise Approach to Chose the Cost-Optimal Rectifier Topology

The ideal approach for finding the cost-optimal rectifier topology for each application would be a simple algorithm where only a few basic parameters are used as input, and the output would be the rectifier topology that is the cost-optimal rectifier topology. However, the number of significant parameters is too high that this would become practicable. Therefore, a general step-by-step approach to find the cost-optimal rectifier topology is described in this section.

The idea is to start with the cheapest rectifier topology, calculate the harmonic distortion level and compare it with the set requirements. If the requirements are not fulfilled, the calculations must be repeated with the next cheapest topology. Figure 7-2 shows a flowchart for finding a cost-optimal rectifier topology.

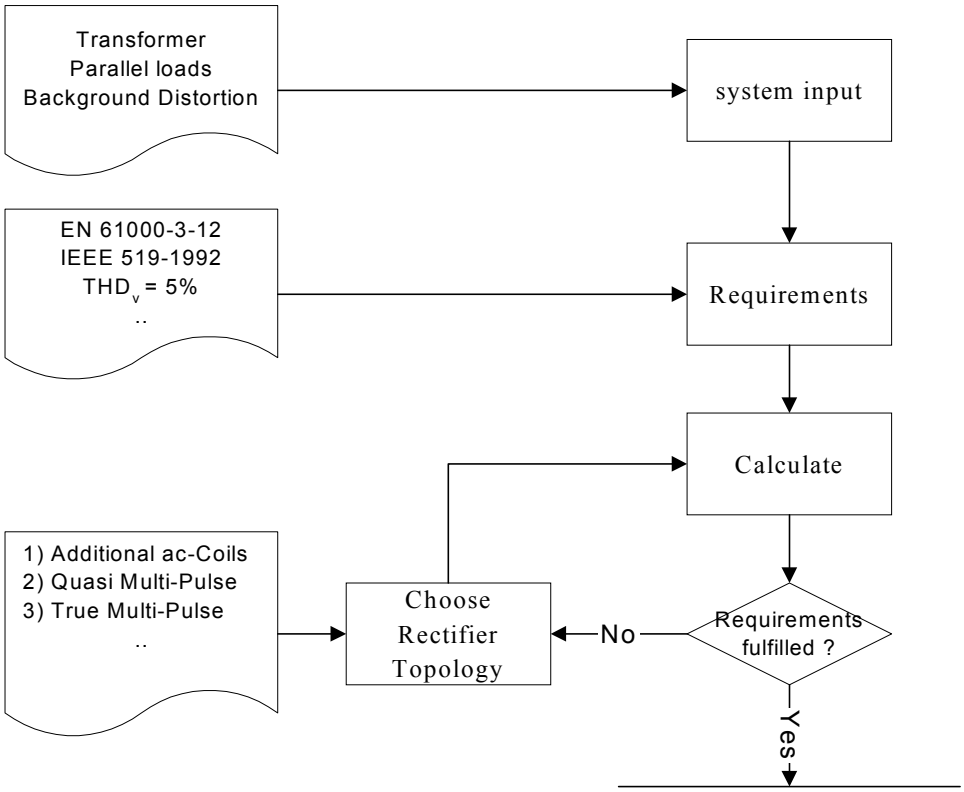


Figure 7-2: Flowchart for finding the cost-optimal rectifier topology for ASD applications.

From Figure 7-2 it is seen that one of the major tasks is to calculate the expected distortion level with the chosen rectifier topology. This is not an easy task, because in order to determine the cost-optimal rectifier topology, the calculations must as a minimum include:

- Harmonic current distortion of the individual rectifier topologies.
- Harmonic system current distortion also when paralleling different rectifier topologies, such as single-phase and three-phase diode rectifiers.
- Impedance values for the system voltage distortion including parallel loads such as capacitor banks and passive filters.
- Resulting voltage distortion calculations with background distortion.

Ideally, the calculations should also include the harmonic current distortion calculations of the individual rectifier topologies at non-sinusoidal supply voltages. However, as described in Chapter 4 and Chapter 5 this requires circuit based calculation tools.

As mentioned, easy-to-use tools to do these kinds of calculations are required to keep the pre-engineering costs low for topologies such as the quasi 12-pulse topology. Also the calculation tool must be easy available which excludes circuit based simulation tools.

In the following a calculation tool is described that fulfils most of the set requirements.

7.2.1 Calculation tool

The calculation tool presented is developed for the MATLAB simulation package and it is based on the analytical models of the three-phase and single-phase diode rectifiers presented in Chapter 4.3. MATLAB allows easy and fast development of the basic ideas for this calculation tool. Furthermore, for future use the MATLAB code can easily be converted to a C-code if required.

Ideally, the calculation tool should include the harmonic current distortion calculation of all the discussed rectifier topologies. However, the developed tool is (so far) only able to handle the three-phase diode rectifier with additional ac- or dc-inductance, quasi 12-pulse topology and mixing single- and three-phase diode rectifiers as shown in Figure 7-3.

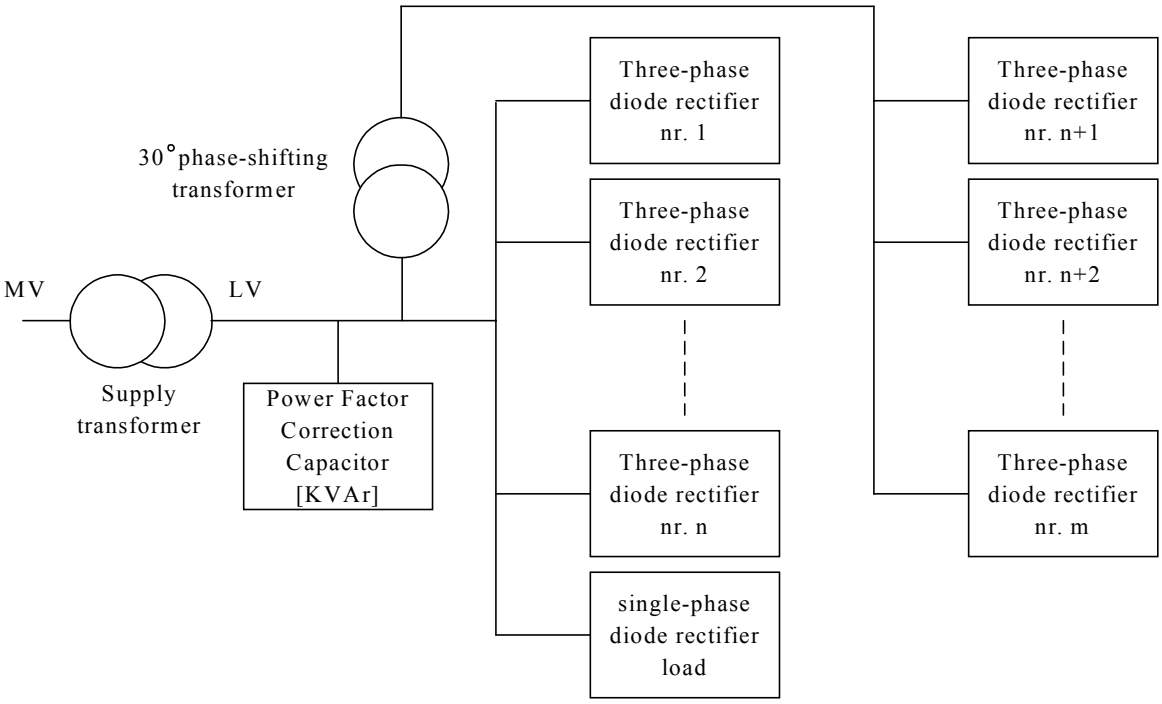


Figure 7-3: Diagram of the simulated system.

The required input data to the program are:

- Transformer data
- Number of ASD's
- Number of ASD's connected to a phase shifting transformer (quasi 12-pulse)
- dc-link inductance, dc-link-capacitance and ac-coils for each individual ASD
- Amount of single-phase load connected to the same supply transformer
- Power factor correction capacitors connected to the same line
- Background 5^{th} harmonic voltage distortion incl. the phase-angle

Based on the line impedance and the values for the dc-link components the line-currents of the individual three-phase rectifiers are calculated. These current are summed together with the currents calculated for the phase-shifted three-phase rectifiers and the single-phase diode rectifier currents. Based on the system current the voltage distortion is calculated. The impedance for the voltage distortion calculation is considering power factor correction

capacitors connected to the system. Also the resulting voltage is calculated as a geometrical sum of the background distortion and the generated voltage distortion.

The applicability and screen dumps of the calculation tool are shown in the next section.

7.3 Application Example

In this section a real application is described, and a cost–optimal rectifier topology is achieved, based on the above described calculation tool and the cost-benefit analysis.

A wastewater treatment plant with a total of 34 ASD's is described in the following. The ASD's are divided into four Motor Control Centres (MCC's) with four equally sized supply transformers as shown in Figure 7-4.

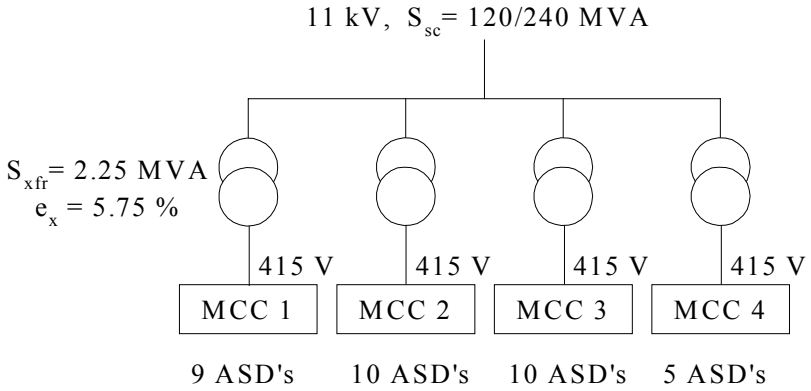


Figure 7-4: Diagram of the wastewater treatment plant.

In the technical specification of the tender it is stated that:

"The harmonic voltage limitation defined in AS/NZS 2279.2 and NZECP36 shall be met for normal operating conditions at the 415 V supply switch board. To achieve compliance with these conditions, full considerations shall be taken of power supply impedance, existing harmonic levels and other loads connected to the power system"

In agreements with AS/NZS 2279.2 and NZECP36 this means that the voltage distortion THD_v shall be less than 5%.

For the calculation part following information is available:

- Maximum HV Fault Level at Transformer HV Terminals: 240 MVA
- Minimum HV Fault Level at Transformer HV Terminals: 120 MVA
- Background Levels of Harmonic Distortion at 11kV: 1.5% THD_v
- Approximate operating capacity of ASD's as a % of ASD rating: 80%
- Supply transformer configuration: 2250 kVA / 11 kV 415 V / Dyn11
- Supply transformer impedance: 5.75%
- Cable between transformer and MCC: 5 meters, 3150A VASS
- Average distance between MCC and ASD: 8 meters

To keep it simple only the transformer with the largest load is considered in this section. Also the background distortion is neglected since the phase-angle is not known. These data are used in the system data input window of the calculation program as shown in Figure 7-5.

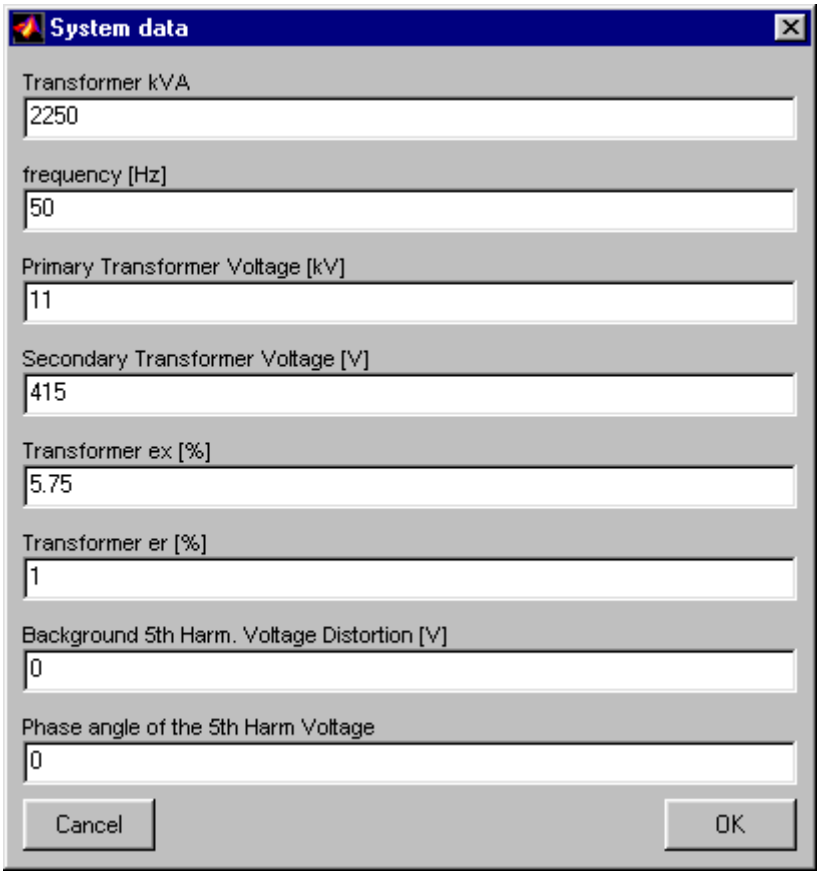


Figure 7-5: System data input window for the used calculation tool.

Transformer 1 has a total motor load of 754 kW (shaft power) consisting of 9 motors as listed in Table 7-1. To find the input power of the ASD's, the efficiency of the motor and the inverter needs to be taken into account. The efficiency of the inverter is assumed to be 0.96. Taking into account the efficiency of the inverter and the motors the total ASD load is 823 kW.

	Motor Shaft Power [kW]	Assumed Motor Efficiency
Motor 1	260	0.96
Motor 2	230	0.96
Motor 3	150	0.95
Motor 4	75	0.94
Motor 5	22	0.92
Motor 6	15	0.91
Motor 7	0.75	0.73
Motor 8	0.55	0.69
Motor 9	0.55	0.69

Table 7-1: Motor-load and motor-efficiency connected to transformer 1 in the wastewater treatment plant.

All ASD's are connected directly to the grid and no phase-shifting transformer is used as shown in Figure 7-6.

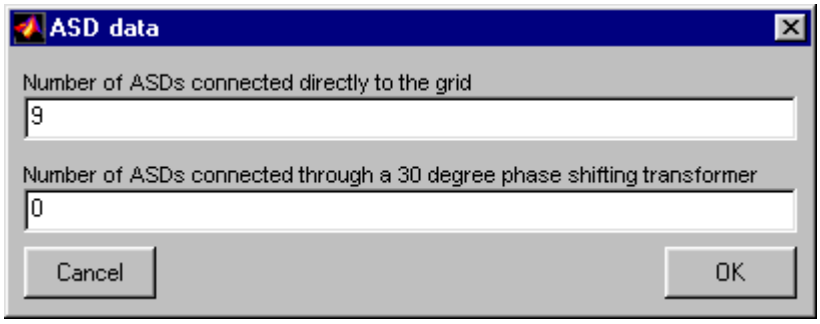


Figure 7-6: Input window for the number of drives connected directly to the grid and for connected through a 30° phase shifting transformer.

According to step-by-step approach to find the cost-optimal rectifier topology, calculation of ASD's connected to a phase-shifting transformer is only used when the requirements set can not be achieved with the cheaper topology. In this case the calculations are first made with built-in dc-link inductance. The ASD's used are Danfoss VLT® 5000 series. These drives do have a built-in dc-link inductance. The dc-link inductance and dc-link capacitor values are known and they are used in the ASD data input window of the calculation tool as shown in Figure 7-7 for ASD nr 1.

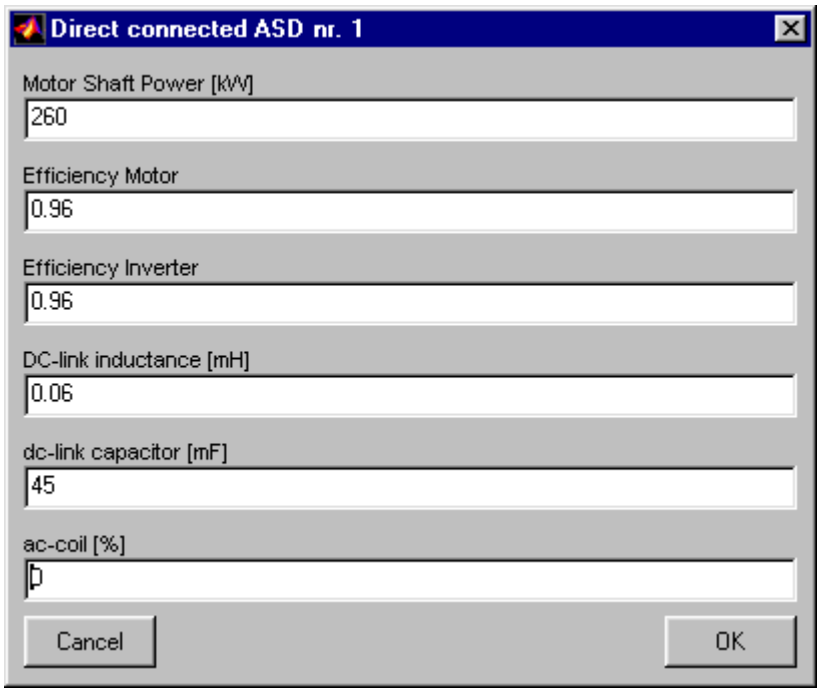


Figure 7-7: ASD data input window for the used calculation tool.

No additional single-phase loads are known, therefore the parallel-connected single-phase diode rectifier load is set to zero as shown in Figure 7-8.

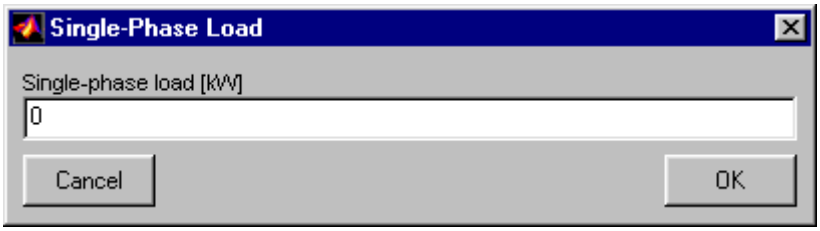


Figure 7-8: Parallel connected single-phase load input window.

Also no power factor correction capacitors are connected to the secondary side of the transformer as shown in Figure 7-9. This means that the line impedance is assumed mainly inductive and therefore is increasing linearly with the frequency as shown in Chapter 3.

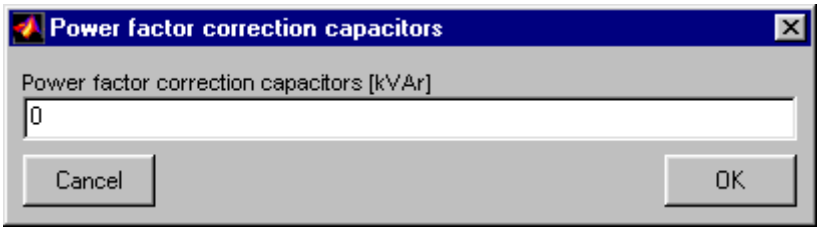


Figure 7-9: Parallel connected power factor correction capacitors input window.

Figure 7-10 shows the calculated system current and Fourier spectrum of the current for transformer 1. Figure 7-11 shows the Fourier spectrum of the voltage at the secondary side of Transformer 1.

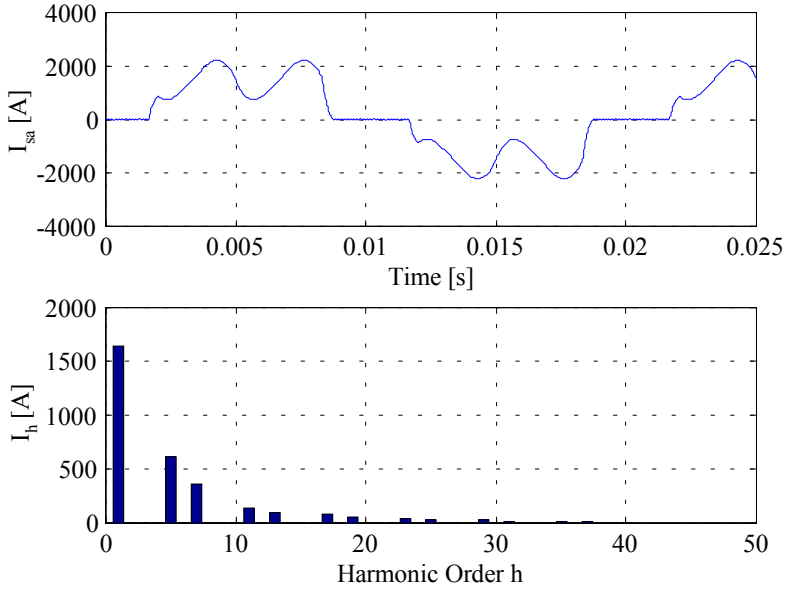


Figure 7-10: Calculated current and Fourier spectrum of secondary side of transformer 1 in the wastewater treatment plant.

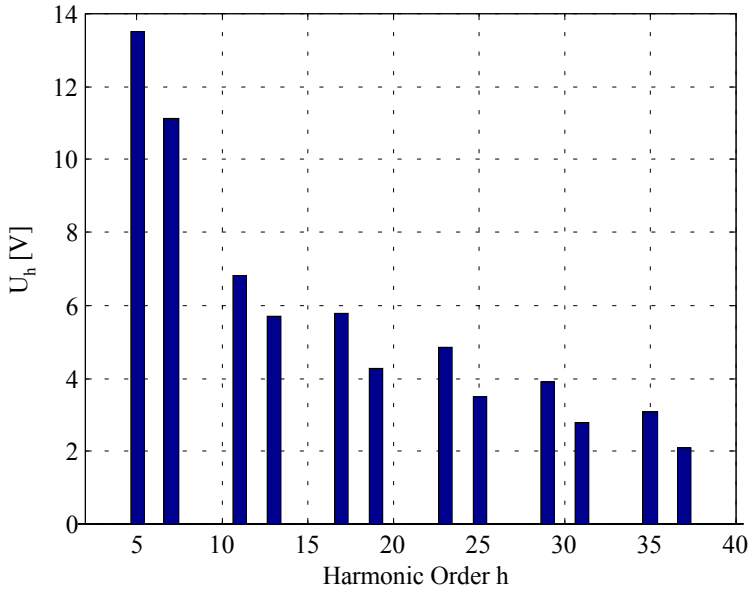


Figure 7-11: Calculated Fourier spectrum of the voltage at the secondary side of transformer 1 in the wastewater treatment plant.

The resulting total harmonic voltage distortion becomes THD_v = 6.7% and the total harmonic current distortion, THD_i = 45%. The THD_v is clearly too high with respect to the specification (≤ 5%). According to Figure 7-2 the next step is to redo the calculations with the next cheapest topology. In this case it is estimated that additional ac-coils are the next cheapest topology.

By choosing 3% ac-coils additional to the existing dc-link inductance for the four largest ASD's, i.e. for the 260 kW, 230 kW, 150 kW and 75 kW ASD, the resulting total harmonic voltage distortion becomes THD_v = 3.9% and the total harmonic current distortion, THD_i = 32%. These values are below the specified limits. Figure 7-12 shows the current and Fourier spectrum of the current for transformer 1. Figure 7-13 shows the Fourier spectrum of the voltage at the secondary side of Transformer 1 when additional 3% ac-coils are used.

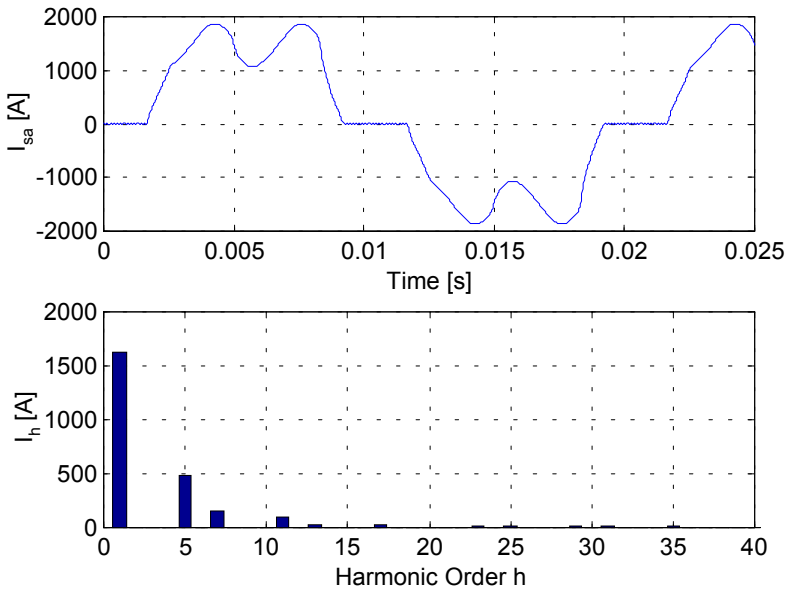


Figure 7-12: Calculated current and Fourier spectrum of secondary side transformer 1 in the wastewater treatment plant when additional 3% ac-coils are used.

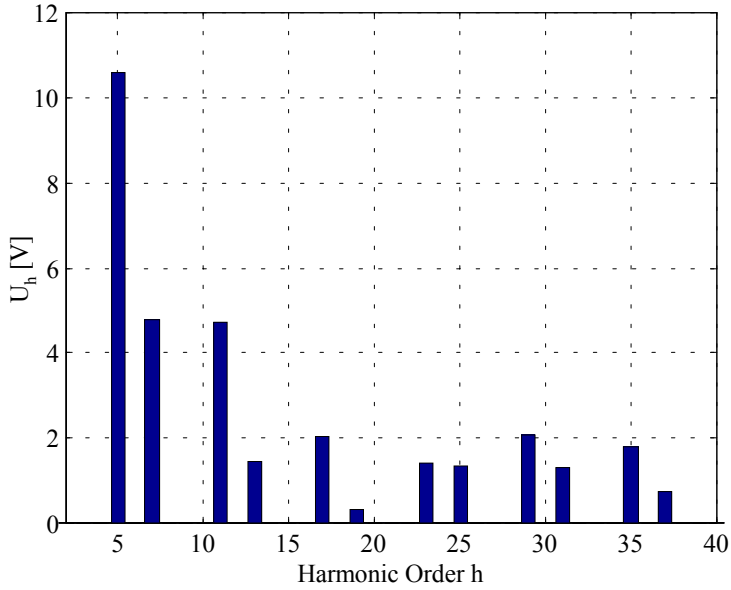


Figure 7-13: Calculated Fourier spectrum of the voltage at the secondary side of transformer 1 in the wastewater treatment plant when additional 3% ac-coils are used.

The simulations shown above are a good example of the effect of additional ac-coils. It can be seen that adding 3% ac-coils reduces mainly the 7^{th} harmonic current and higher frequency. As shown in Chapter 4, the ac-impedance has a significant impact on the commutation of the three-phase diode rectifier. Increasing the ac-impedance increases the commutation time and decreases therefore especially higher harmonics. Since mainly linear inductive line impedance is assumed (the impedance increases with the harmonic order), the higher harmonics have a significant impact on the total harmonic voltage distortion.

7.4 Conclusion

In this chapter a cost - benefit analysis is presented based on available market information and it is shown that the price for the available topologies is increasing for a decreasing harmonic current distortion. Also other cost-driver such as installation costs, pre-engineering and increased rms current are discussed and it is concluded that these cost drivers can differ widely depending on the application. However, these cost drivers can be significant and must therefore be included in a total cost analysis.

A general step-by-step approach to find the cost-optimal rectifier topology that fulfills individual requirements is proposed. An easy to use calculation tool is developed for doing the required calculations.

The applicability of the stepwise method to find the cost-optimal rectifier is demonstrated by a real application example. It can be concluded that by a few calculations a cost optimal rectifier topology is found for the application example. The required voltage distortion limit of 5% is not exceeded, by adding ac-coils to the existing dc-link inductance to the four largest ASD's.

8. Conclusion

The main intention of this thesis is to provide models and tools that allow easy prediction of the harmonic distortion of ASD's in a given system and to find reasonable (economical) solutions if the harmonic distortion is exceeding acceptable levels.

In the introduction it is pointed out that the main cause for harmonic distortion in the power system today is the diode rectifier. However, calculation of the harmonic distortion of the diode rectifier is not always easy. Therefore, one of the objectives identified in the introduction is to develop calculation models and methods to predict the harmonic distortion of the diode rectifier in a given application.

The effects of harmonic distortion, such as damaging or mal-functioning of various equipments, are widely known. But the level of harmonic distortion where these effects occur is not clearly defined. Therefore, finding an acceptable level for harmonic distortion is another objective identified in the introduction.

Several harmonic reduction techniques exist and in the introduction it is shown that there are widely accepted alternatives for the single-phase diode rectifier. However, it is more difficult to find alternatives for the three-phase diode rectifier. Thus, another important objective for this thesis is to analyze different possible rectifier topologies, especially for ASD's because these are believed to be a main contributor to the harmonic distortion in the near future. The final objective stated in the introduction is to point out the cost-optimal topology in a given application.

Based on the results presented in this thesis, as summarized below, it is believed that these four objectives stated are fulfilled.

8.1 Summary of the Thesis

In an attempt to find an acceptable level for the harmonic distortion, the international standards IEC 61000-2-2 and IEC 61000-2-4, defining the compatibility level for low frequency disturbances in the public and industrial power supply systems, are reviewed in chapter 2. Furthermore, the harmonic limiting standards EN 61000-3-2, EN 61000-3-12 and IEEE 519-1992 are summarized. It is found that even though harmonic current limits are stated, the objective of these standards is to limit the resulting harmonic voltage distortion. Thus, the voltage distortion is the most important factor. An acceptable level to the voltage distortion is found in the range of THD_v 5% - 8% and an individual harmonic voltage distortion of 3% - 6%.

In Chapter 3 and Chapter 4 models and calculation methods for predicting the harmonic distortion in a given application are discussed. Simple voltage distortion calculation methods are shown in Chapter 3. It is found that the total harmonic voltage distortion is proportional to the harmonic constant, Hc, and the short circuit ratio. It is pointed out that exact calculation of the resulting harmonic voltage distortion takes the background distortion into account. An example shows that the background distortion must be added geometrical to the calculated voltage distortion in order to find the correct resulting voltage distortion. Finally, it is recognized that the impedance values, which must be known for

calculation of the harmonic voltage distortion, can be difficult to find. Especially, if power factor correction capacitors are connected to the system or if backup generators are used. On the other hand, it is shown that simple, linear impedance models can be sufficient in most cases. This is verified by some experimental results.

Four levels of models for calculation of the harmonic current generated by both the single-phase and three-phase diode rectifier are presented in Chapter 4. The first level is an ideal model where the diode rectifier basically is treated as an independent (harmonic) current source. The second level is an empirical model, where simulated (or measured) values of the harmonic currents of the diode rectifier for different parameters are stored in tables. The actual harmonic currents are then found by interpolation between the stored data. The main advantage of this method is a simplicity that allows harmonic calculations in an spreadsheet. On the other hand, a large amount of data needs to be generated by more detailed simulations or measurements. The third level is found by analytical calculations. This gives some flexibility compared to the empirical model and very precise calculations are shown possible. The main disadvantage is that there exist no analytical models for non-ideal conditions, such as pre-distorted supply voltage. The fourth level is the use of circuit-based simulators, which guarantees high precision even under non-ideal conditions. However, for full utilization of a circuit-based simulator exact knowledge of all parameters is necessary.

By use of the numerical circuit based simulator SABER the phase-angle of the individual harmonic currents of different diode rectifier types is analyzed in Chapter 4. It is found that the 5^{th} harmonic current of the individual diode rectifier types is limited to a narrow band and that the 5^{th} harmonic current of the single-phase diode rectifier normally is in counter-phase with the 5^{th} harmonic current of the three-phase diode rectifier. These are very important points, because almost arithmetical summation of the 5^{th} harmonic current of the same rectifier type and harmonic cancellation of the 5^{th} harmonic current when mixing the single- and three-phase diode rectifiers is expected.

Finally, in Chapter 4 some basic characteristics of the diode rectifier are discussed and it is shown that the harmonic current of the diode rectifier is depending on several parameters, which practically makes a simple, exact prediction of the harmonic currents generated by the diode rectifier impossible.

In Chapter 5 selected rectifier topologies with a high input power factor are presented. The topologies discussed are the three-phase diode rectifier with ac- and dc-coils, the active rectifier, 12-pulse rectifier and an integrated single-switch approach.

It is shown that using ac- or dc-coils is a very simple and efficient method to reduce the current harmonics compared to the basic diode rectifier. Furthermore, the dc-link inductance exhibits some advantages compared to the ac-coils, such as lower losses and compact design. It is shown that adding a 3% - 6% dc-link inductance to the basic diode rectifier the diode rectifier can comply with the current limits of EN61000-3-12. However, it is also shown that a maximum short circuit ratio of 333 or an additional 0.3 ac-inductance is required to comply with the PWHD limit of the EN 61000-3-12.

The 12-pulse topology is an often used alternative to the 6-pulse diode rectifier, especially for ASD's. The main advantage is that the 12-pulse topology is a passive rectifier topology with a total harmonic current distortion of less than 20%. Also the 12-pulse rectifier is quite simple to design compared to other (active) topologies. However, the need for transformers makes the solution heavy and bulky. Furthermore, it is shown that the 12-pulse topology is sensitive to unbalanced and pre-distorted grid.

The active rectifier is probably the most elegant rectifier topology for ASD's due to a THD_i of less than 5%, bi-directional power flow, the possibility to reduce the dc-link capacitor size and a controllable dc-link voltage, which enhances the speed range of the ASD. However, this is not a low cost solution. The superior performance comes on the expense of a complex control strategy compared to other solutions, lower efficiency than the diode rectifier and extra switching losses in the inverter of the ASD. Also EMI becomes a significant issue and EMI filters are necessary to comply with European EMI standards.

The integrated single-switch third harmonic injection approach is essential an add-on solution to standard ASD's. The proposed scheme has shown that significant reduction of line-side harmonics is possible with the proposed approach. The advantages compared to other solutions, such as no extra components (extra losses) in series with the power flow and independence of the line impedance, makes this approach a potential solution for ASD's. The disadvantage of this scheme is that the injected current is circulating through the dc-link capacitor.

In Chapter 6 different system level harmonic reduction techniques are presented. It is shown that mixing single- and three-phase diode rectifier loads always reduce the total amount of 5^{th} and often the 7^{th} harmonic current. Furthermore, it can be concluded that adding a three-phase rectifier to an existing single-phase load will not increase the current THD_i at the transformer but actually lower the THD_i. Because the harmonic background distortion mainly is caused by a large number of single-phase non-linear loads it is clearly shown that three-phase rectifiers to some level actually can reduce the 5^{th} harmonic voltage and thereby the harmonic voltage distortion. It is also shown that when single-phase diode rectifiers are present a three-phase diode rectifier should be preferred to a 12-pulse rectifier, because the cancellation effect of the three-phase diode rectifier will lower the THD_i compared to the 12-pulse rectifier. These are important results. Careful system design taking these phenomena into account is a cost effective solution to lower the harmonic distortion.

With a THD_i of less than 20% in most of the operating area, the quasi 12-pulse topology is competitive or even superior to a true 12-pulse rectifier. It is stated that a reduction of the voltage distortion by a factor of two can be expected compared to a 6-pulse diode rectifier with dc- or ac-coils. For large new plants quasi multi-pulse performance on the MV-line should be considered. However, as shown the performance is very dependent on the amount of background distortion. If there is some amount of background distortion on the MV-line, and assuming that this distortion comes from single-phase diode rectifiers, the best result is obtained by just connecting the converters to a standard transformer.

Capacitor banks for displacement power factor correction can be used for passive filtering in applications where displacement power factor correction is needed. Significant harmonic

reduction can be achieved. However, these filters need careful system design and are therefore only useful in large plants. A lot of the problems arising with the use of passive filters, such as large reactive power generation and resonance conditions can be avoided when using an active filter instead of passive filters. The active filter has many advantages, such as low (system) current THD_i (less than 10% is achievable), lower kVA rating than the load current and high reliability (the apparatus connected can continue even if the active filter breaks down).

In Chapter 7 a cost - benefit analysis is presented based on available market information and it is shown that the price for the available topologies is increasing for a decreasing harmonic current distortion. Also other cost-driver such as installation costs, pre-engineering and increased rms current are discussed and it is concluded that these cost drivers can differ widely depending on the application. However, these cost drivers can be significant and must therefore be included in a total cost analysis.

A general step-by-step approach to find the cost-optimal rectifier topology that fulfills individual requirements is proposed. The applicability of the stepwise method to find the cost-optimal rectifier is demonstrated by a real application example. An easy-to-use calculation tool is developed for doing the required calculations. It can be concluded that by a few calculations a cost optimal rectifier topology is found for the application example.

8.2 Conclusions and Contributions

The most important conclusion drawn and the new results obtained in this thesis are summarized below.

By reviewing different standards and recommendations it is found that existing current limits are based on the objective to keep the voltage distortion below a certain level. Thus the voltage distortion is the key issue and a total harmonic voltage distortion level of 5% – 8% and an individual harmonic voltage distortion of 3% - 6% is found to be an acceptable level. Because the voltage distortion is found to be the key issue in limiting the harmonic distortion the following can be concluded.

- Since the voltage distortion of non-linear load is highly system (impedance) depending, the amount of acceptable harmonic current emission is system depending too. Thus unambiguous defined harmonic current limits valid for all kind of systems is impossible to state.

The systematic analysis of the individual harmonic current phase-angles of different type of diode rectifiers is considered to be unique (See also Appendix D.1). This analysis has led to some very important findings.

- The 5^{th} harmonic current of the individual diode rectifier types is limited to a narrow band and the 5^{th} harmonic current of three- and single-phase diode rectifiers are normally in counterphase.
- The phase angle of higher order harmonics differs widely as a function of the line-impedance even if the same type of diode rectifier generates these.

Based on these findings the following can be concluded.

- The 5th harmonic distortion is the most significant harmonic distortion on the power system. The reason for this is the dominating amount of single-phase diode rectifier connected to the power system (compared to other non-linear loads). Because the phase-angle of the 5th harmonic current is limited to a narrow band almost arithmetical summation can be seen, while the higher order harmonics are cancelled due to their almost random phase-angle.
- Consequently, as long as the single-phase diode rectifier is the dominating harmonic generator on the grid, connecting a three-phase diode rectifier will reduce the 5th harmonic current and voltage distortion in the power system. However, this might not be true locally on the LV-grid where three-phase diode rectifiers can be dominating, e.g. close to a water pumping station, areas with heavy industry etc. Furthermore, this might not be true in North America, where the power system differs from the European.

Several harmonic reduction techniques both on apparatus and system level are analyzed in this thesis. Four high power factor rectifiers are discussed in this thesis. The following contributions are made with respect to high power factor three-phase rectifiers.

- It is shown possible that the three-phase diode rectifier with built-in dc-coils can comply with the future EN 61000-3-12 (issue 2000-08-04).
- A novel line-voltage estimator for voltage oriented control of the active rectifier is presented. (See also Appendix D.3)
- The integrated single-switch third harmonic injection scheme is considered to be a new topology. (See also Appendix D.2)

On a system level four harmonic reduction techniques are presented and the following contributions to system level harmonic reduction techniques are made.

- Even though the quasi 12-pulse rectifier topology is well known, the analysis presented in this thesis and showing almost true 12-pulse rectifier performance is considered unique.
- Also the analysis showing harmonic cancellation by mixing single-and three-phase diode rectifiers is considered unique.

Based on the analysis made on the different harmonic reduction techniques some important conclusions can be drawn.

- Where a three-phase diode rectifier is used some amount (e.g. 3%) of ac- or dc-coils should be used, due to advantages such as increased lifetime of the dc-link capacitor and significantly reduced harmonic current emission compared to the basic diode rectifier.
- Active topologies such as the active filter and active rectifier are emerging technologies. However, even though superior to any of the other proposed topologies with respect to low frequency harmonic current emission, the active rectifier and active filter are not expected to be dominating compared to the other topologies (especially the diode rectifier) in the future. The reason is mainly two factors. 1) The relatively high costs and 2) taking the acceptable voltage distortion limits into account, sinusoidal current is not really required in most applications.
- If several three-phase diode rectifiers are used in an application the quasi 12-pulse topology is comparable or even superior to the true 12-pulse rectifier. Especially

when some background distortion is present and the voltage distortion is the main concern.

- Finally, if the voltage distortion is the main concern, the background distortion needs special attentions, because (as shown in this thesis) the simple three-phase diode rectifier might be the (cost- and performance-wise) optimal solution.

Furthermore it is found that it is impossible to point out *the* cost-optimal rectifier topology for all applications and that fulfills all requirements. However a step-by-step approach is proposed to find the cost-optimal topology in a given application. It is shown that it is possible to find a cost optimal rectifier topology by few calculations in a given application.

8.3 Future Work

Several aspects of harmonic distortion have been considered in this thesis. However, there are still many aspects that need more attention in the future. Some of these aspects are listed below.

- The harmonic impedance has shown to be of great importance, thus general (but simple) harmonic impedances model of the LV-distribution line needs to be developed.
- For the active solutions, such as the active rectifier and active filter more focus should be on the current control with LCL filters where most papers today only consider L-filters. Also the issue of EMI needs in general more attention.
- A more sophisticated current control for the integrated single-switch third harmonic injection scheme could result in even lower harmonic current emission than presented in this thesis. Future work on this topology should therefore consider this possibility.
- A general easy-to-use harmonic calculation tool, that would be able to calculate the harmonic distortion for several of the discussed rectifier topologies, could be developed. So far only the single/three-phase diode rectifier and the quasi 12-pulse scheme are included. The effects of pre-distorted grid and background distortion should be taken into account.
- More application examples to improve the step-by-step method (and the calculation tool) needs to be analyzed (including on-site measurements to verify the calculations).

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A. Measurements at Kyndby

This appendix describes some measurements made at DEFU's 10 kV laboratory in Kyndby and NESA A/S's low voltage (LV) grid (07.09.'98 - 10.09.'98). The primary goal with this series of measurements is to verify the harmonic cancellation effect by mixing single- and three-phase diode rectifies and to verify the models of the LV cables and the MV/LV transformer. The secondary goal is to determine the influence of switched currents and voltages on the MV-side. Therefore an active rectifier will be connected to the LV grid where measurements are made on the primary and secondary side of the transformer.

All low voltage measurements are made with a Dranetz power analyser. The Dranetz power analyser has only 128 points per (fundamental) period. This is a quite poor resolution, therefore some selected measurements are verified with a Tektronic oscilloscope (1024 points per period).

The MV-line measurements are sampled with a sample frequency of 19.841 kHz, where the current signals are measured with a Rugowski coils.

Three measurements series are made:

1. In measurement series 1 the voltage and current distortion on the LV side is measured as a function of the short circuit power. This is measured for a three-phase rectifier with dc-link inductance, a single-phase rectifier without dc-link inductance and for mixing these apparatus.
2. In measurement series 2 a simple measurement is made for a three-phase rectifier without dc-link inductance. The short circuit power is fixed.
3. In measurement series 3 both the voltages and currents of the low and medium voltage side are measured. In this series the measurement of the active rectifier are included.

A.1 Measurement series 1

A three-phase and a single-phase diode rectifier are connected to the grid and the harmonic currents and voltages are measured as a function of the short circuit power. The short circuit power is varied by using four different combinations of LV-cables. These LV-cables are part of the NESA A/S LV-grid laboratory within the area of DEFU's 10 kV laboratory in Kyndby. For every combination of the cables the load of the three-phase rectifier is varied in six steps (no-load - full load). For every load-step measurements are made with and without connection of the single-phase rectifier. The load of the single phase rectifier can not be varied. A total of 48 measurements are made in this measurement series. The used system is sketched in Figure A-1.

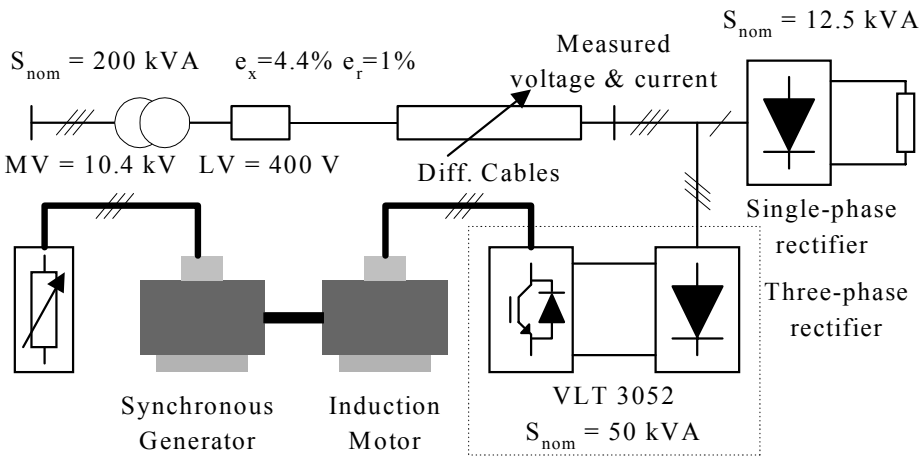

Figure A-1: A sketch of the system used for measurement series 1

There is used a 200 kVA transformer, a Danfoss frequency converter VLT 3052 (three-phase diode rectifier ca. 50 kVA) and a single-phase diode rectifier (ca 12.5 kVA).

The four combinations of cables are:

1) 10 meter four wire 50mm^2 Al.
2) 40 meter four wire 50mm^2 Al.
3) 240 meter four wire 50mm^2 Al.
4) 240 meter four wire 50mm^2 Al. + 200 meter four wire 25mm^2 Al.

The (50 Hz) impedance and short circuit power for these 4 combinations, including the impedance of the transformer $Z_t = 0.008 + j0.0352\ \Omega$, is:

1) $Z_1 = 0.01441 + j0.03592 = 0.0387\Omega\ \angle 68º$, $S_{sc} = 4.13$ MVA
2) $Z_2 = 0.03364 + j0.03808 = 0.0508\Omega\ \angle 49º$, $S_{sc} = 3.14$ MVA
3) $Z_3 = 0.16184 + j0.05248 = 0.1701\Omega\ \angle 18º$, $S_{sc} = 0.94$ MVA
4) $Z_4 = 0.40184 + j0.06748 = 0.4075\Omega\ \angle 10º$, $S_{sc} = 0.39$ MVA

The results of this measurement series are presented in the following way:

- In section A.1.1 the power and the THD values for the current (THD_i) and the voltage (THD_v) for phase 'a' are shown. Furthermore, the time of the measurements are listed.
- In section A.1.2 the percentage and absolute values for the 5th and 7th harmonic current and voltages are presented.

Because of the large amount of data the results shown in the tables can be confusing to the reader. Therefore special cases will be stressed out by figures. It should be noted that there is a large amount of data stored in the Dranetz measurements and only some results can be shown here. For example the 3rd harmonic is not covered here.

A.1.1 Total harmonic distortion

Cable	10m 50mm^2	40m 50mm^2	240m 50mm^2	240m 50mm^2 + 200m 25mm^2
No load	P = 0.06 kW THDv 1.00%	P = 0.18 kW THDv 0.93 %	P = 0.12 kW THDv 0.97	P = 0.04 kW THDv 0.96
1-phase rectifier only	P = 8.1 kW THDi 114 % THDv 3.48%	P = 8.2 kW THDi 109 % THDv 3.68%	P = 7.4 kW THDi 89 % THDv 6.38 %	P = 6.7 kW THDi 74 % THDv 8,95 %
3-phase rectifier only	P = 4.6 kW THDi 78 % THDv 2.28 %	P = 4.5 kW THDi 77 % THDv 2.21 %	P = 4.3 kW THDi 69 % THDv 2.66 %	P = 4.3 kW THDi 57 % THDv 3.20 %
3-phase & 1-phase	P = 13.4 kW THDi 63 % THDv 3.35 %	P = 13.1 kW THDi 60 % THDv 3.70 %	P = 11.2 kW THDi 51 % THDv 5.63 %	P = 9.7 kW THDi 40 % THDv 8.51 %
3-phase rectifier only	P = 7.4 kW THDi 58 % THDv 2.85 %	P = 7.4 kW THDi 56 % THDv 2.66 %	P = 7.6 kW THDi 47 % THDv 3.47 %	P = 7.7 kW THDi 40 % THDv 4.24 %
3-phase & 1-phase	P = 15.8 kW THDi 53 % THDv 3.98 %	P = 15.4 kW THDi 50 % THDv 4.39 %	P = 13.7 kW THDi 38 % THDv 5.93 %	P = 11.8 kW THDi 29 % THDv 8.31 %
3-phase rectifier only	P = 10.9 kW THDi 46 % THDv 3.16 %	P = 10.9 kW THDi 44 % THDv 3.24 %	P = 11.1 kW THDi 38 % THDv 3.97 %	P = 11.3 kW THDi 34 % THDv 5.47 %
3-phase & 1-phase	P = 19.0 kW THDi 43 % THDv 4.42 %	P = 18.2 kW THDi 42 % THDv 4.72 %	P = 16.7 kW THDi 30 % THDv 6.03 %	P = 15.1kW THDi 25 % THDv 8.99 %
3-phase rectifier only	P = 14.0 kW THDi 42 % THDv 3.83 %	P = 14.5 kW THDi 39 % THDv 3.80 %	P = 14.7 kW THDi 35 % THDv 4.93 %	P = 12.9 kW THDi 32 % THDv 6.16%
3-phase & 1-phase	P = 21.9 kW THDi 38 % THDv 4.84 %	P = 21.8 kW THDi 36 % THDv 5.23 %	P = 20.2 kW THDi 27 % THDv 6.95 %	P = 16.5 kW THDi 23 % THDv 9.29 %
3-phase rectifier only	P = 16.7 kW THDi 37 % THDv 4.20 %	P = 16.2 kW THDi 37 % THDv 4.15%	P = 16.7 kW THDi 34 % THDv 5.41 %	P = 15.3 kW THDi 29 % THDv 7.02%
3-phase & 1-phase	P = 24.2 kW THDi 36 % THDv 4.84 %	P = 23.9 kW THDi 34 % THDv 5.24 %	P = 21.8 kW THDi 26 % THDv 6.78 %	P = 18.8 kW THDi 22 % THDv 9.74 %

Table A-1: The power (in phase a) and the THD values for the current (THD_i) and voltage (THD_v) of phase a.

Table A-1 shows as expected the current THD_i for both the single-phase and three-phase rectifier is decreased with increased impedance while the voltage THD_v is increased. Furthermore, the current THD_i of the three-phase rectifier is decreased with increased load (Three-phase only).

However, the interesting and not predictable part takes place when mixing the single and three phase load (3-phase & 1-phase). The following figures will show the current and voltage THD_v as a function of the three-phase load when mixing single-phase and three-phase diode rectifiers where the load of the single-phase diode rectifier is fixed.
Figure A-1 shows the THD for the measurements with the 10m 50mm^2 cable.

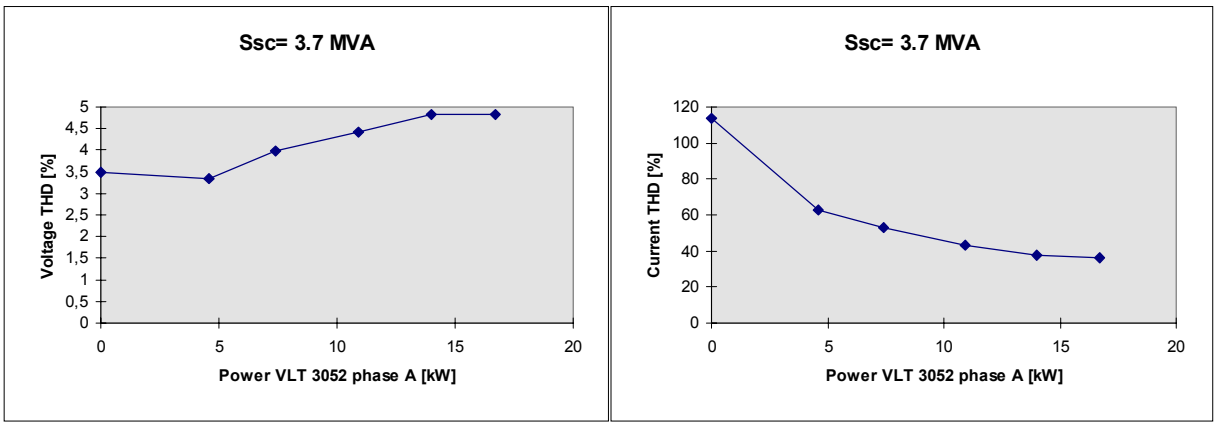

Figure A-1: The THD of the voltage and the current as a function of the per phase (phase a) power of the three-phase rectifier with constant power (8.1 kW) on the single-phase rectifier.

Figure A-2 shows the THD for the measurements with the 40m 50mm^2 cable.

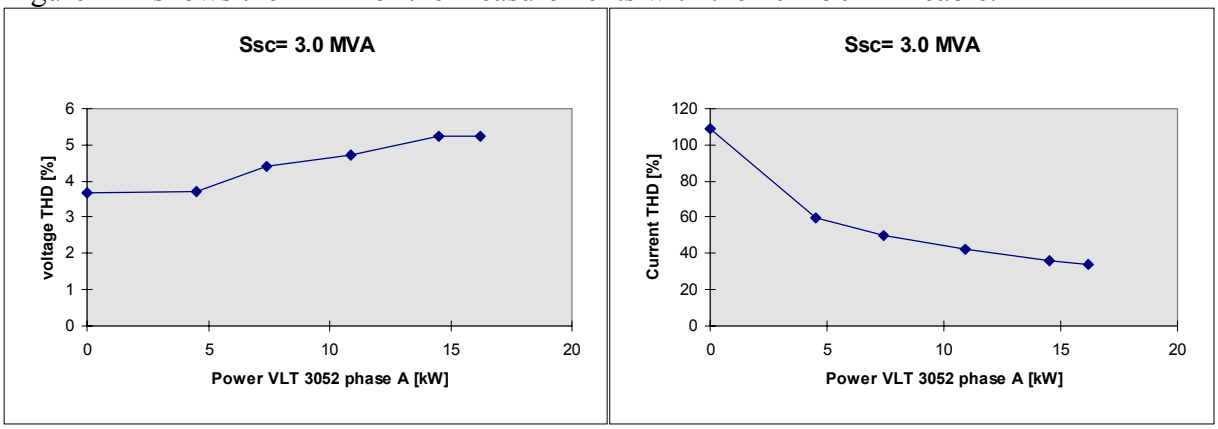

Figure A-2: The THD of the voltage and the current as a function of the per phase (phase a) power of the three-phase rectifier with constant power (8.2 kW) on the single-phase rectifier.

Figure A-3 shows the THD for the measurements with the 240m 50mm^2 cable.

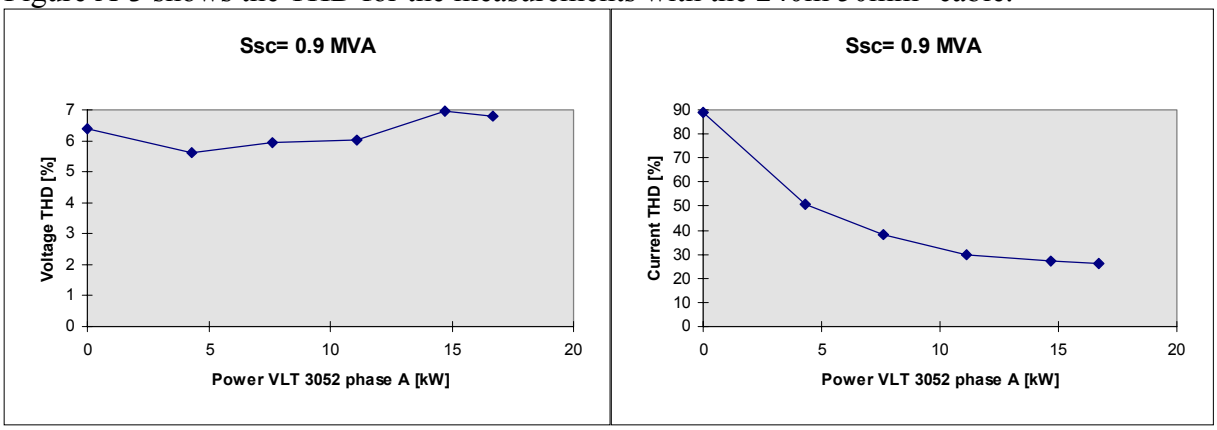

Figure A-3: The THD of the voltage and the current as a function of the per phase (phase a) power of the three-phase rectifier with constant power (7.4 kW) on the single-phase rectifier.

Figure A-4 shows the THD for the measurements with the 240m 50mm^2 + 200m 25mm^2 cable.

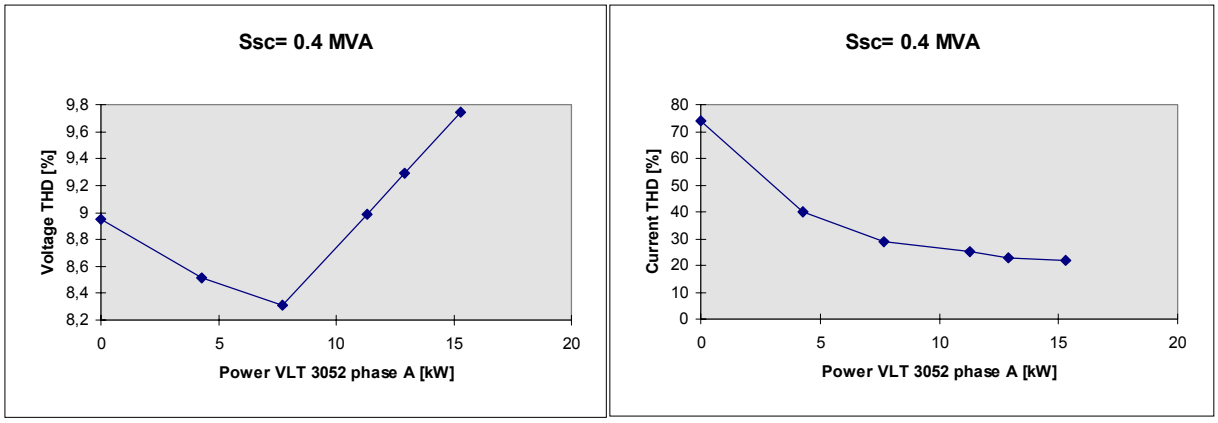

Figure A-4: The THD of the voltage and the current as a function of the per phase (phase a) power of the three-phase rectifier with constant power (6.7 kVA) on the single-phase rectifier.

It is clearly shown that the current THD is decreased significantly when connecting three-phase diode rectifier load to existing single-phase rectifier load. This is due to different phase angles of the 5th and 7th harmonic current. Furthermore, in some cases the voltage THD actually is decreased when connecting a three-phase diode rectifier to the grid with existing single-phase non-linear loads. (See also Figure A-3 and Figure A-4).

A.1.2 The 5th and 7th harmonics

For illustrating that the current and voltage THD reduction comes from reduction (cancellation) of the 5th and 7th harmonic the 5th and 7th harmonic current and voltage will be shown in Table A-2.

Cable	10m 50mm2	40m 50mm2	240m 50mm2	240m 50mm2 + 200m 25mm2
No load	v5 = 0.80 % v7 = 0.21 %	v5 = 0.83 % v7 = 0.15 %	v5 = 0.84 % v7 = 0.17 %	v5 = 0.87 % v7 = 0.14 %
1-phase rectifier only	v5 = 1.67 % v7 = 1.61 % i5 = 62.4 % i7 = 38.0 %	v5 = 2.12 % v7 = 1.60 % i5 = 60.0 % i7 = 33.7 %	v5 = 3.56 % v7 = 1.19 % i5 = 43.4 % i7 = 14.4 %	v5 = 4.15 % v7 = 0.24 % i5 = 28.7 % i7 = 1.2 %
3-phase rectifier only	v5 = 1.12 % v7 = 1.12 % i5 = 63.3 % i7 = 42.1 %	v5 = 1.28 % v7 = 1.15 % i5 = 62.9 % i7 = 41.6 %	v5 = 1.54 % v7 = 1.53 % i5 = 58.4 % i7 = 34.6 %	v5 = 1.96 % v7 = 1.67 % i5 = 49.9 % i7 = 24.6 %
3-phase & 1-phase	v5 = 0.90 % v7 = 1.41 % i5 = 22.9 % i7 = 23.2 %	v5 = 0.88 % v7 = 1.70 % i5 = 20.6 % i7 = 20.7 %	v5 = 2.03 % v7 = 1.73 % i5 = 14.5 % i7 = 11.4 %	v5 = 2.68 % v7 = 1.23 % i5 = 5.1 % i7 = 5.3 %
3-phase rectifier only	v5 = 1.46 % v7 = 1.25 % i5 = 48.6 % i7 = 28.0 %	v5 = 1.56 % v7 = 1.07 % i5 = 47.2 % i7 = 26.8 %	v5 = 2.05 % v7 = 1.54 % i5 = 41.2 % i7 = 19.1 %	v5 = 2.76 % v7 = 1.59 % i5 = 36.4 % i7 = 12.5 %
3-phase & 1-phase	v5 = 0.23 % v7 = 1.98 % i5 = 17.9 % i7 = 23.3 %	v5 = 0.64 % v7 = 2.09 % i5 = 16.6 % i7 = 21.7 %	v5 = 1.34 % v7 = 2.56 % i5 = 9.6 % i7 = 13.3 %	v5 = 1.69 % v7 = 2.24 % i5 = 8.9 % i7 = 8.1 %
3-phase rectifier only	v5= 1.75 % v7 = 1.04 % i5 = 39.0 % i7 = 20.0 %	v5 = 1.88 % v7 = 1.00 % i5 = 37.8 % i7 = 18.4 %	v5 = 2.52 % v7 = 1.39 % i5 = 34.1 % i7 = 13.1 %	v5 = 3.89 % v7 = 1.47 % i5 = 31.1 % i7 = 8.1 %
3-phase & 1-phase	v5 = 0.06 % v7 = 2.12 % i5 = 14.1 % i7 = 22.8 %	v5 = 0.28 % v7 = 2.24 % i5 = 13.5 % i7 = 21.5 %	v5 = 0.84 % v7 = 2.96 % i5 = 10.1 % i7 = 13.6 %	v5 = 0.73 % v7 = 3.36 % i5 = 11.9 % i7 = 8.9 %
3-phase rectifier only	v5 = 2.25 % v7 = 1.08 % i5 = 35.8 % i7 = 16.1 %	v5 = 2.24 % v7 = 1.08 % i5 = 33.9 % i7 = 14.8 %	v5 = 3.12 % v7 = 1.56 % i5 = 31.1 % i7 = 10.4 %	v5 = 4.35 % v7 = 1.80 % i5 = 29.0 % i7 = 8.1 %
3-phase & 1-phase	v5 = 0.12 % v7 = 2.27 % i5 = 12.3 % i7 = 20.9 %	v5 = 0.12 % v7 = 2.75 % i5 = 11.7 % i7 = 19.9 %	v5 = 0.19 % v7 = 3.59 % i5 = 11.5 % i7 = 13.5 %	v5 = 0.23 % v7 = 3.99 % i5 = 13.8 % i7 = 9.2 %
3-phase rectifier only	v5 = 2.06 % v7 = 1.24 % i5 = 32.0 % i7 = 13.8 %	v5 = 2.33 % v7 = 1.06 % i5 = 32.3 % i7 = 13.7 %	v5 = 3.61 % v7 = 1.53 % i5 = 30.4 % i7 = 9.7 %	v5 = 5.20 % v7 = 1.92 % i5 = 27.0 % i7 = 6.9 %
3-phase & 1-phase	v5 = 0.66 % v7 = 2.69 % i5 = 11.5 % i7 = 19.9 %	v5 = 0.15 % v7 = 2.69 % i5 = 11.7 % i7 = 19.4 %	v5 = 0.22 % v7 = 3.73 % i5 = 13.1 % i7 = 13.2 %	v5 = 0.93 % v7 = 4.62 % i5 = 14.5 % i7 = 8.9 %

Table A-2: The 5th and 7th harmonic current and voltage in percent of the fundamental.

The following figures shows the 5th and 7th harmonic current and voltage as a function of the three-phase load when mixing single-phase and three-phase diode rectifiers where the load of the single-phase diode rectifier is fixed.

Figure A-5 shows the 5th and 7th harmonic distortion for the measurements with the 10m 50mm^2 cable.

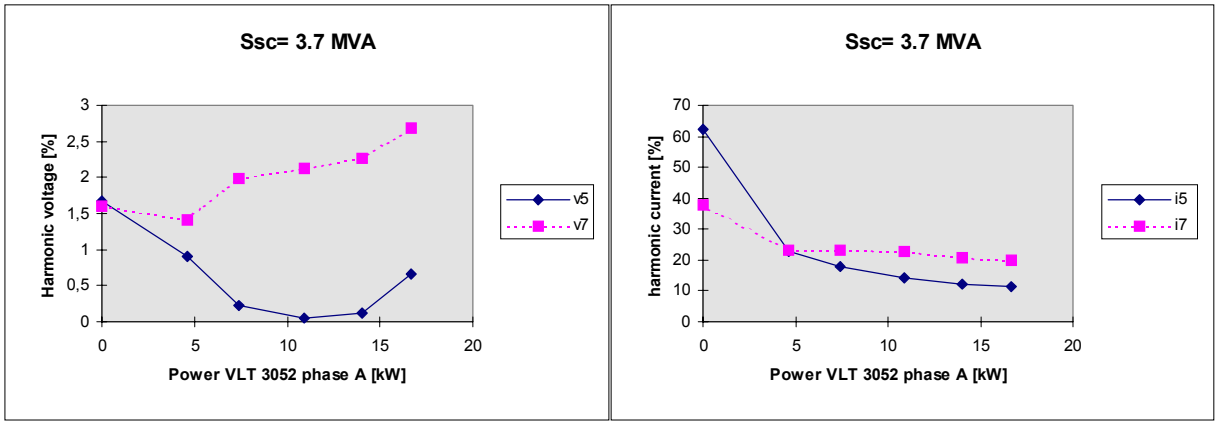

Figure A-5: The 5th and 7th harmonic voltage and current as a function of the per phase (phase a) power of the three-phase rectifier with constant power (8.1 kW) on the single-phase rectifier.

Figure A-6 shows the 5th and 7th harmonic distortion for the measurements with the 40m 50mm^2 cable.

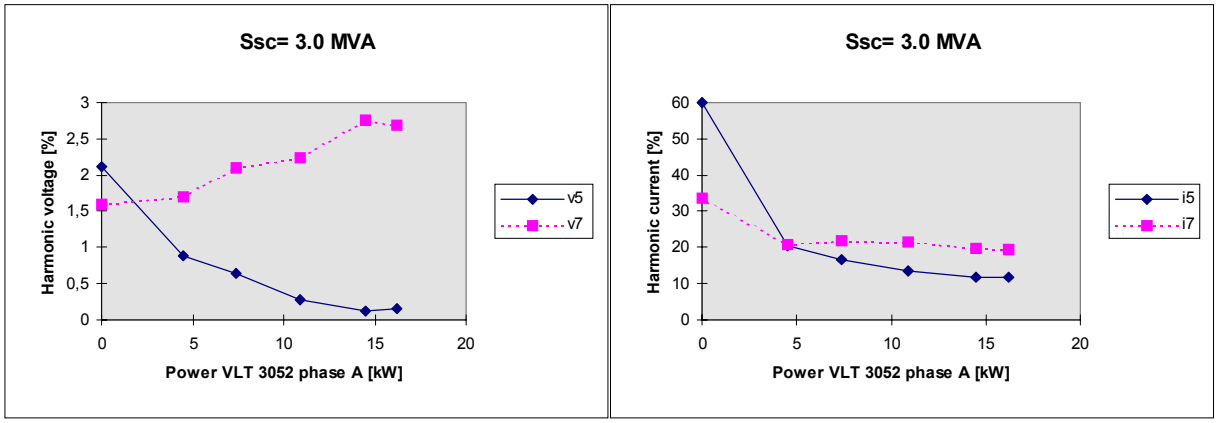

Figure A-6: The 5th and 7th harmonic voltage and current as a function of the per phase (phase a) power of the three-phase rectifier with constant power (8.2 kW) on the single-phase rectifier.

Figure A-7 shows the 5th and 7th harmonic distortion for the measurements with the 240m 50mm^2 cable.

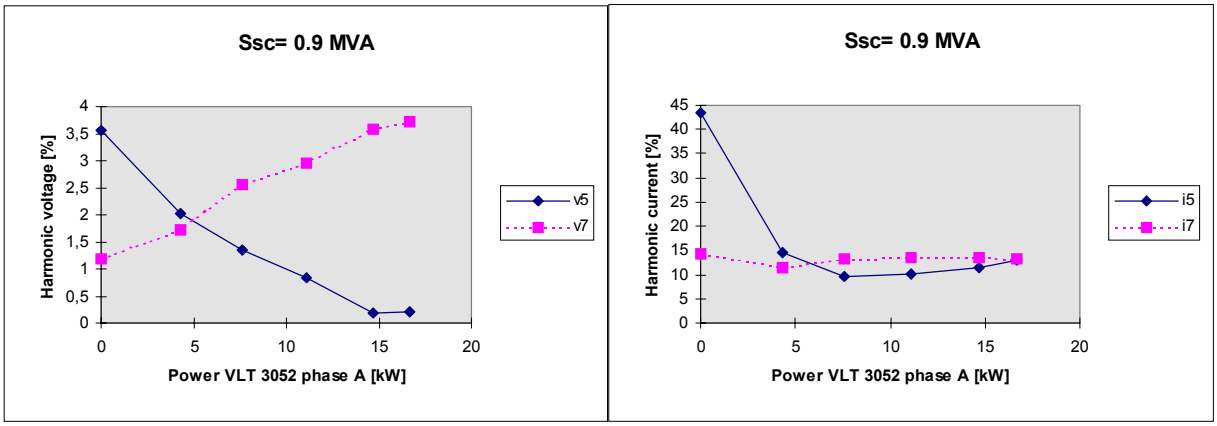

Figure A-7: The 5th and 7th harmonic voltage and current as a function of the per phase (phase a) power of the three-phase rectifier with constant power (7.4 kW) on the single-phase rectifier.

Figure A-8 shows the 5th and 7th harmonic distortion for the measurements with the 240m 50mm^2 + 200m 25mm^2 cable.

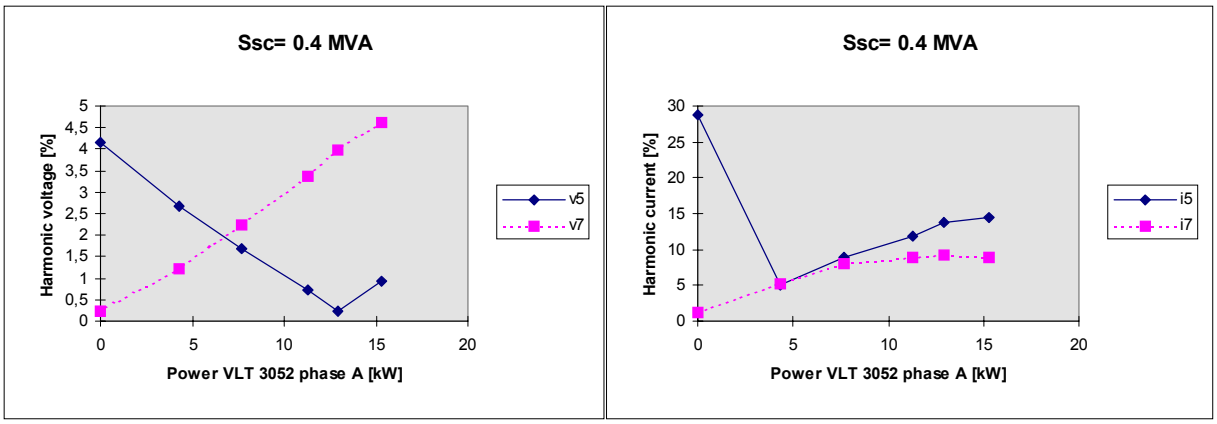

Figure A-8: The 5th harmonic voltage and current as a function of the per phase (phase a) power of the three-phase rectifier with constant power (6.7 kW) on the single-phase rectifier.

Again it is clearly shown that the 5th and partly the 7th harmonic current is decreased when connecting a three-phase diode rectifier to an existing single-phase diode rectifier load.

The reader could wonder why it seems that the 7th harmonic voltage increases even though the 7th harmonic current is more or less constant as shown in Figure A-7. The reason is quit simple: The current is expressed in percent of the fundamental and a constant 7th harmonic current (in percent of the fundamental) as a function of the (fundamental) load is in reality a increasing 7th harmonic current (in absolute values) and hence the 7th harmonic voltage is increasing.

The absolute values of the 5th and 7th harmonic current are shown in Table A-3.

Cable	10m 50mm2	40m 50mm2	240m 50mm2	240m 50mm2 + 200m 25mm2
No load				
1-phase rectifier only	i5 = 22.49 A i7 = 13.68 A	i5 = 21.83 A i7 = 12.25 A	i5 = 14.78 A i7 = 4.90 A	i5 = 9.15 A i7 = 0.39 A
3-phase rectifier only	i5 = 12.90A i7 = 8.59 A	i5 = 12.44 A i7 = 8.22 A	i5 = 11.30 A i7 = 6.69 A	i5 = 9.86 A i7 = 4.86 A
3-phase & 1-phase	i5 = 13.57 A i7 = 13.78 A	i5 = 12.03 A i7 = 12.08 A	i5 = 7.00 A i7 = 5.95 A	i5 = 2.44 A i7 = 2.55 A
3-phase rectifier only	i5 = 15.85 A i7 = 9.14 A	i5 = 15.54 A i7 = 8.84 A	i5 = 14.23 A i7 = 6.58 A	i5 = 13.29 A i7 = 4.55 A
3-phase & 1-phase	i5 = 12.50 i7 = 16.31 A	i5 = 11.49 A i7 = 15.00 A	i5 = 6.17 A i7 = 8.56 A	i5 = 5.29 A i7 = 4.80 A
3-phase rectifier only	i5 = 18.69 A i7 = 9.58 A	i5 = 18.43 A i7 = 8.99 A	i5 = 17.44 A i7 = 6.72 A	i5 = 17.00 A i7 = 4.46 A
3-phase & 1-phase	i5 = 11.86 A i7 = 19.23 A	i5 = 11.05 A i7 = 17.58 A	i5 = 8.04 A i7 = 10.86 A	i5 = 9.34 A i7 = 7.04 A
3-phase rectifier only	i5 = 22.28 A i7 = 10.00 A	i5 = 22.03 A i7 = 9.63 A	i5 = 21.45 A i7 = 7.17 A	i5 = 18.84 A i7 = 5.24 A
3-phase & 1-phase	i5 = 11.94 A i7 = 20.32 A	i5 = 11.51 A i7 = 19.67 A	i5 = 11.22 A i7 = 13.21 A	i5 = 11.91 A i7 = 8.22 A
3-phase rectifier only	i5 = 23.65 A i7 = 10.21 A	i5 = 23.47 A i7 = 9.95 A	i5 = 24.10 A i7 = 7.66 A	i5 = 21.25 A i7 = 5.45 A
3-phase & 1-phase	i5 = 12.46 A i7 = 21.54 A	i5 = 12.62 A i7 = 20.91 A	i5 = 13.96 A i7 = 14.06 A	i5 = 15.17 A i7 = 9.28 A

Table A-3: The 5^{th} and 7^{th} harmonic current in absolute values.

It should be noted that the ac-impedance has the most influence on the higher harmonic currents (mainly dominated by the commutation). This is the reason why the 5^{th} harmonic current is quit constant for the three-phase rectifier (which has a dc-link inductance) and the 7^{th} harmonic current is filtered by the ac-impedance. (For the higher harmonics this filtering is even stronger).

A.2 Measurement series 2

Instead of the Danfoss frequency converter a Fuji frequency converter is used in measurement series 2. The measurements are made with a 10m four wire 50mm^2 Al. cable (combination 1) connected between the transformer and the frequency converter. The measurements are made without connection of the single-phase diode rectifier.

The Fuji frequency converter is a FRENIC 5000GS9 (FRN45G9S) with a rated input of 69 kVA. The Fuji frequency converter has no dc-link filter which will result in higher harmonic currents compared with the Danfoss VLT 3052.

The results are shown in Table A-1:

Power [kW]	0	4.2	7.5	10.8	15.1	16.3
Time	15.42	15.45	15.46	15.47	15.50	15.51
THDv [%]	0.92	2.59	3.53	4.34	5.26	5.61
THDi [%]	-	106	91	84	75	73
i5 [%]	-	79	71	69	63	62
i7 [%]	-	61	51	44	38	36
v5 [%]	0.82	1.52	2.12	2.77	3.63	3.70
v7 [%]	0.16	1.39	2.15	2.47	3.01	3.04

Table A-1: The results of measurement series 2.

As expected the harmonic distortion of this three-phase frequency converter without an dc-link inductance is somewhat higher than the harmonic distortion of the Danfoss VLT 3052 with dc-link inductance. (At full load the total harmonic distortion for the Danfoss VLT 3052 was: $THD_i = 53\%$ $THD_v = 3.98\%$.)

A.3 Measurement series 3

For measurement series 3 the same system is used as sketched in Figure A-1. In measurement series 3 the cable length is fixed (10m). The MV measurements are made on the secondary side of the 50/10 kV transformer used for supplying the 10kV laboratory. The distant between the 50/10 kV transformer and the 10/04 kV is about 3.5 km. There is no other load on the 10 kV line besides the 10/04 kV 200 kVA transformer and the respective load.

The measurements presented her are:

- VLT 3052 at full load (50 kVA)
- The single phase rectifier (12 kVA)
- Mixing of VLT 3052 (full load) and the single phase rectifier
- Active rectifier

There exist some other measurements which will not be presented here: VLT 3052 with partial load, mixing the VLT 3052 (partial load) with the single phase rectifier and measurements with the FUJI frequency converter with full and partial load. This measurements are not presented because they basically shows the same as presented here with the other measurements.

A.3.1 VLT 3052 with full load

Figure A-1 shows the measured MV currents when the VLT 3052 is connected to the transformer with full load.

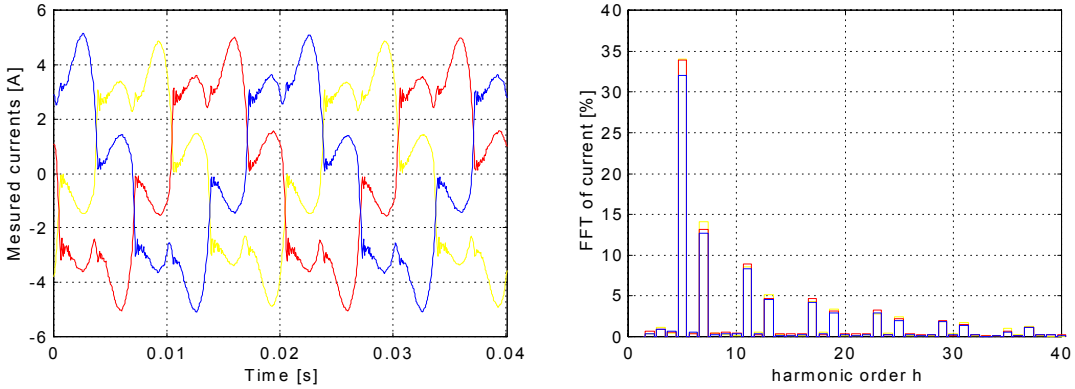

Figure A-1: Measured phase currents of MV line and the respective fourier spectrum of the currents.

The total harmonic distortion is calculated to:
$THD_{i,a}$ = 38.9%, $THD_{i,b}$ = 38.5% and $THD_{i,c}$ = 36.4%
$THD_{v,a}$=0.61%, $THD_{v,b}$=0.77% and $THD_{v,c}$= 0.70%
The THD calculated up to the 40th harmonic.

The harmonic voltages are not affected compared to the background distortion.

A.3.2 Single-phase rectifier

Figure A-2 shows the three currents when the single-phase rectifier is connected to the transformer. Since the transformer is a delta/wye transformer the single phase current affects two phases while the third phase is not affected. The small (sinusoidal) current in the third phase which also can be seen in the other two phases is the magnetising current of the transformer.

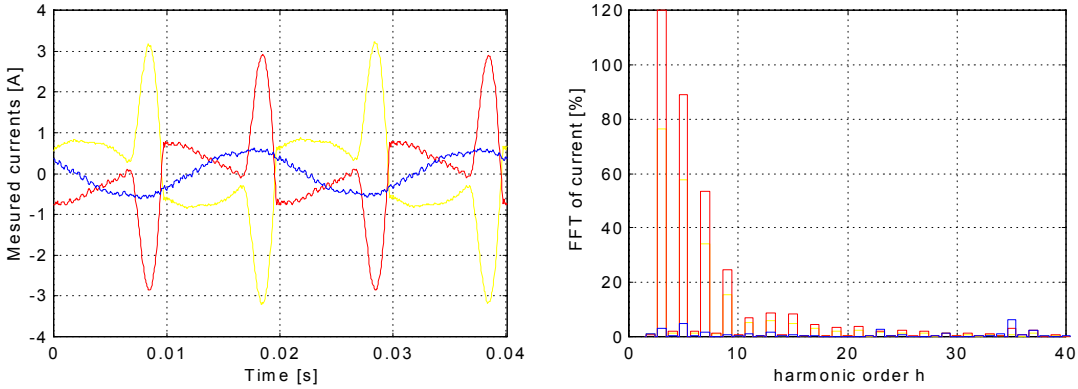

Figure A-2: Measured phase currents of MV line and the respective Fourier spectrum of the currents.

As it can be seen in the Fourier spectrum of Figure A-2 the current of phase b is more distorted than the current of phase a. This could be caused by the placement of the peak current of the single-phase rectifier, which is placed two different places on the period of the magnetising current.

The total harmonic distortion is calculated to:
$THD_{i,a}$ = 103.4%, $THD_{i,b}$ = 161.5% and $THD_{i,c}$ = 10.1%

$THD_{v,a}$=0.57%, $THD_{v,b}$=0.77% and $THD_{v,c}$= 0.69%
The harmonic voltages are not affected compared to the background distortion.

A.3.3 Mixing single-phase rectifier and VLT 3052 with full load

Figure A-3 shows the three currents when the single-phase rectifier and the VLT 3052 with full load is connected to the transformer. The interesting part is that the current distortion is reduced in all three phases compared to the current when only the three phase rectifier is connected. Furthermore, the current of phase a and b is significantly reduced compared to when only the single-phase rectifier is connected while the current distortion in phase c naturally is increased.

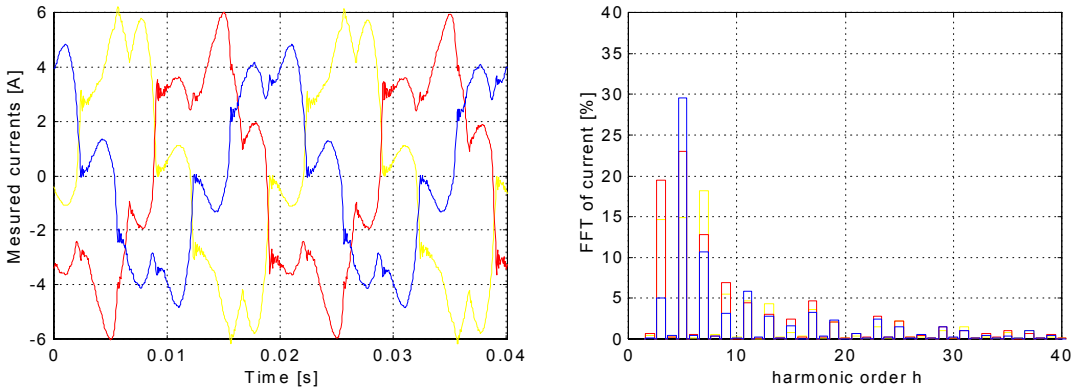

Figure A-3: Measured phase currents of MV line and the respective fourier spectrum of the currents.

The total harmonic distortion is calculated to:
$THD_{i,a}$ = 29.5%, $THD_{i,b}$ = 34.6% and $THD_{i,c}$ = 33.2%
$THD_{v,a}$=0.71%, $THD_{v,b}$=0.64% and $THD_{v,c}$= 0.55%

The harmonic voltages are not affected compared to the background distortion.

A.3.4 The active rectifier

Figure A-4 shows the current of phase a measured directly on the active rectifier while Figure A-5 shows the current of all three phases on the medium voltage line while the active rectifier is connected.

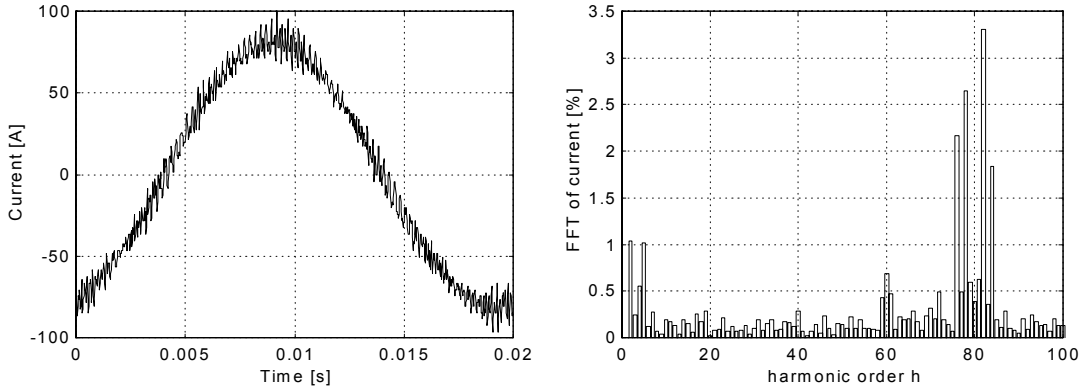

Figure A-4: Current of the active rectifier in phase a on the secondary side (0.4 kV) of the transformer.

The calculated total harmonic current distortion (to the 40th harmonic) of the LV current of phase a is $THD_{i,a} = 1.8$ %.

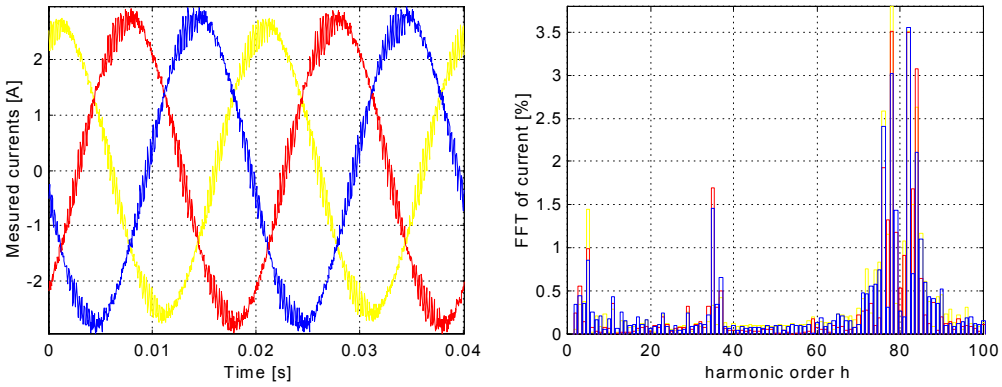

Figure A-5: Current of the active rectifier in the three phases on the MV line.

The total harmonic distortion on the MV line is calculated to:
$THD_{i,a} = 1.8$ %, $THD_{i,b} = 2.3\%$ and $THD_{i,c} = 2.2\%$
$THD_{v,a}=0.87$ %, $THD_{v,b}=0.61\%$ and $THD_{v,c}= 0.96\%$
The THD calculated up to the 40th harmonic.

It should be noted that the fourier spectrum and the current THD_i on both the LV and the MV side almost is identical. This means that the switched current goes right through the transformer and will not only affect neighbour users on the same transformer but also will affect apparatus connected to the MV line or users on other transformers.

Because the THD value only is calculated up to the 40th harmonic the voltage THD_v is unaffected by the switching frequency, but a small amount of 0.1% voltage distortion around the 80th harmonic is measured.

A.4 Conclusion

The measurements were primary made for verifying the models of the diode rectifier, LV cables and the MV/LV transformer used for SABER simulations. Verifying of these models are shown in Chapter 3. However, some conclusions can be drawn from these measurements only.

It is clearly shown that adding a three-phase diode rectifier load to an existing single-phase rectifier load (or visa versa) will reduce the current THD_i. In some cases (very weak grid) even the voltage distortion is reduced. It is also shown that this harmonic distortion reduction is caused by cancellation of the 5th harmonic.

The secondary goal is to determine the influence of switched currents and voltages on the MV-side. Here it is clearly shown that the switching noise is transferred through the transformer without any reduction.

B. Hc and THD_i Values for the Diode Rectifier

In this Appendix the enlarged Figures of the Hc and THDi values of the diode rectifier as a function of the short circuit ratio are shown. The idea is that the Hc-values shown can be used to calculate the total harmonic voltage distortion as shown in chapter 3.

B.1 Basic Three-Phase Diode Rectifier

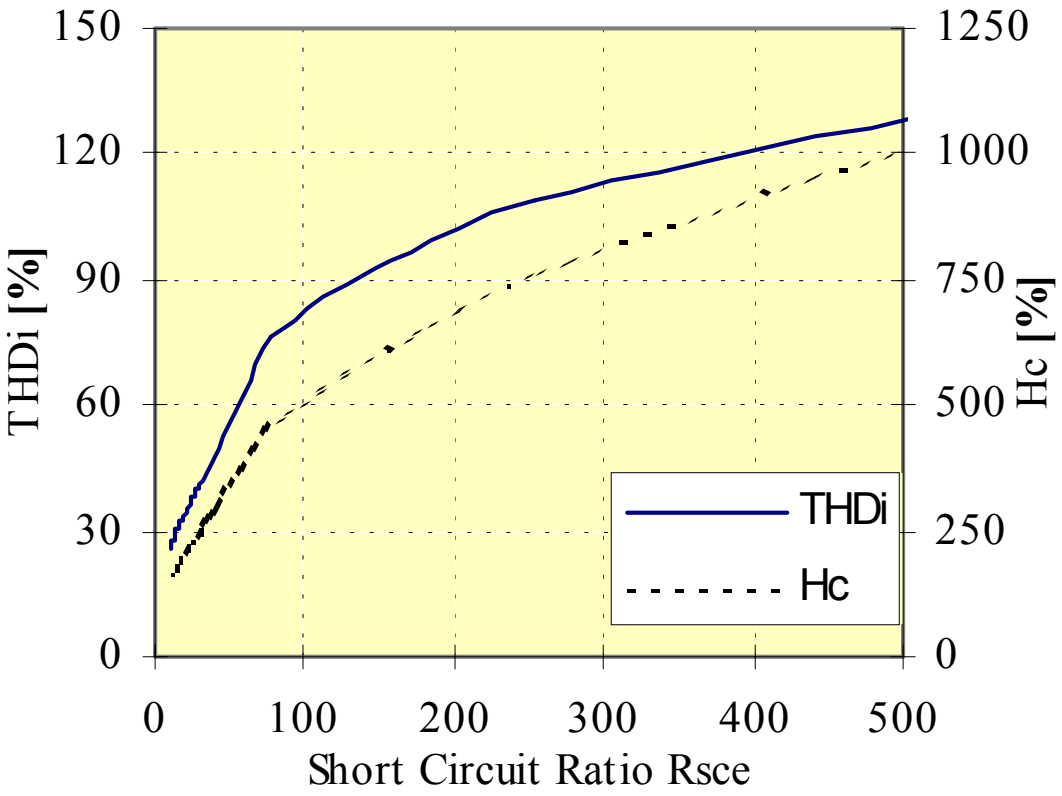

Figure B-1: Hc and THD_i values for the three-phase diode rectifier as a function of the short circuit ratio without any dc-link inductance.

B.2 Three-Phase Diode Rectifier with 3% dc-link Inductance

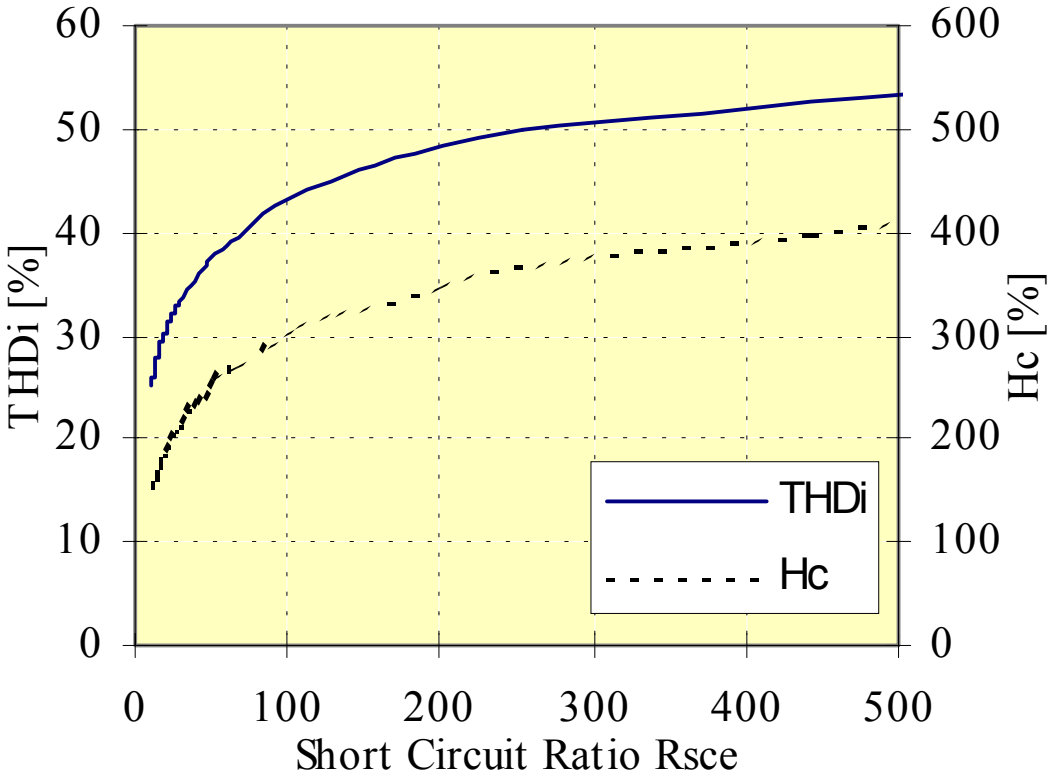

Figure B-2: Hc and THD_i values for the three-phase diode rectifier as a function of the short circuit ratio with a 3 % dc-link inductance.

B.3 Basic Single-Phase Diode Rectifier

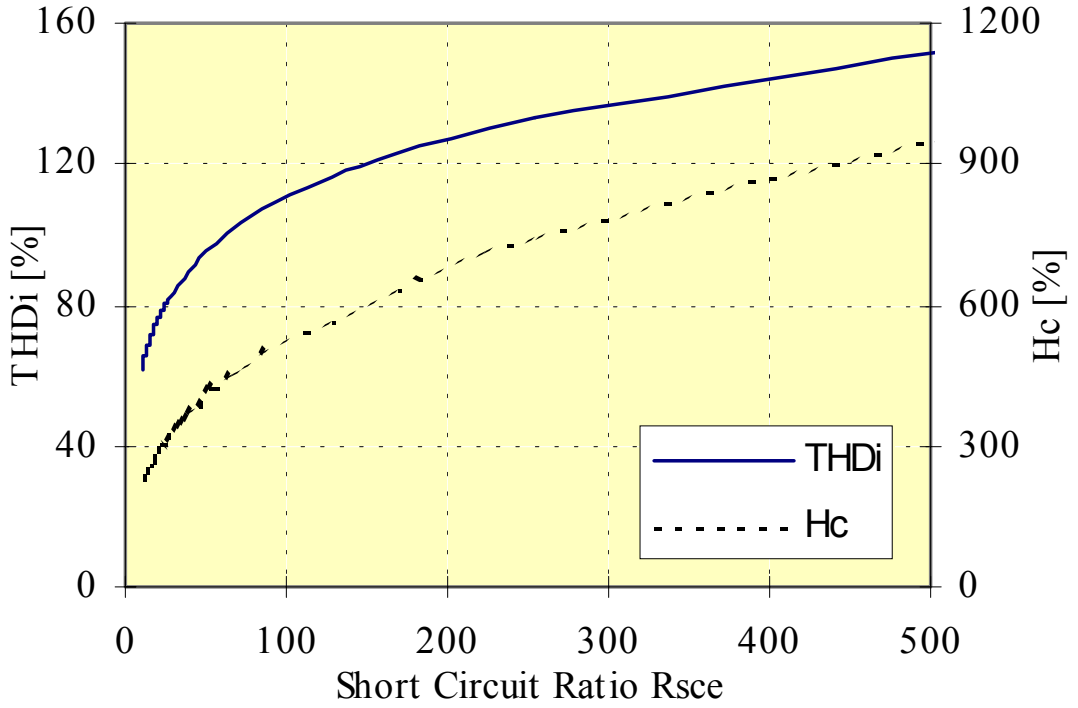

Figure B-3: Hc and THD_i values for the single-phase diode rectifier with varying short circuit ratio.

C. Single Switch Boost Rectifier

Even though the focus is on three phase rectifiers excellent solutions exist for the single-phase rectifier based on the boost topology. This solution is to some extend also applicable for the three-phase rectifier therefore this solution is reviewed here.

A single-phase rectifier followed by a dc-dc converter (Figure C-1 a) is widely used for active power factor correction (PFC). The dc-dc converter following the diode rectifier can be as various as boost, buck, buck-boost etc. depending on the application. Furthermore, in the recent years the focus has been on zero current switched (ZCS) and zero voltage switch (ZVS) of the used dc-dc converters, in order to reduce the power losses.

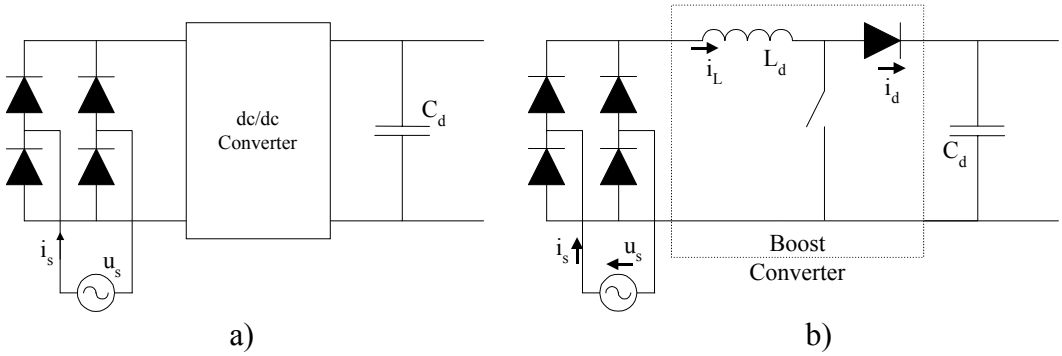

Figure C-1: Diode rectifier followed by a dc-dc converter.

The amount of papers concerning different topologies and their control is tremendous and describing all of them would be out of the scope of this thesis. For describing the principals of these topologies the operation of the diode rectifier followed by the single switch boost dc-dc converter (Figure C-1 b) will be explained in the following. However ref. [Salmon 1995] gives an overview of the different topologies for PWM boost rectifiers both for single and three-phase ac supplies.

The main control strategies can be classified into two groups:

- The multiplier approach
- The voltage follower approach

Controlling the dc-dc converter as a current sink and still control the dc-link requires feedback from both the line current i_s and the value of the rectified line voltage $|u_s|$. The feedback control loop is shown in Figure C-2. Because of the multiplier in the control loop this type of control is called the multiplier approach.

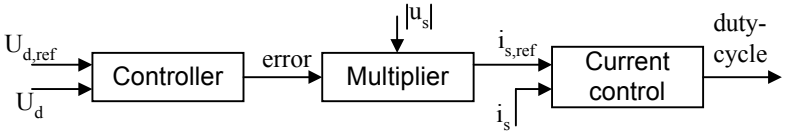

Figure C-2: Control block diagram for the multiplier approach.

The voltage follower approach is a straight forward approach and can easily be explained. Assuming the current is zero at the moment where the boost switch is turned-on. The input phase would be shorted through the rectifier diodes, the inductor and the boost switch.

Consequently the current would increase proportional with the supply voltage. Hence if the duty-cycle of the boost switch is constant and the current is zero before the next turn on the average current would follow the supply voltage. This type of control is called the voltage follower approach.

Rectifiers under multiplier control usually operate at continues conduction mode (CCM) while rectifiers under voltage follower approach usually operates under discontinues conduction mode (DCM). Converters operating under DCM are usually used for low power applications while CCM becomes necessary when higher power level is required. This is due to current stress on the switch and the current ripple in the inductor gets to large at higher power levels. [Lai, Smedly 1997]. Both the DCM and CCM are shown in Figure C-3.

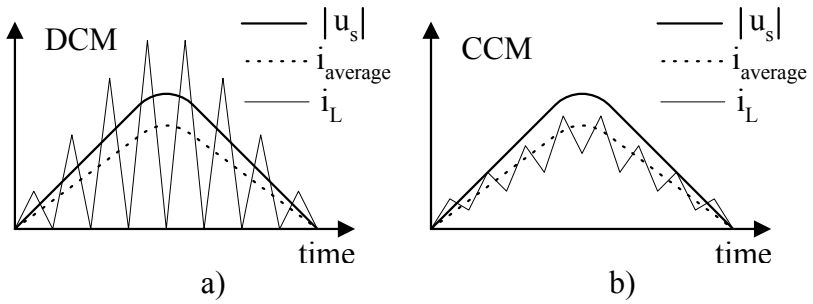

Figure C-3: a) The rectified line voltage, the average line current and the line current for the DCM. b) The rectified line voltage, the average line current and the line current for the CCM.

It can be concluded that the main advantage of the multiplier approach is the possibility to obtain CCM, while the disadvantage are the line current and rectified line voltage feedback. However in the recent years some papers has been presented control methods for CCM without the multiplier and the voltage sensor, such as [Maksimovic 1994] and [Maksimovic et al.1995].

The Voltage follower control has the advantage of its simplicity and there is no need for feedback, except for the feedback of the dc-link voltage. The main disadvantage is that this approach is limited to low power applications due to high stresses of the switch and the inductance. Furthermore, the diodes of the rectifier has to be of the fast-recovery type since the discontinued current is filtered on the line side of the rectifier. This means that the on-state losses would be higher compared to diodes used in the standard diode rectifier [Mohan et al. 1995].

Both control strategies have following disadvantages:

- An EMC filter must be used on the input-line in front of the rectifier to prevent the conducted- and common-mode noise to enter the utility grid.
- High switching frequency is necessary to keep L_d and the current ripple as small as possible. Hence the switching frequency is a compromise between a small inductance and the switching losses.
- Power diode in series with the power flow resulting increased losses compared to the standard diode rectifier.

- For satisfactory performance a boost ratio (M) of at least 1.5 is necessary [Mao et al. 1997]. This increases the switching losses of the inverter.

A major advantage for the single-switch boost topology is that there exist several integrated circuits, which gives a cheap solution. Therefore especially for low power applications there is no need for further investigations of this topic even though there is always need for improvements.

For three-phase converters [Prasad et al. 1989] was the first to introduce dc-dc converter in the dc link as shown in Figure C-4. The main difference to the single-phase boost topology is that the only way to control the current of the three phases with one switch is to use the voltage follower approach and thereby having DCM. Because of the above mentioned disadvantages and the disadvantages of the voltage follower approach this solution is impractical for high power three phase applications.

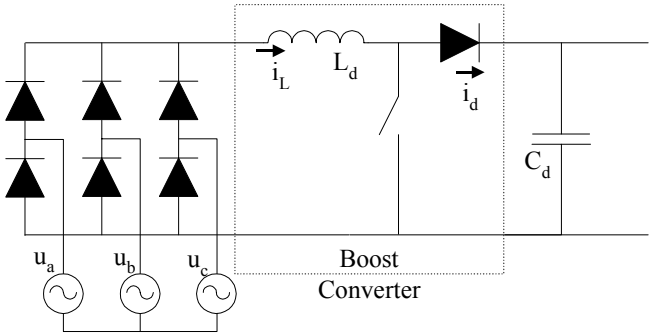

Figure C-4: Three-phase diode rectifier followed by a boost converter. This topology was first presented by [Prasad et al. 1989].

D. Publications

1 Steffan Hansen, Peter Nielsen, Frede Blaabjerg ”Harmonic Cancellation by Mixing Nonlinear Single-phase and Three-phase Loads” IEEE Trans. on Industry Applications, Vol. 36, No. 1, 2000, pp. 152 - 159.

2 Steffan Hansen, Prasad N. Enjeti, Jae H. Hahn, Frede Blaabjerg ”An Integrated Single-Switch Approach to Improve Harmonic Performance of Standard PWM Adjustable speed drives” IEEE Trans. on Industry Applications, Vol. 36, No. 4, 2000, pp. 1189-1196.

3 Steffan Hansen, Mariusz Malinowski, Frede Blaabjerg, Marian Kazmierkowski ”Sensorless Control Strategies for PWM Rectifier” Conf. Proceed. of IEEE-APEC ‘00, New Orleans, USA, Vol. 2, pp 832 – 839.

4 Steffan Hansen, Peter Nielsen, Paul Thøgersen “Harmonic Distortion and Reduction Techniques of PWM Adjustable Speed Drives – A Cost Benefit Analysis” Conf. Proceed. NORpie/2000, Aalborg, Denmark, pp. 271-277.

Other related publications:

Steffan Hansen, Uffe Borup, Frede Blaabjerg ”Quasi 12-pulse rectifier for Adjustable Speed Drives” paper accepted for IEEE APEC Conf., 2001

Mariusz Malinowski, Steffan Hansen, Marian Kazmierkowski, Frede Blaabjerg, Gill Marques ”Virtual Flux Based Direct Power Control of Three-Phase PWM Rectifiers” Conf. Proceed. of IEEE-IAS ‘00, Rome, Italy 2000, Vol. 4, pp. 2369 - 2375.

Steffan Hansen, Prasad N. Enjeti, Jae H. Hahn, Frede Blaabjerg ”An Integrated Single-Switch Approach to Improve Harmonic Performance of Standard PWM Adjustable speed drives” Conf. Proceed. of IEEE-IAS ‘99, Phoenix, USA, Vol. 2, pp.789 – 796.

Steffan Hansen, Peter Nielsen, Frede Blaabjerg ”Harmonic Cancellation by Mixing Non-linear Single-phase and Three-phase Loads” Conf. Proceed. of IEEE-IAS ‘98, St. Louise, USA 1998, Vol. 2, pp.1261 - 1269.

Steffan Hansen, Peter Nielsen, Paul Thøgersen “Harmonic Distortion Reduction Techniques of PWM Adjustable Speed Drives – A Cost Benefit Analysis” Power Quality Assurance Magazine, scheduled for: Vol. 11, No. 6, Nov/Dec 2000

Harmonic Cancellation by Mixing Nonlinear Single-Phase and Three-Phase Loads

Steffan Hansen, Peter Nielsen, and Frede Blaabjerg, *Senior Member, IEEE*

***Abstract*—The voltage on the distribution line is, in most cases, distorted even at no load of the transformer. This is due to the "background" distortion on the medium-voltage line caused by the large number of single-phase nonlinear loads, such as PC's, TV's, VCR's, etc. This paper proposes a method to mix single-phase and three-phase nonlinear loads and reduce the harmonic currents significantly. The dependence of the phase angle of the harmonic currents as a function of the short-circuit impedance is investigated using SABER for the three-phase and the single-phase diode rectifier both with and without dc-link inductance. The phase angle of the fifth harmonic current of a three-phase diode rectifier is always in counterphase with the fifth harmonic current of a single-phase diode rectifier. This leads to the conclusion that adding three-phase rectifier load can actually improve the power quality at the transformer. This is also validated by a number of on-site measurements in several applications of three-phase adjustable-speed drives.**

***Index Terms*—Diode rectifier, harmonic cancellation, harmonic distortion, nonlinear load.**

I. Introduction

THE exploding use of personal computers and electric loads controlled by power electronics has led to a severe increase of current harmonics drawn from the distribution line. These harmonic currents can, in worst cases, result in the following:

- overheating or derating of transformer;
- overheating of wiring;
- damaging of capacitor banks;
- resonance;
- malfunction of electronic equipment;
- communication interference;
- distorted supply voltage.

Due to the impedance of the distribution line, the harmonic currents lead to harmonic voltage distortion, which results in increased losses or damaging of parallel loads and, in the worst case, to system instability. Because of the drawbacks mentioned, the interest in harmonic distortion has increased in both manufacturers of electronic equipment and the utilities. Some utilities may even consider increasing the charge paid by the customers generating the distortion because of increased losses in transformer and transmission lines.

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This paper deals with the effect of mixing the nonlinear load of three- and single-phase diode rectifiers. Furthermore, the influence of the nonlinear load regarding the voltage background distortion is investigated. The voltage distortion on the transformer secondary side has two origins. One part is coupled from the medium-voltage (MV) side (background distortion) and the other part is generated by the voltage drop in the transformer itself caused by the harmonic currents of the load (load distortion).

Large adjustable-speed drives (ASD's) have often been accused of distorting the distribution line. This paper will show that large three-phase ASD's actually can enhance the resulting voltage distortion with respect to the voltage background distortion.

Because of different phase angles, the addition of the harmonic currents and voltages must be geometrical and not arithmetical, as shown by [1] and [2]. Reference [2] has shown that the background voltage distortion can be reduced when connecting a six-pulse diode rectifier to the distribution line, while the distortion is increased when connecting single-phase diode rectifiers to the distribution line. A complete analysis of the influence of the harmonic currents phase angle from both single- and three-phase rectifier has not yet been done. This leads to the question of phase-angle dependency of the harmonic currents regarding the network impedance for both the single-phase and three-phase diode rectifiers.

Reference [4] has made an investigation into the influence of the short-circuit ratio and the dc-link capacitor on the amplitude and the angular displacement of the harmonic currents regarding the fundamental voltage of a six-pulse diode rectifier. The influence of the dc-link inductance in the rectifier is not included. In [5], the harmonic currents phase-angle dependency of the dc-link inductance for both a single- and three-phase diode rectifier is shown. The influence of the ac-side impedance is not included. This is done in this paper.

This paper will analyze the phase angle of the harmonic currents in single- and three-phase diode rectifiers both with and without dc-link inductance. The effect of mixing both single- and three-phase diode rectifiers will be analyzed, too. Furthermore, the influence of the harmonic currents phase angle on the background voltage distortion will be investigated. A number of experimental results will validate the theory.

II. Harmonic Voltage Background Distortion

The voltage on the low-voltage (LV) distribution line is, in most cases, distorted, even at no load. This is due to the background distortion on the MV and high-voltage (HV) line. References [1] and [6] have pointed out that the harmonic current

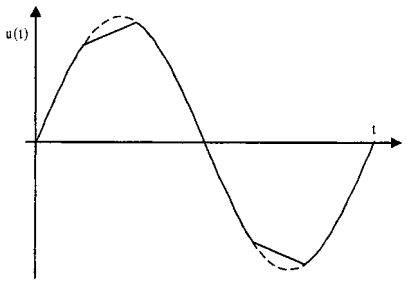


Fig. 1. Typical background voltage waveform with distortion from single-phase loads.

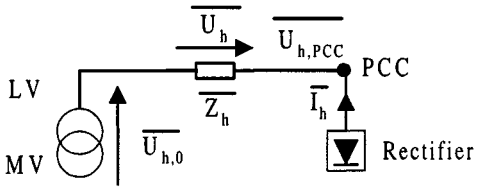


Fig. 2. Harmonic voltage on the PCC as a sum of voltage drop at the transformer and background distortion.

distortion in the MV distribution system is caused by a large number of switch-mode power supplies used in PC's, TV's, VCR's, and stereos connected to the LV line. These current distortions add up in the MV and HV networks. This means the harmonic background voltage distortion is mainly caused by a large number of small single-phase diode rectifiers. The resulting voltage with this kind of load is shown in Fig. 1 and can be seen/measured almost everywhere across Europe. The dominant harmonic voltage is the fifth harmonic. In the MV and HV network, the third harmonic is hardly present, since it is not transmitted over the delta–wye transformer which is widely used for LV distribution lines. Reference [1] has also observed that the higher harmonics tend to cancel each other, since the phase angle of the higher harmonics differs widely.

The resulting harmonic voltage distortion to be measured at the transformer secondary side equals the geometrical sum of the background voltage distortion and the load distortion. A circuit diagram is shown in Fig. 2.

This means the resulting voltage distortion is dependent on the background voltage distortion, the amplitude and phase angle of the harmonic current and the harmonic impedance. This is also shown in (1)

$$\overline{U_{h,\mathrm{PCC}}} = \overline{U_{h,0}} + \overline{U_h} = \overline{U_{h,0}} + \overline{I_h}(R + jhX) \qquad (1)$$

where

$U_{h,\mathrm{PCC}}$	resulting voltage distortion at the point of common coupling (PCC);
$U_{h,0}$	background distortion;
U_h	voltage drop of the harmonic currents;
I_h	hth harmonic current;
R	real part of the impedance Z_h;
jhX	imaginary part of the impedance Z_h as a function of the harmonic number h.

It is important to notice that the background voltage distortion is fixed and will not change as a function of the load on the secondary side of the transformer. This is because the background distortion comes from the MV side and, thereby, has a high short-circuit power. To give an example of the background voltage distortion, a measurement on an MV line is done. These measurements are shown in Figs. 3 and 4.

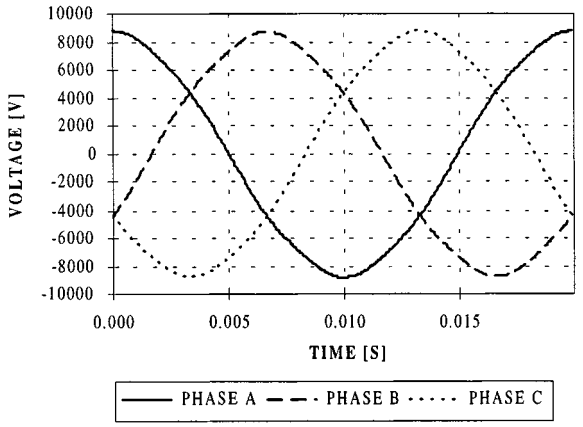


Fig. 3. Measured phase voltages on a 10-kV distribution line.

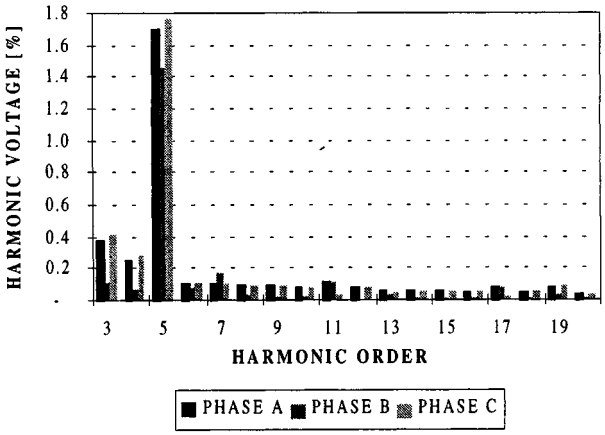


Fig. 4. Harmonic analysis of the measured 10-kV distribution line voltages.

The voltages are measured at the secondary side of a 50/10-kV transformer. The 10-kV distribution line is supplying 16 MV/LV substations where three substations are supplying industry, eight substations are supplying a domestic area, and five substations are supplying miscellaneous. As expected, the dominant harmonic voltage is the fifth harmonic. However, the fifth harmonic current is below 1% when the voltages were measured. This means that the fifth harmonic voltage originates from the 50-kV line.

III. Harmonic Analysis of Rectifier

A commonly used model of the diode rectifier is to assume that the rectifier works as a harmonic current generator. However, simulations in [4] and [5] have shown the harmonic currents of the rectifiers are dependent on both ac impedance and, if any, the impedance of the dc-link filter inductance.

Therefore, simulations using SABER are made with respect to both varying ac-side impedance and with/without a dc-link inductance.

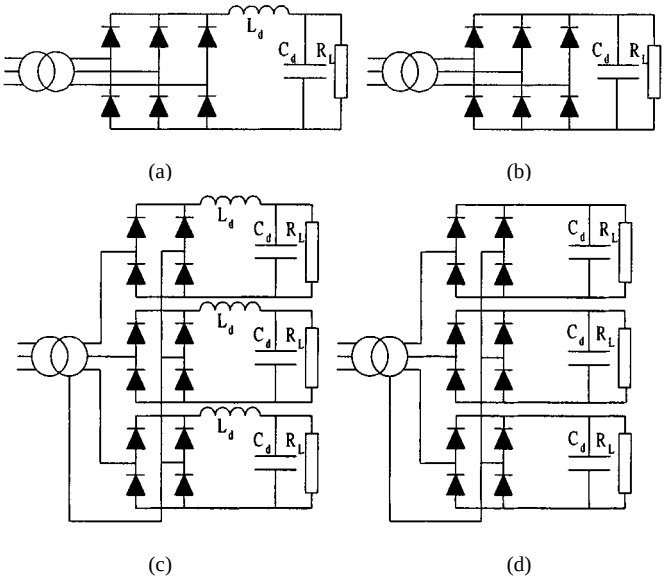


Fig. 5. Circuit diagrams of the simulations. (a) Three-phase rectifier with dc-link inductance. (b) Three-phase rectifier without dc-link inductance. (c) Single-phase rectifier with dc-link inductance. (d) Single-phase rectifier without dc-link inductance. $S_{\rm xfr} = 200$ kVA–6 MVA; $e_x = 5\%$; $e_r = 0.9\%$.

The per-unit notation used in the following is obtained by dividing the 50-Hz impedance ($Z_{50\,\rm Hz}$) by the base impedance (Z_B) of the transformer or rectifier. This is shown in (2)

$$Z_B = \frac{U_{\rm LL}^2}{S_{\rm nom,\,1}} \qquad Z_{pu} = \frac{Z_{50\,\rm Hz}}{Z_B} \tag{2}$$

where $U_{\rm LL}$ is the line-to-line voltage and $S_{\rm nom,\,1}$ is the fundamental nominal power of the transformer or rectifier chosen as base.

The circuit diagrams of the simulations are shown in Fig. 5. A transformer with $e_x = 5\%$ and $e_r = 0.9\%$ is connected to a three-phase diode rectifier with [Fig. 5(a)] or without [Fig. 5(b)] a dc-link inductance. The fundamental input power of the three-phase rectifier is $S_{L,\,1} = 200$ kVA. A similar simulation is also made with three single-phase rectifiers with [Fig. 5(c)] and without [Fig. 5(d)] a dc-link inductance. The fundamental input power of the single-phase rectifiers is $S_{L,\,1} = 67$ kVA each. This gives a three-phase load of 200 kVA. The dc-link capacitor used in Fig. 5(a)–(d) is $C_d = 30\%$ related to the rectifier per-unit notation. The dc-link inductance used in Fig. 5(b)and (d)is $L_{\rm dc} = 3\%$ and it is also related to the rectifier per-unit notation. $L_{\rm dc} = 3\%$ is in the lower end of the average value used in the industry (usually, 3%–5%).

The transformer size $S_{\rm xfr}$ is varied from 200 kVA to 6 MVA which gives a varying ac-side impedance on the secondary side of the transformer. The short-circuit power on the secondary side of the transformer is thereby varied from 4 to 120 MVA which gives a short-circuit ratio $R_{\rm sc} = S_{\rm sc}/S_{L,\,1} = 20$–$600$.

The harmonic currents are simulated with a step of $R_{\rm sc} = 20$. The results of the simulations are shown in the polar plots in Figs. 6 and 7. The line–neutral voltage of phase *A* forms the reference vector (cosine representation) and all angles are measured with respect to this reference vector.

The fifth harmonic current of the three-phase rectifier is within the range of 110°–215°, while the fifth harmonic current of the single-phase rectifier is within the range of 295° and 45°. The phase angles of the fifth harmonic current for the single- and three-phase rectifier differ up to 110° and they are often in counterphase. This means the geometrical sum of the fifth harmonic current of the three- and single-phase rectifier will always be significantly less than the arithmetical sum, and often a total reduction can be obtained. Furthermore, if the only load is a large single- or three-phase rectifier load, there will be no cancellation of the fifth harmonic current because they will be in phase. Due to the large amount of single-phase nonlinear loads on the LV line, the fifth harmonic voltage is the most dominating harmonic distortion on the MV line.

The seventh harmonic current of the three-phase rectifier is in the range of 30°–230°, while it is in the range of 255° and 60° for a single-phase diode rectifier. The worst case is a dc-link inductance in the three-phase rectifier while the single-phase rectifier is connected to a strong distribution line where an arithmetical addition is possible. In a typical case, a large number of single-phase rectifiers is without any dc-link inductance and connected to a weak line (long cables) and a few three-phase rectifiers with dc-link inductance are connected to a strong line (near the transformer); then, the seventh harmonic currents will be in counterphase.

The phase angle of the seventh harmonic current for the single-phase rectifier differs almost 180°. This means that there will be some cancellation of the seventh harmonic current of single-phase rectifiers.

The 11th and 13th harmonic currents for both the single- and three-phase rectifier are in the range of a complete cycle and they are, therefore, very dependent of the transformer impedance (and cable). The phase angle of the 11th and 13th harmonic current differs so much, that there is a high possibility that they will be cancelled in the distribution line.

Another interesting conclusion is that using a dc-link inductance makes the amplitude and phase angle of the harmonic current less dependent on the ac-line impedance. The dc-link inductance of the single-phase rectifier behaves like an ac line impedance.

Figs. 6 and 7 give a powerful tool to evaluate the phase angle and amplitude of possible rectifier configurations as a function of $R_{\rm sc}$ in many industrial applications.

IV. Harmonic Current and Voltage Distortion Reduction

In a typical industrial distribution network or a large office building, there will be a few large three-phase nonlinear loads, e.g., ASD for heating and ventilation, while there will be many small single-phase nonlinear loads, in particular, PC's. The short-circuit capacity $S_{\rm sc}$ in an LV network is mainly limited by the LV transformer and the LV cable impedance. The MV impedance can be neglected.

A case study is done and simulations are carried out to evaluate the results of Figs. 6 and 7. A small supply system from a

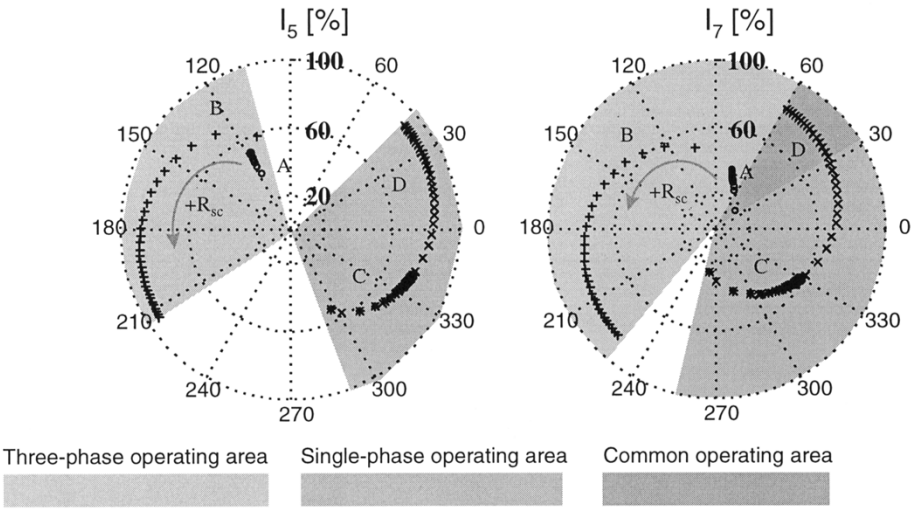


Fig. 6. Polar plots of the fifth and seventh harmonic current as a function of $R_{\rm sc}$. $R_{\rm sc} = 20$–600 with a step of 20 and $\arg Z_{\rm sc} = 80°$. o: three phase with $L_{\rm dc}(A)$; +: three phase without $L_{\rm dc}(B)$; *: one phase with $L_{\rm dc}(C)$; x: one phase without $L_{\rm dc}(D)$.

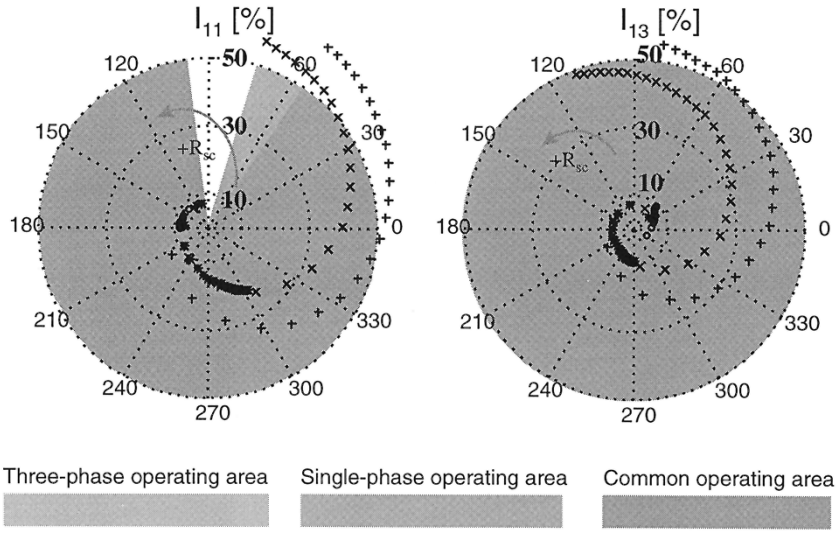


Fig. 7. Polar plots of the 11th and 13th harmonic current as a function of $R_{\rm sc}$. $R_{\rm sc} = 20$–600 with a step of 20 and $\arg Z_{\rm sc} = 80°$. o: three phase with $L_{\rm dc}(A)$; +: three phase without $L_{\rm dc}(B)$; *: one phase with $L_{\rm dc}(C)$; ×: one phase without $L_{\rm dc}(D)$.

DY5-coupled 1-MVA distribution transformer is simulated. The MV side is assumed sinusoidal and balanced. The transformer is loaded with single-phase rectifiers (the total load is 170 kW) and a 170-kW three-phase rectifier. The three-phase rectifier is located near the transformer with a 50-m 90-mm2 copper cable. The single-phase rectifier loads are evenly distributed on the three phases with a 200-m 50-mm2 copper cable. It is assumed that the single-phase rectifiers are plugged into the wall sockets and, therefore, a long cable is used for the single-phase rectifiers. Fig. 8 shows the simulated system.

The synchronous reactance of the cable is 0.07 Ω/km and the capacitive effects are ignored. The impedance of the cables are shown by their per-unit values related to the transformer. The fundamental voltage drop across the long cable is about 7% at 170-kW single-phase rectifier load. Related to the rectifier per-unit notation, the cable impedance equals 7.3% + j1.5%. The impedance of the cable is the dominant short-circuit impedance as seen from the single-phase rectifiers and some differences from the simulations in Fig. 6 are expected as the short-circuit impedances there were predominantly inductive.

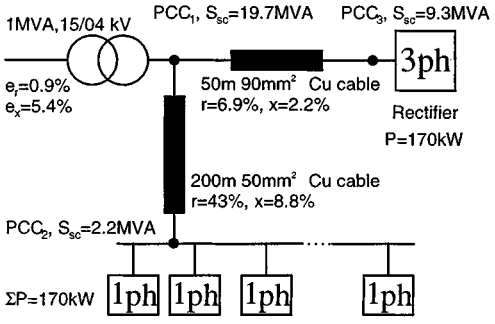


Fig. 8. Simulated system with transformer, cable, and load. The impedances of the cables are shown by their per-unit values related to the transformer.

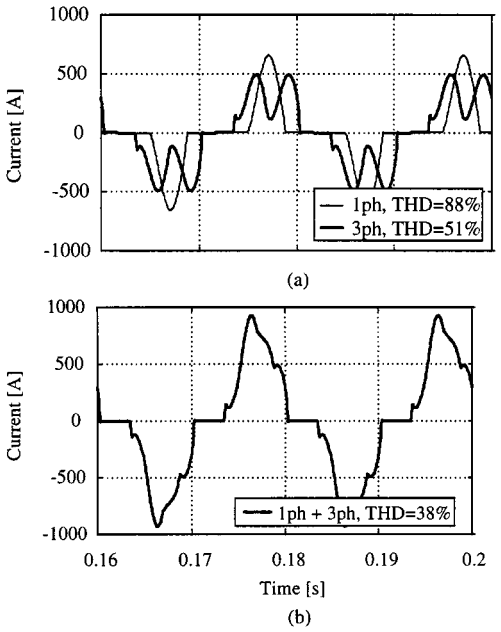


Fig. 9. Simulated currents drawn in the system. (a) Rectifier currents. (b) Total current in the secondary windings of the transformer.

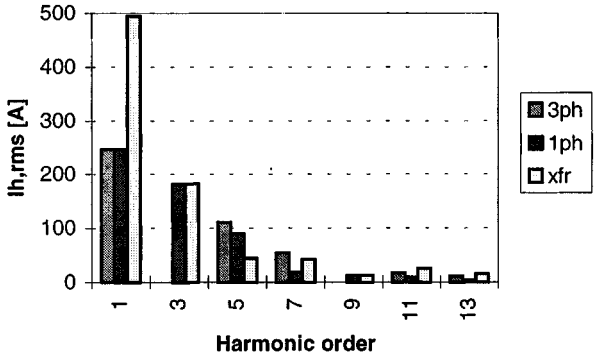


Fig. 10. Harmonic spectrum of rectifier and transformer currents.

Fig. 9(a) shows a simulation result of the currents drawn by the two rectifier groups. The currents add up in the secondary winding of the transformer, which is shown in Fig. 9(b).

Intuitively, it is seen that the two waveforms are supporting each other well. The single-phase current has a "valley-filling" effect on the three-phase current, and the resulting waveform looks more sinusoidal than each of the two individual currents.

The total harmonic distortion (THD) of the three-phase current is 51% and 88% for the single-phase. When the currents are added in the transformer, the resulting distortion is only 38%. This reduction in the distortion is mainly due to fifth harmonic cancellation, as can be seen more clearly from Fig. 10. Fig. 10 shows the harmonic spectrum of the three currents of Fig. 9.

The fundamental components of the two rectifier loads add up arithmetically in the transformer. This means that the fundamental components are in phase. The third harmonic is not present in the spectrum of the three-phase load and, therefore, the third harmonic component of the single-phase rectifier is seen directly in the transformer. The interesting part is to observe what happens with the fifth harmonic current. In this case, a 110-A current from the three-phase rectifier is seen and 90 A from the single-phase rectifier.

On the transformer, only about 45 A is seen. This is only about 20% of the arithmetical sum of the two rectifier contributions. The seventh harmonic component in the transformer equals less than 60% of the arithmetical sum. Again, the polar plots show their applications. Plotting the fifth and seventh harmonic currents in polar coordinates (see Fig. 11) shows that the fifth harmonics are almost exactly in counterphase and, thus, almost cancelling each other completely. The seventh harmonics are added with an obtuse angle, which still shows a reduction.

The phases of the fifth and seventh harmonic currents are plotted in Fig. 11 along with the traces from Fig. 6. The three-phase rectifier operates with a short-circuit ratio $R_{sc} = 55$, while the single-phase rectifiers have a short-circuit ratio (to the total power) of 10, which is a very weak grid. The resistive nature of the cable and the small short-circuit ratio gives a deviation for the single-phase rectifier, but still the angles are added within the area as defined in Fig. 6.

It can be concluded that adding a three-phase rectifier to an existing single-phase load or visa versa will not increase the current THD at the transformer, but actually lower the THD and, thereby, lower the losses in the transformer. A similar effect can be obtained on the MV line, even if the single-phase nonlinear load is fed by a different transformer than the three-phase nonlinear load. This, of course, is provided that the transformers have the same winding arrangement.

In Section II, it was stated that the harmonic background distortion is caused by a large number of single-phase nonlinear loads. The above simulations lead to the statement that the resulting voltage distortion can be reduced when connecting a three-phase diode rectifier to the utility grid due to (1).

Another simulation example is carried out to verify this statement. A small supply system from a DYn5-coupled 10/04-kV 800-kVA distribution transformer is simulated. The MV side is assumed to be distorted with the amplitude and phase angle of fifth harmonic voltage of the measured voltages in Fig. 3.

The transformer is loaded by a three-phase diode rectifier with a 3% dc inductance and varying nominal load from 0 to 650 kW. The three-phase rectifier is located near the transformer. This is shown in Fig. 12.

The impact of the rectifier load on the transformer for the fifth harmonic voltage is shown in Fig. 13.

Increasing the three-phase nonlinear load of the transformer, the resulting fifth harmonic voltage distortion will decrease. At approximately 12% of the nominal transformer power, the minimum distortion below 1% is reached. At approximately 25% rectifier load of nominal transformer power, the resulting fifth harmonic voltage distortion has reached the same level as under no-load conditions (background distortion). Above 25%, the resulting fifth harmonic voltage distortion is higher than the background fifth harmonic voltage distortion.

V. Test Results

On an MV distribution line laboratory, some measurements were made. The advantage using this laboratory is that all parameters are known and no other users are disturbing the LV and

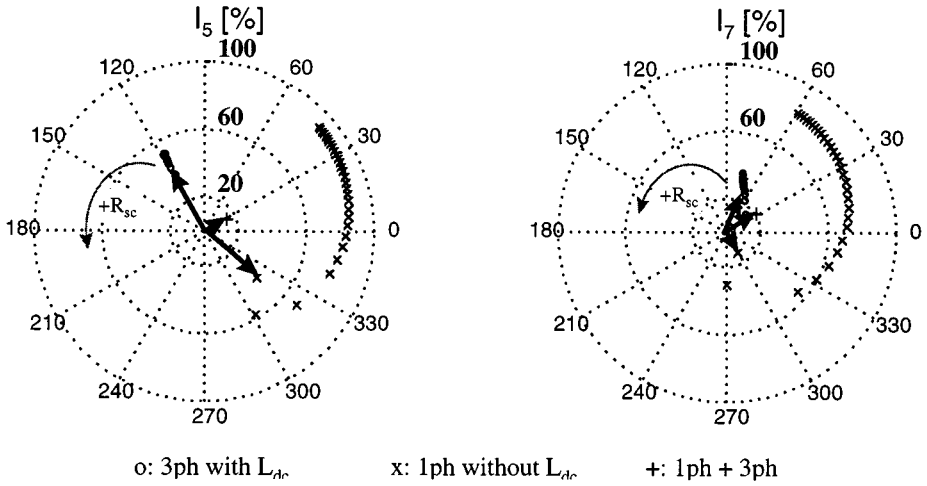


Fig. 11. Polar plots of the fifth and seventh harmonic currents of the simulations together with the traces from Fig. 6.

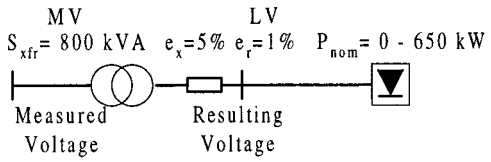


Fig. 12. Circuit diagram for simulation of rectifier influence on the resulting voltage distortion taking the voltage background distortion into account.

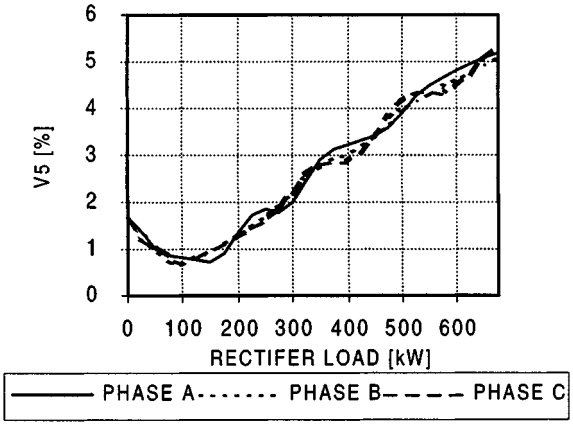


Fig. 13. The fifth harmonic voltage as a function of the rectifier load at the transformer.

MV line. The system shown in Fig. 14 is the only load on the distribution system. A three-phase ASD ($S_{nom,1} = 50$ kVA) with a 5.4% dc-link inductance and a 43% smoothing capacitor is connected to a 200-kVA transformer via a 10-m cable. The short-circuit power at the end of the cable is 3.7 MVA. A single-phase rectifier with a resistive load and no dc-link inductance is connected to phase *A*.

The currents of the three-phase, single-phase, and the sum of both currents are shown in Fig. 15(a). The harmonic currents are shown in Fig. 15(b). It is shown that fifth harmonic current is significantly reduced. The fifth harmonic current of the three-phase load is 22.5 A and the fifth harmonic current of the single-phase load is 23.5 A, while the sum only is 12.5 A. This is only

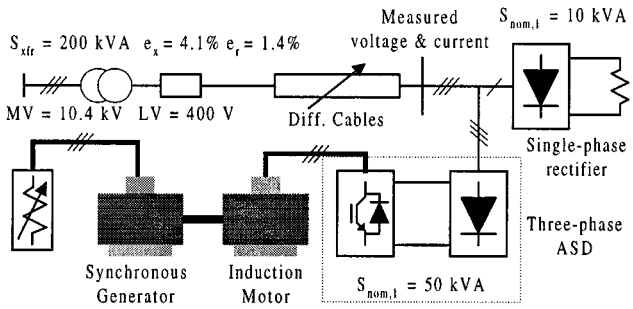
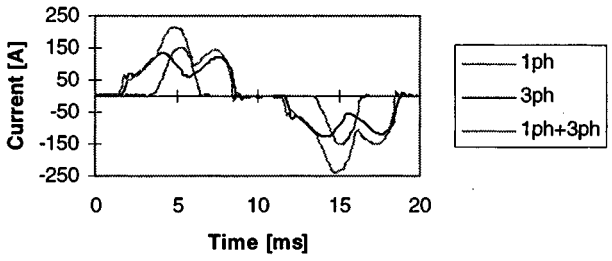
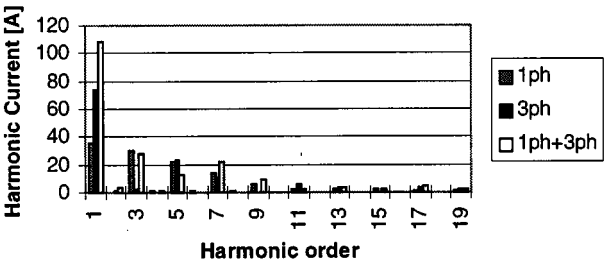


Fig. 14. Circuit diagram of the load system on the MV distribution line laboratory.



(a)



(b)

Fig. 15. (a) Measurements of the single-phase, three-phase, and the sum of both currents. (b) Harmonic spectrum of single-phase current, three-phase current, and the sum of both currents.

27% of the arithmetical sum of both rectifiers. This is in good agreement with the simulations of Figs. 9 and 10. The THD of

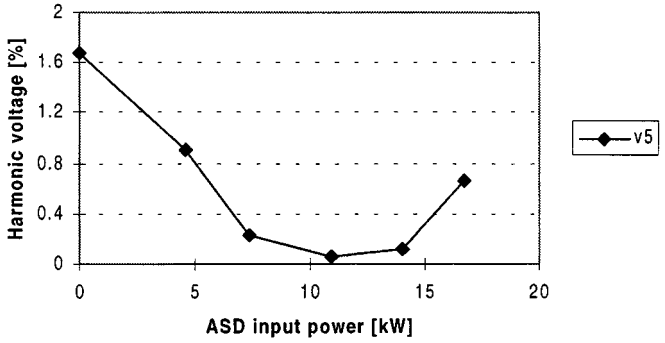


Fig. 16. Fifth harmonic voltage as a function of the drive input power.

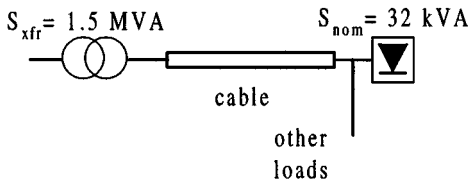


Fig. 17. Circuit diagram of the system where the measurements were done.

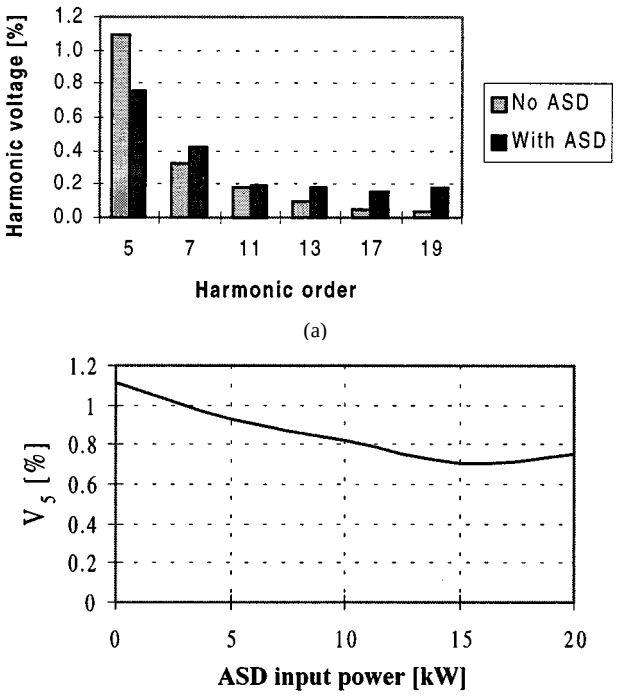


Fig. 18. (a) Measurements of the resulting voltage distortion with and without a three-phase ASD. (b) Fifth harmonic voltage as a function of the drive input power.

the sum of both currents is 36.5% compared to 113.5% of the single-phase rectifier and 37% of the three-phase rectifier.

Fig. 16 shows the fifth harmonic voltage as a function of the input power of the ASD. The load of the single-phase rectifier is fixed. At no load of the ASD, the fifth harmonic voltage is 1.7%, only generated by the single-phase rectifier. At approximately 11-kW load of the ASD, the fifth harmonic voltage has a minimum of 0.06%.

These interesting results have also been observed on site in several applications. Some measurements have been done at an office building. They have been done on a three-phase 32 –kVA ASD with a 4.3% dc-link inductance and a 28% smoothing capacitor. The ASD is connected to a 1.5-MVA transformer via a cable. The short-circuit power at the end of the cable is 5.4 MVA. A circuit diagram of the system is shown in Fig. 17. The resulting harmonic voltages are measured as a function of the drive input power.

Fig. 18(a) shows the harmonic voltages both without ASD (background voltage distortion) and with the fully loaded ASD. The fifth harmonic voltage is lower with the ASD than without. This is in good agreement with the analysis carried out in this paper. Fig. 18(b) shows the fifth harmonic voltage as a function of the drive input power. There is a good agreement with the simulated result shown in Fig. 13, where the background voltage distortion approximately has the same level.

The seventh harmonic voltage is slightly increased. The 11th remained constant and the 13th is increased. Actually, in this measurement, the voltage THD was decreased from 1.33% to 1.19% when the ASD was operating.

VI. Conclusion

This paper has shown that mixing single- and three-phase nonlinear loads gives a reduced THD. The reason is that the fifth and seventh harmonic currents of single- and three-phase nonlinear loads often are in counterphase.

Furthermore, it can be concluded that adding a three-phase rectifier to an existing single-phase load or visa versa will not increase the current THD at the transformer, but actually lower the THD and, thereby, lower the losses in the transformer. Careful system design taking these phenomena into account is a cost-effective solution to lowering the harmonic distortion.

It is clearly shown that three-phase rectifiers actually can reduce the harmonic voltage distortion. This leads to an important point: limiting the harmonic currents from three-phase nonlinear equipment does not always assure a better power (voltage) quality. Care should, therefore, be taken when setting strict limits to harmonic current emission for three-phase diode rectifiers because of their positive effect.

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Frede Blaabjerg (S'86–M'88–SM'97), for a photograph and biography, see this issue, p. 130.

An Integrated Single-Switch Approach to Improve Harmonic Performance of Standard PWM Adjustable-Speed Drives

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***Abstract*—In this paper, an integrated single-switch approach to improve harmonic performance of standard pulsewidth modulation adjustable-speed drives (ASD's) is presented. The approach is essentially an add-on solution to a standard ASD topology. The approach is based on circulating a third harmonic current to reduce the harmonics of the line current. The dynamic braking chopper available in standard ASD's is used to control the amplitude of the third harmonic circulating current. Analysis, design, and simulations are presented to determine the performance of the proposed scheme with different line impedance and with and without dc-link inductance in the ASD. Utility input current distortion well below 15% is obtained. This paper also presents how this new approach is capable of reducing the harmonic distortion in multiple drives. The paper includes experimental results using a 480-V 10-kW commercial ASD retrofitted with the proposed approach.**

***Index Terms*—Adjustable-speed drive, harmonic distortion, power quality, rectifiers, third harmonic injection.**

I. Introduction

THE expanding use of electric loads controlled by power electronics such as PC's, TV's, stereos, and adjustable-speed drives (ASD's) has made power converters an important and unquestionable part of modern society. Nevertheless, the increasing use of power converters has also led to an increase of current harmonics drawn from the utility grid.

In the last decade, major focus has been on harmonic reduction techniques and, as a result of this, several useful harmonic reduction techniques exist for the single-phase rectifier. However, finding the right solution for the three-phase rectifiers is still very difficult. This seems to be true especially for industrial ASD's where the price and reliability have the highest priorities. Even though there exist many proposals for the three-phase rectifier, many of the existing solutions may not be qualified for a grade-purpose ASD. The solution is either only practical for low-power applications or the price and complexity are too high. Some summaries on three-phase harmonic reduction techniques can be found in [1]–[5].

So far, most customers of ASD's use the low-cost diode rectifier and accept the harmonic currents. Harmonic reduction equipment such as an active filter or active rectifier is only used when there are severe problems with harmonic distortion. Due to the new standards, such as IEEE 519-1992 and EN 61000-3-2/EN 61000-3-12, a more general solution is desired for the ASD.

Some requirements for the three-phase rectifier used for ASD's are as follows.

- The harmonic distortion of the input current should be as low as possible. However, a unity power factor is not necessary.
- There should be no increased dc-link voltage, because higher dc-link voltage warrants redesign of the pulsewidth modulation (PWM) inverter.
- The operation of the rectifier should be independent of the line impedance.
- No additional components in series with the power flow path should be used, due to increased losses.
- Bidirectional power flow is normally not necessary.
- In general, an electrical isolation between the utility input and the output of the power electronic converter is not needed.
- The cost, power losses, and size compared to the diode rectifier should be as small as possible.

Note that the only requirement limiting the use of the diode rectifier is the first requirement in the list above.

The third harmonic injection scheme for the three-phase diode rectifier for reducing the harmonic currents has shown some promising results and has been presented among others in [6]–[10].

However, these approaches suffer from some disadvantages.

- The schemes in [6] and [7] need a line-synchronized controllable external third harmonic current source.
- These schemes also need an input transformer with access to the neutral terminal for circulating the third harmonic current.
- The schemes in [9] and [10] have two diodes in series with the power flow path which increases the losses.

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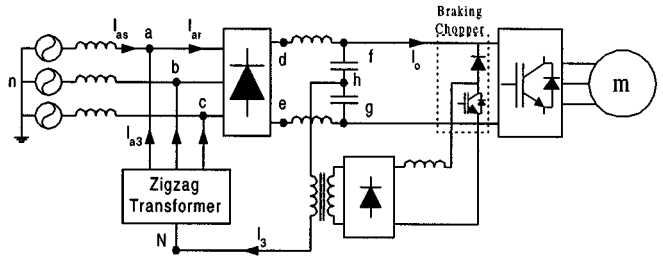

Fig. 1. Proposed integrated single-switch approach to improve harmonic performance of standard adjustable-speed drives.

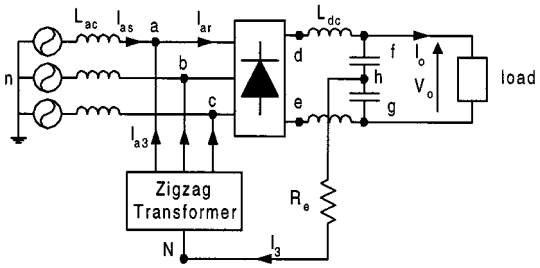

Fig. 2. Simplified diagram of the proposed scheme showing the basic idea.

- These schemes also have a high dc-link voltage due to the boost operation and, therefore, increase the losses of the PWM inverter.

The scheme presented in [8], compared to [9] and [10], exhibits the following advantages.

- There are no additional components in series with the power flow path.
- The dc-link voltage is the same as for the diode rectifier.
- The third harmonic circulating current is automatically generated.

However, the scheme in [8] is most suitable for a rectifier with a high dc-link inductance and small dc-link capacitors (e.g., dc motor drives). Furthermore, the circulating third harmonic current is uncontrolled and the optimum total harmonic distortion (THD) is valid only at one operating point.

In this paper, an extension of the scheme in [8] is presented, where the principal of operation basically is the same as in [8]. However, by employing an integrated single-switch boost converter in the scheme, it becomes suitable for improving the harmonic performance of a standard PWM-ASD. The new aspects of this paper are: 1) analysis of the modified scheme of [8] applied to a standard PWM-ASD and 2) effective control of the circulating current. Furthermore, in Section IV, it is shown how the proposed approach is capable of reducing the line-side harmonic currents of multiple ASD's.

The paper includes a detailed design procedure along with component ratings. Detailed simulation and experimental results are also shown.

II. Proposed Topology

Fig. 1 shows the circuit topology of the proposed scheme. In this paper, a zigzag transformer is employed to create a neutral "*N*." Further, a single-phase transformer is connected between "*N*" and the dc-link mid-point "*h*." On the secondary side of the single-phase transformer a single-phase boost power-factor-correction circuit is implemented as shown in Fig. 1. Since the voltage between "*N*" and "*h*" is predominantly 180 Hz (third harmonic), the single-phase boost converter action results in thirrd harmonic injected current I_3 and drastically improves the utility power quality performance of the ASD. It should be noted that the dc-link capacitor midpoint and a dynamic braking chopper (insulated gate bipolar transistor (IGBT) and diode) exist in most standard ASD's.

The advantages of the proposed scheme (Fig. 1) are the following.

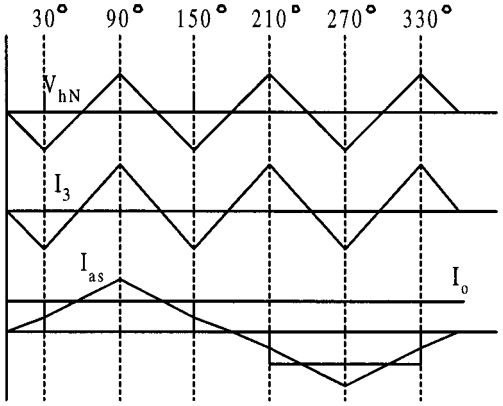

Fig. 3. The voltage V_{hN} between the dc-link midpoint "h" and the neutral "N". The current I_3 is in phase and shape with the voltage. The line current I_{as} can be reconstructed as a function of the dc-link output current I_o and the circulating third harmonic current I_3.

- No additional components in the power flow path are needed.
- The dc-link voltage has the same level as with a diode rectifier.
- The operation of the new scheme is independent of the line impedance.
- The approach is an add-on solution. (Once the ASD is modified for the presented scheme, the ASD can easily be sold with the proposal if required.)
- It has high reliability because the diode rectifier still works even when the boost rectifier is down.
- Using the diode and the IGBT of the dynamic braking circuit, low cost can be achieved.
- Multiple drive connection is possible.

III. Principle of Harmonic Reduction with the Proposed Scheme

For description of the proposed scheme, the simplified diagram of Fig. 2 is used, since the boost converter behaves like a variable resistor.

As shown in Fig. 3 the shape of the voltage V_{hN} between the dc-link midpoint 'h' and the neutral of the zigzag transformer "N" is triangular in nature due to the 120° conduction mode of the six-pulse diode rectifier. Interconnection between point "h" and point "N" via a resistor R_e results in a circulating current I_3, in shape and phase with the voltage V_{hN}. This circulating current is essentially a third harmonic current and is injected into the three phases "a," "b," and "c" via a zigzag transformer.

In each phase, a third of the circulating current is injected. Depending of the conduction mode of the six-pulse diode rectifier, three different modes are considered for each phase. For phase "a," these three modes are described below.

Mode 1: Phase "a" is not conducting. In this case, a third of the circulating current I_3 is injected into the source. The source current of phase "a", I_{as}, equals

$$I_{as} = -\frac{I_3}{3}. \tag{1}$$

Mode 2: This is the positive conduction mode. The upper diode of phase "a" in the six-pulse diode rectifier is conducting. Half of the circulating current is flowing into the rectifier via phase "a." The other half is flowing into the rectifier via the lower diode of phase "b" or "c." The upper diode of phase "a" is also conducting the load current into the rectifier. Therefore, the source current of phase "a," I_{as}, equals

$$I_{as} = I_o + \frac{I_3}{2} - \frac{I_3}{3} = I_o + \frac{I_3}{6}. \tag{2}$$

Mode 3: This is the negative conduction mode. The lower diode of phase "a" in the six-pulse diode rectifier is conducting. Half of the circulating current is flowing into the rectifier via phase "a." The other half is flowing into the rectifier via the upper diode of phase "b" or "c." The lower diode of phase "a" is also conducting the load current back to the source. Therefore, the source current of phase "a", I_{as}, equals

$$I_{as} = -I_o + \frac{I_3}{2} - \frac{I_3}{3} = -I_o + \frac{I_3}{6}. \tag{3}$$

The source current can now be reconstructed as shown in Fig. 3. A detailed description of the principles of the third harmonic injection scheme can be found in [8].

In a standard PWM-ASD, the harmonic content of the input current depends both on the dc-link inductance and the ac-line reactance. However, the input current seldom has a square-wave form as assumed in the description above. In some cases, the input current can be discontinuous. Therefore, finding the optimal amplitude of the circulating current that results in the lowest current THD in an analytical way is quite cumbersome. In this paper, the SABER simulator is used for the analysis part. The analysis is based on per-unit quantities with the following definitions:

$$\begin{aligned}
\text{input line–line voltage } V_{ab} &= 1 \text{ per unit} \\
\text{output power } P_o &= 1 \text{ per unit} \\
\text{rectifier output dc voltage } V_o &= 1.35 \text{ per unit} \\
\text{output dc current } I_o &= P_o/V_o = 0.7407 \text{ per unit} \\
\text{base impedance } Z_b &= V_{ab}^2/P_o = 1 \text{ per unit.}
\end{aligned}$$

The scheme of Fig. 2 is implemented in SABER. The capacitor banks in the dc link equal 10.5% (percentage of the base impedance as defined above). The simulations are done with and without a 2.6% dc-link inductance. The frequency is 60 Hz and the ac impedance is varied, i.e., the short-circuit ratio R_{sc} is varied from 20 to 500. The short-circuit ratio is defined as the ratio between the short-circuit power S_{sc} at the point of connection and the fundamental input power of the ASD S_1. After a total of 90 simulations to analyze the input current THD, the results are shown in Figs. 4 and 5.

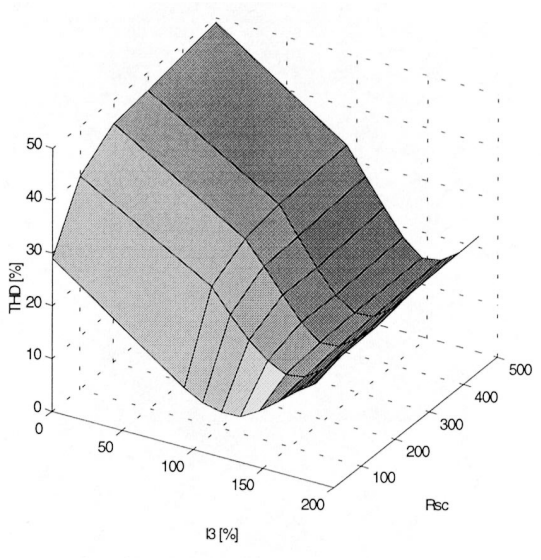

Fig. 4. Current THD of the input power as a function of the circulating current in percentage of the output current and the short-circuit power. The dc-link inductance of the six-pulse diode rectifier equals 2.6%.

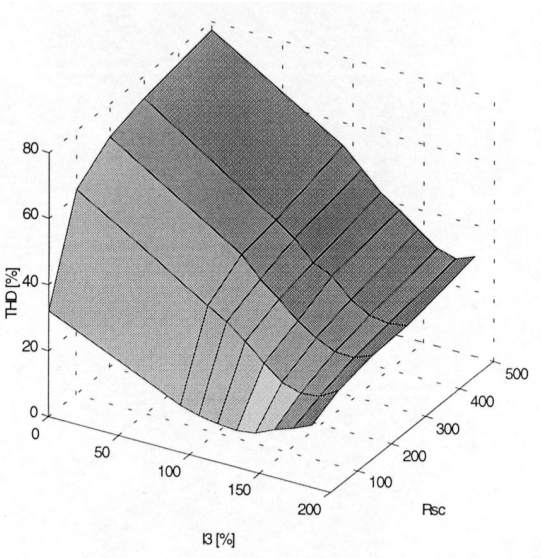

Fig. 5. Current THD of the input power as a function of the circulating current in percentage of the output current and the short-circuit power. There is no dc-link inductance in the six-pulse diode rectifier.

It can be seen from Fig. 4 that using a dc-link inductance of 2.6% and a circulating current (I_3) of approximately 150% of the output current (I_o) results in an input current THD of less than 15% and it is independent of the line reactance. On a weak utility grid ($R_{\text{sc}} = 20$), a circulating current of 120% gives a minimum THD of 9%. Fig. 5 shows that the circulating current has to be somewhat higher (180%) when no dc-link inductance is used. Only at a weak grid ($R_{\text{sc}} = 20$) can an input current THD of 15% be achieved. Here, the circulating current (I_3) has only to be 140% of the output current (I_o).

The power dissipated in the resistor equals the circulating current times the voltage V_{hN}. The voltage V_{hN} and the current I_3 can be presented as [8]

$$V_{hN} = V_{ab}\,\frac{-3\sqrt{2}}{8\pi}\,\sin(3\omega t)$$
$$I_3 = -\hat{I}_3\,\sin(3\omega t) \tag{4}$$

where ω is the angular frequency of the fundamental voltage of utility grid.

The instantaneous power losses in the resistor R_e can be calculated as

$$P_{3,\text{inst}} = V_{ab}\hat{I}_3\,\frac{3\sqrt{2}}{16\pi}\,(1-\cos(6\omega t)). \tag{5}$$

It should be noted that, by employing the boost converter to emulate the variable resistor R_e (Fig. 2), the only power losses are the switching and conduction losses in the converter.

IV. Performance of the Proposed Scheme

For galvanic isolation of the boost converter, a single-phase transformer is required. The output of the boost converter is connected to the dc-link capacitor bank of the ASD and, therefore, the boost converter needs no outer voltage loop control. For integration of the boost converter in the ASD, the diode and the IGBT of the braking chopper circuit of the standard ASD is used.

To evaluate the proposed scheme, some simulations are made using the SABER simulator. The simulated system consists of a 10-kW three-phase rectifier, 480-V line-to-line voltage, and the frequency is 60 Hz. The utility grid is modeled by some line inductance. The base impedance of the rectifier equals $Z_b = 23.04\ \Omega$ (calculated as defined in Section II). The total capacitance of the dc-link capacitor banks equals 10.5% of the base impedance. The transformers are ideal with no leakage inductance and a high magnetizing inductance. The transformer ratio of the single-phase transformer is 1:4. The switching frequency of the boost converter is about 8 kHz. The short-circuit ratio R_{sc} is varied from 20 to 500. Again, simulations are made with and without a 2.6% dc-link inductance.

A. With DC-Link Inductance

As expected, varying the ac-line impedance and thereby the short-circuit ratio has shown that there is small difference in the behavior of the proposed system between a weak and a strong utility grid. The current and the Fourier spectrum of the current are shown in Figs. 6 and 7.

The THD of the current is 9% with a short-circuit ratio of 20, while the THD is 13% with a short-circuit ratio of 500. The amplitude of the circulating current on the primary side of the single-phase transformer is 17.7 A (rms). The output current I_o equals 15 A.

B. Without DC-Link Inductance

As expected, without the dc-link inductance the harmonic distortion of the input current is increased at a high short-circuit ratio. This is shown in Fig. 8. The THD of the current is 23.6%,

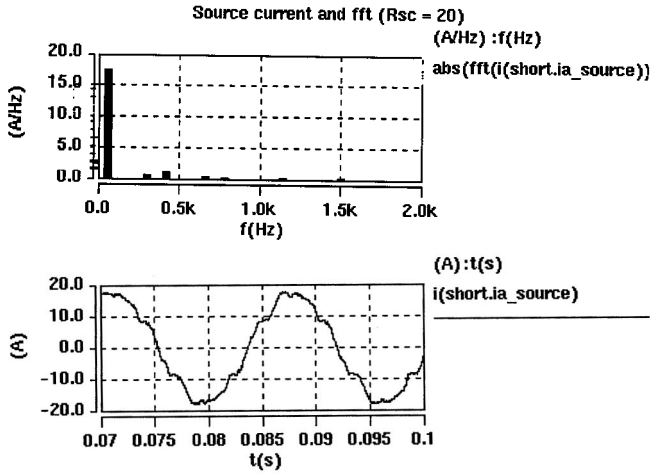

Fig. 6. Line current and the Fourier spectrum. The short-circuit ratio $R_{\text{sc}} = 20$ and the THD of the line current is 9%.

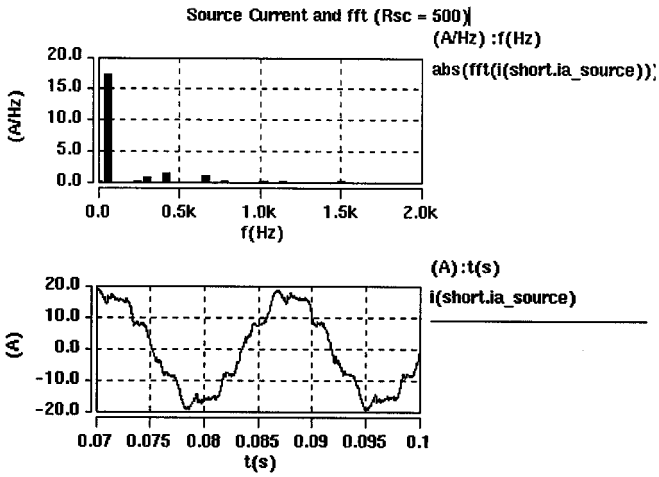

Fig. 7. Line current and the Fourier spectrum. The short-circuit ratio $R_{\text{sc}} = 500$ and the THD of the line current is 13%.

while the short-circuit ratio equals 500. The amplitude of the circulating current on the primary side of the single-phase transformer is 21.1 A (rms). The output current I_o equals 15 A.

In a system with a weak utility grid, the performance of the proposed solution is almost as good as with the dc-link inductance. This is shown in Fig. 9. The THD of the current is 10% with a short-circuit ratio of 20. The amplitude of the circulating current on the primary side of the single-phase transformer is the same as that with dc-link inductance, 17.7 A (rms). The output current I_o equals 15 A.

C. Adaptation of the Proposed Scheme for Multiple Drives

Interconnection of multiple drives is also possible. Two 10-kW ASD's are connected in parallel as shown in Fig. 10. By interconnection of the dc link, it is assured that both diode rectifiers are equally loaded, even when one of the ASD's is braking. For preventing load oscillations, the connection has to be made on the line side of the dc-link inductance. The midpoints of the dc-link capacitors in the ASD's are connected

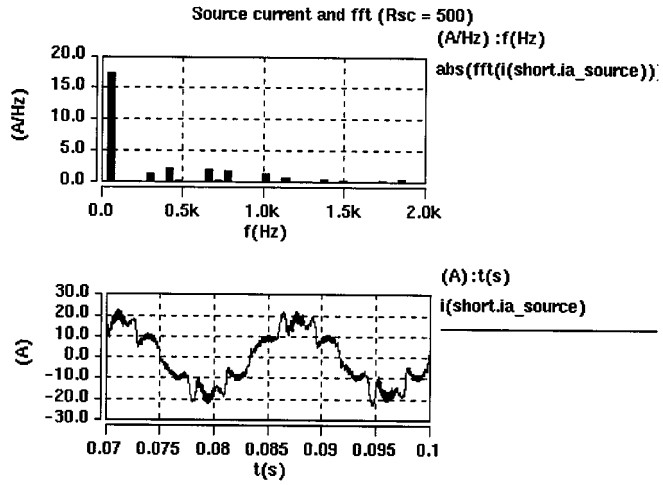

Fig. 8. Line current and the Fourier spectrum. The short-circuit ratio $R_{\rm sc} = 500$ and the THD of the line current is 23.6%.

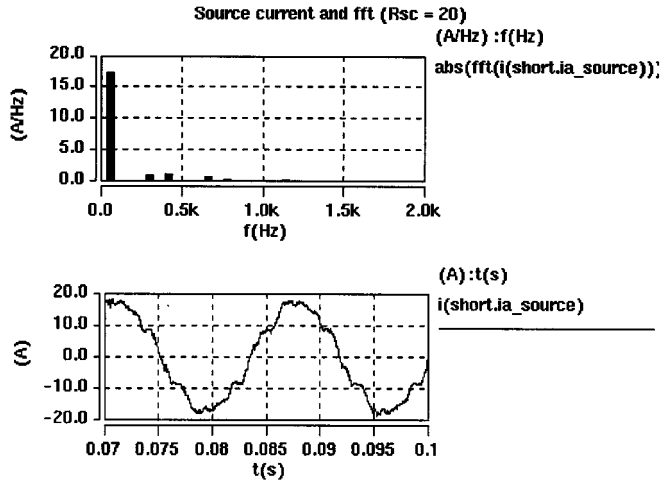

Fig. 9. Lline current and the Fourier spectrum. The short-circuit ratio $R_{\rm sc} = 20$ and the THD of the line current is 10%.

together to ensure that the circulating current is divided equally between both rectifiers.

Fig. 11 shows the result when both drives are operating under full-load condition. The simulations are made with a short-circuit ratio $R_{\rm sc} = 100$. Fig. 12 shows the result when one of the drives operates at half load and the other drive operates at full load. It is shown that the differences in the loads of both drives do not influence the harmonic performance of the proposed scheme. The current THD equals 11.6% and 12.5%, respectively.

D. Discussion of the Simulated Results

It is demonstrated that, for a low short-circuit ratio, a single-digit current THD can be achieved, and when series inductance (either dc or ac inductance) is used, as in the case with the dc-link inductance, a THD well below 15% can be achieved, even for a (very) high short-circuit ratio. Only in the case of no series inductance and a high short-circuit ratio is the result not satisfying. Also, the circulating current becomes somewhat

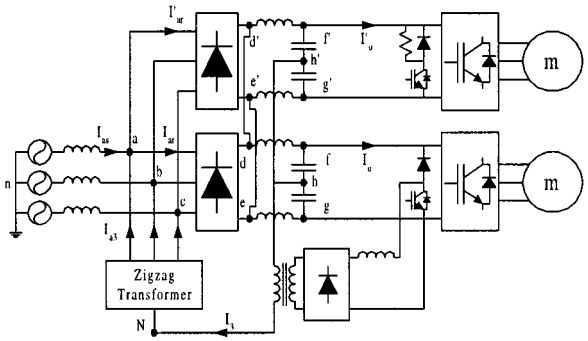

Fig. 10. Interconnection of two ASD's. One uses the dynamic braking chopper for the proposed scheme, while the other uses the dynamic braking chopper for braking resistor.

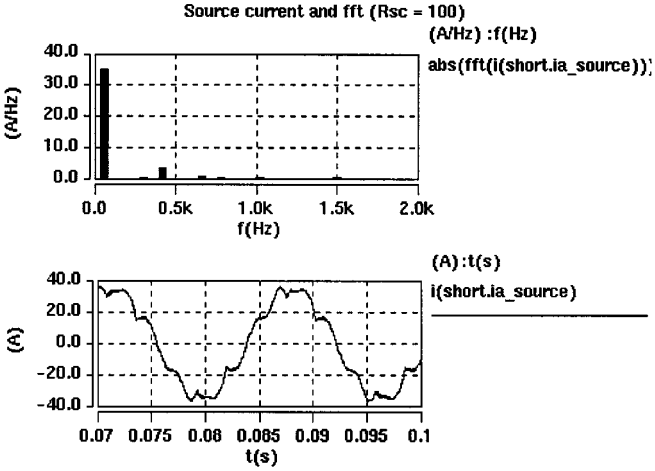

Fig. 11. Line current and the Fourier spectrum with interconnection of two ASD's. The THD of the line current is 11.6%. Both ASD's operate at full load.

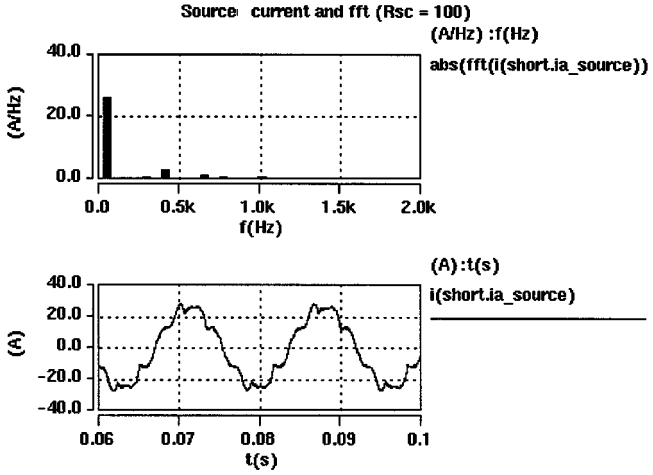

Fig. 12. Line current and the Fourier spectrum with interconnection of two ASD's. The THD of the line current is 12.5%. One ASD operates at full load while the other operates at half load.

higher in this case. To fulfill the demands of independent operation of the line impedance, stated in Section I, one should use an additional inductance. Either an ac inductance or, as presented in this paper, a split dc-link inductance can be used. However,

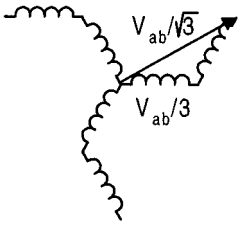

Fig. 13. Voltage across the windings on a zigzag transformer.

the interconnection of multiple drives should only be done when dc-link inductances are used to prevent load oscillations.

V. Design Example

In this section, the design of the zigzag transformer, the single-phase transformer, and the boost converter are presented in per-unit quantities.

Ratings of various components are calculated based on a rectifier using a dc-link inductance, hence, $I_3 = 1.20 * I_o$.

A. Zigzag Transformer Voltampere Rating

The voltage across the zigzag transformer is illustrated in Fig. 13. The voltage on the primary (and secondary) winding V_{wd} of the transformer is

$$V_{wd} = \frac{V_{an}}{\sqrt{3}} = \frac{V_{ab}}{3}. \quad (6)$$

The current in the phase windings (I_{a3}) is $1.2 * I_o/3$. Thus, the voltampere rating of the transformer is

$$VA_{\text{zigzag}} = 3\,\frac{V_{ab}}{3}\,\frac{1.2 \cdot I_o}{3} = \frac{1.2 \cdot I_o \cdot V_{ab}}{3} = 0.296 \text{ pu}. \quad (7)$$

B. Single-Phase Transformer and Boost Converter Voltampere Rating

The transformer ratio of the single-phase transformer should be chosen with care. Since no outer voltage control loop is necessary, the output of the boost rectifier is connected directly to the capacitor banks of the ASD. In a boost converter, the dc-link voltage must always be somewhat higher than the amplitude of the input voltage. In [8], it is shown that V_{hN} basically is given by $V_{hN} = 0.169 V_{ab}$. Since the output voltage is $1.35 V_{ab}$ and a boost factor of 1.5 is normal for a boost converter, the transformer ratio "k" can be calculated as

$$k = \frac{1.35 \cdot V_{ab}}{1.5 \cdot 0.169 \cdot \sqrt{2} \cdot V_{ab}} = 3.77. \quad (8)$$

The voltampere rating of the single-phase transformer is then given by

$$VA_{\text{single-phase}} = 0.169 \cdot V_{ab} \cdot 1.2 \cdot I_o = 0.15 \text{ pu}. \quad (9)$$

The single-phase transformer has to be designed to operate at a frequency of three times the fundamental line frequency. The voltampere rating of the boost converter is the same as the voltampere rating of the single-phase transformer.

VI. Experimental Results

An experimental setup is built in the Power Quality and Power Electronics Laboratory, Texas A&M University, College Station. The rectifier of a 480-V 10-kW commercial ASD is used to be retrofitted with the proposed approach.

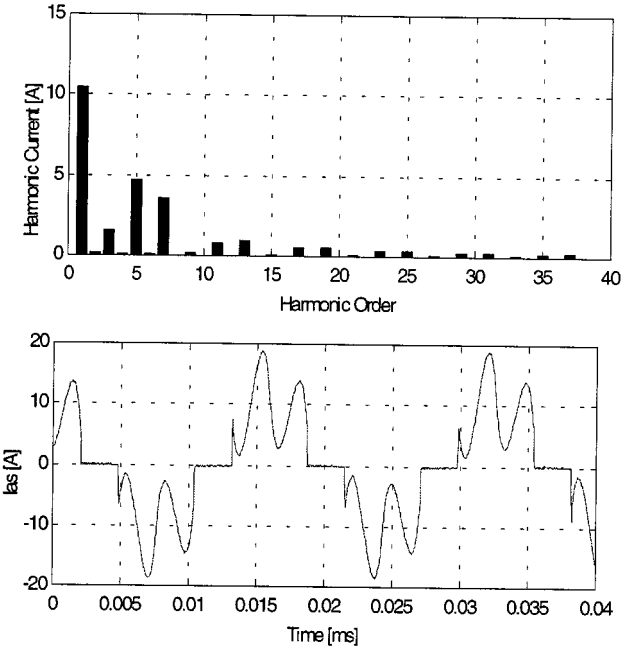

Fig. 14. Fourier spectrum and a time plot of the line current without use of the proposed scheme. Current THD = 60%. Load is approximately 5.8 kW.

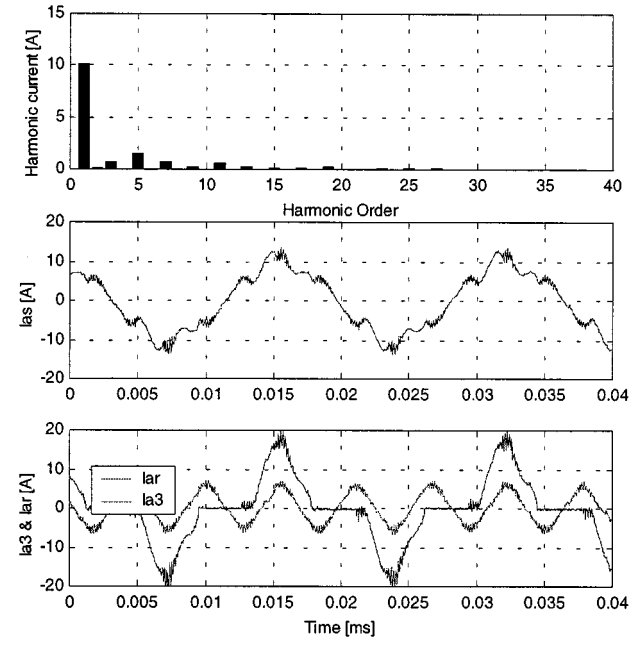

Fig. 15. Fourier spectrum and a time plot of the line current with the use of the proposed scheme. Current THD = 19%. Load is approximately 5.8 kW. Lower plot shows the third harmonic current of one transformer phase as well as the phase current in the diode rectifier itself.

The value of the dc-link inductance is 1.6 mH (2.6%) and the value of the two dc-link capacitors is 2.2 mF (total 10.5%). The rectifier is connected close to a 480-V 60-Hz 75-kVA transformer with 6% short-circuit impedance. Therefore, the short-circuit ratio is approximately 125. The rectifier is loaded with a 77-Ω power resistor; this equals approximately 5.5 kW.

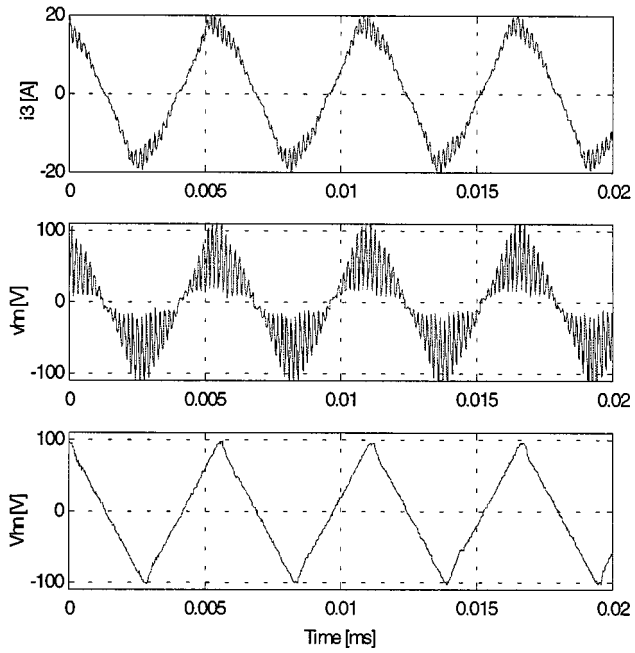

Fig. 16. Current and voltage of the primary side of the single-phase transformer. Lower plot shows the voltage V_{hN} when the converter is not switching.

The boost converter is of the continues conduction mode (CCM) type. The control is performed by two integrated circuits (current controller and multiplier). The reference to the current controller is given by multiplying the rectified voltage V_{hN} and an rms current reference. The rms current reference is in this setup given manually. The switching frequency is about 6 kHz.

Fig. 14 shows the line current and the Fourier spectrum without the proposed approach. The power is about 5.8 kW. The current THD equals 60%. Also, a small amount of a third harmonic current can be seen, which indicates some degree of unbalance on the utility grid.

Fig. 15 shows the line current and the Fourier spectrum with the proposed approach. The current THD equals 19%. It is clearly shown that the amount of the fifth and seventh harmonic current is significantly reduced. The lower plot of Fig. 15 shows the phase current of the zigzag transformer I_{a3} and the current of the rectifier I_{ar}. It should be noted that the peak current of the rectifier is not higher with the new proposed approach than without, so no derating of the diodes is necessary.

Fig. 16 shows the current and the voltage on the primary side of the single-phase transformer V_{hN}. The lower plot of Fig. 16 shows the voltage while the converter is not switching. It can be seen that the current I_3 is in shape and phase with the voltage V_{hN}.

VII. Conclusion

In this paper, an integrated single-switch approach to improve harmonic performance of standard PWM-ASD's has been presented. The approach is essentially an add-on solution to standard ASD's. The proposed scheme has shown that significant reduction of ASD-generated harmonics is possible with the proposed approach. The advantages compared to other solutions, such as no extra components (extra losses) in series with the power flow and independence of the line impedance, makes this approach a potential solution for ASD's.

Also, advanced programming of the current reference has not been considered so far, but it is likely that applying a more intelligent current control than used in this paper can reduce the harmonic current distortion further. Future work on this scheme should, therefore, consider this possibility.

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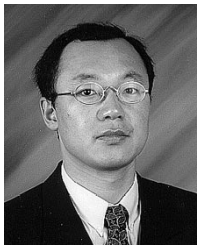

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Sensorless Control strategies for PWM Rectifier

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***Abstract* – In this paper two different control strategies for PWM Rectifier without line voltage sensors are compared. The Direct Power Control (DPC) which has no need for line voltage measurements is compared to the conventional Voltage Oriented Control (VOC) strategy in rotating coordinates with a novel line voltage estimator. The steady-state performance of both strategies is compared with regards to voltage unbalance and pre-distorted grid. Furthermore, the use of discontinuous modulation is motivated in the classical control strategy and is analyzed along with the novel line voltage estimator. It is shown that the VOC strategy with line voltage estimator exhibits several advantages compared to DPC. Some simulations and experimental results verifying the comparison are presented.**

I. INTRODUCTION

Thanks to well known capabilities such as: power regeneration, low harmonic input current distortion and controlled dc-link voltage, PWM rectifiers are often used in high performance adjustable speed drives (ASD's) where frequent acceleration and de-acceleration is required. New standards appear such as IEEE 519-1992 and IEC 61000-3-2 / IEC 61000-3-4 which intend to limit the harmonic current of power electronic converters. Therefore, the PWM rectifier is believed to replace the diode rectifier also in medium performance applications in the future.

However, reducing the cost of the PWM rectifier is vital for the competitiveness compared to other front-end rectifiers. The cost of power switching devices (e.g. IGBT) and digital signal processors (DSP's) are generally decreasing and further reduction can be obtained by reducing the number of sensors. Sensorless control exhibits also advantages such as improved reliability and lower installation costs.

The basic control of the PWM rectifier is easiest explained by Fig. 1. The line current vector i_s is controlled by the voltage drop across an inductance L interconnecting the two voltage sources (grid and rectifier). The inductance voltage U_L equals the difference between the line voltage U_s and the converter voltage U_{conv}.

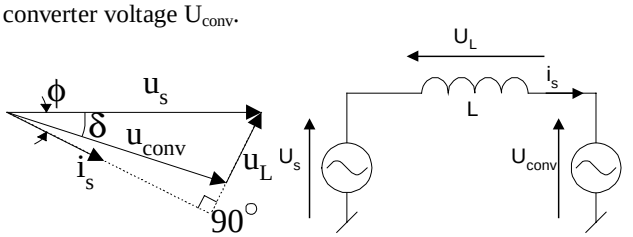

Fig. 1. General vector diagram for the PWM rectifier.

It is clear that some sensors must be used for proper control of the line current vector i_s. Normally the PWM rectifier needs three kinds of sensors:

- dc-voltage sensor
- ac-line current sensors
- ac-line voltage sensors

The dc-voltage and the ac-line current sensors are an important part of the over-voltage and over-current protection, while it is possible to replace the ac-line voltage sensors with a line voltage estimator.

An important feature for a voltage estimator is to estimate the voltage correct also under unbalanced conditions and pre-existing harmonic voltage distortion. Not only the fundamental component should be estimated correct, but also the harmonic components and the voltage unbalance has to be estimated exactly. This is an important point, so it is possible to either compensate for this error [1], [2] and obtain sinusoidal line currents or to let the current follow the voltage with the advantage of a higher total power factor [4].

One of the most popular strategies is a conventional line Voltage Oriented Control (VOC) [1] - [3] in rotating coordinates with line voltage measurements. Recently, a Direct Power Control (DPC) method [4] has gained some attention. The scheme presented in [4] has the advantage that no line voltage measurements are required.

This paper presents an analysis of the steady-state performance for the DPC and the conventional VOC method along with a novel ac-line voltage estimator with regards to pre-existing harmonic voltage and voltage unbalance. Also the use of discontinuous modulation (DPWM) [9] is motivated and is implemented for the conventional VOC without voltage sensors. Some simulations are made in the SABER simulator and experimental results verifies the simulations.

II. CONTROL STRATEGIES

In this section a short introduction of the DPC and the conventional VOC strategy is given. Also the line voltage estimators are described. The properties of both methods are summarized in Table I.

A. Direct Power Control (DPC)

The main idea of DPC is proposed by [4] and it is similar to the well known Direct Torque Control (DTC) for induction

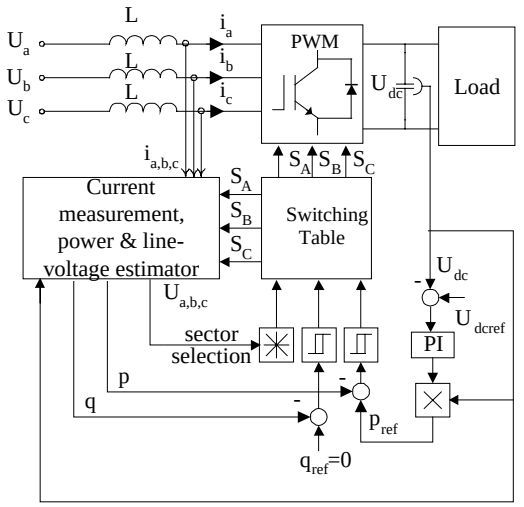

Fig. 2. Control structure of the DPC in a PWM rectifier.

motors. Instead of controlling torque and stator flux the instantaneous active and reactive power are controlled. A diagram of the control structure for DPC is shown in Fig.2.

The instantaneous values of active (p) and reactive power (q) are estimated by equations (1) and (2):

$$p = L\left(\frac{di_a}{dt}i_a + \frac{di_b}{dt}i_b + \frac{di_c}{dt}i_c\right) + U_{dc}\left(S_A i_a + S_B i_b + S_C i_c\right) \quad (1)$$

$$q = \frac{1}{\sqrt{3}}\{3L\left(\frac{di_a}{dt}i_c - \frac{di_c}{dt}i_a\right) - U_{dc}[S_A(i_b - i_c) + S_B(i_c - i_a) + S_C(i_a - i_b)]\} \quad (2)$$

where:
S_A, S_B & S_C are the switching states of the PWM rectifier.
i_a, i_b & i_c are the measured line currents.
L is the inductance between the grid and the PWM rectifier.

The estimated values of p and q are compared with the reference values. The active power reference (p_{ref}) is set by the dc-link voltage controller while the reactive power reference is set to zero for unity power factor. The switching states are then directly controlled by two hysteresis controllers and by an optimal switching table which can be found in [4]. This very simple solution allows precisely control of instantaneous active and reactive power and errors are only limited by the hysteresis band. No transformation into rotating coordinates is needed and the equations are easy implemented.

The ac-line voltage sector is needed as an input for the switching table, therefore knowledge of the line voltage is essential. However, once the estimated values of active and reactive power are calculated and the ac-line currents are known, the line voltage can easily be calculated as shown in equation (3).

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \frac{1}{i_\alpha^2 + i_\beta^2}\begin{bmatrix} i_\alpha & -i_\beta \\ i_\beta & i_\alpha \end{bmatrix}\begin{bmatrix} p \\ q \end{bmatrix} \quad (3)$$

where:

u_α, u_β are the estimated values of the three-phase voltages u_a, u_b and u_c in the fixed α-β reference frame (See also Fig. 3.).
i_α, i_β are the measured three-phase currents i_a, i_b and i_c in the fixed α-β reference frame (See also Fig. 3.).

B. Conventional Sensorless Voltage Oriented Control (VOC)

In the conventional VOC space vectors in the rotating d-q coordinates are used as shown in Fig. 3.

By placing the d-axis of the rotating coordinates on the line voltage vector a simplified dynamic model can be obtained. The equations for the grid and the converter are in the rotating dq-coordinates expressed as:

$$u_{d,s} = R \cdot i_d + L\frac{di_d}{dt} + u_{d,conv} - \omega_s \cdot L \cdot i_q \quad (4)$$

$$u_{q,s} = 0 = R \cdot i_q + L\frac{di_q}{dt} + u_{q,conv} + \omega_s \cdot L \cdot i_d \quad (5)$$

The voltage $u_{q,s}$ equals zero per definition and for unity power factor the current i_q is controlled to zero while the reference for the current i_d is set by the dc-link voltage controller.

The advantage of the rotating d-q coordinates is that the controlled quantities such as voltages and currents become dc-values. This simplifies the expressions for control purpose and low sampling frequency can be used to control these quantities with a simple PI-controller. However, the disadvantage is that for a exact decoupling of the d- and q-axis the knowledge of θ is essential. Normally, the line voltages are measured for calculation of θ.

In order to reduce the costs a line voltage estimator is used. It is possible to calculate the voltage across the inductance by differentiating the current flow through it. The line voltage can then be estimated by adding the rectifier voltage reference to the calculated voltage drop across the inductor. However, this approach has the disadvantage that the current is differentiated and noise in the current signal is gained through the differentiation. To avoid this a novel voltage estimator based on the power estimator of [4] is presented.

In [4] the current is sampled and the power is estimated several times in every switching state. This is not desired in the VOC because the currents i_d and i_q can be controlled with a fairly low sampling frequency (2 - 10 kHz).

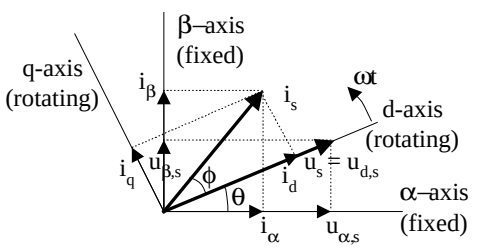

Fig. 3. Coordinate transformation of line voltage and current from fixed a-b coordinates to rotating d-q coordinates.

In traditional space vector modulation (SVM) for three-phase voltage source inverters the currents are sampled in the zero-vector states because no switching noise is present and a filter in the current feedback for the current control loops can be avoided [7] [8]. Using equation (1) and (2) the estimated power in this special case can be expressed as:

$$p = L\left(\frac{di_a}{dt}i_a + \frac{di_b}{dt}i_b + \frac{di_c}{dt}i_c\right)$$
$$q = \frac{3L}{\sqrt{3}}\left(\frac{di_a}{dt}i_c - \frac{di_c}{dt}i_a\right) \quad (6)$$

Note, in this special case only the active and reactive power in the inductor can be estimated.

Since p and q are dc-values, it is possible to prevent that noise of the differentiated current has influence on the estimated active and reactive power by the use of a simple (digital) low-pass filter. This ensures a robust and noise insensitive performance of the voltage estimator.

The estimated voltages across the inductance L equal:

$$\begin{bmatrix} u_{L\alpha} \\ u_{L\beta} \end{bmatrix} = \frac{1}{i_\alpha^2 + i_\beta^2}\begin{bmatrix} i_\alpha & -i_\beta \\ i_\beta & i_\alpha \end{bmatrix}\begin{bmatrix} p \\ q \end{bmatrix} \quad (7)$$

where:

$u_{L\alpha}$, $u_{L\beta}$ are the estimated values of the three-phase voltages across the inductance L in the fixed α-β coordinates.

The estimated line voltage u_{est} can now be calculated by adding the voltage reference of the PWM rectifier to the estimated inductor voltage.

$$\vec{u}_{est} = \vec{u}_{conv} + \vec{u}_L \quad (8)$$

The control structure of the proposed scheme is shown in Fig. 4.

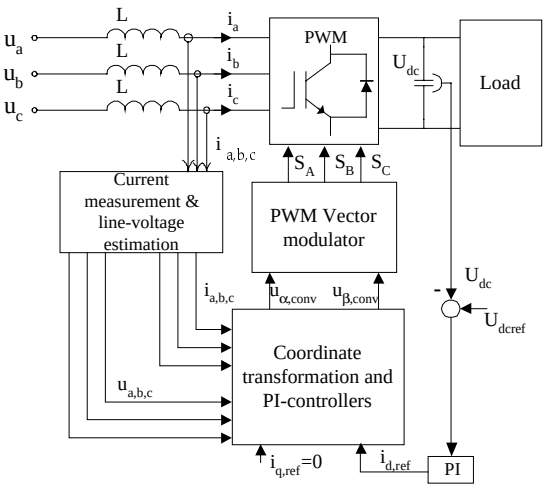

Fig. 4. Control structure for conventional VOC with line voltage estimation.

III. MODULATION STRATEGIES

There is no need for PWM modulation in the DPC because the switching states are determined by table based errors in the instantaneous active and reactive power. However, in the conventional VOC the modulation strategy has a strong influence on the performance of the PWM rectifier.

For the sake of easy microprocessor implementation and high performance, two modulation strategies are most popular: space vector modulation with symmetrical zero states (SVPWM) and discontinuous modulation where only two phases are switched (one phase is always clamped to 1 or to 0).

One disadvantage of DPWM compared to SVPWM is a higher harmonic ripple at low modulation index. But under normal conditions the active rectifier operates at high linear modulation index.

Both modulation methods possess high linearity and low time-consuming algorithms. Comparing the two modulation strategies it becomes clear that discontinuous modulation

TABLE I. Comparison of sensorless control strategies for PWM rectifier.

	Direct power Control	Voltage Oriented Control
Controller	Non-linear hysteresis controllers	Linear PI controllers
Modulation	Table based variable switching frequency. Therefore: • High value of inductance is needed (about 10 %) (important point for the line voltage estimator, because smooth shape of current is needed). • The wide range of switching frequency can result in trouble when designing the necessary input filter. • Calculation of power and voltage should be avoided at the moment of switching, because this gives high errors of the estimated values.	Space vector based constant switching frequency. Therefore: • Fixed switching frequency (easier design of the input filter). • Advanced modulation strategies, such as DPWM, can be used.
Algorithm	Very simple	More complicated
Complexity	No coordinate transformation	Coordinate transformation and decoupling between active and reactive components is required
Sampling frequency	Very high (80 kHz) • Fast microprocessor is required • Fast A/D - converters are required	Low sampling frequency (≤ 10kHz) can be used for good performance • Cheaper A/D converters

Total power factor	High - Current follows exactly the line voltage	Lower than for DPC

provides lower switching losses in the converter. About 50 % reduction of the switching losses can be obtained [6].

A more practical advantages for the industry is shown by [6]. Discontinuous modulation can reduce the size of the input filter under the assumption of two times higher switching frequency and the same switching losses compared to SVPWM.

IV. RESULTS

Simulations and experiments with a PWM rectifier has been performed to analyze and compare the DPC with the conventional VOC strategies. The main parameters of the system under consideration are summarized in Table II. The research has been carried out for two cases:

- Ideal line voltage (balanced and sinusoidal)
- Distorted line voltage with 5% 5th harmonics and 4.5% unbalance

The degree of voltage unbalance is defined as:

$$u = \frac{e_n}{e_p} \tag{9}$$

where: e_p is the positive sequence input voltage vector
e_n is the negative sequence input voltage vector

The per-unit quantities are based on the following definitions:

- Input line-line rms voltage U_{ab} *= 1 per unit*
- Fundamental apparent input power S_1 *= 1 per unit*
- Base impedance $Z_b = U^2_{ab}/S_1$ *= 1 per unit (100%)*

The inductance (L) is normally in the range of 5% - 10% (related to the PWM rectifier). The presented simulations and experiments are made with a 8.7% boost inductance. The line impedance is neglected.

TABLE II. System parameters.

AC Line side		
Parameter	Value	Unit
Input Voltage (U_{ab})	400	V
Inductance (L)	12.6	mH
Input power (S_1)	3.5	kVA
Switching frequency (Average)	5	kHz
DC Link side		
Voltage	600	V
Capacitor	1000	µF

A. Simulation Results

A PWM rectifier with the presented control schemes has been simulated using SABER. The simulated waveforms for DPC, VOC with SVPWM and VOC with DPWM are presented in Fig. 5, Fig. 6 and Fig. 7 respectively. These oscillograms are obtained for the same operation conditions. Note, that the estimated line voltage follows the actual line voltage very close for both under pre-distorted and unbalanced conditions as well as under ideal conditions. The current total harmonic distortion factor (THD) for the three control schemes are summarized in Table III together with the different operating conditions and experimental results.

a) b)

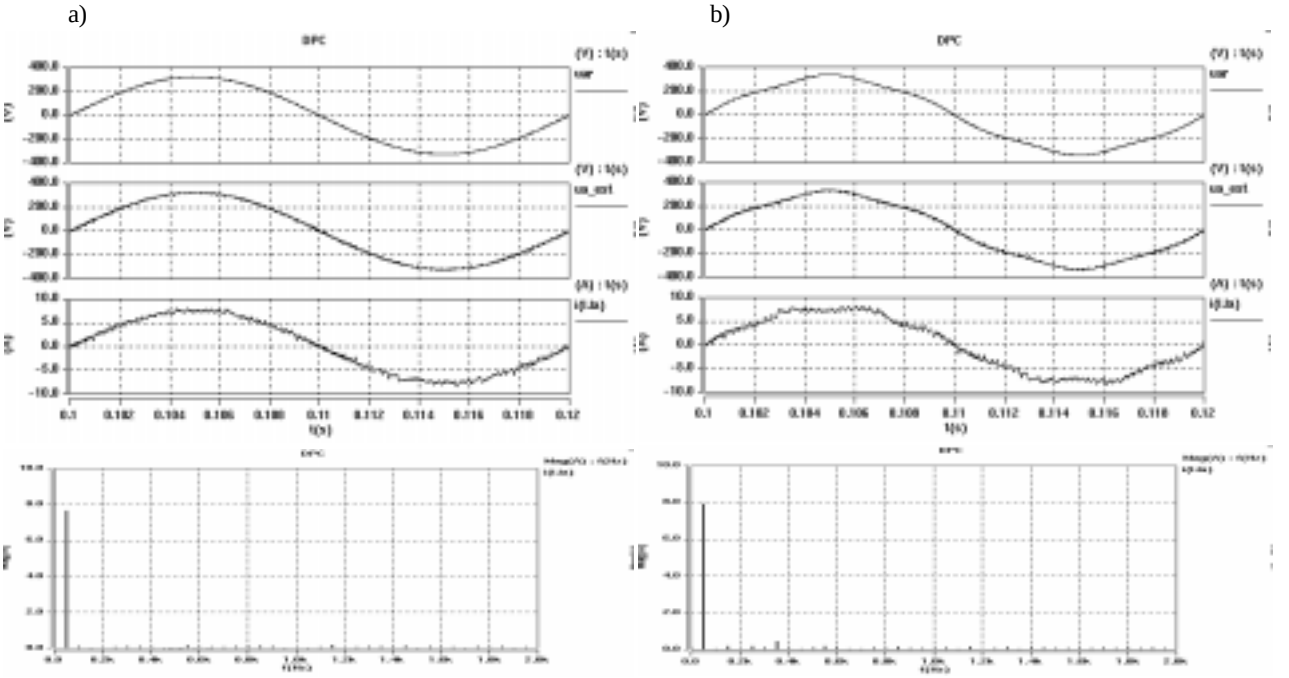

Fig. 5. Simulations results for the sensorless DPC scheme: (a) under balanced sinusoidal supply. (b) under 4.5% voltage unbalance and 5% 5th harmonic non-

sinusoidal supply. From the top: Line voltage, estimated line voltage and input current, together with the harmonic spectrum of the input current for DPC.

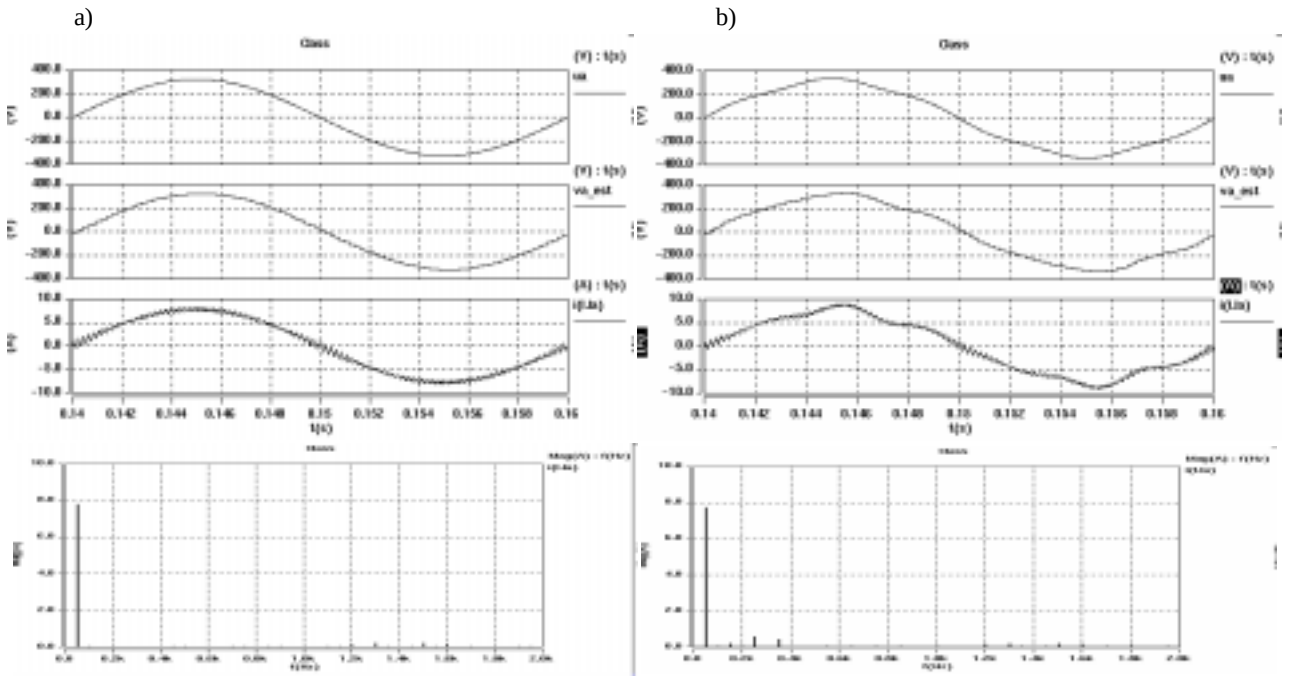

Fig. 6. Simulations results for the sensorless VOC scheme with SVPWM: (a) under balanced sinusoidal supply. (b) under 4.5% voltage unbalance and 5% 5th harmonic non-sinusoidal supply. From the top: Line voltage, estimated line voltage and input current, together with the harmonic spectrum of the input current.

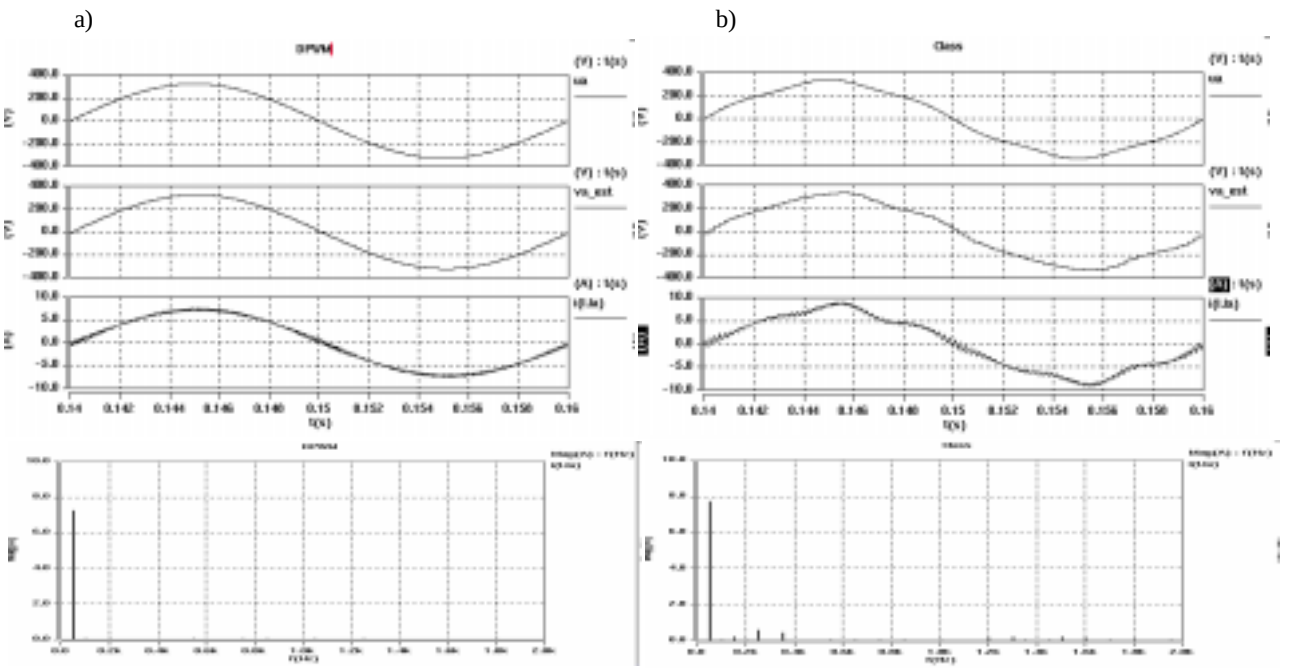

Fig. 7. Simulations results for the sensorless VOC scheme with DPWM: (a) under balanced sinusoidal supply. (b) under 4.5% voltage unbalance and 5% 5th harmonic non-sinusoidal supply. From the top: Line voltage, estimated line voltage and input current, together with the harmonic spectrum of the input current.

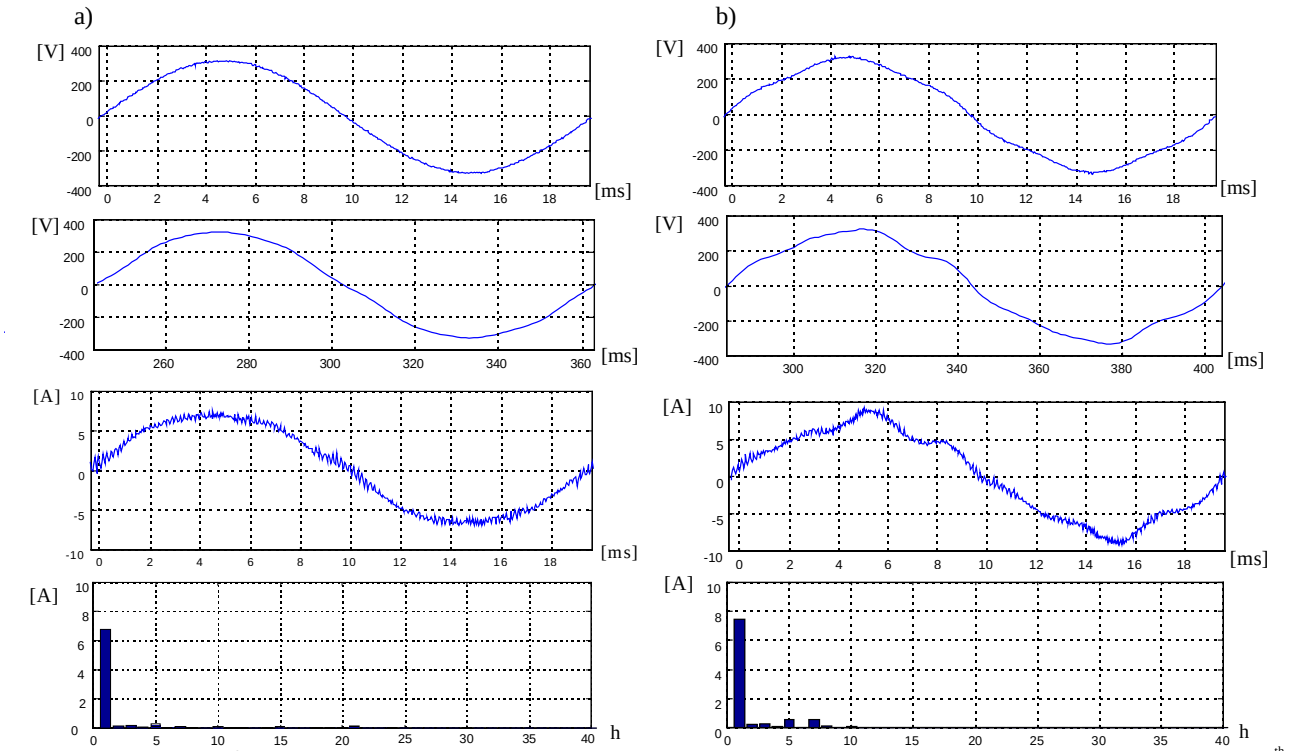

Fig. 8. Experimental results for the sensorless VOC scheme with SVPWM: (a) under balanced sinusoidal supply. (b) under 4.5% voltage unbalance and 5% 5th harmonic non-sinusoidal supply. From the top: Line voltage, estimated line voltage, input current and the harmonic spectrum of the input current.

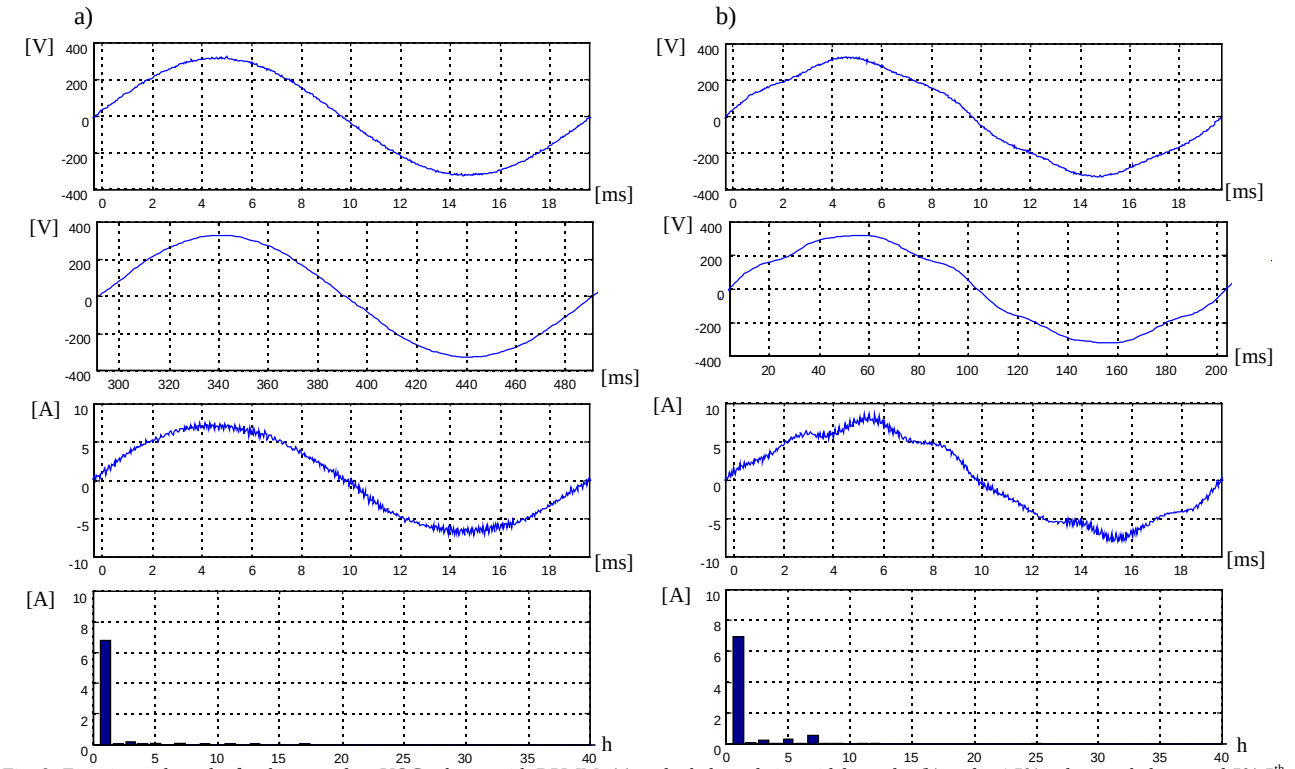

Fig. 9. Experimental results for the sensorless VOC scheme with DPWM: (a) under balanced sinusoidal supply. (b) under 4.5% voltage unbalance and 5% 5th harmonic non-sinusoidal supply. From the top: Line voltage, estimated line voltage, input current and the harmonic spectrum of the input current.

TABLE III. Simulation and experimental results

Control strategy	Sampling frequency	Switching frequency	THD of line current			
			Sinusoidal voltage		Unbalanced and distorted line voltage	
			Simulation	Experimental	Simulation	Experimental
DPC	80 kHz	5 kHz (average)	5.6 %	-	8.9 %	-
VOC with SVPWM	5 kHz	5 kHz	4.5 %	6.1 %	9.2 %	11.8 %
VOC with DPWM	10 kHz	6.66 kHz	2.6 %	3.1 %	8.0 %	10.1 %

B. Experimental Results

An experimental setup is used in the laboratory of the Institute of Energy Technology at Aalborg University. The laboratory setup consist of a three-phase 30 kVA programmable power supply, two commercial inverters controlled by two DSP's (ADSP 21062) and a motor-generator setup as load. Unfortunately, it was not possible to implement the DPC control in this setup because very high sampling frequency is required. However, the results obtained with the VOC scheme show to be very close to the simulated results. Therefore, the simulated results of the DPC are used to make the final conclusion of the comparison of the presented sensorless control strategies.

The experimental results for the conventional VOC strategy with SVPWM and no ac-line voltage sensors are shown in Fig. 8. The experimental results for VOC with DPWM and no ac-line voltage sensor are shown in Fig. 9. The current total harmonic distortion factor (THD) for the two control schemes are summarized in Table III together with the different operating conditions and the simulated results.

VI. CONCLUSION

In this paper two different control strategies for PWM rectifier are presented. The DPC which has no need for line voltage measurements is compared to the conventional VOC strategy in the rotating coordinates along with a novel line voltage estimator. It is shown by simulations and experimental results that both line voltage estimators performs very well even under unbalanced and pre-distorted conditions. Furthermore, the current follows the voltage fairly well with both control strategies. However, sometimes sinusoidal currents are desired even under unbalanced and pre-distorted conditions. For the conventional VOC scheme some compensating algorithms exists [1], [2], while there is a lack of those algorithms for the DPC. Also the VOC exhibits other advantages compared to the DPC. The most important advantage is the lower sampling frequency, why cheaper A/D converters and micro-controllers can be used.

Therefore, the conventional VOC scheme with DPWM should be preferred in a standard industrial purpose PWM rectifier.

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Harmonic Distortion and Reduction Techniques of PWM Adjustable Speed Drives – A Cost-Benefit Analysis

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ABSTRACT

In this paper the line side harmonic distortion of three-phase low voltage adjustable speed drives (ASD's), in the range of a few kW to some hundreds kW, and the harmonic reduction techniques dominating the ASD market are presented. The most significant advantages and disadvantages of these techniques are discussed and a cost-benefit analysis is made. Finally some example calculations are made on a real application.

I. INTRODUCTION

A number of advantages, such as energy savings, smaller and cheaper apparatus, have increased the use of electric loads controlled by power electronic converters over the last decades. In consumer electronics we find power electronic converters almost everywhere, e.g. PC's, TV's, stereos, VCR's and in household equipment. In the industry adjustable speed drives (ASD) and uninterruptible power supplies (UPS) are commonly used power electronic converters.

But the increasing use of power electronic converters has also led to an increase of current harmonics drawn from the utility grid. International standards, such as the IEEE 519, EN 61000-3-2 and EN 61000-3-12 have been made to protect the power system from harmonics and to reduce the uncertainty the customers of power electronic equipment may experience with regards to harmonic distortion. Unfortunately, these standards have some unwanted effects for ASD's:

In some standards the harmonic currents are limited to a level that requires expensive measures and the economical advantage that ASD's gives (e.g. due to energy savings) are vanishing. In the heating, ventilation and air-conditioning (HVAC) market this may result in that the payback time for using ASD's become too high and the customer prefers a HVAC unit without any ASD control. This results in increased energy consumption, which probably was not the intention of the harmonic limiting standard.

Another undesirable effect of the harmonic limiting standards is that they may be misinterpreted and become misleading. Articles, such as ref. [1], using sentences like "Equipment like……..are sensitive to harmonic distortion" have been the reason why consulting engineers and customers of ASD's now fear harmonics even though they may never have experienced any problems. They specify (or buy) expensive converters or filters where it may not be necessary. Therefore a fair discussion of harmonics is needed.

In this paper the harmonic distortion of three-phase low voltage (LV) ASD's, in the range of a few kW to some hundreds kW (shaft power), and the harmonic reduction techniques dominating the ASD market today are presented. The most significant advantages and disadvantages are discussed and a cost-benefit analysis is made for the harmonic reduction techniques of ASD's. Finally some example calculations on real applications are made.

The line side harmonic distortion of PWM ASD has only partly been covered by a large amount of papers dealing with this subject in general. Most papers are focusing on the harmonic current distortion of the basic 6-pulse rectifier used in PWM ASD [2] – [7], while the harmonic voltage distortion is a less covered subject [8] – [10].

The main purpose of the international standards is to protect the power system from unwanted harmonic voltage distortion. Also it is the harmonic voltage distortion that disturbance other loads or users. Therefore the harmonic voltage distortion is the most important subject and is therefore also considered in this paper.

Several papers have already compared different harmonic reduction techniques suitable for ASD's [11] –[14]. However, most papers are focusing on the harmonic performance of the rectifiers. Experience shows that the harmonic reduction technique with the best harmonic performance is normally not required in a typical application. Therefore this paper presents a cost-benefit analysis that hopefully will enable users and customers of ASD's to find the technology that fits their requirements.

II. HARMONIC DISTORTION OF PWM ASD'S

The PWM ASD with a basic 6-pulse rectifier as shown in Fig. 1 has typical a input current waveform as shown in Fig. 2.

In this particular case the total harmonic current distortion (THD_i) equals 70 %. Where THD_i is defined as:

$$THD_i = \sqrt{\sum_{2}^{40}\left(\frac{I_h}{I_1}\right)^2} \cdot 100\,\% \qquad (1)$$

where

I_h harmonic current of the order h.
I_1 fundamental current.

The harmonic current of the basic 6-pulse is very depending on the grid the rectifier is connected to [8], [15]. In general a high harmonic distortion (up to THD_i = 120 %) can be expected when the rectifier is connected to a strong grid and a low harmonic distortion when connected to a weak grid (down to THD_i = 35 %).

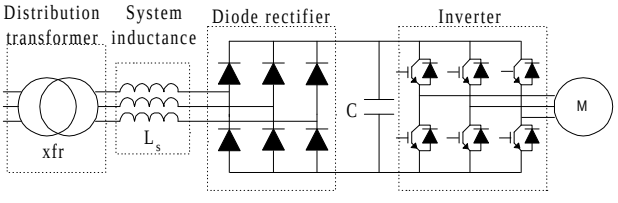

Fig.1. Basic ASD with a simple diode rectifier without any use of harmonic reduction techniques.

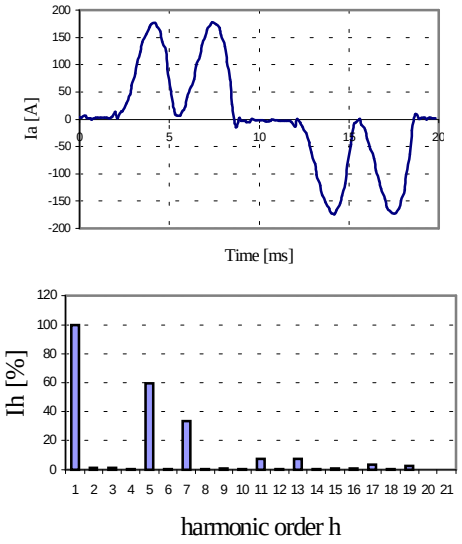

Fig.2. Typical line current of a basic 6-pulse rectifier and the Fourier series of the current. The current THD_i in this particular case equals 70%.

Normally, the harmonic currents are considered to flow from the non-linear load into the source. Because of the impedance between the equipment and the utility source the harmonic current is generating a voltage drop. This harmonic voltage drop is the reason why the utility voltage is not sinusoidal at the connection point but becomes distorted. If the harmonic impedance and the harmonic currents are known, the individual harmonic voltages ,V_h, can easily be calculated by equation (2):

$$\overrightarrow{V_h} = \overrightarrow{I_h} \cdot \overrightarrow{Z_h} \tag{2}$$

where

Z_h Harmonic impedance of the order h.

Unfortunately neither the harmonic impedance nor the harmonic currents are easy to determine exactly in a given system. Another problem in calculating the harmonic voltage distortion is that the harmonic voltages may be influenced by other parameters such as resonance, pre-distorted and unbalanced voltage [17], [18].

A. Simple Voltage Distortion Calculations

Making some assumptions, such as balanced and sinusoidal supply voltage and that no capacitors are located near the ASD, an estimate on the voltage distortion can be made quite simple.

Let us consider a typical industrial distribution system where some ASD's are used as shown in Fig. 3.

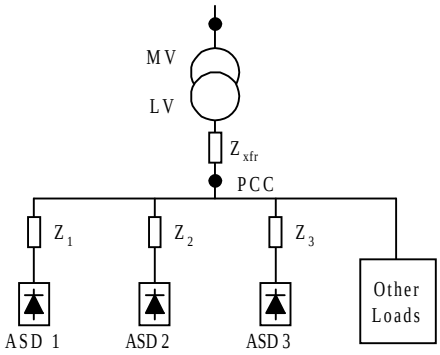

Fig. 3. Typical industrial distribution line.

Normally the impedance of the medium voltage (MV) line is neglected, since the impedance on the LV-line and the transformer (Z_{xfr}) generally is at least 90% of the total impedance and commonly more [19]. Also capacitive effects are frequently neglected in order to do simple calculations. Therefore, it is possible to calculate the voltage distortion at the point of common coupling (PCC), in this case the transformer, only knowing the impedance of the transformer and the harmonic currents. Also important to know is, that the transformer impedance is mainly inductive, so that equation (2) can be rewritten as:

$$\overrightarrow{V_h} = \overrightarrow{I_h} \cdot h\overrightarrow{X_{xfr,1}} \tag{3}$$

where

$X_{xfr,1}$ fundamental transformer reactance.

In a system where more ASD's are present, as in Fig. 3, it is convenient to reduce the system under investigation as shown in Fig. 4. Here the rectifier represents the sum of all ASD loads.

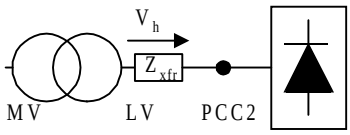

Fig. 4. Reduced system under consideration. The total rectifier load is summed to one virtual rectifier load.

Often the total harmonic voltage distortion (THD_v) is used as an indication if potential harmonic problems are present. This simplifies the calculations significantly as shown in the following. The voltage THD_v is defined as:

$$THD_v = \sqrt{\sum_{2}^{40}\left(\frac{V_h}{V_1}\right)^2} \cdot 100\% \tag{4}$$

The harmonic voltage V_h is depending of the harmonic currents and the harmonic impedance. Assuming that the impedance is purely inductive equation (4) can be rewritten as:

$$THD_v = \sqrt{\sum_{2}^{40}\left(\frac{hX_1 I_h}{V_1}\right)^2} \cdot 100 = \frac{1}{I_{sc}}\sqrt{\sum_{2}^{40}(hI_h)^2} \cdot 100 \tag{5}$$

For calculation of the total harmonic voltage distortion it is convenient to define the so-called harmonic constant Hc [15]:

$$Hc = \sqrt{\sum_{2}^{40}\left(h\frac{I_h}{I_1}\right)^2} \cdot 100\% \tag{6}$$

The definition of Hc reminds somewhat of the definition of the current THD_i. But in the Hc definition the harmonic currents are weighted by its order. The harmonic constant relates to the voltage THD_v like:

$$THD_v = Hc \cdot \frac{I_1}{I_{sc}} = Hc \cdot \frac{S_1}{S_{sc}} \tag{7}$$

The voltage distortion can now be calculated by the ratio fundamental load power to the system short circuit power times Hc. Fig. 5a shows the values for different short circuit ratios for the basic 6-pulse rectifier and Fig. 5b shows the Hc values for a 6-pulse rectifier with a 3% build-in dc-coils.

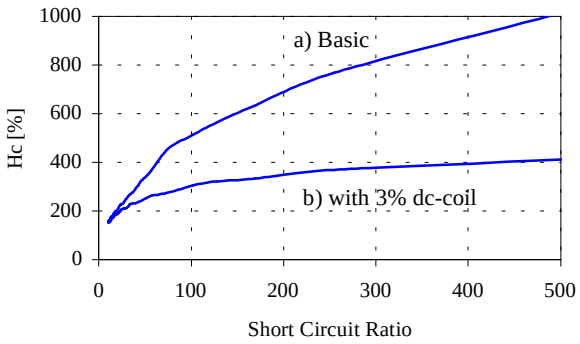

Figure 5. Hc values for different rectifier types and short circuit ratio. a) Basic 6-pulse rectifier b) 6-pulse rectifier with 3% dc-coil.

B. Example calculation

To illustrate the simplicity of the above-mentioned calculation method an example is showed here. Let us consider a system where an ASD load of 300 kW fundamental input power is connected to a 1 MVA transformer. To be sure that the system complies with the IEEE-519 it is necessary to determine the resulting voltage distortion at the PCC. In this case the PCC is the transformer. The transformer impedance is ex = 5%. The short circuit power on the secondary side of the transformer is therefore 20 MVA and the short circuit ratio equals 66. The non-linear load is a 6-pulse rectifier with build-in dc-link inductance. Using Fig. 5b the Hc value is read to be 250.

The resulting voltage distortion can now be calculated by the use of equation (7).

$$THD_V = Hc \cdot \frac{S_1}{S_{sc}} = 250 \cdot \frac{300KVA}{20000KVA} = 3.75\% \qquad (8)$$

III. HARMONIC REDUCTION TECHNIQUES

In this section the harmonic reduction technique dominating the ASD market are presented. The performance indexes such as THD_i, Hc and THD_v are summarized in Table 2.

The voltage THD_v is based on the assumption that an ASD with a fundamental input power of 300 kW is connected directly to a 1 MVA transformer with a short circuit impedance of 5 %.

A. ac-coils

The most common and easiest harmonic reduction technique is probably the use of ac-coils in front of the ASD as shown in Fig 6. Typical 1 % to 5 % inductors are used. The ac-coils smoothens the line current drawn by the converter. Hereby a significant lower current distortion can be achieved compared to the basic ASD. Another advantage is that the continuous dc-link current obtained by adding ac-coils increases the lifetime of the dc-link capacitors.

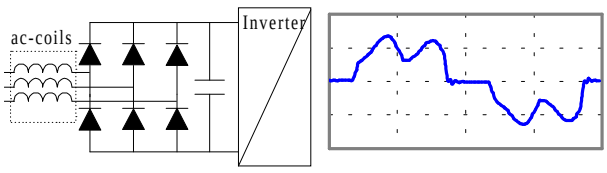

Fig. 6. Basic ASD with ac-coils and the line current.

The drawback is a reduced dc-link voltage because of increased commutation time. The reduction of the dc-link voltage can approximately be calculated by equation (9) [25]:

$$\Delta V \approx 0.5 \cdot X_{ac} \qquad (9)$$

where: X_{ac} is the ac-reactance in percentage.
ΔV is the reduction of the dc-link voltage in percentage

I.e. 3% ac-reactance reduces the dc-link voltage by 1.5 %.

B. dc-coils

Similar effects as with ac-coils can be obtained with dc-coils build-in to the ASD as shown in Fig 7. Here the ripple current in the dc-link is smoothened by the inductor. Typical between 3 % and 5 % inductors are used. Also the lifetime for the dc-link capacitor is increased as with ac-coils. The advantage compared to ac-coils is that the dc-link voltage is not reduced due to commutation voltage drop in the rectifier.

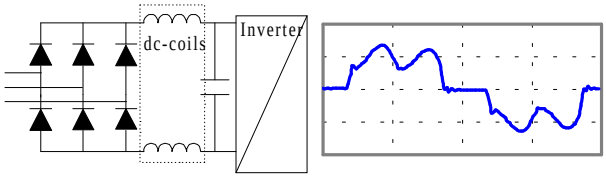

Fig. 7. Basic ASD with dc-coils and line current.

C. Grid enhancement

Another obvious method to reduce the voltage distortion is to strengthen the grid and hereby reducing the supply impedance. This can be obtained by using a larger distribution transformer. However, the current distortion will not be reduced. If a basic ASD (no ac- or dc-coils) is used the current distortion will increase because the inductance in front of the drive is reduced.

Because of the nature of this harmonic reduction technique this approach is not useful for retrofit applications, but can be used to design a given system into some voltage harmonic requirements.

D. Passive Filter

Passive harmonic trap filters have commonly been used in large plants where harmonics have been a problem, i.e. HVDC. These filters have the disadvantage that each single system has to be engineered separately due to risk of resonance problems and has therefore not been an alternative for low and medium power ASD's.

Recently some companies have developed tuned and broadband, of the shelf, passive filters, which can be connected in front of the ASD [20]. However, disadvantages such as increased rms current due to the reactive power of the capacitors remains. Also these filters are quite heavy and bulky.

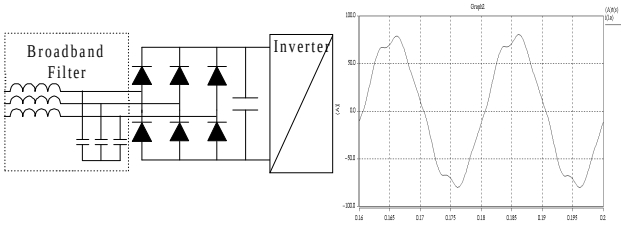

Fig. 8. Passive Broadband filter.

E. Active PWM Filter

An alternative to the passive filter is the active PWM filter. The active PWM filter gives excellent performance and controls the harmonic and fundamental currents. Also no pre-engineering is needed before connecting them to a given system.

Today we can find several manufactures of active PWM filters for the general power quality market [23], [24] and some of them are now moving into the ASD market.

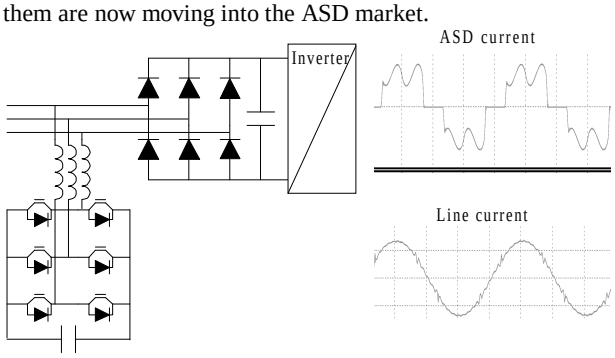

Fig. 9. ASD with active PWM filter.

Besides that the PWM active filter has a complex control structure and needs six active switches the biggest disadvantage of active PWM filter is that switching directly on the mains makes design with respect to EMC a challenge. Unless a proper designed low-pass passive filter is used between the line and the active filter, switching noise will be present both in the line-current and in the line-voltage [22].

F. Active PWM Rectifier

Because of capabilities such as: power regeneration, low harmonic input current distortion and controlled dc-link voltage, PWM rectifiers are often used in high performance adjustable speed drives (ASD's) where frequent acceleration and de-acceleration is required. Because of the harmonic limiting standards the PWM rectifier is believed to be a realistic alternative to the diode rectifier also in medium performance applications in the future [21]. A diagram of an ASD with a PWM rectifier is shown if Fig 10.

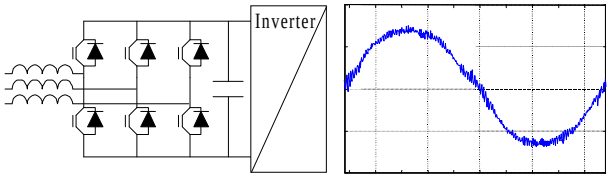

Fig. 10. ASD with active PWM rectifier.

Similar to the PWM active filter, the active rectifier has a complex control structure and needs six active switches. Again a properly designed low-pass passive filter is needed in front of the PWM active rectifier and an EMC correct design can be a challenge [22].

G. 12-pulse

12-pulse rectifiers are the standard harmonic reduction technique used in ASDs, when ac-coils or dc-coils not are sufficient. It seems that the parallel 12-pulse rectifier has lately forced out the traditional three-winding serial 12-pulse rectifier in low voltage applications, as shown in Fig. 11.

This is due the fact that the parallel 12-pulse rectifier can use smaller autotransformers instead of the bulky three-winding transformer with galvanic isolation. However, the serial 12-pulse rectifier has some advantages at pre-distorted or unbalanced supply voltage, where a more equal current sharing is obtained. This ensures a better performance and protects the diodes for overload at non-ideal conditions. [15]

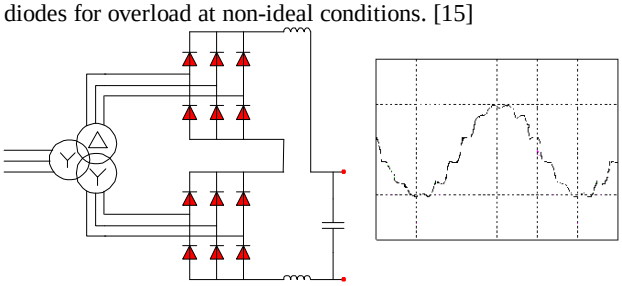

Fig. 11. Serial 12-pulse rectifier.

H. Quasi 12-pulse

An often used, but in the literature less well-documented technique, is the quasi 12-pulse rectifiers. Connecting some ASD's to a 30° phase shifting transformer and others directly to the line, as shown in Fig. 12, results in harmonic cancellation of the 5^{th} and 7^{th} harmonic currents. However, total cancellation will only be achieved when the load is balanced between these two systems.

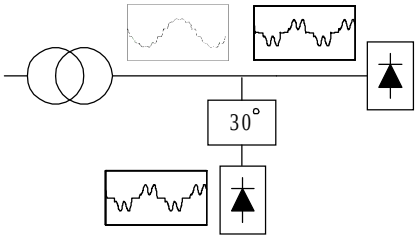

Fig. 12. Quasi 12-pulse rectifiers.

Compared to ac-coils or build-in dc-coils, experience shows that the typical voltage distortion will be decreased by a factor of two by introducing the quasi 12-pulse technique.

I. Mixing single- and three-phase diode rectifiers

Mixing three- and single-phase rectifier loads gives usually a better harmonic performance than each load type would on their own. Fig. 13 gives an example where the current THD of a three-phase rectifier has current THD_i of 51 %, the single-phase rectifier has a THD_i of 88 % and the sum of these two currents gives a THD_i of only 38 %. The reason for this is that the 5^{th} and 7^{th} harmonic current of single-phase diode rectifier often are in counter-phase with the 5^{th} and 7^{th} harmonic current of three-phase diode rectifiers [8].

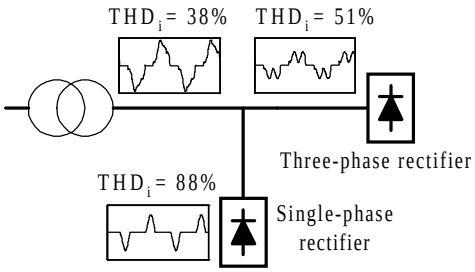

Fig. 13. Mixing single-phase and three-phase diode rectifier.

	THDi [%]	Hc [%]	rms current [%]	THDv [%]	Comments
Basic ASD	35 – 120	200 - 1000	110-150	7.5	Hc = 500 assumed.
ac-coils	30 – 50	150 - 400	106-110	3.75	Hc = 250 assumed.
dc-coils	30 – 50	150 - 400	106-110	3.75	Hc = 250 assumed.
Grid enhancement	System depending	System depending	System depending	System depending	Decreasing the system impedance will decrease the harmonic voltage distortion.
Passive filters	10 -20	System depending	System depending	System depending	Because of the capacitors needed in the passive filters the rms current is high even though the THDi is low.
Active PWM Filters	5 – 15	Design depending	100-101	Design depending	Passive filters are necessary to filter for switching noise. Hc and THDv are depending on the filter design and switching frequency.
Active PWM rectifier	5 –10	Design depending	100-101	Design depending	Passive filters are necessary to filter for switching noise. Hc and THDv are depending on the filter design and switching frequency.
12-pulse	15 – 25	75 - 150	101-103	1.875	Hc = 125 assumed.
Quasi 12-pulse	15 – 25	75 – 150	101-103	1.875	Hc = 125 assumed.
Mixing single- and three-phase rectifiers	System depending	System depending	System depending	System depending	5^{th} harmonic cancellation on both voltage and current is expected.

Table 2. Performance index of the harmonic reduction techniques available for ASD's on today's market.

In general this cancellation effect can be difficult to predict. However, if a large amount of single-phase diode rectifiers are connected to the same line as the ASD a better harmonic overall performance may be obtained with a six-pulse rectifier instead of a 12-pulse rectifier which do not cancel the 5^{th} and 7^{th} harmonic current of the single-phase load. The consequences of the harmonic cancellation effects should be considered both in new and in retrofit applications. (Maybe a more expensive rectifier technology for your ASD will result in a worse result than a 6-pulse rectifier with ac- or dc-coils.)

J. Realistic combinations

Some of the mentioned harmonic reduction techniques can be combined for better harmonic performance or utilization of the transformer. In an ASD with build in dc-coils it can be difficult to increase the inductance for better harmonic performance. Here ac-coils are often used optionally to further improve the harmonic performance.

Another interesting combination is to use ASD's with either ac- or dc-coils and to connect an active PWM filter to these drives. The PWM filter should be rated for the amount of harmonic current it must filter, therefore a smaller PWM filter may be used in combination with drives using ac- or dc-coils compared to a basic ASD.

IV. COST-BENEFIT ANALYSIS

Besides the cost for the ASD including one of the presented rectifier topologies other costs become quite significant in a total cost analysis. The most important cost drivers, which are discussed in the following, are:

- Protection, cables, transformer etc. (rms current)
- Installation (number of extra components e.g. filters)
- Pre-engineering
- Lifetime

The THD_i contributes to the rms current as shown in equation (10):

$$I_{rms} = I_1 \cdot \sqrt{1 + THD^2} \tag{10}$$

Let us assume a basic ASD with a $THD_i = 80$ %. Here the rms current is 128 % of the active current I_1. An ASD with dc-coils and a $THD_i = 40$ % increases the rms current only by 8 % compared to I_1. Here is a significant cost factor. E.g. using ac-coils or using an ASD with build-in dc-coils reduces the rms current compared to the basic rectifier and the transformer can be utilized better. Also a smaller cable cross-section and protection gear may be used which again can contribute to some cost savings. Furthermore, using ac- or dc-coils guarantees continuous current into the dc-link, which increases the lifetime of the dc-link capacitors. This could be a second order cost factor.

But which one of these two is the best solution? Drives with build in dc-coils is a compact space saving design with higher efficiency than drives with ac-coils. Also, since dc-coils usually are build-in, no extra installation costs have to be taken into account as with ac-coils. However, optional ac-coils give one the possibility to choose which size the ac-coils must have to fulfill the specifications and therefore a more optimal solution may be obtained.

The tricky part comes when these cheap adjustments and even a combination of ac- and dc-coils (combo) are not sufficient. Several options are possible and some of these solutions are marked quite aggressively.

It is impossible to determine a general harmonic reduction technique for ASD's that is the optimal solution in all applications. There is a difference whether the ASD is connected to an existing plant or the plant is to be planned. Also there is a difference if several ASD's are used or only one large ASD.

If several ASD's are used the quasi 12-pulse rectifier is a possibility. Also passive and active filters are solutions to reduce the harmonic distortion on a system level. However, even though solutions on a system level seem cheaper than apparatus level solutions, some kind of pre-engineering is needed for the system level solution. Predicting the costs for the pre-engineering is quite difficult because different systems and requirements will result in different costs.

No pre-engineering or extra installations cost are needed when using an apparatus level solutions, such as the 12-pulse rectifier. Alternatively if power regeneration is required, a PWM rectifier can be used. This saves the dynamical braking resistor.

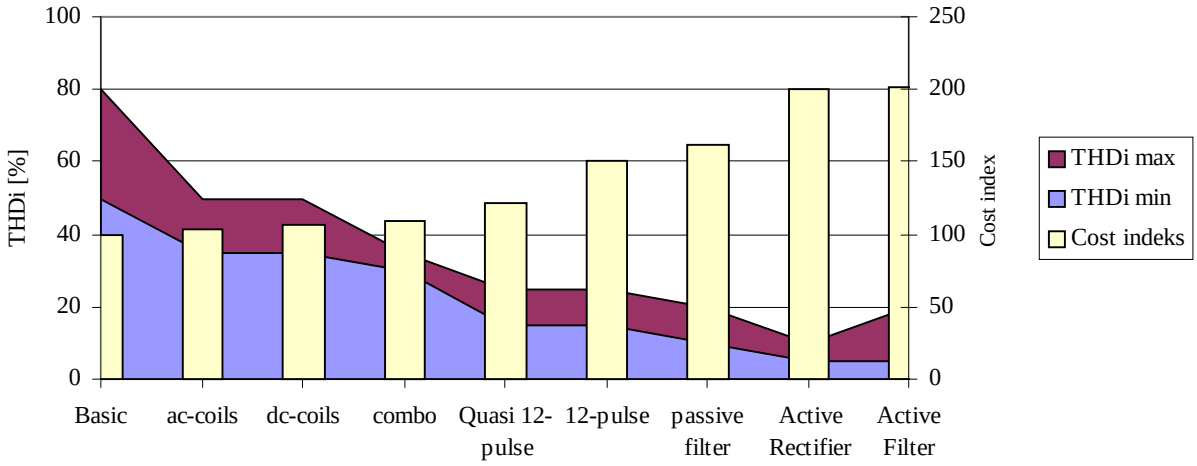

Fig.14. Cost – benefit of harmonic reduction techniques for three-phase ASD's.

However, the price per equipment is quite high compared to other rectifier topologies. But in a system where only one large ASD is connected this may be a good solution.

Fig. 14 shows the harmonic performance versus the estimated costs of the presented harmonic reduction techniques.

Methods like mixing the single-phase and three-phase diode rectifier loads, e.g. HVAC and PC's, are not taken into account, because the resulting harmonic distortion is difficult to predict. But it is important to notice that, because of the harmonic cancellation effect of single-phase and three-phase rectifiers, a 12-pulse rectifier very well may result in worse harmonic distortion than a 6-pulse rectifier.

V. EXAMPLE CALCULATIONS

In the following there is made an example calculation and the result is summarized in table 3.

Eight ASD's with basic diode rectifiers and a total fundamental input power of 190 kW for HVAC units are connected to a 400KVA transformer with 5 % impedance. The voltage distortion is calculated to be THD_v = 7.1 %. Using ASD's with build-in dc-coils or ac-coils brings the THD_v down to 5.4 %. The price for these options is only slightly increased. To bring the voltage distortion below 5 % it is possible to use ASD's with build-in dc-coils and add 3 % ac-coils and voltage distortion is reduced to THD_v = 4.6 %. The estimated extra costs for the ac-coils equals = 400 €. But we also have to take the extra installation costs into account. The estimated cost increases with approximately 200 €.

However, this is a critical application, e.g. a hospital, and therefore the voltage distortion must be below 3%. [16]. This is not possible to obtain with reasonable sized ac-coils.

Different options are now available and are summarized in table 3. Solving the problem on the apparatus level by using 12-pulse or active PWM rectifier will typically increase the ASD price with a factor 1.4 – 2.0. The advantage of doing so, is that these techniques typically are standard solutions offered by the ASD manufacturer and no pre-engineering or extra installation costs occur.

Solving the problem on a system level can reduce the costs especially when more than one ASD are used as in this case. This, however, needs some pre-engineering to find the suitable technique. In this case it is assumed that the pre-engineering costs are 800 €.

In a plant to be planned transformer de-rating is one method to reduce the voltage distortion. E.g. by using an 800 KVA transformer and no ac-coils the voltage distortion equals THD_v = 2.7 %. Another option is to use a 630 KVA transformer and add 3% ac-coils to the ASD's. This brings the THD_v = 3.0.

Using the quasi 12-pulse technique and ASD's with build in dc-coils the THD_v = 2.7. The extra costs for four auto-transformers costs are approximately 1600 €. Again we have to add some extra installations costs. It should be noted that using a system level harmonic reduction technique it is always a god idea to use either ac- or dc-coils, because this reduces the amount of harmonic current to be absorbed by the system.

Active or Passive filters are an obvious method to reduce the harmonic distortion on a system level. Active filters are technically superior to passive filters. But the costs for a passive (of the shelf) filter tends to be less than for an active filter. In this particular case the active filter costs approximately 15000 €, while the passive filter costs 8000€.

VI. CONCLUSION

It is no easy task to find the optimal rectifier topology when buying ASD's. But it can be concluded that using ac- or dc-coils is always good idea even if the desired harmonic distortion level is not exceeded with a basic 6-pulse rectifier.

In most cases ac- or dc-coils will be sufficient to ensure a low harmonic distortion level and at the same time ensure the best efficiency, highest reliability and lowest cost compared to other harmonic reduction techniques.

However, there are applications where the harmonic requirements are strict and if a large ASD load is present the specified harmonic level may be exceeded. Here several options are possible. In general finding a harmonic reduction technique that fulfils all requirements set in such applications is difficult to find. But it seems that using a system harmonic reduction technique exhibits most advantages.

	Vthd [%]	Equipment Cost [€] (Drives + coils etc.)	Other Costs [€] (pre-engineering, installation etc.)	Cost index
Basic ASD	7.1	17,000		100
ASD with ac-coils	5.4	17,000 + 400 = 17,400	200 (installation.)	104
ASD with dc-coils	5.4	18,000		106
ASD with dc- and ac-coils	4.6	18,000 + 400 = 18,400	200 (installation.)	109
Quasi 12-pulse	2.7	18,000 + 1,600 = 19,600	200 (installation.) + 800 (pre-engineering.)	121
Passive filter	2	18,000 + 8,000 = 26,000	500 (installation.) + 800 (pre-engineering.)	161
Active PWM filter	-	18,000 + 15,000 = 33,000	500 (installation.) + 800 (pre-engineering.)	202
12-pulse ASD	2.7	25,500		165
Active PWM rectifier	-	34,000		200

Table 3. Cost index of the harmonic reduction techniques available for ASD's on today's market.

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