Three-level (TL) based isolated DC/DC converters with improved performances

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BY
DONG LIU

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AALBORG UNIVERSITY
DENMARK

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by

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CV

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His main research interests include renewable energy technology, DC/DC converters, and multilevel converters.

ENGLISH SUMMARY

AC grids are widely used nowadays for the electrical distribution system. However, the clear merits including no frequency stability, no reactive power, and simple system control of DC grids make it become the promising solution for the future electrical distribution system. In DC grids, DC/DC converters are one of most important composed components. Generally, increasing DC bus voltage is effectively way to decrease transmission power loss in DC grids. Three-level (TL) based isolated DC/DC converters (TL-IDCs) are one of most attractive choices for DC grids of DC bus with medium voltage because voltage stress of power switches is half of input voltage. Accordingly, this project mainly focuses on unidirectional TL-IDCs for DC loads such as data centre, electric vehicle, and so on.

The current research about TL-IDCs mainly includes following topics: 1) reducing switching noises; 2) increasing the converter's efficiency; and 3) increasing the converter's power density. However, only a few papers pay attentions on performances of TL-IDCs including input capacitor, power device, and transformer. Accordingly, this project investigates the control strategies to enhance the performances of input capacitor, power switch, and transformer in TL-IDCs.

For improving the input capacitor performance, this project proposes a zero-voltage switching (ZVS) control strategy including a periodically swapping modulation (PSM) strategy for four-switch half-bridge three-level (FS-HBTL) DC/DC converter to balance two input capacitors' currents, which would thus balance input capacitors' thermal stress and lifetime. Additionally, input-parallel output-parallel (IPOP) TL isolated DC/DC converters are proposed in this project for balancing and minimizing currents among input capacitors, which would thus reduce input capacitor's size or prolong input capacitor's lifetime.

For improving the power device performance, the proposed PSM strategy can be also utilized for TL-IDCs with asymmetrical control strategy to balance power devices' currents in, which would thus balance the power devices' thermal stress and power loss.

For improving the isolated transformer performance in full-bridge (FB) diode-clamped TL isolated DC/DC converter, this project proposes a new double phase-shift (DPS) control strategy to decrease voltage changes on the transformer by generating the multi-level voltage, which would thus decrease voltage change stress and voltage change rate (dv/dt) on transformer.

Finally, simulation results and experimental results both verify proposed strategies and topology.

DANSK RESUME

AC grids are widely used nowadays for the electrical distribution system. Men, de klare meriter, herunder ikke frekvensstabilitet, ingen reaktiv kraft, og enkel systemkontroll av DC grids gjør det til en lovende løsning for fremtidens elektriske distribusjonssystem. In DC grids, DC/DC converters are one of the most important composed components. Generally, increasing DC bus voltage is the effective way to reduce transmission power loss in DC grids. Three-level (TL) based DC/DC converters (TL-IDCs) are one of most attractive choices for DC grids or DC bus with medium voltage because voltage stress or power switches are half or input voltage. Følgelig, dette projekt fokuserer hovedsakelig på unidirectional TL-IDCs for DC-belastninger som datasenter, elektrisk kjøretøy, og så videre.

De huidige onderzoek over TL-IDC's omvat hoofdzakelijk volgende topics: 1) reducing switching noises; 2) increasing the converter's efficiency; and 3) increasing the converter's power density. Men, kun et par papirer betaler opmærksomheder på forestillinger eller TL-IDCs, inklusive input-kondensator, strømforsyning og transformer. Consequently, this project investigates the control strategies to enhance the performance of input capacitor, power switch, and transformer in TL-IDCs.

For at forbedre indgangskondensatorens ydeevne foreslår dette projekt en nulspændingsomskifter (ZVS) kontrolstrategi, herunder en periodisk swapping modulation (PSM) strategi for fire-switch halv-bridge tre-niveau (FS-HBTL) DC/DC konverter til balance to indgangskondensatorer 'strømme, hvilket således vil balancere indgangskondensatorernes termiske stress og levetid. Derudover foreslås input parallelle output parallelle (IPOP) TL isolerede DC/DC omformere i dette projekt for at afbalancere og minimere strømninger mellem indgangskondensatorer, hvilket således reducerer indgangskondensatorens størrelse eller forlænger indgangskondensatorens levetid.

For at forbedre effektenhedens ydeevne kan den foreslåede PSM-strategi udnyttes til TL-IDC'er med asymmetrisk kontrolstrategi for at afbalancere strømforsyningernes strømme i, hvilket således vil balancere strømforsyningsenhedernes termiske spænding og effekttab.

For at forbedre den isolerede transformator ydeevne i fuldbro (FB) diode-clampede TL-isolerede DC/DC-omformer, foreslår dette projekt en ny styringsstrategi med dobbelt faseforskydning (DPS) for at reducere spændingsændringer på transformeren ved at generere multiniveauet spænding, hvilket således ville mindske spændingsændringsspændingen og spændingsændringshastigheden (*dv/dt*) på transformeren.

Endelig kontrollerer simuleringsresultater og eksperimentelle resultater både foreslåede strategier og topologi.

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LIST OF ACRONYMS

DPS	Double phase-shift
FB	Full-bridge
FS-HBTL	Four-switch half-bridge three-level
HBTL	Half-bridge three-level
IPOP	Input-parallel output-parallel
IDCs	Isolated DC/DC converters
PSM	Periodically swapping modulation
TL	Three-level
TL-IDCs	Three-level based isolated DC/DC converters
ZVS	Zero-voltage switching

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CHAPTER 1. INTRODUCTION

1.1. BACKGROUND AND MOTIVATIONS

The clear advantages of DC grids such as no frequency stability, no reactive power, and simple system control make DC grids become promising choice for future smart power distribution system [1-8] in comparison with AC grids [9-11]. Additionally, DC-based data centres are being developed quickly nowadays [12], [13]. The liberalization of energy market also drive the requirement for developing DC grids technology, which has resulted in installations of large scale clean energy as fuel cells, wind power, solar power, and so on. Moreover, DC interfaces have already been widely employed for end-use consumers at various applications.

The general layout of DC grids is shown as Fig. 1-1.

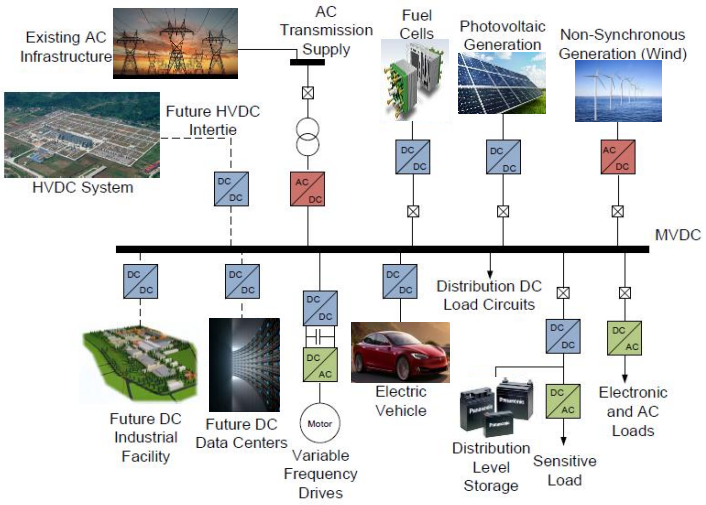
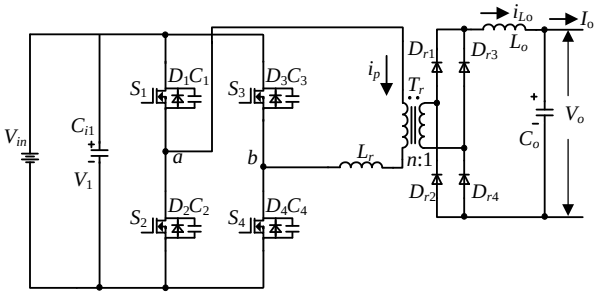


Figure 1-1 General DC grids architecture layout.

Generally, performances of DC grids are highly determined by DC/DC converters since voltage grade conversion and power transmission in DC grids are highly depended on these DC/DC converters [14-16]. Therefore, DC grids desires for DC/DC converters with high performances. Accordingly, this Ph.D. project aims at improving performances of DC/DC converters in aspect of the converter's reliability.

So far, literatures proposes many DC/DC converters which are mainly categorized into two types named non-isolated DC/DC converters [17-26] and isolated DC/DC converters (IDCs) [27-37]. Non-isolated converters cannot obtain galvanic isolation and high voltage conversion gain. Contrarily, IDCs can obtain high voltage gain, galvanic isolation due to isolated transformer and thus improve system safety. Accordingly, this project focuses on IDCs. Many IDCs have been proposed categorized into three kinds named two-level based IDCs, three-level based isolated DC/DC converters (TL-IDCs), and modular multilevel isolated DC/DC converters (MMC) [38] as presented in Fig. 1-2.

The minimal numbers of power switches are needed in two-level based IDCs [39-47] among these three kinds of converters. However, power switches' voltage stress of two-level based IDCs is full input voltage, which would thus lead high *dv/dt* on transformer, high switching loss, large electromagnetic interference (EMI) [48], [49]. MMC [50-57] differentiate themselves from other converters with good power quality, low voltage stress of power devices, and small EMI. However, MMC needs more power switches and voltage transducers, and would thus lead to increasing cost and complex control algorithm (such as voltage balancing control of capacitor) [59-62]. TL-IDCs [62-69] have merits of lower switch voltage stress, smaller output filter size, and lower EMI when comparing with two-level based IDCs. Comparing with MMC, TL-IDCs have advantages of fewer circuit components, lower cost, and easier control algorithm.



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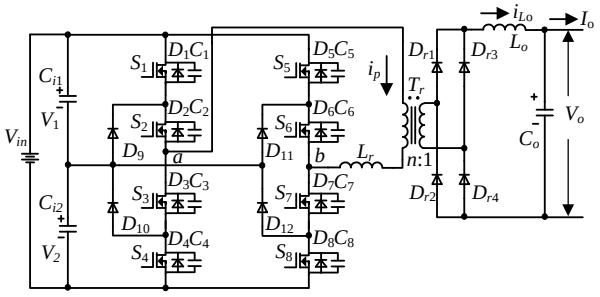

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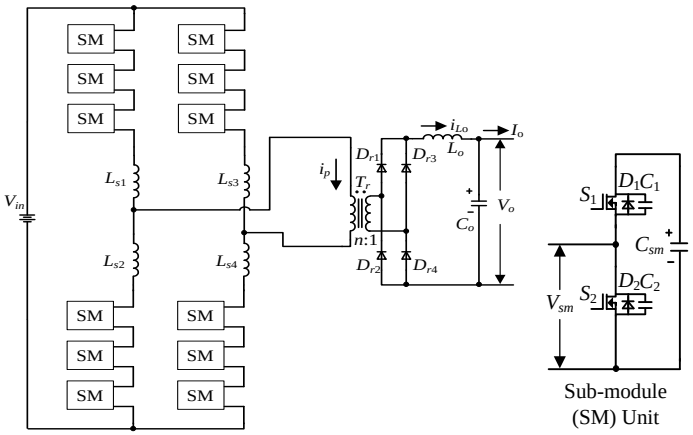


(c)

Figure 1-2 Three basic kinds. (a) Two-level isolated DC/DC converter. (b) TL isolated DC/DC converter. (c) MMC.

Comparison results between three basic kinds of DC/DC isolated converters are listed in Table 1-1. This Ph.D. project focuses on investigating unidirectional TL-IDCs' for DC loads such as data centre, electric vehicle in DC grids.

Tabel 1-1 Comparison results about three basic kinds of converters

Converter Topology	Voltage of Switches	Voltage Balance Control Complexity	Cost
Two-level based IDCs	input voltage	no	low
TL-IDCs	half input voltage	easy	medium
MMC	less than or equal half input voltage based on the number of modules	complex	high

1.2. LITERATURE REVIEW

In 1992, a novel half-bridge TL (HBTL) isolated DC/DC converter presented in Fig. 1-3(a) was first proposed [62] to reduce power devices' voltage stress. Due to TL structure, power devices' voltage stress is decreased to be half of input voltage, which would make power devices with low-voltage-rated applicable for TL-IDCs. Therefore, TL-IDCs can be utilized in DC grids with DC bus of medium voltage.

Besides HBTL isolated DC/DC converter in [62], there are also other basic topologies of TL-IDCs presented in Fig. 1-3.

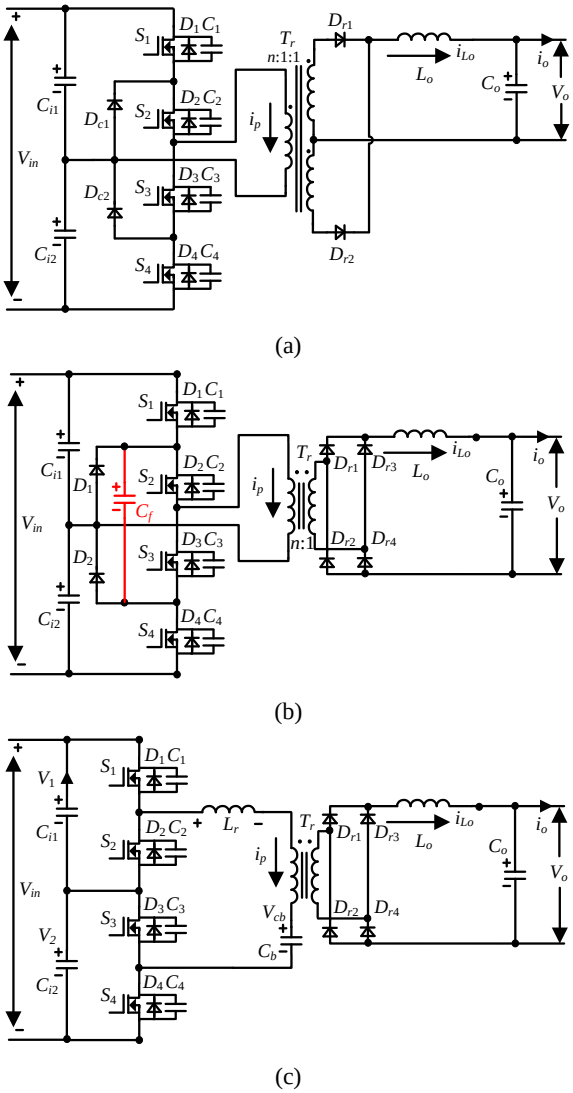


Figure 1-3 Basic topologies of TL IDCs. (a) Diode clamped HBTL isolated DC/DC converter [62]. (b) Diode clamped HBTL isolated DC/DC converter with flying capacitor [63]. (c) FS-HBTL isolated DC/DC converter [75].

A HBTL isolated DC/DC converter including an added flying capacitor presented in Fig. 1-3 (b) was proposed in [63], which makes phase-shift control applicable. Reference [75] proposed a FS-HBTL isolated DC/DC as shown in Fig. 1-3 (c).

Comparing with conventional diode clamped HBTL IDCs [62], [63], FS-HBTL DC/DC converter has less components due to removing two clamping diodes.

So far, many studies have been done based on these basic topologies of TL-IDCs [70-97]. Based on investigation of these studies, there are mainly following three research topics:

- Expanding load range of soft switching achievement of TL-IDCs [70-74];
- Simplifying the circuit structure of TL-IDCs [75-80];
- Reducing the circulating current of TL-IDCs [83-88].

1.3. RESEARCH OBJECTIVES

Based on the above literature reviews, former studies about TL-IDCs mainly pay attention on aspects of reducing switching noises, increasing efficiency, and improving power density. However, only a few papers discuss about the reliability performances of TL-IDCs. Therefore, this Ph.D. project aims to investigate TL-IDCs' reliability to improve performances of TL-IDCs including input capacitor, power device, and transformer performance.

1.3.1. INPUT CAPACITOR PERFORMANCE

Capacitor is one of most important components in terms of failure rate in practical working operations of power electronic systems [89], [90]. Many working conditions (e.g. temperature, humidity, current, voltage) play important roles in the reliability of capacitors. For the power electronics field, the rating voltage and current on the capacitor are fundamental factors for selecting the capacitor. The universal methods in the power electronics field to improve the capacitor reliability are: 1) reducing capacitor's voltage stress; 2) reducing capacitor's current. Because more than one input capacitor is utilized in TL-IDCs, many studies pay attentions on how to balance input capacitors' voltages. For instance, a voltage balancing control strategy was proposed in [91] to balance input capacitors' voltages in FS-HBTL isolated DC/DC converter presented in Fig. 1-3(c). Reference [92] proposed a TL hybrid isolated DC/DC converter with balanced input capacitors' voltage, whose circuit structure is presented in Fig. 1-4. Additionally, a FB TL-based isolated DC/DC converter was proposed in [93] as presented in Fig. 1-5, which has voltage auto-balance ability of input capacitors.

However, few papers investigate input capacitors' currents of TL-IDCs. Normally, capacitor temperature is mainly decided by capacitor current and ambient temperature around capacitor. More significantly, capacitor temperature would make a crucial influence on the capacitor's lifetime. Accordingly, this project focuses on

reducing and balancing input capacitors' currents of TL-IDCs, which can thus improve input capacitor reliability by reducing input capacitors' thermal stress and balancing input capacitors' lifetime.

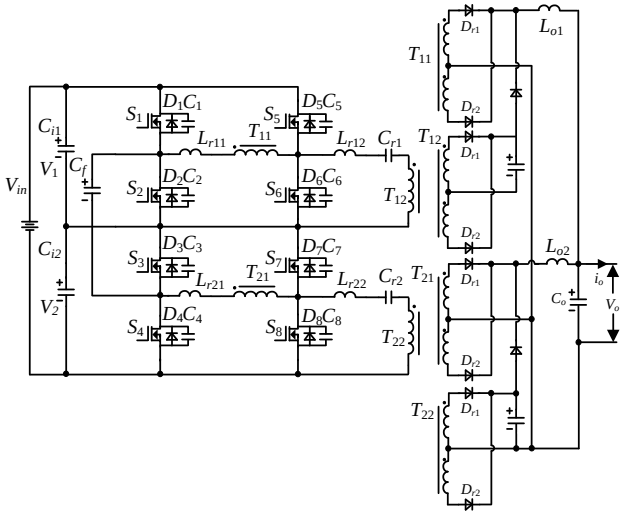


Figure 1-4 TL hybrid isolated DC/DC converter [92].

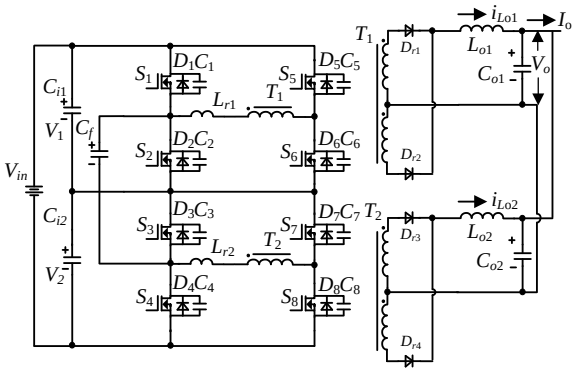


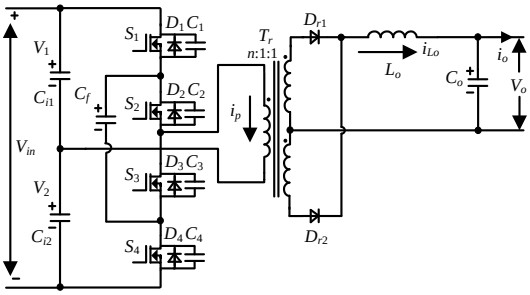
Figure 1-5 FB TL-based isolated DC/DC converter with voltage auto-balance ability of input capacitors [93].

A ZVS control strategy including a periodically swapping modulation (PSM) strategy is proposed in this project to balance input capacitors' currents for FS-HBTL isolated DC/DC converter, which can thus balance input capacitors' thermal stress and lifetime. Additionally, IPOP TL IDCs are proposed in this project to reduce and balance input capacitors' currents, which can thus prolong and balance input capacitors' lifetime.

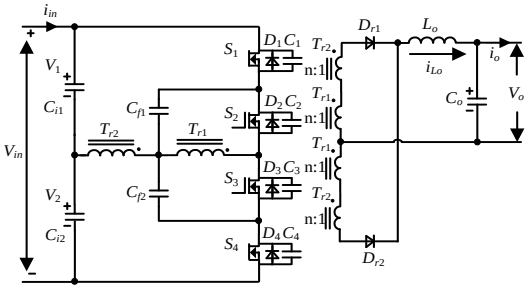
1.3.2. POWER DEVICE PERFORMANCE

The power device is another one of most significant components in power electronic systems because power generation and output/input voltage (or output/input current) are controlled by adjusting power devices' switching patterns. In addition, the cost of power devices normally occupies the dominant proportion in whole cost of power converter. Therefore, improving the reliability of power devices is significantly meaningful for enhancing the performances of converter. Normally, the temperature of power device is one of most significant parameters to judge whether the power switch operates reliably. Therefore, the thermal behaviors of power devices are quiet related to whole power electronic system's reliability performance.

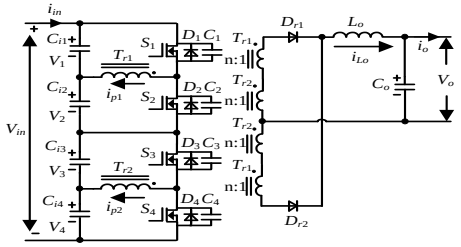
Generally, current through the power device is one of key factors that decides power device's power loss and thermal behavior. Asymmetrical modulation strategy is one of widely used modulation strategies for TL-IDCs [75], [94-96] as presented in Fig. 1-3(c) and Fig. 1-6.



(a)



(b)



(c)

Figure1-6 (a) Flying capacitor TL isolated DC/DC converter. (b) HBTL isolated DC/DC converter including two transformers. (c) Dual HBTL isolated DC/DC converter.

Reference [94] proposed a flying capacitor based TL isolated DC/DC converter featuring with simple structure. Reference [95] proposed a TL isolated DC/DC converter including two transformers to reduce transformer windings' current stresses. Reference [96] proposed a TL isolated DC/DC converter including two transformers and two half-bridge structures. Additionally, reference [75] proposed a FS-HBTL isolated DC/DC converter, which has less circuit components comparing with diode-clamped TL isolated DC/DC converter. But, there exists one significant issue caused by asymmetrical modulation strategy in these TL-IDCs [75], [94-96] that primary power devices' currents are imbalanced, which would thus lead power devices' power loss and thermal stress imbalance. Accordingly, the proposed PSM strategy are utilized for these TL-IDCs to balance primary power devices' currents, which would thus improve converter's reliability performance by balancing power devices' power loss and thermal stress.

1.3.3. TRANFORMER PERFORMANCE

The transformer is also one of significant components in isolated power converters because the transformer not only can provide high voltage conversion gain but also can isolate the electronic connection from primary to secondary side. Accordingly, improving the performance of transformer is meaningful for enhancing the performances of isolated converters. Normally, *dv/dt* is one of important factors which can make influence on the transformer of TL-IDCs. Accordingly, transformer's reliability can be improved by reducing *dv/dt* and voltage stress on transformer, which is helpful for improving converter's electromagnetic interference (EMI).

Chopping plus phase shift (CPS) and DPS control were proposed in [97] and [98] respectively for FB diode-clamped TL isolated DC/DC converter presented in Figure 1-7. However, high voltage change on transformer is caused by these control strategies, which would thus lead high *dv/dt* and electromagnetic interference (EMI). Therefore, a FB TL isolated DC/DC, as presented in Fig. 1-8, with a passive filter and a corresponding control strategy was proposed in [99], which can not only

decrease *dv/dt* but also balance input capacitors' voltages. But, added passive filter decreases converter's efficiency and voltage conversion gain. Therefore, this project proposes a new DPS control strategy for FB diode-clamped TL isolated DC/DC converter, which can decrease *dv/dt* and voltage stress on transformer.

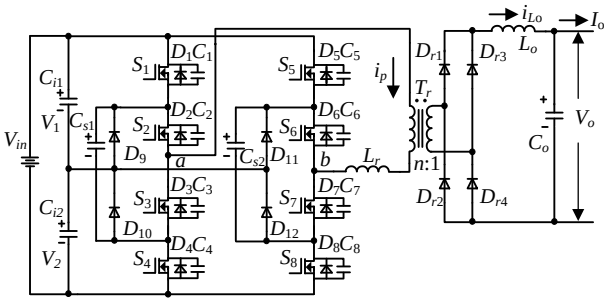


Figure 1-7 FB TL isolated DC/DC converter with flying capacitors.

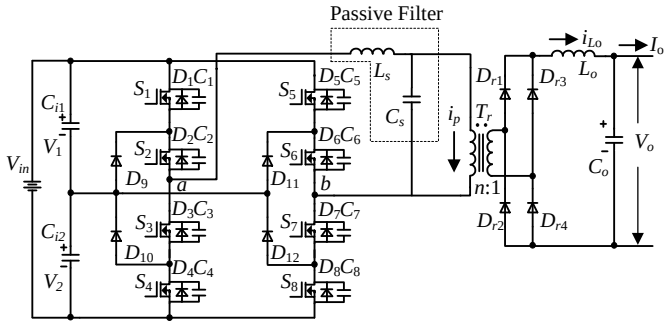


Figure 1-8 Improved FB TL isolated DC/DC converter [99].

1.4. THESIS OUTLINE

The organization about this thesis is introduced as follows.

Chapter 2 introduce a ZVS strategy including a PSM strategy for FS-HBTL isolated DC/DC converter to balance two input capacitors' currents, which can thus balance input capacitors' thermal stress and lifetime. In addition, this project proposes IPOP TL IDCs for balancing and minimizing input capacitors' currents, which would thus prolong capacitors' lifetime or reduce capacitors' size. Published papers related to this chapter are J1, J2, C2, and C3.

Chapter 3 illustrates that the proposed PSM strategy is utilized for TL-IDCs with asymmetrical modulation strategy. There exists power devices' current imbalance issue in TL-IDCs with asymmetrical modulation strategy, which would lead

unbalanced power loss and thermal stress of power devices. Accordingly, the proposed PSM strategy is utilized for these TL-IDCs to eliminate such current imbalance. Through using proposed strategy, power devices' power loss and thermal stress would be balanced, which would thus increase the converter's reliability. Published paper related to this chapter is J3.

Chapter 4 introduces a new DPS control strategy for FB diode-clamped TL DC/DC converter. Because conventional control strategies causes the high *dv/dt* on isolated transformer, a new DPS strategy is proposed in this project to decrease *dv/dt* on transformer through generating multi-level voltage. Therefore, the proposed control strategy would decrease *dv/dt* and stress on transformer and is helpful for converter's EMI. Published paper related to this chapter is C1.

Chapter 5 concludes the works of this thesis and introduces future works.

1.5. LIST OF PUBLICATIONS

A list of publications is given below. There are three published journal papers and three published conference papers related to this thesis. Three journal papers are marked as J1 ~ J3 and three conference papers are marked as C1 ~ C3.

Journal papers:

J1. **D. Liu**, F. Deng, Z. Gong, and Z. Chen, "Input-parallel output-parallel (IPOP) three-level (TL) DC/DC converters with interleaving control strategy for minimizing and balancing capacitor ripple currents," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 3, pp. 1122-1132, Sep. 2017.

J2. **D. Liu**, F. Deng, Q. Zhang, and Z. Chen, "Zero-voltage switching PWM strategy based capacitor current-balancing control for half-bridge three-level DC/DC converter", in *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 357-369, Jan. 2018.

J3. **D. Liu**, F. Deng, Q. Zhang, and Z. Chen, "Periodically swapping modulation (PSM) strategy for three-level (TL) DC/DC converters with balanced switch currents", in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 412-423, Jan. 2018.

Conference papers:

C1. **D.Liu**, F. Deng, Z. Gong, and Z, Chen, "A double phase-shift control strategy for a full-bridge three-level DC/DC converter", in 42nd Annual Conference of the IEEE Industrial Electronics Society (IECON), Florence, Italy, 2016.

C2. **D.Liu**, F. Deng, Q. Zhang, Z. Gong, and Z, Chen, "Input-parallel output-parallel (IPOP) three-level (TL) DC/DC converters with minimized capacitor ripple currents", in IEEE Annual Southern Power Electronics Conference (SPEC), Auckland, New Zealand, 2016.

C3. **D.Liu**, F. Deng, and Z, Chen, "A ZVS PWM control strategy with balanced capacitor current for half-bridge three-level DC/DC converter", in 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, USA, 2017.

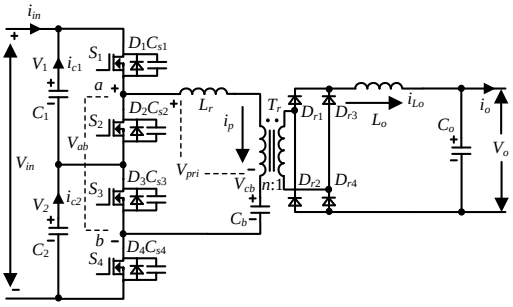
CHAPTER 2. IMPROVING INPUT CAPCITOR PERFORMANCES

This chapter aims at improving input capacitor performances of TL-IDCs. Firstly, a ZVS control strategy including a PSM strategy for FS-HBTL isolated DC/DC converter is proposed to balance input capacitors' currents. Additionally, IPOP TL IDCs are proposed to balance and decrease input capacitors' currents. Finally, summary is given.

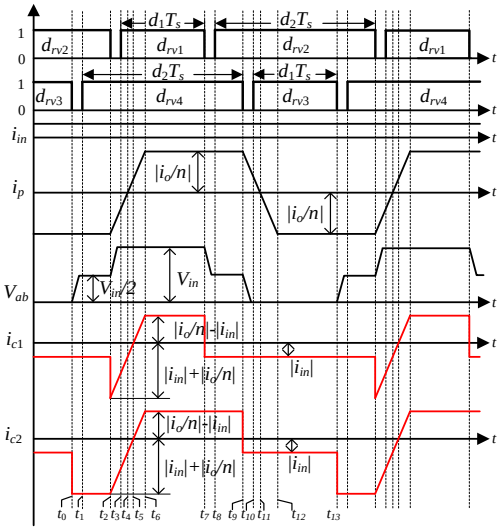
2.1. ZVS CONTROL STRATEGY WITH BALANCED INPUT CAPACITOR CURRENT

2.1.1. INPUT CAPACITOR CURRENT IMBALANCE ISSUE

Figure 2-1(a) presents the FS-HBTL isolated DC/DC converter [75]. In Figure 2-1(a), V_{in} is input voltage; C_1 and C_2 are two input capacitors to split V_{in} into two voltages V_1 and V_2; S_1 - S_4 are power switches; D_1 - D_4 are power diodes; T_r is isolated transformer; L_r is leakage inductor of T_r; C_{s1} - C_{s4} are parasitic capacitors of S_1 - S_4; C_b is DC-blocking capacitor; D_{r1} - D_{r4} are four rectifier diodes; L_o is filter inductor; and C_o is filter capacitor. Additionally, the input current is i_i; currents flowing through C_1 and C_2 are i_{c1} and i_{c2}; primary voltage and current on T_r are V_{pri} and i_p; the current through L_o is i_{Lo}; the voltage on C_b is V_{cb}; the output current and voltage are i_o and V_o; voltage from point a to b is V_{ab}; and transformer's turns ratio is n. Figure 2-1(b) presents the operation principle of conventional control strategy [75], in which driving signals for S_1 - S_4 are d_{rv1} - d_{rv4} and d_1, d_2 are duty cycles during one switching time period T_s. Several assumptions are used to simplify following analysis: 1) L_o is regarded as a constant current source; 2) S_1 - S_4 are considered to be ideal, so impacts from parasitic capacitors can be ignored; 3) i_{in} is regarded to be constant because of impact from total inductance of input power supply plus input line on i_{in}.



(a)



(b)

Figure 2-1 (a) Circuit structure. (b) Conventional control strategy [75].

Based on Figure 2-1(b), the expression of i_{c1} and i_{c2} can be given as

$$i_{c1}=\begin{cases}-i_{in} & t_0\le t<t_2\\ i_p-i_{in} & t_2\le t<t_7\\ -i_{in} & t_7\le t<t_{13}\end{cases} \tag{2.1}$$

$$i_{c2}=\begin{cases}i_p-i_{in} & t_0\le t<t_9\\ -i_{in} & t_9\le t<t_{13}\end{cases} \tag{2.2}$$

In addition, the expression of i_p can be given as

$$i_p=\begin{cases}-\dfrac{i_o}{n} & t_0\le t<t_2\\ -\dfrac{i_o}{n}+\dfrac{V_{in}}{2\cdot L_r}\cdot(t-t_2) & t_2\le t<t_6\\ \dfrac{i_o}{n} & t_6\le t<t_9\\ \dfrac{i_o}{n}-\dfrac{V_{in}}{2\cdot L_r}\cdot(t-t_9) & t_9\le t<t_{12}\\ -\dfrac{i_o}{n} & t_{12}\le t<t_{13}\end{cases} \tag{2.3}$$

Substituting (2.3) into (2.1) and (2.2), i_{c1} and i_{c2} can be rewritten as

$$i_{c1}=\begin{cases}-i_{in} & t_0 \le t < t_2 \\ \dfrac{V_{in}}{2\cdot L_r}\cdot(t-t_2)-\dfrac{i_o}{n}-i_{in} & t_2 \le t < t_6 \\ \dfrac{i_o}{n}-i_{in} & t_6 \le t < t_7 \\ -i_{in} & t_7 \le t < t_{13}\end{cases} \tag{2.4}$$

$$i_{c2}=\begin{cases}-\dfrac{i_o}{n}-i_{in} & t_0 \le t < t_2 \\ \dfrac{V_{in}}{2\cdot L_r}\cdot(t-t_2)-\dfrac{i_o}{n}-i_{in} & t_2 \le t < t_6 \\ \dfrac{i_o}{n}-i_{in} & t_6 \le t < t_9 \\ -i_{in} & t_9 \le t < t_{13}\end{cases} \tag{2.5}$$

Time periods [t_2-t_6] and [t_9-t_{12}] in Figure 2-1(b) are the same and obtained by

$$t_6-t_2=t_{12}-t_9=\frac{4\cdot L_r\cdot i_o}{n\cdot V_{in}} \tag{2.6}$$

Based on (2.4) ~ (2.6), under conventional control strategy, root-mean-square (RMS) value of i_{c1}, i_{c2} named $i_{c1\_rms\_con}$, $i_{c2\_rms\_con}$ are obtained by (2.7) and (2.8).

$$i_{c1\_rms\_con}=\sqrt{{i_{in}}^2+\frac{{i_o}^2\cdot d_1}{n^2}+\frac{8\cdot L_r\cdot i_{in}\cdot {i_o}^2}{n^2\cdot V_{in}\cdot T_s}-\frac{2\cdot i_{in}\cdot i_o\cdot d_1}{n}-\frac{8\cdot L_r\cdot {i_o}^3}{3\cdot n^3\cdot V_{in}\cdot T_s}} \tag{2.7}$$

$$i_{c2\_rms\_con}=\sqrt{{i_{in}}^2+\frac{{i_o}^2\cdot d_2}{n^2}+\frac{8\cdot L_r\cdot i_{in}\cdot {i_o}^2}{n^2\cdot V_{in}\cdot T_s}-\frac{2\cdot i_{in}\cdot i_o\cdot d_1}{n}-\frac{8\cdot L_r\cdot {i_o}^3}{3\cdot n^3\cdot V_{in}\cdot T_s}} \tag{2.8}$$

Based on (2.7) and (2.8), the deviation between $i_{c1\_rms\_con}$, $i_{c2\_rms\_con}$ named $\Delta i_{c\_rms\_con}$ is (2.9).

$$\Delta i_{c\_rms\_con}=\left|i_{c1\_rms\_con}-i_{c2\_rms\_con}\right|=\frac{{i_o}^2\cdot(d_2-d_1)}{n^2\cdot\left(i_{c1\_rms\_con}+i_{c2\_rms\_con}\right)} \tag{2.9}$$

In (2.7) and (2.8), $i_{c1\_rms\_con}$ and $i_{c2\_rms\_con}$ are imbalanced.

2.1.2. ZVS CONTROL STRATEGY

Figure 2-2 presents proposed ZVS strategy for FS-HBTL isolated DC/DC converter. In Figure 2-2, d_{rv1}-d_{rv4} are driving signals for S_1-S_4; d_1 is duty cycle in one switching time period; and d_{loss} is duty cycle loss.

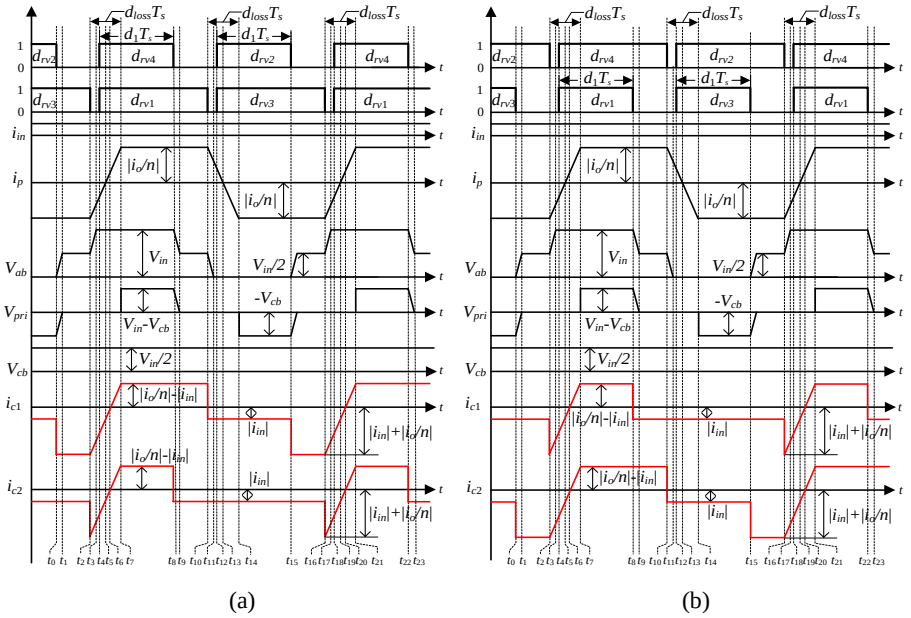


Figure 2-2 Proposed ZVS strategy. (a) Operation mode I. (b) Operation mode II.

Under operation mode I, duty cycle of d_{rv1}, d_{rv3} are 0.5, and duty cycle of d_{rv2}, d_{rv4} are d_1. Contrarily, under operation mode II, duty cycle of d_{rv2}, d_{rv4} are 0.5, and duty cycle of d_{rv1}, d_{rv3} are d_1. d_1 should be smaller than 0.5. From Figure 2-2, it can be seen that i_{c1} and i_{c2} in two operation modes are just opposite. Furthermore, i_{c1} is bigger than i_{c2} under operation mode I, contrarily i_{c2} is bigger than i_{c1} under operation mode II. Therefore, major difference between two operation modes is two input capacitors' currents.

2.1.3. PSM STRATEGY

Based on major difference of two operation modes, a PSM strategy is proposed to balance i_{c1} and i_{c2} through swapping two proposed operation modes in each switch time period (presented in Figure 2-3). Under proposed PSM strategy, operation mode I is utilized during first switching time period, and operation mode II is utilized during second switching time period. Therefore, proposed PSM strategy would balance i_{c1} and i_{c2} during every two switching time periods.

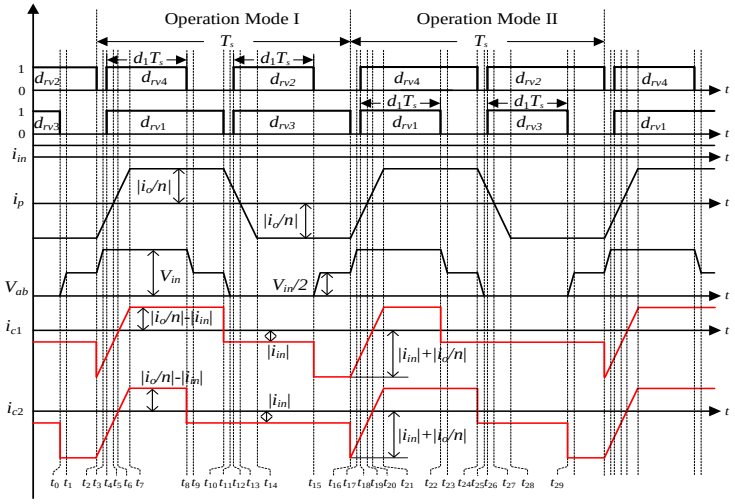


Figure 2-3 Proposed PSM strategy [100].

In Figure 2-3, i_{c1} and i_{c2} can be given as (2.10) and (2.11); i_p can be given as (2.12).

$$i_{c1}=\begin{cases} -i_{in} & t_0 \le t < t_2 \\ i_p - i_{in} & t_2 \le t < t_{10} \\ -i_{in} & t_{10} \le t < t_{15} \\ i_p - i_{in} & t_{15} \le t < t_{22} \\ -i_{in} & t_{22} \le t < t_{29} \end{cases} \tag{2.10}$$

$$i_{c2}=\begin{cases} i_p - i_{in} & t_0 \le t < t_8 \\ -i_{in} & t_8 \le t < t_{16} \\ i_p - i_{in} & t_{16} \le t < t_{24} \\ -i_{in} & t_{24} \le t < t_{29} \end{cases} \tag{2.11}$$

$$i_p=\begin{cases} -\dfrac{i_o}{n} & t_0 \le t < t_2 \\ -\dfrac{i_o}{n}+\dfrac{V_{in}}{2\cdot L_r}\cdot(t-t_2) & t_2 \le t < t_7 \\ \dfrac{i_o}{n} & t_7 \le t < t_{10} \\ \dfrac{i_o}{n}-\dfrac{V_{in}}{2\cdot L_r}\cdot(t-t_2) & t_{10} \le t < t_{14} \\ -\dfrac{i_o}{n} & t_{14} \le t < t_{15} \end{cases} \tag{2.12}$$

i_{c1}, i_{c2} are rewritten as (2.13) by substituting (2.12) into (2.10) and (2.11).

$$i_{c1}=\begin{cases} -i_{in} & t_0 \le t < t_2 \\ \frac{V_{in}}{2\cdot L_r}\cdot(t-t_2)-\frac{i_o}{n}-i_{in} & t_2 \le t < t_7 \\ \frac{i_o}{n}-i_{in} & t_7 \le t < t_{10} \\ -i_{in} & t_{10} \le t < t_{15} \\ -\frac{i_o}{n}-i_{in} & t_{15} \le t < t_{16} \\ \frac{V_{in}}{2\cdot L_r}\cdot(t-t_2)-\frac{i_o}{n}-i_{in} & t_{16} \le t < t_{21} \\ \frac{i_o}{n}-i_{in} & t_{21} \le t < t_{22} \\ -i_{in} & t_{22} \le t < t_{29} \end{cases} \tag{2.13}$$

$$i_{c2}=\begin{cases} -\frac{i_o}{n}-i_{in} & t_0 \le t < t_2 \\ \frac{V_{in}}{2\cdot L_r}\cdot(t-t_2)-\frac{i_o}{n}-i_{in} & t_2 \le t < t_7 \\ \frac{i_o}{n}-i_{in} & t_7 \le t < t_8 \\ -i_{in} & t_8 \le t < t_{16} \\ \frac{V_{in}}{2\cdot L_r}\cdot(t-t_2)-\frac{i_o}{n}-i_{in} & t_{16} \le t < t_{21} \\ \frac{i_o}{n}-i_{in} & t_{21} \le t < t_{24} \\ -i_{in} & t_{24} \le t < t_{29} \end{cases} \tag{2.14}$$

Time periods [t_2 - t_7] and [t_{16} - t_{21}] in Figure 2-3 are the same as (2.15).

$$t_7-t_2=t_{21}-t_{16}=\frac{4\cdot L_r\cdot i_o}{n\cdot V_{in}} \tag{2.15}$$

Based on (2.13) ~ (2.15), RMS value of i_{c1}, i_{c2} under proposed strategy named $i_{c1\_rms\_pro}$, $i_{c2\_rms\_pro}$ are

$$i_{c1\_rms\_pro}=i_{c2\_rms\_pro}=\sqrt{{i_{in}}^2+\frac{{i_o}^2}{2\cdot n^2}+\frac{8\cdot L_r\cdot i_{in}\cdot {i_o}^2}{n^2\cdot V_{in}\cdot T_s}-\frac{2\cdot i_{in}\cdot i_o\cdot d_1}{n}-\frac{8\cdot L_r\cdot {i_o}^3}{3\cdot n^3\cdot V_{in}\cdot T_s}} \tag{2.16}$$

From Table 2-1, it could be obtained that: 1) under conventional strategy, $i_{c1\_rms\_con}$, $i_{c2\_rms\_con}$ are unbalanced, and $i_{c1\_rms\_con}$ is smaller than $i_{c2\_rms\_con}$ because d_2 is higher than d_1 in normal operations; 2) in proposed strategy, $i_{c1\_rms\_pro}$, $i_{c2\_rms\_pro}$ become the same, which means that proposed strategy can eliminate two input capacitors' current imbalance.

By substituting parameters in Table 2-2 into (2.7), (2.8), and (2.16), Figures 2-4 and 2-5 can be obtained. Figure 2-4 presents calculated RMS value of i_{c1}, i_{c2}. Figure 2-5 presents results about deviation $\Delta i_{c\_rms\_con}$ calculated by (2.9).

Tabel 2-1 Calculation formulas about RMS value of i_{c1}, i_{c2}

Control Strategy	RMS Value	Theoretical Calculation Formula
Conventional Control Strategy	$i_{c1\_rms\_con}$	$\sqrt{i_{in}^2+\frac{i_o^2\cdot d_1}{n^2}+\frac{8\cdot L_r\cdot i_{in}\cdot i_o^2}{n^2\cdot V_{in}\cdot T_s}-\frac{2\cdot i_{in}\cdot i_o\cdot d_1}{n}-\frac{8\cdot L_r\cdot i_o^3}{3\cdot n^3\cdot V_{in}\cdot T_s}}$
	$i_{c2\_rms\_con}$	$\sqrt{i_{in}^2+\frac{i_o^2\cdot d_2}{n^2}+\frac{8\cdot L_r\cdot i_{in}\cdot i_o^2}{n^2\cdot V_{in}\cdot T_s}-\frac{2\cdot i_{in}\cdot i_o\cdot d_1}{n}-\frac{8\cdot L_r\cdot i_o^3}{3\cdot n^3\cdot V_{in}\cdot T_s}}$
	$\Delta i_{c\_rms\_con}$	$\frac{i_o^2\cdot(d_2-d_1)}{n^2\cdot(i_{c1\_rms\_con}+i_{c2\_rms\_con})}$
Proposed Control Strategy	$i_{c1\_rms\_pro}$ $i_{c2\_rms\_pro}$	$\sqrt{i_{in}^2+\frac{i_o^2}{2\cdot n^2}+\frac{8\cdot L_r\cdot i_{in}\cdot i_o^2}{n^2\cdot V_{in}\cdot T_s}-\frac{2\cdot i_{in}\cdot i_o\cdot d_1}{n}-\frac{8\cdot L_r\cdot i_o^3}{3\cdot n^3\cdot V_{in}\cdot T_s}}$

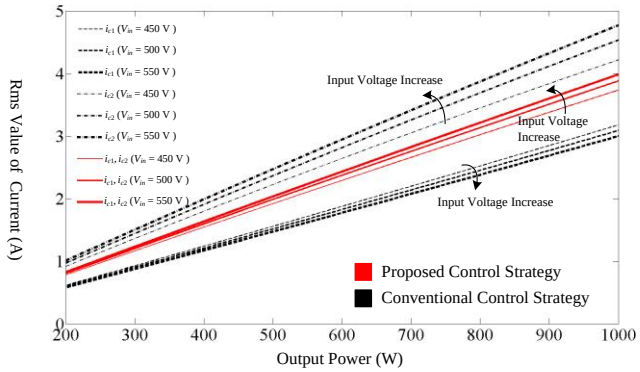


Figure 2-4 Calculated RMS value of i_{c1}, i_{c2} (V_o = 50V).

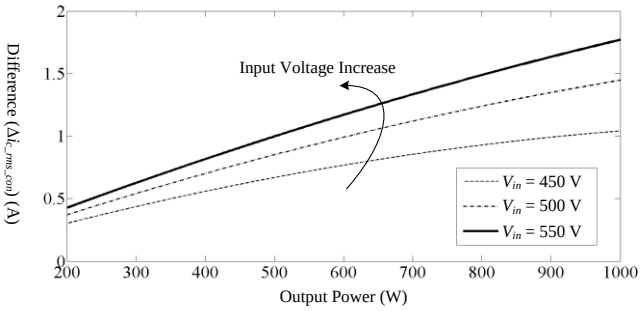
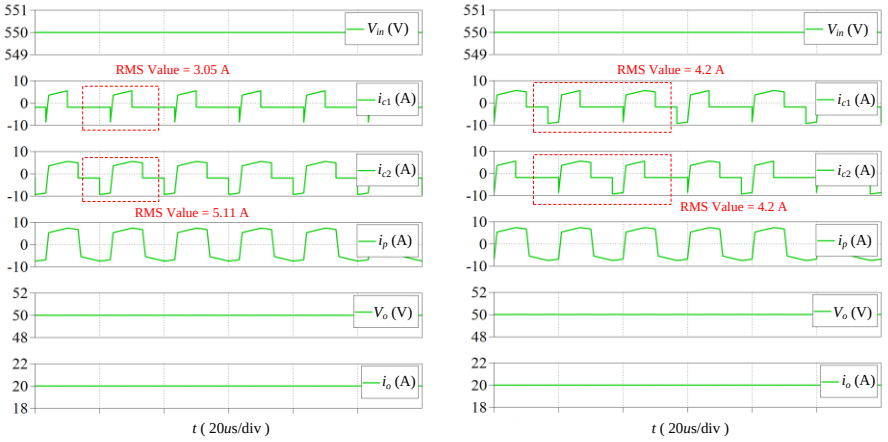


Figure 2-5 Calculated deviations between RMS value of i_{c1}, i_{c2} under the conventional control strategy (Vo = 50V).

2.1.4. SIMULATION AND EXPERIMENTAL VERIFICATION

A. Simulation verification

Table 2-2 presents parameters of simulation model. Figure 2-6 presents simulation results. As marked in Figure 2-6(b), i_{c1}, i_{c2} are same during every two switching time periods under proposed strategy. In Fig. 2-6, $i_{c1\_rms\_con}$, $i_{c2\_rms\_con}$ are 3.05 A and 5.11 A respectively, but $i_{c1\_rms\_pro}$, $i_{c2\_rms\_pro}$ are both 4.2 A.



(a) (b)

Figure 2-6 Simulation results (V_{in} = 550 V, V_o = 50 V, P_o = 1 kW). (a) Conventional strategy. (b) Proposed strategy.

B. Experimental verification

Table 2-2 presents parameters of established prototype; Figure 2-7 presents the hardware of established prototype (1 kW).

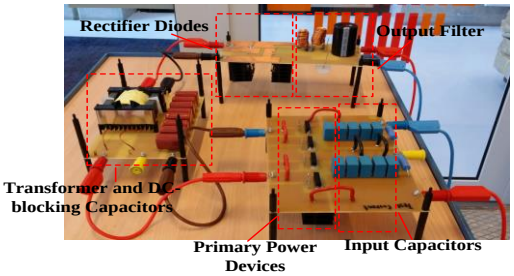


Figure 2-7 Hardware of established prototype.

Tabel 2-2 Parameters of simulation model and experimental prototype

Description	Parameter
Power Switches S_1 - S_4	SPW47N60C3
Rectifier Diodes D_{r1} - D_{r4}	MBR40250TG
Turns Ratio of Transformer T_r	25 : 8
Leakage Inductance L_r (uH)	20.7
Output Filter Capacitor C_o (uF)	470
Output Filter Inductor L_o (uH)	140
Input Capacitors C_1 and C_2 (uF)	14.4
DC-blocking Capacitor C_b (uF)	12
Switching Frequency (kHz)	50
Dead Time (ns)	400
Input Inductance (uH) (Including the output inductance of the input power supply and inductance of the input line)	60

Figure 2-8 illustrates control block of proposed strategy.

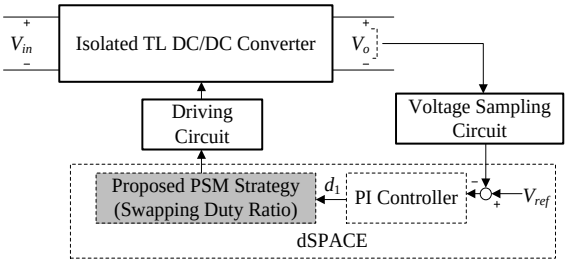
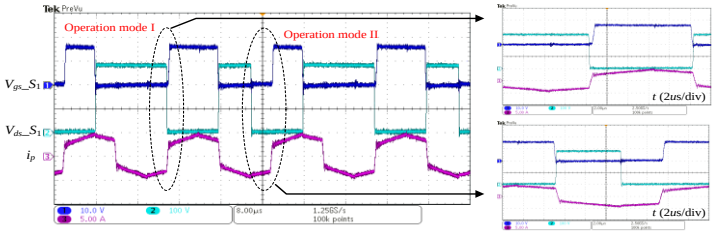
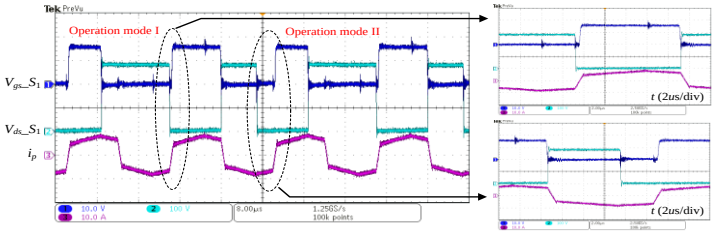


Figure 2-8 Control block of proposed PSM strategy.

Figures 2-9 and 2-10 show ZVS achievement performances in proposed control strategy, in which $V_{ds}\_S_1$, $V_{ds}\_S_3$ are drain-source voltage of S_1, S_3 and $V_{gs}\_S_1$, $V_{gs}\_S_3$ are driving signal of S_1, S_3.

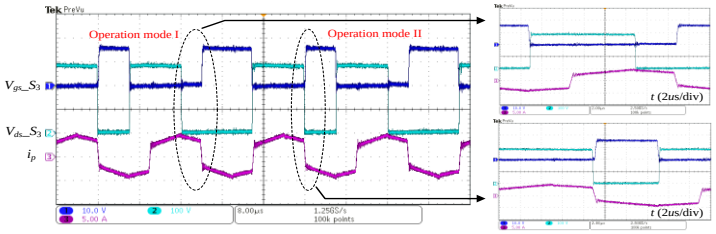


(a)

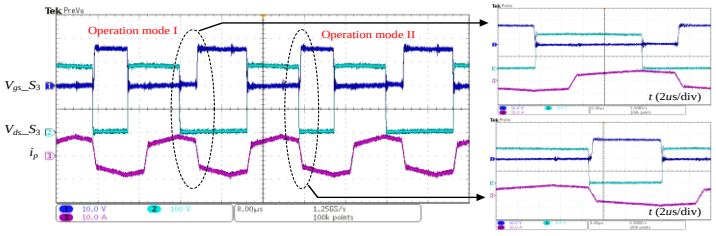


(b)

Figure 2-9 ZVS performance of S_1 (V_{in} = 550 V, V_o = 50 V). (a) P_o = 500 W. (b) P_o = 1 kW.



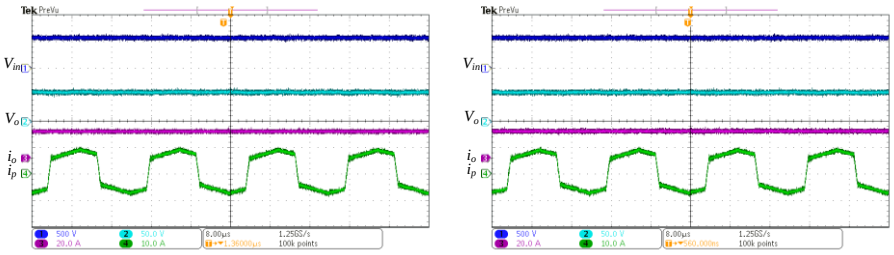
(a)



(b)

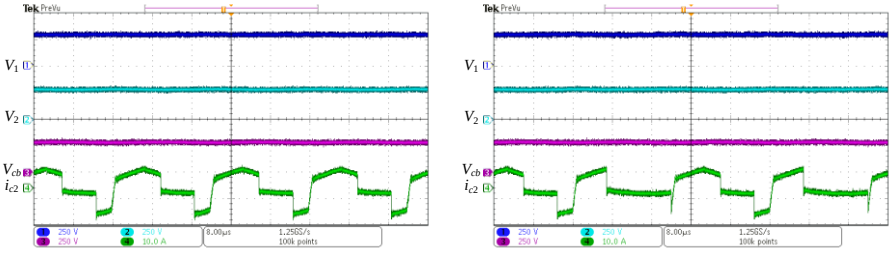
Figure 2-10 ZVS performance of S_3 (V_{in} = 550 V, V_o = 50 V). (a) P_o = 500 W. (b) P_o = 1 kW.

Figures 2-11 ~ 2-13 present experimental results. In Figure 2-13 (P_o = 1 kW), $i_{c1\_rms\_con}$, $i_{c2\_rms\_con}$ are 3.16 A and 5.18 A respectively; $\Delta i_{c\_rms\_con}$ 2.02 A; but $i_{c1\_rms\_pro}$, $i_{c2\_rms\_pro}$ are both 4.37 A, which validates that proposed PSM strategy can eliminate current imbalance among input capacitors caused by conventional strategy.



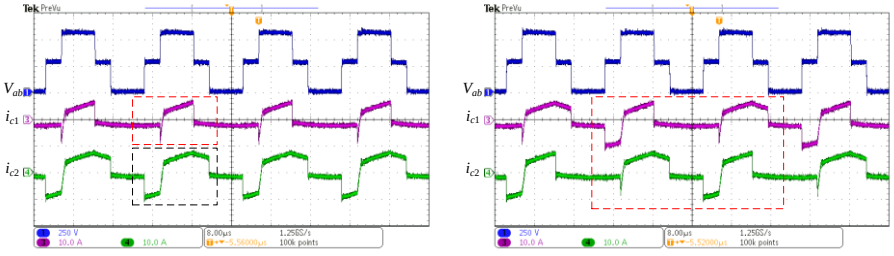
(a) (b)

Figure 2-11 Experimental results of V_{in}, V_o, i_o, and i_p (V_{in} = 550 V, V_o = 50V, P_o = 1 kW) [100]. (a) Conventional strategy. (b) Proposed strategy.



(a) (b)

Figure 2-12 Experimental results of V_1, V_2, V_{cb}, and i_{c2} (V_{in} = 550 V, V_o = 50V, P_o = 1 kW) [100]. (a) Conventional strategy. (b) Proposed strategy.



(a) (b)

Figure 2-13 Experimental results of V_{ab}, i_{c1}, and i_{c2} (V_{in} = 550 V, V_o = 50V, P_o = 1 kW) [100]. (a) Conventional strategy. (b) Proposed strategy.

Figure 2-14 demonstrates experimental RMS value about i_{c1}, i_{c2}.

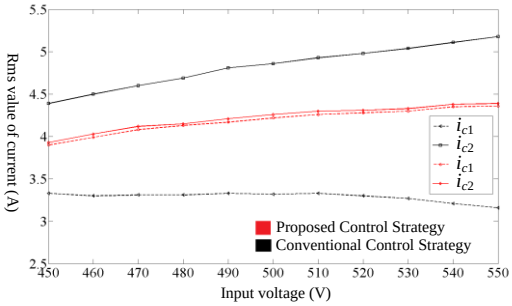


Figure 2-14 Experimental RMS value of i_{c1}, i_{c2} (V_o = 50 V, P_o = 1 kW).

Figure 2-15 presnets the dynamic performance.

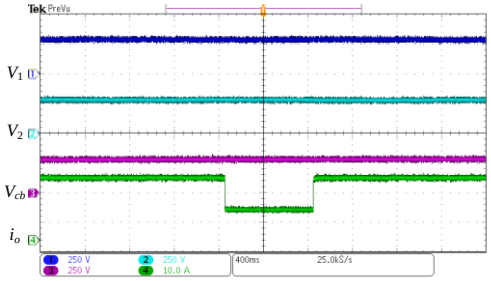


Figure 2-15 Dynamic performances under load changes (1 kW to 500 W to 1 kW) (V_{in} = 550 V V_o = 50 V).

Figure 2-16 presents experimental efficiency results. It is noted that the efficiency results are calculated by (measured V_o × measured i_o) / (measured V_{in} × measured i_{in}).

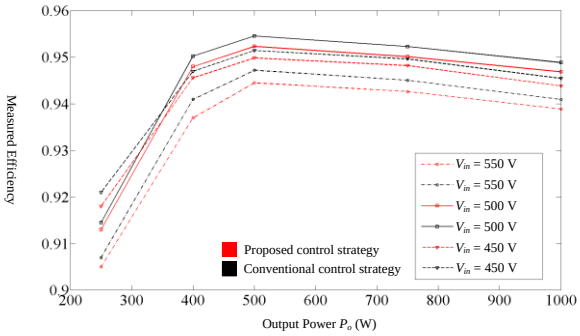


Figure 2-16 Experimental efficiency results (V_o = 50 V).

2.2. IPOP TL ISOLATED DC/DC CONVERTERS

2.2.1. CIRCUIT STRUCTURE

Figure 2-17 presents the IPOP TL IDCs including dual FS-HBTL IDCs (named Module I and Module II). In Figure 2-17, V_{in} is input voltage; C_1 and C_2 are input capacitors to split V_{in} into two voltages V_1 and V_2; and C_o is filter capacitor. In Module I, S_1-S_4 are power switches; D_1-D_4 are power diodes; T_{r1} is isolated transformer; L_{r1} is leakage inductance of T_{r1}; C_{b1} is DC-blocking capacitor; D_{r1}-D_{r4} are four rectifier diodes; L_{o1} is filter inductor. Module II is the same as Module I. In Figure 2-17, i_{in} is input current; current through C_1 and C_2 are i_{c1} and i_{c2} respectively; primary current of T_{r1} and T_{r2} are i_{p1} and i_{p2}; current on L_{o1} and L_{o2} are i_{Lo1} and i_{Lo2}; voltage on C_{b1} and C_{b2} are V_{cb1} and V_{cb2}; output voltage and current are V_o and i_o; voltage from point a to b is V_{ab}; the voltage from point c to d is V_{cd}; turns ratios in T_{r1} and T_{r2} are n_1 and n_2.

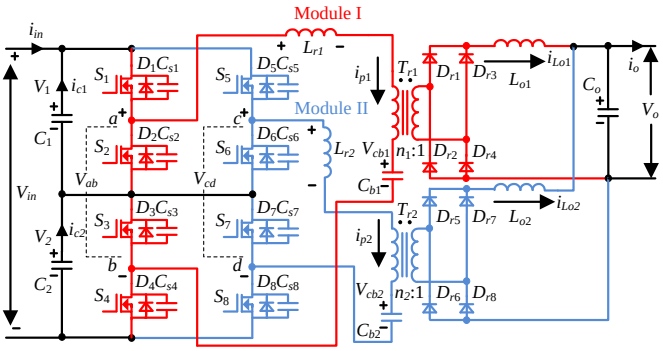
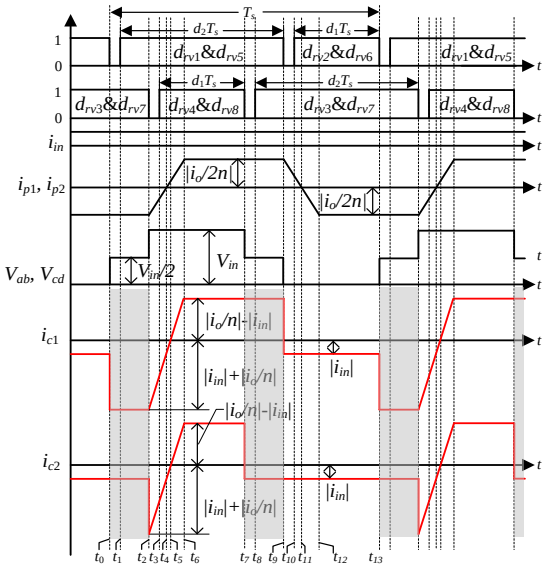


Figure 2-17 Circuit structure.

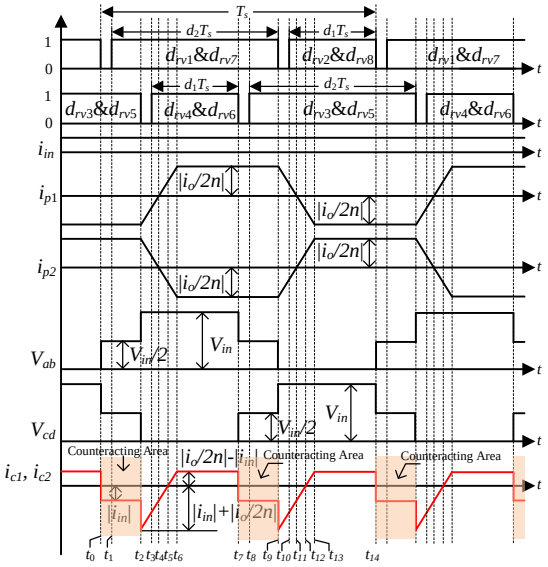
2.2.2. WORKING PRINCIPLE

Some assumptions are used to simplify following analysis: 1) L_{o1} and L_{o2} are the same and regarded as constant current sources; 2) S_1 - S_8 and D_1 - D_8 are ideal; 3) C_1, C_2, C_{b1}, and C_{b2} are regarded as constant voltage sources and $C_1 = C_2 = C_{in}$, $C_{b1} = C_{b2} = C_b$, $V_1 = V_2 = V_{in}/2$, $V_{cb1} = V_{cb2} = V_{cb} = V_{in}/2$; 4) the parameters of T_{r1} and T_{r2} are identical: $n_1 = n_2 = n$ and $L_{r1} = L_{r2} = L_r$; 5) i_{in} is regarded to be constant because of impact from inductance (input power supply's output inductance plus input line inductance) on i_{in}.

Figure 2-18 presents working principle of proposed converters. In Figure 18, d_{rv1}-d_{rv8} are driving signals for S_1-S_8, d_1-d_2 are duty cycles during one switching time period. As drawn by color in Figure 2-18(a), i_{c1} and i_{c2} are unbalanced without interleaving control strategy. On contrary, under interleaving control strategy, i_{c1} and i_{c2} become much smaller and balanced.



(a)



(b)

Figure 2-18 (a) Without interleaving control strategy. (b) With interleaving control strategy. [101]

Equivalent circuits are presented in Figure 2-19 to explain proposed converters' working process.

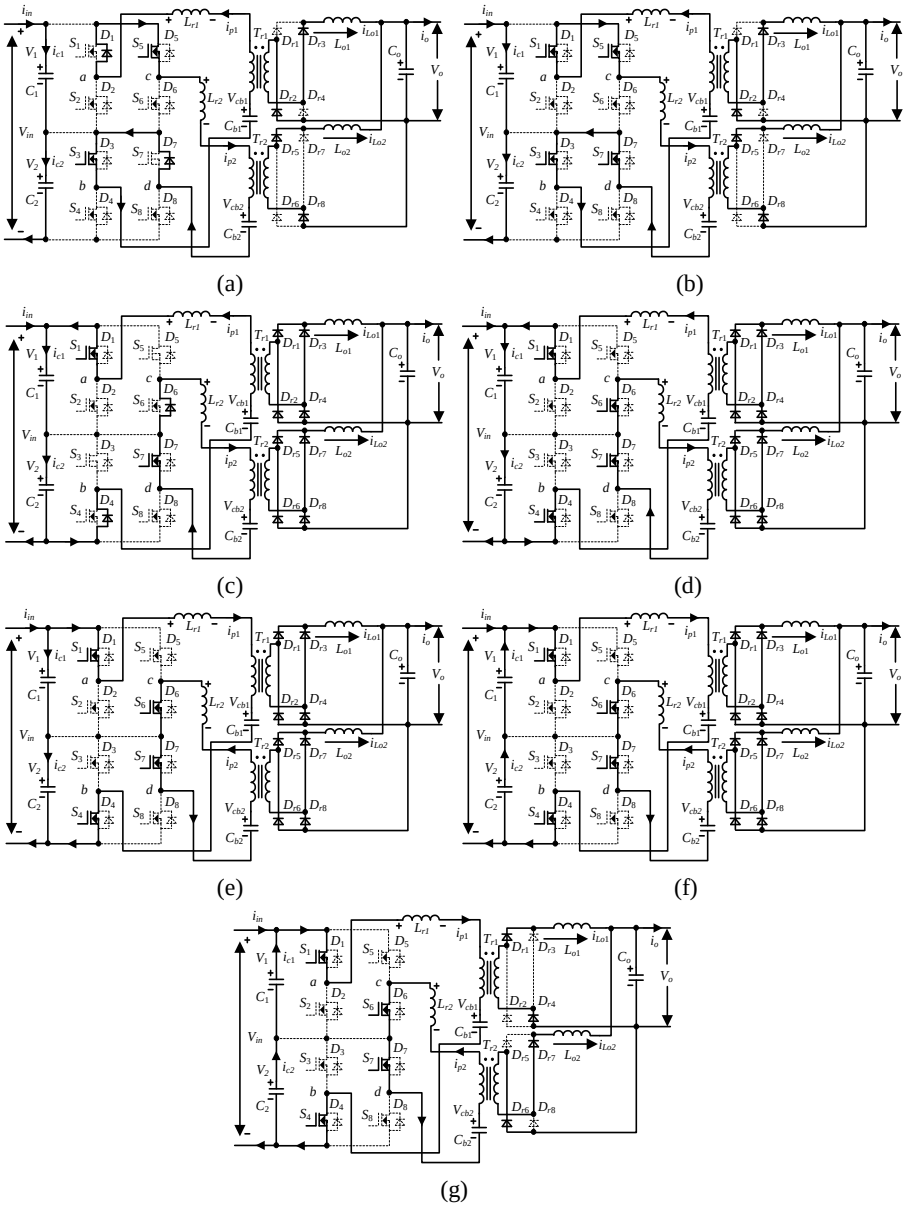


Figure 2-19 Equivalent circuits with interleaving control strategy [101]. (a) [t_0-t_1]. (b) [t_1-t_2]. (c) [t_2-t_3]. (d) [t_3-t_4]. (e) [t_4-t_5]. (f) [t_5-t_6]. (g) [t_6-t_7].

2.2.3. CURRENTS ON INPUT CAPACITORS

Based on Figure 2-18(b), i_{c1} and i_{c2} can be expressed as

$$i_{c1} = i_{c2} = \begin{cases} -i_{in} & t_0 \le t < t_2 \\ i_{p1} - i_{in} & t_2 \le t < t_7 \end{cases} \tag{2.17}$$

i_{p1} and i_{p2} are given as

$$i_{p1} = -i_{p2} = \begin{cases} -\dfrac{i_o}{2 \cdot n} & t_0 \le t < t_2 \\ -\dfrac{i_o}{2 \cdot n} + \dfrac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) & t_2 \le t < t_6 \\ \dfrac{i_o}{2 \cdot n} & t_6 \le t < t_7 \end{cases} \tag{2.18}$$

Substituting (2.18) into (2.17), i_{c1} and i_{c2} are rewritten by

$$i_{c1} = i_{c2} = \begin{cases} -i_{in} & t_0 \le t < t_2 \\ \dfrac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) - \dfrac{i_o}{2 \cdot n} - i_{in} & t_2 \le t < t_6 \\ \dfrac{i_o}{2 \cdot n} - i_{in} & t_6 \le t < t_7 \end{cases} \tag{2.19}$$

Time periods [t_2-t_6] and [t_9-t_{13}] in Figure 2-18(b) are the same and can be obtained by

$$t_6 - t_2 = t_{13} - t_9 = \frac{2 \cdot L_r \cdot i_o}{n \cdot V_{in}} \tag{2.20}$$

According to (2.19) and (2.20), RMS value of i_{c1}, i_{c2} under interleaving control strategy named $i_{c1\_rms\_II}$, $i_{c2\_rms\_II}$ are

$$i_{c1\_rms\_II} = i_{c2\_rms\_II} = \sqrt{{i_{in}}^2 + \frac{{i_o}^2 \cdot d_1}{2 \cdot n^2} + \frac{4 \cdot L_r \cdot i_{in} \cdot {i_o}^2}{n^2 \cdot V_{in} \cdot T_s} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n} - \frac{2 \cdot L_r \cdot {i_o}^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}} \tag{2.21}$$

RMS value of i_{c1}, i_{c2} without interleaving control strategy presented in Figure 2-18(a) named $i_{c1\_rms\_I}$, $i_{c2\_rms\_I}$ are

$$i_{c1\_rms\_I} = \sqrt{i_{in}^{\ 2} + \frac{i_o^{\ 2} \cdot d_2}{n^2} + \frac{4 \cdot L_r \cdot i_{in} \cdot i_o^{\ 2}}{n^2 \cdot V_{in} \cdot T_s} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n} - \frac{4 \cdot L_r \cdot i_o^{\ 3}}{3 \cdot n^3 \cdot V_{in} \cdot T_s}} \tag{2.22}$$

$$i_{c2\_rms\_I} = \sqrt{i_{in}^{\ 2} + \frac{i_o^{\ 2} \cdot d_1}{n^2} + \frac{4 \cdot L_r \cdot i_{in} \cdot i_o^{\ 2}}{n^2 \cdot V_{in} \cdot T_s} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n} - \frac{4 \cdot L_r \cdot i_o^{\ 3}}{3 \cdot n^3 \cdot V_{in} \cdot T_s}} \tag{2.23}$$

Based on (2.22) and (2.23), deviation between $i_{c1\_rms\_I}$, $i_{c2\_rms\_I}$ named $\Delta i_{c\_rms\_I}$ is

$$\Delta i_{c\_rms\_I} = i_{c1\_rms\_I} - i_{c2\_rms\_I} = \frac{i_o^{\ 2} \cdot (d_2 - d_1)}{n^2 \cdot (i_{c1\_rms\_I} + i_{c2\_rms\_I})} \tag{2.24}$$

Tabel 2-3 Calculation formulas about RMS value of i_{c1}, i_{c2}

Control Strategy	**RMS Value**	**Theoretical Calculation Formula**
Without the interleaving control strategy	$i_{c1\_rms\_I}$	$\sqrt{i_{in}^{\ 2} + \frac{i_o^{\ 2} \cdot d_2}{n^2} + \frac{4 \cdot L_r \cdot i_{in} \cdot i_o^{\ 2}}{n^2 \cdot V_{in} \cdot T_s} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n} - \frac{4 \cdot L_r \cdot i_o^{\ 3}}{3 \cdot n^3 \cdot V_{in} \cdot T_s}}$
	$i_{c2\_rms\_I}$	$\sqrt{i_{in}^{\ 2} + \frac{i_o^{\ 2} \cdot d_1}{n^2} + \frac{4 \cdot L_r \cdot i_{in} \cdot i_o^{\ 2}}{n^2 \cdot V_{in} \cdot T_s} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n} - \frac{4 \cdot L_r \cdot i_o^{\ 3}}{3 \cdot n^3 \cdot V_{in} \cdot T_s}}$
	$\Delta i_{c\_rms\_I}$	$\frac{i_o^{\ 2} \cdot (d_2 - d_1)}{n^2 \cdot (i_{c1\_rms\_I} + i_{c2\_rms\_I})}$
With the interleaving control strategy	$i_{c1\_rms\_II}$, $i_{c2\_rms\_II}$	$\sqrt{i_{in}^{\ 2} + \frac{i_o^{\ 2} \cdot d_1}{2 \cdot n^2} + \frac{4 \cdot L_r \cdot i_{in} \cdot i_o^{\ 2}}{n^2 \cdot V_{in} \cdot T_s} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n} - \frac{2 \cdot L_r \cdot i_o^{\ 3}}{3 \cdot n^3 \cdot V_{in} \cdot T_s}}$

Through substituting parameters in Table 2-4 to calculation formulas in Table 2-3, calculation results of $i_{c1\_rms\_I}$, $i_{c2\_rms\_I}$, $i_{c1\_rms\_II}$, and $i_{c2\_rms\_II}$ are obtained in Figure 2-20. Fig. 2-20 demonstrates that: 1) $i_{c1\_rms\_I}$, $i_{c2\_rms\_I}$ are different, but $i_{c1\_rms\_II}$, $i_{c2\_rms\_II}$ are same; and 2) $i_{c1\_rms\_II}$, $i_{c2\_rms\_II}$ are much smaller than $i_{c1\_rms\_I}$, $i_{c2\_rms\_I}$.

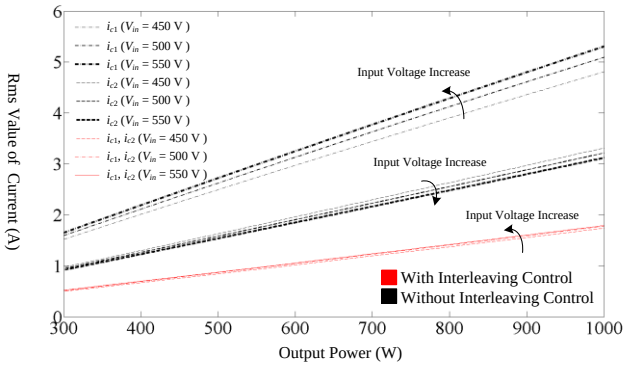
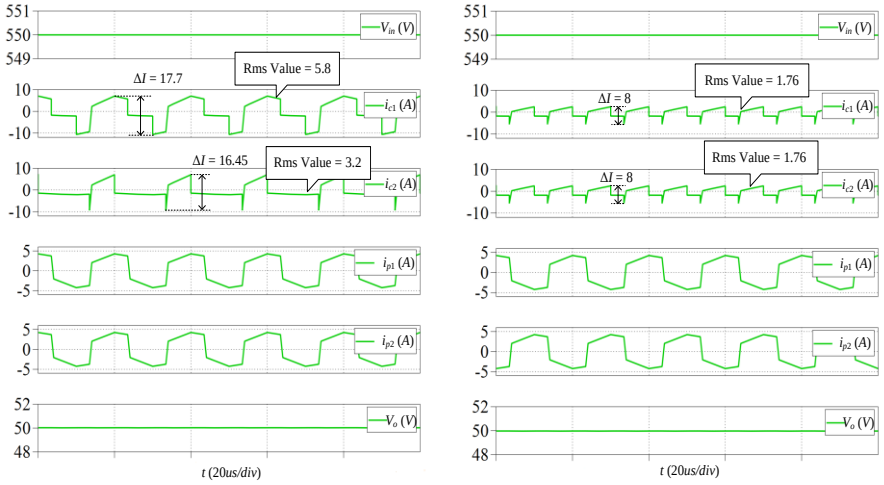


Figure 2-20 Calculation results about RMS value of i_{c1}, i_{c2} (V_o = 50 V).

2.2.4. SIMULATION AND EXPERIMENTAL VERIFICATION

A. Simulation verification

Table 2-4 presents parameters of simulation model. Figure 2-21 presents simulation results, in which 1) $i_{c1\_rms\_I}$, $i_{c2\_rms\_I}$ are 5.8 A and 3.2 A respectively; and 2) $i_{c1\_rms\_II}$, $i_{c2\_rms\_II}$ become the same and decrease to both 1.76 A. Therefore, simulation results verify that i_{c1}, i_{c2} can be effectively balanced and greatly decreased.



(a) (b)

Figure 2-21 Simulation results (V_{in} = 550 V, V_o = 50 V, and P_o = 1 kW). (a) Without interleaving control strategy. (b) With interleaving control strategy. [101]

B. Experimental verification

Table 2-4 presents parameters of established prototype. Figure 2-22 presents built prototype's hardware.

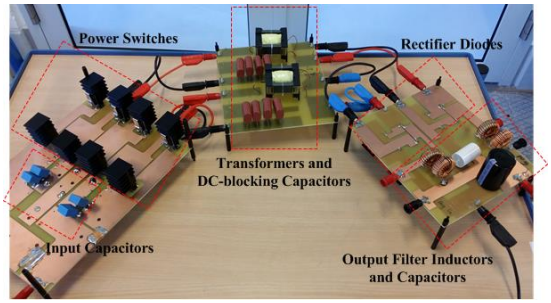
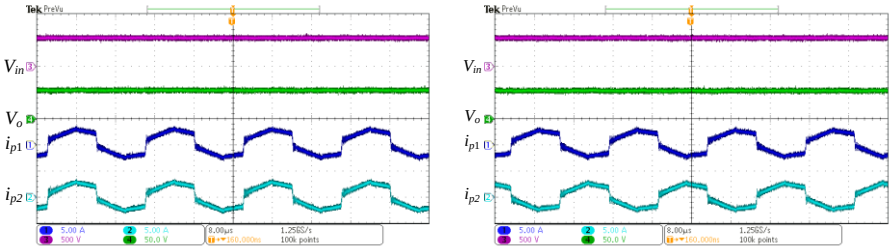


Figure 2-22 Hardware of established prototype.

Tabel 2-4 Parameters in simulation and experiments

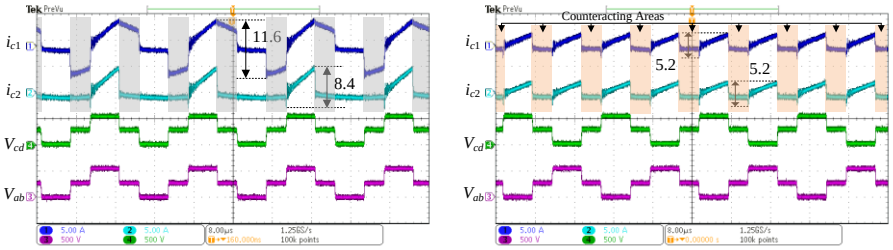
Description	Parameter
Power switches S_1 - S_8	SPW47N60C3
Rectifier diodes D_{r1} - D_{r8}	MBR20200CTG
Turns Ratios of T_{r1} and T_{r2}	38 : 13
Leakage Inductances L_{r1} and L_{r2} (uH)	30
Output Filter Capacitor C_o (uF)	470
Output Filter Inductors L_{o1} and L_{o2} (uH)	100
Input Capacitors C_1 and C_2 (uF)	14.4
DC-blocking Capacitors C_{b1} and C_{b2} (uF)	6
Switching Frequency (kHz)	50
Dead Time (ns)	400

Figures 2-23 ~ 2-26 show experimental results.



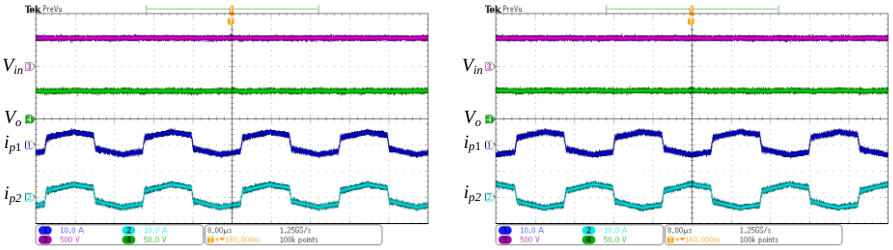
(a) (b)

Figure 2-23 Experimental results of V_{in}, V_o, i_{p1}, and i_{p2} under 500 W (V_{in} =550 V, V_o = 50 V) [101]. (a) Without interleaving control strategy. (b) With interleaving control strategy.



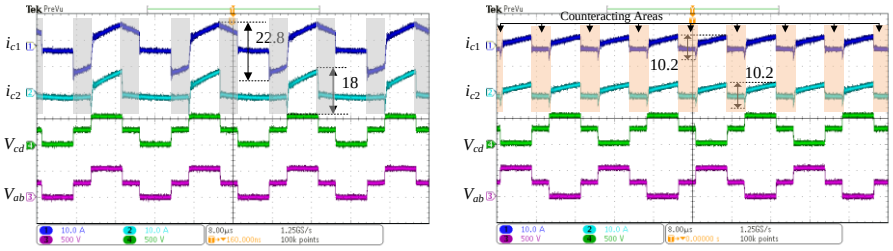
(a) (b)

Figure 2-24 Experimental results of i_{c1}, i_{c2}, V_{ab}, and V_{cd} under 500 W (V_{in} =550 V, V_o = 50 V) [101]. (a) Without interleaving control strategy. (b) With interleaving control strategy.



(a) (b)

Figure 2-25 Experimental results of V_{in}, V_o, i_{p1}, and i_{p2} under 1 kW (V_{in} =550 V, V_o = 50 V) [101]. (a) Without interleaving control strategy. (b) With interleaving control strategy.



(a) (b)

Figure 2-26 Experimental results of i_{c1}, i_{c2}, V_{ab}, and V_{cd} under 1 kW (V_{in} =550 V, V_o = 50 V) [101]. (a) Without interleaving control strategy. (b) With interleaving control strategy.

When P_o is 500 W in Figure 2-24, $i_{c1\_rms\_I}$, $i_{c2\_rms\_I}$ are 3.2 A and 1.68 A respectively; contrarily $i_{c1\_rms\_II}$, $i_{c2\_rms\_II}$ are almost the same and decrease to 0.978 A and 0.971 A respectively. When P_o is 1 kW in Figure 2-26, $i_{c1\_rms\_I}$, $i_{c2\_rms\_I}$ are 5.6 A and 3.19 A, so deviation between them is 2.41 A; contrarily $i_{c1\_rms\_II}$, $i_{c2\_rms\_II}$ are almost same and reduce to 1.69 A and 1.68 A respectively.

Figure 2-27 presents experimental results and theoretical calculations of RMS value of i_{c1} and i_{c2}, in which the differences between the theoretical calculation and experimental results are very slight.

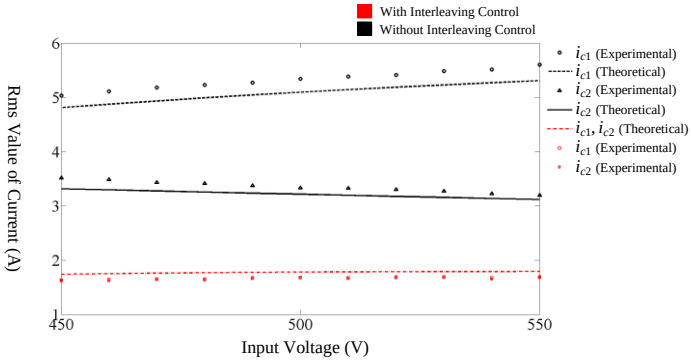


Figure 2-27 RMS value of i_{c1} and i_{c2} (V_o = 50 V and P_o = 1 kW).

2.3. SUMMARY

Firstly, this chapter proposes a ZVS strategy including a PSM strategy for FS-HBTL isolated DC/DC converter to eliminate current imbalance among input capacitors, which can thus balance the two input capacitors' thermal stress and lifetime. Simulation and experimental results both validate proposed ZVS strategy and modulation strategy. The papers related to these contents are J2 and C3.

Secondly, this chapter proposes IPOP TL IDCs to balance and minimize two input capacitors' currents, which can thus 1) reduce input capacitors' size; and 2) balance two input capacitors' thermal stress and lifetime. Simulation and experimental results both validate proposed converters.

The papers related to this chapter are J1 and C2.

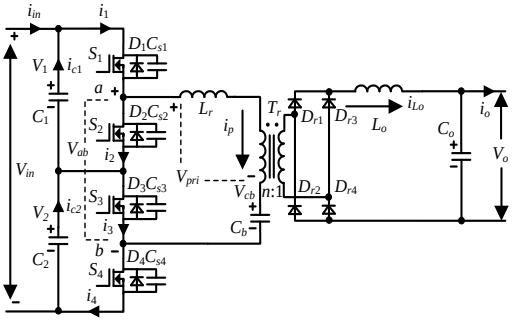
CHAPTER 3. IMPROVING POWER DEVICE PERFORMANCE

This chapter aims at improving power device performance of TL-IDCs. The proposed PSM strategy can be also utilized for TL-IDCs with asymmetrical modulation strategy to balance power devices' currents. This chapter analyzes FS-HBTL isolated DC/DC converter [75] as an instance to illustrate current imbalance issue and power devices' currents under proposed PSM strategy. The analysis about current imbalance issue and working process under proposed PSM strategy of other TL-IDCs [94-96] (mentioned in Section 1.3.2) are similar.

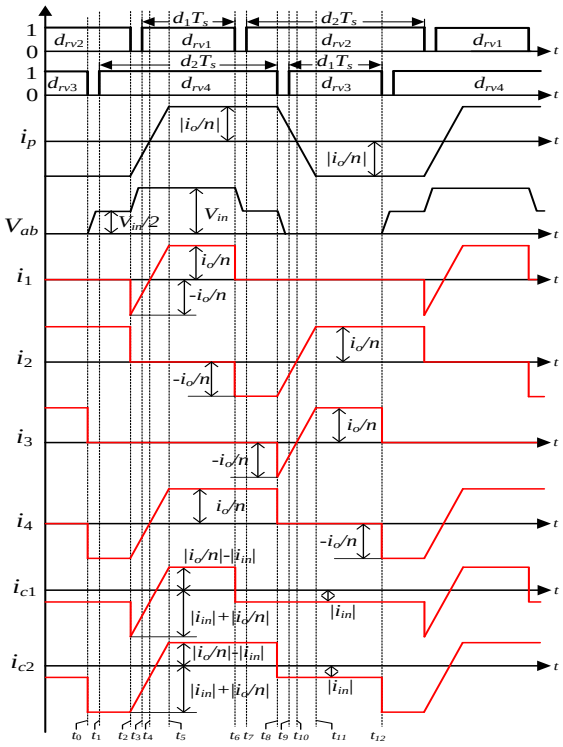
3.1. POWER DEVICE CURRENT IMBALANCE ISSUE

Figure 3-1(a) presents the FS-HBTL isolated DC/DC converter's circuit structure [75] and Figure 3-1(b) presents asymmetrical modulation strategy [75]. In Figure 3-1(a), V_{in} is input voltage; C_1 and C_2 are two input capacitors to split V_{in} into two voltages V_1 and V_2; S_1 - S_4 and D_1 - D_4 are power switches and diodes; T_r is isolated transformer; L_r is the leakage inductance of T_r; C_{s1} - C_{s4} are parasitic capacitors of S_1 - S_4; C_b is the DC-blocking capacitor; D_{r1} - D_{r4} are four output rectifier diodes; L_o is filter inductor; C_o is filter capacitor. In Figure 3-1(a), input current is i_{in}; primary current on T_r is i_p; currents on (S_1, D_1), (S_2, D_2), (S_3, D_3), and (S_4, D_4) are i_1, i_2, i_3, and i_4; the currents on C_1 and C_2 are i_{c1} and i_{c2}; the current on L_o is i_{Lo}; the voltage on C_b is V_{cb}; V_o is output voltage; i_o is output current; voltage from point a to b is V_{ab}; and the turns ratio of T_r is n. In Figure 3-1(b), d_{rv1} - d_{rv4} are driving signals for S_1 - S_4; d_1 and d_2 are duty cycles during one switching time period; d_2 is 1 - d_1 when ignoring dead-time.

Some assumptions are used to simplify following analysis: 1) L_o is regared as a current source; 2) S_1 - S_4 and D_1 - D_4 are ideal; 3) C_1, C_2, and C_b are regarded as constant voltage sources (V_{in}/2).



(a)



(b)

Figure 3-1 (a) Circuit Structure. (b) Asymmetrical modulation strategy [75].

In Figure 3-1(b), current pairs (i_1, i_3) and (i_2, i_4) are same during each switching time period. Therefore, only i_1, i_2 are given as

$$i_1 = \begin{cases} -\frac{i_o}{n} + \frac{V_{in}}{2 \cdot L_r} \cdot t & [t_2 - t_5] \\ \frac{i_o}{n} & [t_5 - t_6] \end{cases} \tag{3.1}$$

$$i_2 = \begin{cases} \frac{i_o}{n} & [t_0 - t_2] \\ -\frac{i_o}{n} & [t_6 - t_8] \\ -\frac{i_o}{n} + \frac{V_{in}}{2 \cdot L_r} \cdot t & [t_8 - t_{11}] \\ \frac{i_o}{n} & [t_{11} - t_{12}] \end{cases} \tag{3.2}$$

Time periods [t_2 - t_5] and [t_8 - t_{11}] are the same and can be calculated by

$$t_5 - t_2 = t_{11} - t_8 = \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in}} \tag{3.3}$$

Based on (3.1) ~ (3.3), RMS value of i_1, i_2, i_3, and i_4 in asymmetrical modulation strategy named $i_{1\_rms\_c}$, $i_{2\_rms\_c}$, $i_{3\_rms\_c}$, and $i_{4\_rms\_c}$ are

$$i_{1\_rms\_c} = i_{3\_rms\_c} = \sqrt{\frac{i_o^2}{n^2} \cdot d_1 - \frac{8 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}} \tag{3.4}$$

$$i_{2\_rms\_c} = i_{4\_rms\_c} = \sqrt{\frac{i_o^2}{n^2} \cdot d_2 - \frac{8 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}} \tag{3.5}$$

From (3.4) and (3.5), it can be observed that the current pairs ($i_{1\_rms\_c}$, $i_{3\_rms\_c}$) and ($i_{2\_rms\_c}$, $i_{4\_rms\_c}$) are imbalanced, which thus would cause the power devices' power loss and thermal stress imbalance and undermine converter's reliability.

3.2. POWER DEVICES' CURRENTS UNDER PSM STRATEGY

Figure 3-2 shows power devices' currents under proposed PSM strategy, in which d_{rv1}-d_{rv4} are driving signals for S_1-S_4; d_1 is duty cycle during one switching time period; d_{loss} is duty cycle loss.

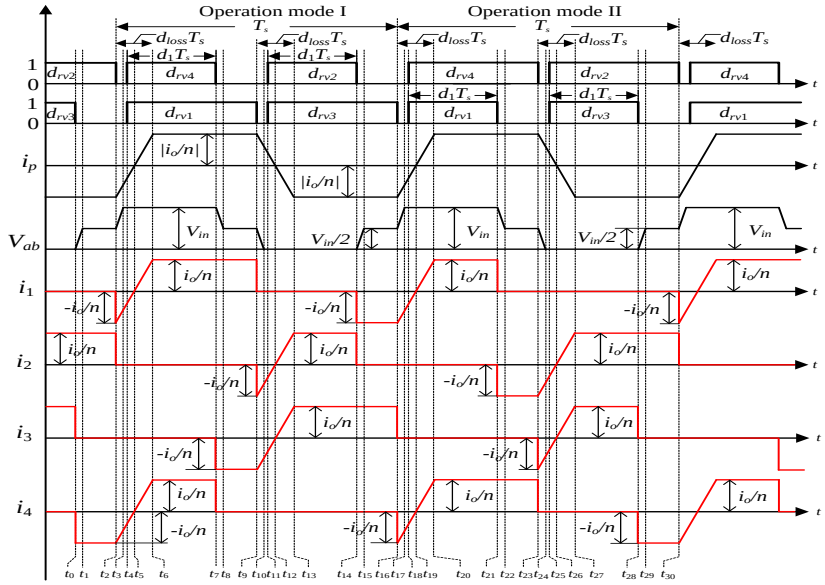
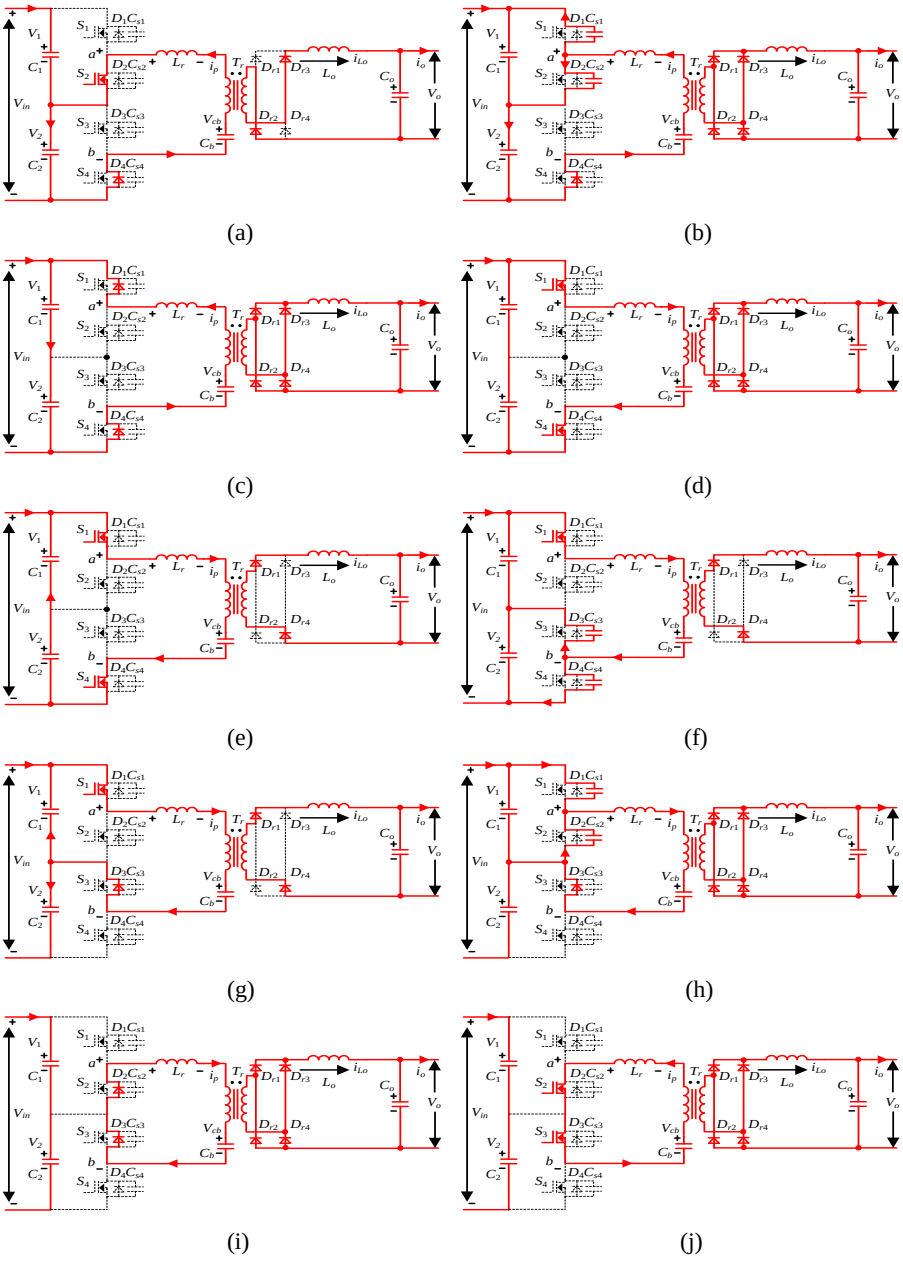
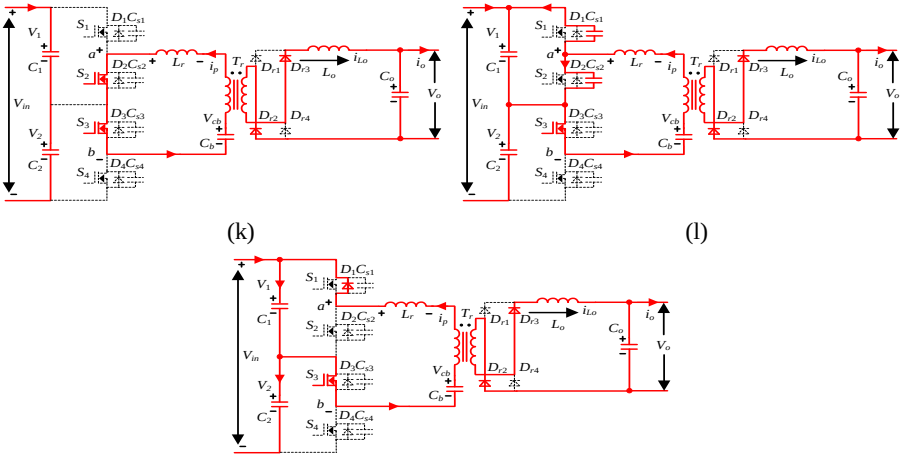


Figure 3-2 Currents on power devices under proposed PSM strategy.

Figure 3-3 presents equivalent circuits to explain working process.





(k) (l)

(m)

Figure 3-3 Equivalent circuits [102]. (a) [before t_2]. (b) [t_2 - t_3]. (c) [t_3 - t_5]. (d) [t_5 - t_6]. (e) [t_6 - t_7]. (f) [t_7 - t_8]. (g) [t_8 - t_9]. (h) [t_9 - t_{10}]. (i) [t_{10} - t_{12}]. (j) [t_{12} - t13]. (k) [t_{13} - t_{14}]. (l) [t_{14} - t_{15}]. (m) [t_{15} - t_{16}].

As presented in Figure 3-2, i_1, i_2, i_3, and i_4 are the same during every two switching time periods. Accordingly, only i_1 is given as

$$i_1 = \begin{cases} -\frac{i_o}{n} + \frac{V_{in}}{2 \cdot L_r} \cdot t & [t_2 - t_6] \\ \frac{i_o}{n} & [t_6 - t_9] \\ -\frac{i_o}{n} & [t_{14} - t_{16}] \\ -\frac{i_o}{n} + \frac{V_{in}}{2 \cdot L_r} \cdot t & [t_{16} - t_{20}] \\ \frac{i_o}{n} & [t_{20} - t_{21}] \end{cases} \tag{3.6}$$

In Figure 3-2, the time intervals [t_2 - t_6], [t_9 - t_{13}], [t_{16} - t_{20}] and [t_{23} - t_{27}] can be obtained by

$$t_6 - t_2 = t_{13} - t_9 = t_{20} - t_{16} = t_{27} - t_{23} = \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in}} \tag{3.7}$$

Based on (3.6) and (3.7), RMS value of i_1, i_2, i_3, and i_4 under proposed strategy named $i_{1\_rms\_p}$, $i_{2\_rms\_p}$, $i_{3\_rms\_p}$, and $i_{4\_rms\_p}$ are

$$i_{1\_rms\_p} = i_{2\_rms\_p} = i_{3\_rms\_p} = i_{4\_rms\_p} = \sqrt{\frac{i_o^2}{2 \cdot n^2} - \frac{8 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}} \tag{3.8}$$

Tabel 3-1 Calculation formulas about RMS value of i_1 ~ i_4

Control Strategy	RMS Value	Theoretical Calculation Formula
Conventional modulation Strategies	$i_{1\_rms\_c}$ $i_{3\_rms\_c}$	$\sqrt{\frac{i_o^2}{n^2} \cdot d_1 - \frac{8 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}}$
	$i_{2\_rms\_c}$ $i_{4\_rms\_c}$	$\sqrt{\frac{i_o^2}{n^2} \cdot d_2 - \frac{8 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}}$
Proposed modulation Strategy	$i_{1\_rms\_p}$ $i_{2\_rms\_p}$ $i_{3\_rms\_p}$ $i_{4\_rms\_p}$	$\sqrt{\frac{i_o^2}{2 \cdot n^2} - \frac{8 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}}$

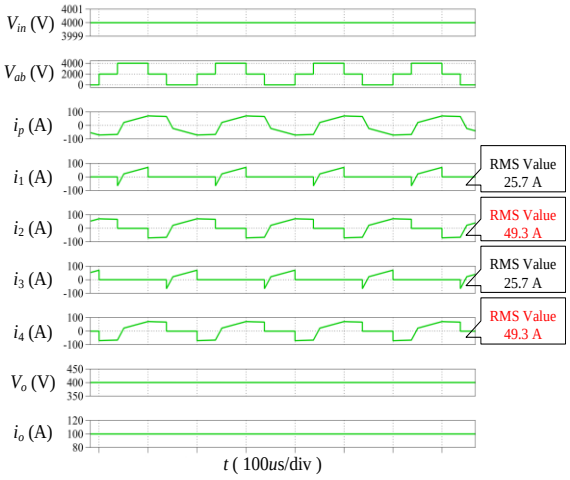
3.3. SIMULATION AND EXPERIMENTAL VERIFICATION

A. Simulation verification

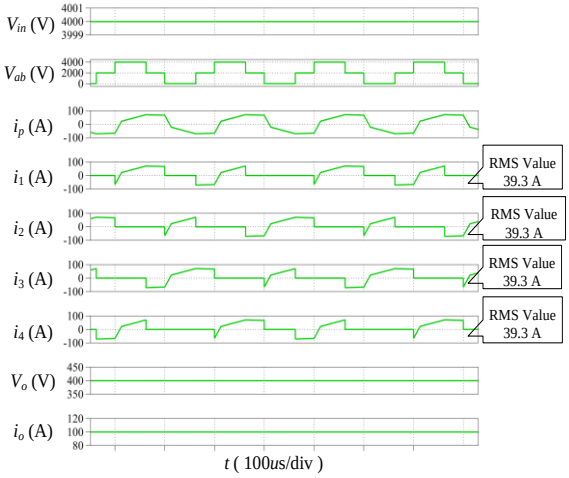
Table 3-2 presents parameters of built simulation model. Figure 3-4 shows simulation results, in which 1) current pairs ($i_{1\_rms\_c}$, $i_{3\_rms\_c}$) and ($i_{2\_rms\_c}$, $i_{4\_rms\_c}$) are 25.7 A are 49.3 A respectively; however, 2) $i_{1\_rms\_p}$, $i_{2\_rms\_p}$, $i_{3\_rms\_p}$, and $i_{4\_rms\_p}$ are all 39.3 A.

Tabel 3-2 Parameters of established simulation model

Description	Parameter
Input voltage V_{in} (kV)	4
Output voltage V_o (V)	400
Output current i_o (A)	100
Turns Ratio of Transformer T_r	15 : 7
Leakage Inductance L_r (uH)	300
Output Filter Capacitor C_o (uF)	4700
Output Filter Inductor L_o (uH)	1500
Input Capacitors C_1 and C_2 (uF)	4700
DC-blocking Capacitor C_b (uF)	100
Switching Frequency (kHz)	5
Dead Time (us)	1



(a)



(b)

Figure 3-4 Simulation results (V_{in} = 4 kV, V_o = 400 V, i_o = 100 A). (a) Asymmetrical modulation strategy. (b) Proposed strategy.

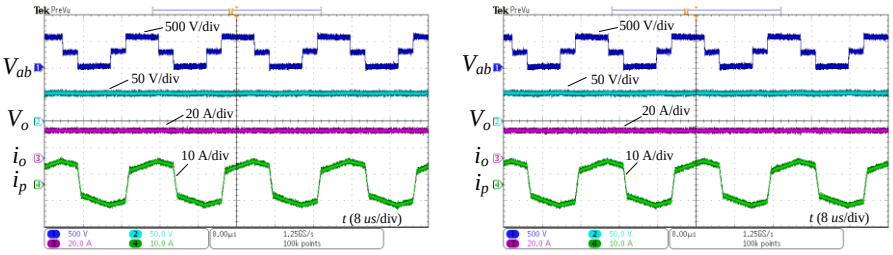
B. Experimental verification

Table 3-3 presents parameters of established prototype. The hardware of established prototype and control block have already been presented in Figures 2-7 and 2-8 respectively, which are not repeated here.

Tabel 3-3 Parameters of established prototype

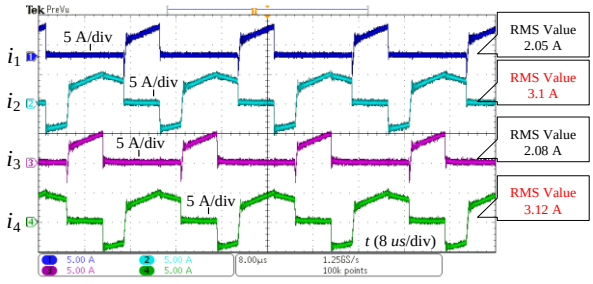
Description	Parameter
Power Switches S_1 - S_4	SPW47N60C3
Rectifier Diodes D_{r1} - D_{r4}	MBR40250TG
Turns Ratio of Transformer T_r	25 : 8
Leakage Inductance L_r of T_r (uH)	20.7
Output Filter Capacitor C_o (uF)	470
Output Filter Inductor L_o (uH)	140
Input Capacitors C_1 and C_2 (uF)	11
DC-blocking Capacitor C_b (uF)	12
Switching Frequency (kHz)	50
Dead Time (ns)	400

Figures 3-5 ~ 3-7 show the experimental results. In Figures 3-6(a) and 3-7(a), $i_{1\_rms\_c}$, $i_{2\_rms\_c}$, $i_{3\_rms\_c}$, and $i_{4\_rms\_c}$ are 2.05 A, 3.10 A, 2.08 A, and 3.12 A under 500 W and 3.86 A, 5.63 A, 3.79 A, and 5.59 A under 1 kW. After utilizing the proposed PSM strategy, $i_{1\_rms\_p}$, $i_{2\_rms\_p}$, $i_{3\_rms\_p}$, and $i_{4\_rms\_p}$ are 2.57 A, 2.61 A, 2.58 A, and 2.64 A under 500 W and 4.75 A, 4.76 A, 4.68 A, and 4.73 A under 1 kW as shown in Figures 3-6(b) and 3-7(b).

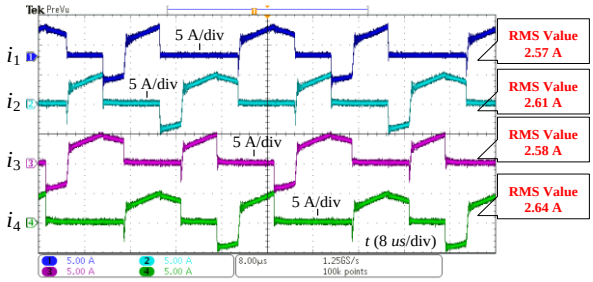


(a) (b)

Figure 3-5 Experimental results of V_{ab}, V_o, i_o, and i_p (V_{in} = 550 V, V_o = 50 V, P_o = 1 kW) [102]. (a) Asymmetrical modulation strategy. (b) Proposed strategy.

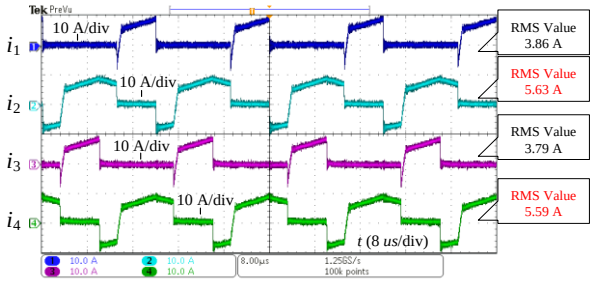


(a)

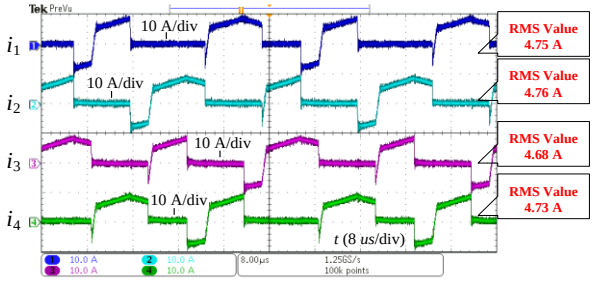


(b)

Figure 3-6 Experimental results of i_1, i_2, i_3, and i_4 (V_{in} = 550 V, V_o = 50 V, P_o = 500 W) [102]. (a) Asymmetrical modulation strategy. (b) Proposed strategy.



(a)



(b)

Figure 3-7 Experimental results of i_1, i_2, i_3, and i_4 (V_{in} = 550 V, V_o = 50 V, P_o = 1 kW) [102]. (a) Asymmetrical modulation strategy. (b) Proposed strategy.

Figure 3-8 presents experimental RMS value of i_1, i_2, i_3, and i_4. The experimental results in Figure 3-8 can verify that proposed strategy would effectively get rid of power devices' current imbalance.

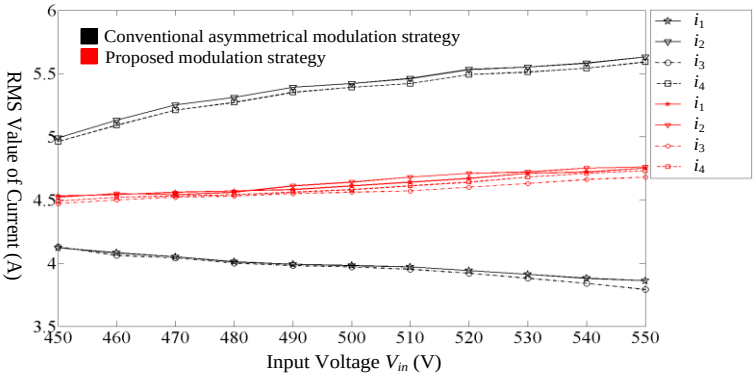
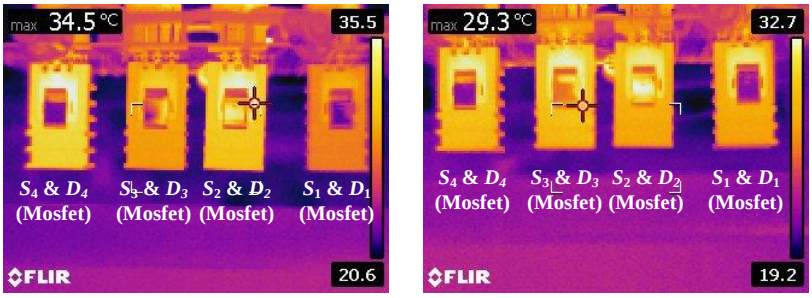


Figure 3-8 Experimental RMS value of i_1, i_2, i_3, and i_4 (V_o = 50 V, P_o = 1 kW).

Figure 3-9 shows comparison results about power devices' thermal stresses between conventional and proposed strategy. From Figure 3-9, it can be observed that: 1) temperature of (S_2, D_2) and (S_4, D_4) are higher than that of (S_1, D_1) and (S_3, D_3) under conventional strategy; and 2) temperature of (S_1, D_1), (S_2, D_2), (S_3, D_3), and (S_4, D_4) are almost same by utilizing proposed strategy; 3) primary power devices' maximum temperature can be reduced from 34.5 C to 29.3 C due to proposed strategy.



(a) (b)

Figure 3-9 Comparison results about power devices' thermal stresses (V_{in} = 550 V, V_o = 50 V, P_o = 1 kW) [102]. (a) Asymmetrical modulation strategy. (b) Proposed strategy.

3.4. SUMMARY

In this chapter, the proposed PSM strategy is utilized for several TL IDCs with asymmetrical modulation strategy to balance power devices' currents, which would thus effectively balance power devices' power loss and thermal stress. Simulation results and experimental results both validate proposed strategy. The paper related to this chapter is J3.

CHAPTER 4. IMPROVING TRANSFORMER PERFORMANCE

This chapter aims at improving transformer performance of FB diode-clamped TL isolated DC/DC converter. Therefore, a new DPS control strategy is proposed to decrease *dv/dt* on transformer.

4.1. VOLTAGE CHANGES ON TRANSFORMER UNDER CONVENTIONAL CONTROL STRATEGY

Figure 4-1 shows structure of FB diode-clamped TL isolated DC/DC converter and working principle under conventional control strategies. In Figure 4-1, V_{in} is input voltage; C_{i1} and C_{i2} are input capacitors to split V_{in} into V_1 and V_2; S_1-S_8 and D_1-D_8 are power switches and diodes; C_1 - C_8 are junction capacitors of S_1 - S_8; C_{s1} and C_{s2} are two flying capacitors; D_9-D_{12} are clamped diodes; T_r is the isolated transformer; L_r is leakage inductance of T_r; D_{r1}-D_{r4} are four rectifier diodes; L_o and C_o are filter inductor and capacitor. Additionally, V_{ab} is voltage from point *a* to *b*; i_p is primary current of T_r; i_{Lo} is current on L_o; V_o and I_o are the output voltage and current; and n is turns ratio in T_r. Figures 4-2 and 4-3 presents conventional control strategies named chopping plus phase shift (CPS) [97] and DPS control [98] for FB diode-clamped TL isolated DC/DC converter. From Figures 4-2 and 4-3, it can be seen that maximum voltage change in these conventional control strategies are both from 0 to V_{in} or 0 to -V_{in} as marked by red color, which would thus cause high *dv/dt*.

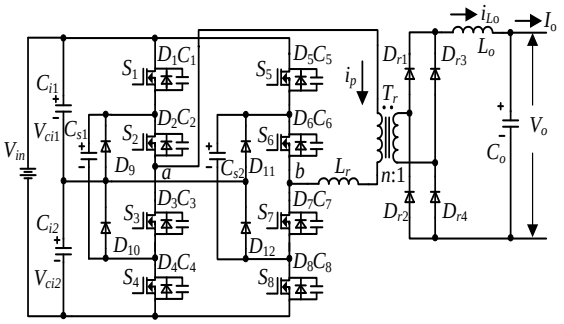


Figure 4-1 Circuit structure.

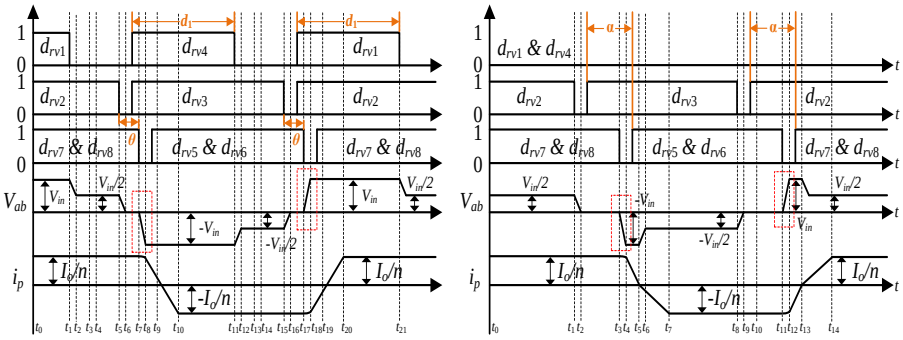


Figure 4-2 Chopping plus phase shift (CPS) control [97]. (a) Three-level mode. (b) Two-level mode.

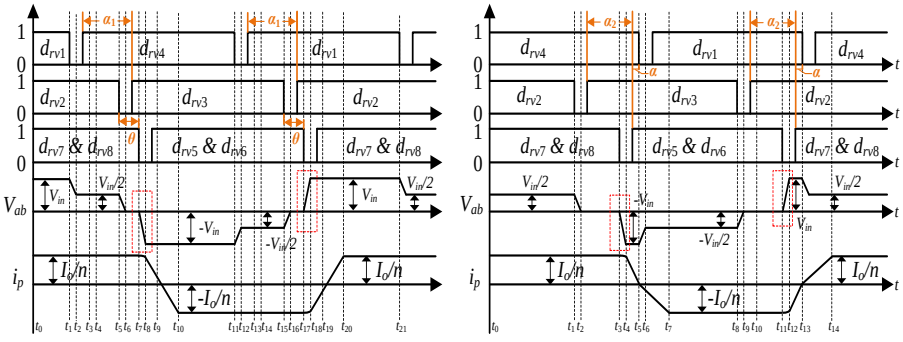


Figure 4-3 Double phase-shift (DPS) control [98]. (a) Three-level mode. (b) Two-level mode.

4.2. PROPOSED DPS CONTROL STRATEGY

Figure 4-4 presents working principle of proposed new DPS control strategy. In Figure 4-4, d_{rv1}-d_{rv8} are driving signals for S_1-S_8; α_1 and α_2 are two time delays.

Some assumptions are used to simplify following analysis: 1) S_1 - S_8 have same parasitic capacitors; 2) C_{i1} and C_{i2} are regarded to be constant voltage sources (V_{in}/2); 3) C_{s1} and C_{s2} are regarded to be constant voltage sources (V_{in}/2); and 4) L_o is regarded to be a constant current source.

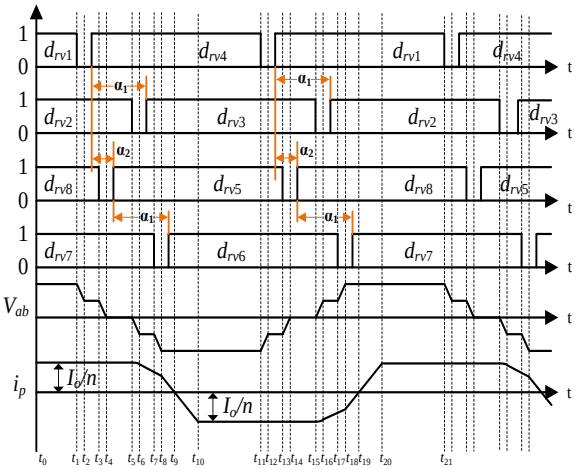
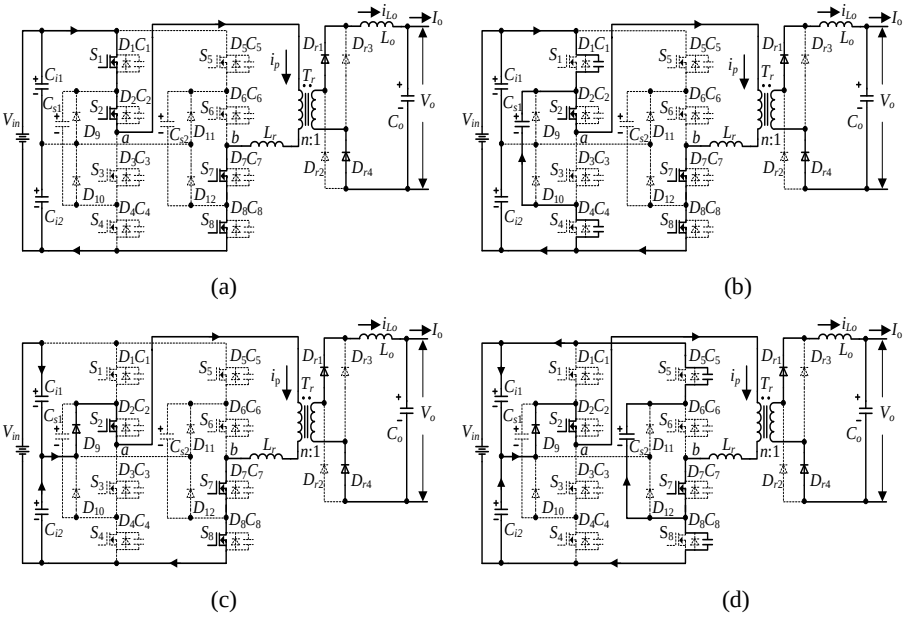


Figure 4-4 Proposed strategy (Three level mode).

Figure 4-5 presents equivalent circuits to explain working process.



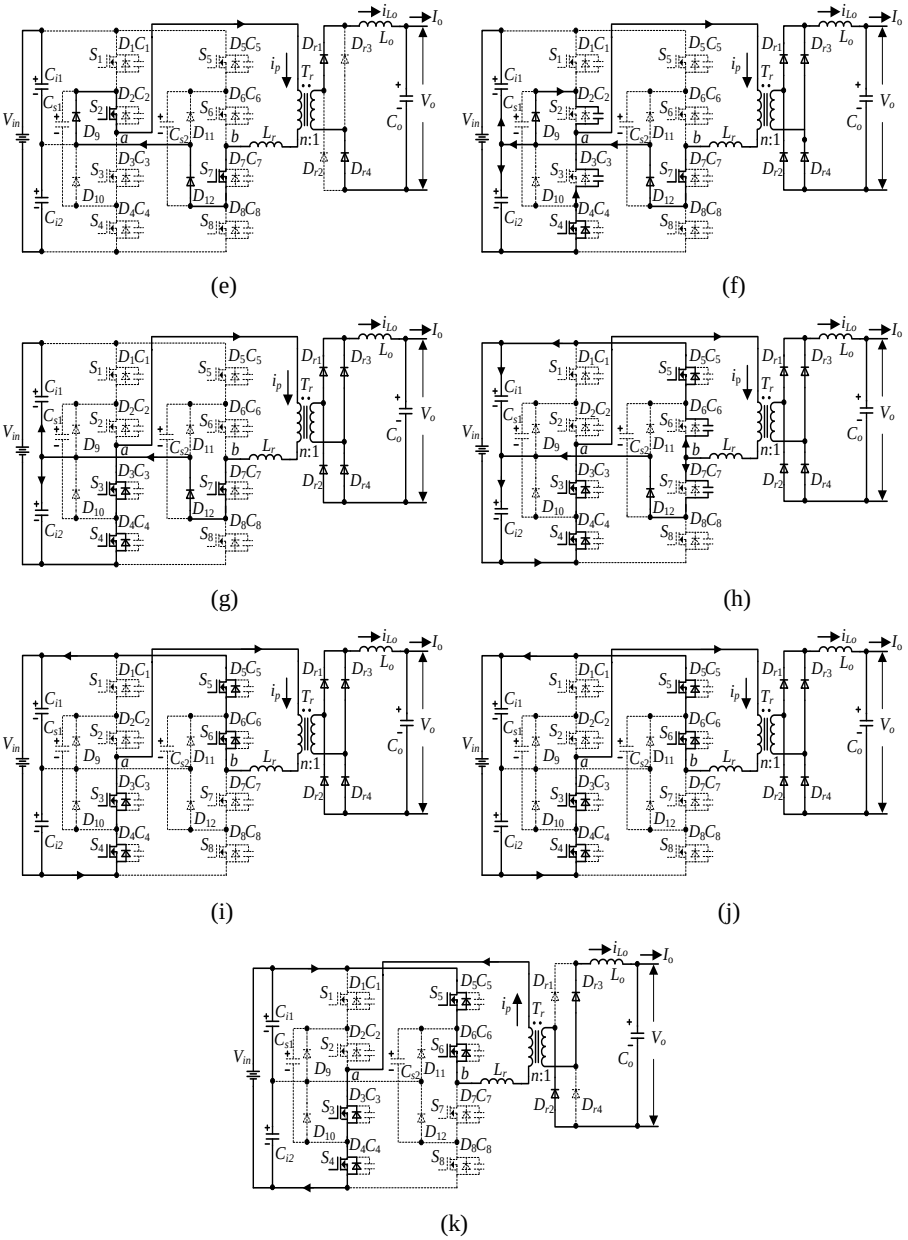


Figure 4-5 Equivalent circuits [103]. (a) [t_0-t_1]. (b) [t_1-t_2]. (c) [t_2-t_3]. (d) [t_3-t_4]. (e) [t_4-t_5]. (f) [t_5-t_6]. (g) [t_6-t_7]. (h) [t_7-t_8]. (i) [t_8-t_9]. (j) [t_9-t_{10}]. (k) [t_{10}-t_{11}].

4.3. SIMULATION VERIFICATION

Table 4-1 presents parameters of built simulation model. In simulations, α_2 is 5us; V_o is controlled by adjusting α_1.

Tabel 4-1 Parameters of established simulation model

Component	Description
Turns Ratio of the Transformer T_r (n : 1)	4 : 1
Input Capacitors C_1 and C_2 (uF)	4700
Output Filter Inductor L_o (uH)	1000
Output Filter Capacitor C_o (uF)	4700
Input Voltage V_{in} (kV)	4
Output Voltage V_o (V)	800
α_2 (us)	5
Output Power (kW)	64
Switching Frequency (kHz)	5

Figures 4-6 and 4-7 show simulation results. From comparison results between conventional strategies [97], [98] and proposed strategy, it can be seen that dv/dt on V_{ab} is decreased after using the proposed strategy. Therefore, voltage stress of transformer would be decreased.

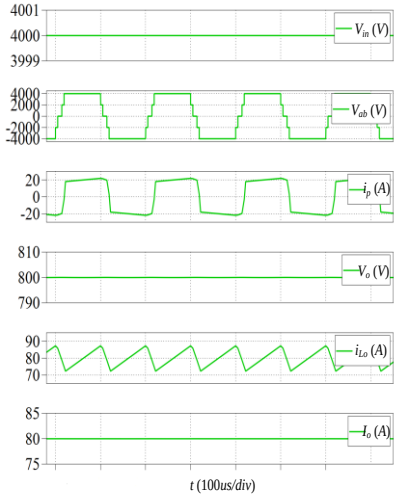
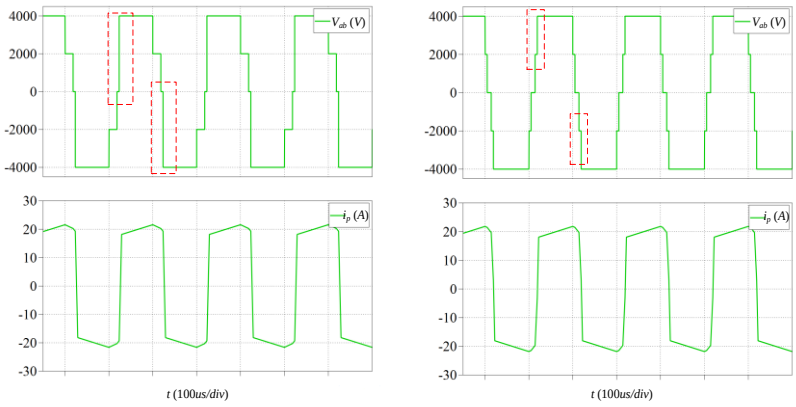


Figure 4-6 Simulation results under proposed DPS strategy.



(a) (b)

Figure 4-7 Comparison results. (a) Conventional strategies. (b) Proposed strategy.

4.4. SUMMARY

This chapter proposes a new DPS control strategy for FB diode-clamped TL isolated DC/DC converter to decrease voltage changes on transformer, which would decrease the *dv/dt* and voltage stress on transformer. Simulation results validate the proposed strategy. The paper related to this chapter is C1.

CHAPTER 5. CONCLUSIONS AND FUTURE WORKS

This project proposes new topology and modulation strategies to improve reliability performances of input capacitors, power devices, and transformer in TL-IDCs.

1) Improving input capacitor performances

There exists an issue of input capacitor current imbalance in FS-HBTL isolated DC/DC converter when utilizing conventional strategy, which would lead input capacitors' thermal stress and lifetime imbalance. Therefore, this project proposed a ZVS strategy including a PSM strategy to balance input capacitors' currents, which would thus balance input capacitors' thermal stress and lifetime. Additionally, this project proposes IPOP TL IDCs to balance and decrease input capacitors' currents, which would thus reduce input capacitors' size and prolong input capacitors' lifetime. Simulation and experimental results both validate proposed control strategy and topology.

2) Improving power device performance

The power devices' current imbalance issue exists in kinds of TL-IDCs with asymmetrical modulation. Accordingly, the proposed PSM strategy are utilized for these TL-IDCs to balance power devices' currents, which would thus increase converter's reliability through balancing power devices' power loss and thermal stress. Simulation results and experimental results both validate proposed strategy.

3) Improving transformer performance

This project proposes a new DPS control strategy for FB diode-clamped TL isolated DC/DC converter. Comparing with conventional control strategies, *dv/dt* and voltage stress on transformer would be reduced by proposed control strategy, which would thus increase converter's reliability. Simulation results validate proposed strategy.

There are many works can be further proceeded in future based on this thesis. The future works include but are not limited to followings:

- Investigate performances (currents on power devices, input capacitors, and flying capacitors) about FB diode-clamped TL IDCs;

- Investigate performances (currents on power devices, input capacitors, and flying capacitors) about T-type TL IDCs;

- Expand proposed PSM strategy to other hybrid TL-IDCs or other types of converters.

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