Advanced Converter-level Condition Monitoring for Power Electronics Components

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Publication date:
2020

Document Version
Publisher's PDF, also known as Version of record

ADVANCED CONVERTER-LEVEL CONDITION MONITORING FOR POWER ELECTRONICS COMPONENTS

BY
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DISSERTATION SUBMITTED 2020

AALBORG UNIVERSITY
DENMARK

Advanced Converter-level Condition Monitoring for Power Electronics Components

Ph.D. Dissertation

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Dissertation submitted Oct., 2020

Dissertation submitted: October 2020

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PhD Series: Faculty of Engineering and Science, Aalborg University

Department: Department of Energy Technology

ISSN (online): 2446-1636
ISBN (online): 978-87-7210-820-9

Published by:
Aalborg University Press
Kroghstræde 3
DK – 9220 Aalborg Ø
Phone: +45 99407140
aauf@forlag.aau.dk
forlag.aau.dk

Printed in Denmark by Rosendahls, 2020

Abstract

Applications, such as traction and offshore wind, demand cost-effective and robust condition monitoring solutions for operation optimization and predictive maintenance. There is still a gap between academic research and industrial applications in condition and health monitoring in power electronic converters from the signal extraction, calibration, and data processing perspectives. This Ph.D. study proposes two converter-level condition monitoring methods that have promising features to bridge the gap.

The first method is based on a converter-level on-state voltage measurement approach. The on-state voltage, such as saturation voltage of IGBTs and forward voltage of diodes, is a widely used electrical parameter for junction and health condition estimation of power semiconductor switches. Conventional methods are mainly at the component-level by adding a measurement circuit for each switch in its gate driver circuit. It suffers from two challenges: 1) gate driver is not always accessible, especially for power converters with design freeze, and 2) it has a relatively high cost and complexity. This study proposes a single measurement circuit connected in the middle-points of the phase legs of a single-phase inverter or three-phase inverter. It can measure on-state voltages of all the power switches, including diodes. Three variants of the circuits have been proposed as well: 1) with external power supply as existing component-level methods do; 2) with a self-power scheme to exclude the power supply which is the most expensive component in the measurement circuit, and 3) simple passive solution without the need of both power supply and self-power circuit. The passive solution reduces the implementation cost to 10% of the widely used component-level on-state voltage measurement circuit for a three-phase inverter application. It provides a plug-and-play solution with better accessibility to both existing and new designs of power electronic converters. Based on the obtained on-state voltage information, the junction temperature and health status estimation are demonstrated on the case study of single-phase inverter.

The second method is based on the digital twin concept without any additional hardware circuitry. This study chooses a Buck converter as the case study to prove the concept by using its digital twin for the degradation status

monitoring of MOSFETs and capacitors. The analytical models of the power stage and controllers are built up for the Buck converter. The in-situ component parameters, such as the on-state voltage of MOSFETs, capacitance, and equivalent series resistance, are estimated based on the existing feedback signals from the physical prototype and the corresponding calculated values from the digital twin. A data cluster method is proposed, which eliminates the calibration requirement for excluding the impact of other factors on the estimated component parameters, such as load level and temperature. The proposed method enables the degradation monitoring of MOSFETs and capacitors in the Buck converter without calibration and additional sensor. The application of the concept has been extended to a single-phase inverter.

The above methods have been experimentally verified, besides the theoretical analyses. An industry-oriented prototype has been designed for the converter-level on-state voltage measurement. The results of the Ph.D. research have been presented in 1 patent, 5 journal papers, and a few other conference publications.

Resumé

Anvendelser, såsom trækkraft og havvind, kræver omkostningseffektive og robuste tilstandsovervågningsløsninger til driftsoptimering og forudsigelig vedligeholdelse. Der er stadig en kløft mellem akademisk forskning og industrielle applikationer i tilstand og sundhedsovervågning i elektriske elektroniske omformere fra signaludvindings-, kalibrerings- og databehandling sperspektiver. Denne ph.d. undersøgelse foreslår to konverter-niveau tilstand overvågningsmetoder, der har lovende funktioner til at bygge bro over.

Den første metode er baseret på en konverterniveau på- spændingsmå -lingstilgang. On-state spænding, såsom mætningsspænding for IGBT'er og fremadspænding af dioder, er en meget brugt elektrisk parameter til kryds og helbredstilstand estimering af effekt halvlederleder switches. Konventionelle metoder er hovedsageligt på komponentniveauet ved at tilføje et målekredsløb for hver switch i dens gate driver-kredsløb. Det lider af to udfordringer: 1) portdriver er ikke altid tilgængelig, især for strømkonvertere med designfrysning, og 2) det har en relativt høj pris og kompleksitet. Denne undersøgelse foreslår et enkelt målekredsløb, der er tilsluttet midtpunkterne af fasebenene på en enfaset inverter eller trefaset inverter. Det kan måle on-state spændinger for alle strømafbrydere, inklusive dioder. Der er også foreslået tre varianter af kredsløbene: 1) med ekstern strømforsyning, som eksisterende metoder på komponentniveau gør; 2) med en selvkraftsplan for at udelukke strømforsyningen, der er den dyreste komponent i målekredsløbet, og 3) enkel passiv løsning uden behov for både strømforsyning og selvkraftkredsløb. Den passive løsning reducerer implementeringsomkostningerne til 10 % af det vidt anvendte komponentniveau på-spændingsmålingskredsløb til en trefaset inverterapplikation. Det giver en plug-and-play-løsning med bedre tilgængelighed til både eksisterende og nye design af elektriske elektroniske omformere. Baseret på den opnåede on-state spændingsinformation, demonstreres forbindelsestemperatur og sundhedsstatusestimering i case study af enfaset inverter.

Den anden metode er baseret på det digitale tvillingekoncept uden yder -ligere hardwarekredsløb. Denne undersøgelse vælger en Buck-konverter som casestudie til at bevise konceptet ved at bruge dets digitale tvilling til ned-

brydningstatusovervågning af MOSFETs og kondensatorer. De analytiske modeller for strømtrinet og controllere er opbygget til Buck-konverteren. Komponentparametrene in situ, såsom on-state spænding af MOSFETs, kapacitans og ækvivalent seriemodstand, estimeres baseret på de udgående feedbacksignaler fra den fysiske prototype og de tilsvarende beregnede værdier fra den digitale tvilling. Der foreslås en dataklyngemetode, der eliminerer kalibreringsbehovet for at udelukke påvirkningen af andre faktorer på de estimerede komponentparametre, såsom belastningsniveau og temperatur. Den foreslåede metode muliggør nedbrydningsovervågning af MOSFET'er og kondensatorer i Buck-konverteren uden yderligere sensor og kalibrering. Anvendelsen af konceptet er blevet udvidet til en enfaset inverter.

Ovenstående metoder er blevet eksperimentelt verificeret ud over de teoretiske analyser. En brancheorienteret prototype er designet til konverterniveau ved spændingsmåling. Resultaterne af ph.d. forskning er præsenteret i 1 patent, 5 tidsskriftsartikler og et par andre konferencepublikationer.

Preface

This PhD thesis is a summary of the PhD project "Advanced Converter-Level Condition Monitoring for Power Electronics Components". This PhD project is supported by Department of Energy Technology, Aalborg University, Denmark.

Firstly, I would like to express my deepest gratefulness to my supervisor, Professor Huai Wang, for his professional, patient, and earnest guidance. Especially, he gave me a chance to pursuit my PhD degree. He is one of the most inspiring, insightful, and kind persons I have ever met. He provides a lot of instructive advices and valuable opportunities for both my research and career. It is my great honor to be one of his PhD students.

I am also grateful to Dr. Yanfeng Shen and Dr. Haoran Wang for their selfless help and effective discussion during my PhD study.

I would also like to thank Dr. Teng Long for inviting me as a visiting student in his group. I benefit a lot from this study abroad in University of Cambridge.

Many thanks to all my colleagues at the Department of Energy Technology, Aalborg University, for their valuable discussion and kind help. Especially, the FBL group, for organizing regular group meeting and various social events.

Finally, I want to thank my family for their consistent support. Last but most importantly, I would like to give my sincerest gratitude to my wife, for her boundless love and more than I can express in words. Without her support and understanding, I wouldn't manage this PhD study. Everything seems possible with she by my side.

Yingzhou Peng
Aalborg University, October 7, 2020

Contents

Report

Part I. Preamble

This part is the preamble of the PhD project, which includes one chapter- **Chapter 1**. Introduction.

1 Introduction

This chapter discusses the background and motivation of the PhD project. The research questions and objectives are discussed. Then, the outline of the PhD thesis is presented to show the flow of this research work.

1.1 Background and motivation

Power electronic converters serve as a key role in power generation, transmission, distribution, and consumption by providing sustainable, flexible, and stable power [1]. It is usually used to achieve the voltage and power conversion between direct current (DC) and alternate current (AC), frequency conversion, and phase conversion in many industrial applications, such as renewable power generation including Photovoltaic (PV) and Wind Turbine (WT), Electric Vehicle (EV) and aircraft, train traction, and Adjustable Speed Drives (ASD) [2–6]. For example, Fig.1 shows the examples of power converter applications. To provide different powers concerning various applications, the type of power converter differs from DC-DC, DC-AC, to AC-DC converters.

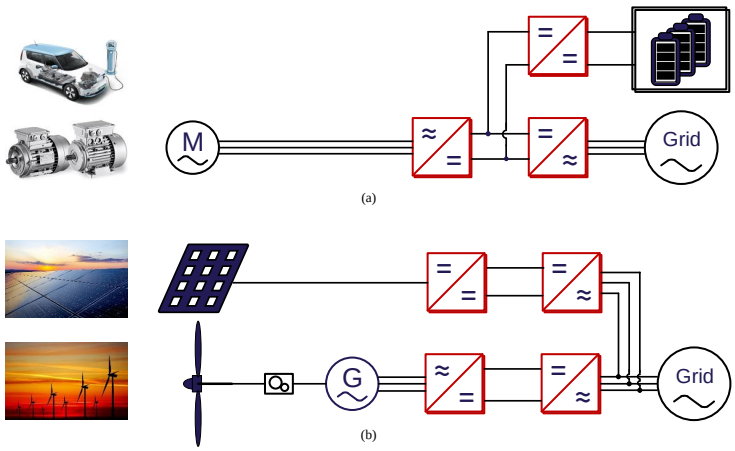


Fig. 1: Typical applications of power converters in: (a) electric vehicle and motor drives; (b) photovoltaic and wind turbine.

Conventionally, the principle design objective of power electronic converter is to improve the competitiveness in terms of economy and performance, which can be achieved by considering the following four factors [7]:

- Cost: it is usually the essential consideration for most applications since maximizing profit is the main target of converter producers.

- Efficiency: Customers prefer to the converters with higher efficiency due to lower energy lost;
- Power density: In some space-critical applications, such as electric vehicle, aircraft, and aerospace, the space for power converter is very limited;
- Manufacturability: Due to the increasing cost of labor and logistics, power converters are expected to be conveniently and economically produced and installed.

In recent decades, power converters are increasingly implemented at harsh and stressful conditions and bear the stresses coming from the temperature variation, mechanical vibration, humidity, and salinity penetration. After a long-term operation, the power converter may become vulnerable and unable to withstand those stresses. Consequently, the unexpected failure of power converter is becoming an issue. For example, field experiences in renewable applications show the critical role of power converters in terms of failure rate and maintenance cost [8]. Moreover, a survey from industry perspective reported that 93 % of respondents regarded reliability as the main issue for power electronic converters. More than 50 % emphasized the importance of improving the condition monitoring tools [9];

Therefore, to optimize the design of power converter, besides the four factors mentioned above, reliability is considered as an additional performance factor since it has significant impact on availability, safety, and operation cost.

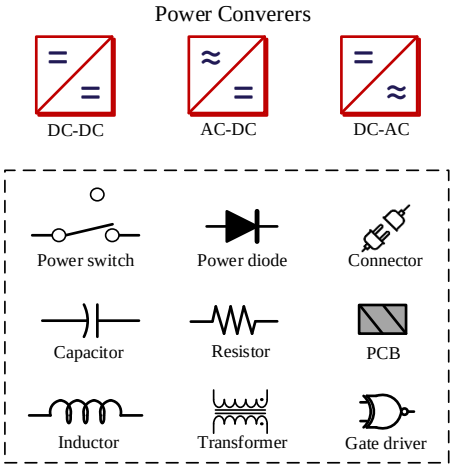


Fig. 2: Basic compositions of power electric converter.

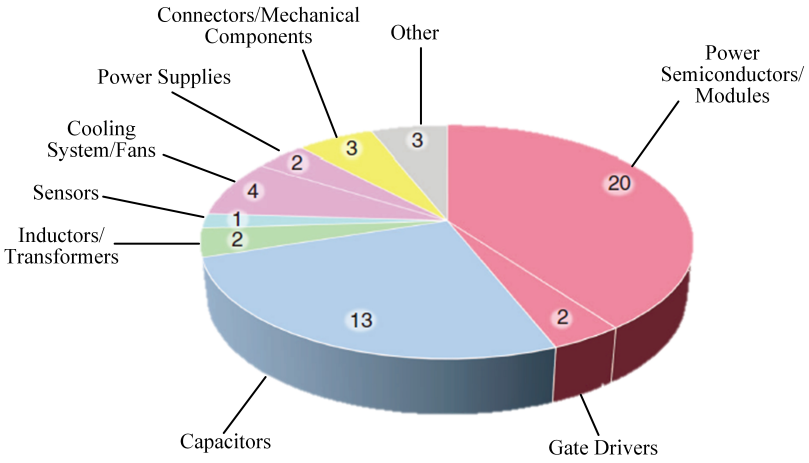


Fig. 3: The importance distribution of components in terms of reliability improvement in power electronics converter systems, from industry experts perspective [10].

The reliability of a power converter is dependent on each composed components, mainly including the power semiconductors/modules (power switches and diodes), capacitor, inductor, resistor, gate drive, and transformer as shown in Fig.2. Among them, power devices and capacitors are considered as the most crucial components that need future research to improve their reliability compared to other components according to the industry experts' answers in an industry survey as shown in Fig.3 [10], accounting for 20% and 13% of the power electronics systems, respectively.

Power device and capacitor are frequently considered as the most vulnerable components among the power converter based on the above information. Besides, they are also essential in terms of function, volume, and cost [7]. Therefore, currently, the reliability-related research mainly focuses on these two components [11].

To mitigate the risk of unexpected failures, researchers are endeavoring to make the power converter more reliable and available by using different strategies over the design and operation phases of power converter as shown in Fig.4, which are detailed below:

- Design phase: reliability should be considered along with efficiency and cost at the very beginning of power converter hardware design. For example, increasing the design margin is one option to improve reliability [9], so that it can meet the reliability requirement under a specific operating condition. Moreover, the distribution of capacitor-bank can be well-designed to improve its lifetime [12, 13]. Also, in some applications, multi-converters are required. A proper uniformity design between these converters can improve the lifetime of the entire multi-

converters system [14]. Additionally, temperature control strategies are used to reduce the junction temperature swing of power devices, resulting in longer lifetime of power devices [15–19]. However, introducing temperature control needs to modify the original controller, which is not preferable. Finally, once the hardware and control strategy of power converter are decided, the lifetime models can be established and used to predict the life cycle of power devices and capacitors [20–22].

- Operation phase: firstly, condition monitoring technology can be used to monitor the health condition of power devices and capacitors in real-time, so that the degradation process and potential failures can be predicted, and the operators can schedule the maintenance to secure the availability of power converters [9, 23–26]. Or, the derating operation can be applied through adaptive control to achieve longer lifetime.

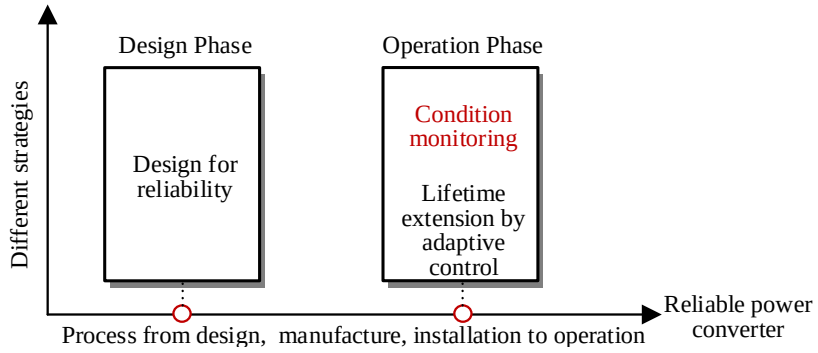


Fig. 4: Strategies of reliability design for power converter at different stages.

With the strategies mentioned above, the reliability and availability of power converter can be improved throughout its whole lifetime. At the hardware design stage, because increasing design margin and guaranteeing uniformity design lead to that the selected components have higher rated power than the required, which means the reliability is increased by sacrificing cost and efficiency in some degrees. At the control design stage, reducing the junction temperature swing needs to modify the conventional mature control algorithms, which may not be readily accepted by converter producers. Establishing lifetime models highly relies on the accuracy of physic and material knowledge of components, which are even different among a population of components with the same product part number. Also, operational and environmental conditions can affect the lifetime model parameters significantly. Thus, it is challenge to predict the real end-of-life of power converters in field applications through lifetime model.

Condition monitoring technology is adopted when the converter is in operation with the ability of online assessing the health condition of the key components. It is reported that the cost of wind farm mainly comes from both in terms of installation cost and operating cost. Particularly, 50 % of the O&M is due to unscheduled maintenance costs [27]. Also, the economic benefits attained through 1 % efficiency improvement for PV manufactures can be easily negated by a few-days downtime due to failures [9]. With the condition monitoring technology: 1) the predictive maintenance can be realized, which improves the availability and reduces the life-cycle cost; 2) the design margin of power converter can be reduced since the health condition becomes accessible, leading to the reduction of design cost further. Most importantly, from the industry perspective, it is reported in [10] that condition monitoring is one of the most important approaches to address the reliability issue of power electronic converter as shown in Fig.5, presenting that the last three listed topics are related to condition monitoring and given high beneficial score by experts.

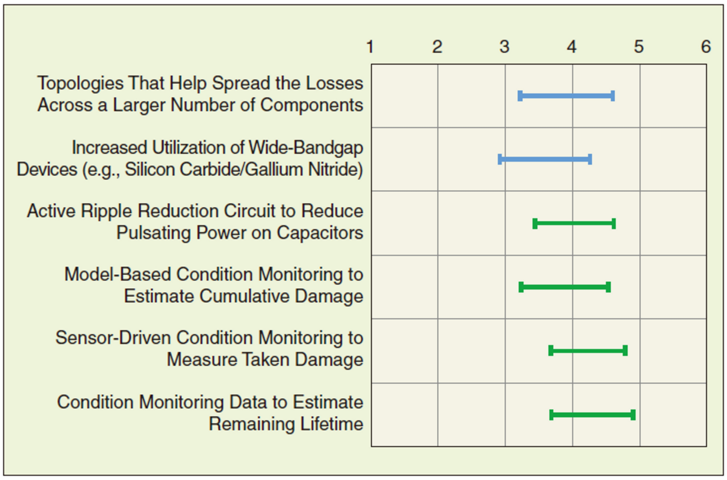


Fig. 5: The possible methods that will address the reliability of power electronics converters in the future, from industry experts' perspective. The scale is from one (not beneficial) to six (very beneficial). [10].

1.2 Literature study on condition monitoring methods for power electronic components

1.2.1 Power switches

Condition monitoring technology for power switches has been developed for decades, starting from failure mechanisms research to laboratory test

[9, 23, 24]. Usually, power switches are well packaged and sealed to achieve electrical, mechanical, and chemical protection. Therefore, the operators are blind to their internal degradation and cannot directly predict potential failures. However, the degraded power switches present abnormal electrical, thermal behaviors, and even acoustic and optic signals, which are taken to research the condition monitoring technologies indirectly. The detailed process of condition monitoring development is shown below:

- Degradation mechanism (Step 1): the failures of power switch are mainly occurred in chip-level and packaging-level. Most of the chip-related failures are due to the overstress caused transient breakdown. Another chip-related failure occurring in the gate oxide-layer of silicon-carbon power switches is reported as well [28, 29], which is due to wear-out. The traditional packaging techniques include wire-bond and press-pack. Among them, the wire-bond is the dominant one due to its well-established and low cost wire-bonding technology. Therefore, the research in this project is based on wire-bond based power switches. It has been unveiled that the degradation of wire-bonding power switches is mainly contributed by the bond-wires lift-off and solder layer degradation for both silicon and silicon-carbon devices [30–33]. It is due to the repeatable stress-strain cycle caused by long-term electrical and thermal cycle [34–37].

- Health indicators (Step 2): The degradation mechanisms described in step 1 can be related to various health indicators, including electrical, thermal, and even acoustic parameters. Among them, the electrical indicators can be extracted from those electrical waveforms as marked in Fig.7 [38–47]. V_{GP} is the miller plateau in the gate turn-on voltage, t_{GP} is the duration time of the miller plateau, V_{th} is the threshold voltage, t_{on} is the turn-on time, t_{d-off} is the turn-off delay time, I_{gss} is the gate leakage current, I_{css} is the collector leakage current, $V_{CE,sat}$ is the on-state voltage. The thermal behavior of power module as shown in Fig.6 can be expressed by the thermal networks as shown in Fig.8. The degradation of solder layer can weaken the capability of power losses dissipation, leading to the increase of thermal parameters R_{th} and C_{th}. Then, T_c is affected indirectly [48, 49]. Additionally, the optic and acoustic indicators were also presented in [50, 51]. Once the indicators are selected, they can be extracted from the electrical terminals (e.g., collector/drain, emitter/source, and gate) [52–60], thermal terminals (e.g., case), and by the optical and acoustic sensing equipment directly.

- Measurement and estimation of health indicator (Step 3): it is verified that all of the health indicators described in step 2 can reflect the degradation of power devices in some degree with laboratory testing. How-

ever, some are hardly measured in real-time, such as the collector and gate leakage current. For those measurable indicators, the corresponding on-line monitoring circuits are designed and tested in the laboratory [61–81]. Moreover, the model based estimation methods can also obtain the health indicators, but are rarely investigated. For example, the capacitance of capacitor was estimated in [82, 83].

- Data processing (Step 4): after the health indicators are obtained through the measurement circuits, data analysis and calibration are required to eliminate the data noise, operational and environmental impacts, consequently, to represent the health level of power devices [39].

To implement condition monitoring in field applications, the selection of indicators can be achieved by following some major considerations: 1) sensitivity to the dominant degradation mechanism of interest; 2) measurement complexity and cost, such as sampling frequency; 3) noise-immune ability, i.e., robustness. For the optical and acoustic indicators, the additional equipment with strong noise-immune ability is required to sense the faint change of optical and acoustic signals. For the thermal indicators, because the change of T_c caused by the degradation of power devices can be easily negated by other neighboring heat sources, leading to lower degradation sensitivity or false detection. Moreover, installing multiple T_c sensors on the case of the module can degrade the capability of the power devices to remove power losses from the semiconductor onto the heatsink. Therefore, it is shown that the majority of condition monitoring researches for power switches focus on electrical indicators that can be extracted from the electrical terminals. Among them, the indicators relative to the switching transient appear to be attractive since the switching properties generally exist while the device is in operation. However, the measuring circuits for these indicators are connected to the gate of devices. Consequently, it is hard to distinguish if the parameter shifts of these indicators is due to the degradation of semiconductor or the gate driver. Meanwhile, integrating monitoring circuits with gate drivers may risk its regular operation, which is critical to a functioning converter. Moreover, the switching indicators are thought to be high frequency and sensitive to voltage, current, temperature, and parasitic parameters of connecting wire, which requires complex measurement circuit.

Alternatively, the on-state voltage of power switches is thought to be the most promising and practical health indicator so far, as it shows higher sensitivity to the degradation of power devices, non-invasive measurement due to the connection with power terminals, and simple measuring circuit due to the relative low frequency feature compared to the switching transient related indicators. Nevertheless, all of these existing on-state voltage measuring methods are designed to monitor a single power switch, calling component-level measurement [78], which causes practical issues while applying to a

converter: 1) The circuit complexity and cost are multiplied to monitor the all power switches in a converter; 2) It is connected to the power terminals of individual switching devices, which may introduce more connecting terminals; and 3) it has one reference ground for each phase-leg, which requires more isolation stages while sampling the data of all devices.

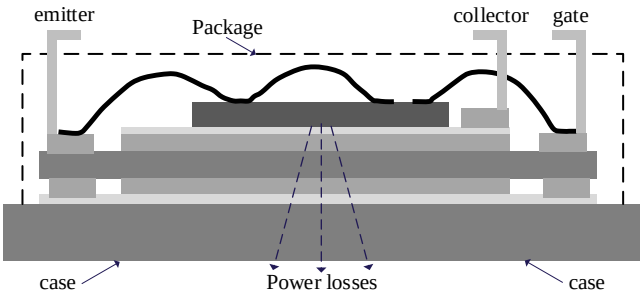


Fig. 6: A standard power module.

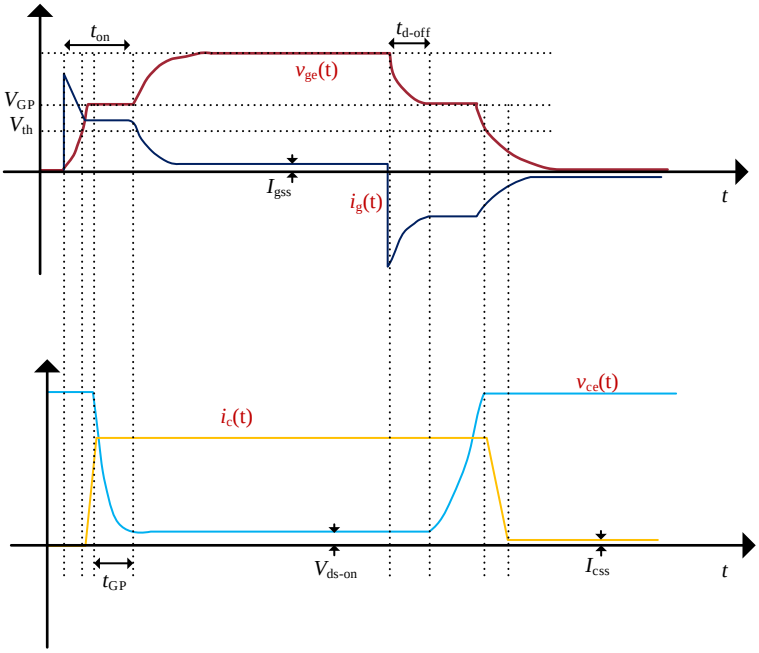


Fig. 7: Typical switching waveforms of power devices.

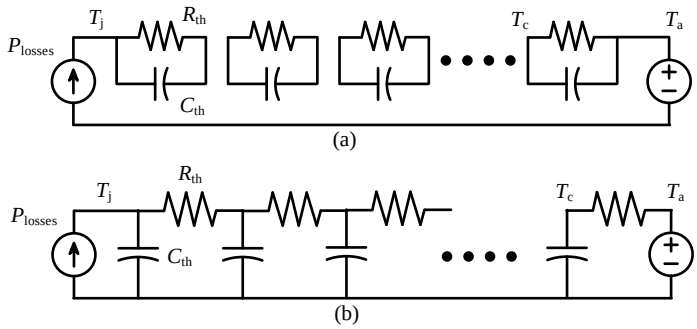


Fig. 8: Typical thermal network of power devices: (a) Foster network; (b) Cauer network.

1.2.2 Capacitors

Capacitors are one of the reliability-critical components in power converters and many efforts have been made to the condition monitoring of capacitors, so as to obtain their on-line health information and predict the potential failure [25, 26].

The simplified equivalent circuit of a capacitor is presented in Fig.9, including a capacitor (C_I), an equivalent series resistor (R_{ESR}), and an equivalent series inductor (L_{ESL}). It is unveiled that the degradation of the capacitor can shift these three parameters [25]. Consequently, the condition monitoring of capacitor can be achieved by monitoring these three parameters based on its impedance in response to frequency as shown in Fig.9. The impedance versus frequency plot of a capacitor can be divided into three regions based on ω_1 and ω_2 (typically 5-10 kHz) [84, 85], showing dominated capacitive impedance in region I, resistant impedance in region II, and inductive impedance in region III. Generally, L_{ESL} can be neglected due to low inductance (nH level) and negligible impedance in region I and II. Therefore, C_I and R_{ESR} are the two leading health indicators for capacitor.

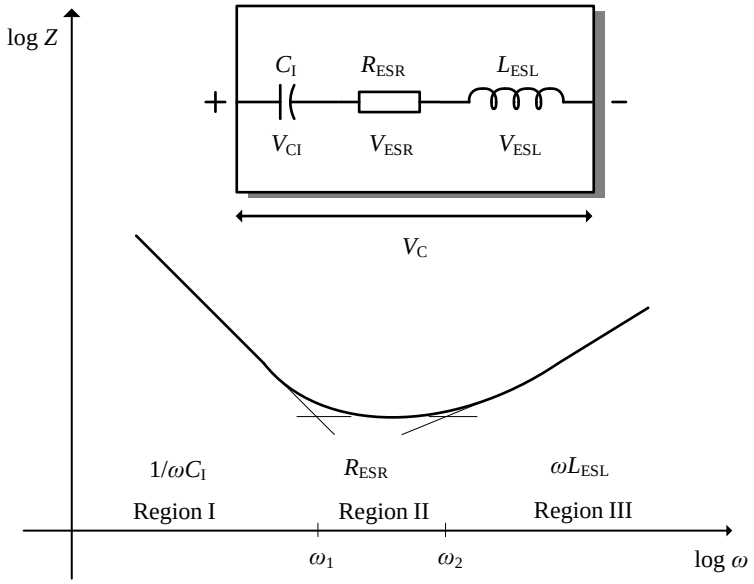


Fig. 9: Equivalent circuit and impedance characteristics of capacitors.

Based on the operational frequency region I and II, there are two main methods to estimate C_I and R_{ESR}: 1) in region I, the capacitance is the dominated value. Usually, the capacitor operates at some special conditions (frequency is less than ω_1), such as off-line discharge and charge transient, converter start-up and shut-down transient. During these particular conditions, the capacitance can be estimated through the charge/discharge curve; 2) in region II, capacitor operates at normal condition (frequency is within ω_1 and ω_2), and the capacitor voltage ripple and current ripple can be used to estimate the R_{ESR}.

Charge/discharge transient based condition monitoring method [86–89] The start-up and shut-down transients are existed in many applications, which can be took to estimate C_I. For example, the discharge process of the DC-link capacitor in a converter can be recorded with the help of a discharge resistor R_d. Then, the discharge process during the shut-down can be expressed by:

$$u_C = U_0 \times e^{-\frac{t}{(R_{ESR}+R_d)C_I}} \tag{1}$$

where u_C is the capacitor voltage during discharge, U_0 is the initial value of u_C. Then, $(R_{ESR} + R_d)C_I$ can be easily obtained through data fitting. Among them, R_d is already known and far larger than R_{ESR}, resulting in negligible R_{ESR}. Finally, C_I can be calculated.

This method is very simple and effective, and can obtain the accurate results without adding any external hardwares. However, it is kind of quasi on-line method due to the requirement on dis/charge event.

Ripple based condition monitoring method [90–98] According to Fig.9, the phase voltage across C_{I} and R_{ESR} at the frequency between ω_1 and ω_2 are depicted in Fig.10 based on the polarity of capacitor voltage V_{C} and current I_{C} (assuming V_{ESL} is negligible). Then, based on the Pythagorean trigonometric, the phase difference between V_{C} and I_{C} can be expressed by:

$$cos\theta = \frac{V_{ESR}}{V_{\mathrm{C}}} \tag{2}$$

then, R_{ESR} can be calculated by:

$$R_{\mathrm{ESR}} = \frac{V_{ESR}}{I_{\mathrm{C}}} = \frac{V_{\mathrm{C}} \times cos\theta}{I_{\mathrm{C}}} \tag{3}$$

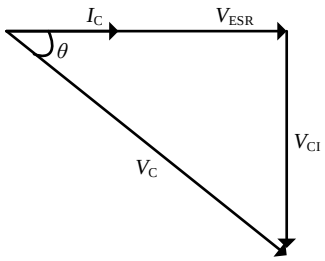


Fig. 10: Phase direction of the equivalent circuit of capacitor by neglecting L_{ESL}.

V_{C} and I_{C} at the frequency between ω_1 and ω_2 can be obtained by using a bandpass filter, θ can be obtained by using a phase detector. It can be seen that the key steps of this method is to extract the ripple values of capacitor voltage and current, which is usually realized by adding the bandpass filters. In practice, capacitor voltage is measured for control or protection. The capacitor current be obtained: 1) by measuring the output currents of power converter and combining the on-off information of each power device; 2) embedding the current sensor inside the capacitor. Overall, the ripple-based method is an on-line condition monitoring and suitable for different applications. However, firstly, the indirect measurement of capacitor current can cause transfer errors and requires the PWM information. Moreover, the ripple extraction needs the bandpass filter and phase detector.

1.2.3 Converter-level methods

Converter-level methods are proposed to realize the condition monitoring from the converter-level terminals, instead of the individual terminals of a single component. To our best knowledge, several converter-level methods have been proposed so far: 1) the harmonic spectrum of the output current of converter, for example, are proposed for monitoring the degradation of power switches [99, 100]. A reduction of fifth harmonic due to the increase of temperature is discovered; 2) another example is the overall efficiency of the converter [101]. The power loss generated among the converter is increased with the degradation of power switches and capacitors, leading to the reduction of overall efficiency. Nevertheless, the issues with the above converter-level methods are: a) both efficiency and harmonic are obtained by measuring the converter-level signals (e.g., DC-link voltage/current, output voltage/current) that are hardly affected by the degradation of power switches and capacitors. Thus, it is difficult to measure these indicators with enough accuracy for degradation monitoring; b) both the degradations of capacitor and power switch can affect these indicators and can not be distinguished; 3) moreover, due to the development of advanced computers and algorithms, the neural-network is recommended to do condition monitoring as well [102, 103]. This method can estimate the health status of the converter components by training an effective neural model that covers the full operation and degradation conditions of converter. However, firstly, the change of converter-level signals caused by component degradation is less than 0.1 % and could be covered by the measurement noise. Secondly, it is a challenge to obtain the training data that covers all possible operation and degradation conditions in field applications. Overall, these existing converter-level methods have low sensitivity in indicating the degradation of converters.

1.3 Project motivation

Existing condition monitoring with component-level methods require complex measurement circuits. For the converter-level methods, they rely on the measurement of converter-level signals. Thus, their degradation sensitivity is much lower than the measurement circuit based component-level methods and the change of converter-level indicators due to degradation could be lower than noise in field applications. Therefore, as the increasing demand for condition monitoring from field power converter applications, the movement toward practical and advanced condition monitoring methods meets new challenges.

- Due to the accessibility to existing or even next generation power electronics converters, the converter-level condition monitoring solutions with less or even without additional hardware are expected;

- Practical applications of condition monitoring face challenges in reducing the measuring circuit complexity, size, and cost. Moreover, a plug-and-play solution with less connecting terminals is desired;
- Health indicators are also dependent on operational and environmental conditions, such as voltage, current, and temperature. Thus, a method capable of excluding these impactors beside degradation is required, which can be achieved by either calibration and data analytics-based methods.
- Software-based methods are relatively preferred from application perspective due to reduced cost and implementation complexity, compared to hardware-based methods.

Therefore, the embodiment of condition monitoring technologies with high performance in terms of complexity, cost, degradation sensitivity, and even hardware-free are still needed.

1.4 Project objectives and limitations

1.4.1 Research questions and objectives

Based on the discussion of the trend for the practical and advanced condition monitoring technologies and the review of the existing methods, the question about how to develop converter-level measurement/estimation methods of health indicators of power electronic components with reduced complexity and cost will be answered in this project. Specifically, the following research questions are to be addressed:

- Is it possible to measure the on-state voltage of power semiconductor devices without accessing its gate or power terminals?
- Is it possible to achieve software based health indicator estimation without the need for training data?
- Is it possible to achieve the condition monitoring of power electronic components without the need of calibration?

With the questions listed above, the overall objective of this PhD project is to research the advanced converter-level condition monitoring methods for power electronics components. The objectives of this project are detailed as follow:

- Circuit design methodology of the converter-level condition monitoring: the on-state voltage of power devices is the most widely reported health indicator so far. Although different measuring circuits have been

proposed in recent decades, they are limited in component-level measurement and hardly used in practical applications. Based on this, a converter-level on-state voltage measuring circuit is designed and developed with the considerations of circuit complexity, size, cost, and practical implementation;

- Implementation of the proposed converter-level condition monitoring circuit: In order to achieve the health assessment of power devices by using the proposed circuit, the practical implementations of the proposed circuit in different applications are investigated. Moreover, the proposed circuit is also capable of estimating the junction temperature of power devices through the monitored on-state voltage;

- Digital twin based condition monitoring for power converters: From the view of industry applications, it would be better if the condition monitoring can be achieved with existing sensors and without additional circuit. The possibility and feasibility of using digital twin to achieve condition monitoring are investigated. The experimental validation is also carried out. Meanwhile, the merits and shortcomings are discussed.

1.4.2 Project limitations

The PhD project studies the design and implementation of converter-level on-state voltage measurement and digital twin based health indicator estimation to achieve the condition monitoring for the key components of power converters with reduced complexity and cost. However, several limitations exist in this project:

- The failure mechanisms of power devices and capacitors considered in the condition monitoring are thermal and electrical stresses related degradation. Humidity, salinity, and other uncertain factors are not included;

- The verification of the proposed methods are limited to the laboratory testing at the time when this thesis is submitted. Field testing is to be performed in the future with industry partners;

- The degradation testing and verification of the proposed digital twin based method for condition monitoring is mainly conducted with Buck converter. The realization of single-phase inverter digital twin is investigated. It is possible to extend the study on the applications for three-phase converters.

Table 1: The related publications for each chapter.

Chapter No.	Relevant Publications
1	-
2	J2, J3, J5, P1
3	J2, J3, J4, J5
4	J1
5	-
6	-

1.5 Thesis outline

The outcome of this project is documented by a PhD thesis, which includes two parts: a report and related disseminations (publications, patents, and tutorial).

The first part is Chapter 1. Introduction, which is the preamble of the report.

The second part is entitled "Hardware based non-invasive converter-level condition monitoring for power semiconductor devices", including two chapters. Chapter 2. Design of the converter-level on-state voltage monitoring circuits. Chapter 3. Applications of the converter-level on-state voltage monitoring circuits.

The third part is entitled "Digital twin concept based system-level condition monitoring for power converters", covering two chapters. Chapter 4. Implementation of digital twin for condition monitoring in DC-DC converters. Chapter 5. Feasibility study on the digital twin for single-phase inverter.

Last chapter of the report is Chapter 6. Summary and Outlook. It includes the summary of the contributions in this project, new research perspective and challenges for future study.

1.6 List of disseminations

The invention and publications from this PhD project are shown below. In order to show the contributions for each chapter, the relationship between the chapters of the PhD thesis and the patent/publications are shown in Table. 1.

Patents

P1. **Y. Peng**, H. Wang, "Non-invasive front-end for power electronic monitoring", filed, P71138DK01, 2020.

Journal Papers

J1. **Y. Peng**, Shuai. Zhao, and H. Wang "A Digital Twin based Estimation Method for Health Indicators of DC-DC Converters" *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1220-1224, Feb. 2021.

J2. **Y. Peng**, Yanfeng. Shen, and H. Wang "A Converter-level On-state Voltage Measurement Method for Power Semiconductor Devices" *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 2105-2118, Feb. 2021.

J3. **Y. Peng**, H. Wang "A Self-Power Method for A Converter-level On-state Voltage Measurement Concept" *IEEE Trans. Power Electron.*, Under review, 2020.

J4. **Y. Peng**, H. Wang "An On-line Calibration Method for TSEP-based Junction Temperature Estimation" *IEEE Trans. Power Electron.*, Under review, 2020.

J5. **Y. Peng**, H. Wang "A Passive Circuit for On-State Voltage Measurement of Power Semiconductor Devices" *IEEE Trans. Power Electron.*, Under review, 2020.

Conference Papers

C1. **Y. Peng**, Yanfeng. Shen, and H. Wang, "A Condition Monitoring Method for Three Phase Inverter Based on System-Level Signal" in *Proc. IEEE PEAC*, pp. 228-233, 2018.

C2. **Y. Peng**, H. Wang, "Parameters Identification of Buck Converter Based on Dynamic Characteristics" in *Proc. IEEE ECCE Asia*, pp. 228-233, 2019.

C3. **Y. Peng**, H. Wang, "Application of Digital Twin Concept in Condition Monitoring for DC-DC Converters" in *Proc. IEEE ECCE*, pp. 228-233, 2019.

Project

P1. H. Wang and **Y. Peng**, "A Power Device On-State Voltage Monitoring Apparatus for Three-Phase Power Electronic Converters", Aalborg University proof-of-concept grant. Feb.01, 2020 - Oct.31, 2020.

Part II. Hardware Based Non-invasive Converter-level Condition Monitoring for Power Semiconductor Devices

In this part, the development of existing component-level on-state voltage monitoring circuits are discussed firstly. Then, the circuit design methodology of proposed converter-level on-state voltage monitoring is introduced. Finally, it's implementations in different applications are illustrated as well. There are two chapters in this part: **Chapter 2**. Design of the converter-level on-state voltage monitoring circuits and **Chapter 3**. Application of the converter-level on-state voltage monitoring circuits.

2 Design of the converter-level on-state voltage monitoring circuits

This chapter studies the existing component-level on-state voltage monitoring circuits with considering circuit complexity, cost, and practical implementation. Then, the circuit design methodology for a series of converter-level on-state voltage monitoring circuits is proposed and introduced. For the view of practical application, the restrictions in component selection for the proposed circuits are fully discussed. Performance testing for each proposed circuit is characterized finally.

2.1 Existing component-level on-state voltage monitoring circuits

On-state voltage refers to the voltage across power device when it is in on-state or it is in current-freewheeling state as shown in Fig.11. $V_{CE,sat}$ is the on-state voltage of power semiconductor devices (e.g, IGBT or MOSFET) and V_F is the forward voltage of freewheeling diode (FWD). Both $V_{CE,sat}$ and V_F have similar features in indicating the health condition of power devices. Therefore, only $V_{CE,sat}$ is used as a representative to analyze the failure mechanism.

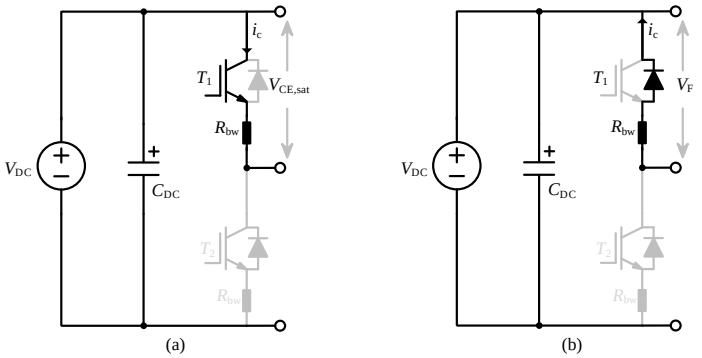


Fig. 11: On-state voltage of power devices showing in a half-bridge.

As mentioned in Chapter 1, the most frequent failure mechanisms that occur in silicon devices are related to package and are primarily attributed to the different coefficients of thermal expansion (CTE) over the materials of chip, solder, and structure layers, and the temperature fluctuation they experience [9]. Specifically, along with repeated thermal cycling, the mismatch in CTE between chip (silicon) and bond-wire (aluminum) causes stress that leads to the cracks and lift-off in bond-wires. Then, the equivalent resistance of bond-wires R_{bw} is increased as well as $V_{CE,sat}$. Another common mismatch of CTE happens between chip (silicon), solder layer (SAC305), and DBC substrate (Al_2O_3), which causes cracks and voids inside the solder layer and weakens the capability of dissipating power losses from the chip onto heatsink. Consequently, the junction temperature of power device is increased, which causes

the increase of $V_{CE,sat}$ as well. For silicon carbon devices, the dominant failure mechanism is the degradation of gate oxide layer [28, 29, 40], which causes the increase of threshold voltage. Then, the device operating in saturation mode exhibits increased on-state voltage [75].

Overall, the on-state voltage is generally sensitive to all of those dominant failure mechanisms. In addition, considering the advantages discussed in Chapter 1, on-state voltage is the most widely used health indicators for power devices. Thereafter, various on-state voltage monitoring circuits have been proposed.

The main concern for on-state voltage measuring is the capability to block the high DC-Link voltage at kV level when power device is in off-state and to precisely measure the on-state voltage up to few V at mV resolution when power device is in on-state. To achieve this, researchers have been struggling to design different circuits for decades. Those circuits have different features in respect to different applications and are discussed as below.

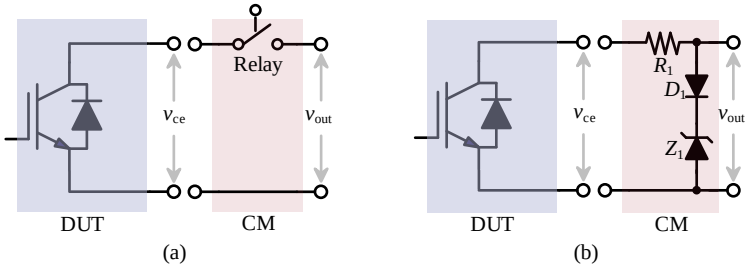


Fig. 12: Component-level on-state voltage monitoring circuits: (a) based on relay [73, 104]; (b) based on zener diode [62, 74].

The first one utilize the relay switch to block the high-voltage and pass the low-voltage as shown in Fig.12(a) [73, 104]. The main concern is the response time for relay switch, which is 3 ms in [104] and 10 ms in [73]. Therefore, the application of relay based circuit is limited. The accuracy is determined by the voltage across relay. Therefore, the input impedance of the sampling circuit in the later stage should be high enough to make sure the current flowing through the relay can be negligible. In addition, the volume of high-voltage relay should be considered and an additional control signal is needed, which makes the circuit more complex.

In addition, Zener diode can be used to replace the relay [62, 74]. In Fig.12(b), the zener voltage of Zener diode V_Z should be larger than the maximum on-state voltage and it works like this: when the input voltage v_{ce} is lower than V_Z, only very small leakage current I_l can go through R_1 and v_{out} can be expressed as:

$$v_{out} = v_{ce} - I_l R_1 \tag{4}$$

when v_{ce} is higher than V_Z, the voltage across Z_1 is claimed to V_Z and the voltage higher than V_Z is withstood by R_1. Then, v_{out} can be expressed as:

$$v_{out} = V_Z + V_{D1} \tag{5}$$

Based on the above analysis, Z_1 should be selected with low leakage current so the measurement error can be reduced. R_1 should be high-voltage resistor and its

resistance should be decided by considering the rated power of R_1, D_1, and Z_1, and the error caused by R_1. In addition, the Zener diode shows better performance than relay in response time. For example, the circuit in [74] presents 100 μs response time.

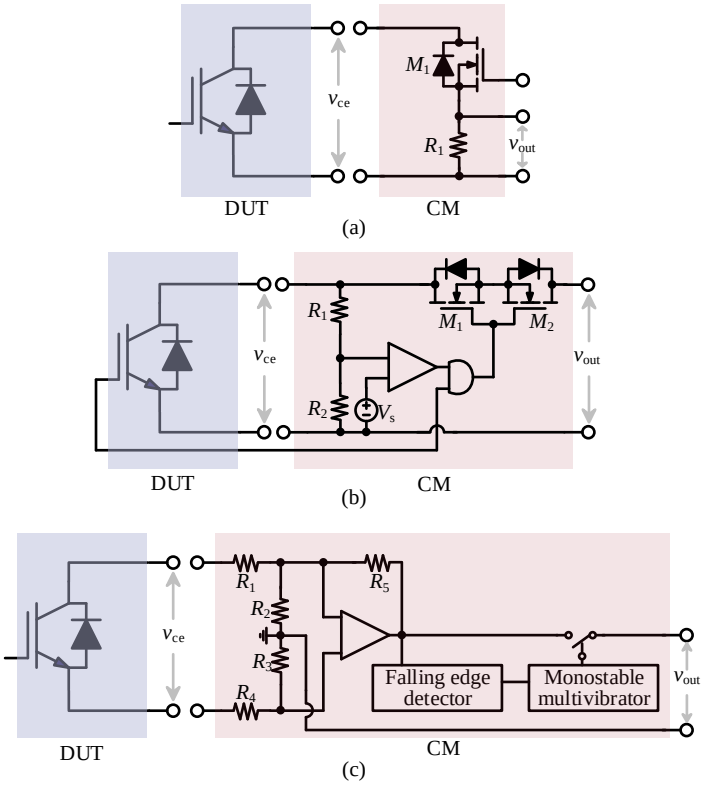


Fig. 13: Component-level on-state voltage monitoring circuits: (a) based on external controlled switch [105]; (b) based on gate driver controlled switch [81]; (c) based on collector signal controlled switch [61].

To reduce the response time, more faster switch devices are selected to block high-voltage as shown in Fig.13 [61, 77, 81, 105]. In Fig.13(a), the MOSFET is turned off when the input voltage v_{ce} is high-voltage and conducted when v_{ce} is low-voltage. Then, v_{out} can be expressed as:

$$v_{out} = v_{ce} \frac{R_1}{R_1 + R_{ds,on}} \tag{6}$$

where $R_{ds,on}$ is the on-state resistance of MOSFET and should be far smaller than R_1 so as the voltage across MOSFET can be neglected.

In Fig.13(b), the MOSFET is connected in series with the device under test (DUT). R_1 and R_2 are used to divide v_{ce}, and the voltage across R_2 is compared with the reference voltage V_s to determine if the v_{ce} is high-voltage or low-voltage. Then the

compared result is sent into an AND gate along with the gate drive signal of the DUT. Then, the output of the AND gate is used as the gate drive signal of M_1 and M_2. It can be seen that the on-off state of MOSFETs is same with that of DUT, so that the high-voltage can be bearded by M_1 and M_2 when the DUT is in off-state. When the DUT is in on-state, v_{out} can be expressed as:

$$v_{\text{out}} = v_{\text{ce}} - V_{\text{M1}} - V_{\text{M2}} \tag{7}$$

where V_{M1} and V_{M2} are the on-state voltage of M_1 and M_2, respectively.

Fig.13(c) uses four resistors R_1 - R_4 to divide v_{ce} firstly. Then, the v_{out} is obtained through a monostable multivibrator. It is controlled by a falling edge detector. Once the v_{ce} is changed from high-voltage to low-voltage, the monostable multivibrator is turned on and v_{out} can be expressed as:

$$v_{\text{out}} = v_{\text{ce}} \frac{R_2 + R_5}{R_1 + R_2 + R_3 + R_4} \tag{8}$$

after a short pre-setting time, the multivibrator will back to off-state itself.

Overall, this group of circuits has very short response time. Their accuracy is determined by the selection of components as shown in (6)-(8). Especially for Fig.13(c), the temperature sensitivity and accuracy of those resistors could impact the accuracy of v_{out} significantly. The introduction of driving signal for the switches makes those circuits a little bit complex. More importantly, introducing driving signal from the gate or collector of the DUT may risk the normal operation of DUT or the monitoring circuit itself.

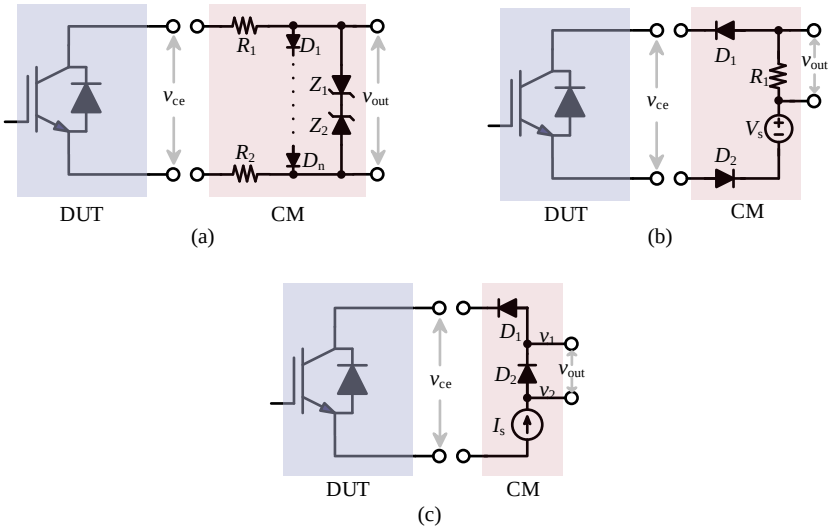


Fig. 14: Component-level on-state voltage monitoring circuits: (a) based on series connected diodes [69]; (b) based on diodes and external reference voltage source [69]; (c) based on diodes and external reference current source [72, 75].

To fix the issue caused by introducing additional gate driving signal. Diodes are used as it is able to block high-voltage and show passive characteristic [69, 72, 75]. In

Fig.14(a), multi diodes are connected in series along with two high-voltage resistors. When v_{ce} is high-voltage, those diodes are conducted and the output voltage v_{out} is claimed to:

$$v_{out} = V_{D1} + V_{D1} + ... + V_{Dn} \tag{9}$$

where V_{Dn} is the forward voltage of D_n. The high-voltage is withstood by those two resistors.

When v_{ce} is lower than the sum of the forward voltages of all diodes, those diodes are blocked and v_{out} is:

$$v_{out} = v_{ce} - V_{R1} - V_{R2} \tag{10}$$

where V_{R1} and V_{R2} are the voltage across R_1 and R_2, respectively. Z_1 and Z_2 are used as protection.

In Fig.14(b), two diodes are used to prohibit the high-voltage from reaching at the output terminal. While D_1 and D_2 are conducted by the reference voltage source V_s if v_{ce} is lower than V_s. Consequently, the output voltage can be obtained as:

$$v_{out} = V_s - V_{D1} - V_{D2} - v_{ce} \tag{11}$$

where V_{D1} and V_{D2} are the forward voltages of D_1 and D_2, respectively. For this circuit, the error is mainly caused by V_{D1} and V_{D2}. To reduce the error, Fig.14(b) is updated as shown in Fig.14(c).

In Fig.14(c), D_1 and D_2 are conducted by the current source when v_{ce} is low-voltage. Then, v_{ce} is:

$$v_{ce} = 2v_1 - v_2 + 2V_{D2} - 2V_{D1} \tag{12}$$

where V_{D1} and V_{D2} are the forward voltages of D_1 and D_2 respectively. If V_{D1} is assumed to equal with V_{D2}, v_{ce} can be accurately measured through v_1 and v_2. Therefore, the accuracy of this circuit is determined by the difference between V_{D1} and V_{D2} while measuring.

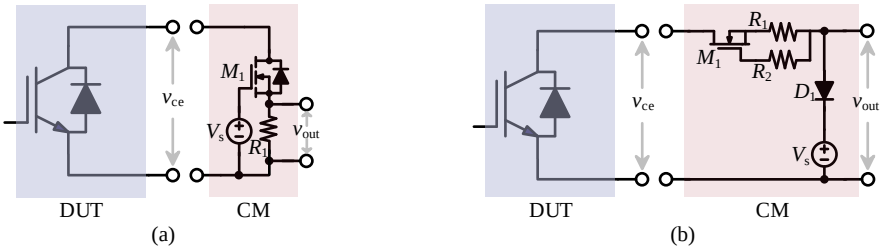


Fig. 15: Component-level on-state voltage monitoring circuits: (a) based on enforced MOSFET [71]; (b) based on depletion MOSFET [76].

To increase the accuracy further, self-controlled switches are used as shown in Fig.15 [71, 76, 106]. In Fig.15(a), the on-off state of enforced MOSFET is controlled by a gate connected voltage source and a source connected resistor. Based on this circuit, the voltage across R_1 can be expressed as:

$$V_{R1} = V_s - v_{gs} = v_{ce} - v_{M1} \tag{13}$$

then, the gate-source voltage of M_1 is:

$$v_{gs} = V_s - v_{ce} + v_{M1} \tag{14}$$

where v_{M1} is the on-state voltage of M_1. When v_{ce} is low-voltage, v_{gs} can be higher than the threshold voltage of M_1, which conducts M_1. Then, v_{out} is expressed as:

$$v_{out} = v_{ce} \frac{R_1}{R_1 + R_{ds,on}} \tag{15}$$

$R_{ds,on}$ is the on-state resistance of M_1. Therefore, if R_1 is far larger than $R_{ds,on}$, v_{ce} can be measured accurately. However, if v_{ce} is high-voltage, v_{gs} can be lower than the threshold voltage of M_1, which makes M_1 works at liner mode and withstands high-voltage.

In Fig.15(b), a depletion MOSFET is used and it works like this: if there is no current, M_1 is in on-state. While, the current going through M_1 and R_1 can forms a negative voltage between the gate and source of M_1, which makes M_1 operates at liner mode and exhibits high impedance. Based on this, if v_{ce} is lower than the reference voltage V_s, there is no current going through M_1, thus, v_{out} is:

$$v_{out} = v_{ce} \tag{16}$$

if v_{ce} is higher than V_s, v_{out} is:

$$v_{out} = V_s + V_{D1} \tag{17}$$

where V_{D1} is the forward voltage of D_1.

Tab 2 summarizes the ten typical component-level on-state voltage monitoring circuits in literature. They are discussed and analyzed in terms of circuit design, operation principle, and applicability to different applications. They are classified into five groups based on the key components to block the high-voltage and pass the low-voltage: relay, zener diode, the MOSFET with complex additional driver, general diode, and the MOSFET with simple self-driver. All of these circuits have different pros and cons in terms of response time, accuracy, and practical application.

Although the on-state voltage monitoring circuits have been developed for decades, they are still not mature enough to be implemented in practical applications. The main challenges are that all of those existing on-state voltage monitoring circuits are component-level solutions and active measurement with the requirement of external power supply, which can induce more practical issues when a power converter needs to be monitored. For example, applying those circuits in a three-phase converter: 1) It has high circuit complexity and cost to monitor six power switches; 2) It is connected to the power terminals of individual switching devices, which requires more connecting terminals; and 3) it has one reference ground for each phase-leg, which introduces isolation issue while sampling data of all devices; 4) it requires the additional power supply for each phase-leg. Overall, a converter-level on-state voltage monitoring circuit is still missing at present.

Table 2: Comparison of existing component-level on-state voltage monitoring circuits

Circuits	Response time	Accuracy	Implementation
Fig.12(a) [104]	at ms level	depends on the equivalent resistance of relay	the volume of relay and its controller can increase the size and complexity of this circuit; limited applications due to response time
Fig.12(b) [74]	at 100 μs level	depends on the leakage current of zener diode and R_1	the volume and power of R_1 should be considered since it needs to withstand high-voltage; limited applications due to response time
Fig.13(a) [105]	(1-10) μs	accuracy is high since R_1 can be far larger than $R_{ds,on}$ in (6)	additional driver for M_1 is needed;
Fig.13(b) [81]	(1-10) μs	depends on the on-state voltages of M_1 and M_2	R_1 and R_2 need to withstand high-voltage; complex circuit with internal driver for M_1 and M_2 and external power supply; the gate driver of DUT may be impacted
Fig.13(c) [61]	(1-10) μs	depends on the characteristics of R_1-R_5	R_1-R_4 need to withstand high-voltage; complex circuit with v_{ce} divider, falling edge detector, and monostable multivibrator
Fig.14(a) [69]	(1-10) μs	depends on the voltage across R_1 and R_2	R_1 and R_2 need to withstand high-voltage; the sum of the forward voltages of D_1-D_n should be higher than the maximum on-state voltage of DUT;
Fig.14(b) [69]	(1-10) μs	depends on the forward voltages of D_1 and D_2 and the reference voltage V_s	external power supply is needed; measurement error caused the forward voltage of diode is an issue
Fig.14(c) [72]	(1-10) μs	depends on the forward voltages of D_1 and D_2	measurement error can be reduced significantly if V_{D1} is same with V_{D1} as much as possible; external power supply is needed
Fig.15(a) [71]	(1-10) μs	accuracy is high since R_1 can be far larger than $R_{ds,on}$ in (15)	external power supply is needed;
Fig.15(b) [76]	(1-10) μs	high accuracy	external power supply is needed

2.2 Proposed circuits for converter-level on-state voltage monitoring

In this thesis, three converter-level on-state voltage monitoring circuits are proposed and discussed in this Section, which achieves the unique feature by connecting to the output terminals of converters, instead of the two power terminals of individual power switch as the conventional methods do as shown in Fig.16. Due to the rich operation modes of converter, the voltages across the inverter output terminals is constructed by the on-stage voltages of all power switches and diodes, and the positive/negative DC-link voltages, which enables the converter-level measurement

of on-state voltage.

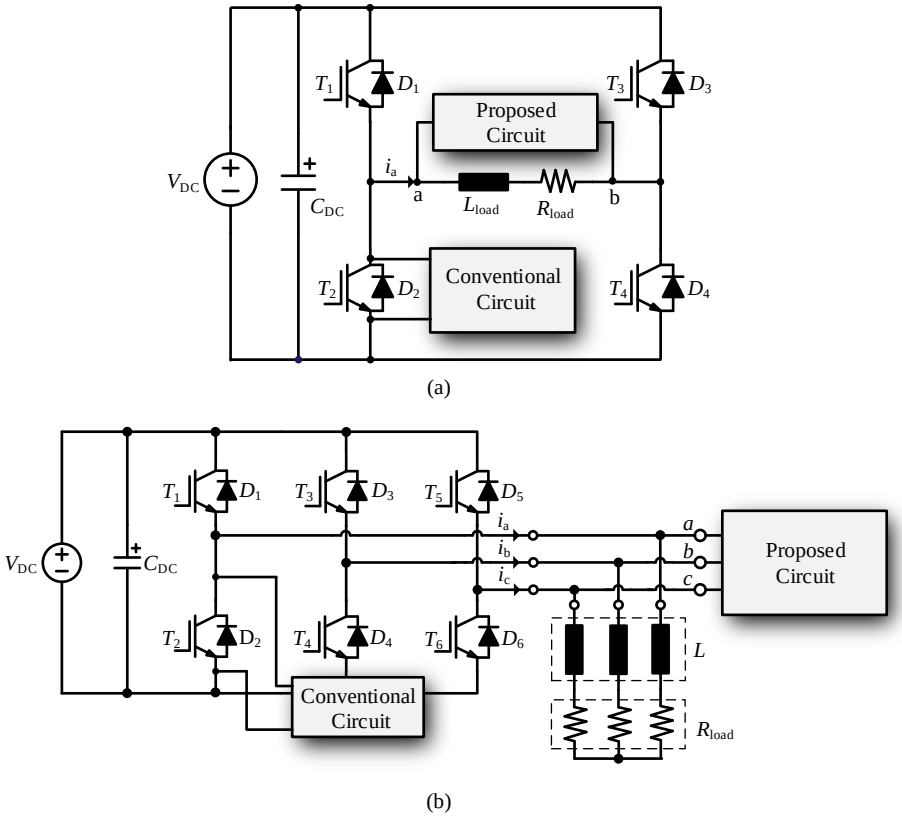


Fig. 16: Comparison of connection to power converter between conventional methods and proposed methods: (a) in single-phase inverter; (b) in three-phase inverter.

2.2.1 Proposed measurement circuit with an external power supply

To block the DC-link voltage and obtain the low on-state voltage, a measurement circuit with an external power supply is proposed as shown in Fig.17, which is composed of two symmetric parts with the function of extracting the on-state voltages from the bipolar output voltage of single-phase inverter v_{ab}. The first part is marked with blue rectangle and is composed of one signal MOSFET M_1, two diodes D_{a1} and D_{a2}, two resistors R_1 and R_2, and one positive reference voltage $V_{\mathrm{ref}+}$. This part is used to prevent any negative voltage and positive voltage higher than $V_{\mathrm{ref}+}$ from reaching at the output terminal of this circuit, and to pass the positive voltage lower than $V_{\mathrm{ref}+}$ only. The second part is marked with red rectangle, including M_2, D_{a3}, D_{a4}, R_3, R_4, and $V_{\mathrm{ref}-}$. It has opposite function with the first part, blocking any positive voltage and the negative voltage lower than $V_{\mathrm{ref}-}$ from v_{ab}, passing the negative voltage higher than $V_{\mathrm{ref}-}$. The bidirectional reference voltage is provided with an

external isolation DC-DC converter, which means this circuit is active.

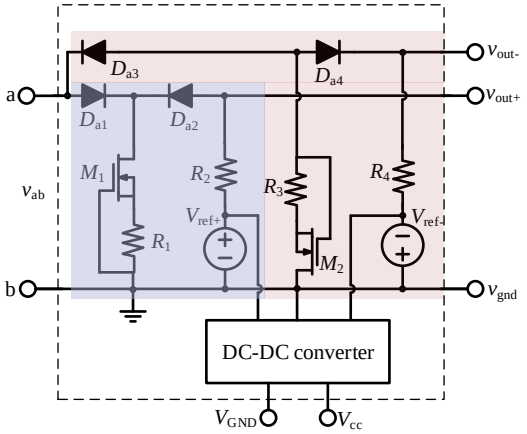


Fig. 17: Proposed converter-level on-state voltage monitoring circuit with external power supply for single-phase converter application [J2].

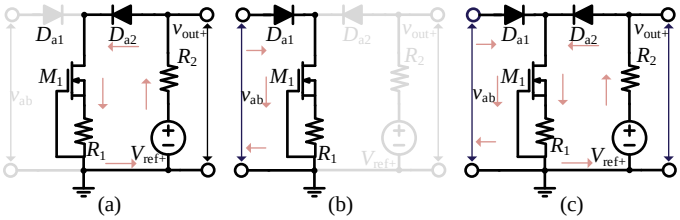


Fig. 18: Operation modes of blue part in Fig.17 [J2].

Among those devices, M_1 and M_2 are N-channel depletion MOSFET and they works like this: when there is no current flowing through M_1, for example, the gate-source voltage is zero and M_1 is in on-state; If there is current flowing through M_1, the gate-source voltage will be negative due to the positive voltage across R_1, which makes M_1 operates at liner mode and exhibits high-impedance. To simplify the analysis process, only the operation modes of blue part in Fig.17 are given as shown in Fig.18. The operation modes of red part circuit can be derived similarly.

- Model a (Fig.18(a)): when v_{ab} is negative, D_{a1} is in reverse-blocked state and D_{a2} is in conducted state, the positive output v_{out+} is:

$$v_{out+} = \frac{R_1}{R_1 + R_2}\left(V_{ref+} - V_{Da2} - V_{M1}\right) + V_{Da2} + V_{M1} \tag{18}$$

  R_1 has much smaller resistance than R_2, leading to a small v_{out+}(e.g., 1 V). V_{Da1} and V_{Da2} are the forward voltage of D_{a1} and D_{a2}, respectively. V_{M1} is the voltage across M_1.

- Model b (Fig.18(b)): when v_{ab} is positively higher than V_{ref+}, D_{a1} is conducted and D_{a2} is blocked. Then, v_{out+} equals to the reference voltage V_{ref+}.

$$v_{out+} = V_{ref+} \tag{19}$$

- Model c (Fig.18(c)): when v_{ab} is in the range of 0 and V_{ref+}, D_{a1} and D_{a2} are conducted as shown in Fig.3(c). Thus, v_{out+} can be described as:

$$v_{out+} = v_{ab} - V_{Da1} + V_{Da2} \tag{20}$$

In practice, V_{Da1} and V_{Da2} can cancel each other out substantially if D_{a1} and D_{a2} are selected with same characteristics as much as possible and are mounted together. Thus, it is reasonable to assume that v_{out+} is equal to v_{ab}. Overall, with the blue and red parts in Fig.17 together, any input voltages out of the range between V_{ref-} and V_{ref+} are clipped to the preset reference voltages, while the input voltage within that range can be measured directly. The functions of the proposed circuit are summarized in Table 3.

Table 3: Overall functions of the proposed circuit.

Modes	v_{ab}	v_{out+}	v_{out-}
I	$[V_{ref+}, +\infty]$	V_{ref+}	-1 V
II	$[0, V_{ref+}]$	v_{ab}	-1 V
III	$[V_{ref-}, 0]$	+1 V	v_{ab}
IV	$[-\infty, V_{ref-}]$	+1 V	V_{ref-}

To apply the proposed converter-level on-state voltage monitoring circuit to three-phase converters, the circuit presented in Fig.17 is partially replicated as shown in Fig.19. The sub-circuits marked with blue and red can share one external power supply due to the common reference ground b.

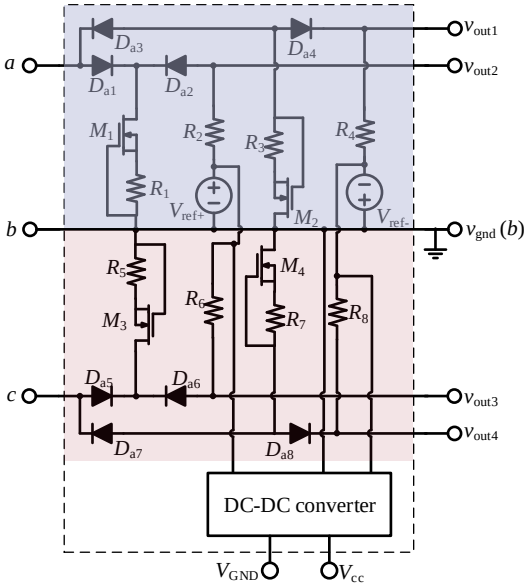


Fig. 19: Proposed converter-level on-state voltage monitoring circuit with external power supply for three-phase converter application [J3].

2.2.2 Proposed measurement circuit with self-power supply

The external power supply is existed in both the conventional methods and the proposed circuits presented in Fig.19. It usually accounts for the total cost and size of the measurement circuit for at least 90% and 30%, respectively. Moreover, two additional connecting terminals are needed for this power supply. Therefore, from the view of practical application, it would be much better if the external power supply can be removed. To address this problem, a self-power supply capable of extracting a stable bidirectional reference voltages from the input voltage is designed in this thesis, as shown in Fig.20.

D_{a9} and D_{a10} are normal diode, Z_1 and Z_2 are Zener diode and their Zener voltage is V_z, M_5 and M_6 are signal N-channel depletion MOSFET. Based on this, when the input voltage of the self-power supply is positive, D_{a9} is conducted and D_{a10} is blocked. C_1 is charged until its voltage reaches at V_z. When the input voltage is negative, D_{a9} is blocked and D_{a10} is conducted. C_2 start to charge until its voltage reaches at -V_z. According to this, the bidirectional reference voltages can be obtained by using the proposed self-power circuit and is the Zener voltage $\pm V_z$. Moreover, the proposed on-state voltage measurement circuit and self-power circuit can share a same ground, which means the isolation is unnecessary. Thus, the external power supply used in conventional methods and Fig.19 can be replaced with the proposed self-power supply.

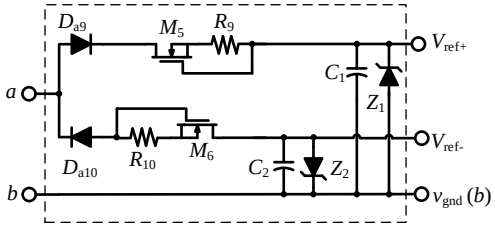


Fig. 20: Proposed self-power supply circuit [J3].

2.2.3 Proposed measurement circuit without power supply

The proposed converter-level measurement circuit with external or self-power supply outperforms conventional component-level methods in many ways. However, the circuit is still a little bit complex. To address this problem, a much simplified measurement circuit is proposed in this thesis as shown in Fig.21, which is able to achieve converter-level monitoring without external or internal (self-power) power supply.

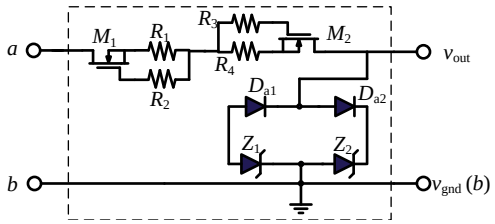


Fig. 21: Proposed converter-level on-state voltage monitoring circuit without power supply for single-phase converter application [J5].

The circuit in Fig.21 enables sampling the change of on-state voltage at mV precision. It consists of few common signal devices without power supply, making it possible to be designed as a compact circuit or a even chip. M_1 and M_2 are signal depletion MOSFET, exhibiting different impedance by controlling the source resistor (R_1 or R_4) and the gate resistor (R_2 or R_3). Z_1 and Z_2 are common Zener diodes, and its Zener voltage V_Z should be higher than the maximum value of the input signal to be measured.

If the input voltage v_{ab} is higher than V_Z, a negative voltage drop across R_2 makes M_1 exhibits high impedance, so that only a very low current (few mA) is allowed to flow. While the anti-parallel body diode of M_2 and D_{a2} are conducted, and thereby the voltage across Z_2 is clamped at V_Z. Accordingly, v_{out} can be expressed as:

$$v_{\text{out}} = V_{\text{Z}} + V_{\text{Da2}} \tag{21}$$

where V_{Da2} is the forward voltage of D_{a2}.

When v_{ab} is lower than $-V_Z$, similarly, the anti-parallel body diode of M_1 and D_{a1} are conducted. M_2 exhibits high impedance and v_{out} can be expressed as:

$$v_{\text{out}} = -V_{\text{Z}} - V_{\text{Da1}} \tag{22}$$

where V_{Da1} is the forward voltage of D_{a1}.

When v_{ab} is within the range between $-V_{\mathrm{Z}}$ and V_{Z}, diode D_{a1}, D_{a2}, Z_1 and Z_2 are all blocked and the voltages across R_1 and R_4 are zero, which means M_1 and M_2 are in on-state. Therefore, v_{out} equals to v_{ab} at this situation as shown below:

$$v_{\mathrm{out}} = v_{\mathrm{ab}} \tag{23}$$

In conclusion, the function of the proposed circuit is to block the voltage higher than V_{Z} and lower than $-V_{\mathrm{Z}}$, while pass the voltage within $-V_{\mathrm{Z}}$ and V_{Z} without error.

To apply the proposed converter-level on-state voltage monitoring circuit to three-phase converters, the circuit presented in Fig.21 is replicated as shown in Fig.22.

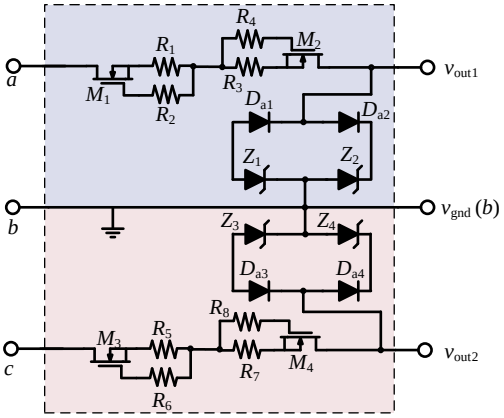


Fig. 22: Proposed converter-level on-state voltage monitoring circuit for three-phase converter application [J5].

2.3 Selection of components

Practically, the embodiment of a product-oriented electric apparatus is closely related to the selection of components in terms of performance, cost, and size. For the circuit with power supply as presented in Fig.17 and Fig.19, the components are selected by following:

- $D_{\mathrm{a1}} - D_{\mathrm{a4}}$: $D_{\mathrm{a1}} - D_{\mathrm{a4}}$ are normal diode with high-voltage endurance. Among them, $D_{\mathrm{a1}}, D_{\mathrm{a2}}$ or $D_{\mathrm{a3}}, D_{\mathrm{a4}}$ are selected with the forward characteristic as same as possible and are mounted closely on the PCB board as the measurement accuracy can be improved by canceling out the forward voltage of $D_{\mathrm{a1}}, D_{\mathrm{a2}}$ or $D_{\mathrm{a3}}, D_{\mathrm{a4}}$.
- $M_1 - M_2$: the main concern about MOSFET is the trade-off between its rated power and physical size. Higher power means higher current can flowing through MOSFET and diodes. Thus, the forward transient time of $D_{\mathrm{a1}} - D_{\mathrm{a2}}$ can be shorter, resulting in shorter response time. Meanwhile, the physical size is increased as well.
- $R_1 - R_4$: these resistors should be selected by considering the accuracy and response time of the proposed circuit, which is discussed later.

- external power supply: the bidirectional reference voltage should be higher than the maximum of the voltage to be measured.

The component selection for the proposed self-power supply circuit (Fig.20) is illustrated by following:

- D_{a9} and D_{a10}: they are normal diode capable of blocking the negative and positive DC-link voltage, respectively.
- M_5 and M_6: the main concern about MOSFET is the trade-off between its power loss. Higher current means the charge speed for C_1 and C_2 can be much faster, while the power loss of MOSFET is increased as well.
- R_9 and R_{10}: they are selected to control the current flowing through MOSFET and make sure it will not exceed the maximum power limit of MOSFET.
- C_1 and C_2: they are used to stabilize the output voltage of this circuit and can be normal SMD ceramic capacitor.
- Z_1 and Z_2: they are used to clamp the output voltage of this circuit and their Zener voltage is same with the reference voltage used in Fig.17 and Fig.19.

Regarding the proposed measurement circuit without power supply as shown in Fig.21, the components are selected by complying with the rules below:

- M_1 and M_2: in this circuit, the current flowing through MOSFET should be as lower as possible. Thus, the considerations for M_1 and M_2 are voltage rating and physical size.
- $R_1 - R_4$: they are selected to control the current flowing through MOSFET and make sure it will not exceed the maximum power limit of MOSFET.
- D_{a1} and D_{a2}: they are used to protect Z_2 and Z_1 from forward conduction, respectively.
- Z_1 and Z_2: their Zener voltage should be higher than the low-voltage to be measured.

2.4 Performance testing

Table 4: Selected components for the proposed measurement circuit in Fig.19 (the selection of this components is for the converter with the DC-link voltage up to 400 V).

Components	Specification	Components	Specification
$D_{a1} - D_{a8}$	ES1JR2 (600 V/1 A)	$M_1 - M_4$	BSS126 (600 V/17 mA)
R_1, R_3, R_5, R_7	200 Ω (SMD)	R_2, R_4, R_6, R_8	6.8 kΩ (SMD)

Table 5: Selected components for the proposed measurement circuit in Fig.22 (the selection of this components is for the converter with the DC-link voltage up to 400 V).

Components	Specification	Components	Specification
$D_{a1} - D_{a4}$	BAS70-04(70 V/200 mA)	$M_1 - M_4$	BSS126 (600 V/17 mA)
R_1, R_3, R_5, R_7	3.3/1.8/1/0.22 kΩ (SMD)	R_2, R_4, R_6, R_8	1 kΩ (SMD)
$Z_1 - Z_4$	BZV55-C6V2 (6.2 V/10 mA)		

Based on the component selection rules described before, the components selected for the measurement circuits with/without power supply are listed in Table 4 and Table 5, respectively. Thereafter, the static accuracy test and dynamic response test of the proposed measurement circuits are designed and carried out.

2.4.1 Accuracy analysis

For the accuracy testing, the input voltage v_{in} of the proposed measurement circuits is the static DC voltage. Both the input voltage and the output voltage v_o are measured simultaneously by using a multimeter at mV level resolution. Meanwhile, the corresponding percentage error between the measured v_{in} and v_o is calculated as well.

Fig.23 gives the testing results. The relative error with the measurement circuit with external/self power supply is 0 when the v_{in} is about 1.75 V. Then, it is increased until v_{in} reaches at 2.8 V. After that, the relative error decreases with the input voltage slowly. This phenomenon is due to the difference between V_{Da1} and V_{Da2} for example. The currents flowing through D_{a1} and D_{a2} are different as the input voltage is changed. The maximum relative error with the selected components is 1.75% when the v_{in} is 3.6 V.

The change trend of ε_r can be roughly analyzed with the help of the measurement circuit in Fig.17 and the component listed in Table 4. If the input voltage is from 1 V to 5 V and the V_{ref+} is 9 V, the voltage drop in R_2 ranges from 8 V to 4 V by roughly assuming V_{Da1} and V_{Da2} can be canceled with each other. Consequently, the current flowing through D_{a2} (I_{Da2}) decreases from 1.2 mA to 0.6 mA. On the other side, with the input voltage increases from 1 V to 5 V, the voltage drop in M_1 and R_1 increases from 0.5 V to 4.5 V by assuming a constant 0.5 V drop in D_{a1}. However, it is difficult to quantitatively determine the specific voltage drop in M_1 or R_1 due to the variable impedance of M_1. Thus, the voltage drop in R_1 is measured and it increases from 0.4 V to 0.9 V with the increasing input voltage. Consequently, the current flowing through D_{a1} (I_{Da1}) increases from 0.8 mA to 3.9 mA. The change trend of I_{Da1} and I_{Da2} are depicted in Fig.24. To summarize, as increasing v_{in} from 1 to 5 V, I_{Da1} and I_{Da2} present opposite change trend, resulting that the ε_r increases from negative to positive. Based on the above analysis, I_{Da1} and I_{Da2} can be changed by adjusting R_1, R_2, and the reference voltage. Then, the variation range of ε_r can be consequently changed or narrowed.

For example, if R_2 is replaced with a 1.8 kΩ resistance, the accuracy distribution is depicted in Fig.23(b). It shows the relative error ε_r is limited to 1% after the V_{in} is

higher than 3.8 V. Especially, ε_r is zero when the V_{in} is 4.91 V. Similarly, increasing reference voltage can also change the accuracy distribution as shown in Fig.23(c). The point with zero ε_r is moved to V_{in}=3.35 V and the range of ε_r less than 1% is moved to V_{in}>2.8 V. Therefore, based on different applications, the relative error of the proposed active measurement circuit can be limited to $\pm$1% for a certain input voltage range by selecting proper components. It is worth mentioning that the minimum input voltage will be increased by decreasing R_2 or increasing V_{ref+}. Because the voltage across M_1 and R_1 is increased so that D_{a1} cannot be conducted with lower input voltage.

Compared to the measurement circuits with external/self power supply, the proposed measurement circuit without power supply has much lower relative error. It is less than 0.12% when the v_{in} is lower than 5 V and does not require any off-line accuracy calibration as shown in Fig.25. When the v_{in} is lower than the clamp voltage of the selected zener diode, the current circulating in this circuit is zero, which causes almost zero error.

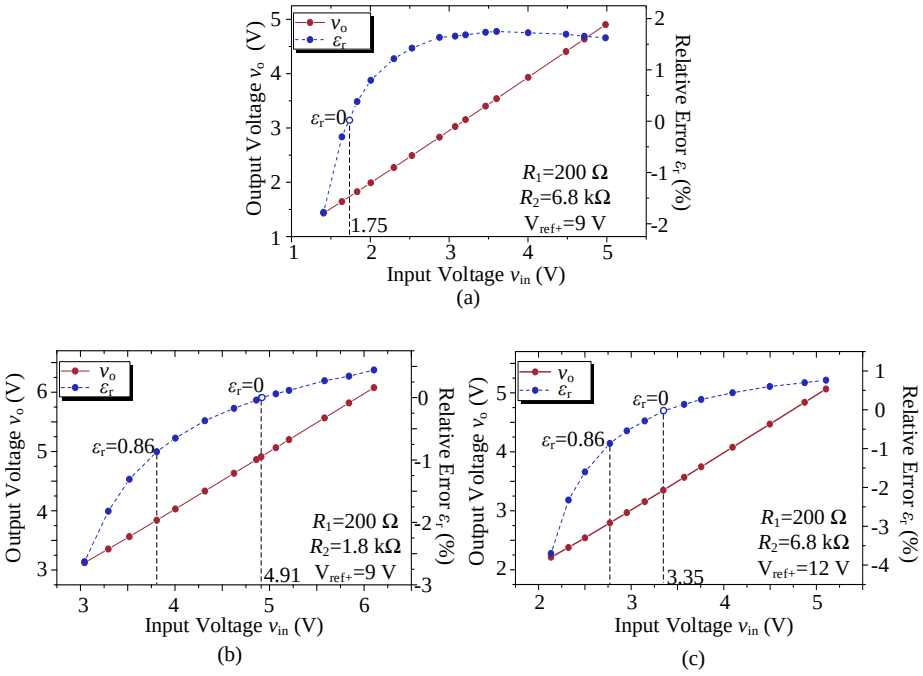


Fig. 23: Results of the static accuracy test of the proposed measurement circuits with external/self power supply [J3] ($\varepsilon_r = (v_o - v_{in})/v_{in}$): (a) R_1=200 Ω, R_2=6.8 kΩ, V_{ref+}=9 V; (b) R_1=200 Ω, R_2=1.8 kΩ, V_{ref+}=9 V; (c) R_1=200 Ω, R_2=6.8 kΩ, V_{ref+}=12 V.

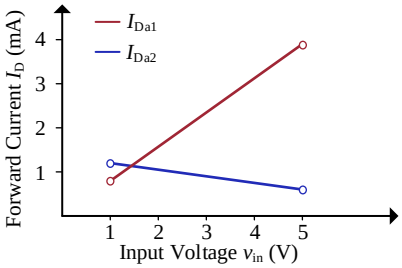


Fig. 24: Change trend of the current flowing through D_{a1} and D_{a2} when the input voltage increases from 1 V to 5 V.

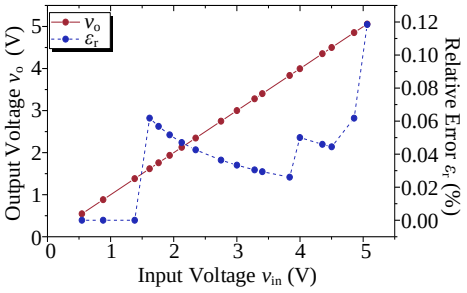


Fig. 25: Results of the static accuracy test of the proposed circuit without power supply [J5].

2.4.2 Dynamic response testing

the step response performance of the proposed circuits is tested with the rising and falling step-change input voltage, respectively, as shown in Fig.26 and Fig.27. The dynamic response of the measurement circuits with external/self power supply are better than that of measurement circuit without power supply, presenting almost zero delay time, no matter in rising or falling testing. While the circuit without power supply presents 200-800 ns rising time and falling time to follow the step-change signal based on different resistance selections. It is due to the internal capacitance (pF-level) of the measurement probe. Especially the parallel connected parasitic capacitances (pF-level) of the D_{a1}, D_{a2}, and Z_1, Z_2 in the proposed measurement circuit, as shown in Fig.28. Those capacitances need to discharge and charge during operation, which consumes time. For the measurement circuits with power supply, the discharge/charge time is negligible due to the sufficient current provided by the power supply. While, for the measurement circuit without power supply, the charge current comes from the input voltage, which is controlled by R_1 and R_3, for example, the operating current in circuit without power supply is less than 5 mA in this case study. Therefore, the smaller R_1 and R_3 are used, the higher charge current is induced, and the fast response can be obtained as shown in Fig.27.

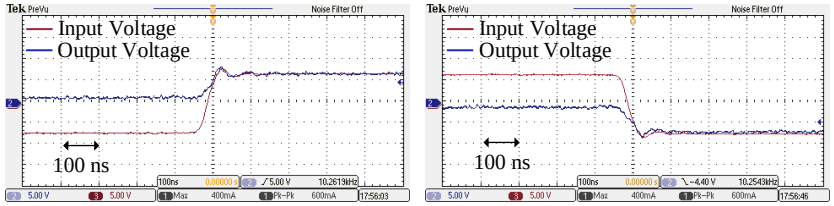


Fig. 26: Results of the dynamic response testing of the proposed measurement circuits with external/self power supply by using the components listed in Table 4 [J3]: (a) rising step-change; (b) falling rising step-change.

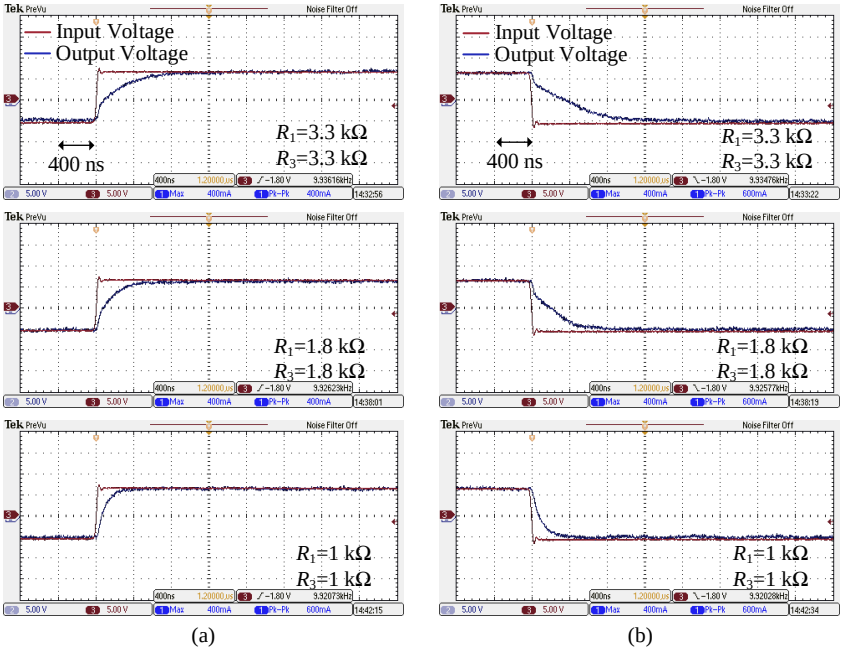


Fig. 27: Results of the dynamic response testing of the proposed measurement circuit without power supply: (a) rising step-change; (b) falling rising step-change.

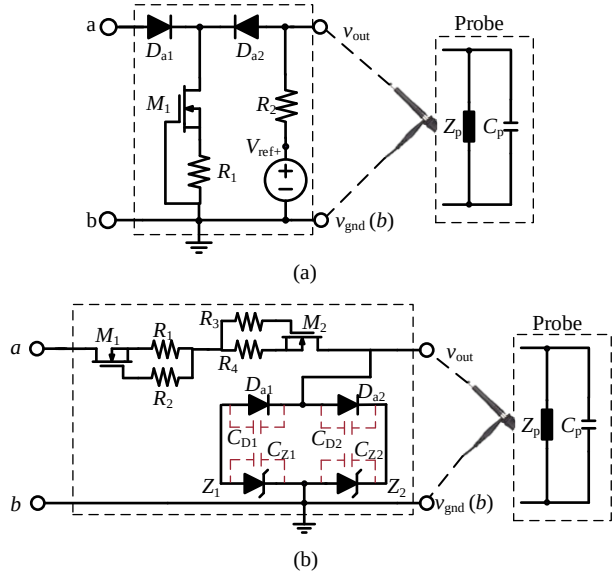


Fig. 28: Proposed measurement circuits with parasitic capacitances and measurement probe: (a) with external/self power supply; (b) without power supply.

Further, if the R_1 and R_3 in the measurement circuit without power supply are set to 220 Ω, the rising time to follow the step-change input voltage is less than 50 ns, as shown in Fig.29. The charge current at this case study is 4 mA, which does not exceeds the maximum limitation of the selected components.

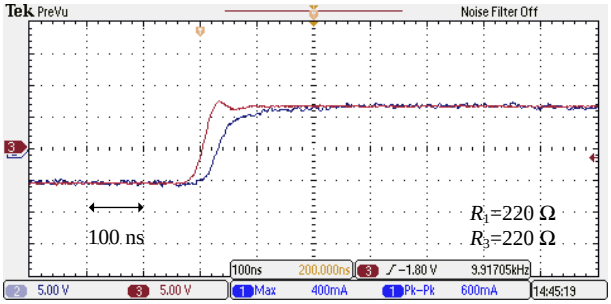


Fig. 29: Achieved fast response of the proposed measurement circuit without power supply [J5].

2.5 Summary

In this Chapter, a series of converter-level on-state voltage measurement circuits are proposed and discussed, including a measurement circuit with external power supply, a measurement with self-power supply, and a simplified measurement circuit without power supply. the evolution of circuit design methodology, operation

principle, and implementation are introduced. Moreover, the restrictions and requirements in component selection and performance testing of the proposed measurement circuits are given. Also, This chapter reviews ten typical component-level on-state voltage measurement circuits in terms of circuit design, operation principle, and applicability firstly, and they are divided into five groups to discuss their merits and shortcomings.

3 Application of the converter-level on-state voltage measurement circuits

This chapter presents the applicability of the proposed measurement circuits, as shown in Fig.30, to different power converters. Particularly, concept and practical implementation are proved with single/three-phase inverters case studies. Then, the applications of proposed circuits are extended to other power converters comprised of one or more phase legs and even a single power semiconductor. Moreover, the ability of the proposed circuits to monitor the junction temperature and degradation of power devices is verified as well.

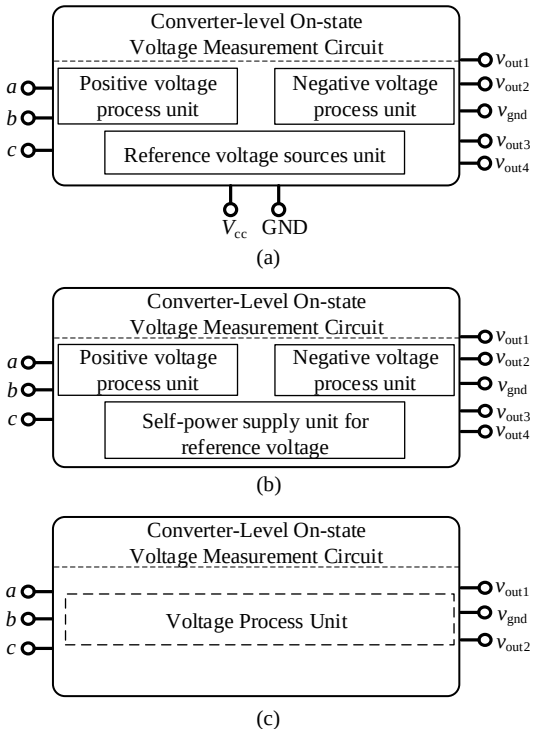


Fig. 30: Three versions of the proposed converter-level measurement circuits for on-state voltage: (a) with an external power supply; (b) with an self power supply; (c) without power supply.

3.1 Implementation in a single-phase inverter

Single-phase inverter, as shown in Fig.31, is widely used in many applications, such as Photovoltaics, data center, and uninterruptible power supply, etc.

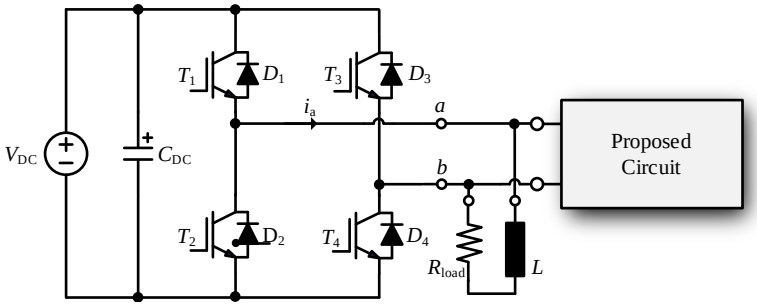


Fig. 31: Implementation in single-phase inverter.

3.1.1 Theoretical analysis

In principle, there are three modulation methods to design controller for single-phase inverter: bipolar SPWM, unipolar SPWM, and hybrid SPWM modulations. With those modulations, one typical difference is the output line voltage v_{ab} as shown in Fig.32. Among them, the v_{ab} with bipolar SPWM merely contains the positive and negative DC-link voltages only, making it impossible to extract the on-state voltages from v_{ab}. An optional solution for this situation is to intentionally operate the converter with unipolar or hybrid modulation for a short-time as the measurement window of on-state voltage. Thus, the proposed circuits are applicable to many single-phase inverter applications.

The inverter with unipolar SPWM modulation is used as an example to illustrate its output voltage v_{ab} in different operation modes in this thesis. Based on the current direction and the on-off information of switches, eight operation modes can be drawn as shown in Fig.33. By referring to those modes, the waveforms of output voltage v_{ab} and current i_a can be drawn as shown in Fig.34. It includes the on-state voltages and DC-link voltages alternatively. Therefore, With the function of the proposed circuits, the low on-state voltage can be measured. There is a little bit difference in the measured results with different converter-level measurement circuits as shown in Fig.35. With the proposed measurement circuits with external/self power supply, there are two output signals for a single-phase inverter as shown in Fig.35(a) and (b). While there is only one output signal as shown in Fig.35(c) if the circuit without power supply is used.

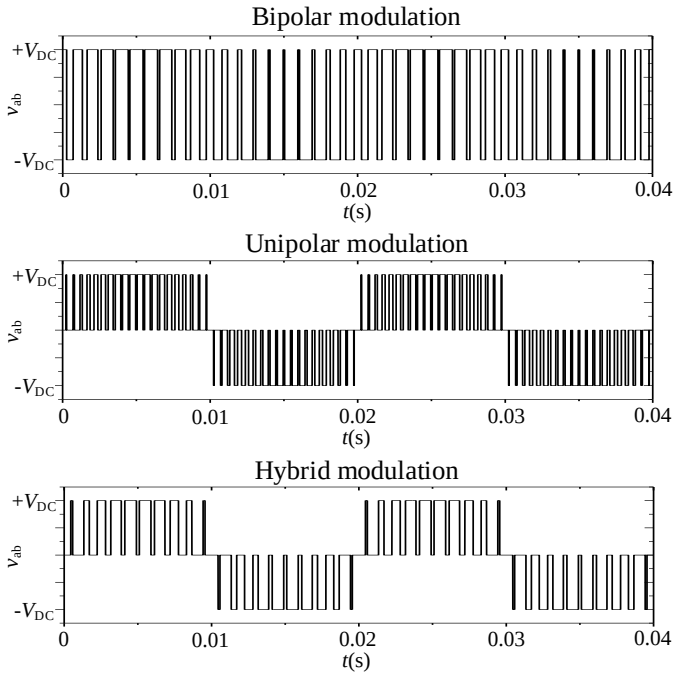


Fig. 32: Output voltage across the middle-point of phase-legs in single-phase inverter with three different modulation methods [J2].

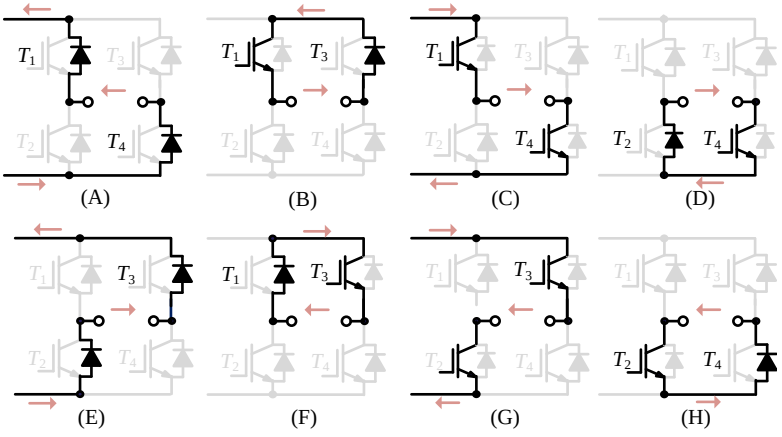


Fig. 33: Operation modes of the single-phase inverter with unipolar or hybrid modulation method [J2].

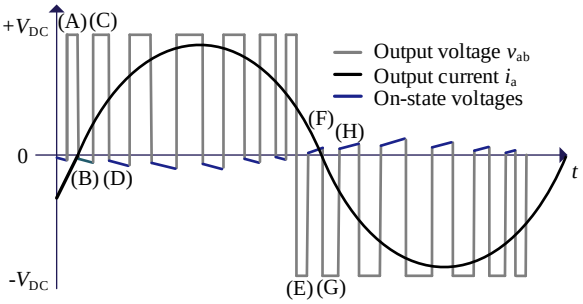


Fig. 34: Output voltage v_{ab} and current i_a of the single-phase inverter over one fundamental period [J2].

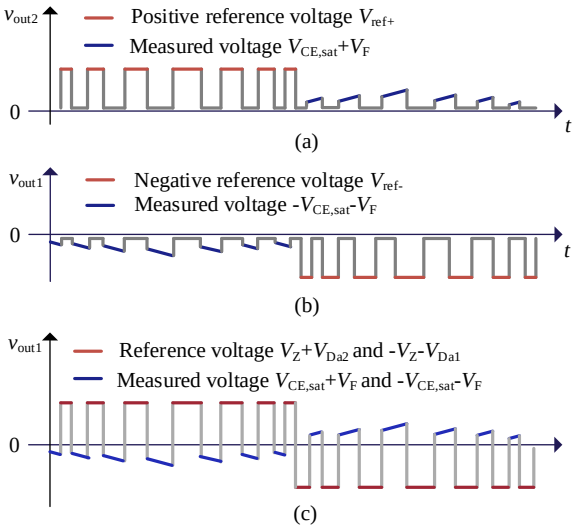


Fig. 35: Theoretical output waveforms of the proposed circuits [J2]: (a) v_{out2} in Fig.19; (b) v_{out1} in Fig.19; (c) v_{out1} in Fig.22;.

By referring to Fig.34 and 35, the expressions of output voltage v_{ab} and the measured voltages with proposed circuits at different modes are listed in Table 6. V_{DC} is the dc-link voltage, $V_{CE,sat1}$-$V_{CE,sat4}$ represent the on-state voltage of T_1-T_4 respectively, and V_{F1}-V_{F4} indicate the forward voltage of D_1-D_4 respectively. Base on the above analysis, all the on-state voltages in a single-phase inverter can be extracted over one fundamental period.

Table 6: The Output Voltages of the Inverter with Unipolar SPWM Modulation and Proposed Circuits in Different Operation Modes

Modes	v_{ab}	v_{out2} in Fig.19	v_{out1} in Fig.19	v_{out1} in Fig.22
(A)	V_{DC}+V_{F1}+V_{F4}	V_{ref+}	-1 V	V_Z+V_{Da2}
(B)	-$V_{CE,sat1}$-V_{F3}	+1 V	-$V_{CE,sat1}$-V_{F3}	-$V_{CE,sat1}$-V_{F3}
(C)	V_{DC}-$V_{CE,sat1}$+$V_{CE,sat4}$	V_{ref+}	-1 V	V_Z+V_{Da2}
(D)	-$V_{CE,sat4}$-V_{F2}	+1 V	-$V_{CE,sat4}$-V_{F2}	-$V_{CE,sat4}$-V_{F2}
(E)	-V_{DC}+V_{F3}+V_{F2}	+1 V	V_{ref-}	-V_Z-V_{Da1}
(F)	$V_{CE,sat3}$+V_{F1}	$V_{CE,sat3}$+V_{F1}	-1 V	$V_{CE,sat3}$+V_{F1}
(G)	-V_{DC}+$V_{CE,sat3}$+$V_{CE,sat2}$	+1 V	V_{ref-}	-V_Z-V_{Da1}
(H)	$V_{CE,sat2}$+V_{F4}	$V_{CE,sat2}$+V_{F4}	-1 V	$V_{CE,sat2}$+V_{F4}

3.1.2 Experimental testing

To test the feasibility and effectiveness of the proposed circuits, a testing platform is built as shown in Fig.36, consisting of a single-phase inverter and the proposed measurement circuit. The device under test (DUT) is a 1200 V/50 A IGBT module (F4-50R12KS4). The specifications of this platform are detailed in Table 7.

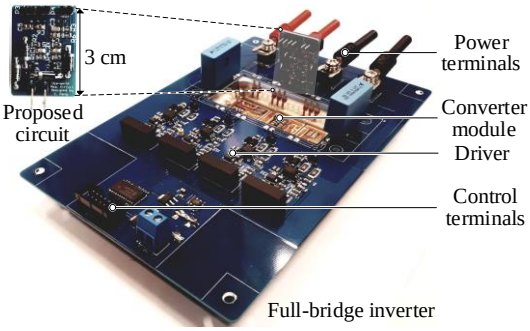


Fig. 36: Prototype of the proposed circuit connected to a single-phase inverter demonstrator [J2].

Table 7: Specifications for the experimental platform.

Parameter	Value	Parameter	Value
DC-link voltage	400 V	Output current (peak)	10-20 A
Switching frequency	10 kHz	Dead time	2 μs
Fundamental frequency	50 Hz	Inductor	1 mH
Load	10 Ω	Modulation	Unipolar SPWM

Firstly, the proposed active measurement circuit is tested and the corresponding results are presented in Fig.37. Clearly, the on-state voltages appeared in v_{out1} and v_{out2} are measurable with common data acquisition equipment since the DC-link voltages have been clipped to the reference voltage that can be adjusted accordingly.

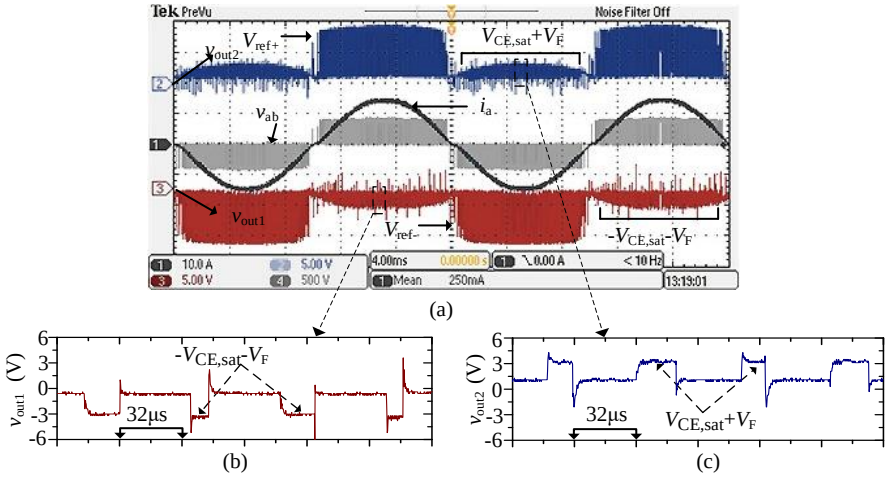


Fig. 37: Measured results from the testing platform with the proposed active measurement circuit [J2]: (a) results over two fundamental period; (b) enlarged part from v_{out1}; (c) enlarged part from v_{out2};.

As mentioned in Chapter 2, the proposed measurement circuit with the external power supply that results in increased cost, size, and complex implementation. Alternatively, a self power circuit is designed to replace the external power supply. Due to this, the reference voltage can be directly obtained from the output voltage of inverter (e.g., v_{ab}) without affecting the functioning inverter as shown in Fig.38. A $\pm$6.2 V bidirectional voltage is effectively obtained, which can be changed by replacing the zener diodes in Fig.20 with different Zener voltage.

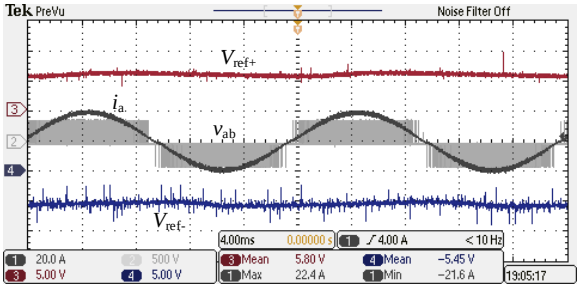
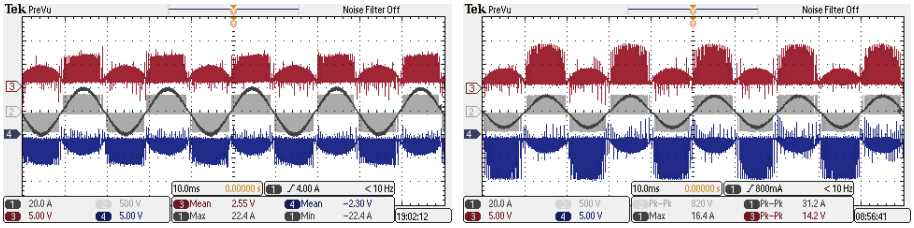


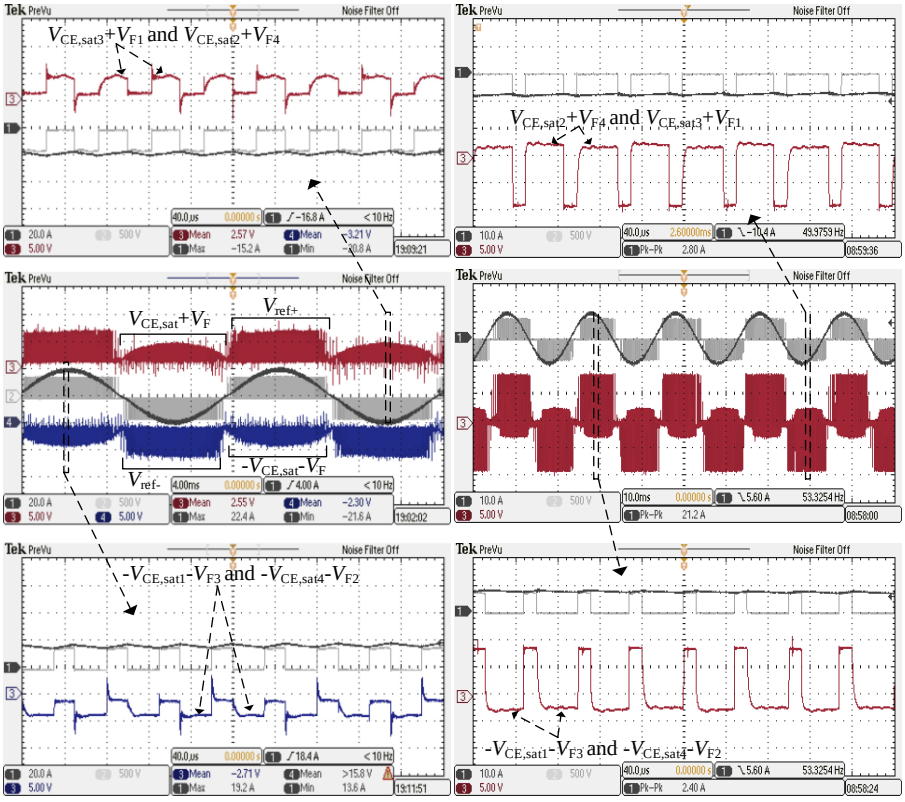
Fig. 38: Bidirectional reference voltage extracted from the output voltage of inverter v_{ab} by using the proposed self-power circuit shown in Fig.20 [J3].

Thereafter, the testings with the measurement circuits with external/self power supply are carried out respectively and the results are comparatively displayed in Fig.39. Functionally, there is no distinct difference between them. However, physically, regarding to the circuit with self power supply, the cost and size are reduced and there is no isolation issue between the main power stage and the measurement circuit.



(a) (b)

Fig. 39: Comparison of the measured on-state voltage waveforms from the proposed circuits [J3]: (a) with self power supply; (b) with external power supply.



(a) (b)

Fig. 40: Measured results from the testing platform: (a) by using the proposed measurement circuit with power supply [J3]; (b) by using the proposed measurement circuit without power supply [J5].

Then, the experimental results of the proposed measurement circuit with external/self power supply are displayed in Fig.40(a) and (b) , respectively. It demonstrates

that the bidirectional DC-link voltage is clipped to a pre-set bidirectional reference voltage. Whereas the on-state voltages included in v_{ab} become detectable. It should be noticed that $V_{CE,sat3}+V_{F1}$ and $V_{CE,sat2}+V_{F4}$, for example, are existed in the measured signal alternatively with the sum format. They can be separated by levering the rich combinations of measured on-state voltages in three-phase converter.

To acquire the on-state voltage data, a 14-bit AD converter is used. The input range of this AD is $\pm$10 V and the symbol $\pm$ is decided by the first bit. The sampling frequency is set to the double switching frequency. Then, the sampled on-state voltages by using the measurement circuits with/without power supply are shown in Fig.41(a) and (b), respectively. In Fig.41(a), during the positive half period of current i_a, the measured data are $V_{CE,sat1}+V_{F3}$ and $V_{CE,sat4}+V_{F2}$ and they are changing along with i_a. In contrast, $V_{CE,sat3}+V_{F1}$ and $V_{CE,sat2}+V_{F4}$ are measured during the another half period. In Fig.41(b), the measured data are similar with that of Fig.41(a), except for that all of the on-state voltages in the single-phase inverter are included in one output signal only.

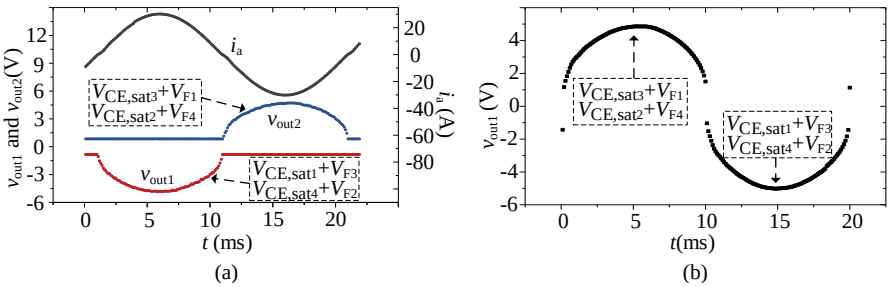


Fig. 41: Measured results from the testing platform: (a) by using the proposed measurement circuit with power supply [J3]; (b) by using the proposed measurement circuit without power supply [J5].

3.2 Implementation in a three-phase inverter

Three-phase inverter is one of the most widely used converters, ranging from wind turbine, PV, EV, train traction to aircraft, etc. Therefore, the implementation of the proposed measurement circuits in three-phase inverter is investigated as shown in Fig.42.

3.2.1 Theoretical analysis

Initially, the operational modes of three-phase inverter are investigated to figure out the compositions of the voltage across the middle-point of each phase-leg. To simplify the analysis process, only the combination of phase leg *a* and *b* is taken as an example, the combination of phase leg *c* and *b* can be derived similarly. In principle, there are twelve modes referring to two phase-legs in a three-phase inverter as shown in Fig.43. They are sequentially and periodically appeared according to the current direction and the on-off information of power switches.

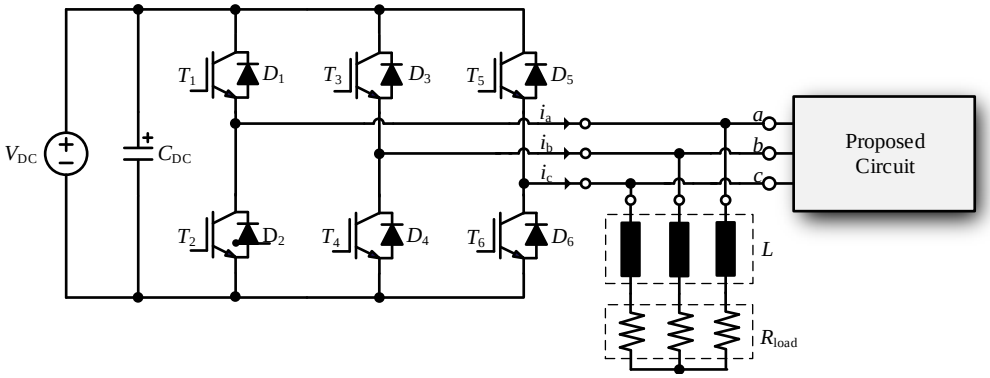


Fig. 42: Connection of proposed measurement circuits to the three-phase inverter.

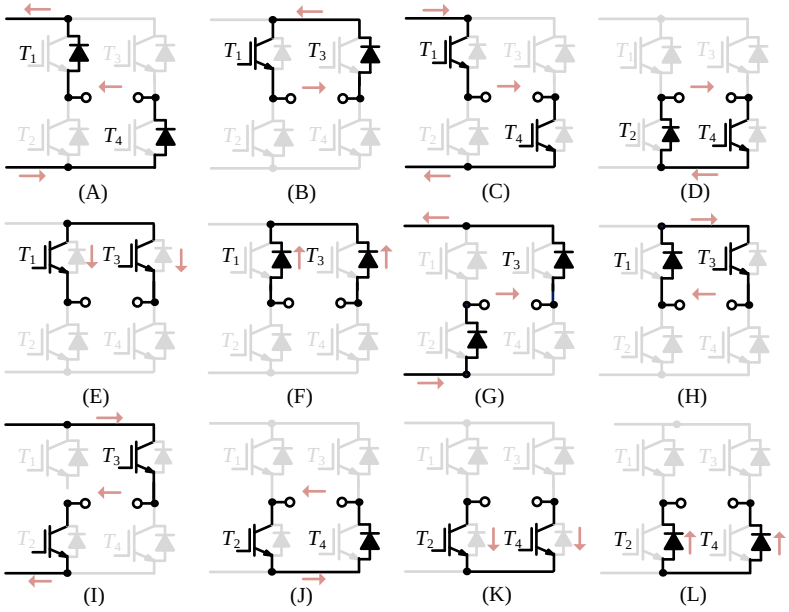


Fig. 43: Potential operation modes of phase a and b in a three-phase inverter with SPWM or SVPWM modulation.

The corresponding expression of v_{ab} at each mode is listed in Table 8. Except for the bidirectional DC-link voltages, the on-state voltage of $T_1 - T_4$ and the forward voltage of $D_1 - D_4$ are existed in the format of mutual addition or subtraction. Likewise, it is reasonable to expect that the on-state voltage of $T_3 - T_6$ and the forward voltage of $D_3 - D_6$ are included in v_{cb}. Considering the function of the proposed measurement circuits, those voltage combinations consisting of on-state voltages are able to be measured accurately by using normal data acquisition equipment since the

DC-link voltages are clipped to a pre-set low reference voltage and they are listed in Table 9. Particularly, the term "Non" in Table 9 means the value is not decided. For example, at mode (E), if $V_{CE,sat3} > V_{CE,sat1}$, v_{out1} is -1 V and v_{out2} is $V_{CE,sat3} - V_{CE,sat1}$. In contrast, if $V_{CE,sat3} < V_{CE,sat1}$, v_{out1} is $V_{CE,sat3} - V_{CE,sat1}$ and v_{out2} is +1 V.

Table 8: Expressions of output voltage v_{ab} in three-phase inverter at different operation states

Modes	v_{ab}	Modes	v_{ab}
(A)	$V_{DC} + V_{F1} + V_{F4}$	(G)	$-V_{DC} - V_{F3} - V_{F2}$
(B)	$-V_{CE,sat1} - V_{F3}$	(H)	$V_{CE,sat3} + V_{F1}$
(C)	$V_{DC} - V_{CE,sat1} - V_{CE,sat4}$	(I)	$-V_{DC} + V_{CE,sat3} + V_{CE,sat2}$
(D)	$-V_{CE,sat4} - V_{F2}$	(J)	$V_{CE,sat2} + V_{F4}$
(E)	$V_{CE,sat3} - V_{CE,sat1}$	(K)	$V_{CE,sat2} - V_{CE,sat4}$
(F)	$V_{F1} - V_{F3}$	(L)	$V_{F4} - V_{F1}$

Table 9: Expressions of output voltages of proposed converter-level on-state voltage measurement circuits (Non means the value dependents on v_{ab}).

Modes	v_{out1} in Fig.19	v_{out2} in Fig.19	v_{out1} in Fig.22
(A)	-1 V	V_{ref+}	$V_Z + V_{Da2}$
(B)	$-V_{CE,sat1} - V_{F3}$	+1 V	$-V_{CE,sat1} - V_{F3}$
(C)	-1 V	V_{ref+}	$V_Z + V_{Da2}$
(D)	$-V_{CE,sat4} - V_{F2}$	+1 V	$-V_{CE,sat4} - V_{F2}$
(E)	Non	Non	$V_{CE,sat3} - V_{CE,sat1}$
(F)	Non	Non	$V_{F1} - V_{F3}$
(G)	V_{ref-}	+1 V	$-V_Z - V_{Da1}$
(H)	-1 V	$V_{CE,sat3} + V_{F1}$	$V_{CE,sat3} + V_{F1}$
(I)	V_{ref-}	+1 V	$-V_Z - V_{Da1}$
(J)	-1 V	$V_{CE,sat2} + V_{F4}$	$V_{CE,sat2} + V_{F4}$
(K)	Non	Non	$V_{CE,sat2} - V_{CE,sat4}$
(L)	Non	Non	$V_{F4} - V_{F1}$

3.2.2 Experimental testing

A three-phase inverter testing platform is developed firstly as shown in Fig.44. Its operational specifications are same with the single-phase inverter platform (refer to Table 7). The DUT is a 1200 V/50 A IGBT module (Infineon-FS50R12KT4).

Fig.45 presents the hardware realization of proposed measurement circuit for three-phase inverter application. A 3D printing housing is used to provide mechanical support and protection. The input terminals are general laboratory-use banana terminals that are plug-and-play connectors. The output terminals are SMA connectors and can be connected with other type of terminals through suitable terminal-adapter.

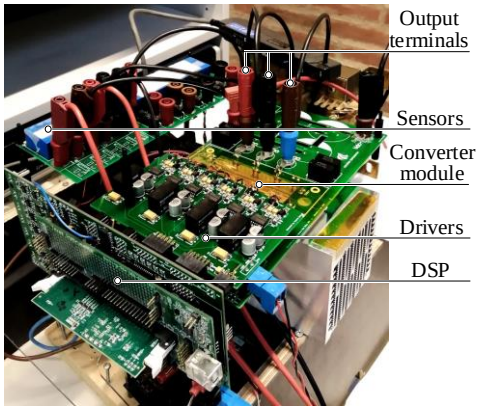


Fig. 44: Testing platform [J3].

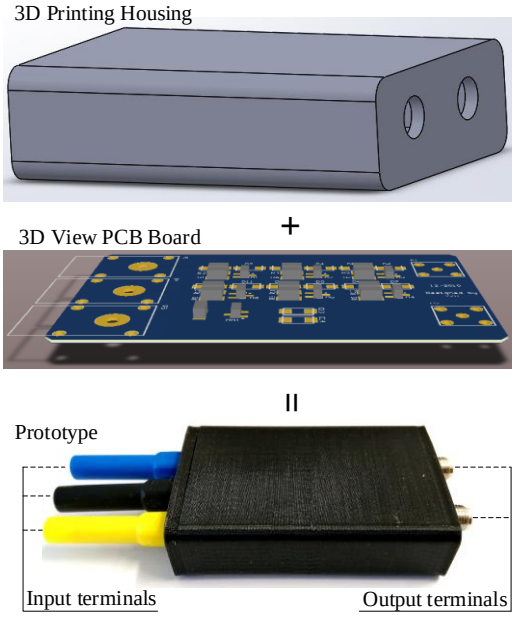
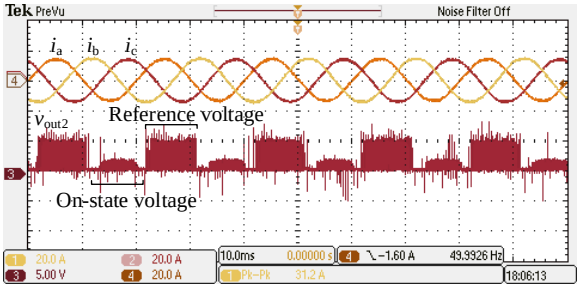
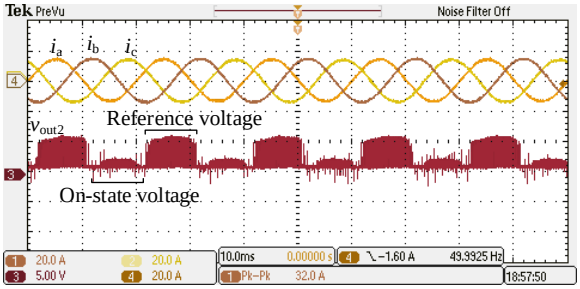


Fig. 45: Prototype of proposed measurement circuit without power supply [J3].

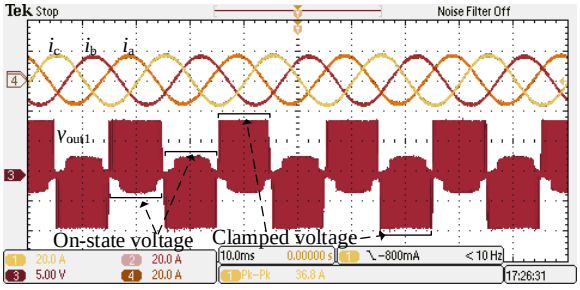
Thereafter, the prototypes of proposed measurement circuits are applied to the functioning three-phase inverter one by one to verify their effectiveness. Part of the testing results is presented in Fig.46. Apparently, all of those three measurement circuits are able to the DC-link voltages and make the on-state voltages detectable from the output line voltages of three-phase inverter.



(a)



(b)



(c)

Fig. 46: Measured results from three-phase inverter by the proposed on-state voltage measurement circuits [J3]: (a) with external power supply; (b) with self power supply; (c) without power supply.

Similarly, a 14-bit AD converter is used as well to acquire the digital on-state voltage data. For instance, the sampled on-state voltages of T_1, T_3, D_1, and D_3 by using the proposed measurement circuit are presented in Fig.47, which differs from the results obtained from single-phase inverter with two more modes: $V_{F1} - V_{F3}$ and $V_{CE,sat3} - V_{CE,sat1}$.

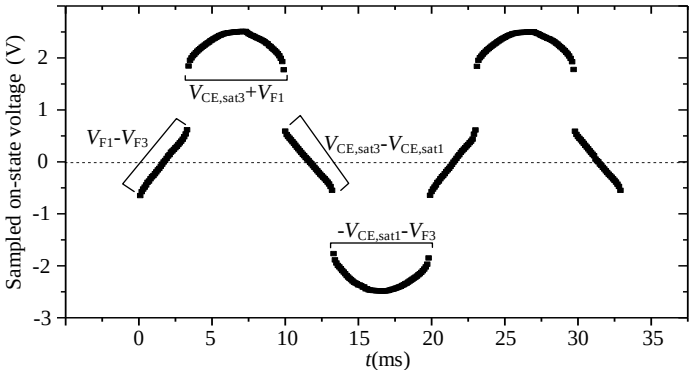


Fig. 47: Sampled on-state voltages of T_1, T_3, D_1, and D_3 [J5].

The sampled on-state voltages in this three-phase inverter are presented in Fig.48. Based on this, the changes of on-state voltage occurred in any power semiconductors of a three-phase inverter can be detected by the proposed measurement circuits.

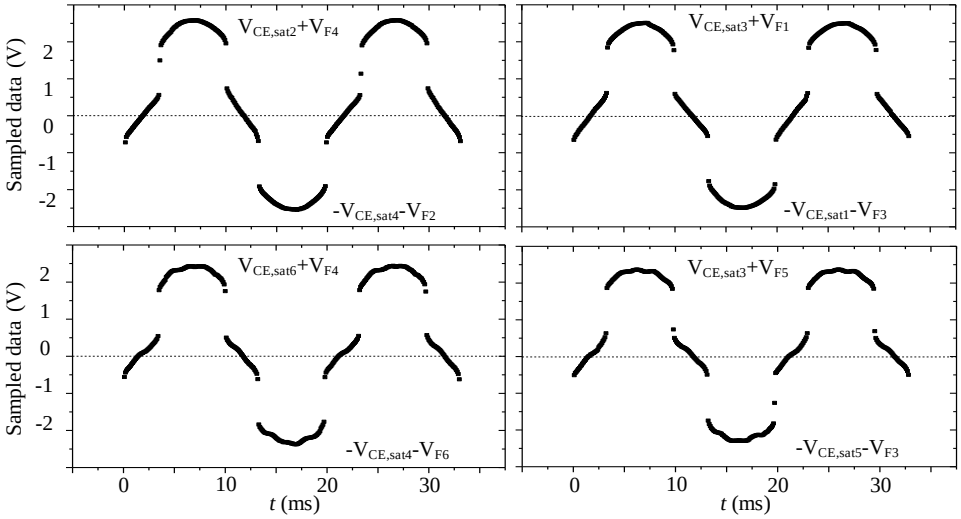


Fig. 48: Sampled on-state voltages of all power semiconductors in a three-phase inverter [J5].

3.3 Implementation in other power converters

Except for the above mentioned single-phase and three-phase inverters that are most widely used power converters, the proposed measurement circuits are also applicable to some other power converters, such as dual-active-bridge (DAB) isolated bidirectional DC-DC converters, multilevel converters (MMC), and even one single power semiconductor applications.

3.3.1 DAB-isolated bidirectional DC-DC converters

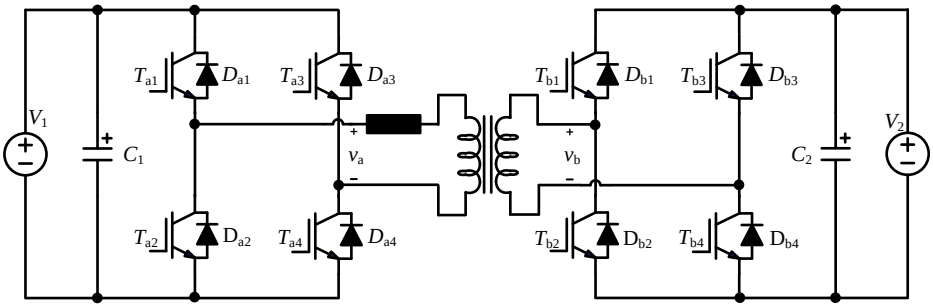


Fig. 49: Topology of DAB.

DAB has been widely applied in many applications, ranging from distributed power systems, energy storages, electric vehicles, and aircrafts [107–110]. Fig.49 shows the topology of a DAB. It contains two full-bridge converters isolated by a transformer. The applicability of proposed measurement circuits depends on the operation modes of DAB that are linked to control strategies. Conventionally, there are four representative control strategies for DAB:

- single-phase-shift (SPS) control: Both full-bridge converters on the two sides of transformer use bipolar modulation, which means both output voltages v_a and v_b contain two-level only without current freewheeling modes. Thus, the proposed method is bot applicable to the DAB with SPS control strategy;
- extended-phase-shift (EPS) control: The output voltage of one full-bridge is two-level while the other one is three-level with current freewheeling modes. When the power flow direction is reversed, the operation modes of the two full-bridges are needed to be exchanged. Therefore, the on-state voltages of the power semiconductors in both sides can be monitored by proposed circuits;
- dual-phase-shift (DPS) control: Both full-bridges keep the same modulation method consistently that makes three-level in both v_a and v_b. Therefore, the proposed circuits are effective to the DABs with DPS control;
- triple-phase-shift (TPS) control: In principle, TPS is similar with DPS except for the different phase-shift-ratio between two full-bridges. Thus, both v_a and v_b contain the on-state voltages that can be extracted by proposed circuits.

In conclusion, except for the DABs with SPS control, the proposed measurement circuits are applicable to the DABs with the rest of three control strategies.

3.3.2 Multilevel converters

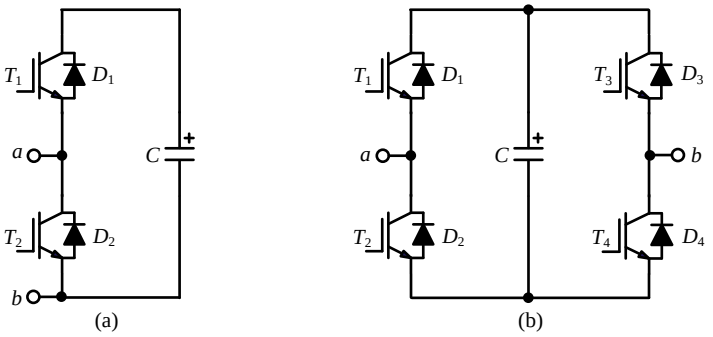


Fig. 50: Submodule of multilevel converter: (a) half-bridge; (b) full-bridge.

Multilevel converters are applied to high-voltage applications [111, 112], and are composed of multiply submodules as shown in Fig.50. For the half-bridge submodule, the proposed circuits can only monitor one power semiconductor (either T_1 and D_1 or T_2 and D_2) with one circuit. While the proposed circuits are able to monitor the all power semiconductors in the full-bridge submodule. Because the voltage v_{ab} contains the on-state voltages when this submodule is in short-circuit modes. For instance, if T_1 and T_3 are in on-state, v_{ab} can be expressed as:

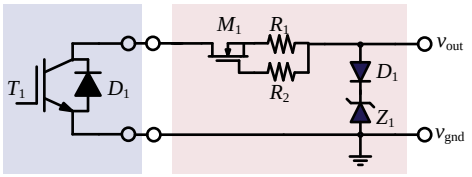
$$v_{ab} = V_{F1} + V_{CE,sat3} \tag{24}$$

where V_{F1} is the forward voltage of D_1, $V_{CE,sat3}$ is the on-state voltage of T_3.

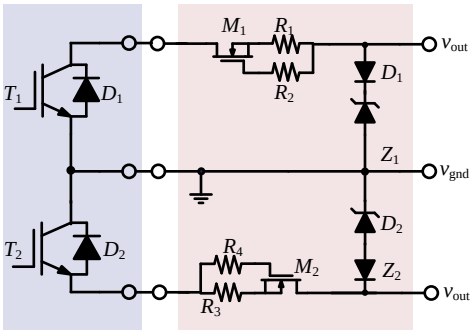
Likewise, the on-state voltages of power semiconductors in the full-bridge submodule are included in v_{ab}.

3.3.3 Single phase-leg and single power semiconductor

The proposed measurement circuit is superior to conventional component-level circuits even in applying to a single power semiconductor or a single phase-leg due to the elimination of power supply as shown in Fig.51. Thus, in principle, the proposed circuits are also applicable to the power converters with only one half-bridge or one power semiconductor.



(a)



(b)

Fig. 51: Application of proposed circuits in: (a)single power semiconductor; (b) single phase-leg.

3.4 Verification of the proposed circuits with power cycling testing

Power cycling testing is a common way to accelerate the degradation progress of power semiconductors. To verify the effectiveness of the proposed circuits, a single-phase power cycling setup is built as shown in Fig.52(a), along with its hardware realization in Fig.52(b). It is set to operate at 400 V/40 A with 1 Hz fundamental frequency and 10 kHz switching frequency. The case of the applied IGBT module is removed and a optic fiber sensor is used to measure it's junction temperature directly.

Fig.53 depicts the operating condition of the developed power cycling setup, including the sinusoidal inductor current and the corresponding swinging junction temperature of T3 from 70 °C to 100 °C. It should be noted that the temperature swings of all chips are not completely same with each other due to the different layout and thermal path, leading to variable lifetimes/power cycles.

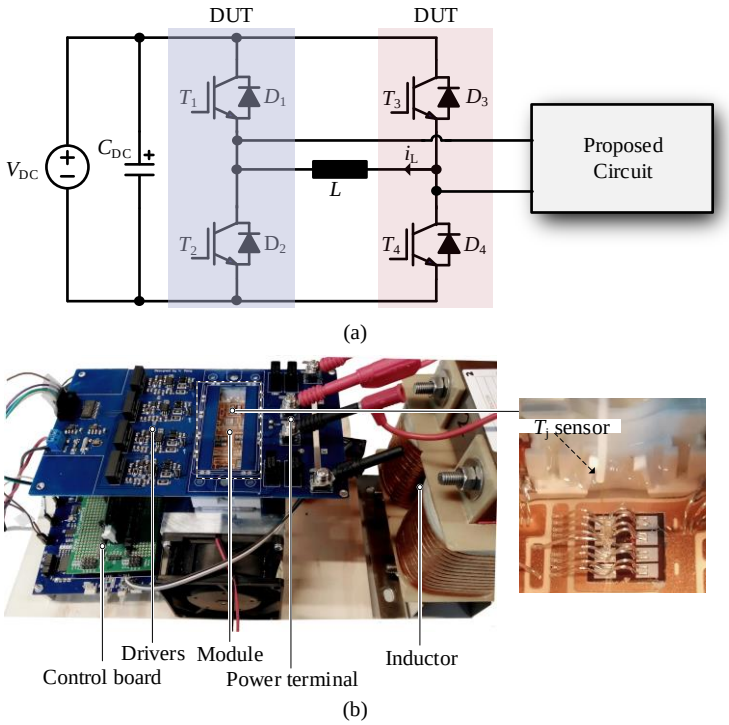


Fig. 52: Single-phase power cycling: (a) topology; (b) hardware.

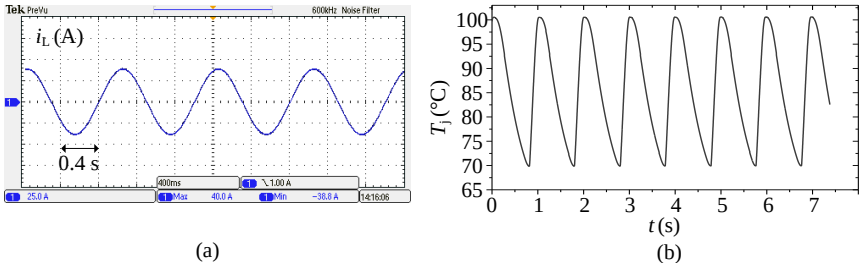


Fig. 53: Operating specification of power cycling setup: (a) inductor current; (b) junction temperature.

In addition, a friendly human-machine interface is designed in Labview as shown in Fig.54, consisting of the configuration area, the data backup area, and the display area of the monitored on-state voltages. The power cycling test lasts for 19 days without interruption until an abrupt change happens. During the power cycling test, only the on-state voltages under the peak inductor current are measured and displayed to indicate the degradation process of the IGBT module. Fig.55 summarizes the monitored results. It can be seen that the fluctuation of the measured on-state voltage is

limited to 10 mV only and the results vary during one day due to the swing of ambient temperature. Among them, $V_{CE,sat2} + V_{F4}$ and $V_{CE,sat3} + V_{F1}$ show the abrupt change due to the wear-out of bond wire at the end of power cycling and are increased by 2% and 1.9%, respectively. While $V_{CE,sat4} + V_{F2}$ and $V_{CE,sat1} + V_{F3}$ have negligible change, which means the corresponding chips are still in health state. To sum up, through the power cycling test, the ability of the proposed circuits in monitoring the degradation process of power semiconductors is verified.

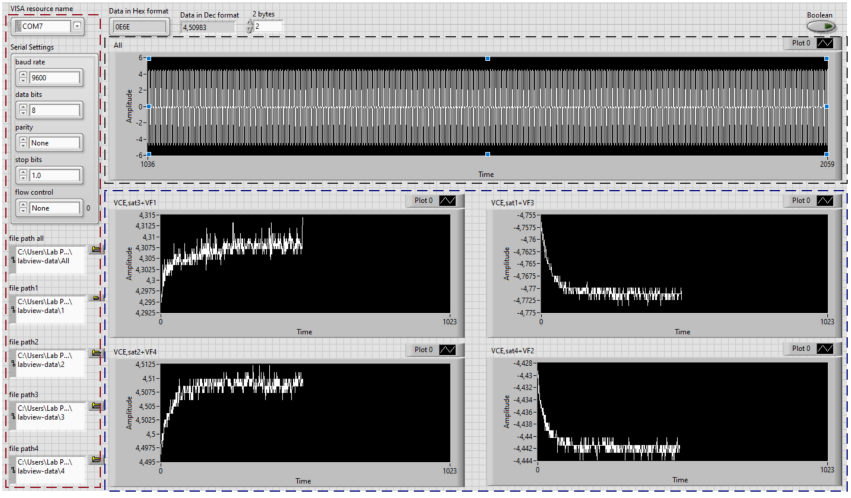


Fig. 54: On-state voltage monitoring interface (red dash rectangle: configuration area; gray dash rectangle: data backup area; blue dash rectangle: monitored on-state voltage with the proposed circuits).

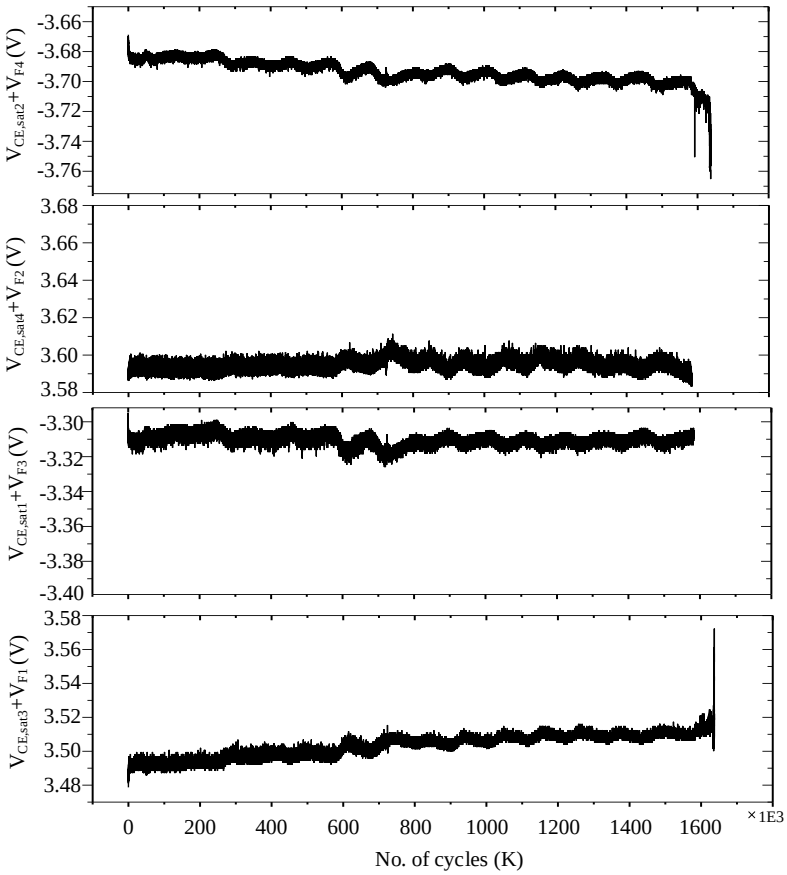


Fig. 55: Monitored on-state voltages over power cycling test ($V_{CE,satx}$ and V_{Fx}) indicate the on-state voltage of T_1 and D_1, respectively.

3.5 Verification of the proposed circuits with junction temperature estimation

The junction temperature T_j estimation with the proposed measurement circuit is verified in the three-phase inverter platform shown in Fig.44. It is noted that, unlike the application in monitoring the degradation of power devices, the measured on-state voltages are the sum or difference between $V_{CE,sat}$ and V_F, which can not be directly used to estimate the T_j of an individual IGBT or Diode since the different devices have different T_j during operation. Therefore, it is necessary to separate them in terms of T_j estimation.

Due to the rich operation modes of the three-phase inverter as shown in Fig.43 and Table 9, these on-state voltages can be separated by using further data process methods, which is not detailed in this thesis.

It is know that $V_{CE,sat}$-based T_j estimation method requires the calibration in ad-

vance. To simplify the experimental process, the case of the IGBT module is removed and an optical-fiber temperature sensor is used to measure the junction temperature of IGBT directly. Meanwhile $V_{CE,sat}$ of device under test is measured at I_C=5 A when this inverter is in operation. Thereafter, two points of T_j and $V_{CE,sat}$ are measured simultaneously as shown in Fig.56, together with their calibrated expression.

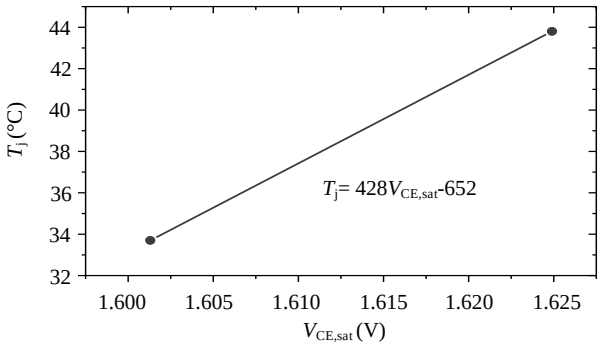


Fig. 56: Calibrated relationship between T_j and $V_{CE,sat}$ at I_C=5.

Fig.57 compares the estimated and measured static junction temperature while the inverter is in operation. Due to the accurate calibration, the measured static T_j with optic-fiber can be accurately estimated by the proposed $V_{CE,sat}$ based method. The proposed method is also verified with dynamic T_j as shown in Fig.58. T_j is changed by turning on and off the forced-air cooling. The error of the estimated T_j is limited to ± 4 °, which proves the feasibility of the proposed measurement circuits in estimating junction temperature through the measured on-state voltage.

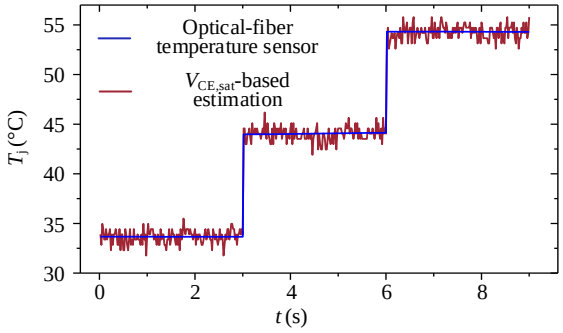


Fig. 57: Comparison between the estimated and measured static junction temperature.

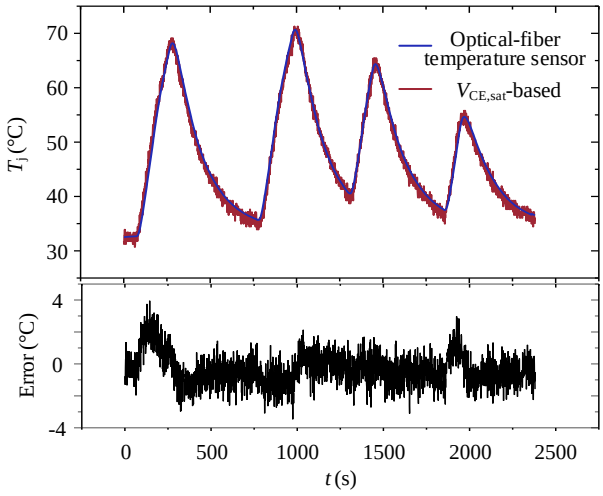


Fig. 58: Comparison between the estimated and measured dynamic junction temperature.

3.6 Summary

The implementation of proposed measurement circuits in different power converters is presented in this chapter. 1) The operation modes of single-phase and three-phase inverter are analyzed firstly. It is found that except for the single-phase inverter with bipolar SPWM modulation, the voltage across the middle-point of phase-legs of any other inverters contains the on-state voltage information of all power semiconductors;

2) To verify the effectiveness and feasibility of proposed measurement circuits, two experimental platforms are established (single-phase and three-phase inverters). Then, the prototypes of proposed circuits are applied to these two platforms, respectively and the on-state voltage information of all power semiconductors is extracted from functioning inverters;

3) The implementations of proposed measurement circuits in DAB DC-DC converters, the submodule of multilevel converters, half-bridge, and even a single power semiconductor are discussed;

4) A power cycling platform is established to accelerate the aging progress of power semiconductors. Based on this, the ability of degradation monitoring of proposed measurement circuits is proved. In addition, the junction temperature estimation of individual power semiconductor by proposed circuits is verified.

Part III. Digital Twin Based System-level Condition Monitoring for Power Converters

In this part, Digital twin is introduced and implemented in power electronics converters for condition monitoring purpose. The basic concept of digital twin is introduced firstly. Then, the digital twin of buck converter is established to achieve the condition monitoring of the degradation process of the key components in converter. Finally, The experimental testing for the proof-of-concept of proposed method is carried out. There are two chapters in this part: **Chapter 4**. Implementation of digital twin based condition monitoring in DC-DC converters, and **Chapter 5**. Feasibility study on the digital twin for DC-AC converters.

4 Implementation of digital twin based condition monitoring in DC-DC converters

This chapter studies the implementation of the digital twin concept in estimating the health indicators of DC-DC power converters firstly. Then, by leveraging the cluster-data based method, the estimated health indicators in different situations are packaged together as a cluster to indicate the degradation level of power converter. As such, the complicated and unpractical calibration between the health indicators and multiple impactors is not required. The demonstration of the proposed method is conducted experimentally with a Buck converter case study.

4.1 Digital twin concept

Digital twin is the digital copy of a physical system, and they nearly share the same operating characteristics. It provides the customers with the ability to optimize its installed products [113]. Besides, it is possible to use a digital twin to realize condition monitoring.

It is worth mentioning that the digital twin could be much more than the traditional circuit simulation software and provides a mirrored linkage between the digital and physical worlds. This interactivity makes the digital twin adaptive itself by analyzing the data coming from the real world.

Numerous degradation monitoring methods have been proposed for power switches and capacitors so far, as discussed in Chapter 1. Nevertheless, most of them are hardware-based measurement circuit, which may not be the best solution for those installed power converters from the view of practical applications. Therefore, some methods are proposed without additional hardware, like the detection of harmonic, efficiency, and neural-network. Nevertheless, those methods are still in initial stage with some practical issues, such as insufficient data for model training and incapability in distinguishing the degradation of both power devices and capacitors. However, the digital twin based condition monitoring method distinguishes itself by taking existing data to identify the health indicator of individual devices, instead of using additional hardware or requiring tremendous data for off-line model training as the above-mentioned methods do.

The digital twin has been widely used in the area of prognostics and health management (PHM) by many companies and institutes to improve the reliability and lifetime of their products, such as the Space Vehicle (NASA) [114], Aircraft [115], Oil/Gas Facilities (British Petroleum) [116], Windfarm (GE) [117], E-Mobility (TESLA) [118], and Power System (Siemens) [119]. However, they are rarely applied in the power electronics to date, with at least three papers published in this regard. [120] and [121] build the digital-twin of a photovoltaic (PV) system (e.g., the solar panels and the power inverters) and power converters (e.g., the DC-DC and AC-DC converters), respectively. They focus on the prompt fault diagnosis of power converters only. Because they build those digital-twins without considering the parasitic parameters of the power converter and assuming that the internal parameters (e.g., inductance, capacitance, and resistance) of the power converter are already known. [122] reports the electro-thermal digital-twin of the power modules applied to the off-shore wind

turbines, including the thermal model and power losses model. It is then used to predict the junction temperature of the power module, so as to estimate the remaining useful lifetime (RUL). Similarly, it also assumes that the parameters of the digital twin are already known. Nevertheless, these parameters depend on the degradation-level of power converter, the environmental and operational conditions, and the tolerance among a population of components. Hence, the exact determination of these parameters cannot rely on the datasheet or off-line measurement. The application of the digital twin concept in power electronics for PHM is still limited that and thesis will make the efforts to.

4.2 Digital twin of Buck converter case study: operation principle

To demonstrate the proposed method, the digital twin of a Buck converter is developed firstly. After that, the particle swarm optimization (PSO) algorithm is introduced to update the insight of digital Buck converter according to the data coming from both physical Buck converter and its digital counterpart, until the difference between them is less than a pre-set criteria. Then, the digital twin is expected to have the same operational behaviors with the physical buck converter.

4.2.1 Modeling of Buck converter

Fig.59 presents the equivalent circuit of Buck converter. R_{dson} is the on-state resistance of MOSFET; R_{L} and R_{c} represent the equivalent resistance of inductor L and capacitor C, respectively; R is load; V_{f} represents the forward voltage of diode; v_{in} is the input voltage.

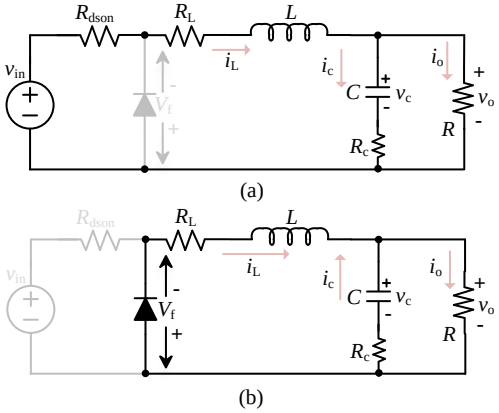


Fig. 59: Equivalent circuit of Buck converter [J1]: (a) MOSFET is in on-state; (b) MOSFET is in off-state.

Based on the basic electrical circuit theory, inductor and capacitor characteristic,

Fig.59 can be expressed as:

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \\ v_o \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}\left(DR_{dson} + R_L + \frac{R_c R}{R_c + R}\right) & -\frac{1}{L}\left(\frac{R}{R_c + R}\right) \\ \frac{1}{C}\left(\frac{R}{R_c + R}\right) & -\frac{1}{C}\left(\frac{1}{R_c + R}\right) \\ \frac{R_c R}{R_c + R} & \frac{R}{R_c + R} \end{bmatrix} \times \begin{bmatrix} i_L \\ v_c \end{bmatrix} + D\begin{bmatrix} \frac{1}{L}v_{in} \\ 0 \\ 0 \end{bmatrix} + (1-D)\begin{bmatrix} -\frac{1}{L}V_f \\ 0 \\ 0 \end{bmatrix} \tag{25}$$

where D represents the on-off state of MOSFET: D is 1 when the MOSFET is in on-state while it is 0 when the MOSFET is in off-state.

The measurable signals in Buck converter are the inductor current i_L and output voltage v_o, which are usually used for control purposes. Therefore, the i_L and v_o from the digital twin should be obtained firstly. To solve this, (25), a differential equation, is linearized by using a 4th-order Runge-Kutta method [123]. It is an effective method to solve differential equations and considered as sufficient in this case study with a negligible error.

To easy the process of derivation, (25) is simplified as:

$$\begin{cases} f_1(i_L, v_c) = \frac{di_L}{dt} \\ f_2(i_L, v_c) = \frac{dv_c}{dt} \end{cases} \tag{26}$$

Then, (26) can be linearized as:

$$\begin{cases} i_{L,n+1} = i_{L,n} + \frac{h}{6}\left(k_{a1} + 2k_{a2} + 2k_{a3} + k_{a4}\right) \\ v_{c,n+1} = v_{c,n} + \frac{h}{6}\left(k_{b1} + 2k_{b2} + 2k_{b3} + k_{b4}\right) \end{cases} \tag{27}$$

where the present time interval is defined as n^{th}, and the next step is represented by $(n+1)^{th}$. k_{a1}-k_{a4} and k_{b1}-k_{b4} defined to obtain the average change rate of n^{th} and

$(n+1)^{th}$ step as shown below:

$$\begin{cases} k_{a1} = f_1\left(x_n, y_n\right) \\ k_{b1} = f_2\left(x_n, y_n\right) \\ k_{a2} = f_1\left(x_n + \frac{h}{2}k_{a1}, y_n + \frac{h}{2}k_{b1}\right) \\ k_{b2} = f_2\left(x_n + \frac{h}{2}k_{a1}, y_n + \frac{h}{2}k_{b1}\right) \\ k_{a3} = f_1\left(x_n + \frac{h}{2}k_{a2}, y_n + \frac{h}{2}k_{b2}\right) \\ k_{b3} = f_2\left(x_n + \frac{h}{2}k_{a2}, y_n + \frac{h}{2}k_{b2}\right) \\ k_{a4} = f_1\left(x_n + hk_{a3}, y_n + hk_{b3}\right) \\ k_{b4} = f_2\left(x_n + hk_{a3}, y_n + hk_{b3}\right) \end{cases} \tag{28}$$

where h is the calculation step time between n^{th} and $(n+1)^{th}$ time step.

The output voltage v_o at $(n+1)^{th}$ time step is derived from (25) as below:

$$v_{o,n+1} = i_{L,n+1}\frac{R_c R}{R_c + R} + v_{c,n+1}\frac{R}{R_c + R} \tag{29}$$

It can be seen that $v_{o,n+1}$ is obtained through $i_{L,n+1}$ and $v_{c,n+1}$. Combining with (26)-(28), (29) can be extended as:

$$v_{o,n+1} = ai_{L,n} + bv_{c,n} + c \tag{30}$$

where the coefficients a, b, and c are composed of by eight parameters (L, C, R_L, R_C, R_{dson}, D, , v_{in}, and V_f). Among them, L, C, R_L, R_C, and R_{dson} are unknown parameters and need to be estimated. v_{in} is physically measured. V_f is measured in advanced and is 1 V in this thesis. Thereafter, the inductor current and capacitor voltage at n^{th} step can be used to calculate the output voltage at $(n+1)^{th}$ step. Then, the on/off of MOSFET D at next step is determined by using the calculated v_o through the following steps.

4.2.2 Modeling of sampling circuit

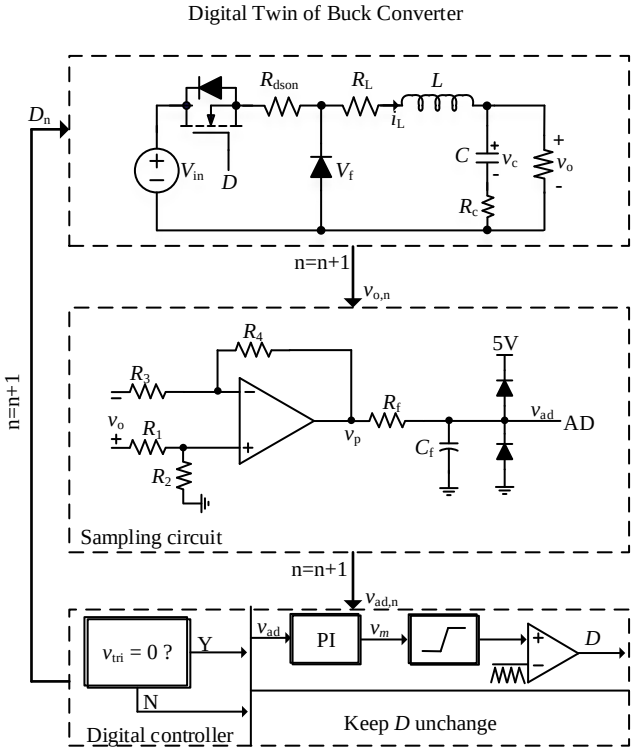


Fig. 60: Developed digital twin of buck converter.

In the physical world, the output voltage is sampled to achieve closed-loop control. Thus, the sampling circuit is modeled as well and is presented in Fig.60, which includes a differential circuit and a R_fC_f low-pass filter. Based on this, v_p can be expressed as:

$$v_{p,n+1} = \frac{(R_3 + R_4)R_2}{(R_1 + R_4)R_5} v_{o,n+1} \tag{31}$$

Thereafter, the sampled voltage v_{ad} is:

$$\begin{cases} v_{ad,n+1} = v_{p,n+1} - R_f C_f \dfrac{dv_{ad,n+1}}{dt} \\ f_3(v_{ad,n+1}) = \dfrac{dv_{ad,n+1}}{dt} = \dfrac{v_{p,n+1} - v_{ad,n+1}}{R_f C_f} \end{cases} \tag{32}$$

with 4th-order Rung-Kutta method again, (32) can be linearized:

$$\begin{cases} v_{\mathrm{ad,n+1}} = v_{\mathrm{ad,n}} + \dfrac{h}{6}\left(k_1 + 2k_2 + 2k_3 + k_4\right) \\ k_1 = f_3\left(y_{\mathrm{n}}\right) \\ k_2 = f_3\left(y_{\mathrm{n}} + \dfrac{h}{2}k_1\right) \\ k_3 = f_3\left(y_{\mathrm{n}} + \dfrac{h}{2}k_2\right) \\ k_4 = f_3\left(y_{\mathrm{n}} + hk_3\right) \end{cases} \tag{33}$$

4.2.3 Modeling of close-loop controller

The close-loop control program of physical Buck converter is replicated directly as it is digital information already.

$$\begin{cases} v_{\mathrm{e,n}} = v_{\mathrm{e,n+1}} \\ v_{\mathrm{m,n}} = v_{\mathrm{m,n+1}} \\ v_{\mathrm{e,n+1}} = V_{\mathrm{ref}} - v_{\mathrm{ad,n+1}} \\ v_{\mathrm{m,n+1}} = v_{\mathrm{m,n}} + K_{\mathrm{p}}(v_{\mathrm{e,n+1}} - v_{\mathrm{e,n}}) + K_I h v_{\mathrm{e,n+1}} \end{cases} \tag{34}$$

where V_{ref} is the reference voltage of v_{o}; v_{e} is the error between v_{o} and V_{ref}; v_{m} is the modulation signal; K_{P} and K_{I} are the internal parameters of proportional-integral (PI) controller.

Then, by comparing v_{m} with a triangular carrier signal v_{tri}, D can be described as:

$$D_{\mathrm{n+1}} = \begin{cases} 1(v_{\mathrm{m,n+1}} \geq v_{\mathrm{tri,n+1}}) \\ 0(v_{\mathrm{m,n+1}} < v_{\mathrm{tri,n+1}}) \end{cases} \tag{35}$$

the frequency of v_{tri} is same with the switching frequency.

The entire digital twin of Buck converter is presented in Fig.60, which is able to operate itself if those internal parameters are known.

4.2.4 Principle of Particle swarm optimization (PSO)

The developed digital twin of Buck converter is still a stand-alone system with unknown internal parameters (e.g., L, C, R_{c}, R_{L}, and R_{dson}). To make it have similar characteristics with the physical converter, PSO algorithm is used as a connecting tool.

PSO is an effective iterative optimization algorithm that can update those unknown parameters and find their best values by comparing the data from digital and physical Buck converters [124]

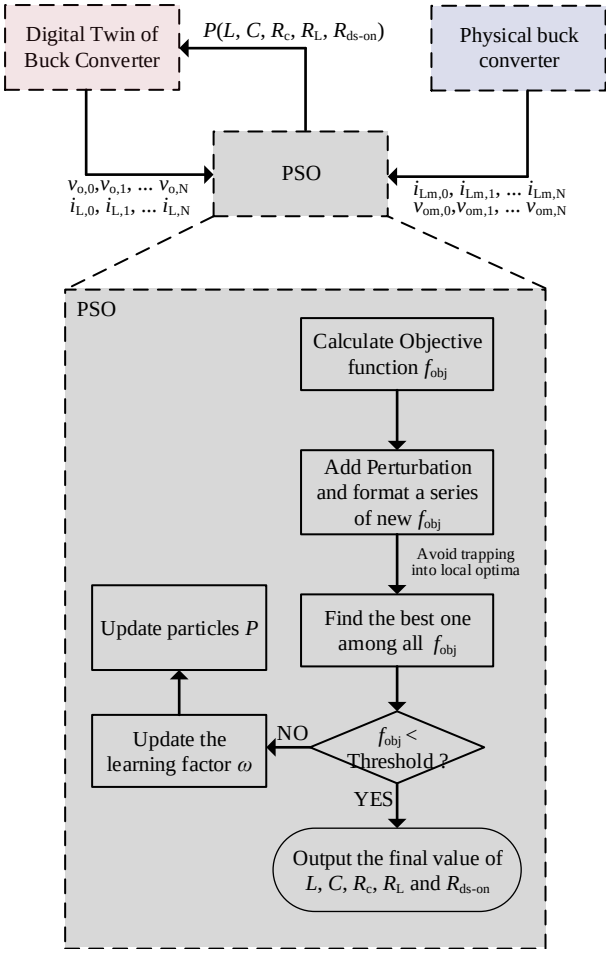


Fig. 61: Application of digital twin with PSO.

For PSO, a proper objective function (or cost function) needs to be constructed firstly, which represents the difference between digital and physical Buck converter as shown below:

$$f_{\text{obj}} = \frac{\sum_{i=1}^{N} \left[(i_{\text{L}} - i_{\text{Lm}})^2 + (v_{\text{o}} - v_{\text{om}})^2 \right]}{N} \tag{36}$$

where i_{L} and v_{o} represent the data calculated by digital twin; i_{Lm} and v_{om} are experimentally measured from the physical Buck converter; N is the size of the measured data. PSO aims to minimize (36) as much as possible.

At the beginning, the parameter group P (L, C, R_{c}, R_{L}, and R_{dson}) is initialized with 25 particles in this case study, which means each of those five parameters has 25 particles. Then, v_{o} and i_{L} are calculated by digital twin for 25 sections, respectively (the number of data contained in each data section is N). Correspondingly, v_{om} and i_{Lm} are measured for one section each from the physical world. After that, the objec-

tive function is obtained by (36). Also, to avoid trapping into local optima, a series of new f_{obj} is formated randomly. After that, if the best f_{obj} so far is smaller than a preset threshold, the parameter set P is supposed to same with the corresponding parameters in physical Buck converter at this moment. Otherwise, each particle of the parameter set P is updated by:

$$\begin{cases} V_{\text{i,j}} = \omega_{i-1} V_{\text{i}-1,j} + 2r_{1,\text{i}-1,\text{j}} \left(P_{\text{G}} - P_{\text{i}-1,\text{j}} \right) + 2r_{2,\text{i}-1,\text{j}} \left(P_{\text{L,i}-1,\text{j}} - P_{\text{i}-1,\text{j}} \right) \\ P_{\text{i,j}} = P_{\text{i}-1,\text{j}} + V_{\text{i,j}} \end{cases} \tag{37}$$

where ω is the learning factor to control the step amplitude through the iteration process [125]; i denotes the iteration number; j is the particle number; $V_{\text{i,j}}$ represents the moving velocity of j^{th} particle at i^{th} iteration; $P_{i,j}$ represents the position of j^{th} particle in i^{th} iteration; $P_{\text{L,i}-1,\text{j}}$ represents the best position of j^{th} particle until $(i-1)^{th}$ iteration; P_{G} is the global optimization so far; r_1 and r_2 are weighting factors and they are set to 2 in this case study.

Thereafter, the iteration loop starts again with the new updated parameters.

4.3 Digital twin of the Buck converter case study: experimental testing for health indicators identification

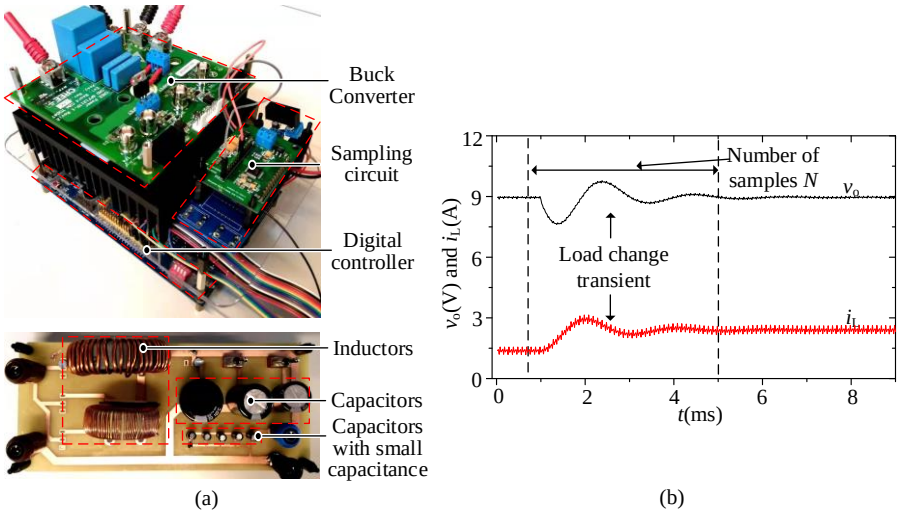


Fig. 62: (a) Platform of buck converter; (b) Measured inductor current and output voltage during load change transient [J1].

Fig.62(a) presents the Buck converter demonstrator. An *LC* module is designed to emulate the degradation of capacitor. The operational specifications of the Buck converter are listed in Table 10. As shown in Fig.62(b), this study takes advantage of the load change evens, which exists in many practical applications. Then, part of the data over the load change transient is used in this case study.

Table 10: Specification of Buck Converter

Parameter	Value	Parameter	Value
V_{in}/V_{ref}	24 V/9 V	f_{sw}	20 kHz
Load 1	4.9 Ω	Load 2	3.3 Ω
L (μH)	782	C (μF)	151
Sampling frequency	50 kHz		

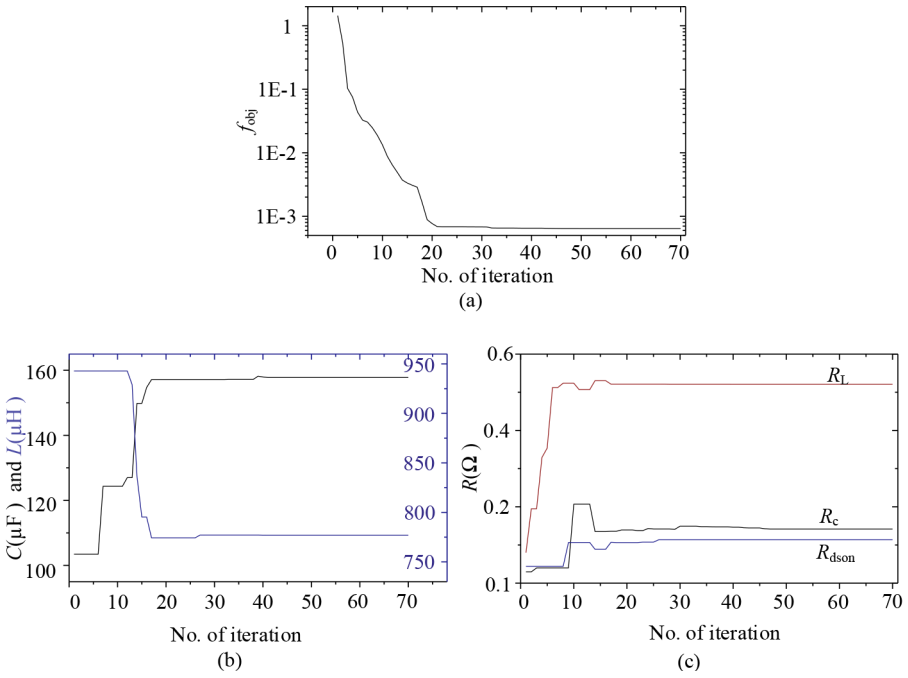


Fig. 63: Process of parameter identification [J1]: (a) objective function; (b) capacitance and inductance; (c) parasitic resistances R_L, R_c and R_{dson}.

With the method illustrated in Fig.61, the best solutions of unknown parameters can be derived as shown in Fig.63. f_{obj} descends to a negligible value after 50 iterations. Meanwhile, the values of those five parameters converge to their best solutions, respectively.

With the best solutions of those parameters, Fig.64 compares the operational waveforms (inductor currents and output voltages) during load change transient from the digital and physical world. It shows that the waveforms from the digital twin and experimental measurement are virtually overlapped, which indirectly proves the feasibility of the proposed digital twin.

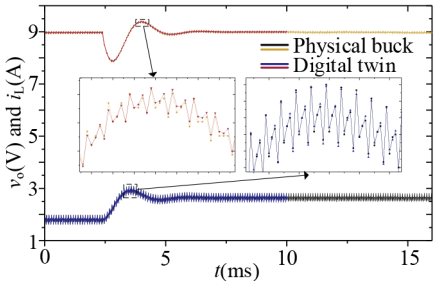


Fig. 64: Comparisons of operational waveforms from digital and physical Buck converter [J1].

4.3.1 Impact of estimation errors

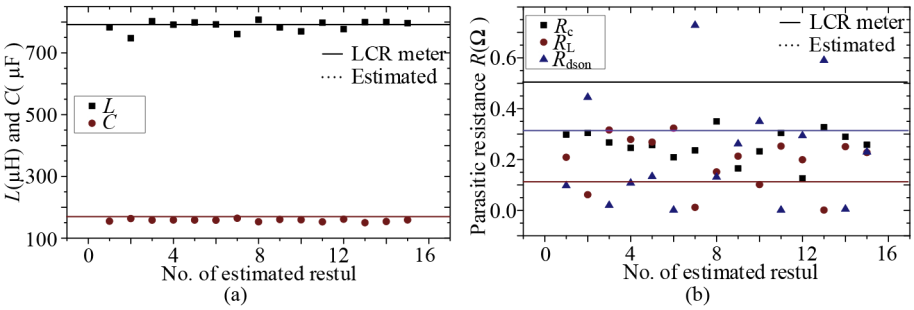


Fig. 65: Comparison of the estimated results (V_{in}/V_o is 24/9 V and load change is from 4.85 to 3.32 Ω) and the measured results by LCR meter (with the measured load change data, the estimation process is repeated for 15 times to show the fluctuation of estimated results) [J1]: (a) inductance and capacitance (b) parasitic resistances.

The consistency of the proposed method is investigated by repeating the process illustrated in Fig.61 for 15 times with the same sector of experimental data. The estimated results are compared with the parameters obtained through off-line measurement (e.g., L, C, R_L, and R_C are measured by LCR meter, R_{dson} is measured experimentally) as presented in Fig.65. The estimated L and C have smaller fluctuation and error. While the estimated parasitic resistances have relatively large fluctuations. Especially for R_L and R_{dson}, they present unacceptable fluctuations. The main reason for this phenomenon is that R_L and R_{dson} are connected in series and will be discussed later. Overall, the estimation error is existed with the proposed method, which is mainly due to the inconsistency of the developed digital twin and the physical converter, such as the unconsidered parasitic parameters of connecting wires, terminals, and loads. Moreover, the measurement accuracy can also affect the estimated results.

4.3.2 Impact of environmental and operational conditions

In field applications, the health indicators alter with environmental and operational conditions as well, besides the degradation level of power converter. Consequently, six operational conditions are chosen to verify the proposed method, as listed in Table 11. Among them, the device under test (DUT) may have different temperatures due to the variable power losses. i_{L} and v_{o} are measured for one time in each condition, but are used to estimate parameters by the proposed method for 15 times. Fig.66 shows the estimated results. It can be seen that L and C change in different conditions, which is mainly attributed to the different temperatures, voltages, and currents. While the estimated results of parasitic resistances are independent of operation conditions. The fluctuations caused by estimation errors are already in a large range, it covers the fluctuations caused by various operation conditions.

Table 11: Different Operation Conditions

Cases	$V_{\mathrm{in}}/V_{\mathrm{o}}$ (V)	$R_{\mathrm{load1}}/R_{\mathrm{load2}}$ (Ω)
Case1 (I)	24/9	4.85/3.32
Case2 (II)	24/9	10.43/4.85
Case3 (III)	48/24	4.85/3.32
Case4 (IV)	48/24	10.43/4.85
Case5 (V)	110/24	4.85/3.32
Case6 (VI)	110/24	10.43/4.85

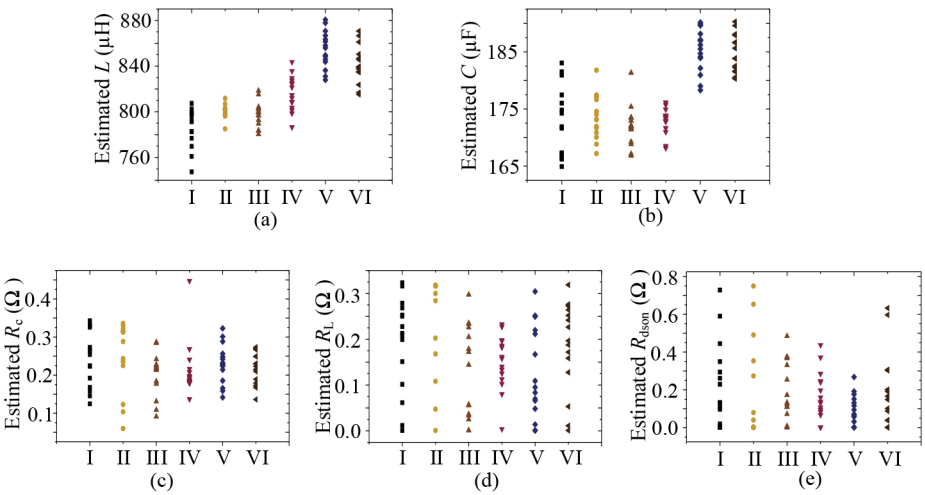


Fig. 66: Estimated results in different operation conditions: (a) L; (b) C; (c) R_{c}; (d) R_{L}; and (e) R_{dson} (I-VI indicate the six operation conditions as listed in Table 11).

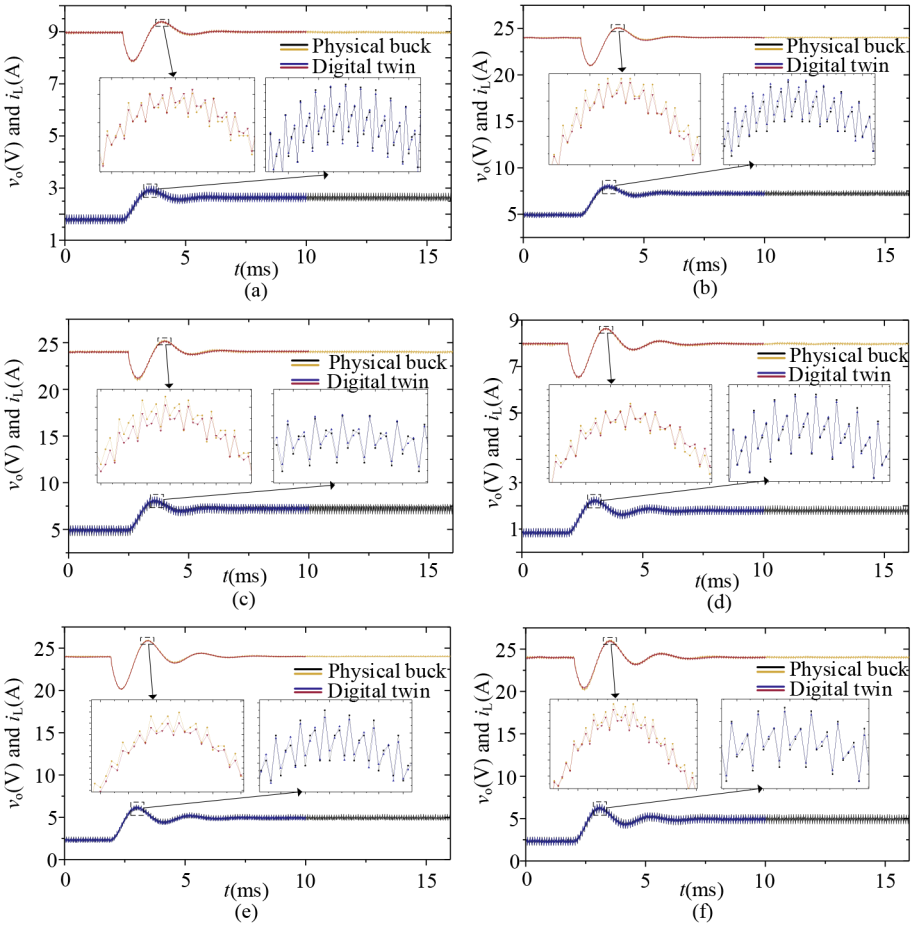


Fig. 67: Comparisons of operational waveforms between digital and physical Buck converter under different operation conditions as listed in Table 11 [J1]: (a) Case1 (I); (b) Case3 (III); (c) Case5 (V); (d) Case2 (II); (e) Case4 (IV); and (f) Case6 (VI).

With the estimated parameters in different conditions, the developed digital twin can output i_{L} and v_{o} as shown in Fig.67. Meanwhile, the corresponding i_{L} and v_{o} measured from the physical world are presented as well. It can be seen that the proposed digital twin virtually share similar operational characteristics with the physical converter in different operation conditions, which verifies the robustness of the proposed method.

4.4 Digital twin of buck converter case study: Experimental testing for degradation monitoring

To verify the ability of monitoring the degradation progress of power converters in variable operation conditions, the proposed method is tested when the degradation

of the critical components in converter happens, including the power semiconductors and capacitors.

4.4.1 Degradation monitoring of capacitor

Table 12: Simulated Degradation of Capacitance During Test.

Caps	C1	C2	C3	C4	C5
Δ C	0%	-2.2%	-4.4%	-6.6%	-8.8%

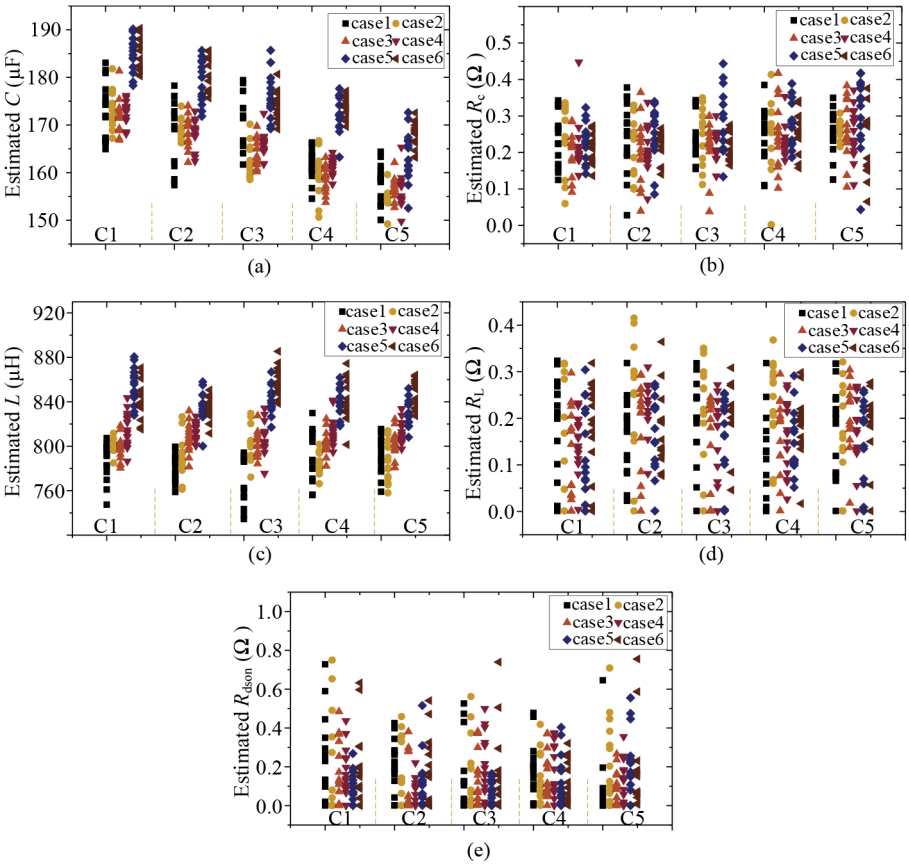


Fig. 68: Estimated C, R_c, L, R_L and R_{dson} when C is decreased (case 1-6 are listed in Table 11, C1-C5 are listed in Table 12) [J1]: (a) C; (b) R_c; (c) L; (d) R_L; (e) R_{dson}.

The end-to-life criteria of capacitor is usually defined as the drop of capacitance by 5% to 20% based on different cases [26], which is simulated by intentionally changing the capacitance: the main capacitor (151 μF) is connected in parallel with extra four

capacitors whose capacitance is 3.6 μF as shown in Fig.62(a). It is a common method to realize the "degradation" of capacitor [86–88]. During the test, the degradation is simulated by removing these extra four capacitors one by one. Meanwhile, the inductor current and capacitor voltage are recorded for one time in each operation condition.

The estimated C and R_c are displayed in Fig.68(a) and (b), respectively. Although the large part of the estimated C and R_c during adjacent situations, such as C1 and C2, are overlapped with each other, the cluster-based C decreases consistently against the simulated degradation of the capacitor. Oppositely, the cluster-based R_c increases slowly while the capacitor is degraded, which proves the proposed method can distinguish the degradation level of capacitor. Besides, the estimated L, R_{L} and R_{dson} keep unchanged while removing extra four capacitors, which agrees with the theoretical analysis.

4.4.2 Degradation monitoring of MOSFET

It is known that MOSFET is the operation-critical components in power converters and its health condition can be effectively indicated by its on-state resistance R_{dson}. Nevertheless, the estimated R_{dson} by the proposed method, as discussed before, shows dramatic fluctuation as well as R_{L}. It is due to the series connection of R_{dson} and R_{L} as shown in Fig.59. Therefore, it is difficult to distinguish them from the proposed method. Alternatively, R_{dson} and R_{L} are represented by a newly defined equivalent resistance in this thesis. By referring to Fig.59, it is known that both R_{dson} and R_{L} work when MOSFET is in on-state. Otherwise, only R_{L} works. Based on this, a new resistance is defined as:

$$R_{\mathrm{Eq}} = R_{\mathrm{L}} + D_{\mathrm{duty}} R_{\mathrm{dson}} \tag{38}$$

where D_{duty} is th ratio of output/input voltage, which can be obtained experimentally. Considering the stable characteristics of inductor, it is reasonable to assume that inductor has a much longer lifetime than MOSFET and capacitor. Thus, R_{L} is assumed to be constant. Consequently, it is possible to indicate the health condition of MOSFET with the newly defined R_{Eq}.

Experimental testing is carried out to verify R_{Eq} as shown in Fig.69. Each of R_{dson} and R_{L} is calculated for 15 times with the proposed method. Then, they are used to calculate the new defined R_{Eq}. It can be seen that the results of R_{Eq} show much higher consistency than that of R_{dson} and R_{L}, which enables the condition monitoring of MOSFET with the proposed method.

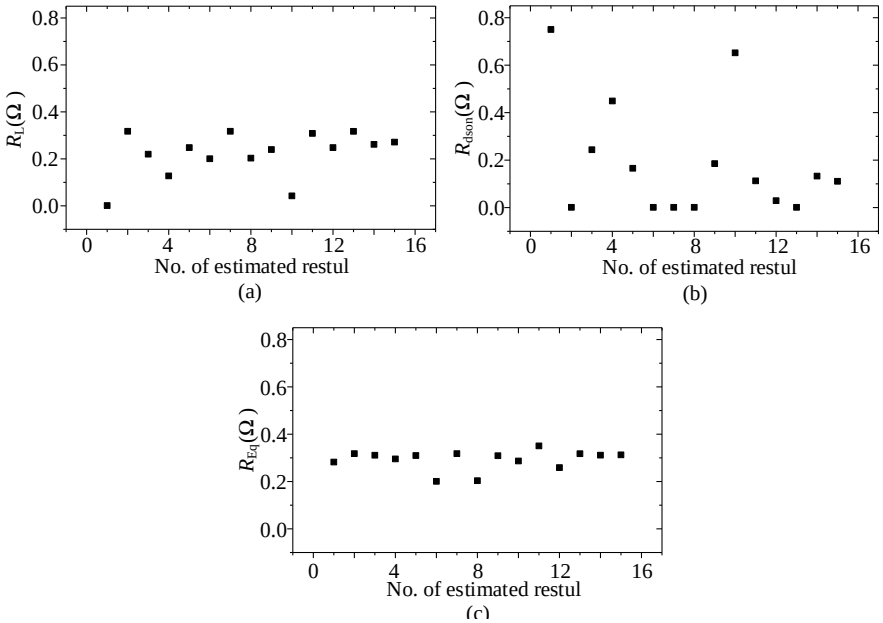


Fig. 69: Estimated R_L, R_{dson}, and R_{Eq} for 15 times [J1].

It is reported in a power cycling study that R_{dson} is increased by 0.3 Ω -1 Ω before the MOSFET used in [126] fails, which is due to the mixture effect of two failure mechanisms of power devices: (1) the package related degradation usually leads to the increase of R_{dson} by 5%-20% as the end-of-life criteria [8, 31]; and (2) the chip-related degradation can cause much higher increment of R_{dson} as the degradation of gate oxide layer can decrease driving voltage. Then, the R_{dson} is increased accordingly due to the MOSFET operating in saturation region [126]. To emulate the degradation process of MOSFET, five MOSFETs with different R_{dson} are selected in this case study as shown in Table 13. After that, they are tested in the developed Buck converter with six operation conditions, as listed in Table 11. Meanwhile, inductor current and output voltage are measured for one time in each case. During testing, the case temperature T_c of each MOSFET is different at each case due to different R_{dson} and operating conditions. T_c is recorded while testing as shown in Table 14, showing higher temperature with higher current (e.g., case 3) and higher R_{dson}. The increasing T_c corresponds to the situations in real application as the degraded MOSFET has higher on-state resistance and power losses, and can cause increasing T_c.

Table 13: On-state Resistance of The selected MOSFETs.

MOSFETs	M1	M2	M3	M4	M5
R_{dson} (Ω)	0.11	0.241	0.385	0.495	0.75

Table 14: Measured Case Temperature when The MOSFETs is in Different Operation Conditions (Unit: °C)

Cases	T_{c-M1}	T_{c-M2}	T_{c-M3}	T_{c-M4}	T_{c-M5}
Case1	27.5	27.8	28	28.8	28.3
Case2	25.7	26.8	26.5	27.1	26.5
Case3	29	39.4	40.9	44	55
Case4	26.5	29.1	29.3	32.8	34.8
Case5	28.4	32.4	36.7	37.3	39.5
Case6	26.1	27.5	28.4	29.7	30.8

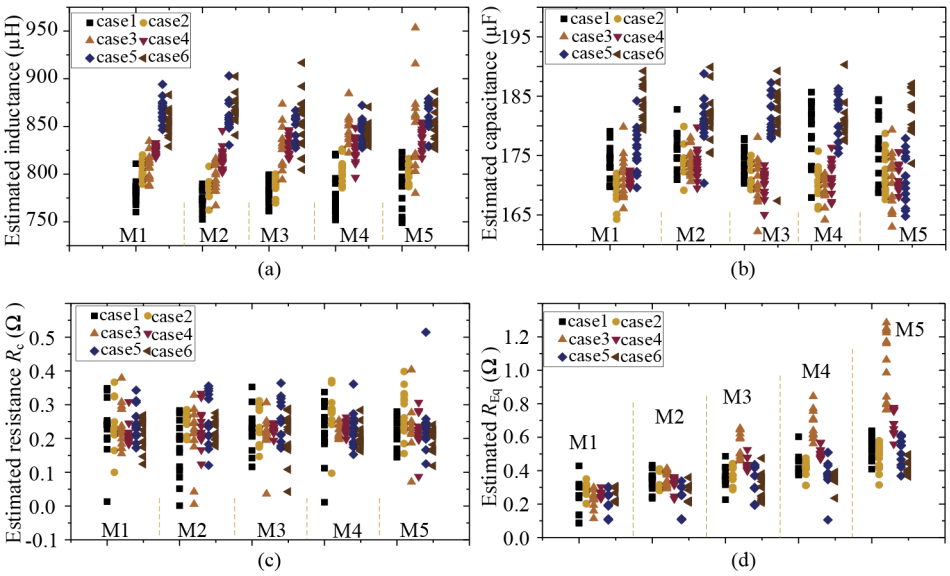


Fig. 70: Estimated parameters under different operation conditions and MOSFETs with different degradation levels [J1]: (a) L; (b) C; (c) R_c; (d) R_{Eq}.

Fig.70 shows the estimated results at different MOSFET degradation levels and operating conditions are presented in a cluster-based data, instead of one data. It indicates that the R_{Eq} increases with the degradation level of MOSFET. Especially the results with the condition in case3 increase dramatically due to the highest case temperature. Comparatively, the results of L, C, and R_c are independent on the degradation of MOSFET.

4.4.3 Simultaneous degradation monitoring of MOSFET and capacitor

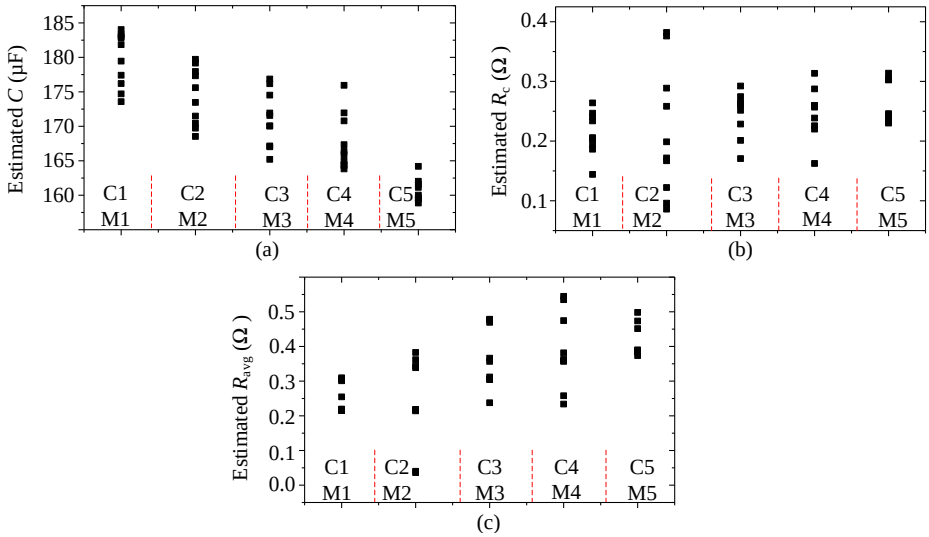


Fig. 71: Estimated parameters during the simultaneous degradation of capacitor and MOSFET under the operation condition case6 (M1-M5 are listed in Table 13, C1-C5 are listed in Table 12) [J1]: (a) C; (b) R_c; (c) R_{Eq}.

In practical applications, the degradation of power switches and capacitors may coincide. Therefore, the capacitor and MOSFET in the physical Buck converter are degraded simultaneously with five levels. Then, the proposed method is conducted and the results are shown in Fig.71. The estimated capacitance and R_c present opposite change trend with the degradation levels. Meanwhile, the R_{Eq} shows an increasing trend. It proves that the proposed method can indicates and distinguishes the simultaneous degradation of capacitor and MOSEFET in a Buck converter.

4.4.4 Data analysis

To avoid the cumbersome calibration process, a data cluster-based method is proposed in this thesis, which packages the obtained data together and gives the qualitative analysis. However, for a practical application, the quantitative analysis is needed. To unify the evaluation, the boxplot technique in MATLAB is applied to analyze the data distribution from the statistic view and quantify the degradation levels. It is an effective tool to statistically analyze the distribution of a group of data and gives the median that represents the feature of this group with higher confidence. The boxplot of the clusters in Fig.68(a), Fig.68(b), and Fig.70(d) are obtained and shown in Fig.72, respectively.

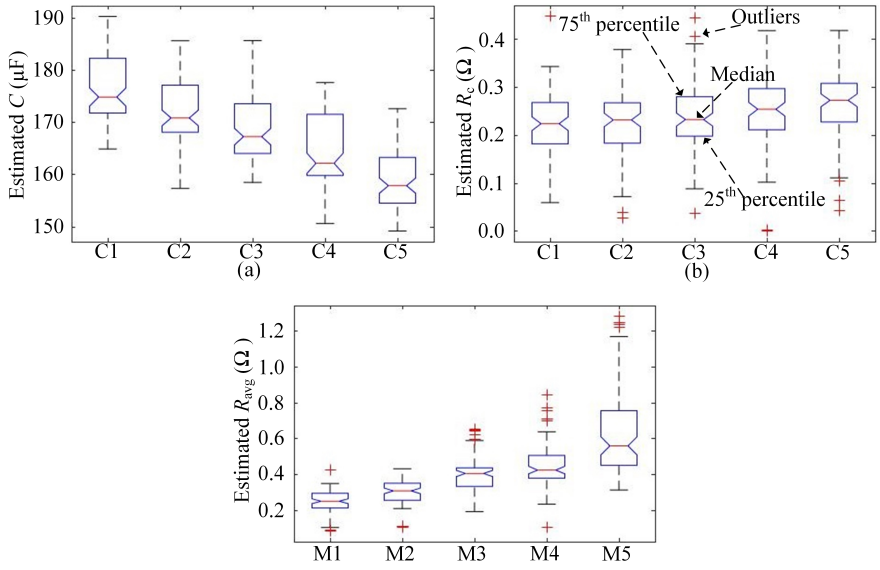


Fig. 72: Probability density distribution of the estimated health indicators [J1]: (a) C; (b) R_c; (c) R_{Eq}.

The median represents the value with highest appearance possibility within the cluster. It can indicate the degradation trend of capacitor and MOSFET effectively. Those outliers out of 95% confidence interval can be seen as bad data. Table 15 lists the median value of each cluster, indicating that the medians of estimated C and R_c are reduced by 9.7% and improved by 21%, respectively in response to the 8.8% decrease due to the simulated degradation. Similarly, the median of estimated R_{avg} is improved from 0.243 Ω to 0.561 Ω while R_{dson} is changed from 0.11 Ω to 0.75 Ω.

Table 15: Obtained Median Value After Data Process

Median (Cap)	C1	C2	C3	C4	C5
C (μF)	174.9	170.9	167.3	162.2	158
R_c (mΩ)	224	232	233	254	273
Median (MOS)	M1	M2	M3	M4	M5
R_{avg} (mΩ)	252	310	407	426	561

4.5 Summary

A digital-twin based condition monitoring method is proposed in this Chapter. It does not require additional measurement circuits. With a Buck converter case study, it is verified theoretically and experimentally. Firstly, the digital twin of Buck converter is established in MATLAB by referring to its physical counterpart. Then, the data coming from both digital and physical converter are processed to estimate the unknown health indicators of Buck converter. Consequently, the results present that:

(1) the digital Buck converter can share the similar electrical behaviors with the physical Buck converter with the estimated parameters; (2) due to the measurement error, modeling error, and different operating conditions of converter, the estimated health indicators fluctuate in a certain range instead of keeping at a stable value, which corresponds to the practical applications. After that, the cluster-based method is proposed to deal with this issue; (3) because of the series connection of R_{L} and R_{dson}, and the stable characteristic of inductor, a new equivalent average resistance R_{avg} is defined in this thesis to indicate the degradation of MOSFET; (4) the statistical method is used to quantitatively analyze and indicate the degradation trend of capacitor and MOSFET; (5) after the capacitor and MOSFET are intensively degraded by 8.8% and 0.64 Ω, respectively, the estimated C, R_{L}, and R_{dson} are changed by 9.7%, 21%, and 0.318 Ω correspondingly.

5 Feasibility study on the digital twin for single-phase inverter

This chapter studies the realization of the digital replica of a single-phase inverter firstly. Then, the PSO algorithm is introduced to analyze the data coming from both the physical single-phase inverter and its digital counterpart. So as to identify the unknown parameters of the digital twin. Thereafter, the experimental verification is given. The advantages and limitations of the implementation of digital twin concept in single-phase inverter, or even three-phase inverter, are discussed finally.

5.1 Establishment of the digital twin for single-phase inverter

Fig.73 depicts the topology of a single-phase inverter with considering the parasitic resistances of IGBT, diode, capacitor (R_C), and inductor (R_L). To simplify the analysis, the parasitic resistance of these four IGBTs is represented by $R_{CE,on}$. Likewise, the parasitic resistant of these four diodes is represented by $R_{D,on}$.

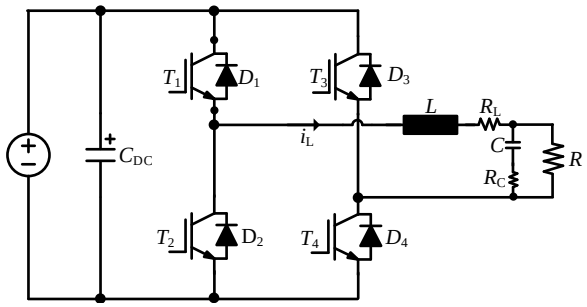


Fig. 73: Topology of single-phase inverter.

Based on the operation principle of single-phase inverter, it can be modeled as:

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_C}{dt} \\ v_o \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}(DR_{CE,on} + (1-D)R_{D,on} + R_L + \frac{R_C R}{R_C + R}) & -\frac{1}{L}\left(\frac{R}{R_C + R}\right) \\ \frac{1}{C}\left(\frac{R}{R_C + R}\right) & -\frac{1}{C}\left(\frac{1}{R_C + R}\right) \\ \frac{R_C R}{R_C + R} & \frac{R}{R_C + R} \end{bmatrix} \times \begin{bmatrix} i_L \\ v_C \end{bmatrix}$$

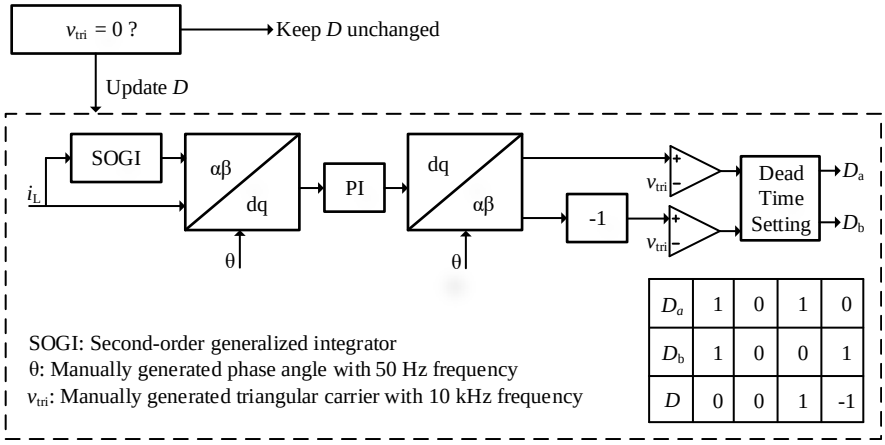
$$+D \begin{bmatrix} \frac{1}{L}V_{DC} \\ 0 \\ 0 \end{bmatrix} \tag{39}$$

where D is related to the on-off state of these four IGBTs. V_{DC} is the DC-link voltage. The load R is connected through a LC filter.

Similarly, (39) can be discretized by using the 4th-order Runge-Kutta method as introduced in Chapter 5 with acceptable accuracy-level:

$$\begin{cases} i_{\mathrm{L,n+1}} = a_1 i_{\mathrm{L,n}} + b_1 v_{\mathrm{c,n}} + c_1 \\ v_{\mathrm{C,n+1}} = a_2 i_{\mathrm{L,n}} + b_2 v_{\mathrm{c,n}} + c_2 \\ v_{\mathrm{o,n+1}} = a_3 i_{\mathrm{L,n}} + b_3 v_{\mathrm{c,n}} + c_3 \\ a_i = f_{ai}(L, C, R_{\mathrm{L}}, R_{\mathrm{C}}, R_{\mathrm{CE,on}}, R_{\mathrm{D,on}}, V_{\mathrm{DC}}, D, R) \\ b_i = f_{bi}(L, C, R_{\mathrm{L}}, R_{\mathrm{C}}, R_{\mathrm{CE,on}}, R_{\mathrm{D,on}}, V_{\mathrm{DC}}, D, R) \\ c_i = f_{ci}(L, C, R_{\mathrm{L}}, R_{\mathrm{C}}, R_{\mathrm{CE,on}}, R_{\mathrm{D,on}}, V_{\mathrm{DC}}, D, R) \end{cases} \tag{40}$$

where the coefficients a_{1-3}, b_{1-3}, and c_{1-3} are the functions with nine variables. Among them, L, C, R_{L}, R_{C}, and $R_{\mathrm{CE,on}}$ need to be estimated. $R_{\mathrm{D,on}}$ is set to a constant (e.g, 20 mΩ) based on datasheet. V_{DC} and R can be obtained off-line. D is calculated later. Thereafter, the digital twin of the data sampling circuit is built as well, which is same with that in Chapter 4. The i_{L} after the digital sampling circuit is used to calculate the on-off state D through the digital close-loop controller as shown in Fig.74. It can be seen that 40 and Fig.74 forms the digital twin of the single-phase inverter.



D_a	1	0	1	0
D_{b}	1	0	0	1
D	0	0	1	-1

Fig. 74: Digital twin of the control of the single-phase inverter.

The PSO algorithm is used to build the connection between the physical single-phase inverter and its digital counterpart as shown in Fig.75. It can update the unknown parameters of the digital converter by comparing the data coming from the digital and physical world. The detail of PSO is presented in Fig.61.

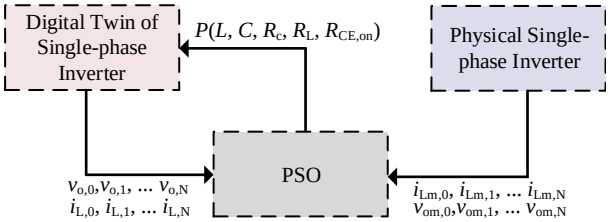


Fig. 75: Parameter estimation of single-phase inverter by using digital twin concept.

5.2 Experimental verification

The experimental verification of the digital twin realization is conducted with a physical single-phase inverter. The operation specification is set to 400 V DC-link voltage, 10 A peak inductor current, and 10 kHz switching frequency. Different *LC* filters are used as listed in Table 16.

Table 16: Value of Applied Inductors and Capacitors measured by LCR meter.

cases	L	C
case1	0.78 mH	4.8 μF
case2	0.78 mH	9.6 μF
case3	1.51 mH	4.8 μF
case4	1.51 mH	9.6 μF

The i_L and v_o over one fundamental period are recorded by the Oscilloscope (LECROY 3024), and used to estimate the unknown parameters of the digital single-phase inverter through the process in Fig.75. To investigate the consistency of the estimated results, the process in Fig.75 is repeated for 20 times with the recored data of each case. The corresponding results are displayed in Fig.76. It can be seen that the estimated *LC* fluctuate in a narrow range and have the error compared to the results measured with LCR meter. While the results of these parasitic resistances swing randomly below 100 mΩ. Those errors are attributed to: (1) The *LC* exhibit different values with the LCR meter measurement and in a operating converter due to different operational conditions; (2) the big difference between the voltages across those parasitic resistances and the DC-link voltage; (3) the accuracy-level of the developed digital twin; (4) the accuracy-level of the measured data from the physical inverter.

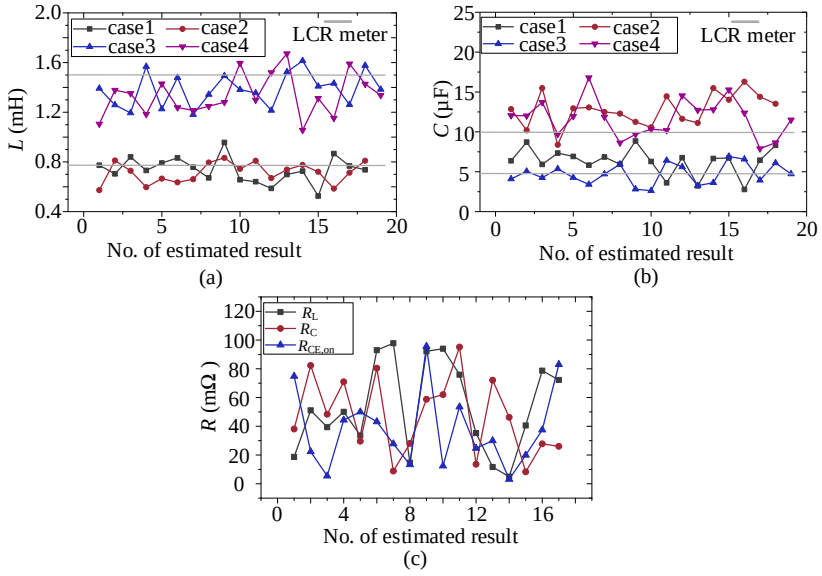


Fig. 76: Estimated results: (a) inductance; (b) capacitance; (c) parasitic resistances.

The estimated LC in Fig.76(a) and Fig.76(b) are averaged and listed in Table 17, along with the measured LC by LCR meter. It shows that although the errors are existed, the developed digital twin can still sense the changes of the LC. With the average of the estimated results in case1 and case4, the developed digital twin can operate itself and its operational waveforms i_{L} and v_{o} are compared with the counterpart of the physical inverter in Fig.77. It can be seen that the operational waveforms coming from both digital and physical inverter are overlapped with each other in a large degree. In overall, the developed digital twin is able to detect the change of LC from 0.78 mH/4.8 μF to 1.51 mH/9.6 μF without adding any additional hardware and intervening in the system to be monitored. While the parasitic resistances of L, C, and power switches can not be identified with the proposed method, which needs to be overcome in the future.

Table 17: Comparison of the Measured LC with LCR Meter and the Average of Estimated LC.

Cases	Measured LC	Estimated LC
case1	0.78 mH/4.8 μF	0.737 mH/6.3 μF
case2	0.78 mH/9.6 μF	0.715 mH/12.8 μF
case3	1.51 mH/4.8 μF	1.38 mH/4.72 μF
case4	1.51 mH/9.6 μF	1.34 mH/11.7 μF

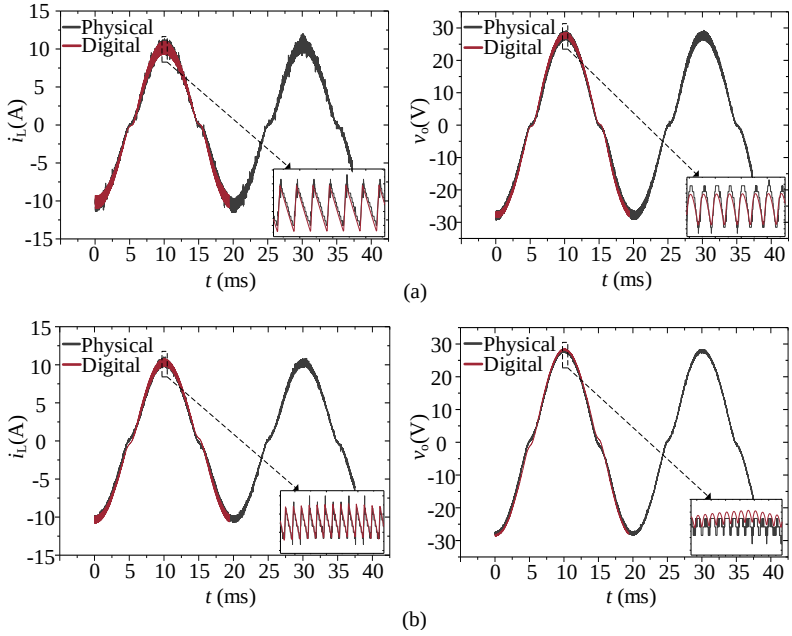


Fig. 77: Comparisons of i_L and v_o between the digital single-phase inverter and its physical counterpart: (a) case1; (b) case4.

5.3 Summary

The realization of the digital twin for a single-phase inverter is introduced in this Chapter with theoretical analysis firstly. It is composed of three parts: the digital twin of single-phase inverter, the physical single-phase inverter, and the particle swarm optimization algorithm. The experiments are conducted with different *LC* to verify the effectiveness of the proposed method. The results show that the change of *LC* from 0.78 mH/4.8 μF to 1.51 mH/9.6 μF can be detected. While the identified parasitic resistances of *L*, *C*, and power switches are randomly distributed below 100 mΩ. With the average of the identified results, the operational waveforms i_L and v_o of the digital twin and the physical single-phase inverter are overlapped with each in a large degree. Based on the results, the issues of the application of digital twin in single-phase inverter for condition monitoring are: 1): It is not able to identify those parasitic resistances; 2) the errors of the identified averaged *LC* are 6-11 % for *L* and 20-30 % for *C*, compared to the values measured by LCR meter. The application of digital twin for single-phase and three-phase converters are still facing various challenges and need to be improved in the future with the methods below: 1) take advantages of the special operation modes of the power converter that are sensitive to the changes of those parameters, e.g., the star-up and dynamics; 2) make the digital twin more close to its physical counterpart in principle; 3)separate the power converter system into several subsystems and build the corresponding sub-digital twins so that the parameter identification can be more simple.

Part IV. Conclusions

This part includes the summary of the contributions in this project, new research perspective and challenges for future study. There are one chapter in this part: **Chapter 6**. Summary and Outlook.

6 Summary and outlook

6.1 Summary and main contributions

The existing component-level health indicator measurement methods are limited to complex circuit and low cost-effectiveness. Also, the existing converter-level methods are not able to identify the source of degradation and present low degradation sensitivity. Moreover, the massive uncorrelated training data is required for artificial neural network based method. Finally, the calibration is required for health indicators to exclude the influences of impactors besides degradation, such as current, voltage, and temperature.

To meet the scientific needs, this project firstly proposes the converter-level on-state voltage monitoring method of power semiconductors for the purpose of condition monitoring. Then, the digital twin concept is studied and used to achieve the system-level condition monitoring of power converters. The main contributions are summarized as below:

- Converter-level on-state voltage monitoring circuits for power semiconductor devices

  Due to the limitations of conventional component-level solutions, a series of converter-level on-state voltage measurement circuits are proposed in this project, including the circuits with external/self power supply, and without power supply. The component selection is well discussed and all of them can achieve the on-line converter-level measurement with high accuracy-level (e.g., less than 0.1%) and fast dynamic response (e.g., less than 50 ns).

- Applications of the converter-level on-state voltage monitoring circuits

  The application of the proposed circuits in different power converters is investigated and discussed. Especially, the experimental verification is conducted with the single-phase and three-phase inverter case studies. It is proved that the proposed circuits have the features of reduced circuit complexity, size, cost, easy-of-implementation, and non-invasion, compared to conventional methods. Moreover, the power cycling testing and junction temperature estimation are conducted to verify the feasibility and effectiveness of the proposed circuits in monitoring the degradation process and junction temperature of power devices in an operating converter.

- Digital twin based condition monitoring in Buck converter

  The implementation of digital twin concept in monitoring the health condition of Buck converter is studied. It outperforms the conventional methods by excluding any additional hardware and being able to monitor both power switches and capacitors. The effectiveness and feasibility of the proposed method is verified with a Buck converter case study. The impacts of environmental and operational conditions are investigated while the key components of the converter are degraded. To exclude the impacts caused by the factors besides the degradation-level of components, a cluster-data based method is proposed so that the health condition can be obtained without off-line calibration.

- Feasibility study on the digital twin for single-phase inverter

The digital twin for a single-phase inverter is realized to monitor the passive components inductor and capacitor by the existing system-level signals (e.g., inductor current and output voltage). Through the experimental testing, it is found that the health indicator of power switches cannot be identified due to its low-sensitivity to the system signals, which can be explained by that the change of the health indicator (e.g., on-state resistance) of power switches is up to few mΩ, while the connected load could be higher than 10-100 Ω. In addition, the estimations of inductance and capacitance have the error by 11 % and 30 %, respectively, which are mainly due to the measurement error of the static voltage/current ripple, and also the accuracy of the developed digital twin. To overcome this issue, the further research needs to be proceeded in the future: 1) separate the digital twin into several sub-systems so that to achieve more accurate model; 2) utilize the special operation modes of power converter that could be more sensitive to the health indicators, such as the start-up transient due to the low power and dynamic response; 3) select more effective AI algorithm to solve the digital twin; 4) the current/voltage sensors with higher resolution and faster response time can be considered as well.

6.2 Research perspectives

The research outcomes of the PhD project brings up new research possibilities for further work:

- Implementation of hardware-based condition monitoring in field power converters

  Due to the complex implementation, intervening with the gate driver, and offline calibration requirement, most of the reported case studies on condition monitoring of power electronic components are still limited in laboratory testing. For field application, more practical issues need to be investigated, such as the measurement noise induced by the parasitic parameters of the connecting wires, the cost, and the size. Based on this, the proposed converter-level monitoring circuits are supposed to be more close to practical applications. Nevertheless, field testing is necessary to prove the assumptions.

  In addition, obtaining the health indicator is still the first step toward to a complete condition monitoring system. Although the data cluster based method is proposed and verified experimentally in laboratory, the variable environmental and operational conditions in practical applications differ from the laboratory condition in the data size and dimension. Therefore, the data processing algorithm need to be investigated, such as data selection, compression, and classification.

- Physics-informed data analysis for condition monitoring of power converters

  By considering that data logging is a future trend for power electronic industry, more and more data are collected anyway for various other purposes as well. It should be noted that the mentioned physics-informed data analytic methods are based on the knowledge of the expert in power electronics field, instead of a black-box based artificial intelligence algorithm since the required diversity

of the data for black-box training cannot be guaranteed in power electronics applications. This project proves that the condition monitoring for power converters can be realized by using the data driven and expert knowledge based method. It uses the existing data and does not require additional hardware. Although various challenges still need to be further solved in the future, it can be expected to be a promising direction to go for power electronics condition monitoring.

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Selected Publications

Journal publication 1

A Digital Twin Based Estimation Method for Health Indicators of DC–DC Converters

Y. Peng, S. Zhao, and H. Wang,

The paper has been accepted in the
IEEE Trans. Power Electron., 2020.

The layout has been revised.

A Digital Twin Based Estimation Method for Health Indicators of DC–DC Converters

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***Abstract*—This article proposes a health indicator estimation method based on the digital-twin concept aiming for condition monitoring of power electronic converters. The method is noninvasive, without additional hardware circuits, and calibration requirements. An application for a buck dc–dc converter is demonstrated with theoretical analyses, practical considerations, and experimental verifications. The digital replica of an experimental prototype is established, which includes the power stage, sampling circuit, and close-loop controller. Particle swarm optimization algorithm is applied to estimate the unknown circuit parameters of interest based on the incoming data from both the digital twin and the physical prototype. Cluster-data of the estimated health indicators under different testing conditions of the buck converter is analyzed and used for observing the degradation trends of key components, such as capacitor and MOSFET. The outcomes of this article serve as a key step for achieving noninvasive, cost-effective, and robust condition monitoring for power electronic converters.**

***Index Terms*—Condition monitoring, dc–dc power converters, digital twin, IGBT, parameter identification, reliability.**

I. Introduction

POWER converters are subject to frequent functional and environmental strains, which can induces failures. The failure mechanisms of power converter are generally separated into two categories: 1) abrupt failure due to over stress conditions; and 2) wearing out and degradation due to long-term operation. The fault diagnosis has been researched for many years to deal with abrupt failures, which is not the content of this article. After long-term operation, some components of power converter become too fragile to withstand the normal electrical and thermal stresses and a collapse of the entire system may happen.

Therefore, the anticipation of the degradation progress of power converter is important and meaningful so the fragile components can be replaced before a breakdown happens and it is called condition monitoring. It is revealed that the degradation progress of the key components in converters can be indicated by the change of their characteristic parameters, such as the ON-state resistance of MOSFET and capacitance of capacitor [1], [2]. Therefore, the measurement of those health indicators is critical and the first step of condition monitoring. Then, data processing method is used to assess the health condition of those key components with considering practical environmental and operational conditions. Overall, condition monitoring could be useful for predictive maintenance based on the estimated degradation level and remaining useful lifetime of the components of interest.

Component-level health indicators have been proposed for monitoring the degradation of power semiconductors and capacitors individually as shown in Table I [3]–[5], which can be classified into two groups: electrical and thermal indicators. Further, electrical indicators can be obtained from either the drain–source/collector–emitter terminals, such as the ON-state voltage or resistance of power semiconductors, which can be measured by using measurement circuits [1], [6]–[8]. These indicators show higher sensitivity to the degradation of power semiconductors among existing indicators. But additional circuits are needed, which increases the implementation complexity. Existing gate-emitter related indicators includes the threshold voltage and miller plateau of power semiconductor, which can be obtained from the gate turn-ON transient voltage waveform [9]–[12]. Since junction temperature is strongly related to the health condition of power semiconductors, temperature sensitive electrical parameters (TSEPs) can also be used as health indicator, such as prethreshold voltage in [13], peak gate current in [14], Kelvin-emitter voltage [15], and switching time in [16]. However, all of these gate related indicators are high frequency signals, demanding the high speed data acquisition circuit with good noise-immune ability, which increases the complexity further. Moreover, the malfunction of the added circuit may induce the failure of the gate driver. Thermal signals are also proposed for condition monitoring, such as case temperature in [17] and [18] and thermal resistance in [19]. However, case temperature may be easily interfered by other heat sources (e.g., the neighboring power modules and components, the ambient temperature) and shows a low degradation sensitivity. The measurement of thermal resistance strongly depends on the accuracy of measuring junction temperature, case temperature and power losses of interested module, which is complicated and difficult.

As for the capacitor, the condition monitoring can be achieved through two ways: 1) taking advantage of the discharge process of capacitor when the power converter is in offline [20]; and 2) by measuring the ripple of capacitor voltage and current, the

Manuscript received November 27, 2019; revised February 16, 2020, April 27, 2020, and June 10, 2020; accepted July 3, 2020. Date of publication July 15, 2020; date of current version September 22, 2020. This work was supported by the Innovation Fund Denmark through the Advanced Power Electronic Technology and Tools (APETT) Project 6154-00010B. Recommended for publication by Associate Editor P. Mattavelli. *(Corresponding author: Yingzhou Peng.)*

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Digital Object Identifier 10.1109/TPEL.2020.3009600

TABLE I
CONVENTIONAL CONDITION MONITORING METHODS

Items	Measured signals	Health indicators	Implementation complexity	Sensitivity to degradation	Invasion to original system
Component-level (power semiconductor)	Electrical signals	On-state voltage [6]–[8]	+++	++++	+++
		On-state resistance [1]	+++	++++	+++
		Threshold voltage [9]	++++	+++	++++
		Miller plateau [10], [11]	++++	+++	++++
		TSEPs [13]–[16]	++++	+++	++++
	Thermal signals	Case temperature [17], [18]	+	+	++
		Thermal resistance [19]	++++	++++	+++
Component-level (capacitor)	Discharge process	Capacitor voltage [20]	++	+++	+
	Capacitor voltage and current ripple	Capacitance and ESR [2], [21]–[23]	++++	++	+++
System-level (single component)	System signals	Frequency response [24]	++++	+	+++
		Harmonic [25]	++++	+	++++
		ANN [26], [27]	++++	++	+
System-level (multi-components)	System signals	Parameter identification [28]–[31]	++	++	+++
Data process	Calibration [6]	Indicators are also sensitive to temperature and current, they need to be calibrated.			
	Noise reduction [32], [33]	The measured indicators may consist of massive noises.			

TSEPs: temperature sensitive electrical parameters. ANN: artificial neural network. ESR: equivalent series resistance

equivalent series resistance (ESR) and capacitance of the capacitor can be obtained [2], [21]. However, in practice, obtaining the ripple requires more steps. First, capacitor current is measured indirectly by combining the input current, output current, and the switching information of the power converter [22], [23], which may cause transfer errors. Then, measuring the ripple requires both the data acquisition apparatus with higher sampling rate and higher resolution, and high frequency pass filter circuit.

From the system-level view, various methods have been proposed to monitor the power semiconductors and capacitors, respectively, as listed in Table I. The frequency response of dc–dc converters is sensitive to the ON-state resistance of power semiconductors in specific situations [24]. In addition, the output current harmonic of inverter is investigated to monitor the degradation of the solder layer of power semiconductor in [25]. Both methods require extra setups and show invasive to the system of interest. Moreover, they cannot distinguish the degradation of power semiconductor and capacitor. Artificial neural network is also a potential way for monitoring the degradation of capacitor [26], [27]. However, it requires offline testing to obtain the enough training data, which is difficult to achieve in practice.

Conventional model-based parameter identification methods are used to modify the controller of power converters as listed in Table I. It is known that the transfer function between the output voltage and duty cycle ratio is discretized when design controller. Thus, the coefficients of transfer function can be calculated by using different algorithms, such as recursive least square (RLS) in [28] and Kalman filter (KF) in [29], which is effective in tuning controller and improving the system performance. However, mapping the coefficients of transfer function into the internal parameters of the converter could cause transfer errors and even does not have feasible solutions when the number of unknown parameters are more than that of the known equations. In [31], a simplified model of boost converter is built and a generalized gradient descent algorithm is applied to calculate the inductance and capacitance. A model for buck converter is developed in [30], where biogeography-based optimization method is used to identify the internal parameters. The main issues with the above methods are that none of them focus on the degradation monitoring of the key components. Moreover, only the coefficients of the model (e.g., transfer function) or part of those physical parameters (e.g., inductance and capacitance) can be obtained. In addition, all of the above methods need to inject extra signal into the controller.

It is worth to mentioning that these measured indicators need to be processed further to reduce noises and to indicate the health status of power converter numerically. Such as low-pass filter and Gaussian process [32], [33]. Finally, calibration with other impactors (e.g., temperature and current) is needed as well. [6].

According to the analysis above, the challenges are still existed in these existing methods and they are expected to updated with the features of noninvasive, calibration-free, without additional circuits and the ability of monitoring both power semiconductor and capacitor.

Digital twin is a virtual representation of a physical system that virtually shares the same characteristics with its physical counterpart. It enables customers to better understand, optimize, predict, and monitor the performance of its installed systems [34], [35]. The concept of digital twin has been applied in power converters for fault diagnosis recently [36], [37], which is achieved by comparing the output signals of the digital twin and its physical counterpart in real-time. In this article, the digital twin concept is used to estimate the health indicators of the key components in power converter, so as the degradation progress of power converter can be monitored. The digital twin technology includes two parts: the digital presentation of a physical system and an advanced algorithm for data analysis.

First, a digital twin concept-based health indicator estimation method is proposed for a dc–dc converter case study. This digital twin is a virtual replica of physical converter and is able to update itself continuously according to the data coming from existing sensors in its physical counterpart. Then, PSO algorithm is applied to do data analysis and make the difference between the digital twin and its physical counterpart smaller than a preset threshold. Finally, a data-cluster concept is proposed to cover the estimated indicators at different possible operations.

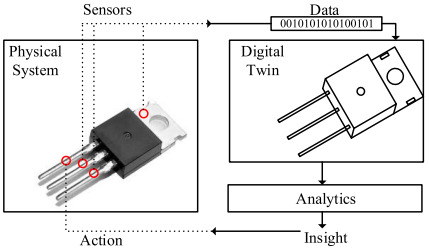

Fig. 1. Example of the application of digital twin.

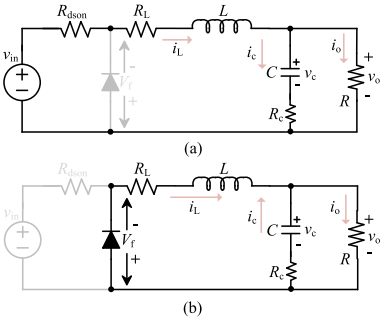

Fig. 2. Equivalent circuits of buck converter: (a) MOSFET is in ON-state; (b) MOSFET is in OFF-state.

The contributions of this article are: 1) it is easy to implement by taking advantage of existing sensors; 2) without additional hardware and modification in the system of interest; 3) it is capable of monitoring the degradation of the key components simultaneously; and 4) by taking advantage of cluster-data based method to achieve the calibration-free and compensate the shortage of the proposed method in the low sensitivity to degradation. Part of the contents of this article have been presented in [38], which mainly discussed the basic idea of the proposed method. In this article, the state-of-the-arts discussion is enriched by considering component-level, system-level, single component, and multicomponents based condition monitoring methods. Moreover, the detail of the digital twin concept is illustrated through a MOSFET-based example and the experimental validation is carried out in a buck converter demonstrator with practical considerations, such as different voltages, currents, loadings, and temperatures. In addition, a data analysis method is also given in this article.

II. Digital Twin of Buck Converter

A. Digital Twin Concept

An example of MOSFET-based digital twin is taken to illustrate the principle of digital twin first as shown in Fig. 1 with seven components and they are explained as follows.

1) *Physical system:* A real physical object or process.
2) *Sensors:* Sensors are used to capture the operational signals of physical system, which could be voltage, current or temperature, etc.
3) *Data:* The data from the sensors represent the operational condition or characteristics of physical system and they are used to update the digital twin continuously.
4) *Digital twin:* A digital replica of physical system.
5) *Analytics:* Analytics techniques are used to process the data from the sensors by using advanced algorithms and make the insights of digital twin same with the insights of its physical counterpart as much as possible.
6) *Insight:* The inside information of digital twin. The insights could be used to guide the action of physical system and better its performance. Also, it can be used to assess the operation condition of physical system.
7) *Action:* According to the insights from analytics, action could be performed to better the performance of physical system or protect the physical system.

B. Buck Converter Modeling

Fig. 2 shows the equivalent circuits of buck converter operating at ON-state and OFF-state, which is represented by

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \\ v_o \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}A & -\frac{1}{L}\left(\frac{R}{R_c+R}\right) \\ \frac{1}{C}\left(\frac{R}{R_c+R}\right) & -\frac{1}{C}\left(\frac{1}{R_c+R}\right) \\ \frac{R_cR}{R_c+R} & \frac{R}{R_c+R} \end{bmatrix} \times \begin{bmatrix} i_L \\ v_c \end{bmatrix} + D\begin{bmatrix} \frac{1}{L}v_{in} \\ 0 \\ 0 \end{bmatrix} + (1-D)\begin{bmatrix} -\frac{1}{L}V_f \\ 0 \\ 0 \end{bmatrix}$$

$$A = \left(DR_{dson} + R_L + \frac{R_cR}{R_c+R}\right) \tag{1}$$

where i_L is the inductor current, v_o is the output voltage and v_c is the capacitor voltage; R_{dson}, R_L, and R_C are the parasitic resistances of MOSFET, inductor and capacitor, respectively; v_{in} is the input voltage and V_f is the forward voltage of diode; and D is 1 when the MOSFET is ON and 0 when the MOSFET is OFF.

Two ways can be applied to solve (1), and obtain i_L and v_c. One is to calculate the eigenvector and eigenvalue of differential equations and construct the general solution. Then, by using the initial values of i_L and v_c, the specific solution of these differential equations can be obtained [30]. This method demands heavy computation, especially the calculation of eigenvector and eigenvalue. The other one is to linearize the differential equations with acceptable accuracy, which is used in this article. Then, the output voltage v_o can be described with discrete time step

$$v_{o,n+1} = i_{L,n+1}\frac{R_cR}{R_c+R} + v_{c,n+1}\frac{R}{R_c+R} \tag{2}$$

where the nth time step is defined as the present time interval, and the $(n+1)$th time step represents the next one. $v_{o,n+1}$ indicates the output voltage at $(n+1)$th step, which is unknown at present nth step. Therefore, in the following discussions, $i_{L,n+1}$ and $v_{c,n+1}$ are derived based on the present values $i_{L,n}$ and $v_{c,n}$,

so that the output voltage at the $(n+1)$th time step can be represented by the inductor current and capacitor voltage at nth time step.

Runge–Kutta is a typical method to solve differential equations [39]. A typical fourth-order Runge–Kutta method is used in this article to linearize the differential equations and it is considered as sufficient for buck converter modeling to achieve an negligible error. To simplify the analysis process, (1) is rewritten as follows:

$$\begin{cases} f_1(i_{\mathrm{L}}, v_{\mathrm{c}}) = \dfrac{di_{\mathrm{L}}}{dt} \\ f_2(i_{\mathrm{L}}, v_{\mathrm{c}}) = \dfrac{dv_{\mathrm{c}}}{dt}. \end{cases} \tag{3}$$

With fourth-order Runge–Kutta method, $i_{\mathrm{L,n+1}}$ and $v_{\mathrm{c,n+1}}$ can be expressed as follows:

$$\begin{cases} i_{\mathrm{L,n+1}} = i_{\mathrm{L,n}} + \dfrac{h}{6}\left(k_{\mathrm{a1}} + 2k_{\mathrm{a2}} + 2k_{\mathrm{a3}} + k_{\mathrm{a4}}\right) \\ v_{\mathrm{c,n+1}} = v_{\mathrm{c,n}} + \dfrac{h}{6}\left(k_{\mathrm{b1}} + 2k_{\mathrm{b2}} + 2k_{\mathrm{b3}} + k_{\mathrm{b4}}\right) \end{cases} \tag{4}$$

where k_{a1}-k_{a4} and k_{b1}-k_{b4} are used to calculate the average change rate between (n)th and $(n+1)$th step shown as follows:

$$\begin{cases} k_{\mathrm{a1}} = f_1\left(x_{\mathrm{n}}, y_{\mathrm{n}}\right) \\ k_{\mathrm{b1}} = f_2\left(x_{\mathrm{n}}, y_{\mathrm{n}}\right) \\ k_{\mathrm{a2}} = f_1\left(x_{\mathrm{n}} + \dfrac{h}{2}k_{\mathrm{a1}}, y_{\mathrm{n}} + \dfrac{h}{2}k_{\mathrm{b1}}\right) \\ k_{\mathrm{b2}} = f_2\left(x_{\mathrm{n}} + \dfrac{h}{2}k_{\mathrm{a1}}, y_{\mathrm{n}} + \dfrac{h}{2}k_{\mathrm{b1}}\right) \\ k_{\mathrm{a3}} = f_1\left(x_{\mathrm{n}} + \dfrac{h}{2}k_{\mathrm{a2}}, y_{\mathrm{n}} + \dfrac{h}{2}k_{\mathrm{b2}}\right) \\ k_{\mathrm{b3}} = f_2\left(x_{\mathrm{n}} + \dfrac{h}{2}k_{\mathrm{a2}}, y_{\mathrm{n}} + \dfrac{h}{2}k_{b2}\right) \\ k_{\mathrm{a4}} = f_1\left(x_n + hk_{\mathrm{a3}}, y_{\mathrm{n}} + hk_{\mathrm{b3}}\right) \\ k_{\mathrm{b4}} = f_2\left(x_n + hk_{\mathrm{a3}}, y_{\mathrm{n}} + hk_{\mathrm{b3}}\right) \end{cases} \tag{5}$$

where h is the calculation step time between nth and $(n+1)$th time step.

Substitute (3) into (5), (5) into (4), and (4) into (2), the final expression of v_{o} can be obtained as:

$$\begin{cases} v_{\mathrm{o,n+1}} = ai_{\mathrm{L,n}} + bv_{\mathrm{c,n}} + c \\ a = f_3(L, C, R_{\mathrm{L}}, R_{\mathrm{C}}, R_{\mathrm{dson}}) \\ b = f_4(L, C, R_{\mathrm{L}}, R_{\mathrm{C}}, R_{\mathrm{dson}}) \\ c = f_5(L, C, R_{\mathrm{L}}, R_{\mathrm{C}}, R_{\mathrm{dson}}) \end{cases} \tag{6}$$

where coefficients a, b, and c are constructed by seven parameters (L, C, R_{L}, R_{C}, R_{dson}, D, and v_{in}) with complicated combinations since there are five layers substitution from (3) to (2). Among them, L, C, R_{L}, R_{C}, and R_{dson} are unknown parameters. D is calculated through the sampling circuit model and close-loop controller model described later. v_{in} is measured from the physical converter. Therefore, the output voltage at $(n+1)$th step can be calculated by using the inductor current and capacitor voltage at nth step. Then, v_{o} is used to determine the ON–OFF state of MOSFET D through the following sampling circuit and close-loop controller model.

C. Sampling Circuit

A typical sampling circuit is adopted, which includes a differential amplifier circuit and a $R_{\mathrm{f}}C_{\mathrm{f}}$ low-pass filter as shown in Fig. 3. The amplifier output voltage v_{p} is

$$v_{\mathrm{p,n+1}} = \frac{(R_3 + R_4)R_2}{(R_1 + R_4)R_5} v_{\mathrm{o,n+1.}} \tag{7}$$

The output of $R_{\mathrm{f}}C_{\mathrm{f}}$ filter v_{ad} is

$$\begin{cases} v_{\mathrm{ad,n+1}} = v_{\mathrm{p}} - R_{\mathrm{f}}C_{\mathrm{f}}\dfrac{dv_{\mathrm{ad,n+1}}}{dt} \\ f_6(v_{\mathrm{ad,n+1}}) = \dfrac{dv_{\mathrm{ad,n+1}}}{dt} = \dfrac{v_{\mathrm{p}} - v_{\mathrm{ad,n+1}}}{R_{\mathrm{f}}C_{\mathrm{f}}}. \end{cases} \tag{8}$$

Based on fourth-order Rung–Kutta method, (8) can be linearized as follows:

$$\begin{cases} v_{\mathrm{ad,n+1}} = v_{\mathrm{ad,n}} + \dfrac{h}{6}\left(k_1 + 2k_2 + 2k_3 + k_4\right) \\ k_1 = f_3\left(y_{\mathrm{n}}\right) \\ k_2 = f_3\left(y_{\mathrm{n}} + \dfrac{h}{2}k_1\right) \\ k_3 = f_3\left(y_{\mathrm{n}} + \dfrac{h}{2}k_2\right) \\ k_4 = f_3\left(y_{\mathrm{n}} + hk_3\right). \end{cases} \tag{9}$$

D. Close-Loop Controller

To obtain modulation signal v_{m}, the close-loop controller is built in digital twin as shown in Fig. 3. The process of controller can be expressed by following linear equations:

$$\begin{cases} v_{\mathrm{e,n}} = v_{\mathrm{e,n+1}} \\ v_{\mathrm{m,n}} = v_{\mathrm{m,n+1}} \\ v_{\mathrm{e,n+1}} = V_{\mathrm{ref}} - v_{\mathrm{ad,n+1}} \\ v_{\mathrm{m,n+1}} = v_{\mathrm{m,n}} + K_{\mathrm{p}}(v_{\mathrm{e,n+1}} - v_{\mathrm{e,n}}) + K_I h v_{\mathrm{e,n+1}} \end{cases} \tag{10}$$

where V_{ref} is the reference of the output voltage, v_{e} is the error between the output voltage and its reference, v_{m} is the modulation signal, and K_{P} and K_{I} are the parameters of the PI controller. Based on (10), the digital twin of buck converter can generate the modulation signal by itself instead of accessing to the physical controller. It is worth to mentioning that the sampling rate of physical buck converter system is usually set to the switching frequency and the time delay in updating the duty cycle ratio should be considered.

Then, the ON–OFF state of MOSFET D is decided by comparing v_{m} with a triangular carrier signal v_{tri} as follows:

$$D_{\mathrm{n+1}} = \begin{cases} 1(v_{\mathrm{m,n+1}} \geq v_{\mathrm{tri,n+1}}) \\ 0(v_{\mathrm{m,n+1}} < v_{\mathrm{tri,n+1}}). \end{cases} \tag{11}$$

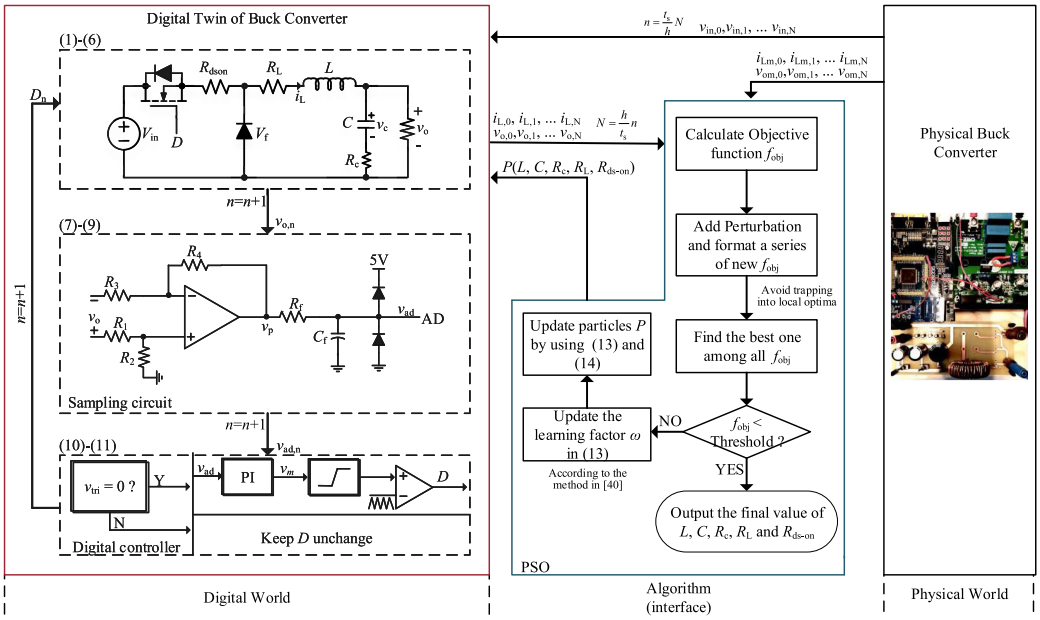

Fig. 3. Case study of the application of digital twin concept in condition monitoring with a buck converter ($n = n + 1$ means updating the time step, R_1–R_4, R_f, and C_f are the parameters of sampling circuit, $v_{\rm tri}$ is the triangular carrier, $f_{\rm obj}$ is the objective function, w is the learning factor in (13), N is the number of sampled output voltage and inductor current from physical converter, n is the total iteration steps of the digital twin for updating parameters one time, $t_{\rm s}$ is the sampling period of measuring output voltage, inductor current, and input voltage from physical converter, and h is the calculation time step interval inside the digital twin).

III. Application of Digital Twin in Condition Monitoring

The final model of the buck converter developed in this article is expressed by (6). It can be seen that the coefficients a, b, and c are highly nonlinear functions with five variables. Therefore, the traditional algorithms, like RLS and KF, are not able to estimate the developed model in this article [40]. Further, the extended Kalman filter (EKF) is proposed to solve the nonlinear problem. However, It suffers instability due to the linearization and costly derivative calculation of Jacobian or Hessian matrices, and its performance deteriorates when the signal model is highly nonlinear [41]. More importantly, a critical point during the design of EKF and unscented Kalman filter is the determination of the covariance matrices of the process noise, the measurement noise, and the initial state vector, which are often estimated from a tedious trail-and-error tuning or self-tuning algorithms [29], [40], [42]. Considering the complex process and restrictions of EKF, PSO is chosen in this article because it is an end-to-end solution, and has a simpler implementation process and better generality to different models. It is agreed that PSO requires more computation than KF-based algorithms. But the computation time of the algorithm is not critical in the application presented here, since the degradation of power electronic components is a slow process itself.

PSO is a population-based iterative optimization algorithm that mimics the swarm behavior in birds flocking and fish schooling to guide the particles to search for the globally optimal solutions [43]. Based on this, it is possible to search for the optimal solutions of the internal parameters of digital twin buck converter. To implement PSO, the first step is to construct an objective function. In this article, the objective function is as follows:

$$f_{\rm obj} = \frac{\sum_{j=1}^{N}\left[\left(i_{\rm L,j} - i_{\rm Lm,j}\right)^2 + \left(v_{\rm o,j} - v_{\rm om,j}\right)^2\right]}{N} \tag{12}$$

where $i_{\rm L,j}$ and $v_{\rm o,j}$ are, respectively, the calculated inductor current and output voltage from the digital twin buck converter. $i_{\rm Lm,j}$ and $v_{\rm om,j}$ are the measured data from the physical buck converter, and N is the sample size of the measured data. The internal parameters of physical buck converter can be obtained by minimizing the objective function defined in (12) with PSO algorithm.

The procedure of the proposed digital twin-based condition monitoring method is shown in Fig. 3, which includes three parts: digital world, physical world, and the interface (PSO algorithm) between them. P represents the parameter set including L, C, $R_{\rm c}$, $R_{\rm L}$, and $R_{\rm dson}$. First, the parameter set P, $i_{\rm L}$, $v_{\rm c}$, and the ON–OFF state D are initialized and n is 0 at the beginning

time step. Then, the inductor current i_{L}, capacitor voltage v_{c}, and output voltage v_{o} at next step can be calculated through (4) and (6), and the time step is updated by $n = n + 1$. Finally, D is updated through the developed sampling circuit and close-loop controller model and sent back into converter model to do next loop calculation.

Because the calculation time step h is different with the sampling period t_{s}. The number of calculated i_{L} and v_{o} n is reduced to N by $N = hn/t_{\mathrm{s}}$ evenly. Then, the calculated i_{L} and v_{o} sets from the digital twin and the measured i_{Lm} and v_{om} sets from the physical one are used to calculate f_{obj} by (12). Thereafter, perturbation mechanism is added to avoid trapping into local optima by constructing a series of new f_{obj}. After that, the best f_{obj} among all f_{obj} is found. If the f_{obj} is smaller than the preset threshold, the output parameter set from the digital twin represents the operational condition of physical buck converter. Otherwise, the parameter set will be updated by the following equations:

$$V_{\mathrm{i,j}} = \omega_{i-1} V_{\mathrm{i-1,j}} + 2r_{1,\mathrm{i-1,j}} \left(P_{\mathrm{G}} - P_{\mathrm{i-1,j}}\right) + 2r_{2,\mathrm{i-1,j}} \left(P_{\mathrm{L,i-1,j}} - P_{\mathrm{i-1,j}}\right) \quad (13)$$

$$P_{\mathrm{i,j}} = P_{\mathrm{i-1,j}} + V_{\mathrm{i,j}} \quad (14)$$

where i is the number of iteration, j is the number of particle, $V_{\mathrm{i,j}}$ is the moving velocity of the jth particle in ith iteration; P_{G} is the global optimization, $P_{\mathrm{L,i-1,j}}$ is the individual optimization of the jth particle until $(i-1)$th iteration; $P_{i,j}$ is the position of the jth particle in ith iteration; and w is the learning factor that is updated continuously according to the method presented in [43]. r_1 and r_2 are weighting factors and are set to 2. The detail about how to chose these factors can be found in [43].

Finally, the new obtained P is sent back into the digital twin of buck converter to do next step calculation.

In addition, the converging process of PSO may trap into local optima. To avoid this, a proper perturbation is needed. In this article, after obtaining the global optimization P_{G} in each iteration, a perturbation factor is introduced to construct a series of new particles. Then, a series of new f_{obj} can be obtained. The detail of the perturbation process can be see in [44].

IV. Application for Condition Monitoring and Experimental Validation

To validate the proposed method, a buck converter demonstrator is built, as shown in Fig. 4(a), and its specifications are presented in Table II. The LC filter module is built by using several different inductors and capacitors, then they can be switched easily during test. This article leverages the load change transients, which is relevant to many practical applications. The example waveforms are shown in Fig. 4(b) and part of the waveform data are used in this article.

A. Parameter Identification

By following the procedure shown in Fig. 3, the parameters of buck converter can be obtained. Fig. 5(a) shows the descending process of f_{obj} and its final value is 6e-4 after 50 generations. Meanwhile, these parameters converge to a stable value after 50 generations as illustrated in Fig. 5(b) and (c), which means the difference of the output waveforms between the digital twin buck converter and its physical counterpart is 6e-4. At this moment, these estimated parameters represent the condition of physical buck converter.

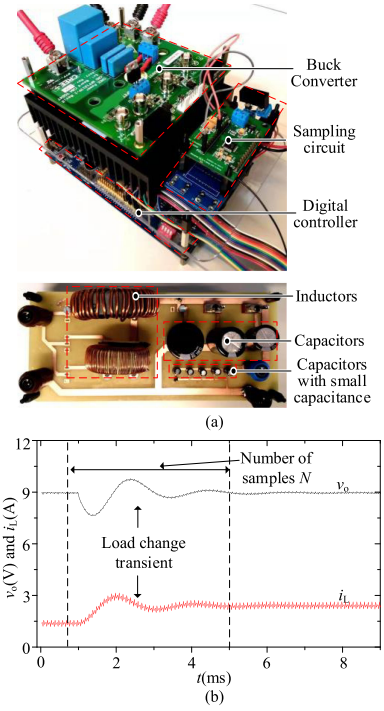

Fig. 4. Experimental setup. (a) Physical buck converter system. (b) Load change transient waveforms of i_{L} and v_{o}.

TABLE II
Specifications of Buck Converter

Specification	Value
$V_{\mathrm{in}}/V_{\mathrm{ref}}$	24 V/9 V
$V_{\mathrm{in}}/V_{\mathrm{ref}}$	48 V/24 V
$V_{\mathrm{in}}/V_{\mathrm{ref}}$	110 V/24 V
Switching frequency f_{sw}	20 kHz
Loading 1/2/3	10.4 Ω / 4.9 Ω/ 3.3 Ω
L (μH)	782
C (μF)	151

The comparisons of i_{L} and v_{o} between the digital twin buck converter and the physical one are shown in Fig. 6. It can be seen that the waveforms are almost overlapped with each other in both dynamic and static responses, which indirectly prove that the estimated parameters by using the proposed method are very close to the real parameters in the physical one.

For condition monitoring, practical issues should be considered. In the rest of this article, the impact of sampling rate, the uncertainty caused by errors, the different voltage conversions, loadings, and temperatures are discussed. Simultaneously

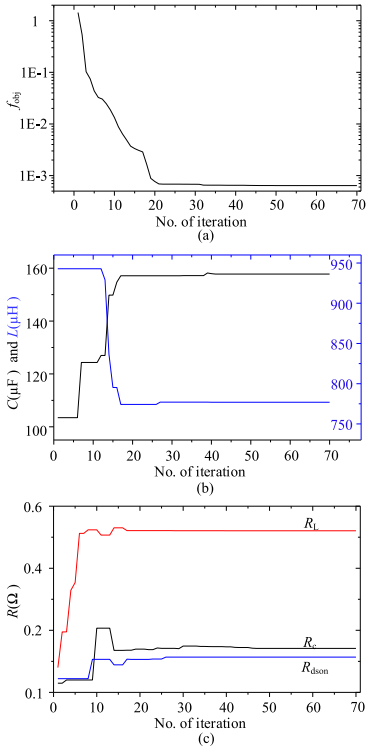

Fig. 5. Process of parameter convergence. (a) Descent process of objective function. (b) Capacitance and inductance. (c) Parasitic resistances $R_{\rm L}$, $R_{\rm c}$ and $R_{\rm dson}$.

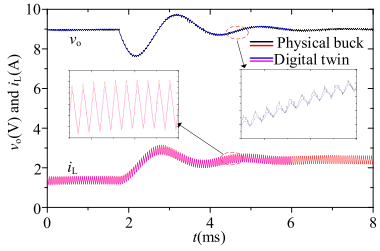

Fig. 6. Comparisons of inductor current and output voltage between digital twin buck converter and its physical counterpart (sampling rate = 1 MHz).

parameter degradation monitoring for capacitor and MOSFET is investigated quantitatively as well.

B. Impact of Sampling Rate

The digital twin works as a sensor-enabled digital model of a physical system. Thus, the sampling rate may affect the accuracy

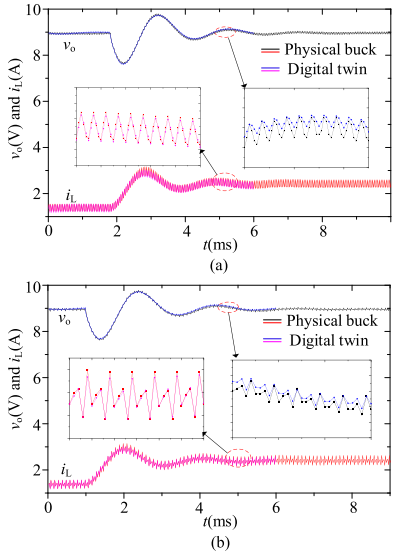

Fig. 7. Comparisons of inductor current and output voltage between digital twin buck converter and its physical counterpart in different sampling rate (the situation when $f_{\rm sr}$ = 1 MHz is presented in Fig. 6): (a) $f_{\rm sr}$ = 100 kHz; (b) $f_{\rm sr}$ = 50 kHz.

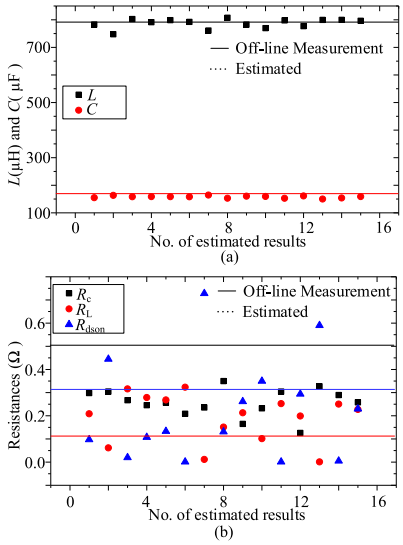

Fig. 8. Estimated results when $V_{\rm in}/V_{\rm o}$ is 24/9 V and the load is changed from 4.85 to 3.32 Ω, and the measured results offline (the proposed method is repeated for 15 times to show the fluctuation of estimated results, but the load change transient data is measured for only 1 time. The $R_{\rm dson}$ is measured offline by conducting a certain current). (a) Inductance and capacitance. (b) Parasitic resistances.

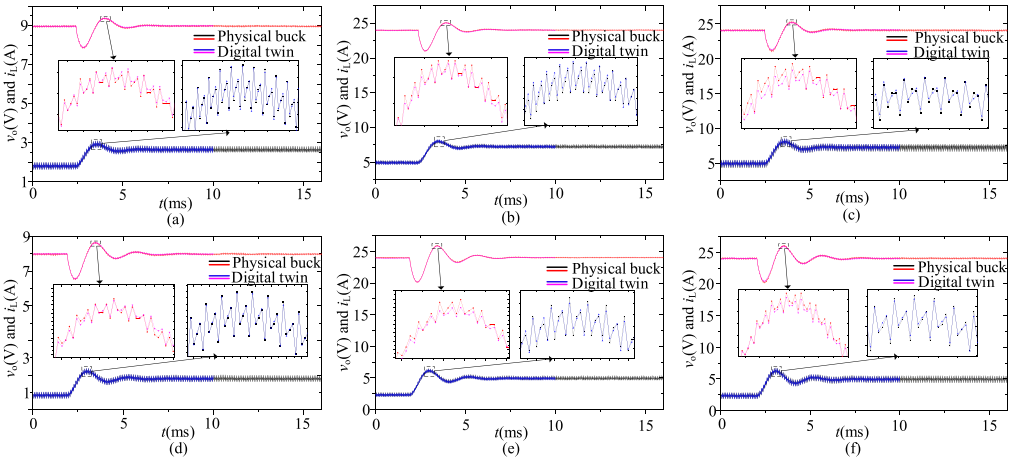

Fig. 9. Comparisons of the output waveforms between the digital twin and its physical counterpart in different operational conditions: (a) case1; (b) case3; (c) case5; (d) case2; (e) case4; (f) case6.

of the results of the digital twin. To uncover this, the proposed method is performed in different sampling rate situations and the results are shown in Fig. 7 (the situation when $f_{\rm sr} = 1$ MHz is presented in Fig. 6). With different sampling rate, the ripples of $i_{\rm L}$ and $v_{\rm o}$ in digital twin and physical one are different. However, they show the same result in dynamic responses. it is known that inductance and capacitance are sensitive to the dynamic responses of $i_{\rm L}$ and $v_{\rm o}$, while the parasitic resistances are sensitive to the ripples of $i_{\rm L}$ and $v_{\rm o}$. Therefore, lower sampling rate could cause higher measurement errors in the ripples of $i_{\rm L}$ and $v_{\rm o}$, which may lead to errors in estimating the results of parasitic resistances.Therefore, to sense the change of the switching ripple, a sampling rate with at least double switching frequency is needed, as shown in Fig. 7(b). In the rest of this article, 50 kHz sampling rate is chosen to acquire $i_{\rm L}$ and $v_{\rm o}$.

C. Impact of Errors

To investigate the consistency of the proposed method, Fig. 8 includes the results of the estimated inductance, capacitance, and parasitic resistances for 15 repeated estimations. It can be noted that the estimated capacitance and inductance exhibit smaller fluctuation along with the results measured offline (LC and their parasitic resistances are measured by *LCR* meter, $R_{\rm dson}$ is measured by conducting a certain current), compared to that of parasitic resistances, since the capacitor and inductor are more sensitive to the load dynamics of the buck converter. Among parasitic resistances, the estimated result of $R_{\rm c}$ is more stable than the results of $R_{\rm L}$ and $R_{\rm dson}$. Because the inductor and MOSFET in buck converter can be seen as in series, which is discussed in the part F of Section IV. Overall, the certain level of estimation errors exist with the proposed method and are caused by: 1) the developed digital twin without considering the parasitic parameters of wires; 2) the sampling circuit without sensing very accurate voltage and current; 3) the different processor of close-loop controller between physical buck converter (DSP) and digital twin (computer); and 4) in relative to the results measured offline, those parameters experience changes when the converter is in operation.

TABLE III
DIFFERENT OPERATIONAL CONDITIONS

Cases	$V_{\rm in}/V_{\rm o}$ (V)	Load change (Ω)
case1	24/9	4.85/3.32
case2	24/9	10.43/4.85
case3	48/24	4.85/3.32
case4	48/24	10.43/4.85
case5	110/24	4.85/3.32
case6	110/24	10.43/4.85

D. Impact of Environmental and Operation Conditions

In practice, the environmental and operation conditions can also affect the values of the health indicators, besides the degradation level of the components of interest, which is a common issue to various condition monitoring methods to date. Moreover, as shown in Fig. 8, there are certain level of estimation errors. One way to address the issue is to calibrate the components of interest at different environmental and operation conditions, as applied in [6] and [7]. Nevertheless, it is time consuming and may not be practical by considering that it is necessary to calibrate each components in each produced unit due to the initial parameter variations among a population of units. In order to avoid the calibration process, this article proposes a data-cluster based method for condition monitoring.

To achieve this, the proposed method is tested in six different operational conditions as listed in Table III. The corresponding results are depicted in Fig. 9, showing that the proposed digital

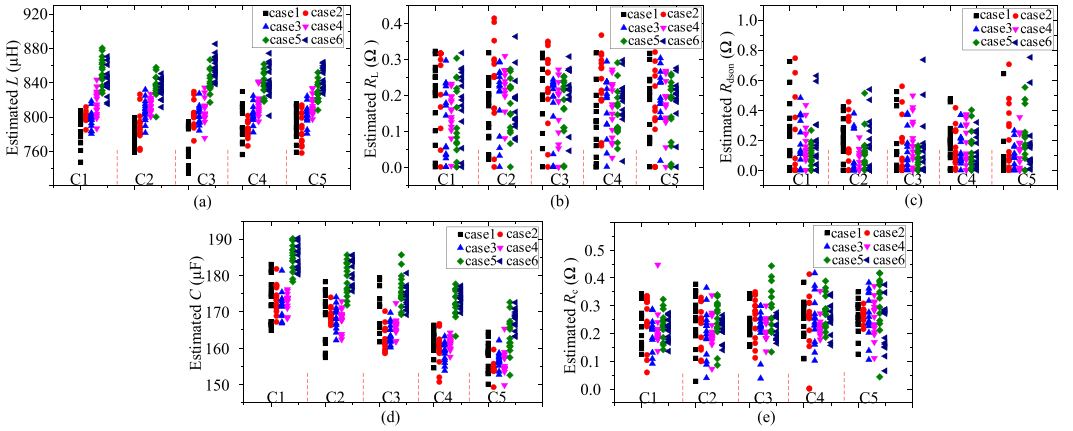

Fig. 10. Estimated results in different operational cases and when C is manually decreased from C1 to C5 (here MOSFET M1 is applied. case 1–6 are described in Table III, C1–C5 are described in Table IV): (a) L; (b) $R_{\rm L}$; (c) $R_{\rm dson}$; (d) C; (e) $R_{\rm c}$.

TABLE IV
PERCENTAGE CHANGE OF CAPACITANCE DURING TEST

Caps	C1	C2	C3	C4	C5
Δ C	0% (165 μF)	-2.2%	-4.4%	-6.6%	-8.8%

TABLE V
ON-STATE RESISTANCES OF THE MOSFETS UNDER TEST

MOSFETs	M1	M2	M3	M4	M5
$R_{\rm dson}$ (Ω)	0.11	0.241	0.385	0.495	0.75

TABLE VI
CASE TEMPERATURE OF THE MOSFETS UNDER TEST IN DIFFERENT OPERATIONAL CONDITIONS (UNIT: °C)

Cases	$T_{\rm c-M1}$	$T_{\rm c-M2}$	$T_{\rm c-M3}$	$T_{\rm c-M4}$	$T_{\rm c-M5}$
case1	27.5	27.8	28	28.8	28.3
case2	25.7	26.8	26.5	27.1	26.5
case3	29	39.4	40.9	44	55
case4	26.5	29.1	29.3	32.8	34.8
case5	28.4	32.4	36.7	37.3	39.5
case6	26.1	27.5	28.4	29.7	30.8

twin is able to present the similar operation characteristics with its physical counterpart even in different operational conditions. The identified parameters are given in next section. In this article, five capacitances and five MOSFETs are used to simulate the degradation level of capacitor and MOSFET as listed in Tables IV and V, respectively. It should be noted that the case temperatures of MOSFETS are different in operation due to the different power losses as recorded in Table VI.

E. Capacitor Degradation Monitoring

It has been revealed that the capacitance may drop by 5%–20% after a long-term operation [5]. Therefore, in this article, another four capacitors with small capacitance (3.6 μF for each one) are in parallel with the original capacitor (151 μF), as shown in Fig. 4(a) and Table IV. Then, these extra four capacitors are taken away one by one to simulate the degradation of capacitor (each one represents the drop of capacitance by 2.2%). In order to cover the fluctuations of the estimated results, the procedure shown in Fig. 3 is performed for 15 times with an individual recorded $i_{\rm L}$ and $v_{\rm o}$. Fig. 10 summarizes the estimated results. The simulated degradation levels of capacitor are indicated with the data clusters from C1 to C5. The operational cases are represented by different colors. The data with the same color represents the distribution of the estimated results at a given condition. Among them, the estimated L, $R_{\rm L}$, and $R_{\rm dson}$ are independent from the change of capacitance. While, for the capacitor related parameters, after taking away the paralleled capacitors one by one, although part of the data within the adjacent clusters are overlapped, collectively, the estimated cluster of capacitances decrease constantly. Meanwhile, the estimated $R_{\rm c}$ has a slightly increasing trend.

The self-heating can only increase the case temperature of capacitor $T_{\rm c}$ by 3 °C. Therefore, a heater is sticked on the surface of the capacitor to increase the $T_{\rm c}$ and to investigate the effect of the temperature on the proposed method. It can be seen from Fig. 11 that the capacitance is increased by only 2–3 μF when $T_{\rm c}$ is increased by 30 °C. While the perturbations of the estimated C and $R_{\rm c}$ are 9 μF and 0.4 Ω with increasing $T_{\rm c}$ by 30 °C, respectively. However, this perturbation is still within the perturbation of the results in Fig. 10. Thus, the proposed cluster-data based method is still effective when the $T_{\rm c}$ of capacitor is changed.

F. MOSFET Degradation Monitoring

Conventionally, the ON-state resistance of MOSFET $R_{\rm dson}$ is effective in indicating its health condition. As discussed before, the estimated $R_{\rm L}$ and $R_{\rm dson}$ fluctuate in a large range. Therefore,

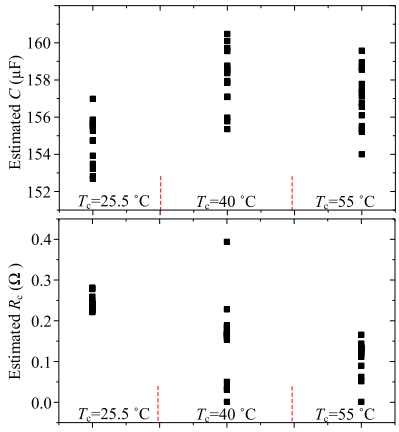

Fig. 11. Estimated C and R_c when case temperature T_c is changed (case 6).

it is challenging to monitor the degradation of MOSFET by using the estimated $R_{\rm dson}$ directly. However, according to Fig. 2 and (1), it can be seen that $R_{\rm L}$ and $R_{\rm dson}$ have almost same impact on $v_{\rm o}$ and $i_{\rm L}$, which means distinguishing them is virtually impossible. To overcome this challenge, a new equivalent period average resistance is proposed and defined as below to represent both $R_{\rm L}$ and $R_{\rm dson}$ in this article:

$$R_{\rm avg} = R_{\rm L} + DR_{\rm dson}. \tag{15}$$

D can be obtained from the digital twin controller. $R_{\rm dson}$ works only when the MOSFET is turned ON, while $R_{\rm L}$ works in the whole switching period. Therefore, $R_{\rm L}$ and $R_{\rm dson}$ can be represented by an equivalent average resistance $R_{\rm avg}$. To verify this, the estimated $R_{\rm L}$ and $R_{\rm dson}$ are illustrated in Fig. 12(a) and (b), respectively, which shows they fluctuate within a relative large range, but $R_{\rm avg}$ keeps stable within a relative small range, as shown in Fig. 12(c). In addition, it is worth to mentioning that inductor usually possesses very stable characteristics and its parameters are not changed during operation. Thus, $R_{\rm avg}$ enables the proposed method to monitor the degradation of MOSFET.

An accelerated power cycling platform was designed in [45], where $R_{\rm dson}$ is used as the indicator of aging process. In this article, $\Delta R_{\rm dson}$ reaches higher value before the MOSFETs actually fail (0.3–1 Ω). Usually, package related aging may only causes 5%–20% increase in $R_{\rm dson}$. Such higher increase shown in [45] is mainly due to the degradation of MOSFET chip as the significantly decrease of the gate-oxide capacitance, which results in the driving voltage drops lower than normal value. Then, the MOSFET operating in saturation region exhibits high output impedance [24]. Based on this, five MOSFETs with different $R_{\rm dson}$ are chosen in this article to simulate the degradation of MOSFET as listed in Table V (the $R_{\rm dson}$ of those MOSFETs are measured experimentally offline). The case temperature of the

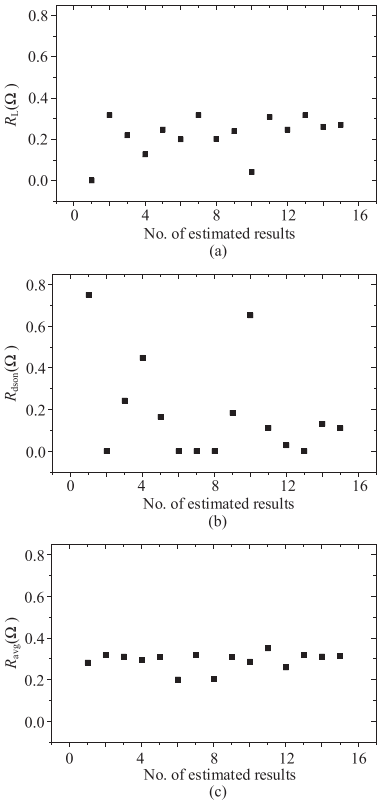

Fig. 12. Estimated parasitic resistances (the proposed calculation procedure is repeated for 15 times): (a) the parasitic resistance of inductor; (b) the ON-state resistance of MOSFET; (c) defined equivalent average resistance of $R_{\rm L}$ and $R_{\rm dson}$ by using equation (15).

MOSFETs in each operational condition is recorded as listed in Table VI, showing higher temperature with higher ON-state resistance, current, and duty cycle, such as those MOSFETs operating in case3. Then, the estimated results over different operational cases and MOSFETs are indicated with different colors and from M1 to M5, respectively, as shown in Fig. 13. The estimated L, C, and R_c are immune from the simulated degradation of MOSFET. While the estimated $R_{\rm avg}$ shows increasing trend from M1 to M5. Especially the relative large increment in case3 and case4 due to the higher temperature, which proves the ability of the proposed method in detecting the degradation progress of the MOSFET in a buck converter.

G. Simultaneous Degradation Test

In practice, the degradation of capacitor and MOSFET may happen simultaneously. Therefore, it is necessary to verify the

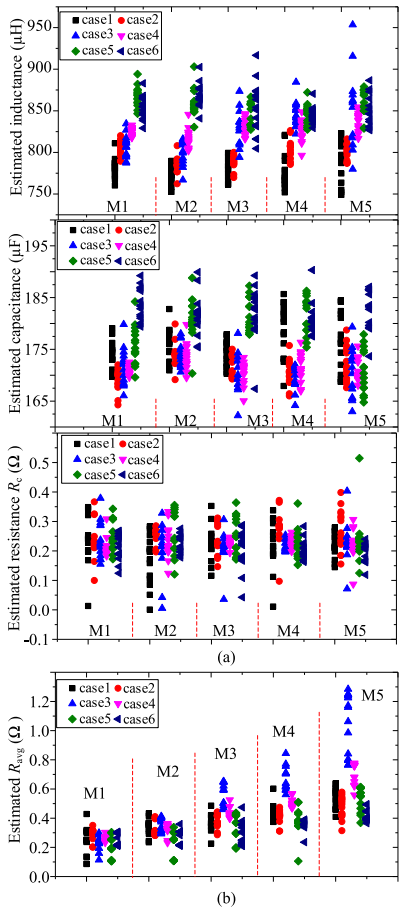

Fig. 13. Estimated results over different operational cases and simulated degradation levels of MOSFET (here the applied capacitor is 165 μF(C1). case 1-6 are described in Table III, the case temperature of MOSFETs are listed in Table VI, M1–M5 are described in Table V): (a) L, C, and R_c; (b) R_{avg}.

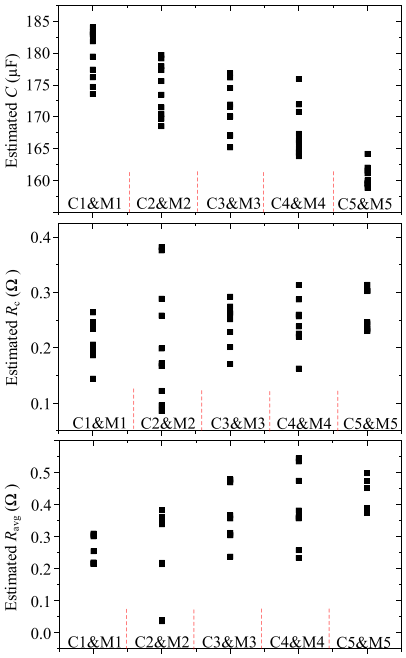

Fig. 14. Estimated C, R_c and R_{avg} when capacitor and MOSFET are degraded simultaneously (case6) (M1–M5 are described in Table. V, C1–C5 are described in Table IV).

ability of the proposed method in monitoring the simultaneous degradation among these two key components. The estimated results are shown in Fig. 14, which proves the degradation trend of capacitor and MOSFET can be identified simultaneously by the proposed method.

H. Data Analysis

Due to the variations from the measurement errors, the temperature factors, and the workloads, the component parameters are obtained as a data cluster. To provide an evaluation standard, the boxplot technique is applied to derive the statistical measures of the data cluster so as to quantify the degradation levels. Boxplot technique is an effective method for the representation of data structure by calculating the statistics including median and quantiles, based on which the degradation trend can be clearly determined. With the data clusters in Fig. 10(d), (e), and 13(b), the respective boxplots of these clusters are calculated and shown in Figs. 15 and 16. As can be seen, there is a clear degradation trend according to the medians of the data cluster, and the details are given in Table VII. Those outliers are those data is out of 95% confidence interval and the existing of those outliers is reasonable due to the experimental noise. The more narrower box means the data are more concentrated. Specifically, the estimated medians of C and R_c are decreased by 9.7% and increased by 21%, respectively, when the capacitor is degraded by 8.8%. Meanwhile, the median of R_{avg} is increased from 0.243 Ω to 0.561 Ω when the R_{dson} is manually increased from 0.11 Ω to 0.75 Ω. Although the estimated parameters are not quite close to the real ones, the relative degradation change of each parameter can be identified, which demonstrates that the proposed method is effective in monitoring the degradation level of the key components in buck converters.

The buck converter is considered as the simplest topology to prove the proposed concept of this article. Nevertheless, it represents the features of many other buck-type converters and voltage-source inverters. Therefore, the applicability of the same

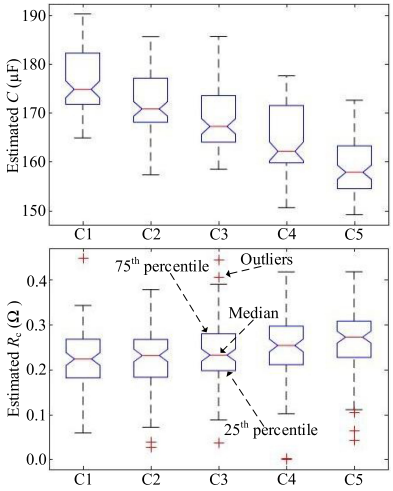

Fig. 15. Probability density distribution of the estimated C and R_c of all obtained data from case 1 to case 7 (C1–C5 are described in Table IV).

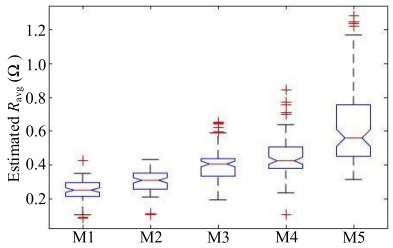

Fig. 16. Probability density distribution of the estimated $R_{\rm avg}$ of all obtained data from case 1 to case 7 (M1–M5 are described in Table V).

TABLE VII
OBTAINED MEDIAN VALUE OF THE IDENTIFIED PARAMETERS AFTER DATA PROCESS

Median (Cap)	C1	C2	C3	C4	C5
C (μF)	174.9	170.9	167.3	162.2	158
R_c (mΩ)	224	232	233	254	273
Median (MOS)	M1	M2	M3	M4	M5
$R_{\rm avg}$ (mΩ)	252	310	407	426	561

concept for single-phase inverters and three-phase inverters can also be expected in the future. Even though, various challenges still need to be further solved.

V. CONCLUSION

In this article, a digital twin concept-based condition monitoring method is proposed and verified through a buck converter case study. The experimental tests are performed to verify its feasibility and the results show that the digital twin of the buck converter can achieve similar output waveforms (inductor current $i_{\rm L}$ and output voltage $v_{\rm o}$) with the physical buck converter. Then, practical considerations are discussed (impact of sampling rate, different operation conditions, temperature and the uncertainty caused by errors). To avoid calibrating the relationship between the health indicator and their impact factors, a cluster-data based method is used in this article. Finally, the capability of monitoring the degradation of key components (capacitor and MOSFET) in converter is verified experimentally. When the capacitance is decreased by 2.2% for each step, the identified cluster of capacitances are able to indicate the degradation process. For MOSFET, the identified $R_{\rm dson}$ cannot be used directly to indicate the degradation of MOSFET. To overcome this, a new equivalent resistance between $R_{\rm L}$ and $R_{\rm dson}$ are defined in this article as $R_{\rm avg}$. Similarly, by calculating a cluster of this new defined resistance, the increase of $R_{\rm dson}$ can be identified. Finally, the probability density distribution-based data process method is used to achieve the characteristic value of each cluster-data which can be used as the final degradation level indicator. For implementation, three signals need to be measured from the physical buck converter by using regular sensors: inductor current, output voltage and input voltage. In addition, dynamic waveforms are prerequisite for this method, which can be achieved from the load change events, input voltage change transient, start-up and shut-down transient.

In conclusion, the feasibility and effectiveness of the proposed method in monitoring the degradation level of capacitor and MOSFET are proved experimentally and practical issues are also considered. Compare to conventional methods, the proposed method provides a feasible and practical solution for condition monitoring of power converter with superiorities in noninvasive, calibration-free, and without additional hardware circuits.

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Journal publication 2

Converter-level On-state Voltage Measurement Method for Power Semiconductor Devices

Y. Peng, Y. Shen, and H. Wang

The paper has been accepted in the
IEEE Trans. Power Electron., 2020.

The layout has been revised.

Letter

A Converter-Level ON-State Voltage Measurement Method for Power Semiconductor Devices

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***Abstract*—This letter proposes a converter-level method for measuring the ON-state voltages of all power semiconductors in a single-phase inverter by using a single circuit only. The proposed circuit distinguishes itself by connecting to the middle point of each phase leg, instead of the two power terminals of individual devices as conventional methods do. It has the advantages of reduced circuit complexity, size, cost, and ease of connection. The principle and theoretical analysis of the proposed converter-level method are discussed. A case study on a single-phase full-bridge inverter is demonstrated to prove the concept.**

***Index Terms*—Converter level, ON-state voltage, power semiconductor, power converter.**

I. Introduction

THE ON-state voltages of power semiconductor devices are the most widely reported temperature sensitive electrical parameters [1] or health indicator [2], including the $V_{\mathrm{CE,sat}}$ of the IGBT, V_{DSon} of MOSFET, and V_{F} of the diode. Many efforts have been made to measuring this low voltage (i.e., in the range from subvolt to few volts) at millivolt resolution from the OFF-state voltage up to few kilovolts.

A review of the hardware-based ON-state voltage measurement methods has been included in [3], which summarizes the low-frequency measurement through relay-switch/Zener-diode [4], and the high-frequency measurement through fast recovery diode/MOSFET [2], [5], [6]. These methods can measure the voltage drop across the two power terminals of a single device, meanwhile, block the high voltage when the device is in the OFF-state. Nevertheless, the common practical challenges of these methods are as follows.

1) It is of high complexity and cost as each switching device needs a measurement circuit.
2) It requires to connect the power terminals of individual switches as shown in Fig. 1, which may be not always feasible due to the accessibility and safety concern for practical converters.
3) It has multiple floating grounds, i.e., the middle point of each phase leg, if it requires to measure the ON-state voltages of all devices in a single-phase or three-phase inverter.

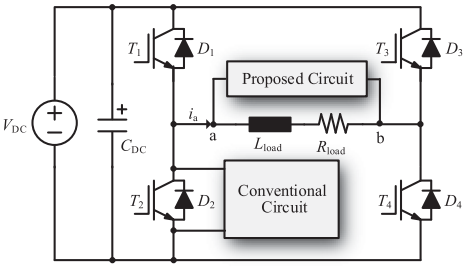

Fig. 1. Comparison of the proposed ON-state voltage measurement method and conventional methods in terms of connection points to an inverter.

Another category of method is algorithm based without additional hardware, such as the digital-twin-based approach applied for a buck dc–dc converter in [7]. However, this method is highly dependent on the architecture of the power converters in terms of topology and control. The complexity in modeling and computation burden is likely to increase for converters with more components, such as a single-phase inverter or three-phase inverter system.

To address the aforementioned challenges, this letter proposes a measurement circuit connected to the middle point of phase legs as shown in Fig. 1. By leveraging the rich information of the single-phase inverter modulation, the voltage across the inverter output terminals contains the ON-stage voltage information of all the IGBT switches T_1–T_4, and diodes D_1–D_4. The main features of the proposed method are as follows.

1) It uses one circuit only to measure the ON-state voltages (e.g., $V_{\mathrm{CE,sat}}$ of IGBT and V_{F} of diode) of all power semiconductor switches in the inverter, leading to reduced complexity, size, and cost.
2) It has better accessibility because of converter-level implementation.

Manuscript received May 12, 2020; revised June 13, 2020; accepted July 6, 2020. Date of publication July 20, 2020; date of current version September 22, 2020. This work was supported by the Innovation Fund Denmark through the Advanced Power Electronic Technology and Tools (APETT) under Project No. 6154-00010B. *(Corresponding author: Yingzhou Peng.)*

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Color versions of one or more of the figures in this letter are available online at https://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2020.3009934

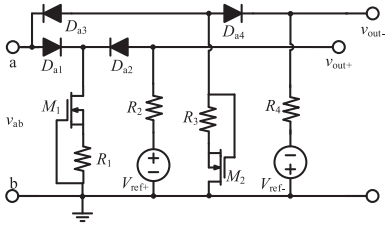

Fig. 2. Topology of the proposed ON-state voltage measurement circuit.

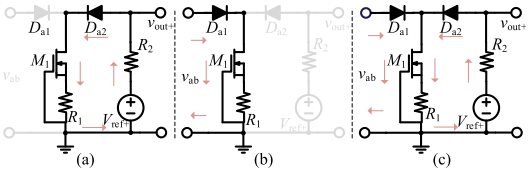

Fig. 3. Operation modes of half of the proposed measurement circuit (the second half is similar in operation modes). (a) When v_{ab} is negative voltage. (b) When v_{ab} is higher than V_{ref+}. (c) When v_{ab} is between zero and V_{ref+}.

3) The isolation stage with the proposed circuit can be simplified as it has one reference ground and two output signals only for a single-phase inverter monitoring.

Therefore, a simpler galvanic isolation from the inverter stage can be implemented compared to component-level methods [4], by adding an isolation stage at the output side of the proposed measurement circuit. The initial concept of the study has been presented in a previous conference publication [8]. In this letter, the circuit implementation and the inverter demonstrator have been redesigned with improved performance in terms of noise, response speed, setting time, and accuracy level. The theoretical analyses of the limitations and applications are added. The remainder of this letter is organized as follows. Section II presents the principle of the proposed method with a case study. Section III gives the proof-of-concept of the method based on experimental testing. Finally, Section IV concludes this letter.

II. Concept and Implementation of the Measurement Circuit

A. Operation Principle of the Proposed Circuit

The proposed converter-level ON-state voltage measurement circuit is shown in Fig. 2. There is one reference ground only in the circuit, which simplifies the implementation. The circuit includes two symmetric parts with the ability to extract ON-state voltages from the bipolar v_{ab}. The first part is composed of a signal depletion MOSFET M_1, fast-recovery diodes D_{a1} and D_{a2}, and a reference voltage source V_{ref+}. The function of this part is to block any negative voltage and high positive voltage from v_{ab}, and to pass low positive voltage only. The second part composed of M_2, D_{a3}, D_{a4}, and V_{ref-}, has similar function, except for that it is used to block any positive voltage and high negative voltage, and pass low negative voltage from v_{ab}. If the gate-source voltage of M_1, for example, is zero, it is in ON-state. If there is current flowing through M_1, the voltage drop in R_1 makes M_1 operates in linear mode. In addition, due to the negligible parasitic inductances, capacitances, and operation current (e.g., 1–4 mA in this case study) of the proposed circuit, the operation of the inverter is not impacted.

The operation modes of the first part are given in Fig. 3 and discussed as follows.

1) *Model 1 [see Fig. 3(a)]:* If v_{ab} is negative, D_{a1} is blocked, D_{a2} is conducted, and M_1 is in the linear mode. The positive output v_{out+} is

$$v_{out+} = \frac{R_1}{R_1 + R_2}\left(V_{ref+} - V_{Da2} - V_{M1}\right) + V_{Da2} + V_{M1} \tag{1}$$

R_1 is selected with a much smaller resistance than R_2, leading to a small v_{out+} (e.g., 1 V) at this model.

2) *Model 2 [see Fig. 3(b)]:* If v_{ab} is positively higher than V_{ref+}, D_{a1} is conducted, D_{a2} is blocked, and M_1 is in the linear mode. Then, v_{out+} equals to the reference voltage V_{ref+}.

$$v_{out+} = V_{ref+}. \tag{2}$$

3) *Model 3 [see Fig. 3(c)]:* If v_{ab} is within 0 and V_{ref+}, both D_{a1} and D_{a2} are conducted, M_1 is in linear mode as shown in Fig. 3(c). It is noted that the voltage across M_1 and R_1 (V_{M1}+V_{R1}) must be as low as possible to make sure D_{a1} is conducted at this model, which is controlled by adjusting R_1 and R_2. Then, v_{out+} can be described as

$$v_{out+} = v_{ab} - V_{Da1} + V_{Da2}. \tag{3}$$

In practice, V_{Da1} and V_{Da2} can be canceled with each other substantially under even temperature [6]. Thus, it is reasonable to assume that v_{out+} is equal to v_{ab}. In addition, the impact of the used resistances caused by different temperatures can be neglected due to their negligible temperature coefficient (e.g., less than $\pm 100 \mathrm{ppm/K}$). Likewise, the second part of the circuit can measure the negative low voltage from v_{ab}. In conclusion, when the input signal v_{ab} is within the range of V_{ref-} and V_{ref+}, the output voltage of the proposed circuit equals to v_{ab}. Otherwise, the output voltage of the proposed circuit is clamped to V_{ref-} or V_{ref+}. It is worth mentioning that the isolation is a common requirement for both component-level methods and proposed method in practical applications. In this letter, since the focus is to present the proof-of-concept of the proposed method, the isolation implementation is not demonstrated.

B. Case Study of a Single-Phase Full-Bridge Inverter

The output voltage between the middle points of the phase legs varies with modulation schemes, as shown in Fig. 4 [9]. Among them, the proposed method does not apply to the inverter with bipolar modulation only due to the absence of current freewheeling states. Nevertheless, this modulation is relatively less used compared to the other two due to lower efficiency and higher filter requirements [9]. An alternative solution for

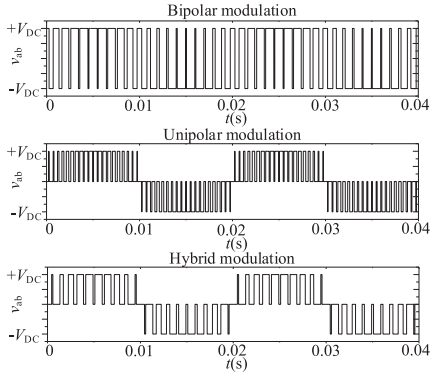

Fig. 4. Output voltage waveforms of a full-bridge inverter with different modulations.

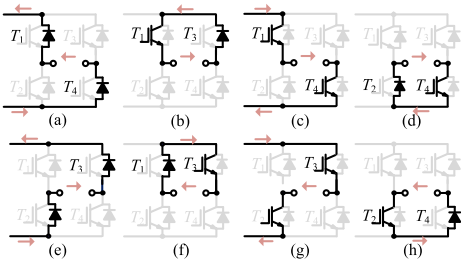

Fig. 5. Operation states of the full-bridge inverter with unipolar SPWM modulation.

TABLE I
OPERATION STATES OF CONVERTER WITH UNIPOLAR SPWM MODULATION AND CORRESPONDING OUTPUT VOLTAGES OF THE PROPOSED CIRCUIT

States	v_{ab}	v_{out+}	v_{out-}
(a)	V_{DC}+V_{F1}+V_{F4}	V_{ref+}	-1 V
(b)	-$V_{CE,sat1}$-V_{F3}	+1 V	-$V_{CE,sat1}$-V_{F3}
(c)	V_{DC}-$V_{CE,sat1}$+$V_{CE,sat4}$	V_{ref+}	-1 V
(d)	-$V_{CE,sat4}$-V_{F2}	+1 V	-$V_{CE,sat4}$-V_{F2}
(e)	-V_{DC}+V_{F3}+V_{F2}	+1 V	V_{ref-}
(f)	$V_{CE,sat3}$+V_{F1}	$V_{CE,sat3}$+V_{F1}	-1 V
(g)	-V_{DC}+$V_{CE,sat3}$+$V_{CE,sat2}$	+1 V	V_{ref-}
(h)	$V_{CE,sat2}$+V_{F4}	$V_{CE,sat2}$+V_{F4}	-1 V

single-phase inverters with bipolar SPWM is to intentionally operate it under unipolar or hybrid modulation for short period of time for the ON-state voltage measurement purpose. Therefore, from this perspective, the proposed method has a wide range of applications.

The corresponding eight operation states of the inverter with unipolar SPWM modulation are shown in Fig. 5. Table I gives the v_{ab} for each operation state. V_{DC} is the dc-link voltage, $V_{CE,sat1}$–$V_{CE,sat4}$ denote the ON-state voltage of T_1–T_4, respectively, and V_{F1}–V_{F4} denote the forward voltage of D_1–D_4, respectively.

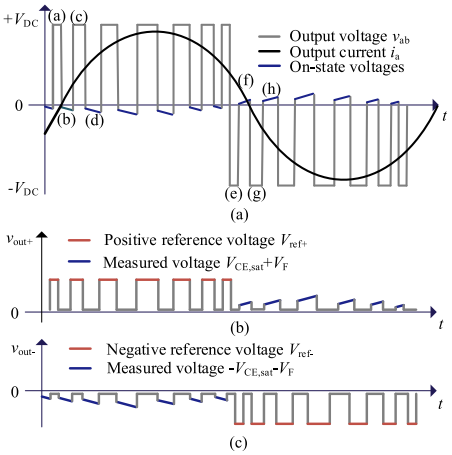

Fig. 6. Output voltage waveforms of the full-bridge inverter v_{ab} with unipolar SPWM modulation.

It can be seen from Table I that the critical indicators $V_{CE,sat}$ and V_F of all IGBTs and diodes are included in v_{ab}. Then, the v_{ab} waveform over one fundamental period is drawn as shown in Fig. 6(a). With the proposed circuit, the high dc-link voltages in v_{ab} are clamped to the positive and negative reference voltages, respectively, whereas the sum of $V_{CE,sat}$ and V_F is retained, as shown in Fig. 6(b) and (c). The specifications of v_{ab}, v_{out+}, and v_{out-} are listed in Table I. Then, the obtained sum of the ON-state voltage of one IGBT and one diode could be useful for health monitoring. As the increase of the sum value or its change rate under a given condition indicates at least one of them degrades. In practice, any one or more of the IGBTs and diodes in one power module reaches the end-of-life implies the failure of the whole power module. Therefore, it is not necessary to separate the ON-state voltage of the IGBT and the diode for health monitoring.

III. EXPERIMENTAL VERIFICATION

A full-bridge inverter is built with a 400-V dc-link voltage and 10-kHz switching frequency. A prototype of the proposed measurement circuit is developed and connected with the output terminals of the inverter, as shown in Fig. 7. The rating of the used MOSFETs is 600 V/ 17 mA. R_1, R_3, and R_2, R_4 are SMD resistor with 200 Ω and 6.8 kΩ, respectively.

A commercial component-level ON-state voltage measurement product is used for comparison purpose [10]. Fig. 8(a) compares the measured $V_{CE,sat2}$, indicating that the proposed circuit has a comparable accuracy level with this product. Fig. 8(b) gives the dynamic response of the proposed circuit with a step change of v_{ab} from −7.5 to 6.5 V. When the input voltage is negative, the circuit operates in Model 1, as shown in Fig. 3(a), and v_{out+} is 1 V. Once the input voltage increases to 6.5 V, the output voltage follows it with a fast dynamic response.

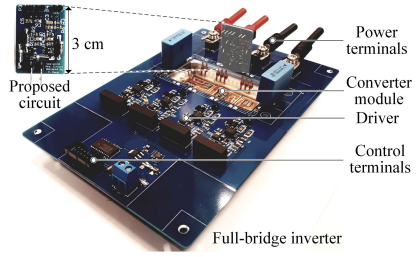

Fig. 7. Experimental prototypes of the full-bridge inverter and the proposed circuit.

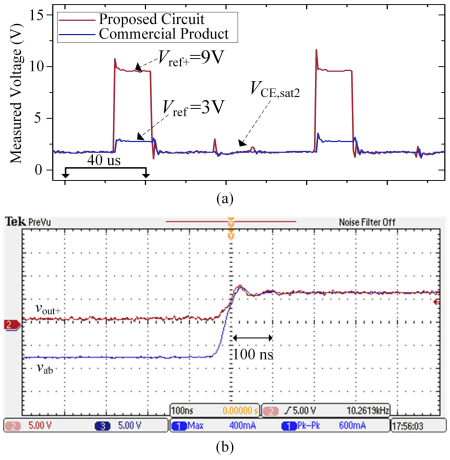

Fig. 8. Performance testing of the proposed circuit. (a) Comparison with a commercial product [10]. (b) Dynamic response with a step change of v_{ab} from −7.5 to 6.5 V.

Fig. 9(a) shows the measured waveforms of v_{ab}, v_{out+}, and v_{out-}. It demonstrates that both of the high positive and negative voltages of v_{ab} are clamped to the reference voltages, while the $V_{CE,sat}$ and V_F are detectable. Fig. 9(b) and (c) shows the zoom-in waveforms of v_{out+} and v_{out-}, respectively. The sum of the ON-state voltage of one IGBT and the corresponding diode shown in Table 1 can be obtained. The voltage spikes in Fig. 9 are mainly attributed to the parasitic inductances of the module terminals, bus bar, and the connecting wires between the inverter and the proposed circuit during the current commutation transient. They can be reduced by well designing the inverter and shorting the connecting wires, and do not impact the accuracy as only the steady value is required during the data analysis step.

Only one point of each pulse in Fig. 9(b) and (c) is extracted with a sampling frequency double of the switching frequency as shown in Fig. 10. The measured ON-state voltages change with the current stresses within one fundamental period, which proves that the proposed circuit can sense the change of $V_{CE,sat}$ and V_F. Among them, $V_{CE,sat3}$+V_{F1} and $V_{CE,sat2}$+V_{F4} are included in

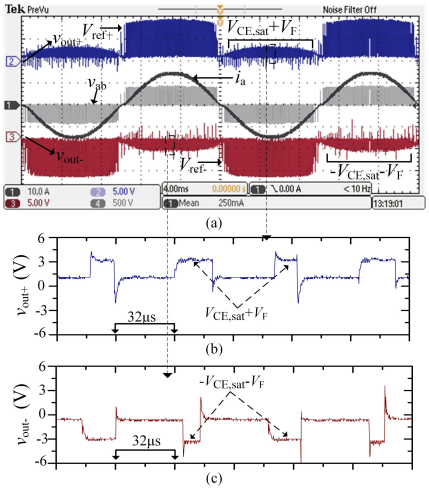

Fig. 9. Experimental results. (a) Waveforms of the full-bridge inverter and the proposed measurement circuit. (b) Zoom-in v_{out+}. (c) Zoom-in v_{out-}.

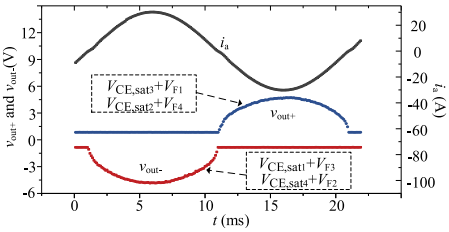

Fig. 10. Extracted ON-state voltages during one fundamental period.

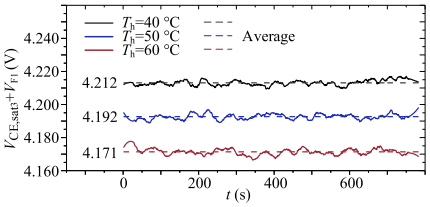

Fig. 11. Extracted $V_{CE,sat3}$+V_{F1} when the instantaneous output current of inverter is within −20.5 and −19.5 A at three heatsink temperature levels.

v_{out+}, $V_{CE,sat1}$+V_{F3}, and $V_{CE,sat4}$+V_{F2} are included in v_{out-}. They can be separated based on the operational states as listed in Table I. The $V_{CE,sat3}$+V_{F1} is sampled one time per fundamental period when the output current i_a is within −20.5 and −19.5 A at three different levels of heatsink temperature T_h. Then, the sampled results over 1 s are averaged as shown in Fig. 11, indicating the proposed method can detect the change of ON-state voltage by 2 mV/°C.

IV. Conclusion

In this letter, the output voltage $v_{\rm ab}$ of a single-phase inverter is analyzed with different modulations and it is found that for the single-phase inverters with unipolar and hybrid modulations, the ON-state voltages of all power semiconductors appear at $v_{\rm ab}$ during the current freewheeling states. Therefore, a converter-level circuit is proposed to extract the ON-state voltages of all power semiconductors from $v_{\rm ab}$, which is verified theoretically and experimentally in this letter. This circuit achieves reduced complexity, size, cost, easy connection, and noninvasive measurement compared to existing solutions. In addition, the proposed circuit can follow the input voltage with a fast dynamic response. In principle, the proposed method is applicable to many converters composed of one or more phase legs.

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Journal publication 3

A Self-Power Solution for the On-State Voltage Monitoring Circuit of Power Semiconductors

Y. Peng, H. Wang

The paper is under review
IEEE Trans. Power Electron., 2020.

The layout has been revised.

A Self-Power Method for A Converter-level On-state Voltage Measurement Concept

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***Abstract*—This paper discloses part of an invention on plug-and-play converter-level on-state voltage measurement methods for power semiconductor devices. To exclude the external power supply required in on-state voltage measurement circuits, a self-power solution is proposed to provide the required bidirectional low-voltage power sources. The application of the measurement circuit with the proposed self-power solution is demonstrated for a single-switch, a single-phase inverter, and a three-phase inverter.**

***Index Terms*—Power semiconductor, converter level, reliability, condition monitoring.**

I. Introduction

On-state voltage in this paper refers to the voltage stress of a power semiconductor during its fully-conducted operation mode. For example, the $V_{\mathrm{CE,sat}}$ of an IGBT, $V_{\mathrm{ds,on}}$ of a MOSFET, and V_{F} of a diode [1]–[3]. It is a parameter widely used for degradation prediction, junction temperature estimation, and protection implementation of power semiconductor devices [3]–[6]. On-state voltage typically ranges from sub-volt to few volts. It needs to be measured from signals including also the off-state voltage stresses up to the rated voltage of the semiconductor of interest. Cost, complexity, and accuracy are three important aspects to be considered for the measurement solutions.

Compared to many other gate-related parameters [7]–[15], On-state voltage has the following outstanding features: 1) it is noninvasive to the gate driver; 2) it has relative low-frequency, which simplifies the measurement significantly; 3) it is relevant to the three typical failure mechanisms (e.g., bond-wires lift-off, solder layer degradation, and gate-oxide layer wear-out) of power devices [3], [6], [16].

Various component-level solutions are proposed in the literature [3]–[5], [17]–[19]. Nevertheless, they still reveal limited performances: 1) they are component-level circuit and require one isolated power supply for each power device or phase-leg, which leads to the increased circuit complexity, size, cost, and complex connection to monitor a three-phase converter for example; 2) they are connected to the two power-terminals of individual power switch, which requires multiple connecting terminals for the application of three-phase converters; 3) they require one reference ground for each phase-leg, which makes the data sampling equipment more complicated. Recently, a converter-level measurement circuit is presented in [20] for a single-phase inverter application. The method has the advantage of significantly reduced cost and complexity. Nevertheless, the reported converter-level method in [20] and existing component-level methods [3]–[5], [17]–[19] require the power supply for generating low-voltage references. Two practical issues exist: 1) the isolated power supply is the most expensive component in the circuit proposed in both component-level and converter-level methods. 2) even though the converter-level method enables a better accessibility to existing power electronic converters, it has not yet fully decoupled from the converters to be measured due to the power supply requirement. This paper aims to realize a plug-and-play converter-level on-state voltage measurement solution with further reduced cost by a self-power method.

Different self-power solutions are presented for other applications [21]–[23]. However, these methods require high-voltage capacitor to withstand most part of the DC-link voltage when the MOSFET/IGBT is in off-state, and an inductor-capacitor energy storage. Another self-power circuit is proposed in [24] to supply gate driver, which takes the rising DC-link voltage during the turn-off transient of MOSFET/IGBT to charge the energy-storage capacitor and needs a specific design for the selected MOSFET, polarization diode, and avalanche diode to achieve the required performance. It is modified in [25] by replacing the polarization diode with a high-voltage resistor to avoid complex design. In addition, the transformer/coupled-inductor is used to extract the required power supply in different converters, e.g., power factor correction (PFC) converter and modular multilevel converter (MMC) [26]–[28]. However, the transform/coupled-inductor is usually bulky. Besides, all of the above solutions are not able to withstand bi-directional high-voltage and provide bi-directional reference voltage. Therefore, a suitable self-power solution for the on-state voltage measurement circuits is not investigated yet and still missing.

This paper discloses one of the methods filed in the invention [29]. The contributions of the presented study are: 1) a self-power method is proposed to enable a plug-and-play solution; and 2) the converter-level on-state voltage measurement concept in [20] is extended to a three-phase inverter application, which represents a wider range of relevant industry applications. Furthermore, its design principle is elaborated to achieve high-accuracy and fast-response. In Section II, the proposed self-power circuit is introduced firstly. Subsequently, the application of the converter-level on-state voltage measurement circuit with the proposed self-power solution in a three-phase inverter is discussed in Section III. The hardware realization, circuit design principle, and experimental verification are, thereafter, presented in Section

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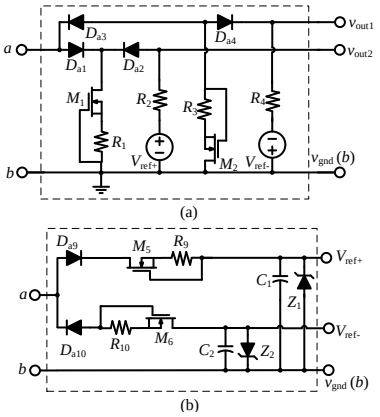

Fig. 1. Topology of the proposed health indicator monitoring circuit: (a) on-state voltage monitoring circuit; (b) self-power circuit to replace the voltage sources $V_{\mathrm{ref}+}$ and $V_{\mathrm{ref}-}$ shown in Fig.1(a) .

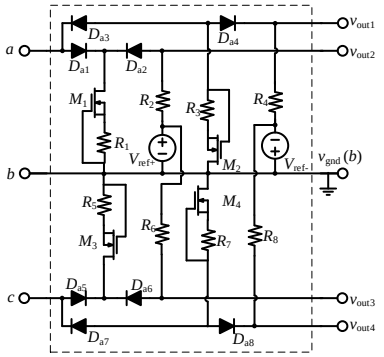

Fig. 2. Topology of the proposed on-state voltage measurement circuit for three-phase inverter.

IV. Section V concludes this paper with an overall summary.

II. Proposed self-power circuit for on-state voltage monitoring circuit

A. Configuration of the converter-level on-state voltage measurement circuit

The basic configuration of the converter-level on-state voltage measurement circuit is depicted in Fig.1(a). $D_{\mathrm{a}1}$-$D_{\mathrm{a}4}$ are normal diode. M_1 and M_2 are signal N-channel depletion MOSFET. $V_{\mathrm{ref}+}$ and $V_{\mathrm{ref}-}$ are the bidirectional reference voltages. The basic function of this circuit is elaborated in Table I, where $V_{\mathrm{Da}1}$-$V_{\mathrm{Da}4}$ are the forward voltage of $D_{\mathrm{a}1}$-$D_{\mathrm{a}4}$, $V_{\mathrm{M}1}$ and $V_{\mathrm{M}2}$ are the voltage across M_1 and M_2, respectively. The detail of the operation principle can be referred to [20].

B. Configuration of the proposed self-power circuit

The proposed self-power circuit is depicted in Fig.1(b). It can replace the external power supply and provide the bi-directional reference voltages. More importantly, it does not affect the normal operation of the power converter.

$D_{\mathrm{a}9}$ and $D_{\mathrm{a}10}$ are normal diode, Z_1 and Z_2 are zener diode with 6.2 V zener voltage in this case study, M_5 and M_6 are depletion MOSFET. Based on this, when the input voltage of the self-power circuit is positive, $D_{\mathrm{a}9}$ is conducted and $D_{\mathrm{a}10}$ is blocked. M_5 operates in the linear mode due to the voltage drop in R_9 and withstands the high-voltage. Then, C_1 is charged until its voltage reaches at 6.2 V. Likewise, when the input voltage is negative, C_2 starts to charge until its voltage reaches at -6.2 V. Accordingly, the bidirectional reference voltage $\pm$6.2 V is obtained. Moreover, the proposed on-state voltage measurement circuit and self-power supply can share the common ground, which excludes the electrical isolation. It is noted that R_9 (R_{10}) are used to control the impedance of M_5 (M_6) and the charging current of C_1 (C_2). The higher R_9 is selected, the less charging current and the higher impedance of M_5 can be induced. Then, the charging time is increased, and further the reference voltage may not be able to reach the preset zener voltage. However, if the R_9 is too low, the higher current can cause the power losses of M_5 exceeds its maximum limitation.

III. Application of the proposed self-powered on-state voltage measurement circuit

A. Implementation

1) Three-phase inverter: The configuration depicted in Fig.1(a) is designed for single-phase converters as discussed in [20], which is replicated partially (the reference voltage can be shared due to the common ground) for three-phase inverter as shown in Fig.2.

Fig.3(a) shows that the measurement circuit is connected to the three-phase inverter through the three output terminals, which achieves plug-and-play and shows non-invasive to the converter. Also, the number of input and output terminals is halved from 16 in conventional methods (including 5 input terminals, 2 power supply terminals, and 9 output terminals) for three-phase inverter application.

To make it simple and understandable, the operation modes of three-phase inverter are analyzed in terms of phase-legs a and b (phase c and b can be derived similarly). According to the direction of phase current, the on-off state of switches, and the SPWM modulation, the operation modes are drew in Fig.3(b). Based on this, one of the output line voltages of the inverter, v_{ab} for example, presents different values in different modes, as listed in Table II. Among these modes, the v_{ab} equals to the sum of the on-state voltage of one IGBT and one diode in current-freewheeling (CFW) modes, such as in the operation mode (B), (D), (H), and (G). It should be noted that the CFW modes are existed in converters with both SPWM and SVPWM modulations as shown in Fig.4, showing that the converter operates at CFW mode when the triangular carrier signal arrives at either top or bottom value.

$V_{\mathrm{CE,sat1}} - V_{\mathrm{CE,sat4}}$ are the on-state voltages of $T_1 - T_4$; $V_{\mathrm{F1}} - V_{\mathrm{F4}}$ are the forward voltages of freewheeling diodes

TABLE I
BASIC FUNCTION OF THE PROPOSED ON-STATE VOLTAGE MONITORING CIRCUIT.

$v_{\rm ab}$	$v_{\rm out1}$	$v_{\rm out2}$
$v_{\rm ab} > V_{ref+}$	$\frac{R_4}{R_4+R_3}(V_{\rm ref-}+V_{\rm Da4}+V_{M2})+V_{\rm ref-}$	$V_{\rm ref+}$
$0 \le v_{\rm ab} \le V_{\rm ref+}$	$\frac{R_4}{R_4+R_3}(V_{\rm ref-}+V_{\rm Da4}+V_{\rm M2})+V_{\rm ref-}$	$v_{\rm ab}-V_{\rm Da1}+V_{\rm Da2}\approx v_{\rm ab}$
$V_{\rm ref-} \le v_{\rm ab} \le 0$	$v_{\rm ab}+V_{\rm Da3}-V_{\rm Da4}\approx v_{\rm ab}$	$V_{\rm ref+}-\frac{R_2}{R_2+R_1}(V_{\rm ref+}-V_{\rm Da2}-V_{M1})$
$v_{\rm ab} < V_{\rm ref-}$	$V_{\rm ref-}$	$V_{\rm ref+}-\frac{R_2}{R_2+R_1}(V_{\rm ref+}-V_{\rm Da2}-V_{\rm M1})$

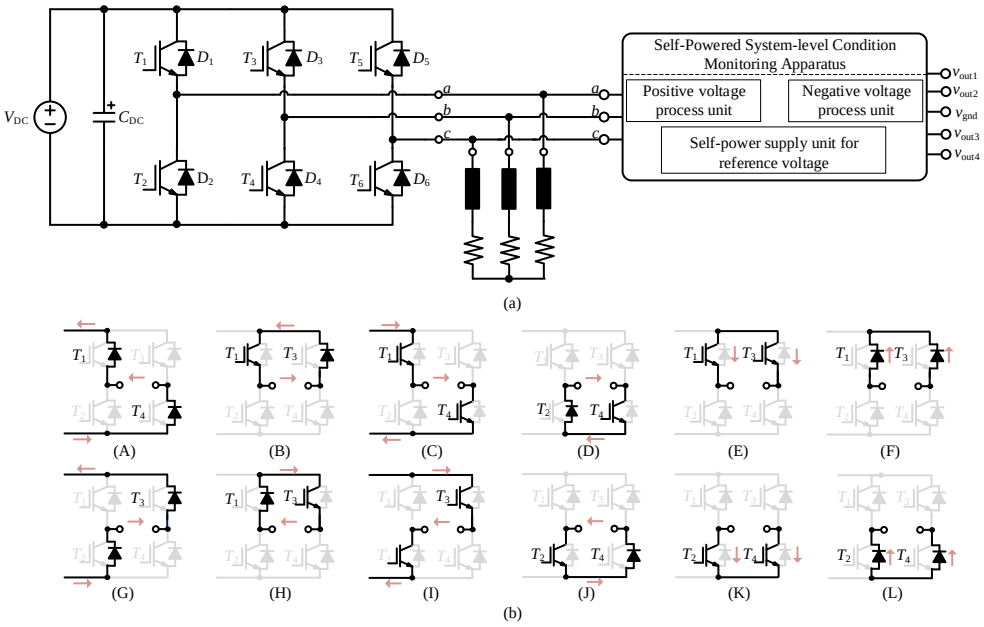

Fig. 3. Implementation of the proposed circuit in three-phase inverter: (a) connection to the three-phase inverter; (b) operation models of phase-legs a and b in the three-phase inverter with SPWM modulation.

TABLE II
VALUE OF THE OUTPUT VOLTAGE OF THE THREE-PHASE INVERTER IN DIFFERENT OPERATION STATES

Operation states	Output voltage $v_{\rm ab}$
A	$V_{\rm DC}+V_{\rm F1}+V_{\rm F4}$
B	$-V_{\rm CE,sat1}-V_{\rm F3}$
C	$V_{\rm DC}-V_{\rm CE,sat1}-V_{\rm CE,sat4}$
D	$-V_{\rm CE,sat4}-V_{\rm F2}$
E	$V_{\rm CE,sat3}-V_{\rm CE,sat1}$
F	$V_{\rm F1}-V_{\rm F3}$
G	$-V_{\rm DC}-V_{\rm F3}-V_{\rm F2}$
H	$V_{\rm CE,sat3}+V_{\rm F1}$
I	$-V_{\rm DC}+V_{\rm CE,sat3}+V_{\rm CE,sat2}$
J	$V_{\rm CE,sat2}+V_{\rm F4}$
K	$V_{\rm CE,sat2}-V_{\rm CE,sat4}$
L	$V_{\rm F4}-V_{\rm F1}$

(FWD) D_1-D_4. It can be seen from Table II that the on-state voltage of T_1-T_4 and D_1-D_4 are included in v_{ab}. Likewise, it can be reasoned that the on-state voltage of T_3-T_6 and D_3-D_6 are included in $v_{\rm cb}$. In conclusion, the output voltages $v_{\rm ab}$ and $v_{\rm cb}$ contain the positive and negative DC-link voltage, and the sum of $V_{\rm CE,sat}$ and $V_{\rm F}$ of power semiconductors. Considering the functions of the proposed circuit, the positive and negative DC-link voltage can be clipped into the preset reference voltages, while the sum of $V_{\rm CE,sat}$ and $V_{\rm F}$ becomes detectable.

2) Single-phase inverter: For the single-phase inverter with unipolar SPWM or hybrid SPWM modulations, the operation modes are same with that of three-phase inverter excluding the modes (E), (F), (K), and (L) in Fig.3(b), which is detailed in [20].

3) Individual power semiconductor: With the self-power function, the plug-and-play is realized, and the circuit size and cost of the proposed method is still lower than that of existing component-level methods even it is applied to an individual power semiconductor.

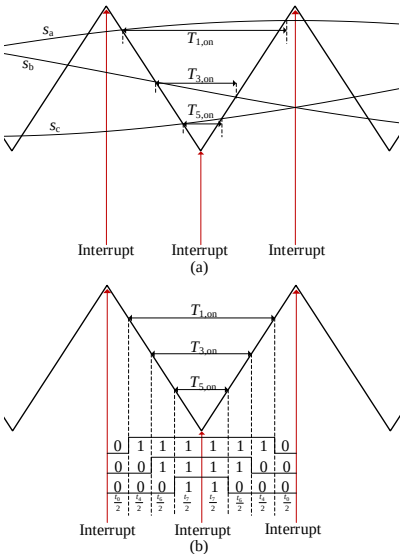

Fig. 4. Different modulation methods: (a) SPWM and (b) SVPWM.

B. Selection of components

The selection of components is discussed to make the measurement circuit has more better performance. Take the half circuit in Fig.1(a) (M_1, R_1, R_3, D_{a1}, and D_{a2}) and the self-power circuit as example:

- D_{a1} and D_{a2} must have the same rating voltage with the DC-link voltage of the converter and share identical electrical characteristics as much as possible. As such, V_{Da1} and V_{Da2} can be canceled with each other to a large degree, leading to a small measurement error.
- The depletion MOSFETs M_1 also must has the rating voltage higher than the DC-link voltage of the converter since it needs to withstand the DC-link voltage when D_{a1} is conducted.
- $R_1 - R_2$ can be SMD resistor due to the mA-level current during operation (e.g., 1.5 mA in this cast study). Among them, R_1 and R_2 are used to control the current flowing through D_{a1} and D_{a2}, respectively. So as to adjust the measurement error, which is discussed in Section IV, Part C.
- Z_1 and Z_2 are used to provide the bidirectional reference voltage. Their zener voltage should be higher than the maximum $V_{CE,sat} + V_F$.
- D_{a9} and D_{a10} are same with D_{a1} and D_{a2} except for the requirement of identical characteristic.
- M_5 and M_6 are the same with M_1.
- R_9 and R_{10} are the same with R_1.
- C_1 and C_2 are used to stabilize the reference voltages.

TABLE III
DESCRIPTION OF THE COMPONENTS USED IN THE PROPOSED CIRCUIT.

Components	Description	Value
M_1-M_6	Signal depletion MOSFETs	17 mA/600 V
D_{a1}-D_{a10}	ES1JR2	600 V/1 A
Z_1-Z_2	Zener diodes	6.2 V
R_1, R_3, R_5, R_7	SMD resistors	200 Ω
R_2, R_4, R_6, R_8	SMD resistors	1.2 k/1.8 k/6.8 kΩ
C_1-C_2	SMD capacitors	10 μF

TABLE IV
SPECIFICATIONS OF THE DEVELOPED INVERTER PLATFORM

Parameters	Value
DC-Link voltage	400 V
Switching frequency	10 kHz
Dead time	2 μs
Inductance	2 mH
AC capacitance	10 μF

IV. EXPERIMENTAL VERIFICATION

A. Hardware realization

The implementation process of the proposed circuit for a single device, single-phase inverter, and three-phase inverter is discussed as summarized in Fig.5, including the power converter stage, monitoring circuit, Analog-Digital converter, digital signal processor, and data storage in computer.

1) Inverter stage: Firstly, the specifications of the three-phase inverter are listed in Table IV, along with its hardware realization as shown in Fig.6. The modulation method for the three-phase inverter is SPWM.

2) Prototype of the proposed apparatus: The prototype of the proposed circuit is designed as shown in Fig.7. The size of this prototype is 3.5 cm×4.5 cm×3 cm, which can be smaller further if the housing and connecting terminals are well-deigned and manufactured. The three input terminals are used to connect the output terminals of the three-phase inverter as shown in Fig.6. It is passive due to the proposed self-power circuit.

3) AD converter and data communication: Once the analog on-state voltage are obtained, they are converted into digital data by using a 14-bit dual channel AD converter and transmitted into a digital signal processor through the optical fiber. Then, the digital on-state voltage information can be processed further and used to assess the health condition of the power semiconductors.

B. Dynamic response testing of the proposed circuit

A fast dynamic response is mandatory for the on-line monitoring of on-state voltage considering the short measurement window during operating converter. The dynamic performance of the proposed circuit is verified with a step-change voltage signal. Fig.8 shows the measured results, indicating that the proposed circuit can follow the step-change input voltage very well, no matter it increases from -7.5 V to 6.5 V or decreases from 7.5 V to -6.5 V.

C. DC accuracy calibration of the proposed circuit

With the selected components in Table III, the accuracy of the proposed circuit is tested with DC input voltage. One of

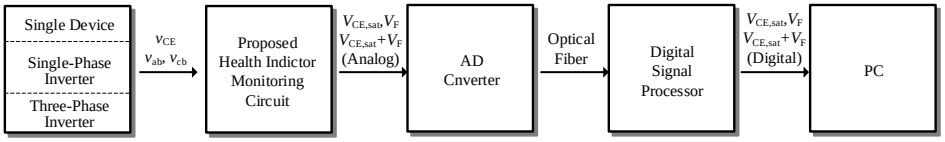

Fig. 5. Implementation process.

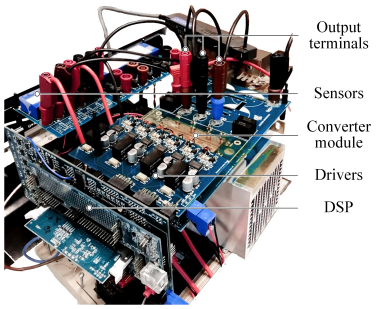

Fig. 6. Demonstrator of three-phase inverter

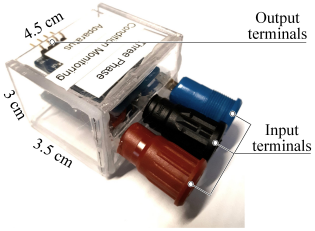

Fig. 7. Prototype of the proposed condition monitoring apparatus.

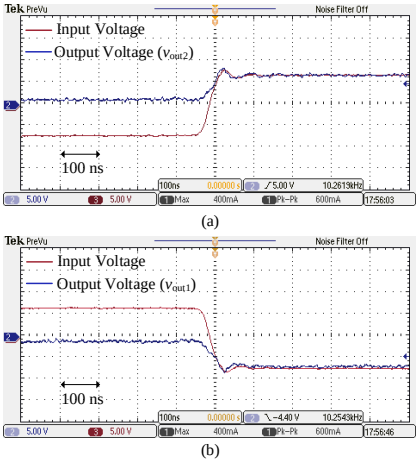

Fig. 8. Dynamic response of the proposed measurement circuit with a step-change input voltage: (a) from -7.5 V to 6.5 V; (b) from 7.5 V to -6.5 V.

the corresponding results are depicted in Fig.9, illustrating the relative error $\varepsilon_{\rm r}$ from a DC input voltage $v_{\rm in}$ to a DC output voltage $v_{\rm o}$ in the range from 1 V to 5 V. $\varepsilon_{\rm r}$ is limited to $\pm 2\%$ with an absolute maximum error 80 mV when $v_{\rm in}$ is 4 V and an absolute minimum error less than 5 mV when $v_{\rm in}$ is within 1.5 V and 1.9 V.

The change trend of $\varepsilon_{\rm r}$ can be roughly analyzed with the help of the circuit in Fig.1. If the input voltage is from 1 V to 5 V and the $V_{\rm ref+}$ is 9 V, the voltage drop in R_2 ranges from 8 V to 4 V by roughly assuming $V_{\rm Da1}$ and $V_{\rm Da2}$ can be canceled with each other. Consequently, the current flowing through $D_{\rm a2}$ ($I_{\rm Da2}$) decreases from 8/6.8 k=1.2 mA to 4/6.8 k=0.6 mA. On the other side, as the input voltage increases from 1 V to 5 V, the voltage drop in M_1 and R_1 increases from 0.5 V to 4.5 V by assuming a constant 0.5 V drop in $D_{\rm a1}$. However, it is difficult to quantitatively determine the specific voltage drop in M_1 or R_1 due to the variable impedance of M_1. Thus, the voltage drop in R_1 is measured experimentally and it increases from 0.4 V to 0.9 V along with the increasing input voltage. Consequently, the current flowing through $D_{\rm a1}$ ($I_{\rm Da1}$) increases from (0.4/200-1.2)=0.8 mA to (0.9/200-0.6)=3.9 mA. To summarize, as increasing $v_{\rm in}$ from 1 V to 5 V, $I_{\rm Da1}$ and $I_{\rm Da2}$ present opposite change trend, resulting that the $\varepsilon_{\rm r}$ increases from -1.7% to 1.7%.

Based on the above analysis, $I_{\rm Da1}$ and $I_{\rm Da2}$ can be changed by adjusting R_1, R_2, and the reference voltage. Then, the variation range of $\varepsilon_{\rm r}$ can be consequently moved or narrowed.

For example, if R_2 is replaced with a 1.8 kΩ resistance, the accuracy distribution is depicted in Fig.10(a). It shows the relative error $\varepsilon_{\rm r}$ is limited to $\pm 1\%$ when the $V_{\rm in}$ is higher than 3.8 V. Especially, $\varepsilon_{\rm r}$ is zero when $V_{\rm in}$ is 4.91 V. Similarly, increasing the reference voltage can also change the accuracy distribution as shown in Fig.10(b). The point with zero $\varepsilon_{\rm r}$ is moved to $V_{\rm in}$=3.35 V and the range of $\varepsilon_{\rm r}$ less than $\pm 1\%$ is moved to $V_{\rm in} \geq$2.8 V. Therefore, based on different applications, the relative error of the on-state voltage monitoring circuit can be limited to $\pm 1\%$ by selecting proper components. Considering the reference voltages generated by the proposed self-power circuit is $\pm$6.2 V and the monitored sum of on-state voltages to indicate the degradation level of the applied IGBT is within 4 V and 6 V in this case study, the selected components are as follows: R_1=200 Ω and R_2=1.2 KΩ, which can achieve same accuracy-level with Fig.10(a).

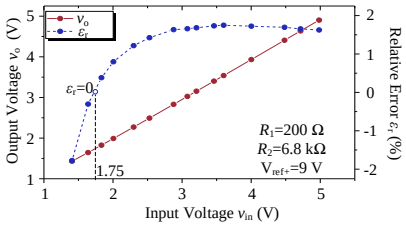

Fig. 9. Accuracy verification of the proposed circuit.

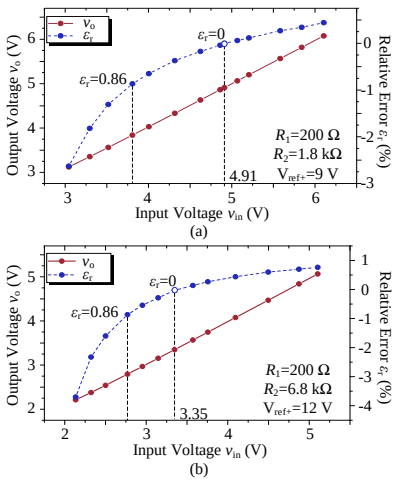

Fig. 10. Accuracy verification of the proposed circuit with different components compared to Fig.9.

D. Measured on-state voltage waveforms from an individual IGBT

The proposed circuit is firstly applied to an individual IGBT in the converter. The relative experimental results are given in Fig.11, including the sinusoidal output current i_a, the measured on-state voltage, and the extracted reference voltage, which verifies the effectiveness of the proposed circuit in extracting the reference voltage and on-state voltage from the two-terminals of IGBT.

E. Measured on-state voltage waveforms from three-phase inverter

There are four output signals of the proposed circuit for monitoring a three-phase inverter as shown in Fig.3(a). $v_{\rm out1}$ and $v_{\rm out2}$, extracted from $v_{\rm ab}$, consist of $V_{\rm CE,sat1} - V_{\rm CE,sat4}$ and $V_{\rm F1} - V_{\rm F4}$. Similarly, $V_{\rm CE,sat3} - V_{\rm CE,sat6}$ and $V_{\rm F3} - V_{\rm F6}$ are included in $v_{\rm out3}$ or $v_{\rm out4}$ extracted from $v_{\rm cb}$. For simplification, only the results measured from the phase leg a and b of the three-phase inverter are given as shown in Fig.12, indicating that the bidirectional high-voltages in $v_{\rm ab}$

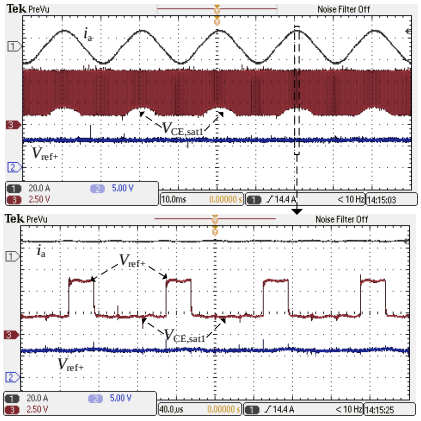

Fig. 11. Measured on-state voltage of an individual IGBT with the proposed circuit.

are clipped to the reference voltages. While the low on-state voltages are retained. The dash rectangle in Fig.12(b) is zoomed-in as shown in Fig.12(c). The low on-state voltages $V_{\rm CE,sat3} + V_{\rm F1}$ and $V_{\rm CE,sat2} + V_{\rm F4}$ are alternatively appeared in $v_{\rm out2}$. Likewise, it can be expected that $V_{\rm CE,sat1} + V_{\rm F3}$ and $V_{\rm CE,sat4} + V_{\rm F2}$ are alternatively appeared in $v_{\rm out1}$. They can be separated based on the operation modes listed in Table II. It is worth mentioning that The voltage spikes in Fig.12(c) are mainly attributed to the parasitic inductances of the module terminals, bus-bar, and the connecting wires between the inverter and the proposed circuit during the current commutation transient. they can be reduced by well designing the inverter and shorting the connecting wires, and do not impact the accuracy as only the steady-value is required during the data analysis step.

F. Result of the self-power supply

The extracted bidirectional reference voltages (e.g., ±6.2 V in this case study) are shown in Fig.13, indicating neglected impact on the inverter. Fig.14 compares the results of the measured on-state voltage waveforms from a three-phase inverter by using the self-power circuit and external power supply, indicating that there is no identical difference between them, which means the proposed self-power circuit is able to replace the external power supply.

G. On-line monitoring of the degradation of power semiconductors

The measured results from the three-phase inverter and single-phase inverter are similar. Therefore, the degradation testing is carried out based on a single-phase inverter for the sake of saving experimental material. The modulation of the single-phase inverter is unipolar SPWM and its specifications are same with the developed three-phase inverter (e.g., 400V DC-Link voltage and 30A peak current). The device under test

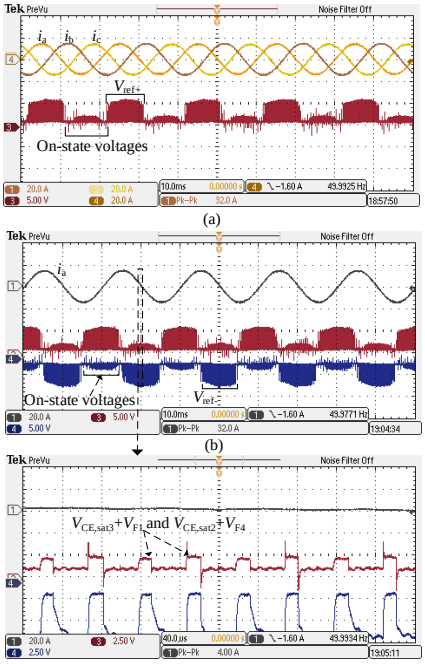

Fig. 12. Experimental results measured from the three-phase inverter: (a) CH1:$i_{\rm a}$, CH2:$i_{\rm b}$, CH4:$i_{\rm c}$, CH3:$v_{\rm out2}$ (b) CH1:$i_{\rm a}$, CH3:$v_{\rm out2}$, CH4:$v_{\rm out1}$; (c) Zoom-in of the rectangle in Fig.12(b).

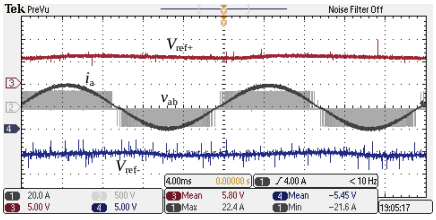

Fig. 13. Output waveforms of the proposed self-power circuit.

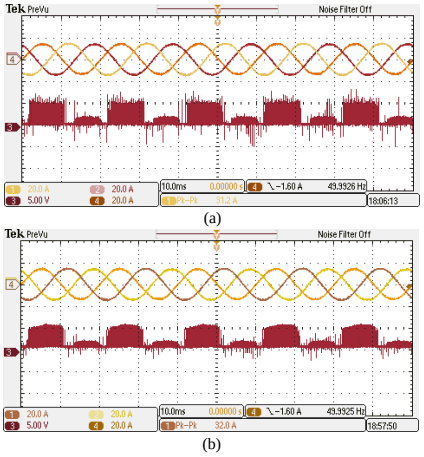

Fig. 14. Comparison of the monitored on-state voltage waveforms by using: (a) external power supply (b) proposed self-power circuit.

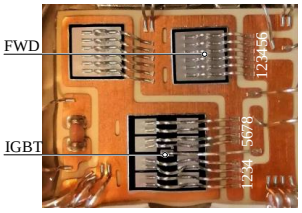

Fig. 15. Internal of the IGBT module under test.

TABLE V
EXECUTED ACTIONS TO SIMULATE THE BOND-WIRES LIFT-OFF OF POWER DEVICES (THE DEVICES UNDER TEST ARE THE IGBT IN T4 AND FWD IN T2).

Cases	Action
#1	New
#2	2 bond-wires of IGBT are cut off
#3	4 bond-wires of IGBT are cut off
#4	6 bond-wires of IGBT are cut off
#5	6 bond-wires of IGBT and 2 bond-wires of FWD are cut off

(DUT) is a 1200 V/50 A converter module (F4-50R12KS4). The IGBT and FWD are connected to the power terminals with 8 and 6 bond-wires, respectively as shown in Fig.15.

To verify the proposed circuit, the degradation mechanisms of IGBT are simulated by cutting off bond-wires and increasing the heatsink temperature ($T_{\rm h}$), respectively. They are reasonable methods and have been verified in many researches [5], [30], [31]. The detail about how to cut off bond-wires is illustrated in Table V. The temperature of heatsink is controlled by a controllable heat plate at 40 °C, 50 °C, and 60 °C accordingly.

For simplification, only the bond-wires of T_4 and D_2 are cut off. For comparison purpose, the on-state voltage of T_2 and D_4 is also sampled. The monitored results are summarized in Fig.16. It shows that $V_{\rm CE,sat2}$+$V_{\rm F4}$ keeps same when bond-wires are cut off, while -$V_{\rm CE,sat4}$-$V_{\rm F2}$ is increased negatively, particularly at the peak point. These bond-wires are connected in parallel and the increment of their equivalent resistance is exacerbated as more bond-wires are cut off. Thus, -$V_{\rm CE,sat4}$-$V_{\rm F2}$ shows slow increase at first three cases (#1, #2 and #3). Then, it shows a relative big jump when 6 bond-wires are cut off (#4). In addition, it is increased further when the two bond-wires of FWD are cut off (#5).

In practice, the change of on-state voltage caused by degradation becomes more larger at higher current. Therefore, the on-state voltage measured at the peak current is used as the health indicator as shown in Fig.17(a). It shows the monitored

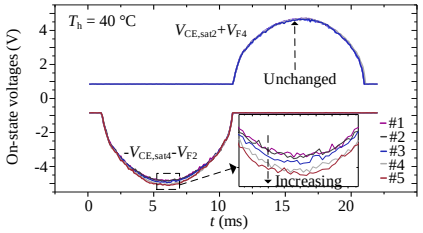

Fig. 16. Monitored on-state voltage among one fundamental period when the bond-wires of T_4 and D_2 are cut off and the heat-sink temperature is changed.

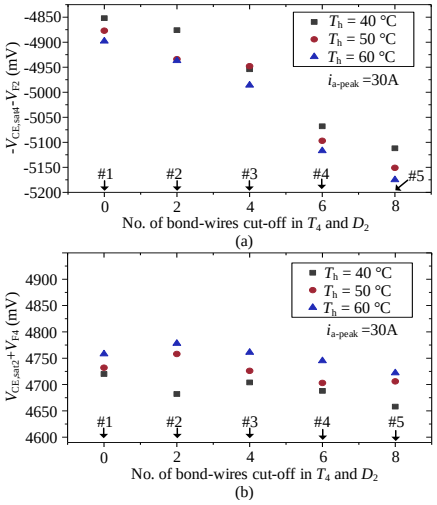

Fig. 17. Monitored on-state voltage at peak current when bond-wires are cut off and heat-sink temperature is increased: (a) -$V_{\mathrm{CE,sat4}}$-V_{F2} (v_{out1}) (b) $V_{\mathrm{CE,sat2}}$+V_{F4} (v_{out2}).

on-state voltage is increased negatively with cutting off the bond-wires and increasing the heatsink temperature by about 270 mV and 50 mV, respectively. While, if the bond-wires is health, the monitored on-state voltage is almost unchanged at the same temperature level as shown in Fig.17(b).

The monitored on-state voltages at peak point are normalized by using their initial value as shown in Table VI, indicating that after cutting off 8 bond wires (6 of IGBT and 2 of FWD), it is increased by more than 5% at each same heatsink temperature level.

V. Conclusion

A self-power solution is proposed for the on-state voltage monitoring circuit of power semiconductor devices in this paper. It can extract the power from the two-terminal of an individual power device or the middle-points of the phase-legs in the three-phase/single-phase inverter without influencing the operation of converter. With the proposed self-power circuit,

TABLE VI
Normalized On-state Voltage with Different Heatsink Temperatures and Numbers of Bond-wires Cut-off.

Cases	T_h=40 °C	T_h=50 °C	T_h=60 °C
#1	1(4852 mV)	1(4877 mV)	1(4898 mV)
#2	1.0050	1.0117	1.0080
#3	1.0210	1.0146	1.0180
#4	1.0445	1.0451	1.0447
#5	1.0536	1.0562	1.0566

the conventional component-level and converter-level on-state voltage monitoring circuits can exclude the external power supply and become plug-and-play application. In addition, the previously introduced converter-level on-state voltage monitoring circuit is extended to monitor a three-phase inverter, and its dynamic response and accuracy are investigated with step-change voltage and DC voltage, respectively. The relative measurement error of the prototype in this paper is limited to $\pm 1\%$ for a specific input voltage range by adjusting the selected resistances and reference voltages accordingly. Particularly, when R_1=200 Ω, R_2=1.8 kΩ, and $V_{\mathrm{ref+}}$=9 V, for example, the relative error is limited to $\pm 0.5\%$ with respect to the input voltage from 4 V to 6 V.

Finally, the ability of monitoring the degradation process and temperature change of power semiconductor is performed with a single-phase case study. According to the results, the on-state voltage is increased by over 5% (about 270 mV) when 6 bond-wires of an IGBT and 2 bond-wires of a Diode are cut off, and 1% (about 50 mV) when the heat-sink temperature is increased from 40 °C to 60 °C, respectively. Overall, due to the features of converter-level monitoring and self-powering, the proposed method can achieve the plug-and-play implementation, and reduced circuit complexity, size, and connecting terminals, compared to existing methods.

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Journal publication 4

An On-line Calibration Method for TSEP-based Junction Temperature Estimation

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The paper is under review
IEEE Trans. Power Electron., 2020.

The layout has been revised.

An On-line Calibration Method for TSEP-based Junction Temperature Estimation

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***Abstract*—This paper proposes a calibration method for junction temperature estimation of power semiconductors based on temperature sensitive electrical parameter (TSEP). It provides on-line calibration by measuring the heatsink/case temperature and the TSEP only in a functional converter, which is achieved by taking the start-up of converter and two thermal-steady states, and does not invade the system of interest. The concept, implementation, and error analysis of the proposed method are presented in this paper. Experimental verification is given to prove the effectiveness, accuracy, and convenience of the proposed method.**

***Index terms*—** Power semiconductor, junction temperature, condition monitoring, power converter.

I. Introduction

The junction temperature of power semiconductors T_j is a critical parameter for the lifetime prediction, condition monitoring, and optimal operation of power electronic systems. [1, 2]. Extensive efforts have been made to junction temperature estimation in the last two decades, which can be summarized into two types.

The first type is based on the power loss model and thermal model of power semiconductors [3–5]. T_j can be obtained from the measured case temperature and the estimated power losses during operation. However, there are some main issues in developing the power loss model and thermal model. For instance, the parameters used for the power loss calculation and thermal model estimation, such as the on-state voltage, switching energy, thermal resistances and capacitances, vary over different IGBT modules/chips, operational conditions, and installations. Thus, using the limited datasheet information to estimate the junction temperature could cause errors. Moreover, the thermal parameters are usually obtained by simulation [3] or off-line measurement [6]. Simulation requires the physical and material information of power modules, which are usually protected by manufacturers. While the off-line measurement of thermal parameters needs to be repeated once the degradation happens, which may be time-consuming and impractical.

The second type is to estimate the T_j indirectly by temperature sensitive electrical parameters (TSEPs), such as the on-state voltage [7, 8], change rate of collector-emitter voltage [9], base-collector voltage drop [10], switching time [11–15], gate peak current [16, 17], pre/threshold voltage [18, 19], miller plateau in gate voltage [20, 21], and Kelvin power emitter voltage [22, 23], etc. If the relationship between the T_j and TSEPs is calibrated in advance, only the TSPEs need to be measured to estimate T_j. In contrary to the first type, it does not require the information of power losses and thermal model, and has much simpler implementation process.

TSEP-based methods are of great interest, which however have not yet reached the maturity level for field applications due to the requirement of calibration. Conventionally, the calibration requires two key factors: 1) obtain the junction temperature information and the corresponding TSEPs; and 2) change the case/heatsink temperature to achieve another temperature-level. There are three main ways to realize the calibration:

- The first method is usually conducted in laboratory by following steps: open the power semiconductor module, and measure the T_j directly by thermal camera or optical fiber and corresponding TSEP [11, 16]; and then, case/heatsink temperature can be changed if the module is placed in a thermostat or amounted on a heat plate [13, 24]. However, this method breaks the power module and can not be used for an installed product in a functional converter.
- The second method does not need to open the power modules. It is performed when the converter is in off-power state and the thermal steady-state of power semiconductors is achieved. At this moment, T_j can be assumed to equal to the case/heatsink temperature. Then, firstly, an additional low-current (e.g., 1 A) is injected while turning on the power switch of interest, or a short conduction-time (e.g., 100 μs) is applied under a given current to the power semiconductor [8, 13, 24, 25], which can cause negligible temperature increase on T_j. Subsequently, except for the thermostat and heat plate, another temperature-level can be achieved by intentionally changing the heatsink conditions [25]. Thereafter, the above two steps can be repeated until the enough points of T_j and TSEPs are obtained. Above discussions show that, by controlling the operation status and cooling system, this method does not invade the power module and is more convenient to the installed product compared with the lab based calibration method. Nevertheless, it can be noticed that this method requires accessing to the controller of the converter or adding additional control, indicating invasive to the software of converter.

  Moreover, a commercial available product from Amantys

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realizes the calibration before the converter start-up [26]. It requires operating the converter under a specific mission profile up to 5 minutes with a wide power rating range, and making the heatsink temperature variation through reducing the coolant flow or fan speed. Although the auto-calibration can be finished before the start-up of converter, this product requires additional controls as well.
To sum up, the challenge is that the methods above are realized by adding additional control programs, which is unexpected from the converter design point of view.

- To exclude the requirement of adding additional control programs, a non-invasive solution is proposed in [27]. It achieves the calibration by logging the on-state voltage of IGBT, output current of converter, and the liquid temperature of cooling system at the whole power range of converter and enough liquid temperature variation (e.g., $\geq$10 °C). It is verified in a field wind power converter by using three-months data logs. However, the results show the estimated junction temperature fluctuates within 20 °C, presenting low accuracy-level. Moreover, this method relies on the huge data measured from a long-term operation. and the calibration process is time-consuming.

This paper proposes an on-line calibration method for TSEPs-based T_j estimation without invading the hardware and software of existing system. It is realized by using a reference temperature (e.g, heatsink temperature) and TSEP during the start-up process and two operating steady-states of a power converter. Compared to existing methods: 1) it does not require the open module; 2) it realizes the calibration without adding additional control programs; 3) it excludes the requirement of long-term data logging as the method in [27] do. Moreover, the proposed method can be performed throughout the service life of power devices in a system to distinguish the impact of degradation. In addition, it should be noted that the reference temperature can also be the case temperature, the NTC temperature of the power device module, or even the ambient temperature, which can be easily achieved. To illustrate the methodology of the proposed calibration method, the on-state voltage is taken as an TSEP example in this paper, which can also be other TSEPs.

The rest of this paper is outlined as follows: the principle and implementation are discussed in Section II. The error analysis and experimental verification are given in Section III, followed by the conclusions.

II. Concept and Implementation of the Proposed Method

By taking IGBT as an example, its T_j has a linear relationship with the on-state voltage $V_\mathrm{CE,sat}$ at a given collector current I_C [2], which can be expressed as:

$$T_\mathrm{j} = aV_\mathrm{CE,sat} + b \tag{1}$$

However, the coefficients a and b have to be obtained. Thus, this paper focuses on the parameterization of a and b by using the information which can be easily measured during the converter operation.

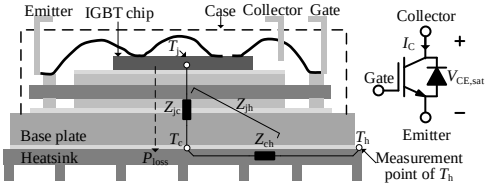

Fig. 1. Structure of IGBT module and its symbol.

A. Calculation of a

The junction temperature of an IGBT chip is a function of the power loss, thermal impedance, and the reference temperature (e.g., heatsink temperature) during the thermal steady-state [3],

$$T_\mathrm{j} = \begin{bmatrix} P_{\mathrm{loss},11} \\ P_{\mathrm{loss},21} \\ \cdots \\ P_{\mathrm{loss,m1}} \end{bmatrix} \times \begin{bmatrix} Z_{\mathrm{jh},11} & Z_{\mathrm{jh},21} & \ldots & Z_{\mathrm{jh,m1}} \end{bmatrix} + T_\mathrm{h} \tag{2}$$

where $P_{\mathrm{loss},11}$ is the power losses of the IGBT chip to be tested, including both conduction and switching losses. $Z_{\mathrm{jh},11}$ is the thermal impedance from the junction of IGBT chip to the heatsink as shown in Fig.1. $P_{\mathrm{loss},21}$-$P_{\mathrm{loss,m1}}$ are the power losses generated by other neighboring chips in the same module. $Z_{\mathrm{jh},21}$-$Z_{\mathrm{jh,m1}}$ indicate the coupled thermal impedance between the tested chip and other chips. By taking the derivative of (1) and (2) with respect to $V_\mathrm{CE,sat}$ at a given I_C,

$$\frac{dT_\mathrm{j}}{dV_\mathrm{CE,sat}} = a = \frac{d\sum_{i=1}^{m}(P_{\mathrm{loss,i1}}Z_{\mathrm{jh,i1}})}{dV_\mathrm{CE,sat}} + \frac{dT_\mathrm{h}}{dV_\mathrm{CE,sat}} \tag{3}$$

Z_jh can be assumed as a constant at a given degradation level. It is known that $V_\mathrm{CE,sat}$ is dependent on collector-emitter current and the junction temperature. During an operating converter: if the root-mean-square (RMS) of line current of an inverter increases from one level to another and T_h keeps constant, the first term on the right side of (3) are dominant. While, if the T_h increases from one level to another and the RMS of line current keeps constant, the second term on the right side of (3) becomes dominant since the increase of T_h causes the negligible $d\sum_{i=1}^{m}(P_\mathrm{losses}Z_\mathrm{jh})$ compared to dT_h. Thus, for the latter scenario,

$$a = \frac{dT_\mathrm{j}}{dV_\mathrm{CE,sat}} \approx \frac{dT_\mathrm{h}}{dV_\mathrm{CE,sat}} \tag{4}$$

Based on the above analysis, the coefficient a is obtained by measuring the change rate of T_h with respect to the change of $V_\mathrm{CE,sat}$ at two or more steady-states. It is feasible as both T_h and $V_\mathrm{CE,sat}$ are measurable. The change of T_h at a specific line current level can be realized by at least two ways: 1) the ambient temperature of the device varies in the application of interest, which induces the change of T_h; 2) it is changed by actively controlling the cooling of the inverter, such as varying the fan speed or liquid velocity.

Therefore, if the $V_{\mathrm{CE,sat}}$ at a given I_{C}, and the T_{h} are measured at two different heatsink temperature levels, a can be calculated by:

$$a = \frac{T_{\mathrm{h-H}} - T_{\mathrm{h-L}}}{V_{\mathrm{CE,sat-H}}(I_{\mathrm{C}}) - V_{\mathrm{CE,sat-L}}(I_{\mathrm{C}})} \quad (5)$$

where the subscript h-H and h-L mean high and low T_{h}, respectively.

B. Calculation of b

Once a is obtained, b can be calculated by substituting one pair of T_{j} and $V_{\mathrm{CE,sat}}$ into (1). Based on the 4^{th} Foster thermal network [4] during the thermal dynamic-state, the T_{j} with response to the P_{loss} is:

$$T_{\mathrm{j}} = \begin{bmatrix} P_{\mathrm{loss,11}} \\ P_{\mathrm{loss,21}} \\ \cdots \\ P_{\mathrm{loss,m1}} \end{bmatrix} \times \begin{bmatrix} \sum_{i=1}^{4} R_{11,\mathrm{i}}(1-e^{-t/\tau_{11,\mathrm{i}}}) \\ \sum_{i=1}^{4} R_{21,\mathrm{i}}(1-e^{-t/\tau_{21,\mathrm{i}}}) \\ \cdots \\ \sum_{i=1}^{4} R_{\mathrm{m1,i}}(1-e^{-t/\tau_{\mathrm{m1,i}}}) \end{bmatrix}^{\mathrm{T}} + T_{\mathrm{h}} \quad (6)$$

where $R_{11,\mathrm{i}}$ and $\tau_{11,\mathrm{i}}$ are the thermal resistance and time constant of the chip to be tested, respectively. $R_{21,\mathrm{i}}$-$R_{\mathrm{m1,i}}$ and $\tau_{21,\mathrm{i}}$-$\tau_{\mathrm{m1,i}}$ are the coupled thermal resistances and time constants between the tested chip and other chips. During the start-up of a power converter, t is a low value (e.g, 20 ms), the term representing the total impedance can be low enough to lead to a negligible difference between the T_{j} and T_{h}, compared to T_{h}. Therefore, b can be calculated by substituting one pair of T_{h} and $V_{\mathrm{CE,sat}}$ measured at the early stage of the start-up into (1). It should be noted that measuring $V_{\mathrm{CE,sat}}$ as earlier as possible during the start-up could limit the error because of a lower $\sum_{i=1}^{4} R_{(1-\mathrm{m})1,\mathrm{i}}(1-e^{-t/\tau_{(1-\mathrm{m})1,\mathrm{i}}})$.

To clarify the implementation process of the proposed method in practical applications, the time sequence is depicted in Fig.2, including three stages:

1) Stage 1 [t_1-t_2]: During the start up, the $V_{\mathrm{CE,sat}}$ is recorded when I_{C} reaches the given sensing current at the first time and the corresponding T_{h} as well. The time duration of this stage is less than a quarter fundamental period (e.g., 5 ms).

2) Stage 2 [t_3-t_4]: After the start-up, the converter arrives at the first thermal steady-state at t_3. Then, the corresponding $V_{\mathrm{CE,sat}}$ at the given sensing current and T_{h} are recorded. This stage duration depends on the thermal response of the applied power module and could be 10 to 100 s.

3) Stage 3 [t_5-]: The line current of the converter keeps unchanged while reducing the fan speed/liquid velocity of the cooling system. After the converter arrives at the second thermal steady-state, the corresponding $V_{\mathrm{CE,sat}}$ at the given sensing current and T_{h} are recorded again.

III. Application of the Proposed Method for the IGBT in a Single-phase Inverter

To verify the feasibility of the proposed method, a single-phase inverter setup is built using the IGBT module F4-50R12KS4, as shown in Fig.3(a), along with its hardware realization in Fig.3(b). The device under test (DUT) is T1 and the applied $V_{\mathrm{CE,sat}}$ measurement circuit is detailed in [28]. The specifications are shown in Table I. V_{dc} is the DC-link voltage; $I_{\mathrm{L,pk}}$ is the peak value of inductor current; f_{sw} is the switching frequency; $I_{\mathrm{C,sensing}}$ is the collector-emitter current of IGBT while measuring $V_{\mathrm{CE,sat}}$ in this paper; L and R are the filter inductor and load, respectively. The module is mounted on a forced-air heatsink. The temperature of the heatsink T_{h} is measured by a K type thermocouple with 0.1 °C resolution, which is displayed by a multimeter. For the comparative study, the plastic case of the IGBT module is removed and Fig.4(a) shows the layout of the applied IGBT module. An optical fiber temperature sensor (OTG-F type from OPsens) is used to measure the T_{j} of DUT directly as shown in Fig.4(b). Its response time and resolution are 5 ms and 0.05 °C, respectively. The sampling frequency of T_{j} can be set to from 100 Hz to 1 kHz.

TABLE I
Specifications of the Single-phase Inverter in the Case Study

Parameters	Value	Parameters	Value
V_{dc}	400 V	R	10 Ω
$I_{\mathrm{L,pk}}$	20 A	L	2 mH
f_{sw}	10 kHz	Dead time	2 μs
$I_{\mathrm{C,sensing}}$	5 A	Module	F4-50R12KS4

It is reported that the temperature distribution on the surface of the chip is uneven and usually the temperature at the center is higher than at the edge [3]. To investigate the temperature difference on the surface of the chip in this case study, two testing points are selected to measure the T_{j} while the inverter is in operation. When the T_{h} is 40 °C, the temperature at the center point and edge point are 51 °C and 49 °C, respectively. This temperature difference should be considered during the accuracy analysis of the proposed method. In the rest of this paper, the measurement point of T_{j} with the optic sensor is at the center of the chip surface.

A. Error analysis

The errors in the parameterizations of a and b are analyzed in this part. For the purpose of error analysis, the thermal impedances are measured experimentally [29]. Fig.5 depicts the self thermal impedance $Z_{\mathrm{jh,11}}$ of the chip to be tested (T1) and the coupled thermal impedances between T1 and other chips in the applied IGBT module, and their steady-state values are listed in Table II. Thereafter, based on the datasheet of the IGBT module and the specifications in Table I, the change of $V_{\mathrm{CE,sat}}$ with response to T_{j} and the power losses of chips can be calculated. Fig.6 graphically plots (3) when $I_{\mathrm{C,sensing}}$ is 5 A. It shows that dT_{h} is 99.5 % of dT_{j}, while dT_{jh} is only 0.5% of dT_{j}. Therefore, for this applied IGBT module, the error is 0.5% theoretically while calculating a.

According to Table I and the corresponding information from datasheet, the average power losses of one IGBT and one diode over one fundamental period are calculated as 16.5 W and 8.6 W, respectively, in this case study. In addition, the thermal resistances and time constants are obtained by

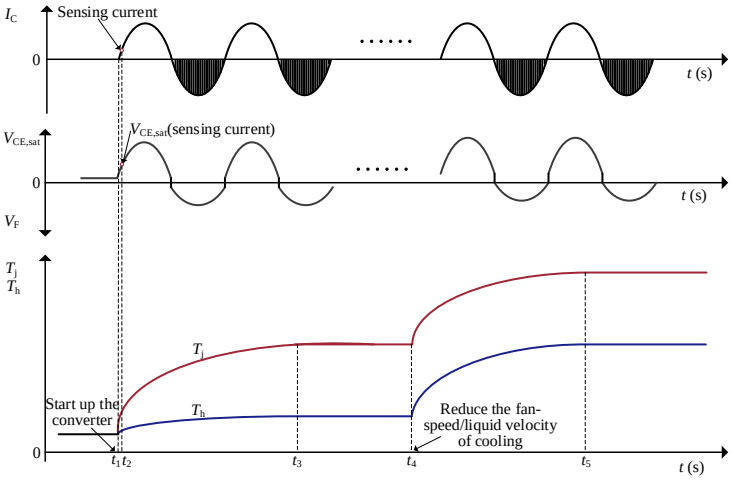

Fig. 2. Time sequence of implementing the proposed method.

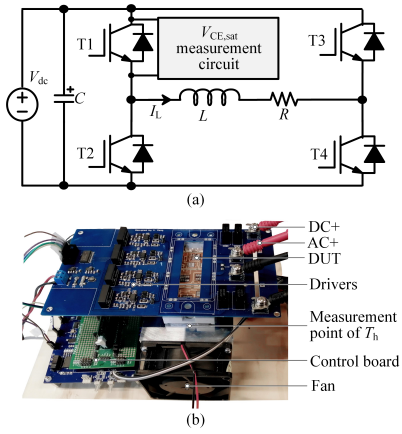

Fig. 3. Experimental setup: (1) topology; (2) hardware (the $V_{CE,sat}$ measurement circuit is connected to the collector and emitter of the DUT).

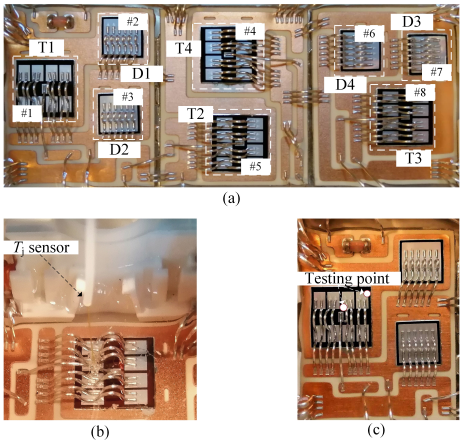

Fig. 4. Layout of the applied IGBT module: (a) marked number of chips; (b) implementation of the optical fiber temperature sensor; (c) junction temperature measuring point.

TABLE II
MEASURED STEADY-STATE THERMAL IMPEDANCES FROM JUNCTION TO HEATSINK OF THE APPLIED IGBT MODULE

Z_{th}	Value (K/W)	Z_{th}	Value (K/W)
$Z_{jh,11}$	0.578	$Z_{jh,51}$	0.069
$Z_{jh,21}$	0.146	$Z_{jh,61}$	0.044
$Z_{jh,31}$	0.175	$Z_{jh,71}$	0.043
$Z_{jh,41}$	0.07	$Z_{jh,81}$	0.038

fitting the measured thermal impedance in Fig.5. To simplify the analysis, it is assumed that the instant power losses of IGBT and diode are represented by the average power losses and independent from the temperature during the start-up. Then, combining with (6), the response of T_j over the start-up is depicted in Fig.7, indicating that the maximum difference between T_j and T_h is 1.3 °C during the first fundamental period (20 ms), which should be lower if the instant power losses is used. It should be noted that the obtained response of T_j is based on the theoretical calculation and some assumptions,

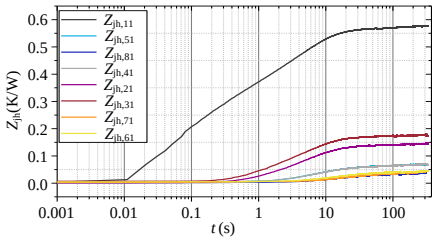

Fig. 5. Measured self and coupled thermal impedances of the applied IGBT module (F4-50R12KS4). $Z_{\mathrm{jh},11}$: self thermal impedance of T1; $Z_{\mathrm{jh},(2-8)1}$: coupled thermal impedance between T1 and other seven chips.

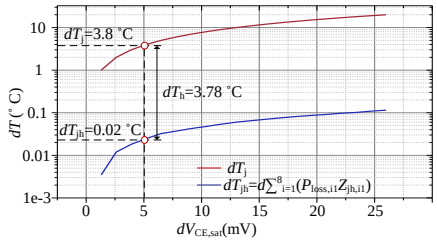

Fig. 6. Variation of dT_{j}, dT_{h}, and dT_{jh} with respect to $dV_{\mathrm{CE,sat}}$ at I_C=5 A based on the datasheet of the applied IGBT module (F4-50R12KS4), Table I, and (3).

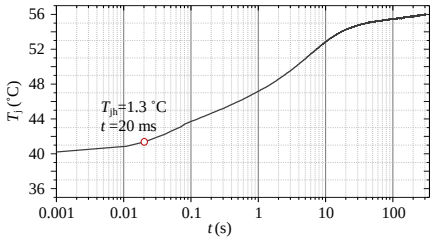

Fig. 7. T_{j} of the applied IGBT module (F4-50R12KS4) with response to the 14 W average P_{losses} in this case study when T_{h} is 40 °C.

which may vary according to different practical installations. Theoretically, for the applied IGBT module, the caused error while calculating b is 1.3 °C.

B. Calibration of the coefficients a and b

Firstly, It should be noted that I_{C} is unaccessible in practical applications and the measured current may not keep at a certain value at every measurement with the 10 kHz sampling frequency. Thus, instant I_{L} is used and measured at a small range in this paper. The implementation of the proposed method is given in Fig.8, which can be programmed as an auto self-calibration process during the start-up of the inverter as listed below:

1) Step 1: The inverter is started up and its inductor current is shown in Fig.9(a). Meanwhile, the T_{j} is recored by the applied optic fiber temperature sensor as shown in Fig.9(b), indicating that T_{j} is increased from T_{h} (40.5 °C) to 52 °C after the start-up for 7 s. Based on the zoom-in figure of Fig.9(b), if $V_{\mathrm{CE,sat}}$ is measured at the first fundamental period (20 ms), assuming T_{h} is equal to T_{j} causes the error by 0.8 °C only. In this paper, the $V_{\mathrm{CE,sat}}$ when I_{L} is within (5, 5.05) A is measured at every fundamental period from the start-up of inverter as shown in Fig.10 and only the first point is used. Besides, it is worth noticing that the start-up is performed six times at the same condition to verify the repeatability of the proposed method. The values of $V_{\mathrm{CE,sat}}$ of the six measurements are plotted in the zoom-in figure of Fig.10. To investigate the fluctuation caused by these measurements, both the highest one (1.742 V) and lowest one (1.738 V) are used to calculate b later;

2) Step 2: $V_{\mathrm{CE,sat}}$ is measured when I_{L} is within (5, 5.05) A once the T_{h} reaches its first stable temperature level. The corresponding $V_{\mathrm{CE,sat}}$ and T_{h} are marked as $V_{\mathrm{CE,sat-L}}$ and $T_{\mathrm{h-L}}$, respectively.

3) Step 3: The fan speed is reduced until T_{h} reaches the second stable level. The $V_{\mathrm{CE,sat}}$ and T_{h} at I_{L} within (5, 5.05) A are measured and marked as $V_{\mathrm{CE,sat-H}}$ and $T_{\mathrm{h-H}}$, respectively. The experimental results of Step 2 and Step 3 are shown in Fig.11, indicating that T_{h} and T_{j} are increased by 21 °C and 21.5 °C, respectively. As a result, T_{jh} is increased from 10.2 °C to 10.7 °C, implying a negligible dT_{jh}.

4) Step 4: By substituting the measured $T_{\mathrm{h-L}}$, $T_{\mathrm{h-H}}$ and $V_{\mathrm{CE,sat-L}}$, $V_{\mathrm{CE,sat-H}}$ into (5), a is obtained as shown in Fig.12 (411.8 °C/V). The negligible difference between $dT_{\mathrm{h}}/dV_{\mathrm{CE,sat}}$ and $dT_{\mathrm{j}}/dV_{\mathrm{CE,sat}}$ verifies that it is reasonable to neglect the terms $d(P_{\mathrm{losses}}Z_{\mathrm{jh}})/dV_{\mathrm{CE,sat}}$ and $d(P_{\mathrm{couple}}Z_{\mathrm{couple}})/dV_{\mathrm{CE,sat}}$ in (3).

5) Step 5: Based on the calculated a, measured T_{h} at the step 1, and (1), two of the measured $V_{\mathrm{CE,sat}}$ in Fig.10 (1.738 V and 1.742 V) are used to calculate b, which are -675.2 (b_1) and -676.9 (b_2), respectively.

C. Practical considerations

There are some practical considerations should be noted: 1) the measurement of I_{L} is set to a small range instead of a certain value based on the sampling frequency and resolution of current sensor; 2) due to the measurement range of I_{L} and the measurement noises, the measured $V_{\mathrm{CE,sat}}$ may fluctuate in a small range as well. Thus, the average of the measured $V_{\mathrm{CE,sat}}$ in steady-state is used to calculate a as shown in Fig.11; 3) the bad data of $V_{\mathrm{CE,sat}}$ may existed due to some high-noise applications. To exclude it, the measured $V_{\mathrm{CE,sat}}$ can be limited to a reasonable range, or compared with its neighboring data. Moreover, the selection of sensing current is based on the trade-off between the error and the sampling rate of current: the higher sensing current has lower change rage that requires lower sampling rate. However, the relative error is increased while calculating b; On the contrary, the lower sensing current

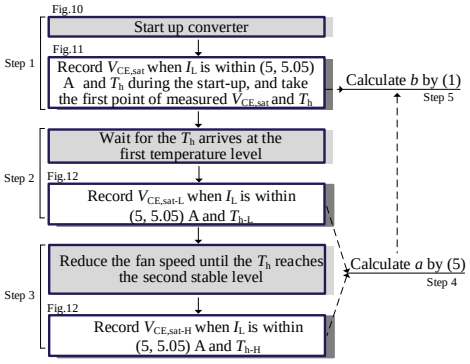

Fig. 8. Implementation process of the proposed method.

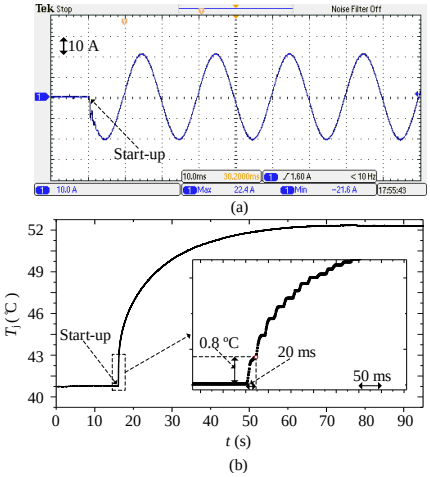

Fig. 9. Start-up of the inverter: (a) Inductor current of converter I_L; (b) Measured T_j with 1 kHz sampling frequency.

has higher change rate, which means for a same sampling frequency, the measured $V_{CE,sat}$ has wider fluctuation. But the relative error is decreased.

D. On-line estimation of T_j

Once a and b are calibrated, (1) can be used to estimate the T_j of the DUT when the inverter is in operation. For the comparison purpose, T_j is also measured directly by an optic fiber thermal sensor. The operating condition is changed by turning on and off the fan of the forced-air cooling manually. Meanwhile, $V_{CE,sat}$ of DUT is measured when I_L is within 5 A and 5.05 A, and transformed into T_j by using (1) as shown in Fig.13. It can be seen that most of the errors between

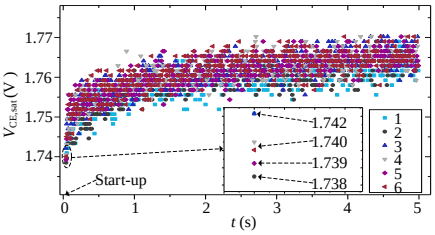

Fig. 10. Measured $V_{CE,sat}$ when I_L is within (5, 5.05) A after the start-up for six times.

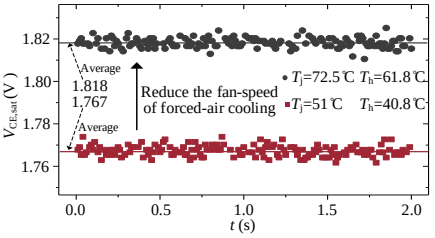

Fig. 11. Synchronous measurement of T_j and T_h before and after the change of the fan speed.

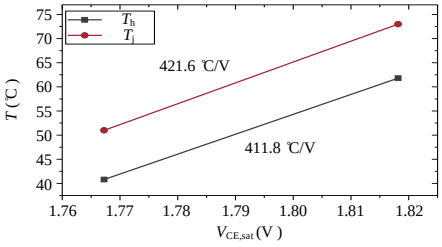

Fig. 12. Comparison between $dT_j/dV_{CE,sat}$ and $dT_h/dV_{CE,sat}$.

the results from the optical fiber temperature sensor and the proposed method with a and b_1 are within absolute 2 °C, and with a and b_2 are within absolute 4 °C, which is mainly caused by: 1) assuming T_j is equal to T_h while calculating b; 2) the measurement of I_L is within a small range, leading to the corresponding $V_{CE,sat}$ fluctuation within a small range as well; 3) the direct measurement of T_j refers to the point with the highest temperature on the chip surface. While the T_j estimated by the TSEP based method refers to the average temperature of the chip surface. Therefore, it is reasonable that the temperature estimated by the proposed method is lower than that of direct measurement. Moreover, the error is increased with increasing temperature, which is due to the positive temperature dependence of the first term on the right side of (3). Thus, neglecting them while calculating a can increase the error at higher temperature. Overall, the proposed method

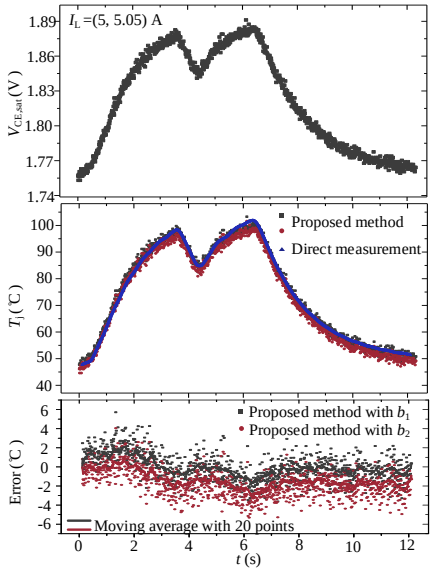

Fig. 13. Measured $V_{\mathrm{CE,sat}}$ when I_{L} is within (5, 5.05) A (top), estimated $T_{\mathrm{j}}^{\dagger}$ with proposed method and measured $T_{\mathrm{j}}^{\dagger}$ with optic fiber temperature sensor (middle), and the corresponding error (the data with the proposed method minus the data with the direct measurement) (bottom).

enables an on-line calibration with a satisfactory accuracy level in junction temperature estimation.

IV. Conclusions

This paper presented an on-line calibration method for the temperature sensitive electrical parameter based junction temperature estimation of power semiconductors. It overcomes the limitation of conventional methods which require invading the physical module or adding additional controls to the converter. Moreover, it does not require a long-term data logging and has much higher accuracy-level. The experiment results from a single-phase inverter show that: 1) the calibration between $T_{\mathrm{j}}^{\dagger}$ and $V_{\mathrm{CE,sat}}$ is achieved by measuring the heatsink temperature and the $V_{\mathrm{CE,sat}}$ when inductor current is within (5, 5.05) A for an operating converter; 2) the estimated error with respect to a direct measurement is limited to 2-4 °C by using the proposed method in the case study. It can be reduced further by measuring $V_{\mathrm{CE,sat}}$ at an earlier stage of the start-up process due to the lower sensing current. Moreover, More fast current measurement can help reduce the fluctuation of the estimated results. Finally, considering the impact of the degradation of power devices on the relationship between $V_{\mathrm{CE,sat}}$ and $T_{\mathrm{j}}^{\dagger}$, the proposed calibration can be conducted periodically.

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Journal publication 5

A Passive Circuit for On-State Voltage Measurement of Power Semiconductor Devices

Y. Peng, H. Wang

The paper is under review
IEEE Trans. Power Electron., 2020.

The layout has been revised.

A Passive Circuit for On-State Voltage Measurement of Power Semiconductor Devices

Yingzhou Peng, *Student Member, IEEE*, Huai Wang, *Senior Member, IEEE*

***Abstract*—This letter proposes an on-state voltage measurement circuit for power semiconductor devices, without external power supply and internal self-power requirement. Three variants of the proposed circuit are presented for both component-level and converter-level applications. A proof-of-concept prototype is developed and tested for a three-phase inverter application.**

***Index terms*—** Power semiconductor, condition monitoring, converter level, on-state voltage, passive circuit.

I. Introduction

The on-state voltages are considered as the critical parameter for power semiconductors (e.g., the $V_{\mathrm{CE,sat}}$ of IGBT, the $V_{\mathrm{ds,on}}$ of MOSFET, and the V_{F} of Diode). It enables the device temperature estimation [1], condition monitoring [2–4], the determination of conduction losses, and consequently remaining useful life prediction. Moreover, it outperforms the gate-related parameters in terms of measurement circuit design, non-invasion, noise immunity, and robustness. Therefore, the exact determination of on-state voltages is of importance for a functioning power semiconductor.

Firstly, various component-level solutions are designed to monitor a single power semiconductor [2, 4–9]. In addition, [10] proposes a converter-level solution to monitor the on-state voltages of all power semiconductors in a single-phase inverter. Nevertheless, all of these solutions need the external power supply to provide the reference voltage or current. Compared to other components in these circuits, the power supply is much expensive by accounting for 80% of the total price at least, which also increases the circuit complexity with additional connections and large volume. To address this issue, one way is to replace the external power supply with a self-power circuit [J3]. However, it is still not the best solution by introducing more components.

To overcome the challenges above, this letter presents a simplified passive circuit without any external/internal power supply and self-power circuit requirements, enabling the fast and accurate component-level/converter-level measurement for on-state voltage. Overall, the proposed method is a plug-and-play solution with a very simple circuit. Compared to the previous converter-level solutions, the number of output signals is halved, resulting in reduced terminals, isolators, and analog-digital converters. The structure of this letter is as follows:

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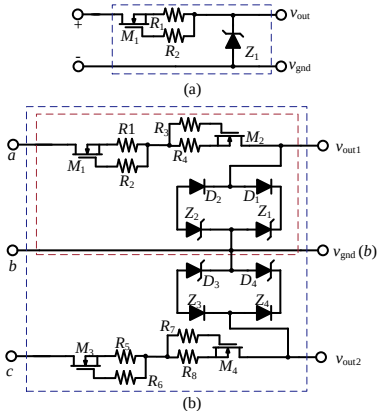

Fig. 1. Topology of the proposed on-state voltage measurement unit: (a) for a single power device; (b) for a single-phase inverter (red dash rectangle) and a three-phase inverter (blue dash rectangle).

Section II presents the concept and implementation of the proposed circuit with a case study; Section III demonstrates the effectiveness based on experimental testings, followed by the conclusion in Section IV.

II. Implementation of Proposed Circuit

A. Function analysis

The basic measurement circuits are shown in Fig.1, enabling sampling the change of on-state voltage at mV precision. It consists of few common signal devices without power supply, making it possible to be designed as a compact circuit or even a chip. The applied MOSFETs (M_1 - M_4) are signal depletion MOSFET, exhibiting different impedance by controlling its source-connected and gate-connected resistors. Z_1 - Z_4 are Zener diodes, and their Zener voltage V_{Z} should be higher than the maximum value of the signal to be measured.

The circuit depicted in Fig.1(a) is for the application of a single device. When the input voltage v_{in} is higher than V_{Z}, which makes Z_1 operates at reverse clamping mode. A voltage drop across R_1 makes M_1 operates at linear mode and exhibits high impedance, so that only a very low current (less than 1 mA) is allowed to flow, and thereby the output voltage is clamped to V_{Z}. Accordingly, v_{out} can be expressed as:

TABLE I
PRICE COMPARISON OF DIFFERENT SOLUTIONS FOR A THREE-PHASE CONVERTER APPLICATION (BASED ON THE PRICE FROM DIGIKEY).

Component	Unit Price (USD)	Quantity [2]	Quantity [10]	Quantity Fig.1(b)
Power supply	3-20	3	1	0
MOSFET (BSS126)	0.15	4	4	4
Diode (low-voltage)	0.04	12	0	4
Diode (high-voltage)	0.1	0	8	0
Zener diode	0.02	0	0	4
Resistor	0.0001	12	8	8
Total price (USD)		10-61	4.4-21.4	0.84

$$v_{\rm out} = V_{\rm Z} \tag{1}$$

If the input voltage is within zero and $V_{\rm Z}$, which is not enough to make Z_1 operates at reverse clamping mode. Thus, there is no current flowing through M_1 and it is in on-state. Consequently, the input voltage can directly reach at the output terminal:

$$v_{\rm out} = v_{\rm in} \tag{2}$$

If the input voltage is negative, it can directly reaches at the output terminal since Z_1 is in forward-conducted status and there is current flowing through the body diode of M_1. Therefore, this circuit cannot withstand the high negative voltage and is only suitable to a single device.

To withstand the bidirectional high voltage, another reverse-connected MOSFET with the corresponding resistors, diode, and zener diode is added, as depicted in the red dash-rectangle in Fig.1(b). Except for the function of the circuit in Fig.1(a), it can block high negative voltage and pass the low negative voltage as well.

When the input voltage is lower than $-V_{\rm Z}$-$V_{\rm D2}$, the anti-parallel body diode of M_1 and D_2 are conducted. Z_2 operates at reverse clamping mode and M_2 exhibits high impedance. Therefore, $v_{\rm out}$ is clamped to $-V_{\rm Z}$-$V_{\rm D2}$.

When the input voltage is within the range between $-V_{\rm Z}$-$V_{\rm D2}$ and $V_{\rm Z}$+$V_{\rm D1}$, diode D_1, D_2, Z_1 and Z_2 are all blocked and the voltages across R_1 and R_4 are zero, which means M_1 and M_2 are in on-state. Therefore, $v_{\rm out}$ equals to $v_{\rm ab}$ at this situation.

To sum up, the function of the circuit in Fig.1(b) is to block the voltage higher than $V_{\rm Z}$+$V_{\rm D1}$ and lower than $-V_{\rm Z}$-$V_{\rm D2}$, while pass the voltage within $-V_{\rm Z}$-$V_{\rm D2}$ and $V_{\rm Z}$+$V_{\rm D1}$.

The application of three-phase inverter can be achieved by replicating the red dash-rectangle part in Fig.2(b) as shown in the blue dash-rectangle in Fig.2(b).

B. Implementation in Three-Phase Inverter

Table I compares the cost of one typical component-level solution [2], active converter-level solution [10], and the proposed circuit in Fig.1(c). The required quantity of each component is for a three-phase inverter application. All the listed prices are based on the bulk purchase (e.g., 1000+ at least) from Digikey. The required power supply can provide the bidirectional voltage and its price varies according to different producers. Take the lowest price as example, its price accounts for 90% and 69% of the total cost in the component-level [2] and converter-level [10] solutions, respectively.

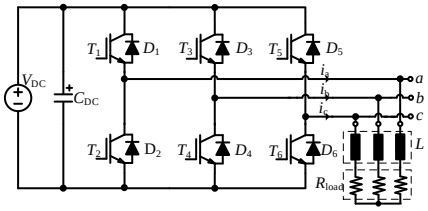

Fig. 2. Topology of three-phase inverter.

TABLE II
OUTPUT VOLTAGE $v_{\rm ab}$ OF THE THREE-PHASE INVERTER WITH CONSIDERING THE DEVICES IN THE UP-BRIDGE OF PHASE a AND b ONLY.

State	T_1	T_3	$i_{\rm a}$	$i_{\rm b}$	$v_{\rm ab}$
A	on-state	off-state	+	-	$V_{\rm DC}$
B	off-state	on-state	-	+	-$V_{\rm DC}$
C	on-state	on-state	+	-	-$V_{\rm CE,sat1} - V_{\rm F3}$
D	on-state	off-state	-	+	$V_{\rm CE,sat3} + V_{\rm F1}$
E	on-state	on-state	+	+	$V_{\rm CE,sat3} - V_{\rm CE,sat1}$
F	off-state	off-state	-	-	$V_{\rm F1} - V_{\rm F3}$

The proposed circuit is demonstrated with a three-phase inverter case study as shown in Fig.2. The input terminals (a, b, and c) of the proposed circuit are connected to the middle-point of each phase-leg in the converter. According to the operation of three-phase inverter [], it can be derived that the output voltages of inverter $v_{\rm ab}$ and $v_{\rm cb}$ include the on-state voltage of IGBT and the forward voltage of diode, the positive/negative DC-link voltages no matter the modulation method is SPWM or SVPWM. Take the devices in the upper bridge of phase a and b as an example, the output voltage $v_{\rm ab}$ can be obtained based on the on-off state of T_1 and T_3, and the current direction of $i_{\rm a}$ and $i_{\rm b}$ as illustrated in Table II. Likewise, the situations for the devices in other bridges can also be derived. $V_{\rm CE,satx}$ denotes the on-state voltage of $T_{\rm x}$, $V_{\rm Fx}$ denotes the forward voltage of $D_{\rm x}$.

In conclusion, the on-state voltages of all power semiconductors in a three-phase inverter are included in the output voltages either $v_{\rm ab}$ or $v_{\rm cb}$. With the function of the proposed circuit, the positive and negative DC-link voltages in $v_{\rm ab}$ or $v_{\rm cb}$ can be clamped to $V_{\rm Z}$+$V_{\rm D2}$ and -$V_{\rm Z}$-$V_{\rm D1}$, respectively. While the on-state voltages are measured preciously.

III. EXPERIMENTAL VERIFICATION

The physical realization of the proposed circuit is shown in Fig.3(a) with three input terminals on the one side and two output terminals on the other side. The circuit size of this prototype is 3.5*3.5 cm with one-side PCB design. The applied depletion MOSFET is BSS126 with 600 V/21mA power rating. Its source and gate connected resistances are 3 kΩ and 1 kΩ, respectively. The Zener voltage V_Z is 9 V and $D_1 - D_4$ are low-voltage diodes.

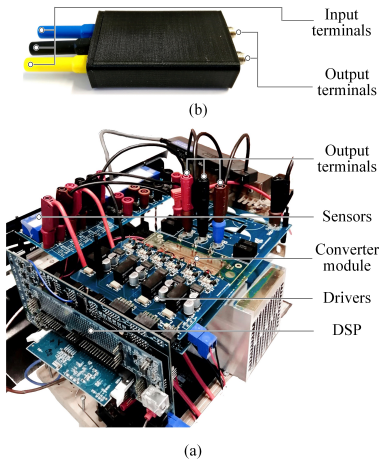

Fig. 3. Experimental setup: (a) three-phase inverter demonstrator; (b) prototype of the proposed passive on-state voltage measurement circuit.

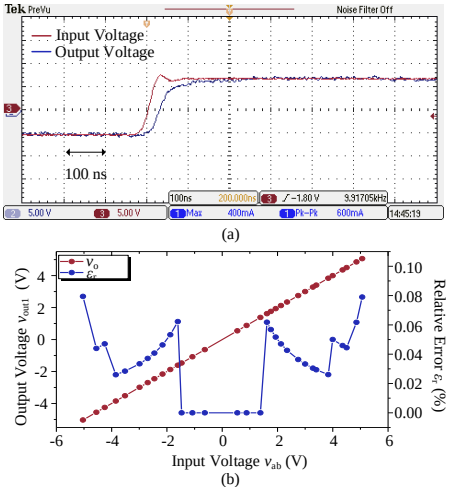

Fig. 4. Performance testing of the proposed circuit: (a) dynamic response with the step-change input voltage from -5 V to +5 V; (b) accuracy testing with the DC input voltage from -5 V to +5 V.

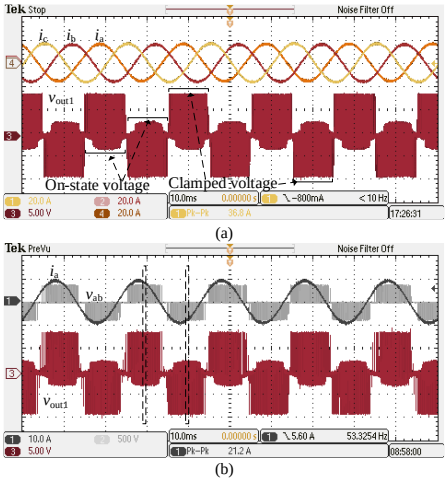

Fig. 5. Measured waveforms from the three-phase inverter and proposed circuit: (1) v_{out1} along with three-phase currents; (b) v_{out1} along with output current i_{a} and voltage v_{ab} from phase a and b .

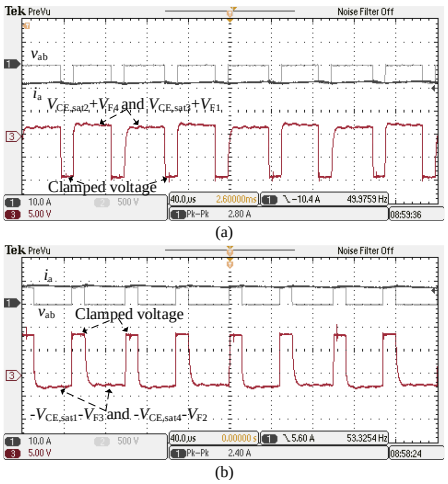

Fig. 6. Zoom-in waveforms from Fig.5(b): (a) measured on-state voltage is positive; (b) measured on-state voltage is negative.

A three-phase inverter demonstrator is developed to test the effectiveness of the proposed circuit as shown in Fig.3(b) and its operation point is set to 400 V/10 A with 10 kHz switching frequency.

The dynamic response is a key feature for the fast-switching applications. It is investigated with a step-change input voltage v_{ab} from -5 V to +5 V, as shown in Fig.4(a), indicating that the response time of the proposed circuit is less than 50 ns. In addition, Fig.4(b) gives the accuracy performance of the proposed circuit tested with a DC input voltage from -5 V to +5 V. The maximum relative error is limited to 0.8%. Especially, the absolute error is less than 1 mV when the input voltage is within ± 4 V.

Based on the analysis above, the on-state voltages of T_1-

T_4 and D_1-D_4 can be extracted from $v_{\rm ab}$, while the on-state voltages of T_3-T_6 and D_3-D_6 can be extracted from $v_{\rm cb}$. For simplification, only the results extracted from $v_{\rm ab}$ are given in this letter. The measured waveforms of the three-phase inverter and the proposed circuit are shown in Fig.5, including the output currents $i_{\rm a}$-$i_{\rm c}$, output voltage $v_{\rm ab}$ and the output signal of the proposed circuit $v_{\rm out1}$. It can be seen from Fig.5(b) that the measured on-state voltage shows variation with the sinusoidal output current $i_{\rm a}$ without any noises. Further, the zoom-in of the dash rectangles in Fig.5(b) are presented in Fig.6, respectively. Then, it can be seen that the positive +$V_{\rm dc}$ and negative -$V_{\rm dc}$ in $v_{\rm ab}$ are clipped into $V_{\rm Z}+V_{\rm D}$ and $-V_{\rm Z}-V_{\rm D}$, respectively. While, the on-state voltages of T_1-T_4 and D_1-D_4 are retained in $v_{\rm out1}$. Meanwhile, it can be expected that the on-state voltages of T_3-T_6 and D_3-D_6 are retained in $v_{\rm out2}$. Overall, the on-state voltages of all power semiconductors in this three-phase inverter can be obtained by using the proposed circuit and they are included in two signals ($v_{\rm out1}$ and $v_{\rm out1}$) separately. It should be noticed that the $V_{\rm CE,sat3}+V_{\rm F1}$ and $V_{\rm CE,sat2}+V_{\rm F4}$ are alternatively existed in Fig.6(a), for example. They can be separated easily with the help of the on-off information of IGBTs and the current direction as listed in Table I.

An on-line 14-bit analog/digital data sampling circuit with the function of optical data conversion/transmission (optical isolation) is also developed to acquire the digital on-state voltage. The results of T_1, T_3, D_1, and D_3 are given as shown in Fig.7. Over one fundamental period, $V_{\rm CE,sat}$ and $V_{\rm F}$ are appeared with different combinations at different time stages. Due to the variation of current, The values of these measured on-state voltages alter continuously, which proves the proposed circuit is able to sense the change of on-state voltage.

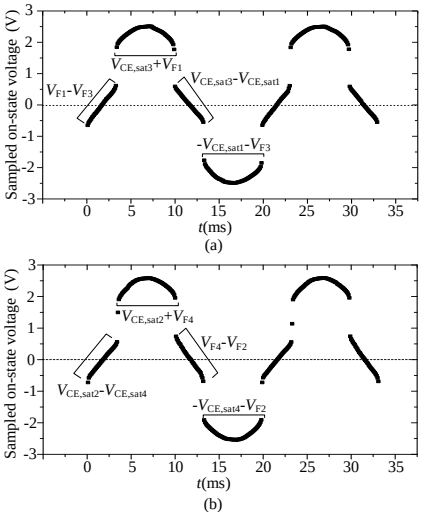

Fig. 7. Sampled on-state voltages of T_1, T_3, D_1, and D_3 with AD converter.

IV. Conclusions

In this letter, a passive converter-level measurement circuit is proposed. It can block the voltages out of the preset bidirectional clamp voltages $\pm(V_{\rm Z}+V_{\rm D2})$ with few components. In addition, the operation of the three-phase inverter is analyzed and it is found that the output voltages $v_{\rm ab}$ and $v_{\rm cb}$ contain the on-state voltages of all power semiconductors in this converter, and the DC-link voltages +$V_{\rm DC}$ and -$V_{\rm DC}$. Thus, with the proposed circuit, the on-state voltages can be extracted from $v_{\rm ab}$ and $v_{\rm cb}$. The achieved dynamic response time ($\leq$ 50 ns) and accuracy ($\leq \pm$0.8%) enables the precise and fast measurement of the on-state voltages. The concept and implementation of the proposed circuit are demonstrated with a three-phase inverter case study, and the experimental results verify its effectiveness. Compared to conventional methods, it achieves reduced circuit size, cost, and convenient implementation without compromising the dynamic response and accuracy. Technically, the application of the proposed method can be extended to many other converters that contain one or more phase-legs, and even a single power converter.

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ISSN (online): 2446-1636
ISBN (online): 978-87-7210-820-9 AALBORG UNIVERSITY PRESS