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Aunsborg, Thore Stig

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SOLID STATE GENERATOR FOR THE FLOAT ZONE PROCESS

BY
THORE STIG AUNSBORG

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Solid State Generator for the Float Zone Process

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Thore Stig Aunsborg

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PhD supervisors: Prof. Stig Munk-Nielsen
Aalborg University

R&D manager Sune Bro Duun
Topsil GlobalWafers A/S

Assistant PhD supervisor: Assoc. Prof. Christian Uhrenfeldt
Aalborg University

PhD committee: Associate Professor Peter Omand Rasmussen
Aalborg University, Denmark

Associate Professor Ziwei Ouyang
Technical University of Denmark, Denmark

Professor Dimosthenis Peftitsis
Norwegian University of Science and Technology, Norway

PhD Series: Faculty of Engineering and Science, Aalborg University

Department: AAU Energy

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Abstract

The float zone method is an industrial process for the production of very high purity silicon single crystals. This silicon is an important substrate material for many electronic components and is therefore vital to the modern power electronics industry. The process relies on high frequency (MHz) induction heating, which is an application area where the generator for supplying the high frequency current is typically based on vacuum tube technology with low energy efficiency. The replacement of the vacuum tube system with a solid state generator is now feasible, in part due to the development and maturity of power devices made from new semiconductor materials. The work in this thesis investigates and expands this opportunity.

The thesis initially presents an overview of the float zone process and the requirements for the high frequency generator. An overview of suitable circuit topologies for this application is then presented and the challenges associated with the generator requirements are discussed.

The thesis studies two main approaches to the construction of a generator system for MHz induction heating using a suitable resonant tank. The first approach utilizes a current source resonant inverter system for which a power module structure is presented with paralleled 1700 V SiC MOSFETs driven by integrated gate drivers. The module and inverter system design, manufacturing, and experimental operation is presented, and it is shown that the fabricated power module achieves higher than 90% efficiency for 2.3 kW output power.

The second approach, which draws on the experiences with development of the first system, utilizes a Class E push-pull resonant inverter topology. The design of the components of the inverter are presented, and the system is experimentally verified for high efficiency operation up to an input power of 5 kW. This approach is argued to be a viable option for the realization of a flexible and efficient inverter system for a full-scale float zone process generator.

Dansk resumé

Float zone metoden er en industriel proces der bruges til produktion af monokrystallinsk silicium med meget høj renhedsgrad. Dette silicium er et vigtigt substratmateriale til mange elektroniske komponenter, og er derfor af vital betydning for den moderne effektelektronikindustri. Processen udnytter højfrekvent (MHz) induktionsopvarmning, hvilket er et applikationsområde hvor strømgeneratoren typisk er baseret på radiorør som har lav virkningsgrad. Det er nu blevet muliggjort at udskifte radiorørssystemet med en transistorbaseret generator, til dels på grund af udviklingen og modningen af effektkomponenter lavet af nye halvledermaterialer. Arbejdet i denne afhandling undersøger og udvider denne mulighed.

Afhandlingen præsenterer indledningsvist et overblik over float zone processen og kravene der stilles til højfrekvensgeneratoren. Udfordringerne forbundet med disse krav bliver dernæst diskuteret, og særligt egnede kredsløbstopologier til applikationen bliver gennemgået.

Afhandlingen undersøger to hovedtilgange til at konstruere en generator til et MHz induktionsopvarmningssystem der bruger en passende svingningskreds. Den første tilgang anvender en strømkilderesonansvekselretter, hvortil strukturen beskrives for et effektmodul med 1700 V siliciumkarbid halvlederkomponenter drevet af integrerede styrekredsløb. Designet, fremstillingen og den eksperimentelle opførsel for effektmodulet og vekselrettersystemet præsenteres, og det vises at det fremstillede effektmodul opnår højere end 90% virkningsgrad for 2.3 kW udgangseffekt.

Den anden tilgang, som trækker på erfaringerne fra udviklingen af det første system, udnytter en klasse E push-pull vekselsrettertopologi. Udlægningen af komponenterne i vekselretteren præsenteres, og anvendelsen til MHz induktionsopvarmning verificeres eksperimentelt for højeffektiv drift ved effektniveauer op til 5 kW. Slutteligt argumenteres der for at denne tilgang er en realistisk valgmulighed til realiseringen af et fleksibelt vekselrettersystem med høj virkningsgrad til en fuldskala float zone proces generator.

Contents

Preface

This thesis is prepared as partial fulfillment of the PhD degree. The research presented herein was carried out as an Industrial PhD project in collaboration between Topsil GlobalWafers A/S and the Department of Energy, Aalborg University, and was funded by the Innovation Fund Denmark (IFD), Topsil GlobalWafers A/S, and the Department of Energy, Aalborg University.

The work was supervised by Professor Stig Munk-Nielsen, Topsil R&D manager Sune Bro Duun, and Associate Professor Christian Uhrenfeldt. I would like to express my sincere gratitude to each of you for giving me the opportunity to work with and learn from you. Thank you for trusting me with the freedom to develop myself both academically and personally, and for playing a major part in making this thesis happen.

I would also like to thank my colleagues at the R&D team at Topsil for the time we have worked together, the valuable guidance and discussions we have had throughout the project, and for creating a welcoming environment for me to learn from your expertise. The same goes for my colleagues at the Department of Energy - thank you all for both the helpful and the unhelpful discussions, and for making work here a worthwhile and enjoyable experience.

Finally, I wish to extend a special thanks to my amazing partner, family, and friends, whose wonderful company matters more to me than any personal accomplishment.

Thore Stig Aunsborg

Part I

Extended summary

Chapter 1

Introduction

The conversion and control of electrical energy is an important building block of the modern world. Prior to the advent and commercialization of the transistor and similar technologies in the middle of the 20th century, this task was accomplished using various forms of vacuum tube technology. Today, however, the conversion of electrical energy is nearly completely dominated by semiconductor-based power electronics, wherein solid state switching devices are used to control and modulate the flow of electrical power [1]. At the heart of all power electronic components are the semiconductor devices, most often made from silicon (Si), which control the flow of power from the source to the load. The components are found everywhere in modern society and in all power ranges, from cellular phone charging stations to electric vehicles, from small motor drives to wind turbines, and from toasters to industrial furnaces. The specifications of the devices and the way in which they are controlled is highly application dependent, and the devices are continuously improved to offer lower conversion losses, higher reliability, and lower cost.

To produce the silicon needed as substrate material for the electronics industries, the two common crystal growth methods applied are shown in Fig. 1.1, which are known as the Float Zone (FZ) process and the Czochralski (CZ) process, respectively [2], [3]. The techniques share quite a few characteristics; in both processes, the aim is to grow a single, monocrystalline ingot of silicon with a low impurity concentration. This is accomplished by melting polycrystalline silicon and allowing the molten silicon to slowly crystallize on a monocrystalline seed crystal in a controlled atmosphere. In CZ growth, the seed is dipped into a melt-containing crucible and then drawn upwards while maintaining a stable crystallization interface, while in FZ growth the bottom part of a feed rod of polycrystalline material is melted while the seed is pulled downwards, resulting in a "floating" molten zone. In order to produce a monocrystalline ingot, the pull rate is high at the initial stages of growth to facilitate the formation of

a *neck* with a diameter of a only few millimeters. Because of the low thermal stress in the thin neck, the propagation and multiplication of dislocations is greatly suppressed, such that a dislocation-free crystal is achieved after a few centimeters of growth [3], [4]. After neck formation, the pull rate is reduced to allow the growth of larger diameter ingots. For both FZ and CZ growth, the crystal is constantly rotated to provide homogeneity and to ensure the production of a cylindrical rod. The desired doping profile can be achieved either by adding dopants to the melt or by post-processing after growth.

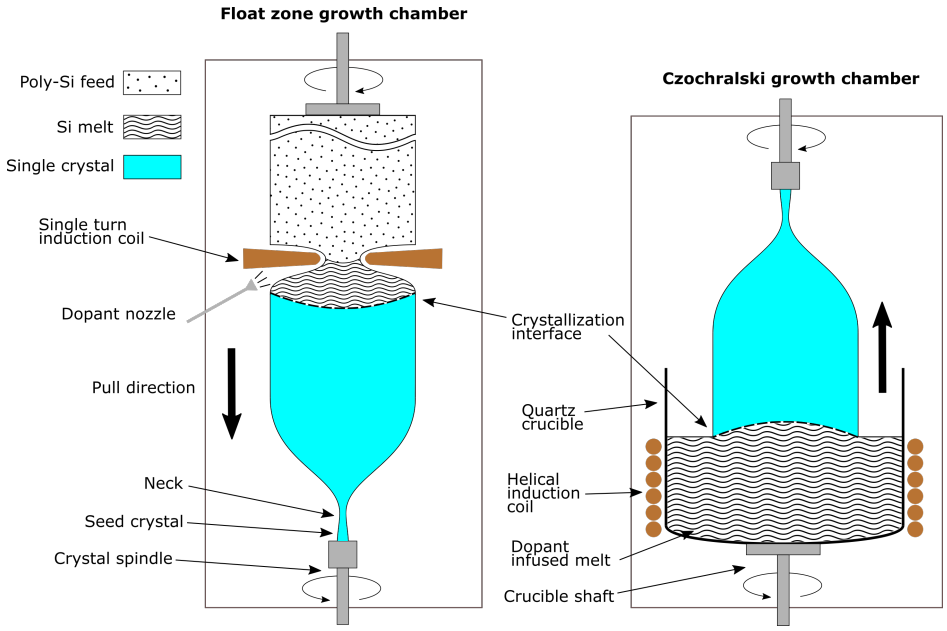


Fig. 1.1: Illustration of the basic setup for the two main crystal growth techniques for silicon.

By production volume, the CZ method is by far the most used of the two techniques, as larger diameter rods can be produced at a lower cost than what is possible with the FZ method [3]. However, since the melt is contained in a quartz (SiO_2) crucible, the produced crystal is inevitably contaminated with the crucible material, primarily oxygen [5]. Some discrete high power silicon components, such as power thyristors and high voltage diodes and IGBTs, have demanding specifications that require a substrate material with very high purity and resistivity, which is impeded by oxygen contamination [6]. The free-standing melt in the FZ method ensures minimal contamination, making the product ideal for higher voltage devices.

The diameter of the produced ingots is an important parameter, both from a device property standpoint and from an economic perspective. Modern FZ crystals are grown using the "needle eye" technique where the upper part of

the molten zone is much narrower than the crystal (see Fig. 1.1) [2], [6]. Using this technique, ingots up to 200 mm in diameter are currently on the market [4]. The power delivery in this process comes from a flat single-turn induction coil surrounding the needle eye in close proximity to the melt. The application of the needle eye FZ technique in seen in the photograph in Fig. 1.2 taken through the viewport of an FZ puller, showing the "pancake" inductor and the hot molten silicon. After the FZ processing the crystal is cut into ingots, which are further cut into thin wafers that are typically polished to a mirror finish. The final product of the process, silicon wafers used for device production, is shown in Fig. 1.3.

Fig. 1.2: Photograph of the FZ process through the view port of an FZ puller [7].

Fig. 1.3: Picture of the product from the silicon FZ process: low-contaminant monocrystalline silicon wafers [7].

The induction heating coil itself is a critical part of the FZ process to allow for contact-free crystal growth, ensure power delivery that results in a suitable heat and force distribution in the melt, and reduce the likeliness of electrical breakdown of the gas causing arcing [2]. By running a high frequency current through the coil an electromagnetic (EM) field is generated, causing eddy currents to flow in the silicon which heat the material through Joule heating. To achieve a smooth melting profile and the required heating profile that facilitates FZ growth, operation frequencies of a few MHz is typically used. This high frequency along with voltage and current requirements result in demanding specifications for the generator system supplying the heating power.

Interestingly, FZ production of silicon is therefore one of the few areas where solid state technology has yet to outmatch vacuum tube systems. As such, it belongs to a set of applications primarily within the field of high frequency/high power amplifier- and oscillator systems, such as e.g. radio frequency (RF) broadcasting amplifiers or industrial MHz heating systems, where tubes are still widely in use [8]–[11]. The FZ process requirements for high quality and large scale crystal growth have made vacuum tubes unparalleled for this type of high frequency heating application. One drawback is, however, that vacuum tubes are typically operated as linear amplifiers with energy efficiencies below 80% [11]–[13] (and generally significantly lower), while solid state based switch-mode circuit topologies can achieve practically realisable efficiencies above 90%, leading to considerable interest in exploiting the advantages of solid state solutions for generators for FZ production and similar processes. The challenge in achieving this goal lies in utilizing the semiconductor devices at the voltage, frequency, and power levels required for the applications.

In order to pursue a solid state generator system suited for FZ and other high frequency processes, researchers are looking toward new material technologies. Historically, power electronics devices were almost exclusively based on silicon due to the availability of high quality substrate material, native oxide properties, and process maturity [14]. While this technology is continually improving, the fundamental material properties of Si means that Si devices are limited in their power- and voltage handling capabilities in the MHz frequency range [15], [16]. In this respect, the material is outclassed by wide band gap (WBG) semiconductors such as gallium nitride (GaN) and silicon carbide (SiC). Recent advances in semiconductor manufacturing have enabled the development of competitive WBG power devices suitable for high frequency application areas [16], [17]. These WBG materials open up the design space for making devices

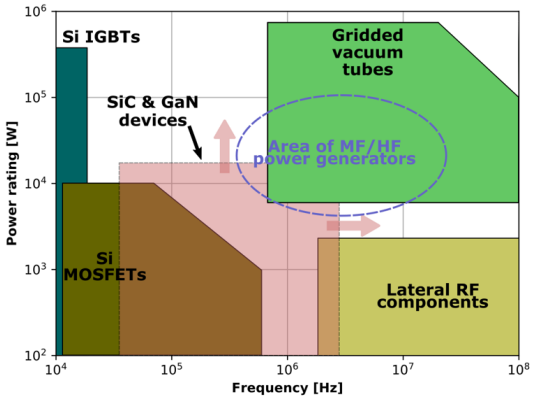


Fig. 1.4: Estimation of the operating ranges of devices used in power generation and conversion. The circled area shows the expanded application area considered here. [Paper A]

with higher breakdown voltage, reduced power losses, and superior switching performance based on the application demands [18]. For the FZ process and similar industry applications, devices with high switching speed and large power handling capability per area are desired, and WBG devices are thus prime candidates for expanding the frequency and power regimes of solid state technology into the demanding application of industrial MHz heating such as FZ production. This opportunity is illustrated in Fig. 1.4, which shows roughly the applicability areas of different device types used in power conversion and indicates the expansion possibilities of WBG devices into the high frequency target area currently dominated by gridded vacuum tubes.

To take advantage of these possibilities, this project revolves around investigations of the utilization of these devices in inverters suitable for a generator system for the FZ process. The basic layout of such a system is shown in Fig. 1.5.

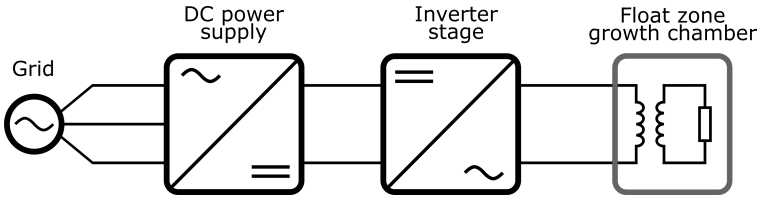


Fig. 1.5: General schematic layout of a generator system for FZ process heating.

1.1 State of the art

Induction heating is a very versatile process with many industrial heating applications, such as boiling, hardening, and welding [19], [20]. While common induction heating generators operate at significantly lower frequencies than the FZ process requires, several applications exist for plasma generators, dielectric heaters, and wireless power transfer which utilize frequencies in the MHz regime and often operate in the ISM frequency bands (6.78 MHz, 13.56 MHz, and multiples) [21]–[23]. Therefore, although the amount of specific literature on generator development for the FZ process is limited, insight may be gained from the considerable research that has been presented by various groups in the fields of MHz inverters for related industrial processes and high frequency resonant inverters in general utilizing WBG devices. An illustrative selection of recent research efforts relevant to the development goals in this project is given in table 1.1 below.

Table 1.1: Selected recent research efforts in high frequency power conversion. The table is expanded from Paper A.

Authors/year	Targeted application(s)	Power switches	Package	Circuit topology	Operating frequency	Output power	Efficiency
Haehre et al. (2014) [24]	HF power generators	1200 V SiC MOSFET	TO-247-3	Class D (full bridge)	2.4 MHz	2.4 kW	90.6%
Ghodke et al. (2016) [25]	Plasma source	900 V SiC MOSFET	TO-263-7	Class D (half-bridge)	2 MHz	3.4 kW	N/A
Choi et al. (2016) [26]	Wireless power transfer	a) 1200 V SiC MOSFET b) 650 V GaN HEMT	a) DE150 b) GaNpx	a) single ended class ϕ_2 b) push-pull class ϕ_2	6.78 MHz	a) 2.2 kW b) 2 kW	a) 93% b) 96%
Guo et al. (2016) [27]	Isolated DC/DC converter	1200 V SiC MOSFET	Bare die	Full-bridge LLC	1.2 MHz	4 kW	97%
Nguyen et al. (2017) [28]	Wireless power transfer	650 V GaN HEMT	GaNpx	Class DE (5 half-bridges)	13.6 MHz	4 kW	96.5%
Denk et al. (2018) [29]	HF power generators	1200 V SiC MOSFET	ISOPLUS-SMPD	Class DE (full-bridge)	2.5 MHz	25 kW	92.5%
Park et al. (2020) [30]	Plasma generator	1200V SiC MOSFET	TO-247-3	Class D (full-bridge)	3.4 MHz	10 kW	97%
Gu et al. (2021) [31]	Wireless power transfer	650 V GaN HEMT	GaNpx	PPT ϕ_2	6.78 MHz	1.7 kW	95.7%

As seen from the table, the application area for MHz inverters is diverse and there are many approaches to high efficiency designs. All of these rely on soft-switching concepts to dramatically reduce the switching losses at high frequency, which is achieved by utilizing circuit topologies with reactive elements to shape the voltages and currents of the switching devices at the switching instant [32]–[34]. Most commonly WBG devices are employed, in particular SiC MOSFETs and GaN HEMTs, and the choice of device is dependent on factors such as switching frequency, voltage requirements, and circuit topology [16], [18], [35]. In order to utilize the fast switching power devices, suitable packaging concepts of the devices must be employed both for discrete devices and power modules [36]–[38]. For MHz frequency operation, driving the switching devices also requires significant consideration [39], [40], as does the development of high efficiency passive components such as transformers and inductors [41], [42].

Within the context of a MHz inverter system for the FZ process, on overview of practical component limitations, circuit topologies, and switching device considerations is given in chapter 2.

1.2 Research objectives

The FZ production of silicon currently relies on vacuum tube oscillators due to demanding process requirements, which means the power efficiency of the production is limited. If a solid state generator based on off-the-shelf components could be utilized instead, significant advantages in energy savings, generator supply security, and process control are envisioned. By employing emerging

WBG semiconductor components, the frequency and power ranges of single solid state power modules is continuously increasing. Therefore, to investigate this opportunity for the FZ industry, the first research objective is

> **To investigate the feasibility of expanding the application range of solid state inverters into the area suitable for FZ production.**

To achieve this first research goal, it is necessary to develop a solid understanding of the challenges associated with operation the relevant devices in this frequency range, many of which are characterized by both theoretical and practical elements. Therefore, the second research objective is

> **To expand the knowledge base on the practical usage of WBG-based devices for MHz inverters through design, development, and verification of operation of relevant power module prototypes.**

To reach these goals the deliberate design of the entire inverter system is necessary, such that the specifics of the process requirements are considered in all aspects of the generator system.

1.3 List of publications

This thesis is based on the work presented in the following papers, which are also included as part II of the thesis.

A "Challenges and opportunities in the utilization of WBG devices for efficient MHz power generation", Thore Stig Aunsborg, Sune Bro Duun, Christian Uhrenfeldt and Stig Munk-Nielsen, *Published in "IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society"*, pp. 5107-5113, 2019.

B "Development of a current source resonant inverter for high current MHz induction heating", Thore Stig Aunsborg, Sune Bro Duun, Stig Munk-Nielsen and Christian Uhrenfeldt, *Published in "IET Power Electronics"*, 15, pp. 1–10, 2022.

C "Class-E Push-Pull Resonance Converter with Load Variation Robustness for Industrial Induction Heating", Benjamin Futtrup Kjærsgaard, Janus Dybdahl Meinert, Thore Stig Aunsborg, Sune Bro Duun, Asger Bjørn Jørgensen and Stig Munk-Nielsen, *Published in "European Conference on Power Electronics and Applications (EPE'22 ECCE Europe)"*, pp. 1-8, 2022.

D "Demonstration of a Class E Push-Pull Resonant Inverter for MHz Induction Heating", Thore Stig Aunsborg, Benoît Bidoggia, Sune Bro Duun, Janus Dybdahl Meinert, Benjamin Futtrup Kjærsgaard, Asger Bjørn Jørgensen and Stig Munk-Nielsen, *Accepted for publication in "Applied Power Electronics Conference (APEC)"*, 2023.

In addition to the appended papers which are included in the thesis, the author has participated in the work on the following papers which have been published during the PhD project period.

1 "High Frequency Resonant Operation of an Integrated Medium Voltage SiC MOSFET Power Module", Asger Bjørn Jørgensen, Thore Stig Aunsborg, Szymon Beczkowski, Christian Uhrenfeldt and Stig Munk-Nielsen, *Published in "IET Power Electronics"*, 13, pp. 475-482, 2020.

2 "Thermal Performance of an Integrated Heat Spreader for GaN HEMT devices", Faheem Ahmad, Thore Stig Aunsborg, Szymon M. Beczkowski, Stig Munk-Nielsen and Asger Bjørn Jørgensen, *Published in "12th International Conference on Integrated Power Electronics Systems (CIPS)"*, pp. 1-6, 2022.

3 "Digital design demonstration of 10kV SiC-MOSFET power module to improve wire-bonding layout for power cycle capabilities", Masaki Takahashi, Thore Stig Aunsborg, Christian Uhrenfeldt, Stig Munk-Nielsen and Asger Bjørn Jørgensen, *Published in "IEEE International Workshop on Integrated Power Packaging (IWIPP)"*, pp. 1-6, 2022.

4 "Analysis of Nonlinear Conductivity Coating used to Improve Electric Field Distribution in Medium Voltage Power Module", Yuan Gao, Yang Yang, Hongbo Zhao, Thore Stig Aunsborg, Stig Munk-Nielsen and Christian Uhrenfeldt, *Published in "IEEE Energy Conversion Congress and Exposition (ECCE)"*, pp. 1-7, 2022.

1.4 Thesis outline

This thesis is structured as follows. Chapter 1 presents the topic of float zone silicon crystal growth from a general perspective, and introduces the state of the art in the field of high frequency inverter structures relevant to the development of an inverter for the float zone process. The research objectives are then presented.

In order to fulfil the research goals, chapter 2 dives deeper into considerations of the float zone process requirements seen from a generator perspective, in order to investigate the feasibility of different approaches to the solid state generator. An overview of directly relevant power electronics concepts is then

briefly given, leading into a discussion of suitable circuit topologies for the inverter and the challenges in realizing the physical generator system. Several of the arguments in this and in the introduction chapter were developed and presented in paper A.

Chapter 3 presents the efforts in the demonstration of a current source resonant inverter for MHz induction heating. The fundamentals of the topology are presented, along with a power module featuring paralleled SiC MOSFETs and integrated gate drivers for transformerless MHz operation of a industrially relevant resonant tank. The design, operation, and discussion of the system is the main content of paper B. In addition, a similar approach with the inclusion of diodes for switch timing variation is briefly presented.

The knowledge and experience in working at MHz frequencies with paralleled WBG components is further developed in chapter 4. Here, a Class E push-pull resonant inverter implementation with load frequency variation robustness is introduced. The basic circuit operating principles of the topology are introduced, along with experimental demonstration and discussion of the operation of the inverter. A low power version of the topology is presented in paper C, while further development of the concept to a higher power implementation is presented in paper D.

Chapter 5 concludes on the findings in the thesis and highlights the main research contributions, ending with a discussion of future work.

Chapter 2

Generator specifications & inverter options

In order to assess the feasibility of developing a generator suitable for the FZ process, the nature of the process demands on the generator system is first overviewed in this chapter.

Succesful growth of silicon by the FZ process is governed by the highly nonlinear and complex interplay of many parameters. The process has been studied and continuously improved since its conception in the early 1950s, and thus the geometries of components and operation specifications are finely tuned to allow for production of large diameter crystals. Because of this, a solid state generator must adhere to the specifications from existing technology. As the generator supplies the heating power to the melt through induction heating, one of the most critical components is the work coil, a schematic of which is shown in Fig. 2.1. This coil is commonly made of copper and the influence of the slits is to promote magnetic field strengthening and consequently heating at the outer regions of the melt surface away from the molten neck. Coupled with the rotation of the crystal, a nearly axisymmetric temperature profile can be achieved in the melt by the use of slits [2].

The work coil geometry is determined entirely by the process requirements and small changes to its geometry may result in drastic variation in the electromagnetic pressure and molten Si temperature distribution profile [2]. Since a single turn coil is used and the load is non-ferromagnetic, the coupling efficiency for the induced magnetic field is limited. This results in the necessity of carefully considering the work coil properties in the FZ generator system design.

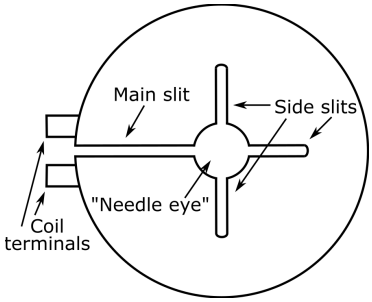


Fig. 2.1: Top-down schematic of a work coil used for FZ growth with the needle eye technique.

2.1 Float zone process requirements

The developed solid state generator system should be integrable with existing industrial FZ production geometries and process specifications. Therefore, the specifications most relevant to the generator development are outlined below.

Power level The power requirement for the FZ generator is self-evidently determined primarily by the need to sustain the zone of molten Si at around 1400°C, and therefore increases for larger crystal diameters. Under the high frequency approximation for the generated electromagnetic (EM) field which assumes, as is typical of the FZ process, that the skin depth is small compared to the inductor and feed rod dimensions [2], [6], the dissipated power density through Joule heating can be written

$$q_{\mathrm{EM}} = \frac{i_{\mathrm{ef}}^2}{\delta\sigma} \tag{2.1}$$

where i_{ef} is the effective density of the surface current, which is directly proportional to the coil current. Empirically, because the coupling to the Si load is weak, many hundreds of amperes are normally required in the work coil, increasing with higher power requirements for large diameter crystal growth, such that the transferred power to the silicon ingot may be in the tens of kW for large diameters. Due to the high currents, resistive heating losses of the coil itself may be of similar magnitude, so considering this as well as losses in connectors and auxiliaries, the output power of the envisioned generator must be scalable within the area shown in Fig. 1.4.

Working frequency The induction heating frequency is a critical parameter for succesful crystal growth. In order to achieve sufficient melting of the feed rod a low penetration depth is required, often illustrated by the skin depth at which the EM field has decayed to 1/e of its surface value

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_r \mu_0}} \tag{2.2}$$

where δ is the skin depth, ρ is the resistivity, f is the frequency, μ_r is the relative permeability, and μ_0 is the vacuum permeability. In the FZ process for larger crystal diameters using the needle eye technique, MHz frequencies are typically required to ensure proper melting of the surface of the silicon. If the frequency is too low, the EM field penetrates deep into the feed rod (see table 2.1), which combined with radiative heat loss leads to the formation of a thin solid layer at the surface, preventing succesful growth [43]. However, too high operating frequency increases the risk of arcing and process instability. Therefore the frequencies currently used in industry and which have a proven track record of succesful results are between 2.4 MHz and 3 MHz, although succesful growth is also possible with slightly lower frequency [2], [44].

Table 2.1: Variation of penetration depth in silicon with coil operating frequency.

		Skin depth, δ [mm]			
Material phase	Resistivity, ρ [Ω·m]	500 kHz	1 MHz	2 MHz	3 MHz
Solid silicon	$2 \cdot 10^{-5}$ [45]	3.2	2.3	1.6	1.3
Molten silicon	$8.3 \cdot 10^{-7}$ [45]	0.65	0.46	0.32	0.27

In addition, normal variations in the coupling to the load during stable operation and within different phases of the growth process means that the work coil inductance is not fixed. If the coil is part of a resonant circuit, the resonance frequency of this circuit is then also not fixed and the oscillator system is therefore typically allowed to drift in frequency during the process to maintain the desired heating profile and force balance surrounding the molten zone. It is thus an additional requirement from the generator that it is capable of operating with high efficiency in a wide frequency range.

Coil voltage The requirement for high coil voltage is an important reason for the usage of vacuum tubes technology in FZ production. From the relations between current, power, and frequency from (2.1) and (2.2) it follows that

$$i_{\text{ef}}^2 \propto f^{-1/2} \Longrightarrow I_{\text{coil}} \propto i_{\text{ef}} \propto f^{-1/4} \tag{2.3}$$

where I_{coil} is the current in the work coil. Assuming a small frequency variation, such that the work coil can be represented by simple constant inductance, and a high quality factor of the coil to neglect the coil resistance, the proportionality between frequency and voltage is found from Ohm's law:

$$V_{\text{coil}} = 2\pi f L_{\text{coil}} I_{\text{coil}} \Longrightarrow V_{\text{coil}} \propto f^{3/4} \tag{2.4}$$

Given that the power requirements, coil geometry, and high operating frequency are entirely specified by the requirements of the melting process it is evident that high voltages must be applied at the coil terminals, and any additional series inductance will result in higher voltage requirements for a given output power. Thus for a common loaded work coil requiring many hundreds of amperes and having an inductance of ≈ 100 nH, multiple kV between the coil terminals is required to achieve the required power delivery to the silicon load in industrial FZ processes.

Arcing protection The need for high frequency current in the work coil and consequently high terminal voltage seen from (2.4) is accompanied by the risk of electric breakdown of the atmosphere in the growth chamber causing arcing [43]. This is especially critical in the high electric field area around the main slit in Fig. 2.1. A small amount of nitrogen is commonly added to the argon atmosphere to reduce the risk of arcing, and using high chamber pressure can increase the breakdown strength of the gas [46]. However, the pressure must be balanced with the growth requirements as higher pressure also promotes convective cooling, increasing the thermal stresses of the growing crystal. In general, avoiding arcing is a key challenge in growing large diameter crystals by the FZ process [2], and since arcing is a relatively common occurrence, the developed generator must be tolerant to this type of event.

Load variation and frequency tracking A common element of induction heating processes is that the equivalent resistive load can vary in a wide range [47], [48]. Although dependent on the specific system, the generator must generally be able to supply the required power during all phases of the growth process. Therefore, a closed loop control scheme with fast response to resistive and inductive loading changes is required for efficient generator operation and sufficient process control. While these consideration of process control opportunities are important in the system design, the development of the closed loop control scheme for the generator is outside the scope of this project.

All the features required for the solid state generator for the FZ process are summarized in table 2.2, along with features that are preferred for a commercial system.

Table 2.2: Requirements and preferred features for a generator for the float zone process.

Parameter	**Requirement**	**Notes**
Output power level	Several tens of kW	Dependent on ingot diameter
Working frequency	2-3 MHz	Variable frequency required
Coil terminal voltage	Multiple kV	Dependent on ingot diameter
Arcing protection	Yes	Should allow fast restart of process
Load variation	Unloaded to full load	Dependent on chamber preheating system
Frequency tracking	Yes	Fast resonance frequency tracking in closed loop
Preferred features		
Inverter components	Off-the-shelf devices	Important for security of supply
Galvanic isolation	Low loss transformer	Low frequency preferred, requires high voltage switches
Power regulation	Fast and flexible variability	Desired for improved process controllability
RF noise robustness	Control system immunity	Adherence to EMC regulation

2.2 Terminology and switching concepts

In order to provide a discuss the possibilities for a solid state inverter that meets the criteria in the previous section, a few relevant power electronic concepts are briefly revisited below.

2.2.1 Wide band gap devices

The ideal switching device that is capable blocking infinite voltage in the OFF-state, has zero resistance in the ON-state, and can instantaneously switch between the two states does not exist. Instead, real semiconductor devices have parasitic resistances, capacitances, and inductances, as shown in Fig. 2.2. For enhancement mode FETs the device works as a switch controlled by the gate voltage ν_{gs} when operated in the ohmic region. When the gate voltage is larger than the threshold voltage $\nu_{\mathrm{gs}} > V_{\mathrm{th}}$ the device is in the ON-state and behaves as a lumped resistor with some nominal value $R_{\mathrm{ds,on}}$. The gate-drain capacitance C_{gd} and the drain-source capacitance C_{ds} are highly non-linear under varying drain-source voltage ν_{ds} while C_{gs} is constant [49]. In device datasheets, these capacitors are commonly represented by the following terminol-

ogy: input capacitance $C_{\text{iss}} = C_{\text{gs}} + C_{\text{gd}}$, output capacitance $C_{\text{oss}} = C_{\text{ds}} + C_{\text{gd}}$, and reverse-transfer capacitance $C_{\text{rss}} = C_{\text{gd}}$.

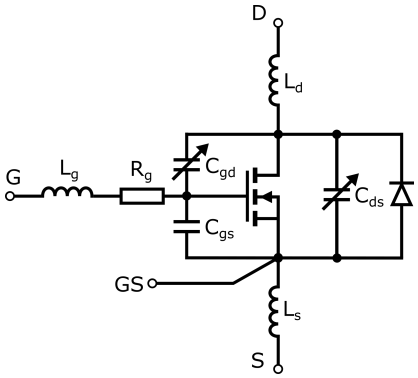


Fig. 2.2: Circuit schematic of a switching MOSFET including the parasitic capacitances. The three main terminals of the device are the drain (D), source (S), and gate (G) terminals, and the (GS) terminal is an optional auxiliary source connection for decoupling the gate loop from the power loop. With the exception of the body diode, any FET will have a similar parasitic layout. Here, R_{g} is the internal device gate resistance, and the inductances from the interconnections shown may be inside the package for discrete devices.

The parasitic elements, and in particular the parasitic capacitances, are highly important to the switching properties of the device, and even more so for high switching frequencies and higher power devices [37], [50]. The possibility for reduction of these device parameters is a major attraction of WBG device technology. The wide band gap results in several beneficial material properties, the most important of which is the higher critical field E_{c}, which is the maximum field strength the material can withstand before the onset of avalanche breakdown [51]. Some of the advantages resulting from this feature in unipolar WBG devices are illustrated in Baliga's Figure of Merit (BFOM) [52], which is concerned with the drift region resistance, and Baliga's High Frequency Figure of Merit (BHFFOM) [53], in which the product of resistance and input capacitance are assessed

$$R_{\text{on,sp}} = \frac{4V_{\text{br}}^2}{\epsilon_{\text{r}}\mu_{\text{n}}E_{\text{c}}^3} \Rightarrow \text{BFOM} = \epsilon_{\text{r}}\mu_{\text{n}}E_{\text{c}}^3 \tag{2.5}$$

$$\frac{1}{R_{\text{on,sp}}C_{\text{in,sp}}} = \frac{1}{2}\mu_{\text{n}}E_{\text{c}}^2V_{\text{G}}^{1/2}V_{\text{br}}^{3/2} \Rightarrow \text{BHFFOM} = \mu_{\text{n}}E_{\text{c}}^2 \tag{2.6}$$

where $R_{\text{on,sp}}$ is the specific on-state resistance, V_{br} is the breakdown voltage, ϵ_{r} is the relative permittivity, μ_{n} is the electron mobility, E_{c} is the critical electric field, V_{G} is the gate voltage, and $C_{\text{in,sp}}$ is the specific input capacitance. These FOMs illustrate the tradeoffs between voltage ratings, die area, on-state losses, and switching performance based on ideal material parameters, and are

presented for Si, SiC, and GaN in table 2.3. The higher FOMs for SiC and GaN indicate a larger power handling capability and better high frequency performance for a device of a given die area and voltage rating.

Table 2.3: Key material parameters for semiconductors for fast-switching power components [Paper A].

	Silicon	4H-SiC	GaN
Band gap, E_g [eV]	1.12	3.23	3.39
Critical E-field, E_c [MV/cm]	0.3	2.5	3.75
Relative permittivity, ϵ_r	11.7	9.66	8.9
Electron mobility, μ_n [cm^2/Vs]	1350	900	1265
BFOM (rel. to Si)	1	319	1392
BHFFOM (rel. to Si)	1	46	146

2.2.2 Switching operation

One of the most important parts of high frequency power conversion is the minimization of switching losses. This is because the losses associated with the switching of semiconductor devices scale linearly with the switching frequency and, neglecting driving losses, can be written as

$$P_{sw} = (E_{on} + E_{off}) f_{sw} \tag{2.7}$$

where E_{on} and E_{off} are the turn-on and turn-off switching energies, respectively. While the magnitude of these losses is generally dependent on complex interactions between the parasitic elements of the components in the circuit [1], [54], it is in most cases necessary for MHz switching of higher voltage components that the switching losses are mitigated through soft switching methods to avoid the concurrency of switch voltage and current during the switching transitions [29], [41]. This can be achieved either through zero voltage switching (ZVS) or zero current switching (ZCS). ZVS ideally eliminates E_{on} by ensuring that $\nu_{ds} = 0$ prior to turn-on, while ZCS eliminates E_{off} by letting the device channel current $i_{ch} = 0$ before and during turn-off. The former is more suitable for high frequency operation of FETs, as generally $E_{on} > E_{off}$ and ZVS eliminates the losses associated with hard switching of the output capacitance equal to $\frac{1}{2} f_{sw} C_{oss} \nu_{ds}^2$ [1], [55], [56]. The way in which soft switching is achieved, and the corresponding waveforms, depend on the circuit topology. An illustrative example of hard- and soft switching waveforms is shown in Fig. 2.3.

The turn-off losses under ZVS conditions may be written as [57]

$$E_{off} = \int_{t_1}^{t_2} \nu_{ds}(t) i_{ch}(t) \mathrm{d}t \tag{2.8}$$

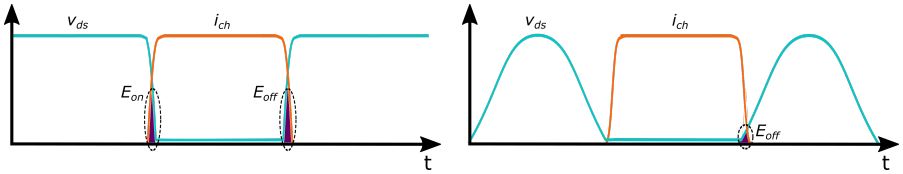


Fig. 2.3: Simplified examples of switch voltage and current during switching events. (a) Hard switching, (b) ZVS soft switching.

where t_1 and t_2 are the beginning and end of the overlap time, respectively. In some resonant circuits a low turn-off switch voltage and low E_{off} is naturally achieved [58], while in others this loss can be minimized by using fast switching devices such that the time period $t_2 - t_1$ is very short. The channel current cut-off speed is primarily controlled by the gate driver, meaning that for a compact gate layout and fast WBG devices, very fast turn-off transitions and nearly zero total switching loss can be achieved using low inductive gate loops and gate drivers with high current capability [55], [59]. Using these techniques with suitable switching devices and circuit topologies, MHz inverter systems can therefore be realized.

2.3 Circuit topologies

The choice of circuit topology of the inverter for the generator system is highly important to the performance and efficiency of the system. As was mentioned in chapter 1, traditional RF amplifier circuits used for vacuum tube generators such as Class A, B, or C have too low operating efficiencies to be useful solutions for the solid state generator. However, as switch-mode inverters with traditional hard switching power devices are also not feasible circuit topologies, circuits allowing soft switching of the power devices are necessary. This can be achieved using e.g. quasi-resonant inverters where reactive components are used in normally hard-switched converters to achieve ZVS or ZCS at the expense of increased component count, higher device stress, and/or higher conduction losses [1], [58], [60]. For induction heating systems, and in RF power conversion systems, resonant inverters (or, equivalently, switched-mode power amplifiers) are typically used for applications requiring high efficiency. In these circuits, soft switching is achieved by utilizing the load network to shape the switch voltage and current. Implementations of these inverters in recent literature were overviewed in section 1.1 and here a brief overview of the topologies will be given with special attention to aspects relevant to MHz induction heating processes.

The selection of inverter circuit topology is dependent on many criteria

established by the application. One of the important metrics is the utilization factor of the switches, that is, the amount of output power that the amplifier generates for a given transistor stress [61]

$$c_{\mathrm{pmr}} = \frac{\eta_{\mathrm{D}} V_{\mathrm{dc}} I_{\mathrm{dc}}}{N V_{\mathrm{ds,p}} I_{\mathrm{ds,rms}}} \tag{2.9}$$

where η_{D} is the switch drain efficiency. This equation is useful as a basic benchmark for comparing different resonant inverter topologies since a circuit with higher c_{pmr} allows higher output power for the same power loss for the utilized switching devices. The switch utilization is compared in table 2.4 for selected resonant inverter topologies.

Table 2.4: Comparison of device stresses for resonant inverter topologies, assuming $\eta_{\mathrm{D}} = 1$. The 'half bridge' is the standard non-resonant ideal half bridge inverter with square switch voltage and current waveforms.

Class	$V_{\mathrm{ds,p}}$	$I_{\mathrm{ds,rms}}$	N	c_{pmr}
Half bridge	1	1.41	2	0.35
D, VSRI	1	1.57	2	0.32
DE (D = 0.25)	1	3.14	2	0.16
D, CSRI	3.14	0.71	2	0.23
E	3.56	1.54	1	0.18
EF_2 / Φ_2	2.1	1.9	1	0.25
E, push-pull	3.56	0.77	2	0.18

In systems where the semiconductor device cost is a critical factor, the c_{pmr} may be the highest weighted optimization parameter in the inverter design, whereas in other applications the device cost may be dwarfed by e.g. cost of auxillary components or costs associated with reduced process uptime in the case of inverter failure. In these applications the reliability of the inverter, reduced EMI, or simplicity of the topology may be prioritized over switch utilization, and therefore determining the most suitable topology for a given application is not trivial. The circuit schematics corresponding to the topologies in table 2.4 are shown in Fig. 2.4 with descriptions below.

Class D VSRI, Class DE, and LLC The basic Class D voltage source resonant inverter (VSRI) is a standard half bridge circuit connected to a series resonant tank at the output as shown in Fig. 2.4a. The voltage across the switches is a square wave that is filtered by the resonant circuit to produce a sinusoidal output current for high quality factors $Q = |P_{\mathrm{react}}|/P_{\mathrm{real}}$. In this topology high c_{pmr} is achieved for a duty cycle $D = 0.5$ (or slightly less to avoid shoot-through), but the energy stored in the switch output capacitance is discharged through the channel each switching cycle, leading to a switching loss that makes high frequency operation unfeasible. By using significant dead

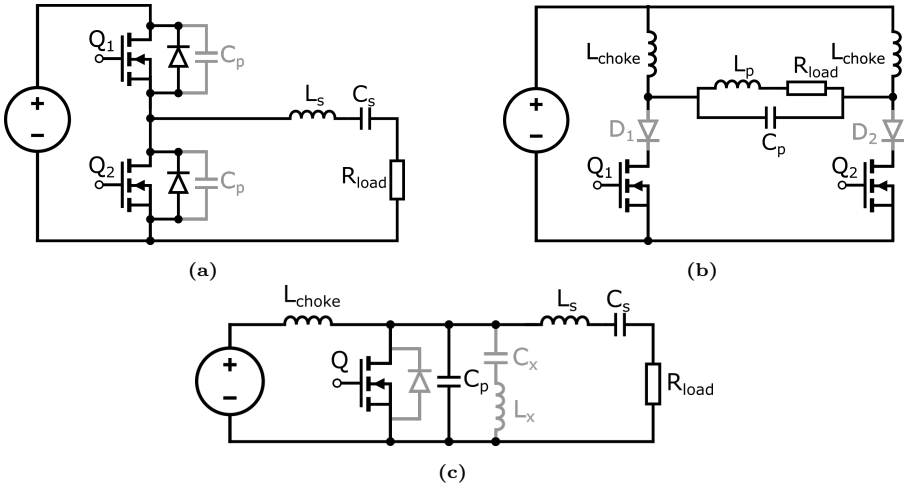


Fig. 2.4: Ideal circuits schematics of load resonant inverters suitable for MHz operation. (a) Class D voltage source resonant inverter (VSRI) with series resonant tank and optional parallel switch capacitance, although in practice some switch capacitance is unavoidable for any inverter. (b) Class D current source resonant inverter (CSRI) with parallel resonant tank and optional series diode. (c) Class E inverter with optional antiparallel diode. The switch utilization in the topology may be improved by additional resonant components in the tank circuit.

time and operation with inductive load, and possibly including external switch capacitance, ZVS can be achieved by charging and discharging C_{oss} using the load current. This reduces the c_{pmr} of the circuit, but allows the switches to turn on with ZVS during body diode conduction to achieve high operating efficiency, and by tuning the reactive parameters, specific operating points can be found where the current through the switch is zero at turn on resulting in zero voltage derivative switching (ZVDS), which is the Class DE operating condition [62], [63].

An appealing variation of the VSRI, which is common in induction heating systems, is achieved by modifying the load network into a series-parallel resonant tank such that it becomes an LLC resonant inverter [47], [64]. This variation is attractive due to, compared to the VSRI, load short-circuit handling capability and in particular the current gain of the parallel resonance tank. As argued in section 2.1, the required current level in the induction coil is many hundreds of Amperes, which is much higher than is desirable to switch in a MHz inverter. By employing a parallel resonant tank with a large current gain, the required transistor current is dramatically reduced without using an impedance matching network with large transformation ratio [65].

The drawbacks of the topology for MHz frequencies are mainly related to the switching potential of the source terminal of the high side switch, as it

means the driving signal must be level shifted for the high side switch while maintaining synchronization with the low side switch. This can be a challenge at high frequency and voltage levels, and therefore the high side driver must have a large common mode transient immunity [34]. These considerations, along with parasitic inductance in the switching loop and the fact that the required dead time may be a significant fraction of the switching period for high frequencies, can make practical implementations of this topology difficult for multi-MHz inverters [32], [66].

Class D CSRI The circuit of the Class D current source resonant inverter (CSRI) is shown in Fig 2.4b. As the dual of the VSRI, in the CSRI the current input to the tank network is a square wave and the voltage is a half sine. The large choke inductors ensure constant current draw from the source. The series diodes are optional when the switches are operated at the resonance frequency of the tank circuit [58], and the implication of including them in the topology is discussed in chapter 3. Like the VSRI, the CSRI has been extensively used for induction heating systems in the kHz regime. The CSRI naturally incorporates a parallel resonant tank with inherent current gain such that the switches ideally only carry the active current in the circuit. This leads to the conventional wisdom for induction heating systems that voltage source inverters are best suited for high impedance coils, while current source inverters are best suited for low impedance coils with high reactive current requirements [67], [68].

In terms of utilization factor, however, the CSRI is not the dual of the VSRI. This is because, from a device perspective and considering only conduction losses, the inverter power is limited by the *peak* of the transistor voltage, whereas it is mainly limited by the *RMS* of the transistor current through the heat dissipation capacity of the semiconductor devices. In spite of this, the topology is inherently attractive for high efficiency RF amplifiers as it has the important advantage for high frequency operation that any parasitic switch parallel capacitance is naturally absorbed into the resonant tank [69], [70]. In addition, since the gates of the both switching devices are referenced to the same potential, there is no high side switch in this topology, and it therefore requires no level shifting.

Class E and derivatives The Class E amplifier was invented as a high efficiency alterative to linear transistorized amplifiers [71]. The basic circuit is shown in Fig. 2.4c. In nominal operation, the circuit elements are precisely tuned for a specific frequency and load such that the conditions for both ZVS and ZVDS are satisfied:

$$\nu_{\mathrm{ds}}(2\pi) = 0, \qquad \left.\frac{\mathrm{d}\nu_{\mathrm{ds}}(\omega t)}{\mathrm{d}\omega t}\right|_{\omega t = 2\pi} = 0 \tag{2.10}$$

Because there is no current running through the switch at the switching instant, the ZVDS condition can ensure that device losses are low even for slow or

mistimed gate signals [34]. In this condition, the antiparallel diode is not required.

Like the CSRI, the standard Class E resonant inverter includes a choke inductor and also incorporates the switch C_{oss} in the resonant network. In addition, parasitic inductance at the input is absorbed by the choke inductor, and parasitic output inductance may be part of the resonant network. The topology includes only a single switch, which avoids problems with timing synchronization at high frequencies, and has the switch gate referenced to ground. Because both the voltage and current are shaped by resonant elements, the Class E inverter has no steep voltage or current flanks which helps to reduce electromagnetic interference (EMI), reduce stress on passive components, and may improve efficiency as steeper voltage transients can increase device operation losses [16], [72].

The largest disadvantage of the Class E topology is the low c_{pmr}. There are several ways this property may be improved, e.g. by shaping the switch current in the Class E push-pull topology to approach the CSRI square wave current waveforms [61], or through topology modifications to the reactive elements such as Class EF_x [33], [73], or Φ_2 [66], [74]. These modifications may be applied to improve the switch utilization at the expense of increased complexity [73].

2.4 Inverter implementation challenges

For any choice of circuit topology, the combination of the requirements from table 2.2 results in a challenging inverter system design for this application. A brief overview of some of the most important challenges is given below.

2.4.1 Switching devices

The choice of switching device material, device technology, package, and voltage and current rating for high frequency applications is dependent on many factors, including operating frequency and environment, cost, and reliability and power density requirements [35], [41], [75]. Both SiC and GaN devices may be applied to resonant high frequency inverters for induction heating [19], [76], and in general to MHz converters as was shown in table 1.1. However, even without considering practical layouts and operating efficiencies, the maximum theoretical operating frequency of any semiconductor device is limited by its RC-network of R_{g} and C_{iss} as

$$f_{\max} = \frac{1}{4R_{\text{g}}C_{\text{iss}}} \tag{2.11}$$

The maximum operating frequency for a device type is thus, in rough terms, inversely proportional to its voltage rating, as can be noted through the similarity between (2.11) and BHFFOM (2.6), but these parameters are highly

dependent on the intended application regime of the designed device. For high frequency and power applications, the device nonidealities therefore become vitally important. These considerations are evident by considering the selected WBG devices with low $R_{\mathrm{ds,on}}$ in table 2.5, which also highlights the inherent challenge in high frequency operation of medium voltage devices.

Table 2.5: Characteristics and maximum theoretical operating frequency of selected WBG power devices, each with low on-state resistance for its voltage class. Expanded from Paper A.

Device	Type	V_{br}	$R_{\mathrm{ds,on}}$	C_{iss}	R_{g}	f_{max}
SCT3040KL	SiC MOSFET	1200 V	40 mΩ	1337 pF	7 Ω	27 MHz
C2M0080170P	SiC MOSFET	1700 V	80 mΩ	2250 pF	2 Ω	56 MHz
UJ3N120070K3S	SiC JFET	1200 V	70 mΩ	985 pF	3.3 Ω	77 MHz
GS66508T	GaN HEMT	650 V	50 mΩ	260 pF	1.1 Ω	874 MHz
GPI65060DDK	GaN HEMT	650 V	25 mΩ	420 pF	2.18 Ω	273 MHz
G2R50MT33-CAL	SiC MOSFET	3300 V	50 mΩ	7301pF	1.2 Ω	29 MHz
10 kV die [77]	SiC MOSFET	10000 V	N/A	5800 pF	3.7 Ω	11.6 MHz

For MHz switching frequencies it is important to note the additional challenge that the charging and discharging of C_{oss} is not lossless [41], [78]. Recent investigations reveal different loss mechanisms for different device types as well as varying scaling factors for frequency and voltage, and that for high efficiency soft switched MHz inverters these losses may cause significantly increased device stresses [16], [35], [79]. These losses are not considered quantitatively for the work in this thesis, but their existence is noted for derating considerations of selected switching devices.

2.4.2 Power scaling and paralleling

At the required power and voltage levels the paralleling of multiple switching devices is necessary both for medium voltage devices with low current rating and for a transformer-based solution utilizing lower voltage devices. Generally, barring difference between devices, higher power handling capability means larger total device capacitances, no matter if the power level reached through a few large-area devices or many smaller devices, as is also shown in table 2.5. From (2.11) a higher C_{iss} limits the maximum switching frequency, but it also increases the required gate drive power and peak current levels to achieve fast switching speed of the power devices [80]. For ZVS resonant inverters, only the gate charge related to ZVS, $Q_{\mathrm{g,ZVS}} \approx C_{\mathrm{iss}}\Delta V_{\mathrm{g}}$ is relevant [59]. Thus for a hard-switched gate driver controlling a soft switched power device, the required amount of driving power is at least

$$P_{\mathrm{g}} = C_{\mathrm{iss}} f_{\mathrm{sw}} \Delta V_{\mathrm{g}}^2 \tag{2.12}$$

Additional driver related losses are present in actual gate driving operation. As is evident from these considerations an increased power level results in a more difficult construction of a high-side driver with low coupling capacitance, particularly for higher operating voltage, since the gate driver power supply needs to supply significant power [81]. Thus from a gate driving point of view, it is therefore important to note the significant difference in driving power requirements for GaN HEMTs and SiC MOSFETs, as GaN devices require significantly less driving power. This is in part due to lower input capacitance, but mainly because these devices are typically operated at levels around 6 V [35]. Compared to the driving voltage of $\Delta V_{\mathrm{g}} = 20$ V that it typical for SiC MOSFETs, from (2.12) this alone accounts for more than 11 times higher driving losses for SiC than for GaN. Advanced gate driver structures such as resonant gate drives may be employed to improve the driving performance for high power FETs at MHz frequency [34], [39], [40].

Another inherent challenge associated paralleling is the static and transient current sharing between dies, gate drive and power loop symmetries, and variance between devices. For the CPM2-1700-0080B SiC MOSFET devices used for most of the experimental work in this thesis (the bare die version of the C2M0080170P from table 2.5) [82], 12 dies are compared for output and tranfer characteristics in Fig 2.5. In overall terms these measurements confirm the datasheet values, although a significant spread in the values of $R_{\mathrm{ds,on}}$ is observed in Fig. 2.5b. The issue of static current balancing is fortunately largely resolved for devices exhibiting a positive temperature coefficient of the resistance [83]. In contrast to $R_{\mathrm{ds,on}}$ the threshold voltage V_{th} has a negative

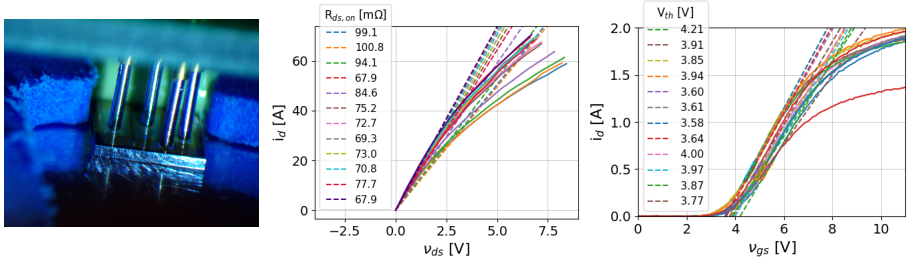


Fig. 2.5: Curve tracing measurements for characterization of MOSFET dies. (a) Photograph of a bare die in the probing station. (b) Output characteristics and fitted $R_{\mathrm{ds,on}}$ at $\nu_{\mathrm{gs}} = 20$ V and $T_{\mathrm{j}} = 25\ ^{\circ}C$. As in the datasheet, the fit intersects the curves at $i_{\mathrm{d}} = 28$ A. (c) Transfer characteristics and fitted V_{th} at $T_{\mathrm{j}} = 25\ ^{\circ}C$. The datasheet threshold voltage is defined as the ν_{gs} value where the current level is 10 mA, requiring milli-ampere measurement precision. Here, we instead determine V_{th} from the data in the linear region on the $i_{\mathrm{d}}/\nu_{\mathrm{gs}}$ curve for $\nu_{ds} = 1$. V_{th} is then the zero-current intercept of the fit of this data under the linear approximation for the drain current $i_{\mathrm{d}} = k\left((\nu_{\mathrm{gs}} - V_{\mathrm{th}})\nu_{\mathrm{ds}} - \frac{\nu_{\mathrm{ds}}^2}{2}\right)$ [1], where k is a constant depending on the physical design and parameters of the MOSFET.

temperature coefficient, so the observed spread in Fig. 2.5c can potentially result in imbalance in the dynamic losses, particularly for elevated operation temperatures[1] [84]. A compact gate loop should be employed to avoid false turn on of the MOSFETs due to low threshold voltage [39], which can also reduce transient current sharing imbalance between devices with varying threshold voltage [85], [86].

2.4.3 Switching stage layout

The layout of the switching stage and minimization of parasitic elements are highly relevant for realizing the potential of fast-switching WBG components [87]–[89]. Fast switching can be achieved both for systems using discrete packaged devices and power module designs, but in all cases require careful consideration current loops, coupling paths, and geometrical and device capacitances [36]. For discrete devices this is particularly true as the package may be the limiting factor for the reasonable operating frequency of the device rather than its own characteristics [35], [37], [38]. Different topologies have different inherent sensitivities to each parasitic element depending on inverter operation and application, and the optimization of the layout is therefore aimed at different parasitic parameters. As a relevant example, the VSRI is highly sensitive to inductance between the DC capacitor bank and the switches, while for the CSRI (as will be discussed further in 3.1.1) the output inductance of the switching stage is the parasitic element requiring most consideration [67].

Concerning the driving stage, it is well known that for any hard switched gate driver the circuit layout should be compact to facilitate fast transitions and minimize voltage overshoots on the power device gate. Considering an ideal step input to the gate circuit, the dynamic response of the gate voltage may be estimated from [77], [90]

$$L_{\mathrm{g}} = \frac{C_{\mathrm{iss}} R_{\mathrm{g}}^2}{4\zeta^2} \tag{2.13}$$

where R_{g} is the gate resistance and ζ is the damping factor. For $\zeta = 1$ a critically damped response is achieved, so (2.13) limits the gate loop inductance in relation to the power device parameters. For fast switching devices this consideration competes with (2.11), and as the allowed inductance scales with the square root of R_{g} which is in parallel for each device, achieving a low enough inductance to avoid voltage overshoot can be a significant challenge for paralleled power devices.

In addition, it is not only the compactness of the loops that is necessary to consider, but for paralleled devices achieving symmetry in gate- and power loops to best utilize the device ratings of each device and promote equal transient

[1] The temperature dependence of the bare dies was similarly confirmed by curve tracing, where no significant deviation from the datasheet values was found.

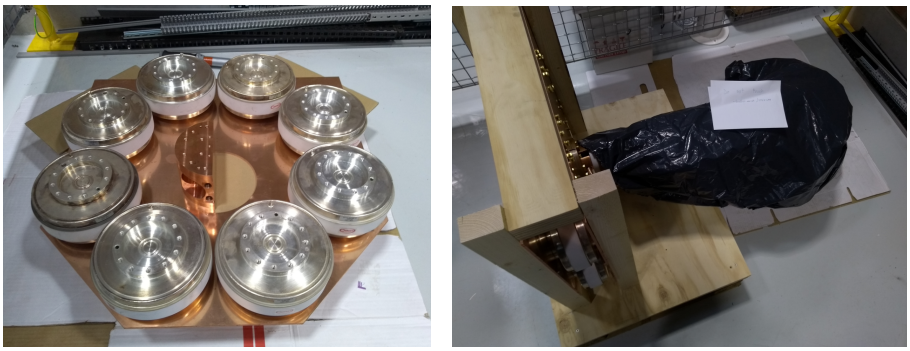
current sharing is also highly important [39], [86]. This is particularly true at high switching frequency where any transient imbalance may be more critical [83].

2.5 Resonant tank

Experimental testing of the developed inverters in a realistic environment is an important part of validating the technology in a relevant setting. Therefore, an experimental setup with high power and voltage capability was constructed to emulate a real FZ process, with a resonant tank system based on similar components to those in vacuum-tube generators in use for FZ processing.

The induction coil is a specialized component that closely mimics an operational FZ coil, and a steel load was used in place of molten Si due to the similar resistivities of these materials. To increase the work coil current a compensating capacitor bank was added to form a parallel resonant tank. Vacuum capacitors were chosen due to their very low ESR and their ability to handle many hundreds of amperes and several kilovolts. The drawback of these components is their large size making compact resonance loops difficult to construct, which due to the high operating frequency can limit the voltage at the coil terminals and thus lower the power delivered to the load at a given capacitor voltage as described in section 2.1.

The constructed resonant tank is shown in Fig 2.6. As is shown in Fig. 2.6a the vacuum capacitors are arranged in a circular pattern where the inverter power module output terminals are to be connected on the left side of the capacitor bank in Fig. 2.6b and the induction coil is on the right.



(a) **(b)**

Fig. 2.6: Photographs of the resonant tank, with (a) the capacitor bank with 8 vacuum capacitors in parallel for a total capacitance of 40 nF and (b) the complete resonant tank including proprietary induction coil mounted in a wooden chassis.

The circular shape is due to the importance of the resonance loop being

as symmetrical as possible to ensure optimal usage of the capacitor ratings, increase the quality factor of the tank, avoid unwanted oscillations, and reduce the harmonic content of the current in the induction coil to improve process control and reduce the risk of arcing.

The impedance spectrum of the resonant tank is shown in Fig 2.7a. Here, except for a series resonance loop around 4 MHz, a sharp and nearly featureless parallel resonance f_{res} is observed at around 2.2 MHz for the no load condition, which demonstrates the inductively balanced layout. Only at much higher frequency a resonance related to the parasitic capacitance of the induction coil C_{c} is observed at around 45 MHz. The current in the inductance coil, if the tank is driven near the resonant frequency, is thus expected to be nearly sinusoidal.

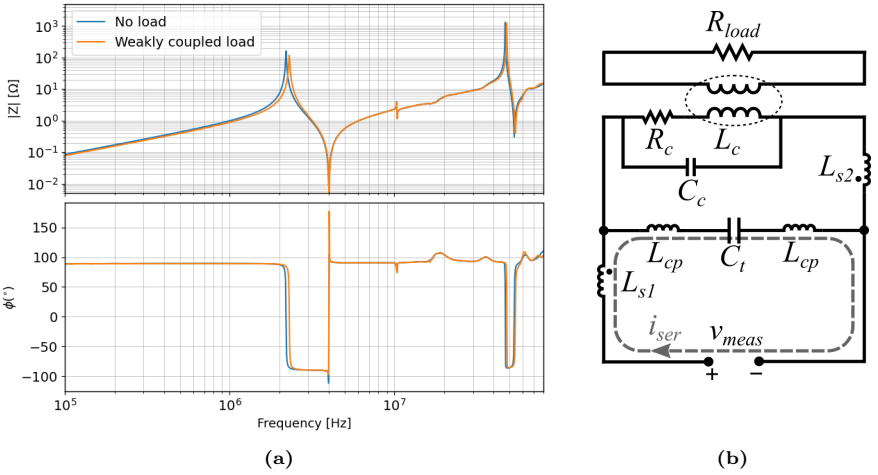


Fig. 2.7: Electrical parameters of the constructed resonance tank. (a) Impedance seen from the input of the tank measured with a Keysight E4990A impedance analyzer. Without any load, the constructed tank has a resonance frequency of around 2.2 MHz, which may increase up to around 3 MHz at full loaded conditions (steel load very close to the coil). (b) Circuit schematic of the tank with the major parasitic elements and series resonance illustrated. L_{s1} and L_{s2} are highly coupled. Subscript c elements are related to the induction coil which may couple to a load.

In practice, the voltage measured at the resonant tank terminals will be slightly lower than the actual capacitor voltage due to two types of parasitic inductance which are illustrated in the tank circuit model in 2.7b. First, the height of the capacitors results in some circularly symmetric inductance L_{cp} in series with the capacitors, so the apparent capacitor voltage measured at the capacitor bank centre terminals will be lower even though this is limited by the busbar-like design. Secondly, the magnetic flux from the inductance of the two copper blocks $L_{\mathrm{s}(1,2)}$ bridging the capacitor bank is closely coupled, but one of them is not part of the parallel resonance circuit while the other is. These blocks will have a similar voltage drop across them but of opposite polarity to

the measured tank voltage, which also contributes to a lower apparent capacitor voltage. In addition to these effects, it is highlighted in 2.7b how the mentioned inductances also form the main inductive elements of the series resonance loop observed around 4 MHz in Fig 2.7a.

The presented resonant tank is used in testing and demonstration of the inverter systems throughout the rest of this thesis.

Chapter 3

Current source resonant inverter development

Based on the discussions in chapter 2, the CSRI is a promising candidate for an FZ process inverter topology. In this chapter, this statement is investigated through the design, manufacture, and testing of power modules suited for the CSRI topology utilizing paralleled 1700 V SiC MOSFETs for MHz operation. Much of the results and discussion in this chapter is published in paper B. This chapter will recap this work and provide additional practical and technical details on the inverter development.

To analyse the design parameters for a CSRI incorporating a low impedance and high power work coil, key parts of the topology and the impact of parasitic elements are outlined below. As was shown in Fig. 2.4, the CSRI may employ series diodes to create unidirectional switches which is the traditional configuration for low frequency applications [58], [67], while another option is using the CSRI topology without the series diodes making the switch bidirectional, as is common for RF amplifiers [70], [91]. A disadvantage of omitting the diodes is that the power level cannot be controlled through the switching frequency, but must instead be regulated through the input current. The advantages, however, besides the reduced component count and cost, is that if switching operation at the resonant frequency is desired, one avoids the additional losses from the forward voltage of the diodes, which is larger than 1 V for SiC JBS diodes, and the introduction of additional loop inductance, both of which are detrimental when operating at the resonance frequency. In addition, even an ideal diode has adverse effects on the MOSFET efficiency for $f_{\mathrm{sw}} = f_{\mathrm{res}}$ when considering its parasitic capacitance as the diode prevents the discharge of C_{oss} of the MOSFET after the voltage across the switch reaches its peak value, resulting in additional switching loss, which is particularly important at high voltage and switching frequency [92].

3.1 Inverter operation

In the CSRI, the input inductors L_{choke} are much larger than the resonant inductor L_{c}, so in steady state the DC current is constant and the input current to the resonant tank is a square wave. Due to its simple structure, the analysis of the CSRI is straightforward and can be viewed as a parallel resonant circuit fed by a current source, as shown in Fig. 3.1.

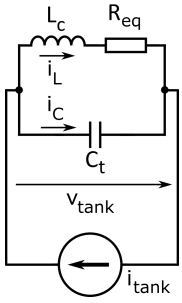


Fig. 3.1: Schematic of the idealized equivalent circuit diagram of the bidirectional CSRI inverter. [Paper B]

The work coil is modelled as an inductance L_{c} in series with an equivalent resistance R_{eq}, which includes both the coil resistance and the resistance of the work piece referred to the coil. The quality factor of the coil is defined as the ratio of reactive to real power

$$Q = \frac{|P_{\text{react}}|}{P_{\text{real}}} = \frac{\omega L_{\text{c}}}{R_{\text{eq}}} \tag{3.1}$$

Considering the circuit in Fig. 3.1 where to coil forms a parallel resonant circuit with tank capacitance C_{t}, the input current to the resonant tank is found by KCL in the Laplace domain is

$$i_{\text{tank}}(t) = i_{\text{Ct}} + i_{\text{Lc}} \;\Rightarrow\; i_{\text{tank}}(s) = sC_{\text{t}}V_{\text{tank}} + \frac{V_{\text{tank}}}{sL_{\text{c}} + R_{\text{eq}}} \tag{3.2}$$

Defining the undamped natural resonance frequency ω_{n} and the damping ratio ζ

$$\omega_{\text{n}} = \frac{1}{\sqrt{L_{\text{c}}C_{\text{t}}}}, \quad \zeta = \frac{R_{\text{eq}}}{2}\sqrt{\frac{C_{\text{t}}}{L_{\text{c}}}} \tag{3.3}$$

gives the impedance

$$\begin{aligned} Z(s) = \frac{V_{\text{tank}}(s)}{I_{\text{tank}}(s)} &= \frac{sL_{\text{c}} + R_{\text{eq}}}{s^2L_{\text{c}}C_{\text{t}} + sC_{\text{t}}R_{\text{eq}} + 1} \\ &= (sL_{\text{c}} + R_{\text{eq}})\frac{\omega_{\text{n}}^2}{s^2 + 2\zeta\omega_{\text{n}}s + \omega_{\text{n}}^2} \end{aligned} \tag{3.4}$$

which is the expression for a second order system. By transferring this to the frequency domain, the impedance becomes

$$Z(s)|_{\mathrm{s=j}\omega} = \frac{R_{\mathrm{eq}}}{(1-\omega^2 L_{\mathrm{c}} C_{\mathrm{t}})^2 + (\omega C_{\mathrm{t}} R_{\mathrm{eq}})^2} + j\frac{\omega(L_{\mathrm{c}} - \omega^2 L_{\mathrm{c}}^2 C - C_{\mathrm{t}} R_{\mathrm{eq}}^2)}{(\omega C_{\mathrm{t}} R_{\mathrm{eq}})^2 + (1-\omega^2 L_{\mathrm{c}} C_{\mathrm{t}})^2} \tag{3.5}$$

ZVS is achieved when switching at the resonance frequency ω_{r}, which corresponds to an impedance phase angle of zero, yielding

$$\angle Z(j\omega_{\mathrm{r}}) = 0 \Longrightarrow \omega_{\mathrm{r}} = \sqrt{\frac{L_{\mathrm{c}} - C_{\mathrm{t}} R_{\mathrm{eq}}^2}{L_{\mathrm{c}}^2 C_{\mathrm{t}}}} = \omega_{\mathrm{n}}\sqrt{1-4\zeta^2} \tag{3.6}$$

For high Q-factors, the damping term becomes small and $\omega_{\mathrm{r}} \approx \omega_{\mathrm{n}}$. In this case, the magnitude of the impedance at the resonance frequency can be written from (3.5) as

$$|Z(\omega_{\mathrm{r}})|_{\omega_{\mathrm{r}}=\omega_{\mathrm{n}}} = \sqrt{\frac{L_{\mathrm{c}}(C_{\mathrm{t}} R_{\mathrm{eq}}^2 + L_{\mathrm{c}})}{C_{\mathrm{t}}^2 R_{\mathrm{eq}}^2}} = R_{\mathrm{eq}} Q\sqrt{Q^2+1} \tag{3.7}$$

For operation at the resonant frequency, the resonant tank acts as a filter allowing only the first harmonic of the square wave tank current. Considering this, the RMS value is expressed as

$$I_{\mathrm{tank}} = \frac{\sqrt{2}}{\pi} I_{\mathrm{in}} \tag{3.8}$$

Through a similar analysis to that for the impedance, the transfer function for the current at the resonant frequency, or current gain, can be found under the high Q-factor approximation [93]

$$\frac{I_{\mathrm{res}}(j\omega_{\mathrm{r}})}{I_{\mathrm{tank}}(j\omega_{\mathrm{r}})} = \frac{1}{1-\omega_{\mathrm{r}}^2 L_{\mathrm{c}} C_{\mathrm{t}} + j\omega C_{\mathrm{t}} R_{\mathrm{eq}}} = -jQ \tag{3.9}$$

Therefore under this assumption the power dissipated in the equivalent resistance R_{eq} can be found from (3.8) and (3.9) as

$$P_{out}(\omega_{\mathrm{r}}) = I_{\mathrm{res}}^2(\omega_{\mathrm{r}}) R_{\mathrm{eq}} = \frac{2 I_{\mathrm{in}}^2 Q^2 R_{\mathrm{eq}}}{\pi^2} \tag{3.10}$$

which, using that $P_{\mathrm{in}} = V_{\mathrm{in}} I_{\mathrm{in}}$, can be used to write the efficiency η through (3.7)

$$\eta = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} = \frac{2 I_{\mathrm{in}}}{\pi^2 I_{\mathrm{tank}}} \frac{V_{\mathrm{tank}}}{V_{\mathrm{in}}} \tag{3.11}$$

For lossless operation $\eta = 1$, the voltage transfer function from input voltage V_{in} to output voltage V_{tank} then becomes

$$\frac{V_{\text{tank}}}{V_{\text{in}}} = \frac{I_{\text{tank}}\pi^2}{2I_{\text{in}}} = \frac{\pi}{\sqrt{2}} \tag{3.12}$$

which results in the peak voltage for the resonant tank and the switching devices of πV_{in} as was shown in table 2.4.

3.1.1 Consideration of parasitic elements

The circuit analysis above with ideal components is modified significantly for high voltage devices switching at MHz frequency. In section 2.3 is was described how one of the large advantages of current source topologies for high frequency applications is the absorption of switch output capacitance into the resonant tank. The result of this, however, is that the conducting switch will carry the reactive current of the closed switch determined by

$$i_{\text{react}} = i_{C_{\text{tank}}} \frac{C_{\text{oss,eq}}}{C_{\text{tank}}} \tag{3.13}$$

Here $C_{\text{oss,eq}}$ is the charge-equivalent output capacitance of the MOSFET given by [94]

$$C_{\text{oss,eq}} = \frac{\int_0^{V_{\text{ds}}} C_{\text{oss}}(V)\mathrm{d}V}{V_{\text{ds}}} \tag{3.14}$$

The currents in the bidirectional CSRI considering the major parasitic elements are shown in Fig. 3.2. As can be seen from (3.9), the high Q-factor of the resonant tank means that a low input current is required even for high resonant current levels. The influence of the parasitic elements of the inverter

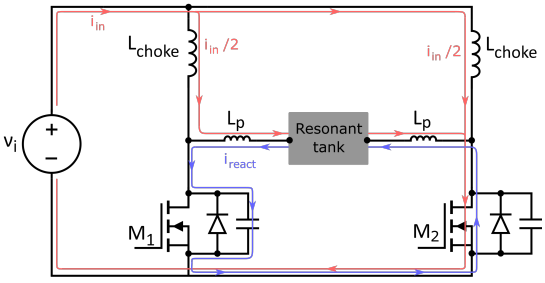


Fig. 3.2: Schematic of the CSRI illustrating additional reactive current path due to parasitic elements. [Paper B]

system is therefore most pronounced for light load conditions where the drain-source resonating current i_{react} may be of a level similar to that of the DC current, especially when utilizing paralleled higher voltage devices. In addition, due to the parasitic inductance in the i_{react} current loop, a high frequency resonance will be present with a frequency of

$$f_{\text{react}} = \frac{1}{2\pi\sqrt{2L_{\text{p}}C_{\text{oss,eq}}}} \tag{3.15}$$

For the presented system this resonance is only very weakly damped due to the loop consisting mostly of large copper planes, vacuum capacitors with low ESR, and MOSFETs with low values of $R_{\text{ds,on}}$. Therefore, these oscillations are easily sustained even if the magnitude of abrupt voltage changes across L_{p} are kept to a minimum.

In general, there are two overall ways in which L_{p} can be managed to avoid creating overvoltages that may result in switch failure. The most direct way is reducing this parasitic inductance to such a low value that it is inconsequential to the control of the semiconductors. The other approach is to introduce an overlap in the gating signals to allow for just enough time for the parasitic inductance current to change direction [95]. For an otherwise ideal CSRI, the overlap is given by

$$\beta = \cos^{-1}\left(1 - \frac{i_{in}\omega L_p}{V_p}\right) \tag{3.16}$$

This approach has the downside that the control of the inverter becomes increasingly dependent on both the resistive loading and the operating frequency, while worsening the transistor utilization factor c_{pmr}, as the real power injected into the resonant tank for the same operating conditions decreases [68]. Thus, for high frequency implementations of the CSRI, minimization of L_{p} is generally preferred.

To illustrate these points, the operation of a bidirectional CSRI inverter is simulated in LTSpice [96] and shown in Fig. 3.3. Reasonable values of the parasitic inductance and capacitances are chosen to model the envisioned MHz inverter system with compact resonant tank and paralleled switching devices, and the large influence of the parasitic parameters is readily observed between the two simulations. The general operation mode of the inverter can be conserved considering the parasitic elements by slight adjustment of the switching frequency and duty cycle. However, it is observed how the current from the capacitive current divider in (3.13) not only results in additional conduction losses for the switches, but also contains an oscillation component with a higher frequency determined by (3.15) that may cause EMI and control issues. Any deviation from optimal operating conditions will increase the amplitude of these

oscillations, which indicates that the operation of the real inverter system will be very sensitive to correct frequency tuning and timing of the gating signals.

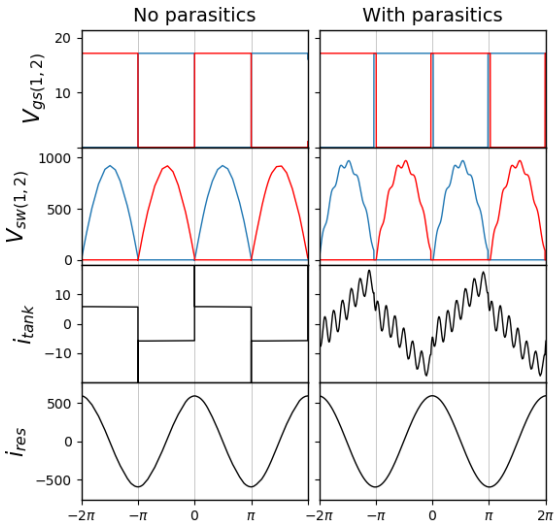


Fig. 3.3: Simulation of the impact of the most important parasitic elements on the CSRI inverter under relevant operating conditions. The CSRI is simulated with a 2.5 MHz resonant tank with a $Q \approx 80$, $V_{in} = 300$, and ideal switches. (a) ideal circuit with no parasitic elements (b) constant $C_{\mathrm{ds}} = 0.6\mathrm{nF}$ and $L_{\mathrm{p}} = 40\mathrm{nH}$ and overlap in the gate signals from (3.16). A small decrease in resonance frequency is evident from the inclusion of C_{ds} in the resonance loop, and a parasitic capacitance current i_{react} with a frequency of f_{react} and a magnitude determined by (3.13). [Paper B]

Therefore, the control for this inverter system is envisioned as a simple system that tracks the tank resonant frequency to lock the switching frequency at $f_{\mathrm{sw}} = f_{\mathrm{res}}$. This can be accomplished by phase-locked loop (PLL) or similar integral controllers, but these have inherent tradeoffs between dynamic tracking performance and steady-state frequency accuracy [97]. Therefore, during the start-up current ramp of the converter or during a transient event such as arcing, the switches may be exposed to high current or voltage stress which may damage the inverter [98]. Another option is to employ a self-oscillating circuit with direct feedback to track the resonance frequency, which has much improved dynamic response [30], [92]. In this approach the inherent propagation delays in the controller must be dynamically cancelled out under varying frequency to avoid phase errors, which may be challenging and require many components for high resolution tuning [97].

3.2 Power module design

The power module for the inverter was designed with the goal of (a) investigating the feasibility of a SiC-based CSRI as a basis for a FZ generator and (b) testing the performance of an integrated power module for MHz operation of paralleled 1700V SiC MOSFETs. Therefore, to demonstrate a flexible power module for a CSRI with the power capability to operate under a wide range of load conditions, the module was designed for power delivery up to 30 kW. The power devices chosen were CPM2-1700-0080B SiC MOSFETs measured in section 2.4.2. Considering switch voltage derating to $0.6 \cdot V_{\text{br}}$, from table 2.4 each leg should be capable of handling an RMS current of 70 A, and therefore paralleling of 4 devices was chosen for a reasonable loss margin for high frequency soft switched operation. The designed module is shown in Fig. 3.4

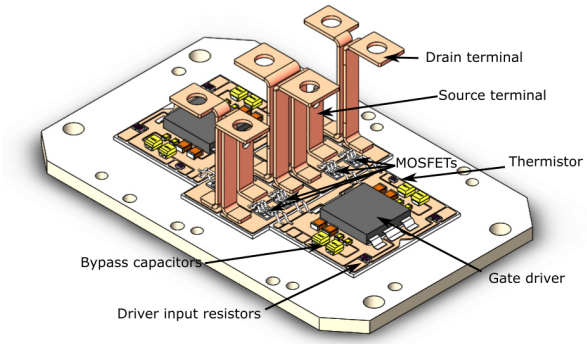


Fig. 3.4: Isometric view of the layout and component descriptions of the designed CSRI power module. [Paper B]

As discussed in section 2.4 one of the challenges presented for MHz inverters based on paralleled power devices is the sourcing and sinking of large currents for driving of the substantial input capacitance in low-inductive driving loops. For full flexibility in switching frequency a hard-switched topology is chosen where IXRFD630 high current totem pole gate drivers [99] are integrated into the power module for each switching leg. This same technique was applied in references [15], [100] and offers both very good thermal performance and low inductive driving loops, and it is well suited for the CSRI topology where the source terminals of both switches are referred to the same potential. For decoupling between power loop and gate loop, auxiliary source connections were used for each MOSFET.

3.2.1 Parasitic minimization

The power module was designed with a priority on achieving a symmetrical, low inductive drain-drain current loop for loss balancing and to ensure similar driving points for the paralleled MOSFETs. This interleaved drain terminal design shown in Fig. 3.5 accomplishes this, while allowing symmetric access to the gate and source terminals of each MOSFET for highly symmetrical gate loops, which are also designed for compactness through the integrated bypass capacitors. Thanks to the large choke inductors the CSRI is less vulnerable to shoot-through issues than voltage source topologies. Therefore, no external gate resistors were added for the purpose of fast switching speed.

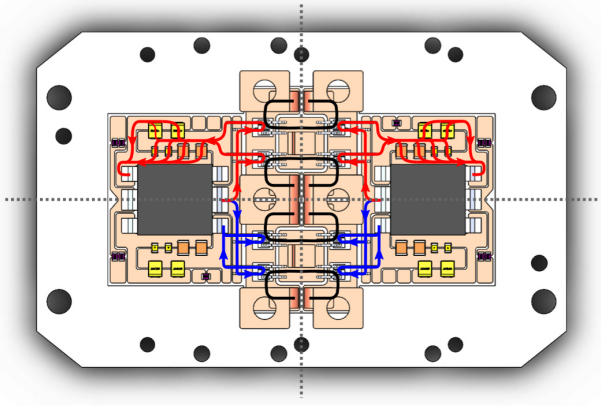


Fig. 3.5: Top-down image of the power module where the red and blue lines mark the gate current for the MOSFETs when clamped to the positive and negative rails, respectively, while black lines mark the drain-drain current paths. Mirror symmetry is indicated by gray dotted lines. [Paper B]

3.2.2 Thermal management

The power module components were mounted on direct bonded copper (DBC) substrate to achieve high voltage insulation and a compact design where all components including power MOSFETs, gate drivers, and auxiliaries fit on the same cooling system. Aluminum nitride ceramic was chosen for its high thermal performance [101], and the assembly was soldered to a copper baseplate for mechanical stability and heat spreading. The manufactured power module is shown in Fig. 3.6. Auxiliary- and measurement connections were interfaced to the control circuit board through a housing with embedded pins.

In order to estimate the temperature of the power module the integrated thermistors are a simple solution, but for 3D stacked structures made of materials with high thermal conductivity the heat flow from the dissipating device

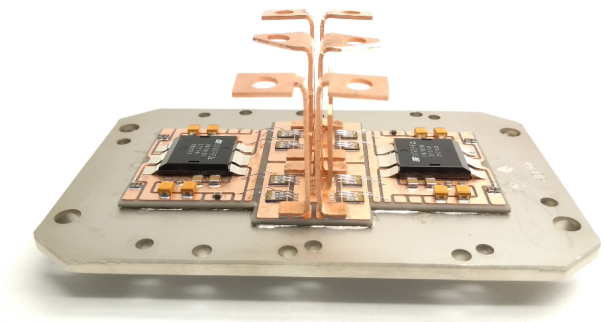
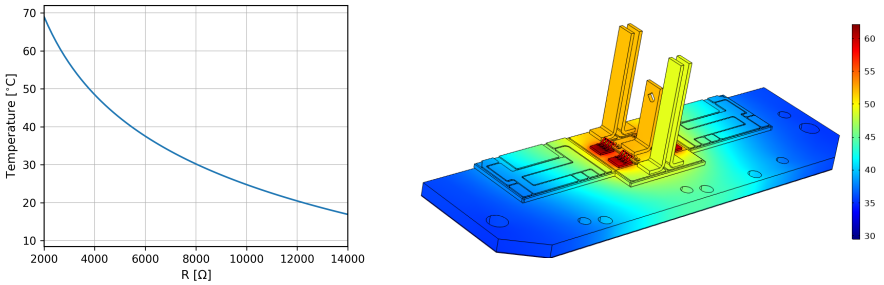


Fig. 3.6: Photograph of the manufactured CSRI power module before silicone gel encapsulation. [Paper B]

generator is highly vertical, so this method has poor accuracy in itself. Instead, as the physical structure and the material properties of each element of the power module is known, the MOSFET temperature can be correlated with the thermistor temperature data through thermal FEM simulations. For this, the thermistor resistance correlation with temperature is measured and fit to the equation

$$R_1 = R_0 \mathrm{e}^{\beta(\frac{1}{T}-\frac{1}{T_0})} \tag{3.17}$$

The resultant fit is shown in Fig. 3.7a. Using this, simulations are conducted in Comsol Multiphysics® [102] to infer the MOSFET junction temperature from the measured thermistor resistance. During operation of the inverter, the power dissipation in the module is measured calorimetrically, so the total power loss in the module is known. In addition, the gate driving power loss can be read from the gate driver power supply, and as there is no external gate driver resistor, the division of the power loss between gate driver chip and power MOSFETs can be approximated by assuming that (2.12) accounts for the loss in the MOSFETs and the rest is in the driver chip. In the simulations, the calorimetrically estimated power loss is applied to the MOSFETs and gate drivers and the convective heat flux coefficient of the water cooling system is sweeped until the average temperature of the copper islands on which the thermistors are soldered matches the measured value. From the resultant model, an example of which is shown in Fig. 3.7b, the estimated MOSFET surface temperature can be directly observed. For a cooling water temperature of 20 °C, it is shown here how a measured thermistor temperature of 44 °C corresponds to a maximum transistor temperature of roughly 62 °C. This rough method for chip temperature estimation assumes equal power dissipation in each MOSFET.



(a) **(b)**

Fig. 3.7: Depiction of the parameters used for estimation of die temperature (a) fitted thermistor curve from measurements on a hot plate (b) FEM simulation correlating the MOSFET temperature with the one at the thermistor location. The baseplate is connected to the cooling system by thermal interface material with an assumed thickness of 100 μm.

3.3 Experimental verification of operation

The final elements required for the CSRI system are the choke inductors, which were constructed as 15 winding EMS-0653327-060 powder cores for an inductance of 49 μH, and the control circuitry. For the verification of inverter operation the resonant tank with steel load does not vary in frequency, and therefore the tests were conducted in open loop using a fully configurable PWM controller implemented on an FPGA with 3.3 ns output signal resolution.

3.3.1 Integrated gate driver performance

The performance of the gate driver circuit with two complementary integrated drivers each driving 4 paralleled 1700 V MOSFETs in the MHz range was first investigated. To account for the underdamped gate voltage behavior and prevent possible damaging overvoltages, the positive gate voltage was set to $\nu_{\mathrm{gs}} = 16$ V instead of $\nu_{\mathrm{gs}} = 20$ V. This compromise can be seen from the MOSFET datasheet to result in a moderate $\approx 10\%$ increase in $R_{\mathrm{ds,on}}$[1]. The operation at 2.5 MHz and 50% duty cycle is shown in Fig. 3.8. A reasonable level of underdamping is observed, along with rise and fall times of around 20 ns. The driving signals are nearly independent of the switching of the complementary driver.

The thermal performance of the integrated gate drivers was investigated under the same operating conditions by monitoring the driver surface and heat sink temperatures with a thermal camera. The results are shown in Fig. 3.9, where the slow temperature rise is due to not actively cooling the heat

[1] This was also verified by curve tracing as in Fig. 2.5

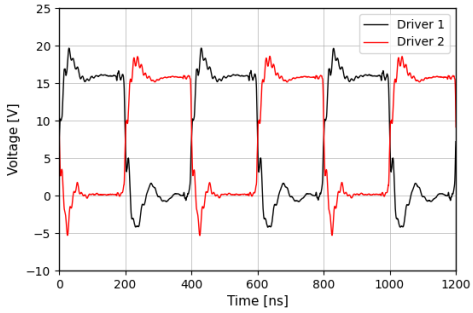
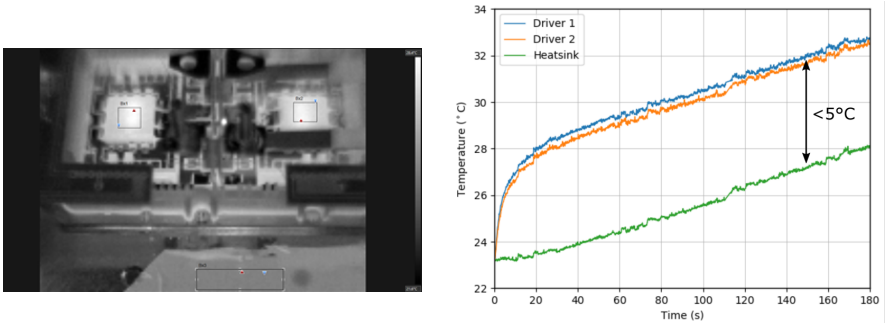


Fig. 3.8: Gate driver output voltages measured at 2.5 MHz with $V_{\text{in}} = 0$ V. [Paper B]

sink. The low temperature increase measured on the driver surface here when the power delivered by the gate driver power supply is 27 W, as well as the small temperature difference between the drivers, indicates that the thermal network of the driver is not limiting the operation frequency of the inverter or the achievable gate driver voltage swing. The integrated gate driver approach therefore seems to be a good solution for low inductance, high frequency hard switched gate driving of paralleled SiC MOSFETs.

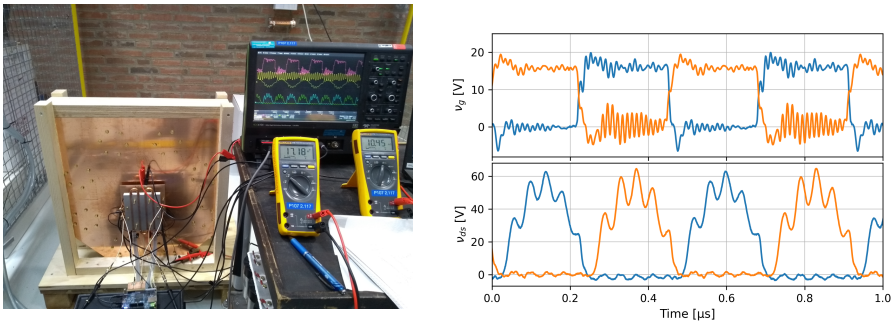


(a) **(b)**

Fig. 3.9: Thermal performance of gate driver measured with a thermographic camera. (a) Infrared image of power module and heat sink and (b) temperature rise for the gate drivers and heat sink for 2.5 MHz operation. [Paper B]

3.3.2 Resonant operation

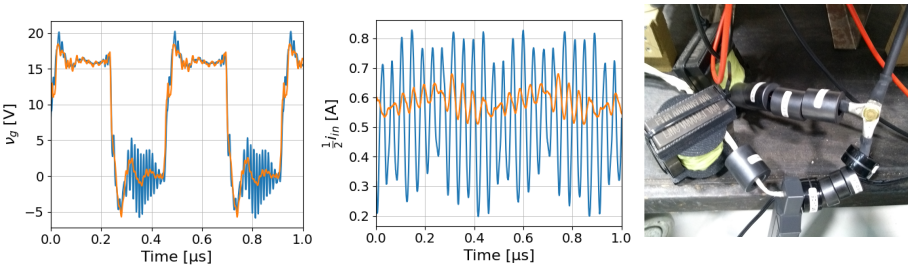
The experimental tests of the CSRI were performed with only the resonant tank circuit resistance without induction load R_{load} in order to simplify the analysis and to highlight the influence of the parasitic elements of the inverter. The power module and auxiliary components were connected to the resonant tank presented in section 2.5, and the initial test setup is shown in Fig. 3.10a.



(a) **(b)**

Fig. 3.10: Test setup with the CSRI inverter. (a) Picture of the experimental setup with the power module assembly mounted directly on the resonant tank and (b) measured gate-source and drain-source voltages of the inverter at $V_{\text{in}} = 17$ V.

The input current during testing was increased gradually from zero with the CSRI operating close to the resonance frequency. As evidenced on Fig. 3.10b, high frequency noise around 100 MHz was observed even at low drain voltage. This behavior is potentially problematic, especially because the gate voltage is not driven negative during turn-off of the MOSFETs, but only if these oscillations are really present on the MOSFET gate capacitances. Thanks to the open module design, the voltage close to the actual voltage at the gates could be measured by piercing the gel at the driver output, which is shown in Fig. 3.11a, verifying that the observed high frequency signal is due to a resonance in the measurement loop.



(a) **(b)** **(c)**

Fig. 3.11: Measurements of high frequency oscillations in the inverter. (a) Gate-source voltage measured on measurement pin (blue) and directly at the driver output (orange), (b) DC inductor current measured with no damping (blue) and with ferrites (orange), and (c) picture of the damping ferrites, DC inductors, and current sensor.

A seemingly similar issue was observed when measuring the inverter input current at the choke inductors. However, this phenomenon was not measurement

related but a real circulating current through the parasitic capacitance of the DC inductors and the resonant capacitor bank, which is effectively a short at tens of MHz. The oscillation frequency of this current was ≈ 25 MHz, fitting well with the approximate resonance frequency of the connection cables and with the 25 pF parasitic capacitance of the DC inductors. As shown in Fig. 3.11b, these were efficiently damped using RF ferrites on the input side of the DC inductors. These examples highlight possible issues with using discrete components for MHz inverters, since any parasitic coupling path is a potential resonant loop.

In addition to the resonant tank voltage waveforms across the drain terminals of the switches, the additional parasitic oscillation predicted by (3.15) is also observed in 3.10b. The frequency of the oscillation cannot realistically be increased, since L_{para} is already is as low as physically feasible. The power module was therefore removed from the tank for simpler testing and monitoring and reconnected through a busbar structure. The tests performed in this configuration are shown in the measurements in Fig. 3.12.

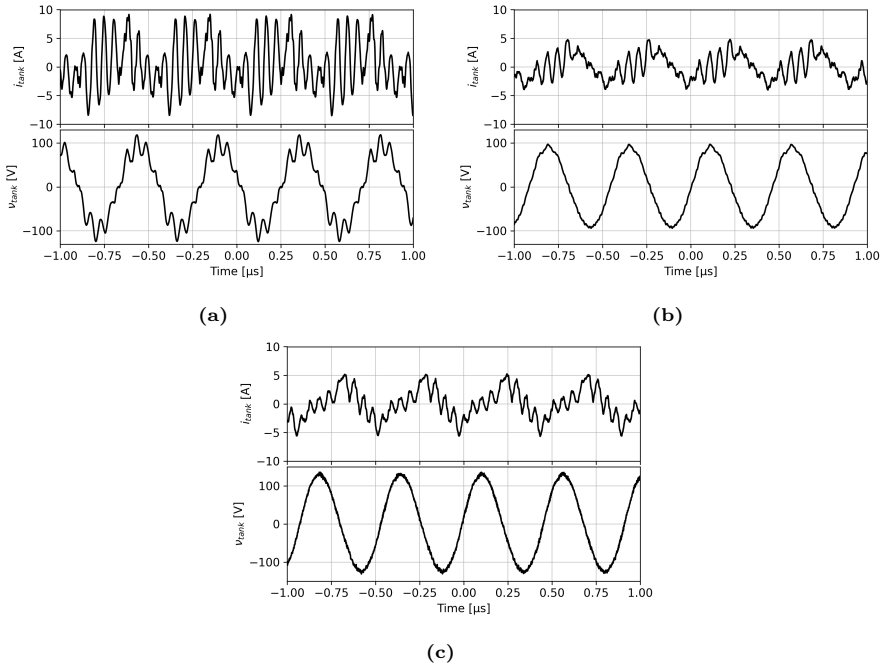


Fig. 3.12: Measurements of the power module output current and the resonant tank voltage close to resonance at $f_{\text{sw}} = 2.17$ MHz. (a) Duty cycle setpoint of $D = 0.52$ and $V_{\text{in}} = 30$ V, (b) $D = 0.41$ and $V_{\text{in}} = 30$ V, and (c) $D = 0.41$ and $V_{\text{in}} = 40$ V [Paper B]. Due to the differences in the turn-on and turn-off delays and the parasitics of the gate loop, the duty cycle setpoint for ZVS is lower than 0.5. At $V_{\text{in}} = 30$ V the parasitic oscillation frequency is $f_{\text{react}} \approx 18$ MHz, which increases to $f_{\text{react}} \approx 20$ MHz at $V_{\text{in}} = 40$ V.

The module output current i_{tank} is measured with a Rogowski coil, and the tank voltage ν_{tank} is the differential voltage across the drain terminal of each leg. Although the input voltage is higher than in Fig. 3.10b corresponding to a smaller $C_{\text{oss,eq}}$, a decrease in f_{react} is observed due to the ≈ 12 nH loop inductance introduced by the busbar, and the overall frequencies of f_{react} fit well with estimated total loop inductance of 34 nH and the expected $C_{\text{oss,eq}}$ from the MOSFET datasheet at these voltages. The amplitude of the parasitic oscillations in Fig. 3.12a can be reduced dramatically by adjustment of the duty cycle, as is shown in Figs. 3.12b and 3.12c. Here, the relatively pure sine output voltage and low amplitude of oscillations indicates that nearly complete soft switching is achieved. It is apparent that for complete soft switching very precise frequency and voltage tuning is required.

This is further evidenced in higher voltage operation as shown in Fig. 3.13, where the amplitude of the oscillations on the waveforms clearly show that complete ZVS is not achieved. The finite driving resolution of 3.3 ns enabled by the open-loop controller is not sufficient to avoid significant amplitude parasitic oscillations. The inverter operation is therefore not robust, and the inverter underwent abnormal operating conditions which resulted in failure of the module, preventing further testing of the system.

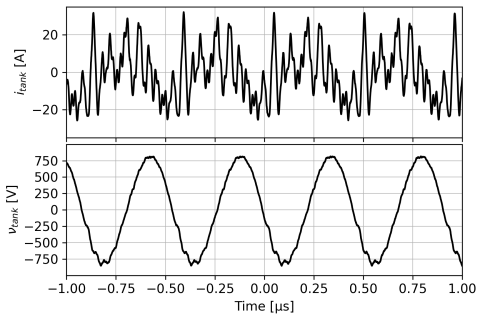
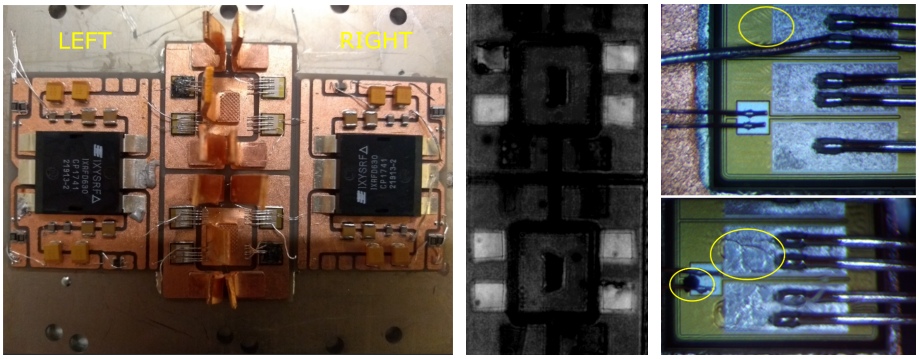


Fig. 3.13: Measurements of the module output current and resonant tank voltage at a switching frequency of 2.19 MHz and $V_{\text{in}} = 280$ V. [Paper B]

Post-mortem analysis, as shown in Fig. 3.14, did not unambiguously reveal the reason for the inverter failure. One option which has been observed on devices similar to the ones utilized here is gate failure due to the high amplitude current pulsing in a fast switching layout with low parasitics [90], resulting in a similar fusing of the device gate structure to that seen on Fig. 3.14c. However, since the maximum applied gate current here is lower, and no evidence of gate structure breakdown was observed prior to this, the origin of the failure is not thought to be related to device structure alone.

As argued in section 2.4.2, the negative temperature coefficient of the threshold voltage can result in uneven current sharing between parallel devices,



(a) (b) (c)

Fig. 3.14: Post-mortem pictures of the failed power module. (a) Top-view picture where the silicone gel and housing has been removed mechanically. (b) Scanning acoustic microscope image highlighting the solder layers of the dies, showing only damage on top-left and bottom-right MOSFETs. (c) Microscope image of the bottom left transistor (bottom) and the transistor just above it (top) on picture (b). The areas where the gate-source has shorted are highlighted, along with evidence of high surface temperature on the source metallization and polyimide.

but given the margin between the expected junction temperature and the device ratings, it seems unlikely that this could initiate the failure during normal operation although it may contribute to its severity. In addition, despite the observation from Fig. 3.14b that the solder layers appear as normal on the intact devices, the partly melted surface metallization of devices on the left leg of the module shown in Fig. 3.14c is clear evidence of high junction temperatures and indicate that very high current transients were present on all devices in this leg prior to failure. The static device characteristics measured after failure revealed reduced drain-source blocking capability for the two devices with shorted gate-source, while the rest of the devices showed expected transistor behavior.

A deeper failure mode investigation was not performed, and the destructive failure of some of the paralleled devices makes finding the root cause unlikely. While the specific failure mechanism is not known, the most likely initiator of the failure is thought to be the gradual loss of soft switching resulting in high frequency noise interfering with the control of the transistors, resulting in false triggering conditions leading to device failure. The low margin for driver timings is therefore a major drawback in this topology implementation.

Prior to failure, the efficiency of the inverter was measured calorimetrically by monitoring the cooling water temperature of the power module heat sink. It is assumed that because of the simple structure, low input current, and the lack of an output transformer, the cables and input chokes contribute negligibly to the total power loss, such that the efficiency can be estimated as

$$\eta = \frac{P_{\text{in}} - P_{\text{module}}}{P_{\text{in}}} \cdot 100 \tag{3.18}$$

The measured efficiency for different power levels is shown in Fig. 3.15. The low efficiency at low power is primarily due to the input power independent gate driver consumption. At higher power ZVS is gradually lost due to imprecisions in the gate driving timing resulting in worse efficiency. Still, up to the power levels tested here, efficiency higher than 90 % is achieved even for this configuration where the power module, and the associated switch parasitic capacitances, are significantly overdimensioned for the applied input currents. Therefore, neglecting any non-idealities of such a system it is expected that an appropriate impedance transformation will allow for better utilization of the switches and improved efficiency. This is supported by comparison of the expected chip temperatures using the method explained in connection with Fig. 3.7, from which the chip surface temperature at the operating point in 3.13 is estimated to be less than 70 °C. In addition, the resonant tank current at this point can be approximately found from $i_{\text{res}} = C_{\text{tank}} \frac{\mathrm{d}V_{\text{tank}}}{\mathrm{d}t}$, which is a conservative estimate for the reasons discussed in section 2.5. From this, 170 kVA of reactive power is oscillating in the resonant tank.

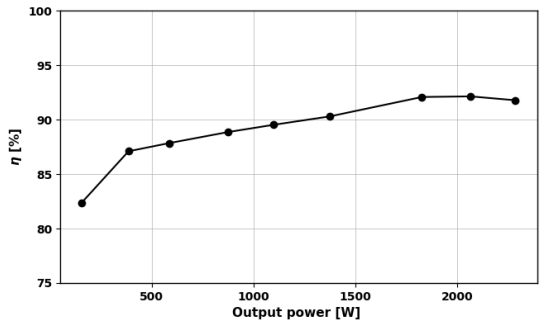


Fig. 3.15: Estimation of the calorimetric efficiency of the CSRI inverter power module at varying output power. [Paper B]

Overall, it was found that the operation of this implementation of the CSRI is not robust, and that it is therefore not a reasonable candidate as a basis for a solid state generator for the FZ process due to the issues with parasitic elements and its reliance on very precise gate signal timing. However, since $> 90\%$ efficiency was achieved in at reasonable voltage levels even for unloaded operation, the presented results validate the performance of the many of the design concepts of the inverter for MHz operation.

3.4 Inclusion of series diodes

From the perspective of a robust industrial solution, experience with the bidirectional CSRI module showed that there are likely significant issues related to the high control resolution required for the driving signal for this topology within this power and frequency regime. This largely stems from the fact that it can ideally only operate at exactly the resonant frequency of the parallel resonant tank, and that the margin for timing deviation is very low. One solution to this issue is the already well known addition of series diodes to the switches, as is common in industrial induction heating systems.

The inclusion of diodes allows operation off-resonance and allows the control of the output power through switching frequency variation. It is however noted the switch voltage ν_{ds} increases for off-resonance switching, as evidenced by the voltage transfer function 3.19 in terms of frequency for a lossless inverter [58]

$$\frac{V_{\mathrm{ds,p}}}{V_{\mathrm{in}}} = \pi \sqrt{1 + Q_{\mathrm{L}}^2 \left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right)^2} \tag{3.19}$$

where ω, ω_0, and Q_{L} are the switching frequency, resonance frequency, and quality factor at this frequency, respectively. This equation is plotted in Fig. 3.16, showing a large penalty for off-resonance switching at high Q factor. Therefore, even including the series diodes the switching frequency of the inverter should be kept close to resonance.

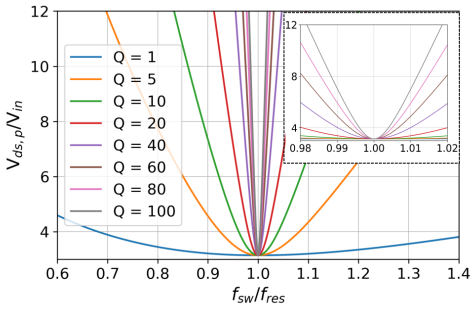
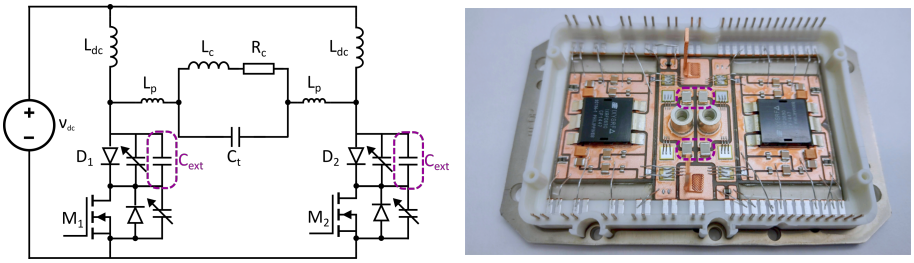


Fig. 3.16: CSRI voltage transfer function at normalized frequencies for different quality factors of the parallel resonant circuit.

In the introduction to this chapter it was mentioned that the inclusion of ideal series diodes prevents the discharge of the MOSFET output capacitance, resulting in additional turn on switching loss. This issue is partially alleviated when the parasitic capacitance of the diode is also taken into account, as C_{oss} can then discharge through charging of the diode junction capacitance.

However, since the diode capacitance is also highly voltage dependent the effective capacitance quickly drops once the diode becomes reverse biased. Therefore, the limited size of the diode capacitance and its nonlinearity means the voltage across C_{oss} at turn on may still be significant. It is therefore theorized that the addition of a fixed capacitance of a few nF in parallel with the diode may be a solution to reducing switching timing sensitivity as well as reduce turn on switching losses in this configuration. The inverter circuit schematic including major parasitic elements is shown in Fig. 3.17a.

To investigate the proposed improvements, two power modules were manufactured, with and without integrated parallel diode capacitors, respectively, as shown in Fig. 3.17b. These modules include one CPW5-1700-Z025A Schottky diode [103] in series with each MOSFET, and a number of improvements to the power module were made based on the previous experience. These include the use of gate resistors for reduced voltage overshoot, and negative gate driving in the OFF state to reduce risk of false turn-on. The number of paralleled MOSFETs is halved to increase the frequency of (3.15). For additional thermal measurements, direct access to the MOSFET and diode surfaces was made for fiber optic temperature sensors, non-encapsulated surface of the gate drivers for thermal camera measurements, and thermistors placed closer to MOSFETs for higher measurement accuracy. Similar thermal measurements to those in Fig. 3.9 showed a less than 3 °C temperature increase relative to the heat sink for operation at 2.5 MHz.



(a) (b)

Fig. 3.17: CSRI with series diodes for improved operational stability. (a) Circuit schematic of the inverter including major parasitic elements and optional external parallel capacitor and (b) picture of one of the manufactured power modules with the integrated capacitors highlighted.

3.4.1 Experimental results

The power module without integrated parallel capacitors was tested using most of the same inverter setup as in section 3.3 with the addition of steel block load to emulate the weakly coupled induction load in the FZ process. For low power operation of 180 W, the measured waveforms are seen in Fig. 3.18a, where the

voltages across the switch elements are shown. It is apparent the ZVS turn on of the MOSFETs is not achieved, although the C_{oss} is only partially hard switched due to the discharging current path through the diode capacitance. The voltage oscillations from the parasitic inductance resonating with the switch parasitic capacitance is still apparent. The inverter is driven only slightly below the apparent tank resonance frequency, but a relatively large phase shift between switch voltage and tank voltage is observed.

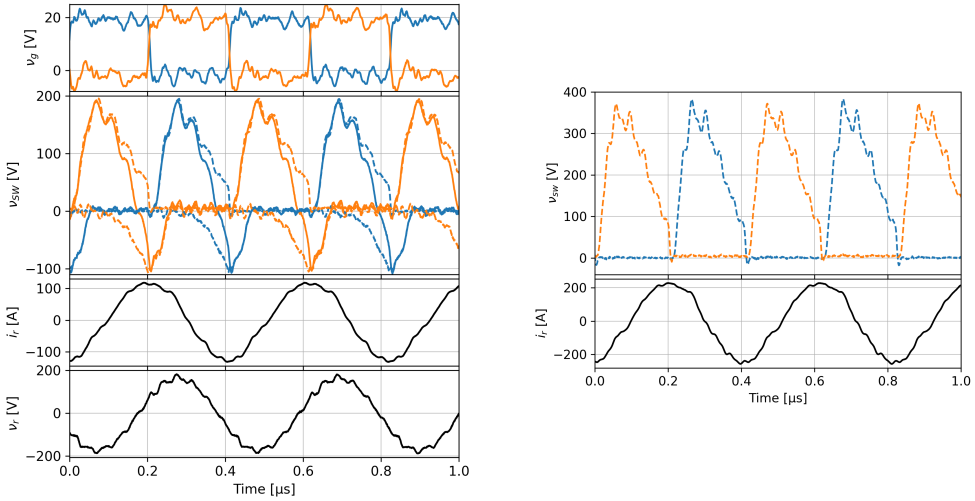


Fig. 3.18: Measured voltage and current waveforms of the CSRI with diodes for moderately loaded operation at 2.41 MHz. (a) Input power of 180 W. For ν_{sw} the solid line is the entire switch voltage and the dotted lines is the same voltage split into the voltage across the diodes and MOSFETs, respectively. The resonant current i_{r} is measured with a PEM CWT Rogowski coil, which adds a small delay so the measured current is not entirely out of phase with the tank voltage. (b) Input power of 700 W, where ν_{sw} is measured across the MOSFETs only.

Increasing the input power to 700 W in Fig. 3.18b, similar behavior for the inverter is observed. Although these waveforms show reasonable operation of the inverter, it was not possible to increase the power level further as electrical noise was interfering with the power supply control, causing repeated overcurrent tripping. The employed noise mitigation strategies were insufficient and operation above the power levels in Fig. 3.18b was not achieved. The concept of employing a fixed capacitance in parallel to the series diodes to reduce the gate signal timing dependence further was not experimentally verified.

3.5 Summary

Prototype CSRI inverters were designed, manufactured, tested, and discussed in this chapter. The general operation of the bidirectional inverter was verified, but the implementation suffered from control issues, which lead to the development of a version with series diodes. This diode iteration of the CSRI cannot be considered thoroughly tested, and the conclusion on the overall viability of the CSRI as a candidate for the FZ process generator is therefore not definitive. Although more research is required on this topic, several important points were clarified in this work. The power module structure performed as expected and demonstrates the approach of applying high-speed gate drivers for the direct driving of paralleled SiC MOSFET devices. This verifies that a high efficiency CSRI for multi-MHz operation can be constructed using paralleled 1700V SiC MOSFET in this type of power module.

As described in section 2.3 the CSRI topology generally lends itself well to high frequency power amplifiers. However, the combination of MHz operating frequencies, paralleled high voltage devices, and the practical construction of an inverter with a large and bulky resonant tank capable of handling many hundreds of amperes of circulating current means that, for the presented implementation, handling the parasitic elements is a significant challenge and will result in additional losses, and may cause unwanted high-frequency oscillations and timing issues. The high sensitivity to driver resolution of the bidirectional topology makes the timing margin for the gate signals narrow. Realistically, the implementation of a higher resolution PWM generation in combination with a robust frequency tracking system is required for reliable operation of this inverter.

Chapter 4

Class E push-pull inverter development

The challenges associated with the requirements for a high efficiency inverter for the targeted application were presented in the previous chapters, and in chapter 3 it was shown how the interplay between device- and circuit parasitic capacitances and inductances can be a detriment to inverter performance. This chapter demonstrates and discusses an implementation of the Class E push-pull topology as an alternative approach to the FZ inverter topology. The main contributions of this chapter are published in papers C and D.

As described in section 2.3, the Class E resonant inverter is attractive for many of the same reasons as the CSRI, with the additional important feature that the output inductance of the switching stage is not undesired and is a deliberate part of the resonance loop. Therefore the requirements for compactness of the inverter system are relaxed, and the hypothesis is that this topology can provide more freedom in the component design, cleaner switching waveforms, and the simple incorporation of an output transformer to decouple the switching stage from the resonant tank.

4.1 Topology description

An important specification for the FZ inverter system is efficient operation under both variable resonant tank frequency and load. There has been significant focus on how to improve the performance of Class E inverters and rectifiers and their derivatives under resistive load variations [66], [73], [104], [105]. This is owed in large part to the use of these converters for e.g. wireless power transfer and battery charging applications, which demand highly varying level of loading depending on coil distances and charging profiles, respectively. However, in these

applications the frequency of the resonant elements is generally fixed, which allows the converters to be tuned to be nearly independent of load resistance for a narrow frequency band for high Q-factors [106], [107]. For the desired implementation in the FZ application, the inverter is required to operate with high efficiency in a range of both resonance frequencies and resistive loads.

The circuit schematic of the considered implementation of the Class E inverter is shown in Fig. 4.1, which is a push-pull version with complimentary switches. Similar to the CSRI, the gates of both switches in this configuration are referenced to ground, which avoids level shifting issues. The switch utilization and the operating conditions are practically the same as the single ended Class E when utilizing an output transformer, but the harmonic content of the output signal is significantly reduced due to cancellation of the even harmonics [108], [109].

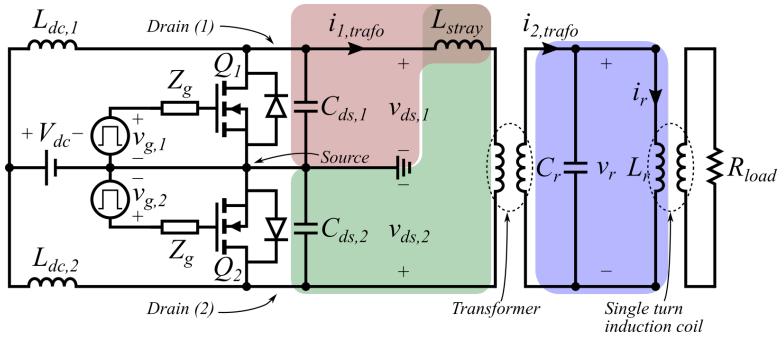


Fig. 4.1: Circuit schematic of the developed variant of the Class E push-pull inverter with the colored areas showing the high frequency resonance loops. [Paper D]

The main variation in the operation of this topology compared to the standard Class E inverter is in using the tuning of a secondary resonance loop to allow similar inverter operation under conditions where the frequency of the resonant tank drifts. As shown in Fig. 4.1 the drain-source capacitance C_{ds} of the switches and an external inductance L_{stray} constitute a resonance loop with frequency f_{ds} that can shape the voltage across the switches nearly independently of the tank resonant frequency f_{res}. The influence of this feature on the waveforms of the circuit is shown in the SPICE simulation in Fig. 4.2 for the inverter operated at the resonance frequency of the tank. Here, the conduction of the diodes provides inherent near-ZVS turn on of the switches during the time T_{B} which means that the topology is relatively insensitive to inaccuracies in gate signal timing as long as the drain-source voltage oscillation is in the negative half cycle during turn on of the switch. Therefore, the tuning condition for the drain-source resonance frequency is

$$f_{\mathrm{res}} = f_{\mathrm{sw}} < f_{\mathrm{ds}} < 2f_{\mathrm{res}} \tag{4.1}$$

As a consequence, the aim in this topology implementation is not to achieve the nominal tuning condition of the Class E inverter for ZVDS, but to drive the switches under varying frequency in suboptimal conditions with diode conduction prior to turn on to achieve ZVS [58], [73]. This has the drawback that the drain-source voltage waveform is narrowed, which increases the ratio $V_{\mathrm{ds,p}}/V_{\mathrm{dc}}$ from the volt-second balance of the DC chokes, lowering the switch utilization in this implementation.

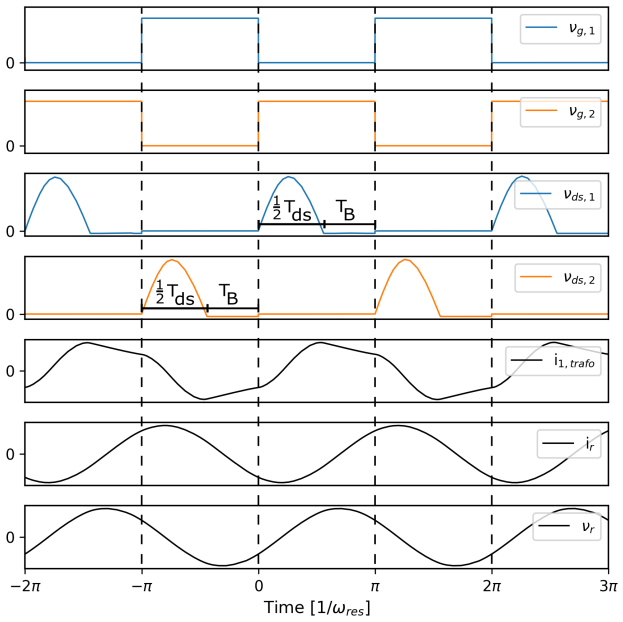


Fig. 4.2: Simulated ideal waveforms of the Class E push-pull resonant inverter topology. This switch in this simulation has an antiparallel diode, but any fast, bidirectional switch could be used. The period of the resonant tank is $T_{\mathrm{res}} = T_{\mathrm{ds}} + 2T_{\mathrm{B}}$. [Paper D]

4.2 Inverter component design

For the frequency range of interest, the inductance required for the drain-source loop can easily be comprised of the stray circuit inductance and the transformer leakage inductance. In this way, the capacitances of the switching devices as well as both the input and output inductances of switching stage are non-parasitic circuit elements. However, the limitation of (4.1) constrains the range of practical choices of switch components and high frequency transformer designs.

4.2.1 Power module

A power module was built for the inverter demonstration on a similar platform to the one developed for the CSRI in section 3.2, and utilizes many of the same design principles; integrated hard switching gate drivers directly driving paralleled 1700V SiC MOSFETs, symmetric and low inductive gate- and power loop layouts, and thermistors for temperature estimation. The gate driver IC IXDN614 [110] was chosen as a replacement for the obsolete IXDRF630 IC, and external $R_{\mathrm{g}} = 1.8\ \Omega$ was used for the gate loops. In addition, integrated high voltage capacitors rated for 2 kV [111] were added in parallel to the MOSFETs to tune the drain-source resonance frequency and reduce its voltage dependence. Assuming that the inductance in the drain-source resonance loop is dominated by the leakage inductance of the transformer, and ignoring the parasitic capacitances from both transformer and power module, the drain-source resonance frequency is

$$f_{\mathrm{ds}} \approx \frac{1}{2\pi\sqrt{2(C_{\mathrm{oss,eq}} + C_{\mathrm{cap}})L_{\mathrm{p}}^{\sigma}}} \tag{4.2}$$

The loop between the MOSFETs and parallel capacitors must have very low inductance to avoid parasitic oscillations, making surface-mounted C0G type capacitors the obvious choice for resonance tuning as they have low ESR, high ripple current capability, and maintain their capacitance rating at high voltage and frequency. The design specifications for this power module are similar enough to those for the module presented in Fig. 3.17b that the same DBC layout can be used. Therefore, in the manufactured Class E push-pull module seen in Fig. 4.3, the loop between the drain terminals is highly compact, even though this is not a requirement in this topology and is a simply a result of reusing the previous design.

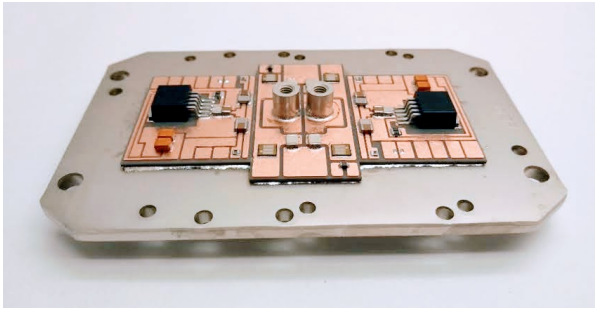
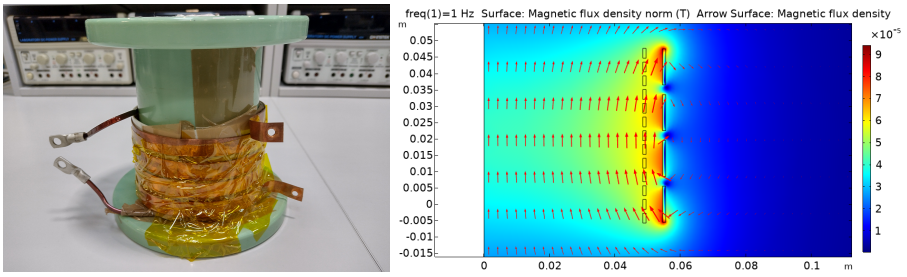


Fig. 4.3: Class E push-pull inverter power module before wire bonding, terminal welding, and potting with encapsulating gel. The DBC layout for the power loop is the same as in 3.17b. [Paper D]

4.2.2 High frequency transformer

For the implementation of the high frequency transformer a coreless layout is chosen to avoid the losses and parasitic elements associated with magnetic cores, which may be a substantial issue at MHz frequencies [41]. The transformer must be able to handle the AC current and voltage levels while providing a high coupling coefficient and efficiency as well as a suitable leakage inductance, which can result in a rather bulky component. For the considered application, this is only a minor drawback.



(a) **(b)**

Fig. 4.4: The helical high frequency transformer design used for initial tests of the inverter. (a) Picture of the 4:13 transformer, and (b) magnetic field simulation of the transformer with open secondary/inner coil in a low frequency approximation. The size of the arrows showing the magnetic flux density are proportional to the flux magnitude.

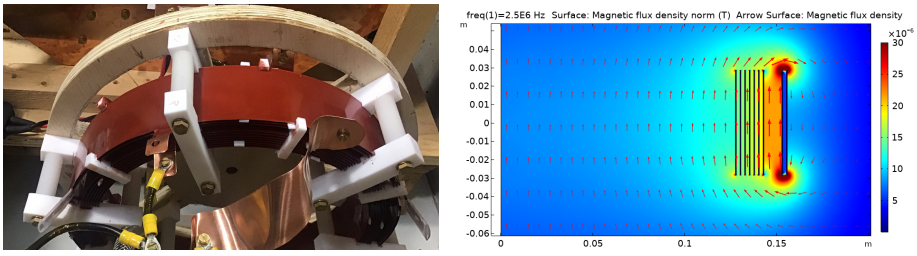
The initial design of a helical transformer is presented in Fig. 4.4 along with a corresponding magnetic field simulation in Comsol. It is noted that the inductances of the transformer are frequency dependent due to the skin effect from (2.2) and the proximity effect, leading to inhomogeneous current distribution and concentration of the magnetic fields at high frequencies which reduce the leakage inductances [42]. Because of this the leakage inductances measured at low frequency may be overestimated, which is exemplified here by comparing simulated inductance matrix values of the transformer for 1 Hz and 2.5 MHz to the measured values:

$$\begin{array}{ccc} \text{Sim. 1 Hz:} & \text{Sim. 2.5 MHz:} & \text{Measured} \\ \begin{bmatrix} 1.81\ \mu\text{H} & 4.41\ \mu\text{H} \\ 4.41\ \mu\text{H} & 16.0\ \mu\text{H} \end{bmatrix} & \begin{bmatrix} 1.70\ \mu\text{H} & 4.24\ \mu\text{H} \\ 4.24\ \mu\text{H} & 15.3\ \mu\text{H} \end{bmatrix} & \begin{bmatrix} 1.8\ \mu\text{H} & 4.2\ \mu\text{H} \\ 4.2\ \mu\text{H} & 14\ \mu\text{H} \end{bmatrix} \end{array} \tag{4.3}$$

The difference is significant enough that it should be kept in mind when considering the frequencies of the resonant elements of the inverter. However, at MHz both the parasitic turn-to-turn and primary-to-secondary capacitances also influence the transformer impedance, which is not accounted for in these magnetic field simulations, although this could be included if more detailed modeling including parasitic effects and skin depth is desired. In addition to

minor geometrical differences these factors mean that significant discrepancy between simulation and measured values of constructed transformers is to be expected. Therefore, the simple magnetics field simulations presented here can mainly be used for estimations of the size and dimensions of the transformers and investigations of the merits of different geometries.

The coupling factor of the helical transformer was measured to be $k = 0.84$, which was regarded as sufficient for acceptable transistor utilization and load coupling. However, this helical design without any active cooling is not suitable for high power operation. While actively cooled versions of this layout are also an attractive option for high frequency transformer applications [112], the feasibility of a passively cooled transformer version was investigated instead. To this end another transformer was manufactured based on a concentric spiral layout of wide copper windings for enhanced cooling efficiency, which is shown in Fig. 4.5.



(a) (b)

Fig. 4.5: The manufactured concentric spiral high frequency transformer. (a) Picture including tabs for adjustment of the primary, secondary, and leakage inductances. Here, the tab is used for 1/8 additional primary turn length. The transformer is 32 cm in diameter the windings are 57 mm wide [Paper D]. (b) magnetic field simulation of the transformer for 2.5 MHz. Due to the high degree of flux concentration near the copper turn edges, the color scale is compressed.

This transformer type has similar primary leakage inductance, lower primary-to-secondary capacitance and much larger exposed surface for passive cooling. The tradeoff for this implementation is a slightly lower coupling factor around $k = 0.75$ and higher turn-to-turn capacitance.

4.3 Experimental verification

The same basic setup structure and components presented earlier were reused for the experimental investigation of this inverter system, including choke inductors, connectors, and resonant tank. The implementations of the components of the prototype system are shown in table 4.1.

Table 4.1: Prototype component values. [Paper D]

Component	Value	Implementation
S1, S2	$R_{\mathrm{ds,on}} = 80$ mΩ $C_{\mathrm{oss}} = 105$ pF @ 1000 V	4x CPM2-1700-0080B
Gate drivers	$\nu_{\mathrm{g}} = -4$ V/ + 18 V	2x IXDN614YI
Module capacitors	$C_{\mathrm{cap}} = 470$ pF	4x C1812X471JGGACTU
Transformer	$n = 2:7$, $L_{\mathrm{p}}^{\sigma} = 1.0$ uH $L_{\mu} = 1.1$ uH	Spiral windings, air-core
DC chokes	$L_{\mathrm{dc}} = 49$ uH	2x EMS-0653327-060 powder cores, 15 windings

4.3.1 Experimental setup

The previously used resonant tank with a steel block load from section 3.4 was reused for this setup. The steel load, as well as the work coil and the power module, were individually water cooled to allow for calorimetric measurements of the power dissipation in each component. The load during operation was kept at a constant distance to the work coil, such that the resonance tank frequency was fixed at $f_{\mathrm{res}} \approx 2.4$ MHz. A picture of the setup is shown in Fig. 4.6.

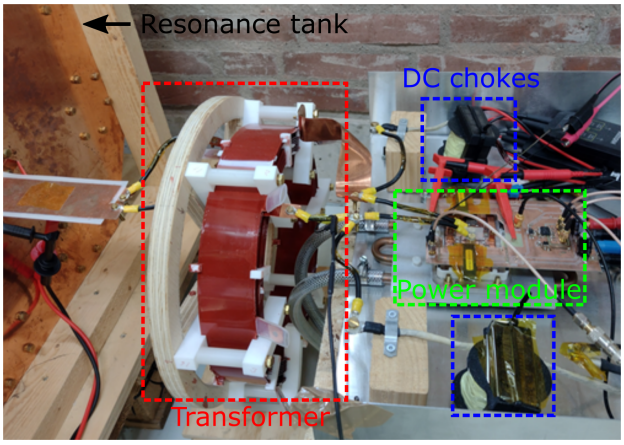


Fig. 4.6: Picture of the experimental setup, with wires and busbars connecting the discrete elements of the inverter system. [Paper D]

To evaluate the tuning of f_{ds}, the impedance of the setup was measured at the power module terminals as shown in Fig. 4.7[1], where the tank resonance frequency is readily observed. The measured impedance is compared with a SPICE model of the inverter system including switch capacitance and transformer model. From the MOSFET datasheet $C_{\mathrm{oss}}(0\mathrm{V}) \approx 2.25$ nF, resulting in a

[1]In paper D f_{res} is mistakenly labeled as f_{tank}, which is corrected in this figure.

total switch capacitance of $2(C_{\text{oss}}(0\text{V}) + C_{\text{cap}}) = 5.44$ nF. Therefore, as the two switches are in series for this measurement, a drain-drain capacitance of 2.72 nF is expected, which when simulated fits well with the measurement. The same simulation is also shown for $C_{\text{ds}} \approx 1.23$ nF, which is the estimated drain-source resonance frequency of a switch at a peak voltage of 800 V from (3.14). This results in $f_{\text{ds}} = 4.56$ MHz, fulfilling the component requirements set by (4.1). For the presented system at this voltage level it would be beneficial to tune f_{ds} to a lower value closer to f_{res}, but to allow for operation from zero voltage, this value is considered a reasonable compromise for testing purposes.

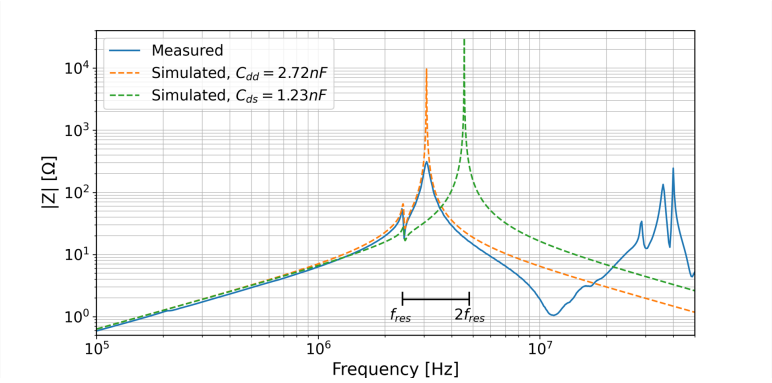


Fig. 4.7: Load impedances measured and simulated from the power module output terminals. The f_{ds} operation range for this load configuration where ZVS is achievable from (4.1) is highlighted. [Paper D]

4.3.2 Results and discussion

Initial tests of the gate and drain waveforms of the inverter operating close to the tank resonance frequency is shown in Fig 4.8. The inverter operates as expected with the drain-source loops ensuring ZVS prior to MOSFET turn on by the conduction of the body diode. However, this operating mode is inefficient as f_{ds} is significantly higher than f_{res} and this diode has a voltage drop of around 4 V. For the required current levels for the inverter, and in particular for paralleled devices, allowing body diode conduction for a significant part of the duty cycle is highly detrimental to the efficiency of the inverter. Therefore, as the drain-source resonance loop determines the voltage across the switch, the duty cycle of the inverter may be tuned to allow only a short time for diode conduction at no additional switching loss. From a control perspective this insensitivity to the timing of the turn on signal relaxes the requirement for duty cycle timing accuracy and improves the robustness, making the inverter suitable for simple frequency tracking control implementations.

The drain-source waveform under variation of the input current is shown

in Fig 4.8b. As $C_{\text{oss,eq}}$ is very large at low switch voltage (4.1) is not satisfied, but for higher switch voltage the MOSFET capacitance drops such that the static capacitance dominates and the resonance frequency variation for changing voltage level is reduced. Since the ZVS behavior of the inverter at low switch voltage is not a major concern, these waveforms show that f_{ds} could be decreased.

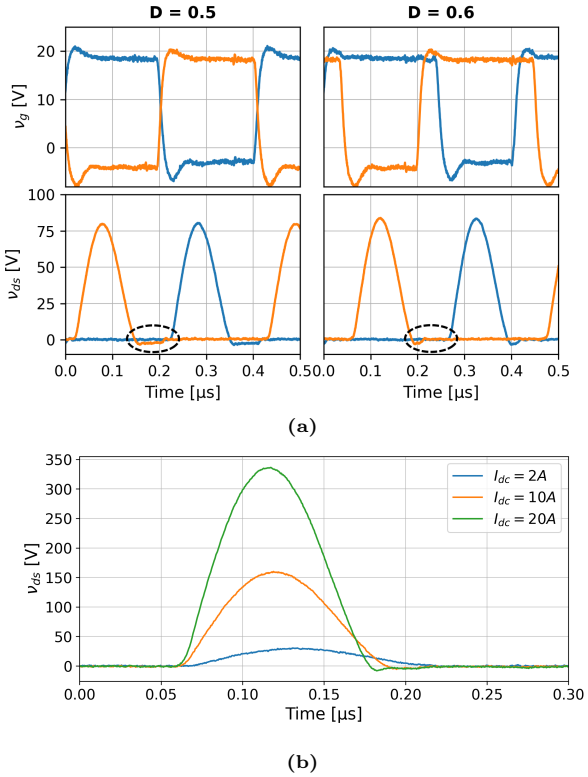


Fig. 4.8: Measured gate- and drain-source voltage waveforms under different operation conditions using the spiral transformer [Paper D]. (a) Duty cycle variation and (b) input current variation.

The main waveforms of the inverter are shown for an input power of 1.35 kW in Fig. 4.9 using the helical high frequency transformer. The small phase shift between the transformer input current and the drain voltages is due to the inherent phase shift of the Rogowski coil used for measuring the current. These waveforms verify the desired operation of the inverter system and only minor influence of undesired parasitic elements. However, from thermographic camera measurements it was found that the temperature of the windings increase rapidly above an input power of 1 kW, and therefore this transformer is unsuitable for higher power operation.

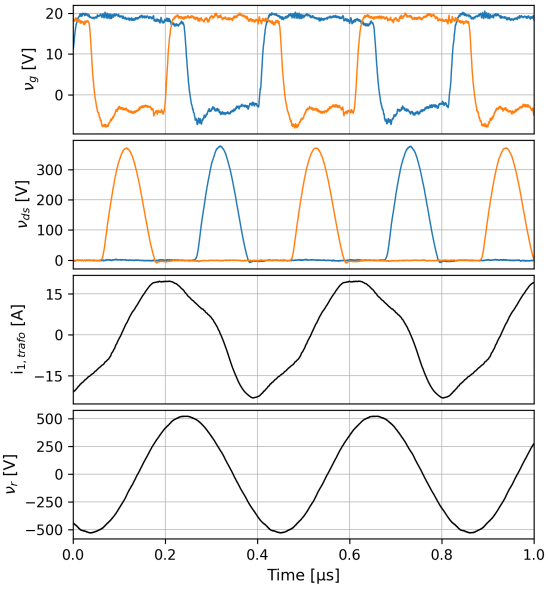


Fig. 4.9: Voltage and current waveforms of the inverter at 1.35 kW input power using the transformer shown in Fig. 4.4.

The power level was increased using the transformer in Fig. 4.5. For higher input power levels of 1.6 kW the resonant tank voltage and current is shown in Fig. 4.10, from which the approximate apparent load resistance in this measurement configuration can be observed at 1.4 Ω. The Rogowski coil transducer was not used above this resonant tank current level due to voltage limitations of the coil.

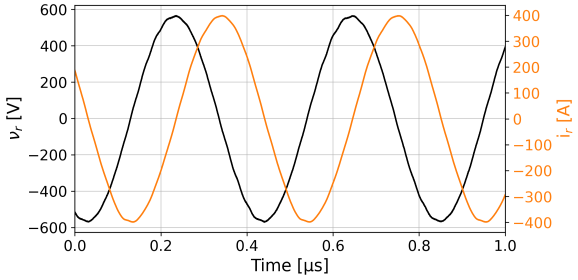


Fig. 4.10: Measured resonant tank voltage and current at 1.6kW input power. [Paper D]

As was reasoned in section 2.1, higher order harmonics or parasitic oscillations in the resonant tank current are highly undesirable for FZ processing. Observing

Fig. 4.10 the voltage and current waveforms of the resonant tank are nearly ideal sinusoids in contrast to the CSRI system presented in chapter 3.

The inverter was tested up to an input power level of 5 kW with the measured waveforms shown in Fig. 4.11. The measured peak drain voltage of the transistors is 800 V and the width of the voltage waveforms is $\frac{1}{2}T_{\mathrm{ds}} = 112$ ns. The frequency of the drain-source resonance loop is then $f_{\mathrm{ds}} = 4.46$ MHz, which matches well with the predictions from Fig. 4.7. Using the previously measured equivalent load resistance of 1.4 Ω, an estimated 363 kVA reactive power is present in the resonant tank at this voltage level.

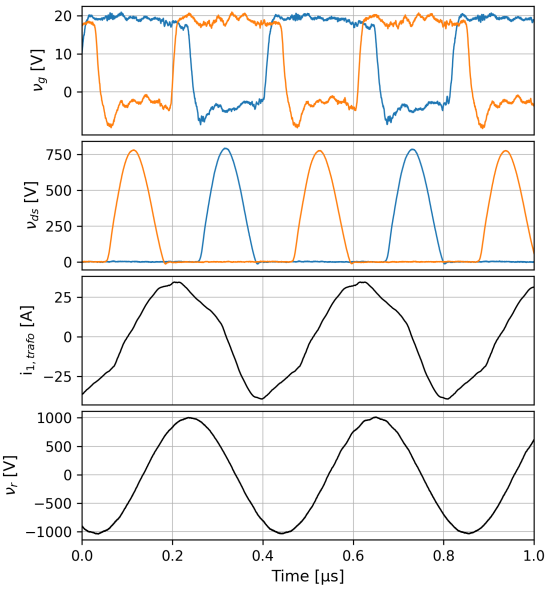


Fig. 4.11: Measured voltages and currents of the inverter at 5kW input power. [Paper D]

The output voltage and current waveforms without significant parasitic oscillations at kilowatt power levels is a major feature of the inherent inclusion of the parasitic elements of the circuit and components in this topology. However, the switch utilization of the inverter operation in Fig. 4.11 is quite low at $c_{\mathrm{pmr}} = 0.127$ compared to the values of the topologies in table 2.4, which is detrimental to efficient inverter performance. This is, in part, because this measurement configuration uses an additional 1/8 tap on the primary of the high frequency transformer to increase the input power level without increasing the input current. As shown in Fig. 4.12 for measurements with and without transformer tap tuned to the same switch voltage, the former outputs significantly more power for moderately increased switch current stress and therefore the operation shown with the solid line measurement has $c_{\mathrm{pmr}} = 0.17$.

This is close to the c_{pmr} of the standard Class E topology operating in nominal conditions from table 2.4 and shows that this implementation of the topology can be tuned to have acceptable switch utilization at kilowatt power levels.

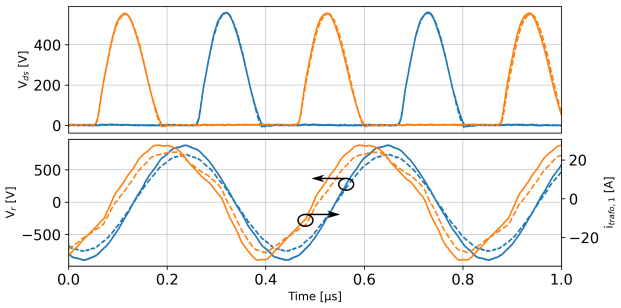


Fig. 4.12: Measured drain-source voltages, resonant tank voltage, and transformer input currents when tapping the transformer and compensating this by slightly adjusting the switching frequency under the same input voltage. The solid lines were measured with parameters $n = 2:7$ and $I_{\mathrm{dc}} = 35.9$ A, while the dashed lines were measured when operating with an additional primary transformer tap 1/8 of a turn and $I_{\mathrm{dc}} = 25.3$ A.

The efficiency of the inverter was measured calorimetrically from the water cooling system after sufficient operation time of the inverter to ensure its components had reached thermal steady state. In this case, for an input power of 4.07 kW, an output power of 3.31 kW was measured in the work coil and steel load, while 0.21 kW was dissipated in the power module. This yields a total system efficiency of 81%, with the power module itself having an operating efficiency of 94%. This is a vast improvement in the power efficiency compared to current vacuum tube oscillators for the FZ process, and can be improved further through optimization of the inverter operating conditions and component design.

4.4 Inverter system scalability

Based on the measured results the presented power module is likely capable of higher power levels than were tested here. Similar analysis to that for the CSRI power module in section 3.2.2 shows that the junction temperature of the MOSFETs is not likely to be close to the operation limit. The inverter was not tested at higher power levels as it requires a redesign of some elements of the test platform, but considering reasonable improvements to c_{pmr} and the waveforms in Fig. 4.11 where an increase of both the transistor voltage and current by up to 50% appears to be feasible, a power level higher than 10 kW seems readily achievable.

While the power module presented in section 3.2 shows that further parallelization of the chosen MOSFET chips is possible, the requirements from (4.1) limits the maximum output capacitance, especially for f_{ds} insensitivity at moderate voltage levels. This parameter must be considered in connection with feasible values of circuit inductance, in particular leakage inductance for the high frequency transformer. The preferred way to further increase the inverter power level is therefore to use multiple modules as shown in Fig. 4.13. Depending on the voltage and power rating of the switching devices and the transformer construction both series and parallel connection of the outputs of the Class E modules seem to be viable ways to reach the required process power level.

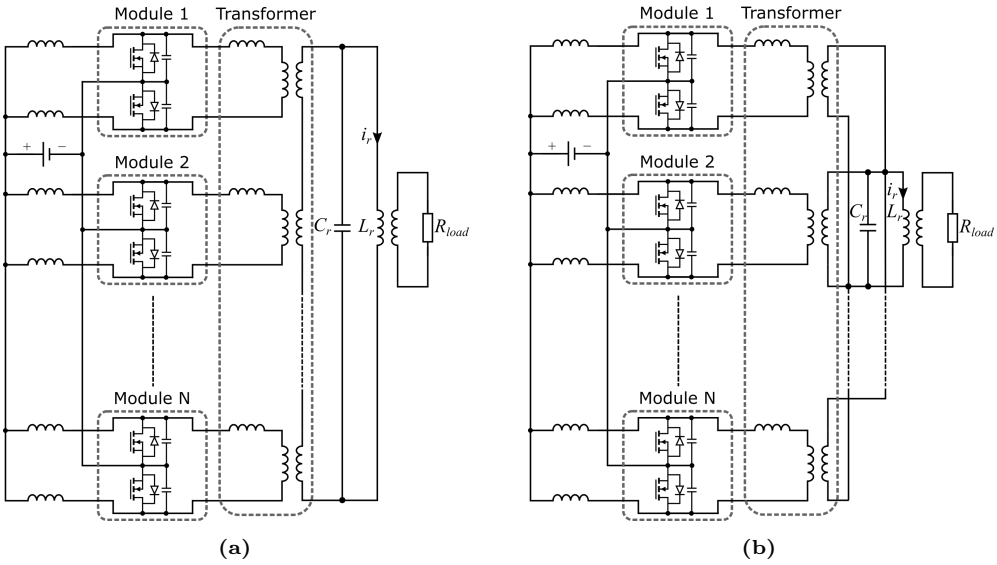


Fig. 4.13: Power module, transformer, and tank connections for a system with multiple Class E inverters. (a) series connection, (b) parallel connection.

4.5 Summary

In this chapter, a Class E push-pull resonant inverter was designed, manufactured, and tested to investigate its merits for MHz induction heating processes. The desired operation of the inverter was verified, and resonant operation was achieved up an input power of 5 kW, with 81% system efficiency and 94% operating efficiency for the presented power module using the developed resonant tank system. The lower sensitivity to drive signal timing and lenient component design are substantial advantages of this topology for this application compared to the CSRI. It was therefore found the inclusions of the parasitic device and

circuit elements in the presented Class E inverter allows for switching waveforms in the MHz range for a power level of multiple kW. The presented system shows promise a scalable solution for the construction of the inverter stage for a full scale FZ process generator system.

Chapter 5

Conclusion & future work

This thesis presents the work done in this project towards realizing a solid state generator for the float zone process. The research objectives as defined in the introduction are

> To investigate the feasibility of expanding the application range of solid state inverters into the area suitable for FZ production.
>
> To expand the knowledge base on the practical usage of WBG-based devices for MHz inverters through design, development, and verification of operation of relevant power module prototypes.

The primary contributions of this work is within the fields of power module design and fabrication and their use in industrial MHz inverters

- The thesis presents an overview of the requirements of a generator for the float zone process, an industrial heating process which has a large potential for energy savings by achieving full utilization of solid state components. Many of the arguments and considerations presented are of general use for RF heating systems.
- The thesis presents multiple power module prototypes utilizing paralleled SiC MOSFETs for MHz operation. These modules demonstrate flexible hard switched gate driving operation of paralleled 1700 V SiC dies, and thereby showcase simple approaches to soft switching paralleled WBG devices in resonant inverters.
- The merits of two different inverter topologies, the current source resonant inverter and the Class E push-pull resonant inverter, were investigated experimentally for MHz induction heating at power levels of multiple kW. The former topology in particular was found to have challenges with the combined frequency and voltage ranges required by the application, and

therefore requires more research to be an employable option. Examples of practical approaches to component and inverter system design, which are often sparse in the published research, have been presented and discussed.

- A inverter system with a Class E push-pull topology utilizing a secondary resonance loop with the transformer leakage inductance for robustness towards both resistive and inductive load variation for MHz induction heating was demonstrated and its merits discussed. This type of inverter is argued to be an attractive candidate for scaling up in power for future FZ generator systems.

5.1 Future work

In the aim towards a full-scale replacement of vacuum-tube generators in FZ production, this research work highlighted areas in need of more exploration. These areas, which are either currently being investigated or planned as future work as part of an upcoming project, are outlined below.

- Increasing the power capability of the test system to experimentally verify the behavior and power limits of the developed the Class E push-pull inverter power module design. In addition, more investigation is needed on the behavior of the inverter under different operating conditions.
- It is envisioned that the developed Class E inverter is well suited for a closed-loop control using a simple frequency tracking system. This feedback system needs to be developed and tested as it is a necessary component in a FZ process with a frequency-varying resonant tank.
- Improving the understanding of the inverter system to develop better predictive simulations of inverter behavior, with the goal of developing a digital twin model to accurately predict component behavior and losses under dynamic load conditions. This work draws on the experience and collaboration with the CoDE[1] project.
- Scaling up the power level of the resonant inverter system to run full-scale FZ processes. From the work in this thesis, it is envisioned how the generator components of a high power system could be designed and combined, and these concepts need to be demonstrated in an industrial environment.
- Investigate to which degree the systems and knowledge developed here are transferable to other RF heating applications. Generalized processes

[1] Center of Digitalized Electronics (CoDE), Aalborg University, an ongoing project on digital design and modeling of power electronics, https://vbn.aau.dk/en/projects/center-of-digitalized-electronics-code

such as dielectric- and induction heating have many similarities from a generator perspective, but their inherent differences demand a more detailed comparative analysis of the specific inverter topology options to determine their attractiveness for each application.

Chapter 6

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Part II

Appended papers

Paper A

Challenges and opportunities in the utilization of WBG devices for efficient MHz power generation

Thore Stig Aunsborg, Sune Bro Duun, Christian Uhrenfeldt, and Stig Munk-Nielsen

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Challenges and opportunities in the utilization of WBG devices for efficient MHz power generation

Thore Stig Aunsborg, Sune Bro Duun, Christian Uhrenfeldt, and Stig Munk-Nielsen

Abstract

This paper reviews major challenges in applying solid state technology to energy efficient industrial high frequency high power generation. Comparisons to vacuum tube technology related to operating frequency, power handling, and thermal design are presented. Challenges and opportunities in applying wide band gap devices to this field are discussed, and recent progress in advancing solid state technology into this area is considered at device and module levels.

A.1 Introduction

Solid state technology has replaced vacuum tubes in almost all low power applications, and in low frequency high power applications. However, within the high power and high frequency regime, vacuum tube technology is still widely used for power amplification in power transmission and amplification systems [1], [2]. Generation of multiple kW of power for industrial processes in the upper medium-frequency (MF) and high-frequency (HF) regimes has traditionally been the realm of vacuum tubes, but in recent years, they are receiving increased competition from solid state technology in these high power areas, in no small part due to the continuous improvement of chip topologies and the commercialization of wide band gap (WBG) devices. The high-speed performance of these devices have blurred the line between the regimes of power conversion by traditional power electronics and RF technology, and are enabling the possibility for cheaper and more efficient HF solid state power generation [3].

In response to this emerging application area for WBG devices, this paper will identify challenges and opportunities with state-of-the-art technologies for power generation in the MHz frequency regime. In section II we describe some inherent differences between solid state technology and vacuum tubes, and discuss efficiency considerations for different circuit topologies and power amplifier systems. In section III the possibilities arising from WBG technology are presented, while section IV discusses the challenges in its application in the MHz switching regime. From these perspectives, section V presents recent progress towards efficient MHz power generation.

A.2 High frequency power delivery processes

Several industrial processes utilize high power generators in the MHz range. Some common applications include dielectric heating, induction heating, and plasma generation [3]–[5]. While the challenges for power generation for each application have some overlap, the available approaches are highly linked to the requirement for output voltage, frequency regime, linearity, efficiency, system size, and protection requirements.

The output frequency is a very important parameter in these processes. In plasma processing, the frequency is usually confined to the ISM bands (13.56MHz and harmonics) to avoid conflict with regulation. In dielectric heating and induction heating, the desired frequencies are largely determined by the penetration depth of the RF field into the material [6]. In addition, the voltage and power requirements for these processes can be a challenge, with some heat treatment applications requiring several kilovolts and 10's of kilowatts, making gridded vacuum tubes the most frequently used technology in these industrial settings, as tube oscillators commonly employ tubes manufactured to operate above 15kV [7], [8].

A.2.1 Efficiency and circuit topologies

The conversion of power from DC to high frequency AC will always result in significant power losses as heat. In managing the thermal dissipation and avoiding overheating of the active devices vacuum tube systems have intrinsic advantages due to a large direct cooling area (see fig. A.1), whereas the semiconductor module structure can limit the attainable power density of solid state amplifiers [2], [9]. There are two general ways to increase the power density of an amplifier without putting additional stress on the active components: (1) increase the cooling efficiency e.g. through direct cooling, fluid flow optimization, high operating temperatures, or improved packaging, or (2) decreasing the amount of generated heat, i.e. increasing the power efficiency. It is thus important to choose an appropriate circuit topology that facilitates higher efficiency, which can be accomplished using what is called switched-mode power amplifiers in RF terminology, the same circuits which are known in the field of power electronics as inverters [10]. Here, these terms will be used interchangeably.

Depending on the application of a given type of amplifier, numerous amplifier circuit types (or "classes") are available (shown in fig. A.2 using MOSFETs as an example). Contrary to switched-mode amplifiers, amplifiers which operate in the saturation region with a constant DC bias voltage, such as class A, class B, or class AB (shown in fig. A.2a), can be employed in applications where the linearity of the signal is a high priority. These, however, have theoretical maximum efficiencies of 78% [11]. In applications of power delivery where input

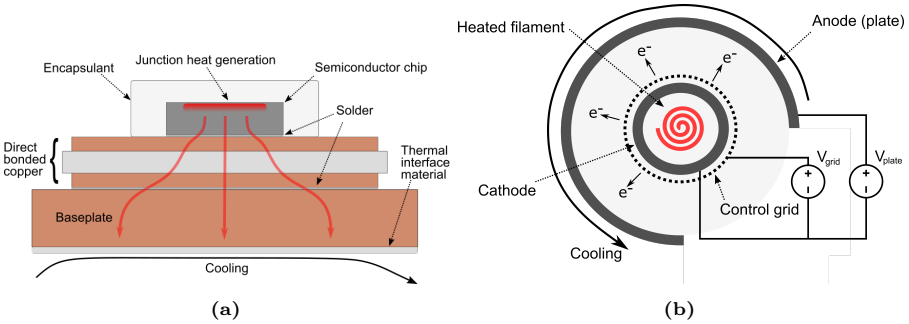

Fig. A.1: Schematics of the considered technologies showing the differences in heat transfer and cooling. a) cross-section view of a traditional semiconductor power module showing the heat dissipation path from junction to cooling system. b) axial view of a vacuum triode, illustrating the direct cooling of the plate.

signal distortion is less critical, class C amplifiers with high reverse bias can be used to supply a narrowband tuned circuit with improved efficiency but reduced power output, which is a common configuration for vacuum tube oscillators, with typical power efficiencies around 75%. The approach in switched-mode power amplifiers (fig. A.2b) is to drive the devices in the triode region between the ON and OFF-states, thereby using the device as a switch, such that a maximum theoretical efficiency of 100% can be achieved in class D or class E (or derivations). This efficiency requires ideal components however, and real devices will experience both switching and conduction losses.

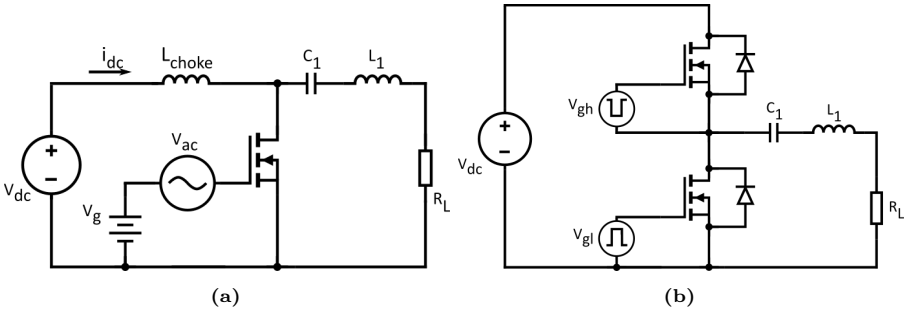

Fig. A.2: Basic circuit topology examples of the two main types of power amplifiers. a) linear amplifier circuit with a tuned output. The amplifier may operate in either class A, B, or C depending on bias V_g. b) switched-mode class D voltage source amplifier with a series resonant tank network.

Different types of semiconductor components can be used in high frequency amplifiers, including both lateral and vertical devices. Several groups have demonstrated high power solid state amplifiers operating in both the HF and VHF regimes, frequently operated in class AB using lateral devices [12]–[15].

These types of RF devices, such as LDMOS and low-voltage GaN HEMTs, are developed for use in RF amplifiers, with many desirable features for high frequency operation such as high gain, high efficiency, and low parasitic capacitances and inductances [16], [17]. However, although lateral RF transistor products have entered the kW range for single components [18], the output power of these devices in any amplifier configuration is still quite limited due to comparatively low voltage rating, and the parallelization requirement to reach high power levels also leads to considerable power losses, degrading efficiency, and risk of disadvantageous operating conditions due to phase mismatches [1], [3], [19]. The low operating voltage for these devices also necessitates high current with accompanying ohmic losses, and for high output voltage requirements, the comparatively low breakdown voltage of these devices sets high requirements for the impedance transformation network [16].

A.3 Emerging WBG devices

In industrial processes where power efficiency is a primary objective, vertical devices operating at high voltages are highly attractive, as multiple kW of power can be achieved in switched-mode amplifiers using a minimum number of components [20]. However, these devices have traditionally been useful only at lower operating frequencies up to a few hundred kHz due to need for low on-state resistance, leading to large chip sizes with accompanying large internal capacitances limiting transient performance for high power components, and paralleling a large number of RF devices has been the only real alternative to gridded tubes in these applications.

Wide band gap devices have been providing real competition to Si devices, particularly in high power and frequency applications. The material properties result in a multitude of beneficial performance parameters, the most important one being the critical electric field E_c, which is defined as the maximum field strength at the onset of breakdown [21]. The importance of E_c is illustrated by Baliga's Figure of Merit (BFOM) [22], which assesses the drift region resistance, and Baliga's High Frequency Figure of Merit (BHFFOM) [23], which assesses the product of resistance and input capacitance in unipolar devices

$$R_{on,sp} = \frac{4V_{br}^2}{\epsilon_r \mu_n E_c^3} \Rightarrow \text{BFOM} = \epsilon_r \mu_n E_c^3 \tag{A.1}$$

$$\frac{1}{R_{on,sp} C_{in,sp}} = \frac{1}{2} \mu_n E_c^2 V_G^{1/2} V_{br}^{3/2} \Rightarrow \text{BHFFOM} = \mu_n E_c^2 \tag{A.2}$$

where V_{br} is the breakdown voltage, ϵ_r is the relative permittivity, μ_n is the electron mobility, E_c is the critical electric field, and V_G is the gate voltage. A larger FOM indicates lower power loss for the semiconductor device for a given chip area. Because these FOMs assess semiconductor material properties they

are only applicable to comparing semiconductor devices, whereas vacuum tubes which have different operation mechanisms are more commonly compared based on the power density of different tube designs [24]. Based on eqs. (A.1) and (A.2), BFOM and BHFFOM are calculated in table A.1 for Si, SiC, and GaN, and show the large opportunity in utilizing WBG materials. The improved electrical parameters and particularly E_c for SiC and GaN, along with the possibility for higher operating temperatures, open the design space to the construction of devices with lower on-state resistance, higher breakdown voltage, and/or lower capacitances than Si, depending on the requirements for the application.

Table A.1: Key material parameters for semiconductors for fast-switching power components [10]

	Silicon	4H-SiC	GaN
Band gap, E_g (eV)	1.12	3.23	3.39
Critical E-field, E_c (MV/cm)	0.3	2.5	3.75
Relative permittivity, ϵ_r	11.7	9.66	8.9
Electron mobility, μ_n (cm^2/Vs)	1350	900	1265
BFOM (rel. to Si)	1	319	1392
BHFFOM (rel. to Si)	1	46	146

This enables WBG transistors to switch faster with lower power loss than Si transistors while having higher voltage ratings [25], resulting in much smaller weight and size for a system of comparable power rating compared to Si, and allows for higher switching frequency and lower cooling requirements. Continuous improvement in these devices in recent years have increased the interest in using switch-mode devices in the MHz regime in high power applications with high efficiency requirements [26], [27]. Fig. A.3 shows the power ranges and frequency regimes of common families of semiconductor devices and gridded vacuum tubes, and illustrates the prospect of expanding the application range of solid state technology in efficient HF power generators using WBG devices.

A.4 Challenges in utilization of WBG devices

In order for switched-mode devices to operate in the MHz range, it is usually necessary to dramatically reduce the switching losses compared to hard-switching inverters. This can be achieved using soft-switching mechanisms that avoid the concurrency of high voltage/current at turn on and/or turn off by using reactive elements to allow switching at the zero crossings [31]–[33]. However, even with circuit topologies that render switching losses of the power devices negligible, there are numerous challenges to achieving high efficiency operation

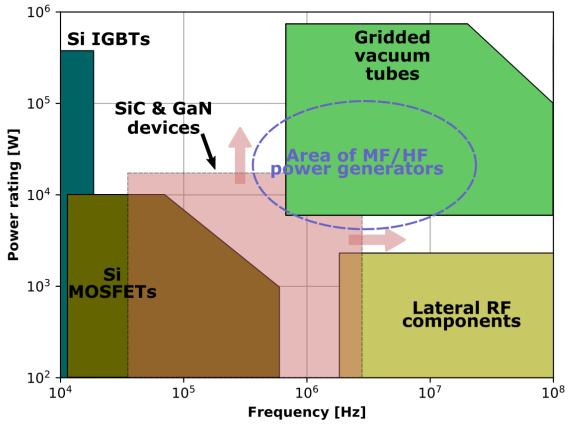

Fig. A.3: Estimation of the operating ranges of devices used in power generation and conversion. The circled area shows the area of interest here. The arrows indicate the frequency and power expansion possibilities for WBG devices. Inspired by [28]–[30].

of power inverters in the HF regime. The most important of these, along with solution or mitigation techniques given in the literature, are presented below.

A.4.1 Gate driving

Although WBG devices can have much smaller chip area than Si for a given V_{br} and $R_{ds,on}$, the input capacitance for power devices is a major challenge in the MHz switching regime. Conventional gate drivers are hard-switched in a push-pull configuration and deliver a square wave voltage to the gate of the power component. This means that energy stored in the input capacitance is dissipated each cycle, which results in power loss and cooling issues, and requires the driver to deliver very high peak currents for fast switching [34], [35]. The two primary factors limiting the frequency of the gate drive, the time constant of the gate resistance and input capacitance and the power dissipation, require careful consideration [32].

High speed gate drivers suitable for RF operation are commercially available, but managing their power dissipation and the gate loop inductance to reduce the gate resistance is a challenge. An approach to solving this issue is to integrate the gate driver on a power module substrate, both allowing fast switching speed due to the absence of an external gate resistance and efficient thermal management [27], [36], or integrating the driver in the same package as the chip as is sometimes done for GaN devices [37]. For higher frequencies, the driver losses may contribute a significant amount to the total power losses, especially at light loads. To combat this issue, several authors have employed the use of a

resonant gate driver using an inductive element (e.g. the parasitic inductance of the gate loop) to resonate with the parasitic capacitance of the power device, reducing the driver requirements at the cost of circuit complexity and control bandwidth [34], [38]–[40].

No matter the driver structure, the theoretical maximum operating frequency is limited by the RC-network of the power device input capacitance C_{iss} and gate resistor R_g to $f_{max} = \frac{1}{4R_gC_{iss}}$ for 50% duty cycle, ignoring efficiency considerations and practical layout [41]. This figure is shown for selected devices in table A.2. Low on-state losses are important to improve efficiency especially for soft-switching inverters, and it is seen that commercially available WBG devices with low $R_{ds,on}$ have the capability of operating in the frequency regime considered in this paper.

Table A.2: Characteristics of selected WBG power devices with low on-state resistance.

Device	Type	V_{br}	$R_{ds,on}$	C_{iss}	R_g	f_{max}
SCT3040KL	SiC MOSFET	1200V	40mΩ	1337pF	7Ω	27MHz
C2M0080170P	SiC MOSFET	1700V	80mΩ	2250pF	2Ω	56MHz
UJ3N120070K3S	SiC JFET	1200V	70mΩ	985pF	3.3Ω	77MHz
GS66508T	GaN HEMT	650V	50mΩ	260pF	1.1Ω	874MHz
GPI65060DDK	GaN HEMT	650V	25mΩ	420pF	2.18Ω	273MHz

A.4.2 Thermal management

It may appear attractive to utilize the ability of WBG devices to operate at higher junction temperatures than Si, allowing more efficient cooling through the larger thermal gradient, similar to tube technology [9]. However, this requires entirely new packaging concepts, and most commercial WBG modules thus have the similar junction temperature limit to Si modules due to current packaging technology limits [42]. Thus, the advantages of the material properties of WBG devices cannot be harnessed without proper packaging technology [43].

Additionally, the need for more efficient cooling is increased due to the generally smaller sizes of WBG chips. Many new packaging concepts have been developed to meet the heat management requirements, in particular using power modules instead of discrete packaged devices. Improved die attach methods such as silver sintering or transient-liquid phase bonding can allow higher operating temperatures and reduce the thermal path from chip to substrate [44], [45], and the use of high thermal conductivity ceramics such as AlN or Si_3N_4 instead of standard Al_2O_3 also improve the power handling capabilities [42]. Other technologies are employing double sided cooling of the power semiconductors, and directly bonding to a heat sink to avoid using any thermal interface material [46]. These types of improvements in the management of device losses are a

key enabling factor for pushing WBG devices to higher power levels through improved packaging concepts.

A.4.3 Electrical parasitics

In order to enable high speed switching, careful design and optimization of modules and discrete devices for mitigation of parasitic capacitance and inductance is required compared to slower Si modules. Much research has been focused on optimizing packaging technologies for low switching loop inductances to allow fast switching. New package designs have improved the high frequency performance of discrete devices [43], [47]. For power module design, a few examples of optimization techniques include the integration of decoupling capacitors [48], flip-chip assemblies [49], hybrid DBC/PCB structures [50], and 3D inductance cancellation designs [51]. Fast switching of high voltages can lead to issues with parasitic capacitive couplings, but these can likewise be reduced through optimizations of power module layout [52]. While new packaging schemes introduce new possibilities for performance optimization, tradeoffs must often be made between thermal performance, parasitic reduction, and cost of manufacture [42], [53].

A.5 Current developments in MHz WBG inverters

The solutions presented above highlight some approaches to better utilize WBG devices, enabling the expansion of their applicable power and frequency ranges. The selected work summarized in table A.3 shows the feasibility of advancing solid state technology into the high power HF regime, the use of various resonant circuit topologies to achieve high efficiency, and the application of optimized RF packages to utilize the performance of WBG devices. Although single switch topologies have lower output power and higher voltage stress of the switching device than resonant bridge topologies [54], these are frequently employed in the MHz range, due to difficulty in reliably driving high side switches at high switching transients, and the high operating frequency resulting in severe gate signal timing requirements [10]. Nonetheless, it is seen that efficiencies above 90% at multiple MHz output frequency can be achieved using switched-mode devices in different topologies, and that both GaN and SiC devices are being used for kW MHz resonant inverters.

Current GaN devices on the market are limited by their lateral design to $V_{br} = 650$V due to electric field limits of the used materials, but some researchers expect the commercialization of higher rated vertical GaN devices in the coming years [61], [62]. SiC device maximum rating on the market is currently 1.7kV, expected to expand to 3.3kV in the near future. The challenge

Table A.3: Selected recent efforts in HF power conversion and generation.

Authors/year	Targeted application(s)	Power switches	Package	Circuit topology	Operating frequency	Output power	Efficiency
Haehre et al. (2014) [55]	HF power generators	1200V SiC MOSFET	TO-247-3	Class D (full bridge)	2.4 MHz	2.4 kW	90.6%
Ghodke et al. (2016) [56]	Plasma source	900V SiC MOSFET	TO-263-7	Class D (half-bridge)	2 MHz	3.4 kW	N/A
Choi et al. (2016) [57]	Wireless power transfer	a) 1200V SiC MOSFET b) 650V eGaN HEMT	a) DE150 b) GaNpx	a) single ended class ϕ_2 b) push-pull class ϕ_2	6.78 MHz	a) 2.2 kW b) 2 kW	a) 93% b) 96%
Guo et al. (2016) [58]	Isolated DC/DC converter	1200V SiC MOSFET	Bare die	Full-bridge LLC	1.2 MHz	4 kW	97%
Nguyen et al. (2017) [59]	Wireless power transfer	650V eGaN HEMT	GaNpx	Class DE (5 half-bridges)	13.56 MHz	4 kW	96.5%
Denk et al. (2018) [60]	HF power generators	1200V SiC MOSFET	ISOPLUS-SMPD	Full-bridge	2.5 MHz	25 kW	92.5%

of high breakdown voltage in vertical devices comes with the requirement of increased die area for equal current handling, leading to higher capacitances [16], [17]. For lower voltage, higher switching frequency, GaN devices seem to achieve higher efficiency than SiC due to very low capacitances and high transconductance, while the vertical SiC devices offer higher breakdown voltages and better product maturity [29].

In order for solid state technology to compete with vacuum tubes in processes requiring multiple kilovolts, higher rated modules are of great interest. For lower frequency applications, SiC devices with V_{br} up to 15kV have been investigated [63]. As previously discussed, the impact on power handling, efficiency, electrical layout, and gate driving means that using higher V_{br} devices at MHz frequencies is a challenge. To exemplify an attempt to push the voltage rating of MHz power inverters, a power module we developed based on 1700V SiC MOSFETs is shown in figure A.4. This module was designed with the challenges presented with this paper in mind, and features integrated gate drivers, high thermal conductivity ceramic, and a symmetrical layout of low-inductive switching loops, and will be tested for efficiency and achievable power density to further investigate the feasibility of using high V_{br} WBG devices for MHz power generation.

A.6 Conclusion

The field of power generation in the MHz regime has traditionally been the realm of vacuum tubes, and challenges associated with applying semiconductor technology to this regime have been presented. It has been shown that with the improvement of device technology and the utilization of WBG materials, the power range of switched mode solid state modules in this frequency regime is expanding. Continuous improvements in both the parameters of power

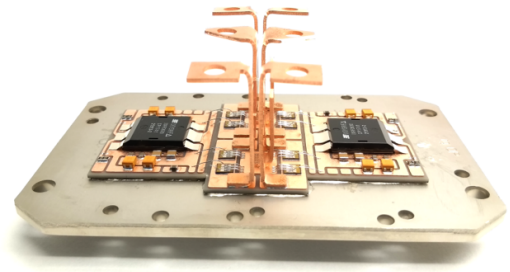

Fig. A.4: Photograph of power module designed for resonant MHz operation based on 1700V SiC MOSFETs.

devices and the electrical and power handling performance of MHz power modules are apparent, promising efficient and cost-effective solutions to MHz power generation. These factors enable solid state technology to provide real competition to vacuum tubes in this field.

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Paper B

Development of a current source resonant inverter for high current MHz induction heating

Thore Stig Aunsborg, Sune Bro Duun, Stig Munk-Nielsen and Christian Uhrenfeldt

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Development of a current source resonant inverter for high current MHz induction heating

Thore Stig Aunsborg, Sune Bro Duun, Stig Munk-Nielsen, and Christian Uhrenfeldt

Abstract

High frequency industrial induction heating processes typically employ resonant inverters to reach high efficiency at high power levels. Advancements in wide band gap (WBG) device technology has made it feasible to push the possible frequency of these processes into the MHz regime using solid state technology. Several topologies can be applied, each with advantages and drawbacks. This paper presents a current source resonant inverter (CSRI) employing a custom designed power module utilizing 1700V SiC MOSFETs for MHz operation of a high-Q resonant tank for induction heating, which presents new challenges in the inverter module design. An integrated gate driver structure is demonstrated driving four MOSFETs in parallel in MHz operation. Theoretical analysis predicts substantial parasitic influence on inverter operation, and thus an inverter is constructed to provide experimental verification of MHz operation, while the challenges associated with high frequency CSRI operation are discussed. In the experimental inverter setup, the fabricated power module achieves >90% efficiency for a calculated reactive power of 170 kVA and 2.3 kW output power during unloaded operation, validating the inverter design for extension to higher power loaded operation.

B.1 Introduction

High power high frequency electrical power is used in several industry applications where power delivery of multiple kW at frequencies of hundreds of kHz to tens of MHz is required. These processes include induction heating, dielectric heating, and plasma processing [1]–[3]. Inverter systems based on solid state components are commercially available for frequencies up to several hundred kHz, with MOSFET-based inverters dominating the upper frequency range [4]. In recent years, several researchers have investigated the feasibility of pushing the frequency limits of single power inverters of several kWs into the MHz regime, primarily facilitated by the usage of wide band gab (WBG) semiconductor devices [5]–[8].

In the design of high power generator systems for induction heating applications at MHz frequencies, oscillators based on vacuum tubes are commonly used

due to the high frequency and power requirements of the processes. This is e.g. the case for some industrial implementations of zone refining processes for the growth and purification of crystals, where induction heating is applied that may require frequencies of multiple MHz [9], [10]. However, the efficiency of vacuum tube oscillators is low, leading to considerable energy loss in these processes [11], [12]. Solid state technology promises improved efficiency in these applications, but as single turn coils are commonly used, the equivalent resistance of the load may be very low, demanding very high coil current to reach the required power deposition in the load [1]. Additionally, common to induction heating applications, coupling between coil and load can vary greatly depending on workpiece temperature, material, and geometry, requiring the power inverter to be adaptable to changing resonant frequency and loading while maintaining efficiency [13]. Combined with the high frequency requirements, this requires careful design of the inverter system to achieve high efficiency.

Several circuit topologies have been applied to induction heating processes, with the common characterization as either current source resonant inverters (CSRI) or voltage source resonant inverters (VSRI) [14]. The choice of topology for a particular application is largely determined by the application demands, such as the desired operating frequency, power output, load impedance, and process specific parameters such as working coil short-circuit probability [15]. For low impedance coils designed for loads with low equivalent resistance, the current in the induction coil must be high to deposit appreciable power in the workpiece, which can necessitate the use of a transformer with considerable losses, especially for high frequency operation [16], [17]. Thus, the conventional wisdom is that voltage source systems are preferred for high impedance coils with multiple turns, while current source systems are better suited for low impedance, single turn coils [1], [18]. However, not much attention has been paid to the application of CSRIs based on solid state power components in this frequency regime, likely in part because the requirements for switching speed, power loss handling, and parasitic influence mitigation puts great demands on inverter design. This paper aims to investigate the feasibility of such an implementation.

The coupling to the load is significantly lower for single turn coils than for high impedance coils. Thus to achieve sufficient power delivery a high current flow in the coil is required, which at MHz frequencies means that a relatively high coil terminal voltage must be applied even for low impedance coils. Using lower voltage switches and a transformer to scale up the coil voltage can be attractive, but this option increases switch current stress, increases losses and component count, and introduces parasitics from the non-ideality of the transformer. Utilizing a transformerless CSRI avoids these issues, but requires the use of relatively high voltage switches. Wide band gap devices such as SiC MOSFETs are promising candidates for this type of application, combining high voltage blocking capability with fast switching action [19], [20]. Due to this, SiC

has been successfully applied to both domestic and industrial induction heating in recent literature, especially for high frequency applications [21], [22]. Even with this approach, however, it can be necessary to parallel switching devices to improve the inverter current handling capabilities to deliver the required power to the load. The use of parallel devices increases both the gate drive requirements and the effective device parasitics, which enhances the need to pay close attention to inverter interconnections and layout to ensure proper functioning of the system at MHz frequencies. The influence of the parasitic elements in the operation of a high frequency CSRI is most pronounced at very high quality factor (Q-factor) of the work coil, which is thus an important operating point for induction heaters with highly variable loads. The highest attainable Q-factor, i.e. unloaded operation, is then a relevant case study to investigate the feasibility of the CSRI using paralleled high voltage SiC MOSFETs in the MHz frequency regime.

To investigate this, this paper aims to demonstrate MHz operation of a bidirectional CSRI power module operating in conjunction with an unloaded parallel resonant tank. The challenges associated with this process, i.e. the simultaneous requirements of frequency, resonant current, power, and voltage ranges, demands special attention to critical design parameters such as parallelization strategy, loss handling, gate driving, parasitic influences in the inverter system, and control requirements. These challenges and the proposed design solutions for utilizing paralleled SiC MOSFETs in MHz operation under these requirements will thus be the focus area of this work. Therefore, to address the need for a flexible power module capable of operating with an industrially relevant resonant circuit, a prototype power module is developed. This module showcases possible approaches to overcoming the challenges discussed above by using an integrated gate driver structure in combination with a highly symmetric power module layout with paralleled 1700V SiC MOSFETs and an inverter system designed for high frequency operation. The inverter fundamentals and specifics relevant to this application are presented in section 2. The developed power module and resonant tank, along with important design considerations, are shown and discussed in sections 3 and 4, respectively. Experimental tests of the integrated gate drive circuitry are presented in section 5, along with demonstrations of resonant operation in unloaded conditions.

B.2 Bidirectional CSRI operation

Although the CSRI topology is well known for induction heating, applying it in the MHz regime using power MOSFETs requires close attention to key design parameters for low impedance coils and high power operation. Therefore, a number of key aspects of the CSRI topology are revisited here and the impact of parasitic elements is analyzed to elucidate important system design parameters.

The most common CSRI configuration employs series diodes to create switches that are unidirectional in current, while another option is using the CSRI topology without the series diodes, as is shown in figure B.1. In the CSRI, the input inductors L_{choke} are much larger than the resonant inductor L_c, so in steady state the DC current is constant and the input current to the resonant tank is a square wave. When series diodes are included, the output power level can be controlled through the switching frequency, whereas this is done by controlling the input current level for the diodeless version. The advantage of omitting the diodes, besides the reduced component count and cost, is that if switching operation at the resonant frequency is desired, not using diodes eliminates the losses associated with their on-state voltage drop (mainly relevant at low switch voltage) and reduces the turn-on losses of the switches by not clamping the voltage of the output capacitance prior to the turn-on event, which is particularly relevant at high operation frequency and high switch voltage as is the case here [23].

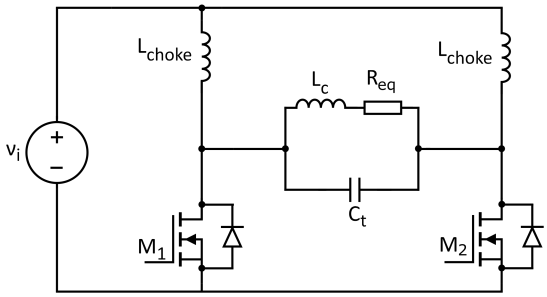

Fig. B.1: Schematic of the bidirectional current source resonant inverter (CSRI).

The induction heating coil is modelled as an inductance in series with an equivalent resistance, which includes both the coil resistance and the resistance of the work piece referred to the coil. The quality factor of the coil is defined as the ratio of reactive to real power

$$Q = \frac{|P_{react}|}{P_{real}} = \frac{\omega L_c}{R_{eq}} \tag{B.1}$$

Considering ideal operation of the resonant tank with coil inductance L_c and tank capacitance C_t as shown in figure B.2, the input current to the resonant tank by KCL in the Laplace domain is

$$i_{tank}(t) = i_{Ct} + i_{Lc} \;\Rightarrow\; i_{tank}(s) = sCV_{tank} + \frac{V_{tank}}{sL + R_{eq}} \tag{B.2}$$

Defining the undamped natural resonance frequency ω_n and the damping

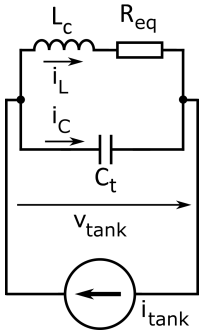

Fig. B.2: Parallel resonant tank of the CSRI.

ratio ζ

$$\omega_n = \frac{1}{\sqrt{L_c C_t}}, \quad \zeta = \frac{R_{eq}}{2}\sqrt{\frac{C_t}{L_c}} \tag{B.3}$$

gives the impedance

$$\begin{aligned} Z(s) = \frac{V_{tank}(s)}{I_{tank}(s)} &= \frac{sL_c + R_{eq}}{s^2 L_c C_t + sC_t R_{eq} + 1} \\ &= (sL_c + R_{eq})\frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \end{aligned} \tag{B.4}$$

which is a well-known second order system. Transferred to the frequency domain, the impedance becomes

$$\begin{aligned} Z(s)|_{s=j\omega} = &\frac{R_{eq}}{(1-\omega^2 L_c C_t)^2 + (\omega C_t R_{eq})^2} \\ &+ j\frac{\omega(L_c - \omega^2 L_c^2 C - C_t R_{eq}^2)}{(\omega C_t R_{eq})^2 + (1-\omega^2 L_c C_t)^2} \end{aligned} \tag{B.5}$$

Zero current and zero voltage switching will occur at the resonance frequency ω_r. The condition for this is tied to an impedance phase angle of zero, yielding

$$\angle Z(j\omega_r) = 0 \Longrightarrow \omega_r = \sqrt{\frac{L_c - C_t R_{eq}^2}{L_c^2 C_t}} = \omega_n\sqrt{1-4\zeta^2} \tag{B.6}$$

Assuming high Q-factors, the damping term becomes small and $\omega_r \approx \omega_n$. In this case, the magnitude of the impedance at the resonance frequency becomes

$$|Z(\omega_r)|_{\omega_r=\omega_n} = \sqrt{\frac{L_c(C_t R_{eq}^2 + L_c)}{C_t^2 R_{eq}^2}} = R_{eq} Q\sqrt{Q^2+1} \tag{B.7}$$

The resonant tank acts as a filter at the resonant frequency, and thus only the first harmonic of the square wave tank current is considered, the RMS value of which is expressed as

$$I_{tank} = \frac{\sqrt{2}}{\pi} I_{in} \tag{B.8}$$

By similar analysis to that for the impedance, the transfer function for the current at the resonant frequency (gain) can be approximated assuming high Q-factor [24]

$$\frac{I_{res}(j\omega_r)}{I_{tank}(j\omega_r)} = \frac{1}{1 - \omega_r^2 L_c C_t + j\omega C_t R_{eq}} = -jQ \tag{B.9}$$

The power consumed by the equivalent resistance in this case is then expressed from eqs. B.8 and B.9 as

$$P_{out}(\omega_r) = I_{res}^2(\omega_r) R_{eq} = \frac{2 I_{in}^2 Q^2 R_{eq}}{\pi^2} \tag{B.10}$$

Applying the previous high-Q assumption that $\omega_r = \omega_n$, the impedance at the resonance frequency is purely real, such that $|Z(\omega_r)| = Z(\omega_r) = V_{tank}/I_{tank}$. Using this and the expression for the input power $P_{in} = V_{in} I_{in}$, the efficiency η can by written using eq. B.7

$$\eta = \frac{P_{out}}{P_{in}} = \frac{2 I_{in}}{\pi^2 I_{tank}} \frac{V_{tank}}{V_{in}} \tag{B.11}$$

Assuming $\eta = 1$ and high Q, the voltage transfer function from input voltage V_{in} to output voltage V_{tank} is then

$$\frac{V_{tank}(j\omega_r)}{V_{in}(j\omega_r)} = \frac{I_{tank}\pi^2}{2 I_{in}} = \frac{\pi}{\sqrt{2}} \tag{B.12}$$

resulting in a peak voltage for the tank and the switches of πV_{in}.

The analysis thus far has considered the ideal case of an inverter without parasitics. To conserve the basic operating scheme and the general validity of equations B.1-B.12 when considering real components, careful attention must be paid to the physical construction and control of the system.

As is apparent from eq. B.9, a CSRI with a high Q-factor of the resonant tank circuit allows large resonant current with comparatively low switch current stress. Another advantages of the CSRI is that the parasitic output capacitance of the transistors are absorbed in the resonant tank capacitance since one of the switch capacitances will always be in parallel with the tank. For this reason, load resonant soft-switching can be achieved even considering device parasitics. This means, however, that the switch which is ON will also conduct the reactive current of the output capacitance of the other leg (blue in figure B.3)

$$i_{react} = i_{C_{tank}} \frac{C_{oss,eq}}{C_{tank}}, \quad C_{oss,eq} = \frac{\int_0^{V_{ds}} C_{oss}(V)\mathrm{d}V}{V_{ds}} \tag{B.13}$$

where $C_{oss,eq}$ is the charge equivalent output capacitance of the MOSFET [25]. In light load conditions, this current can be of the same or higher magnitude

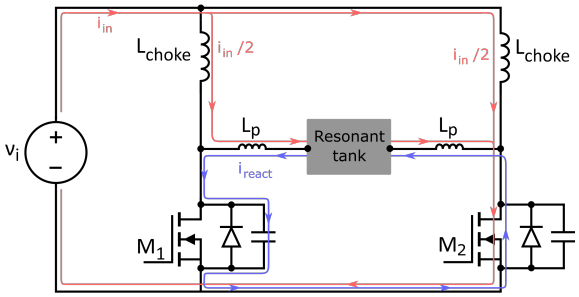

Fig. B.3: Schematic of the CSRI illustrating the current paths during a quarter of a switching cycle.

than the DC current when using paralleled power MOSFETs, signifying a large deviation from the ideal circuit for the unloaded condition. Additionally, since there exists a non-zero loop inductance L_p as shown in figure B.3, there will be high frequency ringing with frequency

$$f_{react} = \frac{1}{2\pi\sqrt{2L_pC_{oss,eq}}} \tag{B.14}$$

This resonance is only weakly damped due to the low $R_{ds,on}$ of the MOSFETs and low equivalent series resistance (ESR) of the capacitor bank. The parasitic inductance can induce voltage spikes across the switches which can be destructive if not managed in the design. The two general approaches to the control of the CSRI is to either minimize the parasitic inductance and thus neglecting it in the control of the semiconductors, or to introduce an overlap between the gating signals amounting to the time it takes for the current in the parasitic inductance to change direction [26]. For an otherwise ideal circuit considering the parasitic inductance, the optimal overlap where this occurs is [27]

$$\beta = \cos^{-1}\left(1 - \frac{i_{in}\omega L_p}{V_p}\right) \tag{B.15}$$

where V_p is the peak value of the voltage across the resonant capacitor. A high Q-factor reduces the required amount of overlap for a given i_{res}, reducing the effect of the parasitic inductance in decreasing the power factor of the

circuit, but for high frequency operation, it is generally preferred to minimize the the parasitic inductance [18]. The operation of the high-frequency CSRI is simulated in SPICE and is shown in figure B.4, where the high Q-factor and switching frequency results in a dramatic change in the input tank current waveform when considering realistic parasitic elements for a compact inverter-tank system. The resonant tank current and switch voltages for both cases can be estimated from B.9 and B.12, respectively. It is seen that by changing the switching frequency slightly and adjusting the duty cycle, the effect of the parasitic elements can be managed. Even so, careful attention must be paid to i_{react}, as on top of producing additional conduction losses, figure B.4 shows that the weakly damped parasitic resonance means that loss of zero voltage switching will introduce high amplitude ringing. The introduction of parasitic elements, inherent to any real system, can make the inverter stability very sensitive to correct frequency tuning, and the succesful operation of the inverter thus requires precise timing of the gating signals.

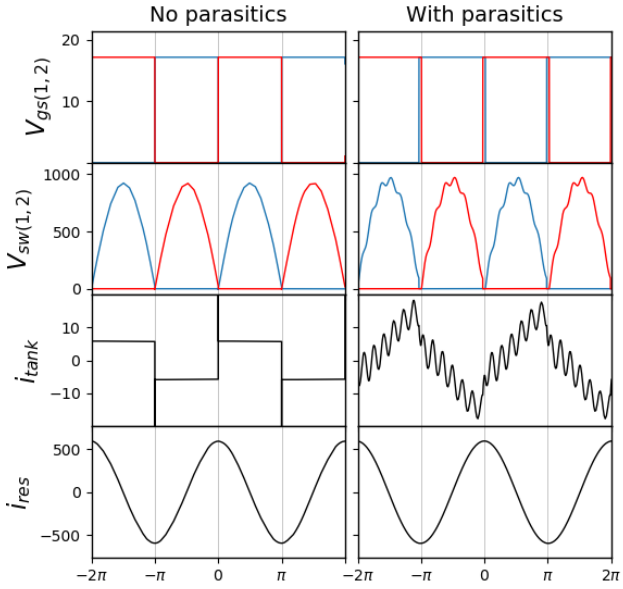

Fig. B.4: Simulations of the CSRI operating with a 2.5 MHz resonant tank with a $Q \approx 80$, $V_{in} = 300$, and ideal switches. (a) no switching device parasitics, with no overlap in the gate signals. (b) with constant $C_{gs} = 0.6$nF and $L_p = 40$nH, including overlap in the gate signals from eq. B.15. A slight decrease in resonance frequency is observed due to absorption of C_{gs} into C_{tank}, and a parasitic capacitance current i_{react} resonating with L_p. The capacitive current magnitude is fixed, but the amplitude of the parasitic oscillations increases with any deviation from optimal operating conditions.

B.3 Design of inverter power module

In order to test the feasibility of using higher voltage SiC MOSFETs in a CSRI topology for the targeted applications, a power module was designed as shown in figure B.5 based on 1700V CPM2-1700-0080B MOSFETs [28]. To demonstrate a flexible module for a CSRI with the possibility of operating in the MHz regime without a transformer under a wide range of load conditions, the module is designed to have the capability of supplying 30 kW at full load. From the input voltage in eq. B.12 and considering a switch voltage derating to 60% of V_{br}, each leg should have a peak current capability of around 100 A. This requires multiple paralleled devices to achieve with a reasonable margin for transistor losses, and thus four MOSFETs were connected in parallel for each switching leg. The parallelization of the MOSFETs in the designed module is thus aimed towards enabling the operation with highly varied loading conditions and power requirements.

Driving the MOSFETs with fast switching performance in the desired frequency range requires special attention to the gate drive circuitry, and it is common to utilize resonant gate drives to source and sink the large currents associated with charging the MOSFET gate [29], [30]. However, in the examined application with variable switching frequency, the resonant behavior can limit the operation frequency range. Additionally, the power loss reduction in the gate drive circuit by using a resonant structure is dwarfed by the copper losses incurred from the high resonant current in the tank. Thus, a conventional hard switched gate drive topology was chosen for flexibility, utilizing an IXRFD630 high current gate driver for each leg. This gate driver is specifically optimized for fast rise and fall times and low thermal impedance through its low inductive package with DBC substrate. The driver can source and sink large peak currents, which is necessary to drive the combined C_{iss} of 9 nF which is expected from the four SiC MOSFETs in each leg. To minimize the inductance in the gate switching loop, as well as to handle the power loss of the driver IC, the driver was mounted directly on a direct bonded copper (DBC) substrate, as was also done in [4], [31]. The CSRI topology is particularly well-suited for this approach since the switches in the CSRI are complimentary and have the same source potential, and thus require identical control and power supply circuits. To reduce the coupling to the power loop, an auxillary source connection was bonded directly to the V_{ss} of the driver.

The power MOSFETs, gate drivers, bypass capacitors, and auxillary components were mounted on a DBC substrate to allow a compact design taking advantage of the high thermal performance of the AlN ceramic [32]. The DBC is soldered to a copper baseplate to provide heat spreading and mechanical rigidity. A plastic housing with embedded pin headers is attached to the module to interface the gate drivers to the supply and measurement PCB.

Low power loop and reactive current loop inductances are advantageous to

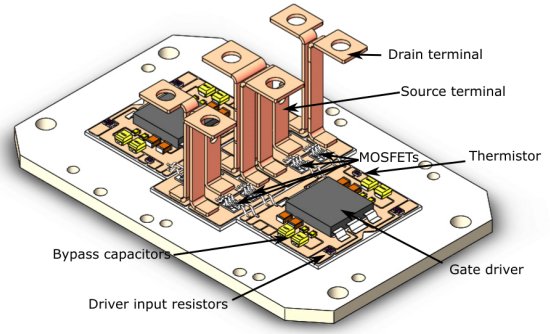

Fig. B.5: Design of the CSRI power module.

minimize the effect of power factor reduction and gate signal compensation. In addition, symmetry in the layout for the power loop for each MOSFET is important for balancing the losses and assuring that each switch has the same optimum driving point. These features were accomplished using interleaved symmetric drain terminals as shown in figure B.6. Symmetry of the gate current paths for each MOSFET is also important to ensure inductance balancing in the gate switching loop, and thus to achieve synchronization of the MOSFET gate voltages. These loops were therefore optimized to be very similar such that the paralleled MOSFETs switch as close to simultaneously as possible. Because four MOSFETs are driven in parallel the effective internal gate resistance is low, and because of the non-negligible gate loop inductance, some degree of underdamping in the driving loop is difficult to avoid without external gate resistance. However, to facilitate fast switching speed for this demonstration module, no external gate resistance was added. This is because the CSRI is inherently not as sensitive to shoot-through issues as voltage source topologies are, and thus some oscillation in gate voltage at turn-off can be accepted in exchange for fast switching capability.

While the presented gate driver integration is key for the handling of gate driver losses and inductance, the integration also implies some inherent capacitive coupling between the driver input and the high voltage copper planes [33]. The IXRFD630 supports an input voltage range from -5 V to $V_{cc} + 0.3$ V, so to avoid accidental false triggering of a turn-off signal, the high input signal to the driver is driven to 10 V through a 50Ω resistor, significantly increasing the voltage margin to the input threshold V_{th} of around 3 V.

The fabricated power module is shown in figure B.7. After the module was tested for gate driver performance, it was finalized by encapsulating it in silicone gel to provide high voltage insulation [34].

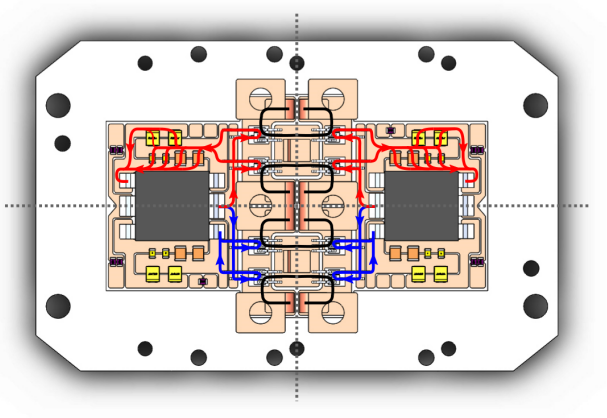

Fig. B.6: Top-down image of the designed power module. Red and blue lines mark the gate current for the MOSFETs when clamped to the positive and negative rails, respectively, while black lines mark the drain-drain current path. The gray dotted lines are symmetry lines.

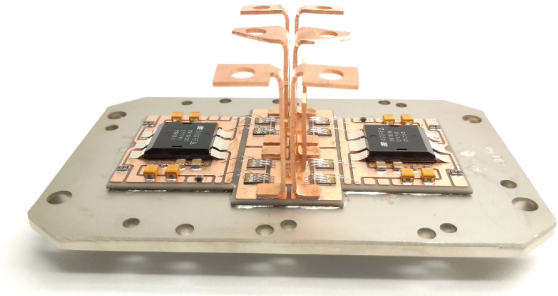

Fig. B.7: Photograph of the fabricated power module before encapsulation.

B.4 Resonant tank system

Some of the most important paramenters in many induction heating processes is the frequency of the coil current and the power delivered to the load. In addition, the physical structure of the coil itself may be highly important to get the desired heating pattern in the workpiece, which fixes the value of the inductance of the tank, as additional series inductance will lower the voltage of the coil terminals and thus the output power for a given workpiece. For the application considered here of high current single turn coils, which may have an inductance on the order of hundreds of nH, this means that a relatively large tank capacitance may be required to achieve the desired frequency and power delivered to the load.

In the case of low impedance workloads, the current in the resonant tank must

be high to dissipate substantial power in the workpiece. Vacuum capacitors are attractive in this application, as they can carry hundreds of amperes and tolerate multiple kilovolts while maintaining very low ESR. However, the capacitance density of vacuum capacitors is limited, requiring special attention to the physical construction of the tank circuit to minimize the parasitic inductance, and if multiple capacitors are connected in parallel, to avoid inductance imbalance by conserving symmetry between the terminals of each capacitor. Thus, to minimize the generation of unwanted oscillations and ensure that the coil current is sinusoidal at the desired frequency, the tank must be constructed such that the circuit functionally matches figure B.2 and equation B.7 remains valid. For this reason, the 8 parallel capacitors in this setup are arranged in a circular pattern, as shown in figure B.8. The power module is connected on one side, while the flat single-turn inductor coil is connected to the other side.

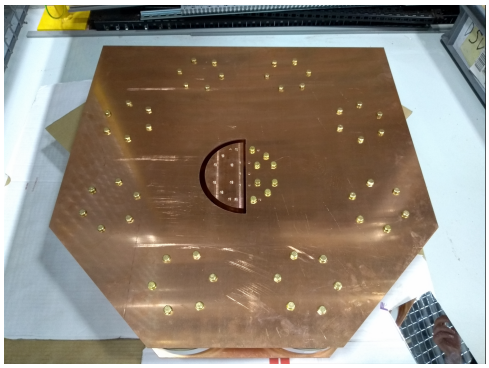

Fig. B.8: Photograph of the resonant capacitor bank with 8 capacitors in parallel for a total capacitance of 40 nF.

The impedance magnitude plot for the constructed high current resonant tank is shown in figure B.9. Except for the unavoidable series resonance of the capacitors with their lead inductance at just above 4 MHz, a sharp and relatively featureless parallel resonance is observed around 2.2 MHz due to the circular symmetry. The coil current is thus expected to be nearly sinusoidal, irrespective of the shape of the input current waveform. From figure B.9, the Q-factor is estimated to be around 75 for the constructed resonant tank.

B.5 Experimental results

As the final elements in the construction of the CSRI, in addition to the power inverter and the resonant tank, the two DC chokes were constructed using 15 winding EMS-0653327-060 powder cores, resulting in an inductance of around 49 μH and an input-output parasitic capacitance of 25 pF. To connect the power

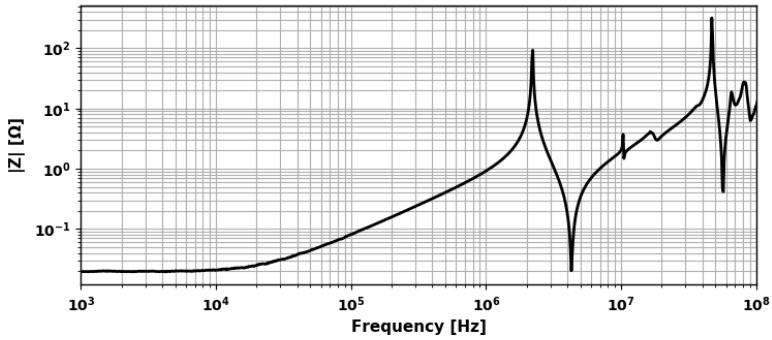

Fig. B.9: Measured impedance at the input to the resonant tank at the centre of the capacitor bank.

module to the resonant tank, a busbar made of a Mylar sheet with silicone adhesive is sandwiched between two copper plates, with a measured inductance of 12 nH and 320 pF parallel capacitance. The gating signals were supplied by a DE0-Nano-SoC FPGA board running a control algorithm providing adjustable duty cycle and output frequency.

The electrical tests were conducted using a Delta Elektronika SM 600-10 DC power supply. The tank voltage is measured using Teledyne Lecroy PPE4kV passive probes, and the gate voltage is measured with Teledyne Lecroy PP019 low voltage probes. The tank input current is measured with a PEM CWT Rogowski current transducer.

The power losses in the active devices are an important metric for inverter performance. However, in this frequency range and considering high frequency ringings in the drain currents, electrical power loss measurements are difficult to assess. The inverter tests were performed on a tests bench with active water cooling for the power module, and thus the dissipated power in the inverter power module was estimated using calorimetric measurements on the water cooling supply for the heat sink.

B.5.1 Gate driver circuit assessment

Driving four power MOSFETs in parallel from a single gate driver sets high demands for the driver IC, and it was investigated on the unencapsulated module whether the two complementary drivers are capable of switching the MOSFETs in the MHz regime. For this purpose, before connection to the resonant tank, the power module was mounted on a heatsink suitable for water cooling, and the temperature of the top of the driver ICs and the heat sink temperature was monitored with a FLIR E40 thermographic camera.

The output voltages of the gate drivers were supplied with +16 V for high output and 0 V for low output relative to the common source potential for

each switch. 16 V high output is chosen to have large margin to the V_{gs} limit of the MOSFET, and although this is not ideal for optimizing the output characteristics, the datasheet for the MOSFET shows only a moderate difference in $R_{ds,on}$ compared to $V_{gs} = 20$ V. Operation at 2.5 MHz and 50% duty cycle is shown in figure B.10. Slightly underdamped behavior of the gate voltage is observed, with rise and fall times around 20ns. It is seen that the output voltage of one driver is only slightly affected of the switching of the complimentary driver, which is important for switching stability.

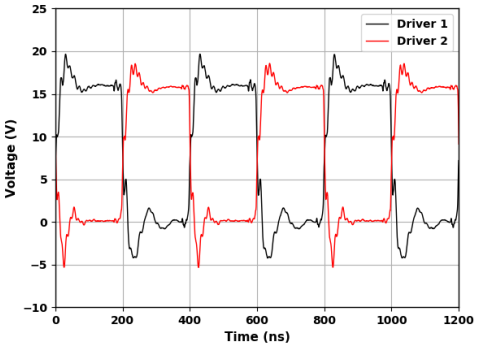

Fig. B.10: Gate driver output voltages measured at 2.5 MHz.

The temperature of the drivers and the heat sink under these operating conditions is shown in fig. B.11, where the DC power consumed by each driver is 14 W. The heat sink is not actively cooled during the test, and thus the slow linear temperature rise is due to heating of the heat sink which is not present during normal operation. The thermal performance is therefore demonstrated by the temperature difference between the driver surface and the heatsink, which reaches a steady value after an initial transient in figure 11. The temperature difference between the drivers are within measurement tolerance, and the steady state temperature difference between the drivers and the heat sink is below 5°C, meaning that the thermal network of the driver is not a bottleneck for higher frequency or driving voltage swings than those used here. This demonstrates the ability of the integrated driver IC to drive the four paralleled 1700V SiC MOSFETs in the MHz regime.

B.5.2 Resonant operation

The unloaded operation tests were conducted under slow variation of the input power to showcase steady state resonant operation, with the CSRI operating at the resonant frequency shown in figure B.12 for $V_{DC} = 40$ V. The clean voltage waveforms indicate that soft-switching is achieved, with the tank input current clearly being primarily reactive. A ripple frequency of around 20 MHz

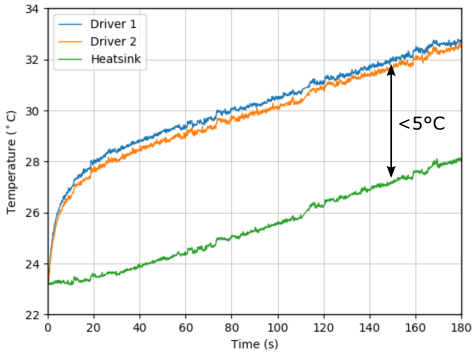

Fig. B.11: Temperature rise for the gate drivers and heat sink for 2.5 MHz operation measured with thermographic camera.

is observed, close to the predicted resonance frequency of 18.5 MHz based on eq. B.14, which is calculated by summing the total L_p from contributions of the busbar, power module, and resonant tank to an estimated 34 nH, and estimating a $C_{oss,eq} \approx 385$ pF for each MOSFET based on the data sheet at this operating point.

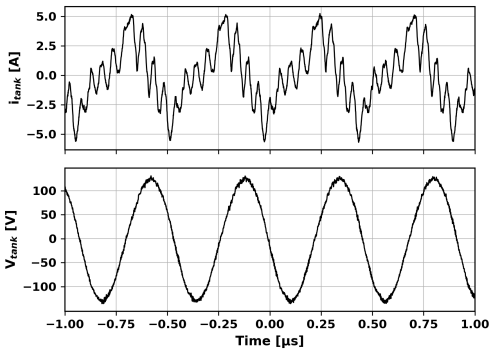

Fig. B.12: Tank voltage and output current of the transistors for a switching frequency of 2.17 MHz and DC voltage $V_{DC} = 40$ V.

When the voltage across the resonant tank is increased to levels nearing the highest operating point of the transistors, the input current to the resonant tank in figure B.13 shows that complete soft switching is not achieved. As was argued in section B.2, achieving soft switching requires very finely tuned driving pulses. In the applied control scheme, there is a finite time resolution of the driving signals of 3.3ns, and thus when the voltage is increased and the output capacitance of the MOSFETs decrease, the gradual change in resonance

frequency can make it difficult to switch precisely at the voltage zero crossings. The loss of soft switching results in large amplitude high frequency ringing that can interfere with the control circuitry and thus limits the operating voltage of the inverter, although the power dissipation in the module is well within the accepted range. Additionally, while the influence of the parasitic elements in general has a negative impact on the quality of the inverter output current, the loss of soft switching reduces this quality further, which can be an important consideration in applications requiring very clean resonant current waveforms. Re-introduction of the series diodes in the CSRI topology could relax the timing requirements in applications where robustness of the control is desired, at the expense of increased losses and component count [24], [27]. Alternatively, using a microcontroller with a high-resolution PWM architecture to create the driving signals, as done in e.g. [35] and [36], would likely also enable operation closer to the breakdown voltage of the switches. The tradeoff in this approach is that if the system is extended to closed loop control, the FPGA is not available for the implementation of a control algorithm with fast real time response.

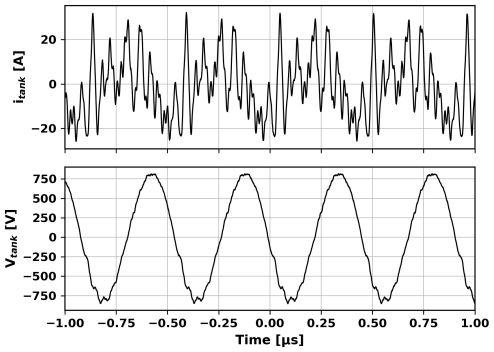

Fig. B.13: Tank voltage and output current of the transistors for a switching frequency of 2.19 MHz and DC voltage $V_{DC} = 280$ V.

For the power module efficiency calculation, it is assumed that the input chokes and cables contribute negligibly to the total losses due to the low input current. This allows the inverter efficiency is estimated as

$$\eta = \frac{P_{in} - P_{module}}{P_{in}} \cdot 100 \tag{B.16}$$

The efficiency is shown for various output power levels in figure B.14. The lower efficiency at low power levels is due to the power consumption of the gate drive circuits, while the drop at high power levels is explained by the gradual loss of soft switching. Still, even with the increase in the switching

losses at higher voltage, efficiency above 90% is achieved. This efficiency is low compared to modern lower frequency induction heating systems [19], [21], [22], but is comparable to other SiC-based MHz inverter systems in the literature [6], [7]. As a large amount of the switch current in the presented measurements is reactive current that is present for any load condition, the efficiency of the inverter is expected to increase with increased loading. At this operating point, using the conservative estimate of the resonant current $i_{res} = C_{tank}\frac{\mathrm{d}V_{Ctank}}{dt}$, a reactive power of 170 kVA is oscillating in the tank circuit. These results showcase that proper design of the inverter system can allow a paralleled SiC MOSFET power module to efficiently drive a high power low impedance coil for MHz induction heating.

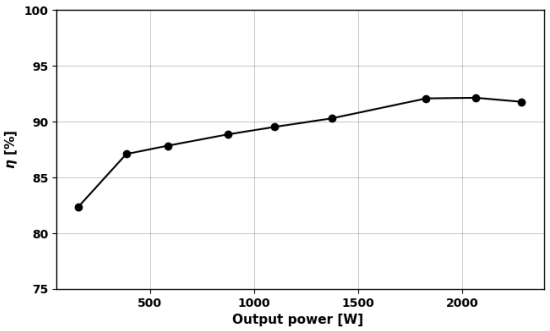

Fig. B.14: Calorimetric measurement of the efficiency of the CSRI power module at varying output power.

B.6 Conclusion

In this paper, a prototype current source resonant inverter for variable frequency MHz induction heating was presented, and key considerations for the use of power devices with increasing blocking voltage in high frequency operation were discussed. A power module with paralleled 1700V MOSFETs and integrated gate drivers was fabricated, with the gate drivers able to switch the four paralleled MOSFETs at 2.5 MHz with a low temperature increase of 5°C. This demonstrates the viability of handling both the thermal driver issues at high frequency and the low gate loop inductance requirements of paralleled SiC MOSFETs by using a hard-switching integrated gate driver structure. The power module was tested with an industrially relevant high-Q resonant tank, where switching at the resonant frequency provides clean voltage waveforms even under unloaded conditions, validating the applied approaches to paralleled SiC MOSFET power module design for the high frequency, high-Q inverter system. At higher voltage the inverter performance was limited due to the loss of soft

switching, which was ascribed to the finite time resolution of the used driving circuit. Still, higher than 90% efficiency was achieved using the test setup at an output power of 2.3 kW in unloaded conditions, with calculated reactive power of 170 kVA. These results demonstrate the succesful application of a CSRI using paralleled 1700V MOSFETs in MHz operation, and are promising for the further expansion of the power range of MHz induction heating inverters.

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Paper C

Class-E Push-Pull Resonance Converter with Load Variation Robustness for Industrial Induction Heating

Janus Dybdahl Meinert, Benjamin Futtrup Kjærsgaard, Thore Stig Aunsborg, Asger Bjørn Jørgensen, Stig Munk-Nielsen, Sune Bro Duun

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Abstract

Emerging wide bandgap devices are extending the operating frequency range and power handling capability of solid state based resonant power converter solutions. Presently, resonant power converters for industrial induction heating are using vacuum-tubes, achieving efficiencies of 50-60 %. By replacing the prevalent vacuum tube technology with a solid state based solution, the efficiency of the industrial induction heating processes is expected to be increased. A design of a Class-E Push-Pull resonance converter using silicon carbide MOSFETs is proposed. A prototype, operating at 2.5 MHz, has been built showing a proof-of-concept of the topology at 4 kVA, achieving an efficiency of 91.8 % with a representative industrial induction heating load.

C.1 Introduction

Resonant converters operating in a high frequency high power range are used in a wide range of industrial applications including dielectric and inductive heating. Dielectric heating includes various drying processes, whereas inductive heating is used for e.g. sawblade hardening and float zone processes [1]–[4]. The float zone processing industry currently uses vacuum-tube technology for the resonance converters with efficiencies ranging from 50-65 % [5], [6]. However, with the higher breakdown voltage, lower on-resistance, higher thermal conductivity and lower gate charge of the silicon carbide (SiC) MOSFETs compared to their silicon counterparts [7], [8], high power radio frequency (RF) applications based on solid state technology is enabled [9]–[13]. Thus, by using wide bandgap (WBG) devices as a replacement for the vacuum-tubes, the efficiency of the float zone process is expected to be increased significantly.

In this paper, a proposed prototype resonance converter using SiC MOSFETs will be built and demonstrated for 2.5 MHz induction heating applications. The next section will present the intended converter design, its functionalities and design considerations. An experimental demonstration is given and a comparison between experiments and digital twin simulations is presented in the following

two sections. Lastly the most relevant findings of this paper are summarized.

C.2 Proposed Topology

The chosen converter topology for the proposed design is a Class-E Push-Pull resonance current source converter, illustrated in C.1a. Recent research utilizing the Class-E Push-Pull converter for inductive power transfer applications has shown high frequency oscillations and voltage spikes during switching instances, which is found to be caused by the stray inductance as presented in [13], [14]. The proposed design intends to utilize the stray inductance by having two distinct resonance loops; (*1*) The drain-source resonance loop, consisting of the stray inductance L_{stray} and the respective drain-source capacitance C_{ds} visualized by the red and green colored areas in C.1a. (*2*) The load resonance tank, illustrated by the blue colored area, consisting of the resonance capacitor C_r and the single turn resonance induction coil L_r which through inductive power transfer will dissipate power in the form of iron losses heating the load object represented by R_{iron}. A sketch of the used single turn coil is shown in C.1b. The concept of the design is to ensure zero-voltage switching (ZVS)

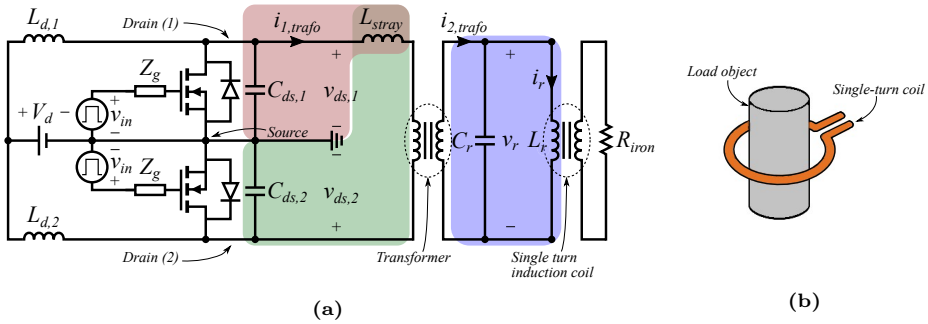

Fig. C.1: (a) Circuit schematic of proposed topology with colored areas illustrating different resonance loops. (b) Sketch of a single turn induction coil.

over a wide range of load resonance frequencies f_r by controlling the drain-source resonance frequency f_{ds}. This is obtained with the following two design considerations; (*1*) Utilizing the leakage inductance of the transformer $L_{lk,trafo}$ the trace/wire inductance from the converter to the resonance load $L_{trace,\sigma}$ is dominated. (*2*) Inserting sufficiently large drain-source capacitors $C_{ds,ext}$ in parallel with the MOSFETs, reduces the influence of the voltage dependent intrinsic output capacitance $C_{ds,\sigma}$ of the MOSFETs.
The two design considerations are summarized in (C.1) and (C.2).

$$L_{stray} = L_{lk,trafo} + L_{trace,\sigma} \simeq L_{lk,trafo}, \qquad L_{lk,trafo} \gg L_{trace,\sigma} \tag{C.1}$$

$$C_{ds} = C_{ds,ext} + C_{ds,\sigma} \simeq C_{ds,ext}, \qquad C_{ds,ext} \gg C_{ds,\sigma} \tag{C.2}$$

By the designers choice the drain-source resonance frequency f_{ds} can be varied by controlling the size of the transformer leakage inductance and the inserted drain-source capacitance.

$$f_{ds} = \frac{1}{2\pi \cdot \sqrt{L_{stray} \cdot C_{ds}}} \simeq \frac{1}{2\pi \cdot \sqrt{L_{lk,trafo} \cdot C_{ds,ext}}} \tag{C.3}$$

By choosing the drain-source resonance frequency f_{ds} higher than the switching frequency f_{sw}, ZVS of the MOSFETs are ensured for a wide range of load variations if the constraint in (C.4) is satisfied.

$$f_{sw} = f_r < f_{ds} \tag{C.4}$$

The mode of operation of the proposed topology is similar to a single-ended Class-E where the turn-OFF of a MOSFET triggers the drain-source resonance circuit and a half sine-wave voltage is generated across the drain-source terminals of the MOSFET [15]. Since the drain-source resonance frequency is higher than the switching frequency, the drain-source capacitor will discharge to 0 V before the MOSFET turns ON, leading to a time period where the body diode is conducting. In C.2a the expected waveforms for the topology are seen, where the drain-drain voltage is defined as $v_{dd} = v_{ds,1} - v_{ds,2}$. As seen from C.2a

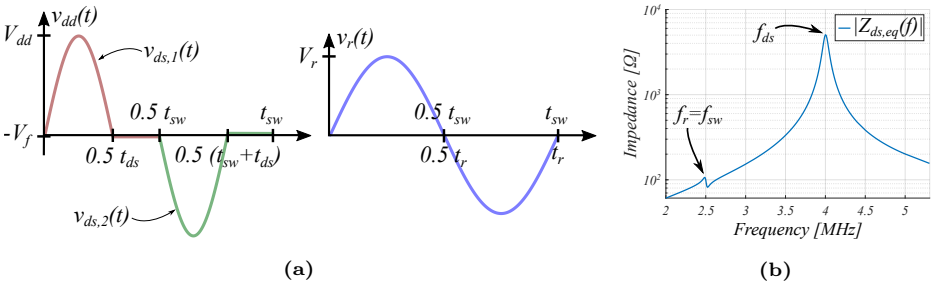

Fig. C.2: (a) Class-E Push-Pull expected voltage waveforms and (b) The absolute value of the equivalent drain-source impedance illustrating the two resonance frequencies of the converter, f_r and f_{ds}.

two time periods are defined; t_{ds} and t_{sw} which represent the drain-source resonance period and switching period respectively, with the switching period being equal to the load resonance period. The two different resonance frequencies of the converter are illustrated as an impedance curve in C.2b. The analytical expressions for the voltage waveforms in C.2a are shown in (C.5) and (C.6).

$$v_{dd}(t) = \begin{cases} V_{ds} \cdot \sin(2\pi f_{ds} \cdot t), & 0 < t \leq 0.5\ t_{ds} \\ -V_f, & 0.5\ t_{ds} < t \leq 0.5\ t_{sw} \\ -V_{ds} \cdot \sin(2\pi f_{ds} \cdot t), & 0.5\ t_{sw} < t \leq 0.5\ (t_{sw} + t_{ds}) \\ V_f, & 0.5\ (t_{sw} + t_{ds}) < t \leq t_{sw} \end{cases} \tag{C.5}$$

$$v_r(t) = V_r \cdot \sin(2\pi f_r \cdot t + \theta) \tag{C.6}$$

Using the analytical expressions in (C.5) and (C.6), the proposed topology shown in C.1a can be reduced to the equivalent circuit diagram in C.3, where $L_{eq,dd}$ is the total equivalent inductance between the drain-terminals and resonance load. As depicted in C.3, the current injected to the load resonance circuit

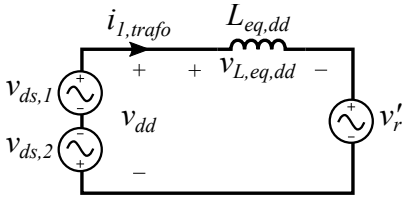

Fig. C.3: Equivalent Class-E Push-Pull circuit diagram.

is dependent on the voltage drop across the equivalent inductance. This can be utilized for controlling the output power of the converter by controlling the phase of this current, similar to a current controlled voltage source converter.

C.3 Experimental Verification

The functionality of the proposed topology is confirmed through experimental verification. A prototype converter is built as shown in C.4. As observed an AC-

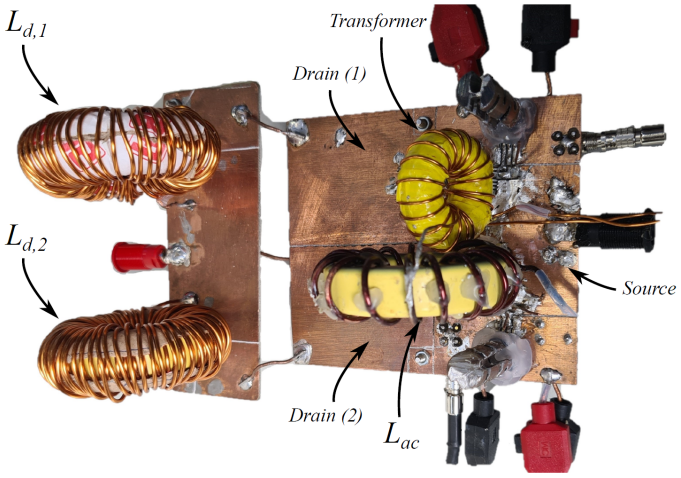

Fig. C.4: Built Class-E Push-Pull prototype converter with a transformer between the converter and load.

inductance L_{ac} is introduced in series with the transformer leakage inductance,

thus the stray inductance will be given as $L_{stray} = L_{ac} + L_{lk,trafo} + L_{trace}$. The AC-inductance is needed to obtain the desired drain-source resonance frequency, without exceeding the 12 A current limit of the chosen Wolfspeed C3M0160120J SiC MOSFETs [16]. The commutation loops of the two MOSFETs are designed with a focus on symmetry to achieve similar impact from parasitic inductance and capacitance on the drain-source voltage waveforms $v_{ds,1}$ and $v_{ds,2}$. All magnetic components are designed using core materials with approximately constant permeability in the 2.5 MHz range. The DC-inductors are designed to achieve near constant DC-supply current. Due to the inductors being self-wound a slight deviation in DC inductance is observed. Using the IXDN614YI [17] gate driver, a low inductive hard switched gate driver design has been achieved through symmetrical layout, allowing for fast switching performance without gate-source voltage oscillations while having no external gate resistance. Circuit parameters are given in C.1.

Table C.1: The circuit parameters used in the built Class-E Push-Pull resonance converter.

Converter side

Components	V_d	$L_{d,1}$	$ESR_{Ld,1}$	$L_{d,2}$	$ESR_{Ld,2}$	L_{ac}	$C_{ds,ext}$
Value	30 V	145 µH	1 Ω	144 µH	1.4 Ω	1.6 µH	440 pF

Load side

Components	$L_{lk,trafo}$	$L_{m,trafo}$	$R_{c,trafo}$	n_{trafo}	L_r	C_r	Q_r
Value	442 nH	4.2 µH	30 kΩ	0.353	93 nH	46 nF	61

The performance of the converter is tested by connecting the secondary side of the transformer to the external resonance tank with a representative single turn induction coil for induction heating purposes designed in [13]. The driver signals for the two MOSFETs are supplied complimentary with a 50% duty cycle. The switching frequency is adjusted until the resonance frequency of the load is met at 2.45 MHz. The resulting experimental results are shown in C.5. As observed ZVS is achieved with a drain-source resonance frequency of 3.9 MHz ($T_{ds} = 256$ ns). This leaves a tolerable margin of load resonance frequency variations greater than 1 MHz for which ZVS can be ensured. The drain-source voltage amplitude of 163 V yields a significantly higher voltage gain than the usual Class-E voltage gain of approx. 3.6, which is due to the volt-second balance of the DC-inductor yielding a voltage gain dependent on the ratio of the switching and drain-source resonance frequencies as shown in (C.7) [15], [18].

$$V_{ds} = (V_d - V_{ESR,Ld}) \cdot 3.562 \cdot \frac{T_{sw}}{T_{ds}} = \big(30\,\text{V} - (1.08\,\text{A} \cdot 1\,\Omega)\big) \cdot 3.562 \cdot \frac{408\,\text{ns}}{256\,\text{ns}} = 164\,\text{V} \tag{C.7}$$

Where the term $V_{ESR,Ld}$ takes into account the DC-voltage drop across the ESR of the DC-inductor, with an observed DC-current of 1.08 A read from the

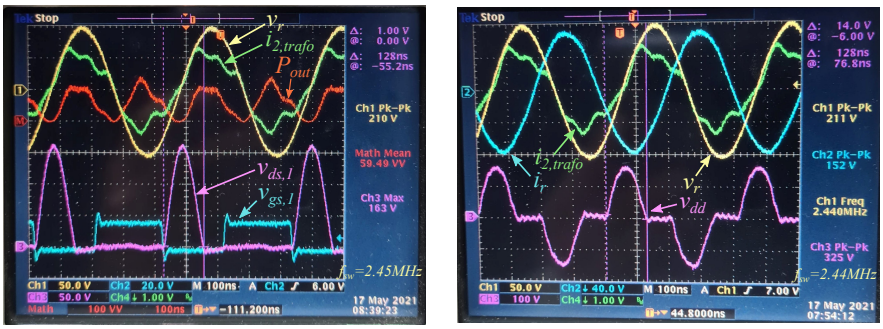

Fig. C.5: Experimental results demonstrating the performance of the built prototype converter, with the drain-source resonance frequency being higher than the switching frequency, thus achieving ZVS. The MOSFETs are operated at the resonance frequency of the load, seen from v_r and $i_{2,trafo}$ being in phase. The drain-drain voltage v_{dd} is following the expected trend derived in (C.5).

DC-supply.

The current i_r in the single turn induction coil and the voltage v_r of the resonance capacitor are observed to be approx. 90° phase-shifted due to the reactive nature of the resonance tank. An apparent power of 4 kVA is observed in the resonance tank, which with a supply input power of only 64.8 W implies a reactive power of approx. 4 kVAr.

From C.5 it is observed that the secondary side transformer current $i_{2,trafo}$ is in phase with the resonance voltage v_r, due to switching at the load resonance frequency. By multiplying these two signals the instantaneous output power is obtained, for which the mean active power transferred to the load object through the single turn induction coil is calculated to 59.49 W with an input DC-voltage of 30 V. Thus, the efficiency of the built prototype converter is 91.8 %.

C.4 Analysis of Design Robustness

A SPICE model of the proposed design is developed to analyze whether the design has obtained the desired robustness and drain-source resonance frequency predictability in regards to the influence of parasitic inductance and capacitance on the drain-source resonance circuit. Three different SPICE model levels are created with increasing complexity; (*Model 1*) an ideal circuit model, (*Model 2*) a model including the parasitic inductance between the circuit elements and (*Model 3*) a model including the parasitic inductance and capacitance between the circuit elements. A 3D model of the circuit board is shown in C.6 and imported into ANSYS Q3D Extractor to extract the mentioned parasitics. This method has in previous studies proven valuable in determining the parasitic influence on the performance for a given circuit design [19].

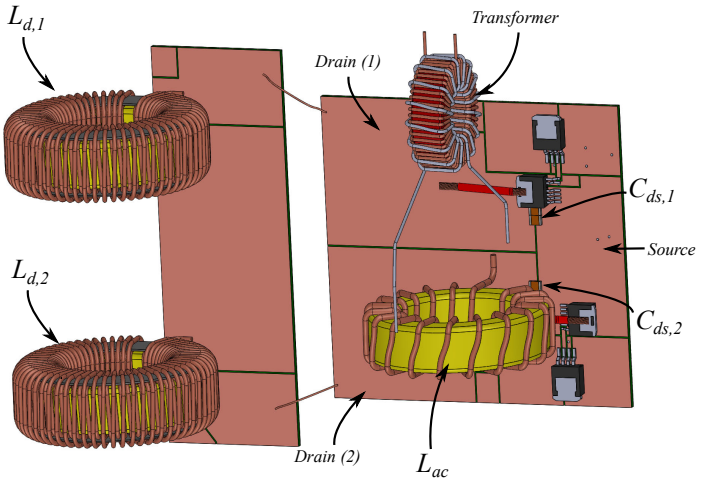

Fig. C.6: 3D model of the built Class-E Push-Pull prototype converter.

The three SPICE models are simulated at an input voltage of 30 V and compared to experimental measurements as shown in C.7.

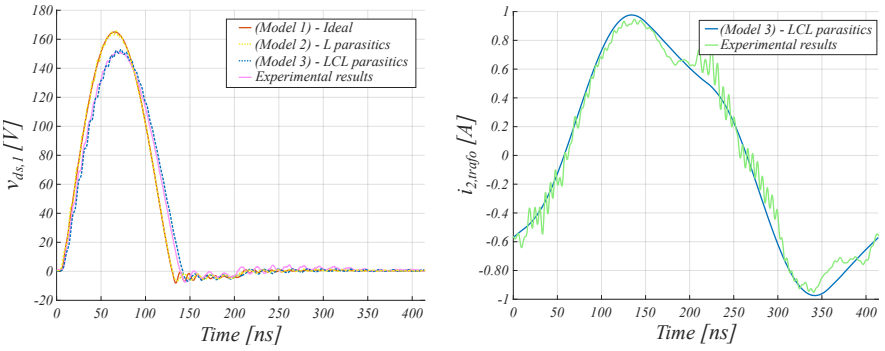

Fig. C.7: Experimental and simulated waveforms with an input voltage of 30 V and a switching frequency of 2.415 MHz. (a) shows the drain-source voltage and (b) shows the secondary side transformer current.

It is observed that the drain-source voltage is similar for both SPICE model 1 and 2. This implies that the drain-source resonance loop in the present design is not influenced by the parasitic inductance between the circuit elements, implying that the first design consideration seen in (C.1) is satisfied. This outcome is expected as the extracted parasitic inductances between the circuit elements are between 10-30 nH which is 2 orders of magnitude smaller than the inserted stray inductance.
However, the two drain-source voltages from SPICE model 1 and 2 do not

match the experimental drain-source voltage. A good similarity is obtained between SPICE model 3 and the experimental measurements, implying that the drain-source capacitance of the present design is influenced by the physical circuit board parasitic capacitance. The parasitic drain-source capacitance is mainly contributed from the capacitance to the bottom side of the PCB, as this is connected to the source plane. The size of the extracted equivalent parasitic drain-source capacitance is read to approximately 80 pF, which is in the same order of magnitude as the external drain-source capacitance of 440 pF. Thus, the constraint in (C.2) is not satisfied leading to a decrease in design robustness in regards to drain-source capacitance, which is also observed from the deviation between the drain-source voltage waveforms in C.7.

Investigating the secondary side transformer current shown in C.7 it is seen that a great resemblance between SPICE model 3 and the experimental measurements is obtained. This indicates that the impedance of both the transformer and the single turn induction coil is modelled adequately which together with the matching drain-source voltage waveforms enables the use of SPICE model 3 for performance predictability of future designs.

Concerning the design considerations in (C.1) and (C.2), the present design has only achieved complete robustness in regards to the parasitic inductance. Ideally the inserted inductance and capacitance should both have been order of magnitudes higher than the parasitic impedances for a fully robust design. Due to the size difference between the stray inductance and the parasitic inductance, it is a possibility for future designs to reduce the inserted stray inductance while increasing the external drain-source capacitance in order to achieve the desired drain-source capacitance robustness. Simultaneously the design constraint from (C.4) has to be considered in order to maintain a drain-source resonance frequency higher than the switching frequency to ensure ZVS. For the present design the current limitation of the MOSFET's has been a constraint which lead to a minimum allowable stray inductance. Due to this minimum allowable inductance it has not been possible to insert a sufficiently large drain-source capacitor while still satisfying the design constraint in (C.4) to ensure ZVS. Ultimately, for future designs a trade-off between robustness in terms of capacitance and inductance has to be made, while ensuring ZVS by satisfying the design constrain in (C.4). Additionally the current limitation of the MOSFET's has to be addressed, which will also aid in the scalability of the proposed design.

C.5 Conclusion

In this paper a proof-of-concept of a 4 kVA, 2.5 MHz prototype Class-E Push-Pull resonance converter for industrial induction heating has been demonstrated with an efficiency of 91.8 %. It is shown how the addition of a transformer and

an external drain-source capacitor can provide load variation robustness and ZVS capability over a wide range of load resonance frequencies. A digital twin simulation based on parasitic extractions is showing a good agreement between experiment and simulation, which for future designs allows for predictability of the converter performance in new design domains.

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Paper D

Demonstration of a Class E Push-Pull Resonant Inverter for MHz Induction Heating

Thore Stig Aunsborg, Benoît Bidoggia, Sune Bro Duun, Benjamin Futtrup Kjærsgaard, Janus Dybdahl Meinert, Asger Bjørn Jørgensen, and Stig Munk-Nielsen

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Abstract

Industrial heating processes operating at frequencies of multiple MHz often have low efficiencies due to the use of vacuum-tube technology. This can be improved using inverters based on wide band gap materials, but requires special attention in topology selection to achieve high efficiency in a range of operating conditions. This paper investigates the merits of the Class E push-pull resonant inverter topology for MHz induction heating. A prototype SiC MOSFET power module is manufactured and experimentally validated in a Class E push-pull inverter system with a commercial induction heating load. The inverter is demonstrated up to a power of 5 kW with high efficiency, verifying the performance of the approach for industrial RF heating systems.

D.1 Introduction

Common industrial heating processes at RF frequencies, such as dielectric heating for curing and drying, or induction heating processes for zone refining of silicon, are limited in their efficiency due to the use of vacuum tube oscillators that are typically only 60-70% efficient [1]–[3]. This can be drastically improved by replacing the tubes with solid state devices, in particular by taking advantage of wide band gap (WBG) technology [4], [5]. In a variety of applications, DC-AC inverters (or equivalently, switched-mode amplifiers) operating with high efficiency at MHz frequencies and several kW have been demonstrated [6]–[9]. These advancements hold promise for further utilization of WBG devices for RF inverters in heating applications by pushing towards higher operating frequency, power delivery, and efficiency of the inverters. In this paper, an approach to this is demonstrated using a resonant inverter system for MHz induction heating based on the Class E push-pull topology. First, the operational principles and merits of the topology are described, after which an experimental setup for validating the performance and efficiency of the system is presented. Lastly, the results of operation with a MHz induction heating load are presented and discussed.

D.2 Topology description

Several topologies of resonant inverters have been applied to induction heating processes, including both current- and voltage source bridge inverters, single switch inverters, and inverters with multiple load elements such as LLC [10], [11]. For low impedance induction heating loads as well as high frequency operation, the Class E push-pull topology investigated here is attractive for several reasons. These include constant current drawn from the DC source, and the use of a parallel resonant tank which allows for current gain as well as inherent work coil short circuit capability [9], [12], [13]. In addition, the switch gates are driven with reference to the same potential and, as shown in red and green in Fig. D.1(a), the circuit can be made in a way that incorporates the switch output capacitance and the circuit stray inductance in a secondary resonance loop that shapes the voltage across the switches to achieve zero voltage switching (ZVS) under a wide range of load frequency variation.

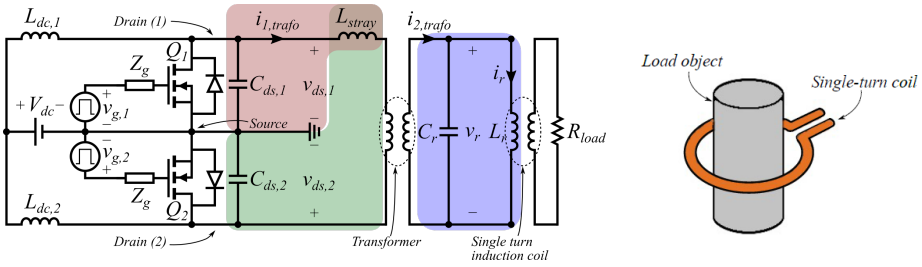

Fig. D.1: a) schematic of the Class E push-pull inverter illustrating the resonant current paths and b) single-turn coil used for high-current induction heating [14].

This is seen in the circuit waveforms for the inverter operated at the tank resonance frequency in Fig. D.2; the diode conduction provides inherent zero voltage switching at turn-on within the time interval T_B allowing for clean switching waveforms at MHz frequencies and reduced sensitivity to inaccuracies in the control timing. The leakage inductance of the transformer, which is the main parasitic inductive element, functions as a simple inductance between two phase-shifted voltage sources (the inverter stage and the resonant tank).

To maximize power transfer to the parallel resonance tank, the switching frequency should be kept relatively close to the tank resonance frequency. The requirement for soft switching of the MOSFETs is that the drain-source resonance voltage is in the negative half cycle at turn on. Thus, by letting the switching frequency follow the resonance frequency during operation, soft

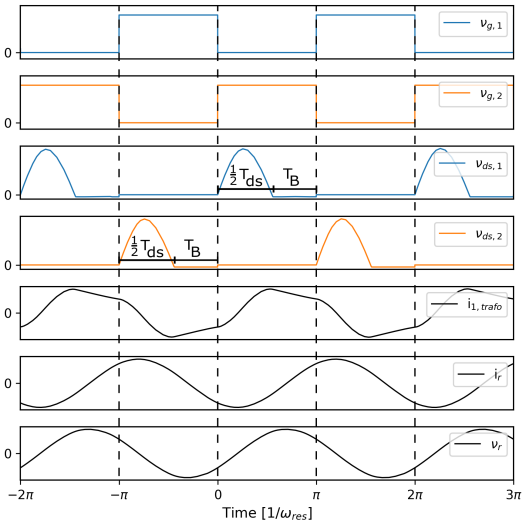

Fig. D.2: Simulated voltage and current waveforms of the Class E push-pull inverter. One tank resonance period is $T_{\mathrm{res}} = T_{\mathrm{ds}} + 2T_{\mathrm{B}}$.

switching is achieved in the frequency range

$$f_{\mathrm{res}} = f_{\mathrm{sw}} < f_{\mathrm{ds}} < 2f_{\mathrm{res}} \tag{D.1}$$

However, the main drawback of the topology, as with the classic single ended Class E amplifier, is the relatively poor switch utilization factor c_{pmr} due to high voltage voltage across the switch given by [15]

$$c_{\mathrm{pmr}} = \frac{\eta_{\mathrm{D}} V_{\mathrm{dc}} I_{\mathrm{dc}}}{N V_{\mathrm{ds,p}} I_{\mathrm{ds,rms}}} \tag{D.2}$$

where η_{D} is the drain efficiency of the amplifier, V_{dc} and I_{dc} are the input voltage and current, respectively, N is the number of utilized switches, $V_{\mathrm{ds,p}}$ is the peak switch voltage, and $I_{\mathrm{ds,rms}}$ is the switch RMS current. To achieve both zero voltage and zero voltage derivative switching (ZVDS), the Class E amplifier has $V_{\mathrm{ds,p}}/V_{\mathrm{dc}} = 3.56$ for the ideal case, and generally larger still when considering the non-linear switch parasitic capacitance [16], [17]. Several alternatives or modifications to the Class E topology, such as the Class F or Class Φ_2, achieve higher c_{pmr} by shaping the harmonic content of the voltage across the switches using additional resonant networks, at the expense of increased complexity [15], [18], [19]. The presented embodiment of the Class E amplifier does not aim to achieve ZVDS, but instead relies on the drain-source resonance loop to achieve ZVS over a wide resonance frequency range given by (D.1). This narrows the

drain-source voltage, which from the volt-second balance of the DC chokes further increases the ratio $V_{\mathrm{ds,p}}/V_{\mathrm{dc}}$, thus lowering c_{pmr} [14]. The topology investigated here is thus mainly attractive in applications where robustness towards frequency variation of the load is valued over switch utilization.

Considering the practical implementation of the inverter, this topology can achieve high efficiency in particular thanks to the incorporation of both capacitive and inductive parasitics. The high frequency of the application considered here means that the transformer leakage inductance is easily used as the primary inductive element in the drain-source loop, which must then be matched with the switch parasitic capacitance, constraining the values of practical elements in this resonance loop.

D.3 Design and components

A prototype inverter system using a Class E push-pull topology for MHz induction heating was manufactured and tested. In addition to providing the normal functions of galvanic isolation and impedance matching (while maintaining high coupling factor), the transformer in this topology must also provide an adequate leakage inductance seen from the primary side to yield the desired drain-source resonance frequency. Because of the high frequency and the relatively low desired inductance values, an air-core transformer was designed and built as shown in Fig. D.3. A spiral layout of flat ribbon windings is used to provide a coupling factor $k > 0.7$ and the desired electrical parameters while maintaining high voltage isolation and good thermal performance.

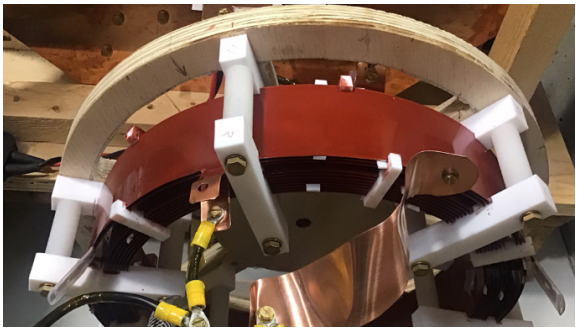

Fig. D.3: Picure of the constructed transformer with tabs for adjustment of the primary, secondary, and leakage inductances.

A custom integrated power module was designed and built for the inverter as shown in Fig. D.4. Each switch is made from two 1700 V SiC MOSFETs in a symmetric layout with auxiliary source connections. High voltage capacitors C_{cap} are added in parallel to the MOSFETs to achieve the desired f_{ds} and reduce its voltage dependency, particularly at higher voltages. For simplicity

of the driving circuit and high operating frequency flexibility, a hard switched gate drive topology is chosen. However, driving the input capacitance of the paralleled MOSFETs at multiple MHz requires the driver IC to source and sink large peak currents. Thus, the driver ICs are integrated in the power module to improve the thermal performance and achieve high switching speed with a small gate switching loop. An advantage of the inverter topology is that neither the input nor the output of the module is sensitive to stray inductance, leading to a large degree of flexibility in the module design.

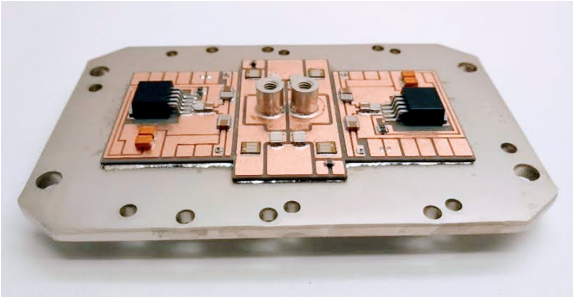

Fig. D.4: Picture of the power module for the inverter before wire bonding, terminal welding, and encapsulation.

The power module, DC chokes, and high-frequency transformer are connected by cables on the primary side, while the secondary side is connected to the parallel resonant tank using a busbar structure, as shown in Fig. D.5. The resonant tank is comprised of a flat single turn inductor coil with a steel block load connected to a 40 nF vacuum capacitor bank [9], yielding the resonance frequency $f_{\text{res}} \approx 2.4$ MHz. The components of the inverter system are summarized in Table I.

Table D.1: Prototype component values.

Component	Value	Implementation
S1, S2	$R_{\text{ds,on}} = 80$ mΩ $C_{\text{oss}} = 105$ pF @ 1000 V	4x CPM2-1700-0080B
Gate drivers	$\nu_{\text{g}} = -4$ V/ + 18 V	2x IXDN614YI
Module capacitors	$C_{\text{cap}} = 470$ pF	4x C1812X471JGGACTU
Transformer	$n = 2:7$, $L_{\text{p}}^{\sigma} = 1.0$ uH $L_{\mu} = 1.1$ uH	Spiral windings, air-core
DC chokes	$L_{\text{dc}} = 49$ uH	2x EMS-0653327-060 powder cores, 15 windings

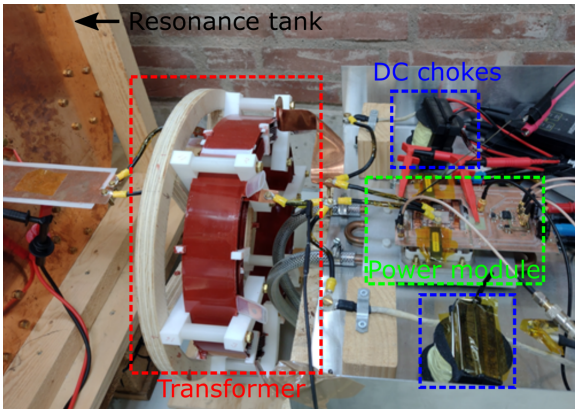

Fig. D.5: Picture of the experimental setup, with wires and busbars connecting the discrete elements of the inverters.

As the parasitic MOSFET output capacitance is highly voltage dependent, it is important to evaluate it at the operating voltage to ensure that drain-source resonance frequency is within the desired range. The capacitance at a given voltage level is found as the charge-equivalent output capacitance [20]

$$C_{\mathrm{oss,eq}} = \frac{\int_0^{V_{\mathrm{ds}}} C_{\mathrm{oss}}(\nu)\mathrm{d}\nu}{V_{\mathrm{ds}}} \tag{D.3}$$

Combined with the fixed capacitance from the module capacitors, and by ignoring other parasitic capacitances from module and transformer and small stray inductances, the drain-source resonance frequency is found from

$$f_{\mathrm{ds}} \approx \frac{1}{2\pi\sqrt{2(C_{\mathrm{oss,eq}} + C_{\mathrm{cap}})L_{\mathrm{p}}^{\sigma}}} \tag{D.4}$$

The impedance seen from the module terminals is seen in Fig. D.6, where the tank resonance is observed at 2.4 MHz. This is compared to a simple SPICE model of the inverter, including switch parasitics and parameters from table D.1. From the datasheet of the MOSFETs $C_{\mathrm{oss}}(0\mathrm{V}) \approx 2.25$ nF, yielding a total switch capacitance of $2(C_{\mathrm{oss}}(0\mathrm{V}) + C_{\mathrm{cap}}) = 5.44$ nF. Since the switch capacitances are in series in this measurement configuration, the apparent drain-drain capacitance is 2.72 nF, which fits well with the measured impedance result. The green dotted line shows the estimated impedance from drain to source for each switch assuming a peak voltage of 800 V according to (D.3) and (D.4). From this, the drain-source capacitance becomes $C_{\mathrm{ds}} \approx 1.23$ nF resulting in $f_{\mathrm{ds}} = 4.56$ MHz, which is within the ZVS operating range determined by (D.1).

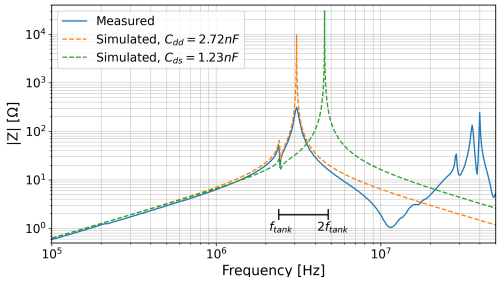

Fig. D.6: Load impedances measured and simulated from the power module output terminals. The usable f_{ds} operation range for this load configuration is highlighted.

D.4 Experimental results

The measurements setup consists of two HDO6034 oscilloscopes, where the high voltage signal of the resonant tank and the MOSFET drains are measured using HVD3605A and HVD3206 differential probes, respectively. The transformer input and resonant tank currents are measured with PEM CWT Rogowski current transducers. The resonant inductor, load, and power module are water cooled with individual cooling loops, allowing the dissipated power and efficiency of each element to be estimated from calorimetric measurements. The gate- and drain voltage waveforms of the induction heating setup when operated close to the tank resonance frequency are shown in Fig. D.7. In contrast to many other

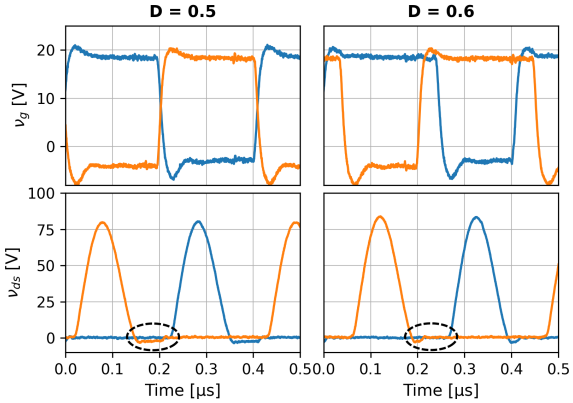

Fig. D.7: Measured voltage waveforms of the inverter under variation of the duty cycle to reduce diode active time.

inverter types, the body diodes of the MOSFETs are carrying current during a significant fraction of the switching period, since f_{ds} may be significantly larger

than f_{res}. The forward voltage of the MOSFET body diode is around 4 V, which means this is potentially a detriment to the inverter efficiency. However, as the drain voltage is shaped by drain-source resonance, there is no switching loss penalty for increasing the duty cycle to turn on the MOSFETs shortly following the start of diode conduction. This insensitivity of the turn-on timing greatly simplifies the operation of the inverter and makes the topology attractive for simple frequency tracking control implementations.

The drain-source resonance frequency variation with transistor voltage is shown in Fig. D.8. For very low voltages, (D.1) is not necessarily satisfied due to the large C_{oss}, but complete soft switching is not required for safe operation at low power. At higher voltage, the static capacitance dominates the MOSFET capacitance, and the resonance frequency variation with voltage is reduced.

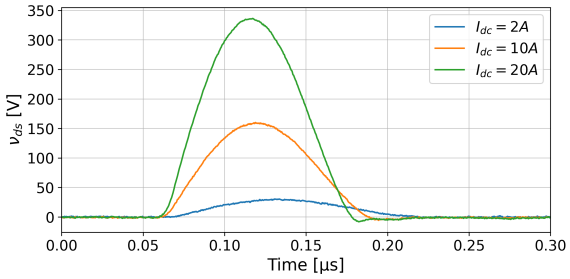

Fig. D.8: Measured drain-source voltage for varying input current showing the voltage dependency of the drain-source resonance frequency.

The measured resonance tank voltage and currents are shown in Fig. D.9. The apparent load resistance is around 1.4 Ω, showing that significant current levels are required for the loosely coupled load. The resonant tank current is not measured at higher voltage levels to have sufficient margin to the voltage limits for the current probe.

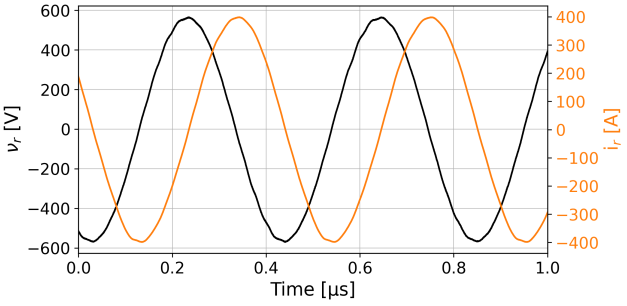

Fig. D.9: Measured resonant tank voltage and current at 1.6 kW input power.

Fig. D.10 shows the measured waveforms for a continuous input power of 5 kW. The inherent inclusion of parasitic parameters in the resonance loops allows for the clean voltage and current waveforms presented here, avoiding unwanted resonances even at high voltage and current levels. The transformer current was measured with a Rogowski probe and thus has a small delay that is apparent as a slight phase shift between the transistor voltage and the transformer input current. For the peak drain voltage 800 V, the voltage waveform width is $\frac{1}{2}T_{\mathrm{ds}} = 112$ ns, corresponding to $f_{\mathrm{ds}} = 4.46$ MHz, closely matching the predictions from Fig. D.6. Using the equivalent resistance value of 1.4 Ω in this load configuration and $V_{\mathrm{r,rms}} = 713$ V at this operating point, an estimated reactive power of 363 kVA is oscillating in the resonance tank.

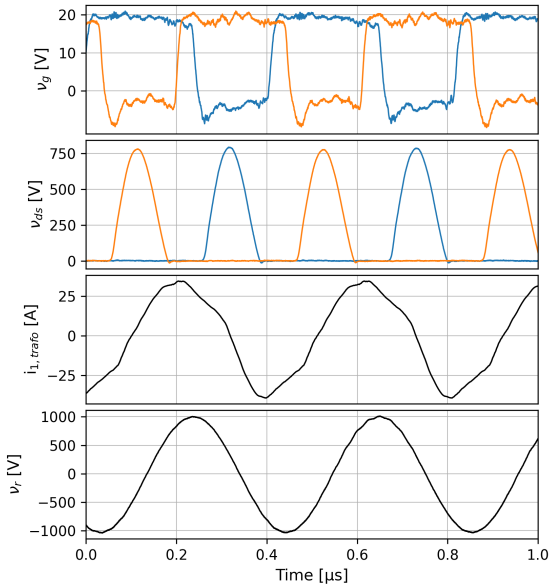

Fig. D.10: Measured voltages and currents of the inverter at 5kW input power.

The efficiency was measured calorimetrically, where the inverter has been operated continuously for 3 minutes to make sure the cooling water temperature had stabilized in each cooling loop. For an input power of 4.07 kW, an output power of 3.31 kW was dissipated in the resonant coil and load, while 0.21 kW was dissipated in the power module, yielding a system efficiency of 81% and a power module operational efficiency of 94%. The system efficiency is likely to be improved through optimization of the operational parameters and designs of the auxiliary components, while the power module efficiency demonstrates the applicability of the topology for RF heating purposes.

D.5 Conclusions and future work

This paper demonstrates a Class E push-pull resonant inverter for industrial MHz induction heating. The merits of the inverter topology in this application have been presented, and considerations for practical implementations of the inverter blocks have been discussed. A prototype inverter utilizing a 1700 V SiC MOSFET power module and a custom designed transformer has been demonstrated using a relevant industrial load. The system performance has been showcased under different operating conditions up to an input power of 5 kW, and an efficiency of 81% for the whole system and 94% for the power module has been calorimetrically measured. The presented design paradigm demonstrates the applicability of the Class E push-pull inverter for implementations of industrial MHz heating systems. Further studies will focus on improving these parameters and designs to increase the efficiency and scale up the power handling capability of the inverter.

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