Short-Circuit Instabilities in Silicon IGBTs and Silicon Carbide Power MOSFETs

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SHORT-CIRCUIT INSTABILITIES IN SILICON IGBTS AND SILICON CARBIDE POWER MOSFETS

BY
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by

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Preface

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"Life is a constant oscillation between the sharp horns of a dilemma."

by H.L. Mencken

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July 5, 2017
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Abstract

Power semiconductor devices are exposed to different type of stresses over their lifetime, which they need to overcome in order to guarantee long-term reliable operation up to 20 years or more. One of the most typical stresses that the device must withstand is related to short-circuit events, which occur randomly during the component's life. Silicon-based IGBTs are good candidates for limiting the external current in case of a short-circuit event, however their robustness is frequently limited due to instabilities. In this Ph.D. thesis, the short-circuit performance of silicon-based IGBTs has been extensively evaluated, but since Wide-Band Gap (WBG) devices, such as SiC MOSFETs, are rapidly growing as a potential substitute of silicon-based technologies, its robustness with respect to short circuit is also addressed.

One of the most important experimental findings, and also the main motivation of this thesis, is that IGBTs exposed under specific operational conditions suffer from high frequency gate voltage oscillations (i.e., tens of MHz). Such oscillations are very critical in case that they become unstable, which will cause the catastrophic damage of the device. This failure type cannot be explained by any known short-circuit failure mechanism reported in the literature. Therefore, the aim was to investigate which factors could lead the IGBT into an unstable behaviour. This was achieved by using a combination of finite-element device simulations and experimental investigations of 1.2 kV, 1.7 kV, 3.3 kV, IGBTs with different cell technologies (i.e., planar, trench and BIGT).

The experimental results demonstrate that the short-circuit ruggedness strongly depends on the applied DC-link voltage, this means that at low DC-link voltages the oscillations always occur, but at high DC-link voltages oscillations may not observed. A sensitivity analysis on the oscillating behavior's dependence revealed that there are some factors which help to minimize the oscillations: low gate-emitter voltage, high temperature and reduced stray inductance.

The root cause of the oscillation mechanism has been discovered to be as a consequence of a parametric oscillation, whose time-varying element is the Miller capacitance, leading to an amplification mechanism involving the external circuit. As a major achievement of this work, it has been possible to correlate the electric field distortions to

gate capacitance variations, and thus, associate the capacitance variation with charge-storage effects occurring at the surface of the IGBT. The analysis has demonstrated that the primary cause for the excess electron density at the surface of the IGBT is the weak electric field in this region, driven by the Kirk Effect. The carrier drift velocities have a strong impact on the charge balance of the IGBT, especially at low DC-link voltages. Therefore, the low drift velocities will cause electron accumulation effects due to the weak electric field. On the other hand, at high DC-link voltages, the carrier drift velocities become saturated across the whole n-base, which means that the charge-storage effect is no longer present and the input capacitance becomes fixed.

Dansk Abstrakt

Effektelektroniske komponenter anvendt i elektriske energisystemer udsættes for forskellige typer af stress igennem deres levetid og det er stress, som de skal modstå for at sikre en langsigtet pålidelig drift. Levetiden skal være op til 20 år og endda længere. En af de hyppigste belastninger, som komponenterne skal tåle er relateret til kortslutninger, som forekommer tilfældigt igennem komponenternes liv og som stresser dem. Silicium-baserede IGBT'ere er fremragende komponenter, som evner at begrænse strømmen i tilfælde af en kortslutning, men det er observeret at deres robusthed kan være begrænset på grund af ustabilitet. I denne Ph.D. afhandling er silicium-baserede IGBT'er primært blevet evalueret med hensyn til denne ustabilitet, men Wide Band Gap (WBG) baserede komponenter, såsom Silicium Carbide (SiC) MOSFET's er også studeret med hensyn til deres robusthed for kortslutninger, da disse komponenter vokser hurtigt på markedet som en potentiel erstatning for de silicium-baserede komponenter.

Et af de vigtigste eksperimentelle opdagelser, og som også er hovedmotivationen for denne afhandling er, at IGBT'er, når de udsættes for specifikke driftsbetingelser, oplever højfrekvente gate-spændings oscillationer (i 10-30 MHz området). Sådanne svingninger er meget kritiske, hvis de er ustabile, og de kan forårsage katastrofal skade på IGBT'ernr. Denne fejltype kan ikke forklares ved allerede kendte kortslutningsfejlmekanismer, som er rapporteret i litteraturen. Derfor har målet været at forstå fænomenet, der vil umiddelbart vil begrænse de undersøgte IGBT'eres kortslutningsevne i praksis. En bedre forståelse er blevet opnået ved at anvende en kombination af finite-element simuleringer af komponenternes strukturer og foretage eksperimentelle undersøgelser af 1.2 kV, 1.7 kV, 3.3 kV IGBT'ere, som har forskellige interne strukturer i deres opbygning.

De eksperimentelle resultater viser, at robustheden for kortslutningerne stærkt afhænger af den anvendte DC-spænding over IGBT'erne når de testes. Ved lave DC-spændinger forekommer svingningerne altid, mens ved høje DC-spændinger kan oscillationerne i mange tilfælde ikke observeres. En følsomhedsanalyse af oscillationernes afhængighed har vist, at der er nogle faktorer, der hjælper med at minimere oscillationerne såsom lav gate-emitter spænding, høj temperatur og lav spredningsinduktans i kredsen.

Hovedårsagen til oscillationerne har vist sig at være på grund af indgangs-kapacitansen i komponenten, der opfører sig stærkt ulineært og som giver en forstærkningsmekanisme,

der også involverer det eksterne kredsløb. Som et vigtigt bidrag i dette arbejde har det været muligt at korrelere de elektriske felt fordelinger i komponenten med variationer i komponentens kapaciteter og relatere kapacitans-variationen med ladningerne i komponenten, der forekommer på overfladen af selve IGBT'en. Analysen har vist, at den primære årsag til de overskydende elektroner på overfladen af IGBT'en er det svage elektriske felt i denne region, som er drevet af Kirk Effekten. Ladningernes hastighed har en stærk indvirkning på IGBT'ens ladningsbalance, især ved lave DC-spændinger. Derfor vil lave ladnings hastigheder forårsage akkumuleringseffekter af elektronerne på overfladen af IGBT'erne på grund af det svage elektriske felt i denne region. På den anden side bliver ladningernes drifts-hastigheder ved høje DC-koblingsspændinger begrænset på tværs af hele n-basen i IGBT'en, hvilket betyder, at lagringseffekten ikke længere er til stede, og input-kapaciteten bliver konstant og den samlede kreds dermed bliver stabil.

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Chapter 1

Introduction

This chapter presents the background and motivation of this thesis, followed by the problem definition, objectives and outline. A list of the publications related to the work presented in this thesis is included at the end.

1.1 Background and Motivation

1.1.1 Reliability needs for power electronic devices

Power semiconductor device performances are continuously improving in response to the ever increasing demands for more energy-efficient applications. The evolution of power semiconductor devices has always been focused on scaling up the power ratings, while at the same time improving the device performance in terms of efficiency, higher power density, increased robustness and reliability under both normal and abnormal conditions [1,2]. On the one hand, the result from this ceaseless device improvement reaches silicon's theoretical limit, but on the other hand, Wide-Band-Gap (WBG) devices have emerged in the last years to overcome such limitations. This does not necessarily imply that silicon-based semiconductor devices will decline its use. Indeed, the majority of the applications will still use silicon-based devices, basically due to their proven reliability and good cost performance ratio in comparison with WBG devices.

The high penetration level of renewable energy technologies have set ambitious goals for the upcoming years, where maintenance-free systems are needed [3]. This means that power electronics industries compete at the highest level to get the leadership in the power electronics market. For instance, the European Commission has established the *Horizon 2020* target [4], where the imposed requirements by the Renewable Energy Directive (RED) has led to a fast development, and thanks to that, 26% of the today's EU power is generated from renewable energy. Indeed, 10% of the total EU's electricity

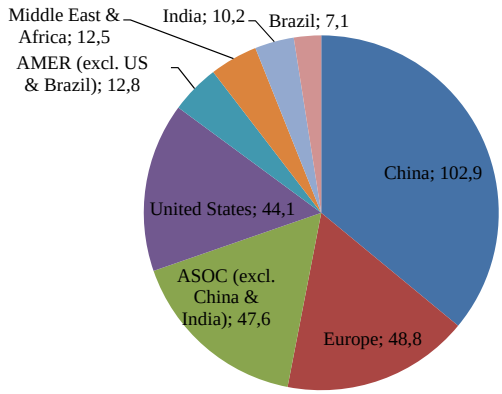

Figure 1.1: *Global trends in renewable energy investment 2015 ($ billion). Source: FS-UNEP [7].*

is generated from renewable electricity, such as wind and solar [5]. The trajectory of European renewable energy sources in 2014 compared with the 2020 targets can be found in [6]. Some countries have already reached their 2020 targets (i.e., Sweden, Bulgaria and Finland), others are progressing slower (i.e., France and Netherlands) but the majority of them are expected to meet and/or exceed the 2020 renewable energy targets. The worldwide trajectories of renewable energy investment in the 2004-2015 period can be found in Fig. 1.1. Here it is observed that China leads with a major advantage over the remaining regions, followed by Europe, United States and Japan [7].

To accelerate the transition towards long-term lifetime of power electronic systems, i.e., typical design targets are about 10 - 20 years [3], reliability studies are indispensable in order to identify the weakest components. The latest reliability survey based on field experiences from power electronics manufacturers [8], demonstrates that about 31% of the 56 responders consider semiconductor devices as the main responsible of power electronic failures. Moreover, today's most dominant semiconductor device is the Insulated-Gate Bipolar Transistor (IGBT), according to [8], 43% choose the IGBT among the available semiconductor devices. This means that the IGBT is one of the most critical components of the whole power system and for this reason many efforts have been devoted to improve its reliability including robustness. So far, Wide-Band-Gap devices have not been adopted in the market as fast as people have hoped. The situation is that this technology has not reached a sufficient level of maturity and therefore, it is still early to talk about the replacement of the well-established silicon technologies.

Prognostics and systems health management are a major driving force to assess the status of a system, by predicting the remaining useful life and or diagnosing abnormal behaviour. Nevertheless, industries are still struggling with failure modes which are

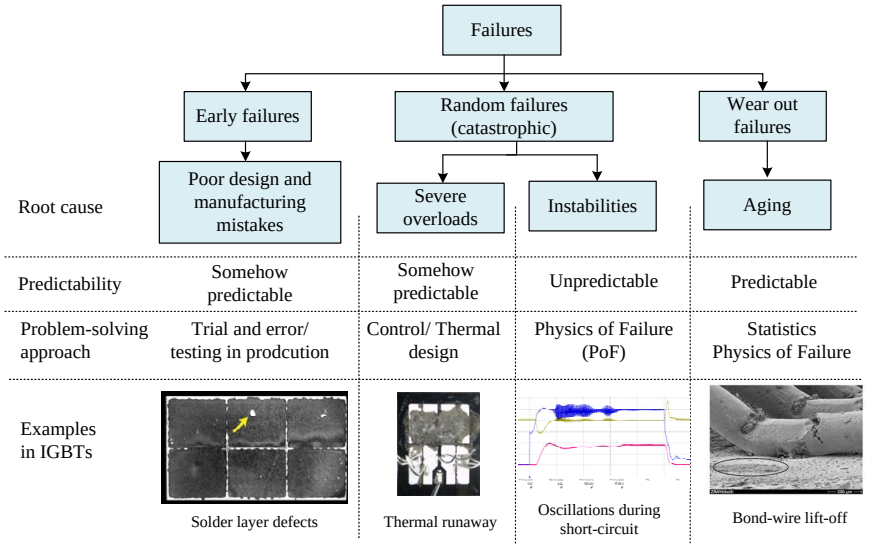

Figure 1.2: *Classification of failures in Power Electronics.*

unpredictable, also known from the *bathtub curve* as random failures [9]. Failure mechanisms can be classified into three categories as illustrated in Fig. 1.2: early failures, random failures and wear out failures. Early failures come from lack of production capabilities such as poor designs and manufacturing mistakes. This type of failure has nothing to do with the degradation of the product and they are typically detected in the first weeks of use. Wear-out failures come from the unavoidable degradation of the component with time and they can often be predicted thanks to health monitoring systems. However, the random or catastrophic failures are the ones which cannot be predicted because they do not show any evidence prior to the failure, only after post-failure analysis and understanding of the root cause is possible to redesign the component to mitigate the problem. As it can be seen in Fig. 1.2, random failures can be broken into two groups [10], i.e. severe overloads and instabilities. Severe overloads are characterized as single-event external stresses such as over-voltage, over-current, short circuit, overheating and cosmic rays, which can be somehow expected and predicted. On the other hand, instabilities are fully dependent on the internal physical mechanisms of the device, causing a loss of control and possible destruction of the device itself. The prediction of instabilities is complex since they could also be triggered by severe overloads and its evolution depends on many parameters, such as temperature, voltage variation, inductive and capacitance effects, unbalanced current distribution and also EMI (ElectroMagnetic Interfece).

It is thus noticeable that catastrophic failures cannot be neglected for fulfilling the imposed high-reliability targets. It is thus of special importance to map which catastrophic failures have been observed, mainly instabilities in this thesis, for one of the most reliability-critical components in power electronics systems - the IGBT. Additionally, as Silicon Carbide (SiC) power MOSFETs are becoming popular and starting to compete with silicon IGBTs, the short-circuit instabilities occurring in SiC power MOSFETs will be briefly discussed.

1.1.2 The short-circuit performance in IGBTs

The IGBT has gained year-by-year a great success thanks to its attractive features by combining both MOS and bipolar structures in order to achieve the optimum trade-off between the switching loss, on-state loss and large safe operation area [11]. However, its optimum performance is often limited by its lack of short-circuit robustness. From the experimental point of view, the IGBT testing conditions defining the short-circuit safe operation area are well-known, such as junction temperature, gate voltage, and maximum short-circuit time. The maximum short circuit time of the IGBT is typically longer than 10 μs, but in some specific applications, IGBTs still fail way earlier than 10 μs, which is the standard desaturation protection time of modern gate drivers, but also the specified value on the device datasheet.

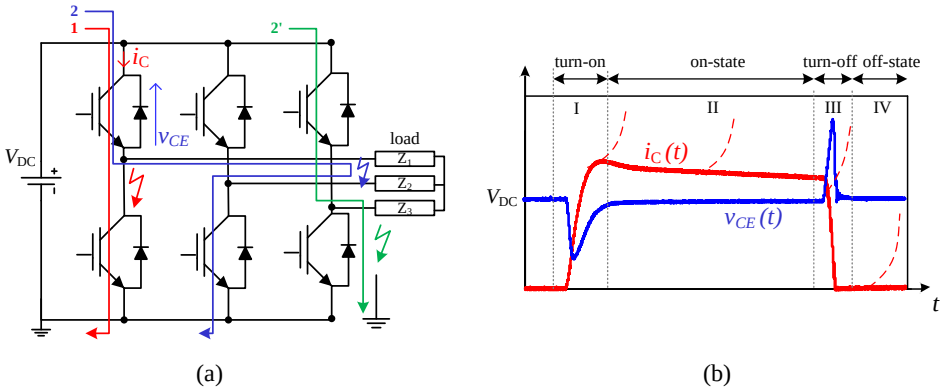

Figure 1.3: *The short-circuit condition applied to IGBTs: (a) short-circuit paths in a three-phase voltage source converter, and (b) types of failures during a short-circuit event.*

In power electronic circuits, a short-circuit can occur in many different ways; the most common ones are type 1 and type 2. Fig. 1.3a shows a traditional three-phase voltage source converter commonly found in motor drives applications. The short-circuit

type 1 is a a short circuit that already exists when the device under test is turned on (path 1 in Fig. 1.3a). This situation occurs when the upper and lower IGBTs are both conducting. On the other hand, the short-circuit type 2 is a short circuit taking place when the IGBT is conducting. In this case, the fault can be observed from the bridge arm to phase (see the path 2 in Fig. 1.3a) and from the bridge arm to ground (see the path 2' in Fig. 1.3a). During the short-circuit event, the IGBT may withstand the overstress and successfully be turned off by the gate driver, or in the contrary, it could lead to a catastrophic failure. The short-circuit failures can be classified into four, depending on the moment at which the failure takes place, as it is shown in Fig. 1.3b. The first failure mode occurs during the turn-on transient, e.g., a failure of the device itself due to some sort of instability. The second failure mode occurs during the on-state, for example if the dissipated energy is greater than a critical value. The third failure mode occurs during the turn-off transient, e.g. a large voltage overshoot. And last, the fourth failure mode occurs during the off-state, typically related to a leakage current increase causing thermal runaway failures.

1.1.3 Overview of short-circuit instabilities in Si-IGBTs

In the following, the instability mechanisms occurring in IGBTs during short-circuit events are discussed: latch-up, negative differential resistance, current filamentation and short-circuit oscillations.

1.1.3.1 Latch-up

One of the most problematic instabilities of the IGBT since its initial release is the latch-up. Basically, the IGBT collector current can no longer be controlled by the gate voltage, similarly as a conventional thyristor. Fig. 1.4a shows the structure of the IGBT together with its equivalent circuit [14]. The IGBT is formed by a couple of NPN/PNP transistors representing a parasitic thyristor that must be kept inactive. The static latch-up mode is triggered if the voltage drop across the shunt resistance, R_s, of the P body layer, is not sufficiently low. On the other hand, the dynamic latch-up mode occurs if a large displacement current flows across the depletion capacitance of the n-drift/ p-body junction, C_s. The problem of latch-up has been solved for today's IGBT designs through different methods as presented in [15], where the most common one is associated to the reduction of the resistivity of the p^+ body region by fabricating a thinner layer underneath the n^+ source. During short-circuit events, the current densities are high, and the lateral hole flow in p-body region could increase the voltage drop across R_s. Another case of latch-up could be caused by the temperature rise, lowering the potential barrier of the n^+ source /p-body junction, leading to the activation of the thyristor.

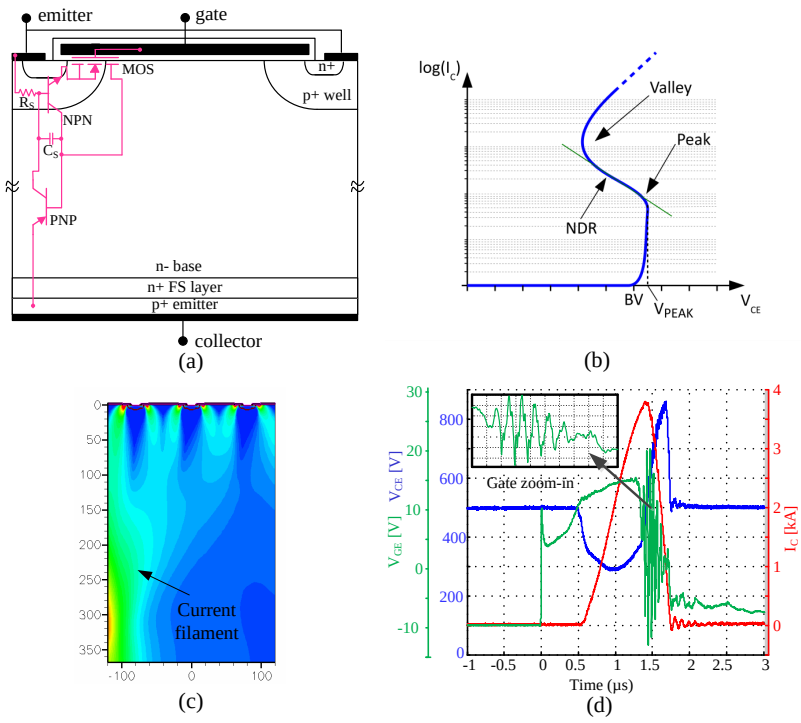

Figure 1.4: *Short-circuit instabilities in IGBTs: (a) IGBT structure highlighting the parasitic thyristor as main cause of latch-up, (b) the NDR region in the I-V curve [10], (c) a device simulation showing the current filamentation mechanism [12], and (d) oscillation phenomena during short-circuit events [13].*

1.1.3.2 Negative Differential Resistance (NDR)

The high temperatures achieved during short-circuit conditions play a major role as the root cause for complex instability mechanisms. A Negative Differential Resistance (NDR) region appears in the I-V curve, as shown in Fig. 1.4b, when the voltage cannot further increase because the electric field peak inside the device is clamped due to avalanche generation conditions [16,17]. In this situation, the current tends to focus on a few cells, as a consequence of the NDR electro-thermal instability. The filamentary current has been validated by means of device simulations in [18]. It is associated with a local temperature increase and formation of hot spots, as demonstrated in [19], with thermo-graphic pictures of a trench IGBT chip. The destructive phenomenon is associated with the high current density of the IGBT, and in particular with the current

gain of the *pnp* bipolar transistor α_{PNP}. The NDR effect and avalanche generation will set in as a function of the α_{PNP}, therefore, in order to counteract this effect, an optimization of the buffer layer and the α_{PNP} have been presented as solutions to the problem [20].

1.1.3.3 Current filamentation

The current filamentation mechanism is still an interesting research topic involving imbalances in the current distribution inside the IGBT chip. Some studies attribute this instability to the high electric fields at the emitter side of the IGBT and consequent impact ionization mechanism [21]. Other studies claim that the IGBT is driven into the NDR region triggering the current filamentation mechanism, as presented above. However, a more recent work shows that the electric field peak during short-circuit conditions is no longer located at the emitter side but transferred to the collector side [12]. In [22], it is explained that the current filament can only set in when the electric field peak is located at the emitter side and the field on the emitter has drop below a critical value. This hypothesis is supported by device simulations (see Fig. 1.4c), where the current filamentation mechanism is located at the emitter of the IGBT and it is caused by the effects coming from the rotation of the electric field (Kirk Effect).

1.1.3.4 Short-circuit oscillations

Gate-voltage oscillations have been observed during short-circuit events, as it can be seen in Fig. 1.4d, which may lead to the device destruction [13]. Until now, the origin of such oscillations has been explained from two different points of view: the external circuit design and the IGBT internal physics mechanisms. Regarding the first one, many efforts have been devoted to mitigate the oscillations: (1) optimization of the layout design [23–25], (2) the increase of the gate resistance [26], (3) stability maps have been proposed to correctly select the external circuit elements to operate the device within its stable region [27,28], and (4) parallel chip configurations have been found to oscillate more than single-chip devices [29,30]. From the internal physics point of view different interpretations have been given: (a) the presence of a negative capacitance under high temperatures and high collector voltages [31,32], (b) the Plasma Extraction Transit Time (PETT) effect and the dynamic IMPact ionization Avalanche Transit Time (IMPATT) effect as the excitation mechanisms for high frequency oscillations during IGBT turn-off [33,34], and (c) optimization of the chip design [25].

1.1.4 Overview of short-circuit instabilities in SiC MOSFETs

In the wake of rapid progress in Wide-Band-Gap semiconductors (WBG) devices, SiC MOSFETs are starting to compete with today's popular Si IGBTs, which slowly approach their limits in terms of power losses, maximum allowable junction temperature

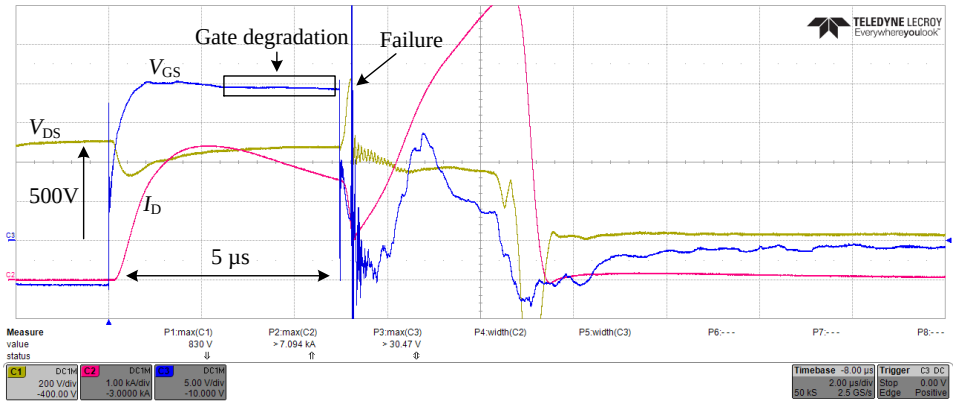

Figure 1.5: *Example of a gate-oxide breakdown failure of a 1.2 kV/ 300 A SiC MOSFET power module performed at 500 V of drain-source voltage.*

and safe operation area [35]. Although the claimed superior performance of SiC devices has been well demonstrated in the literature, many challenges need to be overcome for SiC devices to firmly establish themselves as a mainstream in power electronics systems. One major hurdle is the higher manufacturing cost associated to the SiC technology, but putting this issue aside, SiC MOSFETs also suffer from the ability to withstand stressful conditions such as short circuit events. Short circuits are frequent events in a number of applications (e.g., motor drives), therefore SiC MOSFETs must be able to withstand them up to 10 μs at their nominal voltage and the highest temperature. In the following, a review of failure mechanisms regarding the use of SiC power MOSFETs under short-circuit operations is briefly discussed.

1.1.4.1 Gate-oxide degradation

The gate-oxide degradation is one of the major drawbacks limiting the SiC MOSFET short-circuit robustness. An example of this failure mode can be observed in Fig. 1.5, where a commercial SiC power module rated at 1.2 kV fails within 5 μs at drain-source voltage of 500 V. SiC MOSFETs have smaller oxide thickness and relatively high electric fields at a given gate bias, in contrast with its silicon counterparts. In short circuit, a sufficiently high electric field is applied across the oxide coupled with high current densities at the channel. These features may lead into a degradation of the dielectric material and formation of conductive paths. Experimental evidence of the gate-oxide degradation has been reported by various authors in [36–39], where a decrease of V_{GS} has been correlated with the increase of leakage current between gate and source prior

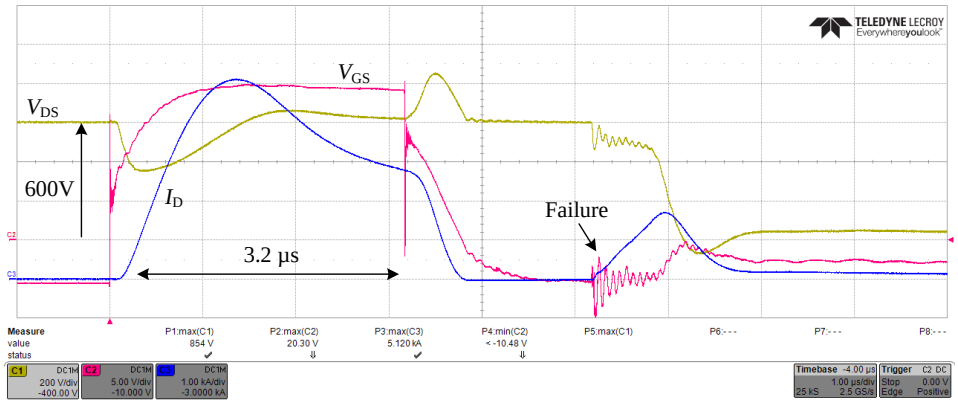

Figure 1.6: *Example of a thermal runaway failure of a 1.2 kV/ 300 A SiC MOSFET power module performed at 600 V of drain-source voltage.*

to the gate breakdown failure [40]. However, the gate leakage current level is not the responsible for the failure [37]; instead, it has been suggested that a tunnelling effect takes place as a consequence of the high electric field and high temperature, which eventually leads to electrons penetrating into the oxide [37, 41]. A Bias Temperature Instability (BTI) effect has also been discussed in [37,41], resulting in an increase of the threshold voltage and decrease of the drain current, mainly attributed to the creation of interface traps and oxide charges coming from the positive/negative gate bias at high temperatures. While the interpretation of the gate degradation phenomenon is still unclear, on the other hand, the location of the trapped charges is nowadays unknown, and further investigation need to be done to confirm the above theories. Steps are being taken on the investigation of the gate oxide degradation by using SEM (Scanning Electron Microscopy) graphs of FIB (Focused Ion Beam) cuts in [42]. Cracks in the Poly-Silicon gate have been identified, however, micro-graphs of the oxide are difficult to take because its small thickness ($\approx$ 50 nm). Understanding the gate-oxide reliability of SiC power MOSFETs requires further investigation, since SiC MOSFETs lack from their short-circuit withstanding capability, far from reaching the standard 10 μs duration at rated voltage and temperature.

1.1.4.2 Thermal runaway

SiC power MOSFETs are also prone to thermal runaway failures during short-circuit events, as several recent works have proved so for discrete devices [43], and modules [36]. An example of this failure mode can be observed in Fig. 1.6, where the current suddenly increases 2 μs after the device turn-off. Two precursors prior to the failure have

been observed: (i) turn-off current tails [36, 40, 43] and (ii) slope change in the current waveform at the end of the short-circuit pulse [43]. The interpretation of the failure mechanism has been possible with the help of thermal maps of the active surface during the thermal runaway failure [44, 45]. The thermal maps evidence unstable behaviour and formation of a hot spot from one side and current imbalance increasing with time indicating device degradation on the other side. The thermal runaway failure has been attributed to thermally generated hole current flowing in the drift region and source p-well by Finite-Element simulations in [43].

Additionally, an important study identifying a non-uniform current distribution inside of the SiC MOSFET cell under short-circuit by introducing cell inhomogeneities can be found in [45]. Channel doping, length and difference on interface traps concentration have been introduced to trigger current density unbalances and hot-spot failures.

1.2 Problem Definition

IGBTs are exposed to different type of stresses over their lifetime, which they need to overcome in order to fulfil the product design specifications. One of the most typical stresses that the device must withstand is related to short-circuit conditions, which occur randomly during the component's life. IGBTs show several instabilities as briefly described in the previous section; among them, the oscillation phenomena often observed under short-circuit events lacks of a conclusive theory to explain the root cause of the unstable operation. In spite of the theories and solutions presented in the literature for suppressing the gate voltage oscillations, the short-circuit robustness is still a problem in modern IGBT devices. As an example, Fig. 1.7 shows the experimental results of a commercial 1.7-kV/ 1-kA IGBT module with trench IGBT technology under a short-circuit test, in which oscillations are clearly observed, implying that this oscillation instability still remains as an unsolved problem. The motivation of this thesis was to understand the process that limits the IGBT short circuit ruggedness by studying the effects on both device, operating conditions and layout influences. To reach this goal, the circuit design parameters and testing conditions that influence the occurrence of the oscillation phenomenon are experimentally tested first, and compared later with mixed-mode device simulations. The physical mechanisms taking place during the short-circuit will be better understood thanks to the mixed-mode simulations with Sentaurus TCAD tool. They will help to suggest solutions that may require a rethinking of the IGBT design and, last but not least, recommended testing conditions will be necessary to avoid oscillations.

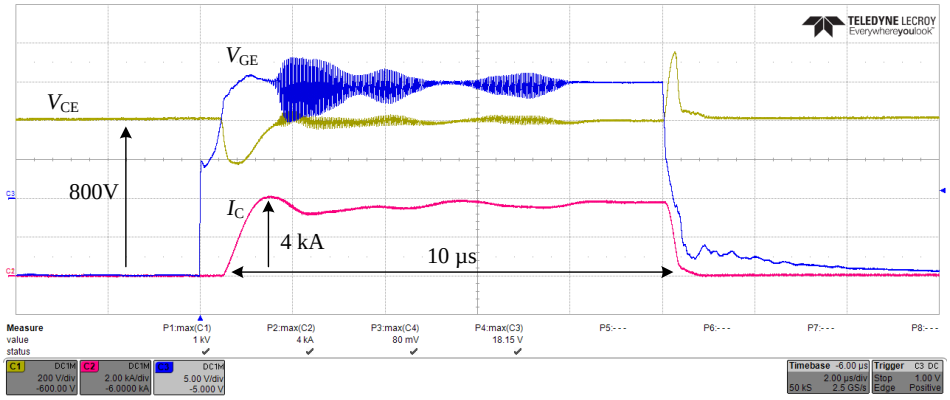

Figure 1.7: *Oscillations during a short circuit test of a 1.7 kV/ 1 kA IGBT power module performed at 800 V of collector voltage. Time scale: 2 µs/div; gate voltage: 5 V/div; collector voltage: 200 V/div; collector current: 2 kA/div [13].*

1.3 Thesis Objectives

The major aim of this thesis is to provide a deep insight into the instability mechanisms occurring in Insulated-Gate Bipolar Transistors (IGBTs) under abnormal conditions. Numerical tools based on finite element methods have been used to study the factors that influence the occurrence of such instabilities. In this work, special focus is given on the gate-voltage oscillations appearing during short-circuit events. At the starting point of this project, experimental tests have been done first, demonstrating that the short circuit ruggedness of IGBTs was limited by the occurrence of critical gate-voltage oscillations. The testing conditions triggering such oscillations and main circuit parameters enhancing them were not known. The root cause of the failure mechanism was not known and the prior-research work and/or theories presented in the literature did not fit with the preliminary short-circuit test results. Overall, this Ph.D. intends to answer the following research question:

- Which is the root cause of the gate voltage oscillations occurring during short-circuit events? How is it possible to increase the short-circuit robustness of silicon IGBTs?

With this research question, the objectives of this PhD thesis are listed below in details:

Experimental evaluation of discrete IGBTs and power modules under short--circuit conditions The short-circuit performance of different IGBT technologies,

such as planar and trench, from different manufacturers will be experimentally investigated. A Non-Destructive Tester (NDT) will be constructed with the capability of repetitively testing semiconductor devices up to 2.4 kV and 10 kA. The testing conditions will be varied, i.e., DC-link voltage, temperature and gate voltage. The layout influence on the oscillations will also be investigated.

Finite-Element device simulations of the IGBT short-circuit performance with TCAD This study is aimed to simulate the gate voltage oscillations observed experimentally during a short circuit event. A sensitivity analysis on the testing conditions and circuit parameters effects will be performed, in order to correlate both simulation and experimental observation to reach a consistent theory.

Evaluation of simulation results, hypothesis and prospective solutions The root cause of the oscillatory phenomenon will be formulated based on the physical mechanisms occurring inside of the IGBT during a short circuit condition. The possibility to damp such oscillations from the external circuit design and/or from the device design will be proposed, with the aim to improve the IGBT robustness under short-circuit conditions.

Evaluation of the short-circuit robustness of silicon carbide MOSFETs As SiC power MOSFETs are a potential substitute of silicon IGBTs, its performance under short-circuit events will be evaluated and compared. The new challenges limiting the short-circuit performance of SiC power MOSFETs will be brought to light.

1.4 Project Limitations

The short circuit characteristic of a semiconductor device depends on the time instant at which the short-circuit occurs. The short-circuit type 1 happens during the turn-on of the DUT; on the contrary, type 2 occurs during the on-state of the DUT. In this work, short-circuit type 1 has been investigated, since the information that can be found in the device's datasheet corresponds with type 1 rather than type 2.

The experiments included in this project have been carried out thanks to two different non-destructive testers. It is well known that the short circuit characteristic strongly depends on specific parameters like temperature, stray inductances and gate driving circuit, which have been taken into consideration. Nevertheless, short-circuit tests on a real field application, where stray inductances may be higher than the ones used in the experimental testers, are not provided.

There are many IGBT designs available in the literature and on the market with different voltage classes, but only two IGBT topologies are considered for the finite-element simulations, e.g., planar and trench-gate designs with blocking capability of

3.3 kV. The outcome from the mixed-mode device simulations and root cause of the oscillations, can later be adopted for other IGBTs having different doping profiles. Minor modifications on the circuit parameters might be necessary in order to simulate the short-circuit oscillations.

The short-circuit capability of SiC power MOSFETs has been experimentally assessed, pointing out the weaknesses and the barriers that the SiC power MOSFET technology must overcome in order to win the competition against silicon IGBTs. Nevertheless, a deep understanding of the failure mechanisms occurring in SiC MOSFETs has not been provided, basically due to two major hurdles: 1) availability of a reliable SiC MOSFET model to be simulated with Sentaurus TCAD, and 2) SiC-based devices have not reached a sufficient level of maturity, meaning that it exists a wide spread of its inherent characteristics, such as threshold voltage V_{th}, saturation current level and on-state resistance. Therefore, the performance of today's devices will most likely be different from the upcoming new generations.

1.5 Outline of the Thesis

This thesis takes the form of a monograph, which is based on a number of publications that are listed at the end of this Chapter and also cited along this Ph.D. thesis. Fig. 1.8 gives a brief overview of the thesis structure with the corresponding research highlights. The monograph consists of 6 chapters and 14 published papers (8 are conference papers and 6 are articles). More in detail, the structure of the thesis is organized as follows:

- Chapter 1 presents the introduction, background and motivation of this thesis. The objectives are stated for a better definition of the investigated problem.
- Chapter 2 shows the short-circuit performance of today's IGBTs with special focus on the oscillation instability. Single chip and parallel-chip configurations are tested under different testing conditions and layout designs, revealing the oscillation phenomena dependence.
- Chapter 3 evaluates the short-circuit oscillation phenomenon in planar IGBTs by the aid of semiconductor device simulations. Mixed-mode simulations have been performed with TCAD on a 3.3 kV IGBT half-cell demonstrating that a single IGBT cell is able to oscillate by itself. A sensitivity analysis will serve as the key stone for the understating of the physical mechanisms driving the IGBT into an unstable operation.
- Chapter 4 deals with the formulation of a consistent theory which explains the root cause of the gate-voltage oscillations. In order to demonstrate the effectiveness of the proposed theory, solutions are given to mitigate the oscillatory behaviour of

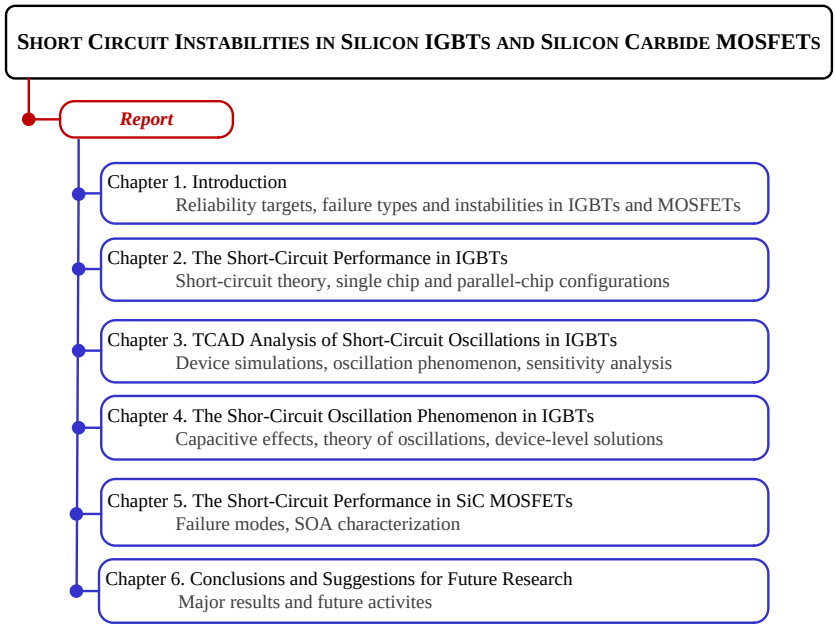

Figure 1.8: *Thesis structure and highlights of each part.*

the IGBT. Indeed, short-circuit device simulations validate the proof of concept of the suggested solutions.

- Chapter 5 gives an insight of the future challenges in emerging technologies, such as silicon carbide, during short-circuit operation. Repetitive short-circuit tests on SiC MOSFET power modules help to collect data to investigate future failure mechanisms and reveal today's safe operation area of state-of-the-art silicon carbide devices.
- Chapter 6 discusses the conclusions and contributions of the thesis together with future research perspectives.

1.6 List of Publications

A list of the papers in relation to this Ph.D. thesis, which are published and/or have been submitted, is given as follows:

Journal Papers

J1. **P.D. Reigosa**, F. Iannuzzo, H. Luo and F. Blaabjerg, "A Short Circuit Safe Operation Area Identification Criterion for SiC MOSFET Power Modules," *in IEEE Transactions on Industry Applications*, vol. 53, no. 3, pp. 2880-2887, May-June 2017.

J2. **P.D. Reigosa**, D. Prindle, G. Paques, S. Geissmann, F. Iannuzzo, A. Kopta and M. Rahimo, "Comparison of Thermal Runaway Limits under Different Test Conditions Based on a 4.5 kV IGBT," *Microelectronics Reliability*, pp. 524-529, Sept. 2016.

J3. **P.D. Reigosa**, R. Wu, F. Iannuzzo and F. Blaabjerg, "Robustness of MW-Level IGBT Modules Against Gate Oscillations under Short Circuit Events," *Microelectronics Reliability*, vol. 55, issue 9-10, pp. 1950-1955, Oct. 2015.

J4. R. Wu, **P.D. Reigosa**, F. Iannuzzo, L. Smirnova, H. Wang and F. Blaabjerg, "Study on Oscillations during Short Circuit of MW-Scale IGBT Power Modules by Means of a 6-kA/1.1-kV Non-destructive Testing System,"*IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, issue 3, pp. 756-765, Sept. 2015.

J5. **P.D. Reigosa**, F. Iannuzzo, M. Rahimo, C. Corvasce and F. Blaabjerg, "Improving the Short-Circuit Reliability in IGBTs - How to Mitigate Oscillations," submitted to *IEEE Transactions on Power Electronics*, in review, 2017.

J6. **P.D. Reigosa**, F. Iannuzzo, M. Rahimo,and F. Blaabjerg, "Capacitive Effects in IGBTs Limiting their Reliability under Short Circuit," accepted to *Microelectronics Reliability*, in review, 2017.

Conference Papers

C1. **P.D. Reigosa**, H. Wang, F. Iannuzzo and F. Blaabjerg, "Approaching Repetitive Short Circuit Tests on MW-Scale Power Modules by means of an Automatic Testing Setup," in *Proc. of the IEEE Energy Conversion Congress and Exposition*, Sept. 2016.

C2. **P.D. Reigosa**, F. Iannuzzo, H. Luo and F. Blaabjerg, "Investigation on the Short Circuit Safe Operation Area of SiC MOSFET Power Modules," in *Proc. of IEEE Energy Conversion Congress and Exposition*, Sept. 2016.

C3. C.G. Suarez, **P.D. Reigosa**, F. Iannuzzo, I. Trintis and F. Blaabjerg, "Parameter Extraction for PSpice Models by means of an Automated Optimization Tool - An IGBT model Study Case," in *Proc. of PCIM Europe*, May. 2016.

C4. **P.D. Reigosa**, F. Iannuzzo, S.M. Nielsen and F. Blaabjerg, "New layout concepts in MW-scale IGBT modules for higher robustness during normal and abnormal operations," in *Proc. of APEC*, pp. 288-294, March 2016.

C5. R. Wu, **P.D. Reigosa**, F. Iannuzzo, H. Wang and F. Blaabjerg, "A Comprehensive Investigation on the Short Circuit Performance of MW-level IGBT Power Modules," in *Proc. of EPE-ECCE Europe*, Sept. 2015.

C6. **P.D. Reigosa**, R. Wu, F. Iannuzzo and F. Blaabjerg, "Evidence of turn-off gate voltage oscillations during short circuit of commercial 1.7 kV/1 kA IGBT power modules," in *Proc. of PCIM Europe*, pp. 916-923, May 2015.

C7. **P.D. Reigosa**, F. Iannuzzo and F. Blaabjerg, "Packaging Solutions for Mitigating IGBT Short-Circuit Instabilities," in *Proc. of PCIM Europe*, pp., May 2017.

C8. **P.D. Reigosa**, F. Iannuzzo and M. Rahimo, "TCAD Analysis of Short-Circuit Oscillations in IGBTs," in *Proc. of ISPSD*, pp., May 2017.

There are also other publications which are not related with the contents of this thesis, however, they are relevant since they have been published during the author's Ph.D. period.

Journal Papers

J1. H. Luo, F. Iannuzzo, **P.D. Reigosa** and F. Blaabjerg "Modern IGBT gate driving methods for enhancing reliability of high-power converters - An overview," *Microelectronics Reliability*, vol. 58, pp. 141-150, 2016.

J2. **P.D. Reigosa**, H. Wang, Y. Yang and F. Blaabjerg, "Prediction of Bond Wire Fatigue of IGBTs in a PV Inverter Under a Long-Term Operation," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7171-7182, Oct. 2016.

Conference Papers

C1. G. Tsolaridis, K. Ilves, **P. D. Reigosa**, M. Nawaz and F. Iannuzzo, "Development of Simulink-based SiC MOSFET modeling platform for series connected devices," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept. 2016.

C2. Y. Shen, H. Wang, Y. Yang and **P. D. Reigosa** and F. Blaabjerg, "Mission profile based sizing of IGBT chip area for PV inverter applications," in *Proc. of the 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, June 2016.

C3. H. Wang, **P.D. Reigosa** and F. Blaabjerg, "A humidity-dependent lifetime derating factor for DC film capacitors," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, pp.3064-3068, 2015.

Chapter 2

The Short-Circuit Performance in IGBTs

This chapter presents the experimental results and investigations on the short-circuit capability of different IGBT technologies and voltage classes. The outcome of these results is of particular importance to reach conclusions on the device and circuit design effects for optimum performance under short-circuit conditions.

2.1 Description of the Experimental Test Bench

The experimental work has been conducted within two research institutions. Most of the experimental activity has been done at the Center of Reliable Power Electronics (CORPE), Aalborg University, Denmark, and some of the work has been undertaken at ABB Switzerland Ltd, Semiconductors, where the author spent nearly 6 months. Therefore, it is of special importance to describe both experimental facilities, whose operating method is based on the non-destructive testing concept.

2.1.1 The operating principle of the Non-Destructive Tester

The basis of the non-destructive technique is to perform repetitive short-circuit testing of power semiconductor devices up to their physical limits, allowing for post-failure analysis if the device suddenly becomes damaged. The design of such testing facility needs to fulfil with the following requirements: series protection switches are a must to rapidly turn-off the short-circuit current in case of failure, high rated current devices are needed to sustain the large short-circuit currents and a low busbar inductance is desired to minimize voltage overshoots and mitigate device instabilities. The test bench has to

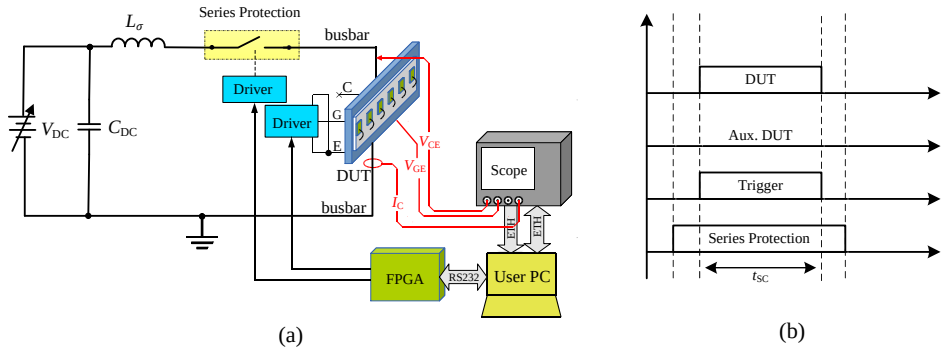

Figure 2.1: *The principle of the Non-Destructive Testing (NDT) system for short-circuit operation: (a) circuit schematic, and (b) time settings for short-circuit type 1 [46].*

be flexible, in order to adapt several fixtures for testing modules with different housing packages. Finally, the system must be highly automated for supervising the repetitive short-circuit sequence, always aiming at safety protection and remote control.

In Fig. 2.1, the schematic of the setup is illustrated together with the typical timings during a short-circuit type 1. The capacitance C_{DC} is connected to the Device Under Test (DUT), through the busbar and series protection, providing the energy needed for the short-circuit test. The capacitance C_{DC} is first charged up to the desired voltage, then the series protection is closed and the DUT is connected directly to the C_{DC} capacitor to perform a short-circuit at the DUT's turn-on. The series protection acts as a circuit breaker and it is programmed to open a few microseconds after the test, ensuring that the current is turned off in a controlled way.

2.1.2 Description of the 2.4-kV/ 10-kA Non Destructive Tester (NDT) at CORPE

Fig. 2.2 shows a picture of the non-destructive testing facility developed for repetitive short-circuit tests. The description of the hardware and software implementations has been previously reported in [36, 47]. From the picture, it can be recognized the components schematically illustrated in Fig. 2.1, whose ratings are listed in Table 2.1. The measurement equipment employed can be found in Table 2.2. The tester consists of a bank of ten capacitors representing C_{DC} and four IGBT power modules arranged in parallel as part of the series protection, whose total current capability is 10 kA. An optimized round busbar has been designed by means of a commercial CAD tool (Computer Aided Design tool) and a FEM (Finite-Element Method) software. The goal was

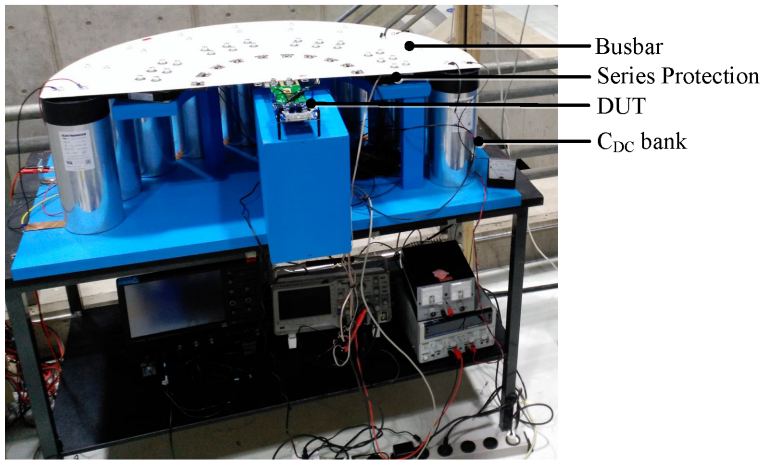

Figure 2.2: *A picture of the 2.4-kV/ 10-kA Non-Destructive Testing (NDT) test bench for repetitive short-circuit tests [36].*

to minimize the stray inductance and ensure that the current is shared evenly between the four IGBT power modules consisting the series protection [48].

Table 2.1: *Ratings of the main elements in the NDT setup.*

Characteristic	**Value**
DC Maximum voltage	2.4 kV
DUT Maximum current	10 kA
DC capacitors, C_{DC}	10 x 1100 μF, 2400 V
Stray inductance in the main loop	50 nH
Series protection	4 Dynex DIM1500ESM33-TS000 3-kA/ 3.3-kV

The experiments reveal that the overall inductance including the capacitors and the series protection is about 50 nH, which could be considered large for short-circuit testing purposes, however, it is more realistic if compared with the stray inductance values that can be found in the field. The DUT and series protection gate drivers are synchronized by means of a Field-Programmable Gate Array (FPGA), providing the precise timings with an accuracy of 10 ns. A LeCroy HDO6104-MS oscilloscope is connected to the PC by means of an Ethernet link and to the FPGA through an RS-232 bus [47]. The oscilloscope acquires the electrical waveforms V_{GE}, V_{CE} and I_C.

The 2.4-kV/ 10 kA NDT provides the possibility to perform repetitive tests by means of an original automated tool having a Graphical User Interface (GUI), whose

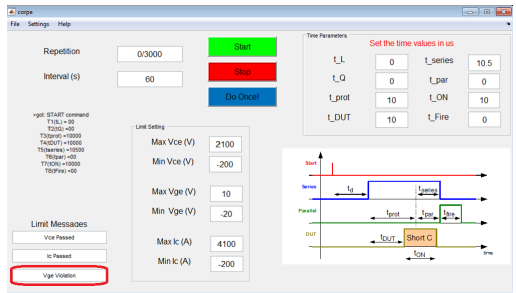

Figure 2.3: *A screen-shot of the Graphical User Interface to perform the repetitive short-circuit sequence. A sample violation condition is evidenced [47].*

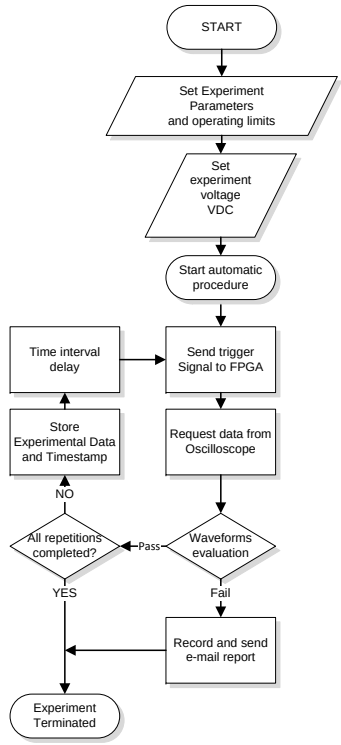

Figure 2.4: *Flowchart of the implemented repetitive short-circuit sequence [47].*

Table 2.2: *Equipment list.*

Device	**Type**	Bandwidth (-3 dB)
Oscilloscope	LeCroy HDO6104-MS	1 GHz
Current Probe	CWT30 (6 kA) Rogowski current probe	30 MHz
HV Passive Probe	LeCroy PPE 1.2 kV	300 MHz
Passive Voltage Probe	Tektronix TPP0200	200 MHz

appearance can be observed in Fig. 2.3. This tool has been thoroughly described in [47], thus, just a brief explanation is given in the following. The parameters that can be modified are the time settings, the number of tests to be performed and the time interval between consecutive tests. With the aim to safeguard and protect the user, the GUI provides a list of limits for each acquired waveform (pass/fail conditions) to be verified automatically after each test and before starting the next one. The repetitive test sequence can be started and terminated by clicking the START and STOP buttons (see Fig. 2.3), respectively. After each test, the electrical waveforms acquired by the oscilloscope are stored including test index and time stamp and then analysed to evaluate the pass/fail condition. In case that one of the predefined limits (upper or lower limits) is violated, the short-circuit repetitive sequence will be stopped. An email is immediately sent to the user for communicating the type of violation. The flow chart of the test sequence can be observed in Fig. 2.4 [47].

2.1.3 Description of the dynamic test bench at ABB

Fig. 2.5 shows a picture of the dynamic substrate tester that has been used for performing non-destructive short-circuit tests on High-Voltage IGBTs. It consists of a high voltage power supply with a maximum voltage of 6500 V, which is connected to a bank of capacitors. Two IGBT power modules act as a circuit breaker, the busbar stray inductance can be modified manually up to a maximum of 1 μH. The device under test must be mounted on a substrate, since the fixture consists of a substrate press, which is filled with nitrogen during the test to provide electrical insulation. The tester offers some flexibility to adapt fixtures with different substrate geometries, being fully automated and easy to program. A Personal Computer (PC) serves as an interface between the LeCroy LT344 oscilloscope and the two gate driving units for the device under test and the series protection. The platform to program the short-circuit sequence and to analyse the data is based on the Laboratory Virtual Instrument Engineering Workbench, LabVIEW software. The oscilloscope acquires the electrical waveforms V_{GE}, V_{CE} and I_C by means of the measurement equipment listed in Table 2.3.

Figure 2.5: *Picture of the dynamic substrate test bench at ABB for performing short-circuit tests.*

Table 2.3: *Equipment list.*

Device	**Type**	Bandwidth (-3 dB)
Oscilloscope	LeCroy LT344	500 MHz
Current Probe	Pearson 4997 20 kA	20 MHz
HV Passive Probe	LeCroy PPE 20 kV	100 MHz
Differential Voltage Probe	Tektronix P5200	25 MHz

2.2 Short-Circuit Operation of Single-Chip IGBTs

In this section, the short-circuit behavior of single-chip IGBTs is studied by using the non-destructive tester shown in Fig. 2.2. In the following, it will be demonstrated that single-chip IGBTs evidence an instability mechanism occurring under short-circuit type 1, which in turn may lead to oscillations best seen in the gate voltage. The test method has been performed by increasing the short-circuit pulse width after each successful experiment in steps of 1 μs up to 10 μs (i..e, the short circuit duration quoted in the datasheet).

The short-circuit investigation has been conducted by using a combination of modern 3.3-kV IGBTs with different technologies, i.e., planar, trench and BIGT (Bi-mode Insulated Gate Transistor). Additionally, the testing conditions have been varied, such as the DC-link voltage from 200 V up to 1800 V, the case temperature from 25 °C up to 125 °C and the nominal gate voltage from 13 V up to 17 V.

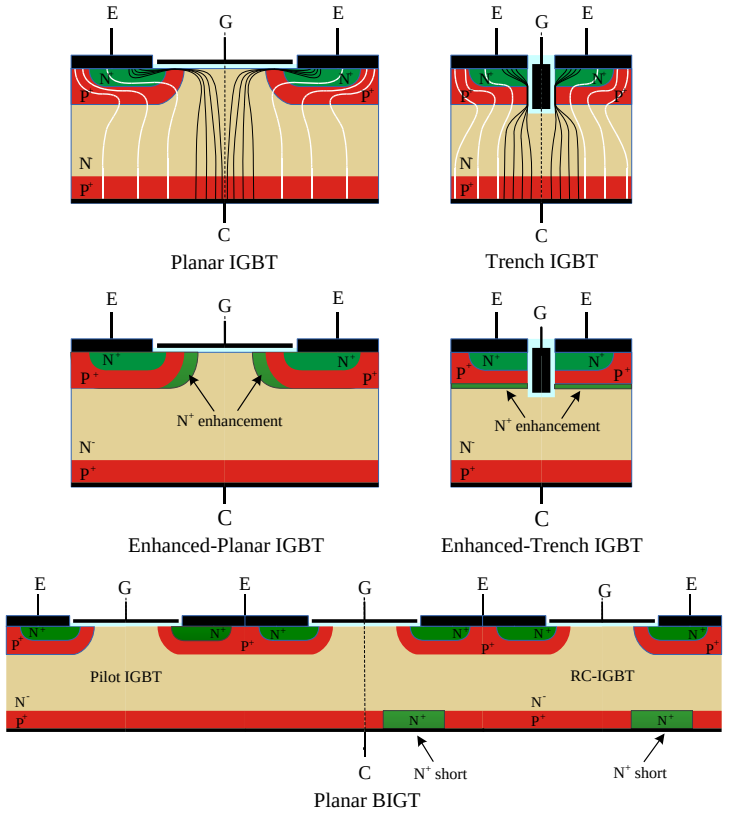

Figure 2.6: *Evolution of the IGBT cell design technology.*

2.2.1 Introduction to device technology

The gate voltage oscillations are investigated by testing different IGBT cell technologies, having the same nominal voltage of 3.3-kV. A brief introduction to the IGBT cell designs that have been tested is given, whose schematic cross section can be observed in Fig. 2.6. Throughout the IGBT evolution, the standard planar IGBT has been the first developed cell technology to be introduced into the market. However, as the planar IGBT devices rapidly approach their limits between conduction losses and turn-off losses, the trench design with its vertical MOS channel has emerged as a potential substitute to overcome the trade-off between on-state losses and turn-off losses [49]. Despite of this, the planar IGBT technology has not been totally forgotten thanks to its good cost-performance ratio; therefore IGBT designers continue working on the device

cell design to achieve similar benefits as the trench IGBT. As a consequence, the carrier enhancement technique began to gain importance, it particularly helped to boost the planar IGBT technology to obtain a similar performance as the trench cell design. The enhancement layer consist of implementing an additional n^+ layer at the emitter side to reduce the $V_{ce(sat)}$, without compromising the turn-off losses. The enhancement n-layer has nowadays been satisfactory implemented in both planar and trench IGBTs, as it is depicted in Fig. 2.6. For planar IGBTs, the best solution is to place the n-layer laterally near the edge of the p-well, to not sacrifice the blocking capability of the device and thus allowing for higher enhancement n-layer doping [50]. On the other hand, for the trench designs, the n-layer fully surrounds the p-region.

A new cell design concept is becoming dominant during the last years, that is the Reverse Conducting IGBT or Bi-mode Insulated Gate Transistor (BIGT), which integrates the IGBT and the free-wheeling diode by utilizing the same silicon chip for both operational modes [51]. In this way, the anti-parallel diode can be integrated in the IGBT cell design by introducing n^+ shorts at the collector side, as depicted in Fig, 2.6. The n^+ shorts act as the cathode for the internal free-wheeling diode. During the diode conduction mode, the p^+ collector regions are inactive and do not interfere with the diode performance. In contrast, the n^+ collector shorts strongly influence the IGBT

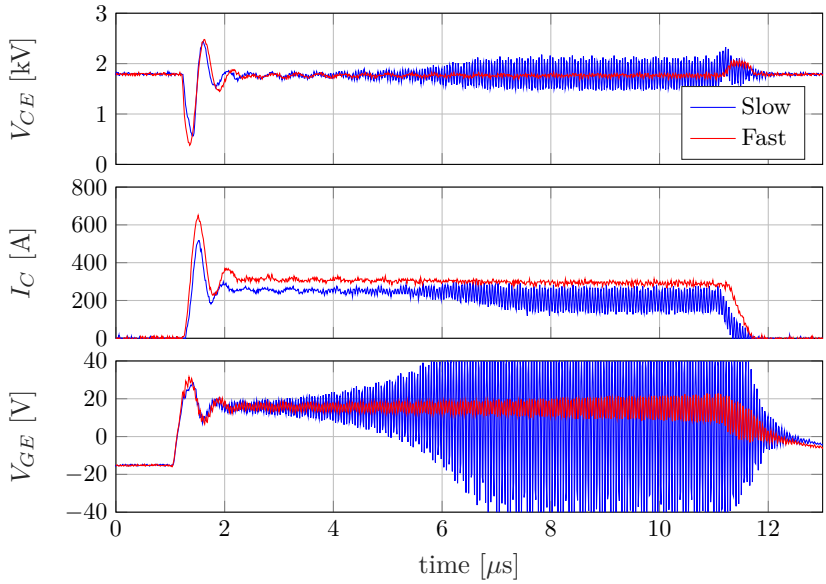

Figure 2.7: *Short-circuit of 3.3-kV SPT$^+$ planar IGBTs having different switching speeds. $R_{g,on} = 2.2\,\Omega$, $L_\sigma = 530\,nH$ and $T_{case} = 25\,^\circ C$.*

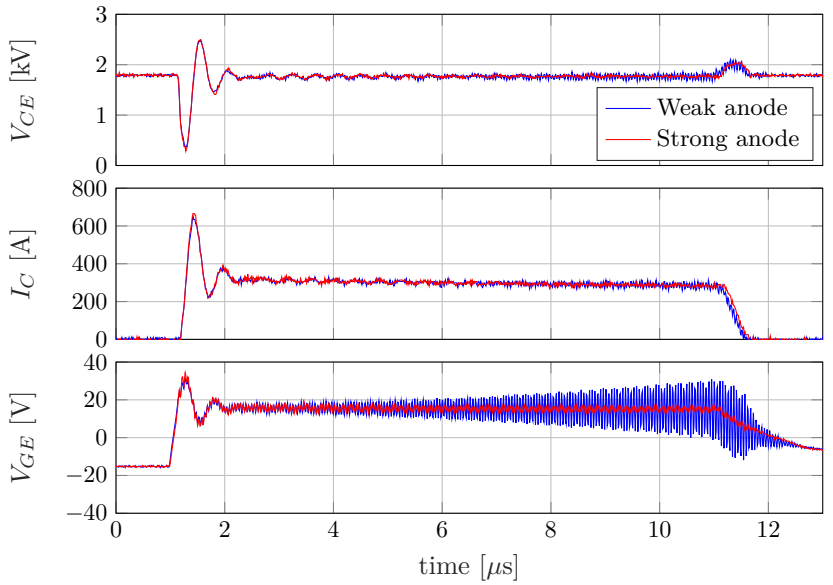

Figure 2.8: *Short-circuit of 3.3-kV SPT$^+$ planar IGBTs with different anode doses. $R_{g,on}$ = 2.2 Ω, L_σ = 530 nH and T_{case} = 25 °C.*

operation mode. The BIGT concept has been efficiently implemented for both planar and trench cell designs in [52].

2.2.2 Short-circuit assessment of 3.3-kV planar IGBT devices

The short-circuit performance of different 3.3-kV Enhanced-Planar IGBTs with Soft Punch Through (SPT) buffer are evaluated to understand which designs are more robust against short-circuit conditions. In the following, the positive sign accompanied to the SPT acronym means that the device has an enhancement n^+ layer.

The short-circuit waveforms in Fig. 2.7 compare two IGBTs whose cell design is the same; however, their switching speeds are different due to lifetime control adjustment. The waveforms show the short-circuit operation at a DC-link voltage of 1800 V for a short-circuit pulse of 10 μs, evidencing an unstable mechanism in the form of oscillations with a frequency of 20 MHz. The results reveal that the slowest IGBT is not an optimum design to achieve high short-circuit capability, since the amplitude of the gate-voltage oscillations are well above 40 V, higher than the maximum nominal voltage that can be applied to the gate according to the datasheet. In contrast, the fast IGBT exhibits a smaller oscillation amplitude, demonstrating a more robust short-circuit performance,

though oscillations are still present.

Furthermore, the IGBT short-circuit capability is assessed by adopting different anode designs, this means that the bipolar transistor gain α_{PNP}, which is an increasing function of the collector current I_C, will be modified as well. Fig. 2.8 shows the short-circuit capability of the 3.3-kV EP-IGBTs fabricated with two different emitter efficiencies, named as strong anode and weak anode. All design parameters except for the anode dose were the same for the two devices. As it can be seen, the oscillatory behavior is best seen with a weak anode design, that is an IGBT with smaller emitter efficiency. Because of lower emitter efficiency, a decrease in the hole current injection from the collector is expected, revealing its big impact on the short-circuit instability of the device. The benefit of employing an IGBT with a strong anode design is corroborated through the experiments; an explanation from the internal physics angle will be formulated and supported by finite-element simulations in Chapter 5.

2.2.3 Short-circuit assessment of 3.3-kV trench IGBT devices

Fig. 2.9 shows the short-circuit performance of the 3.3-kV SPT$^+$ trench IGBT at a DC-link voltage of 1200 V and 1500 V, for a short-circuit pulse of 10 μs and case

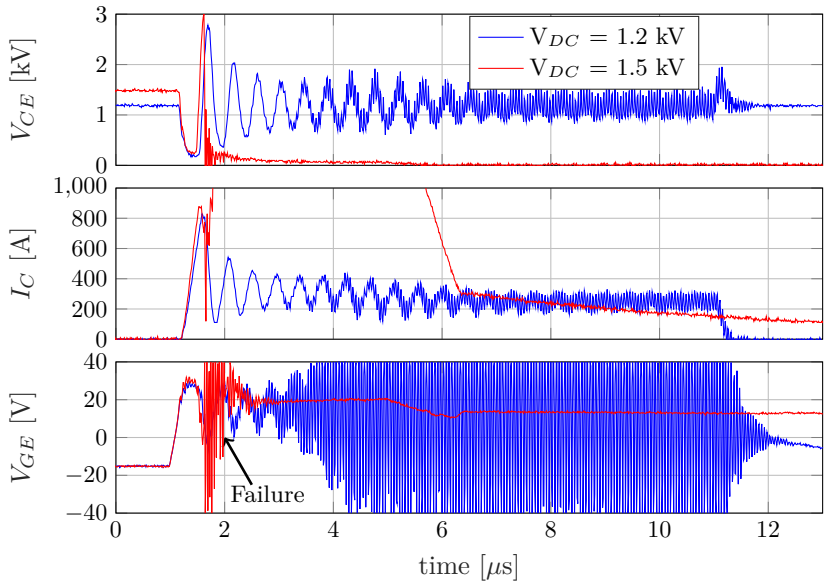

Figure 2.9: *Short-circuit capability of a 3.3-kV SPT$^+$ trench IGBT. $R_{g,on}$ = 2.2 Ω, L_σ = 530 nH and T_{case} = 25 °C.*

temperature of 25 °C. Once more, the short-circuit robustness is severely compromised by the occurrence of oscillations; in this case leading to the destruction of the IGBT. Two oscillation frequencies are observed; the high-frequency one, which is the main focus in this thesis, is in the same range as for the planar IGBTs, being 20 MHz. The low-frequency one, which is associated with the large inductance of the commutation loop, is about 2 MHz.

The trend observed here is that the considered trench IGBT has a negative effect in terms of short-circuit oscillations, when compared with the short-circuit performance of the planar IGBTs. The high gate voltage oscillations lead to uncontrolled short-circuit operations and thus to a catastrophic failure, as confirmed in Fig. 2.9. It is obvious that this instability is compromising the reliability of the IGBT and the whole assembly where it is supposed to be operated. In order to gain a better understanding of this failure mechanism, mixed-mode device simulations will be carried out later in Chapters 3 and 4 with a trench IGBT cell.

2.2.4 Short-circuit assessment of 3.3-kV trench and planar BIGT devices

The recently introduced BIGT device has been tested under short circuit for the two type of cell designs, i.e., planar and trench. The buffer design has been kept the same, which is based on the soft punch through concept. However, the collector p^+ dose has to be increased for obtaining a similar injection efficiency as the standard SPT^+ IGBTs. Fig. 2.10 shows the short-circuit capability of a 3.3-kV SPT^+ planar BIGT and Fig. 2.11 shows the short-circuit capability of a 3.3-kV SPT^+ trench BIGT. The experimental results indicate that the BIGT concept brings a remarkable improvement in short-circuit robustness over the standard IGBTs. For example, the planar and trench BIGTs do not show any sign of high-frequency oscillations between the voltage range from 200 V up to 1800 V. Additionally, while the trench BIGT has a fast turn-on transient resulting in low-frequency oscillations, it is still capable of withstanding the short-circuit event. Definitely, the trench BIGT design is a better solution when compared to the short-circuit operation of the standard trench IGBT in Fig. 2.9, where the trench IGBT fails at a DC-link voltage of 1500 V due to critical oscillations.

Therefore, the combination of higher p^+ collector doping together with the collector n^+ shorts provide an excess carrier concentration profile, which has an added advantage in eliminating the oscillatory behavior. The n^+ shorts at the collector constitute a sink for the electrons, which decreases the amount of excess electrons across the n-base of the device. This confirms that techniques at device level involving the optimization of the carrier concentration profile, helps in counteracting instabilities occurring during short circuit.

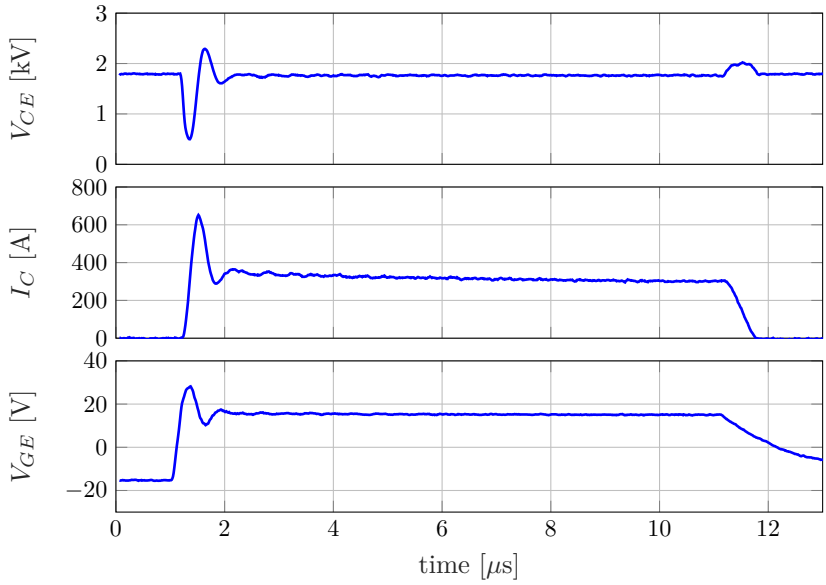

Figure 2.10: *Short-circuit capability of a 3.3-kV SPT$^+$ planar BIGT.*

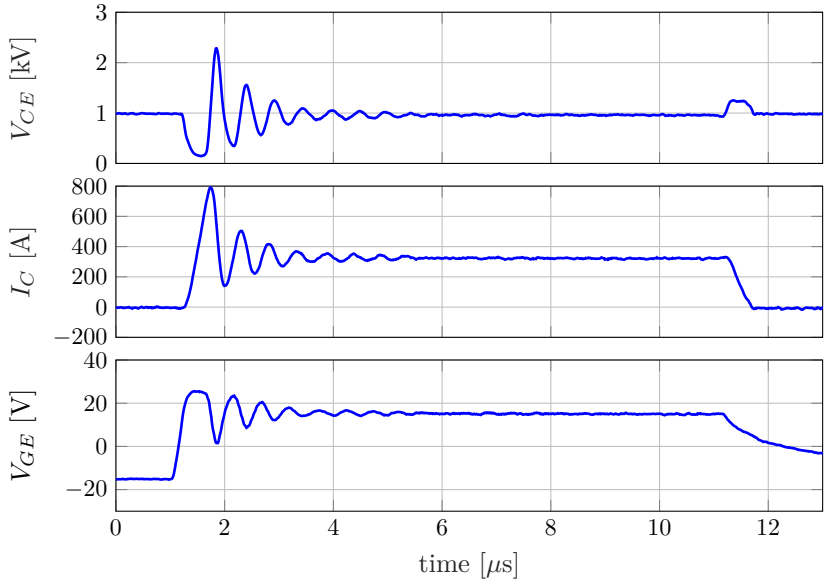

Figure 2.11: *Short-circuit capability of a 3.3-kV SPT$^+$ trench BIGT.*

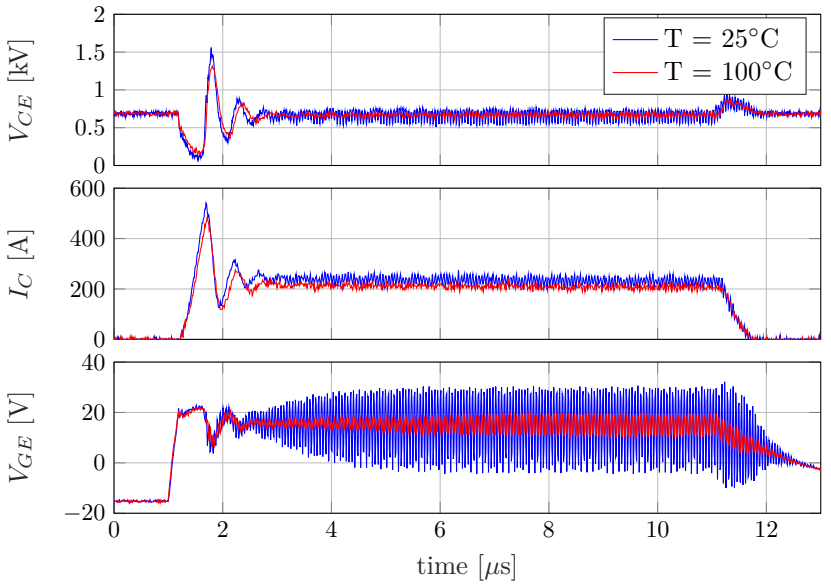

Figure 2.12: *Temperature effect on the short-circuit oscillations of a 3.3-kV SPT$^+$ planar IGBT.*

2.2.5 Influence of testing conditions on the oscillations

The driving factors for triggering the short-circuit oscillations have a strong dependency on the working conditions, such as the temperature, the applied DC-link voltage and the gate driving voltage, as briefly mentioned in [53]. Nevertheless, the evolution of the short-circuit oscillations when the IGBT is tested under different working conditions has not been provided, neither the type of IGBT technology. It is thus the aim of this section to show through experiments, the IGBT's oscillation dependence with the variation of the testing conditions. These parameters cause different mechanisms that affect the amount and position of the excess carrier concentration during short-circuit. Later in this thesis, it would be possible to compare the experimental results with the simulated ones, providing more information about how the testing conditions influence the carrier distribution profile of the IGBT.

2.2.5.1 Temperature effect

Fig. 2.12 shows the the short-circuit performance of a 3.3-kV Enhanced-Planar IGBT tested under two case temperatures of 25 °C and 100 °C. It is evident that higher temperatures help to mitigate the oscillation phenomenon, however, it is important to

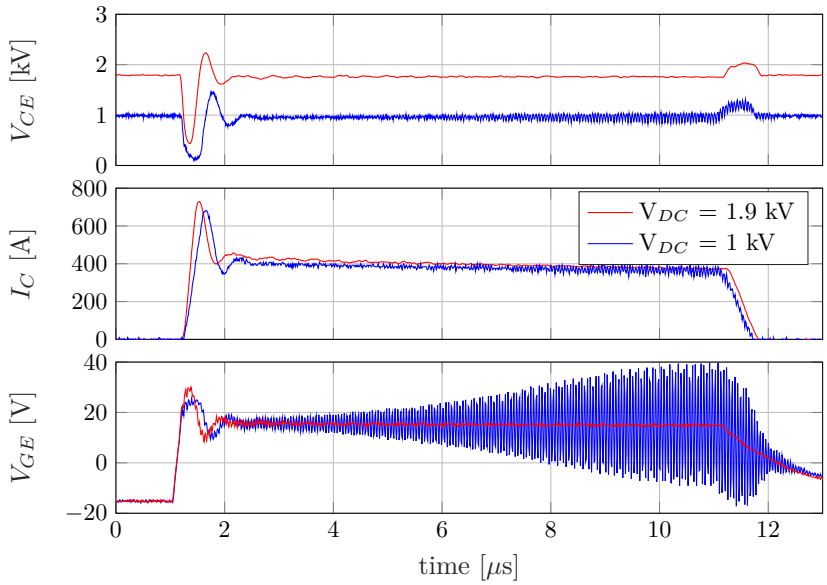

Figure 2.13: *DC-link voltage effect on the short-circuit oscillations of a 3.3-kV SPT$^+$ planar IGBT.*

note that the IGBT still exhibits oscillations. It has been noticed that the self-heating of a single IGBT during the short-circuit pulse is not as strong as the self-heating effect of multi-chip IGBT modules. This can be understood from the short-circuit current level, which does not decay with increasing short-circuit time, as a consequence of the inverse relationship between temperature and channel mobility. Therefore, in this case the oscillation amplitude is not attenuated with increasing short-circuit time, as it will be shown later for multi-chip IGBT modules.

2.2.5.2 DC-link voltage effect

Among the variables that can be modified with regard to the operating conditions, the applied DC-link voltage has been found to be one with the most remarkable impact on the short-circuit oscillation occurrence. Fig. 2.13 reports the short-circuit waveforms of the Enhanced-Planar IGBT chip rated at 3.3-kV, tested under two different voltages of 1 kV and 1.9 kV. It is clear that short-circuit oscillations occur at lower DC-link voltages, while the oscillations disappear at high DC-link voltages, near the nominal voltage of the device.

The results point out that the value of the collector voltage is dictating whether the IGBT will have an oscillatory characteristic or not. The operating collector voltage

mainly affects the electric field strength across the n-base of the IGBT. This, in turn, means that the root cause of the oscillations must be related with a critical electric field, that in case of being too weak will set the conditions to have oscillations.

2.2.5.3 Gate-voltage effect

To investigate any possible correlation between the short-circuit current level and the oscillation phenomenon, the single-chip IGBTs have also been tested at different gate-emitter voltages. The short circuit current and gate-emitter voltage are correlated by the output characteristics of the IGBT, basically through the threshold voltage and the transconductance of the MOS-channel.

Fig. 2.14 shows how the short-circuit waveforms develop with two different gate voltages of 15 V and 17 V, for the 3.3-kV Enhancement-Planar IGBT. The measurements indicate a clear disadvantage if the gate voltage is increased from 15 V up to 17 V, since oscillations appear for the latter case. Driving the IGBT with a higher gate voltage, means that the saturation current will also be higher. This implies that the current density plays a major role in the instability, compromising the short-circuit robustness.

The results point out that the gate-emitter voltage value is a key parameter that

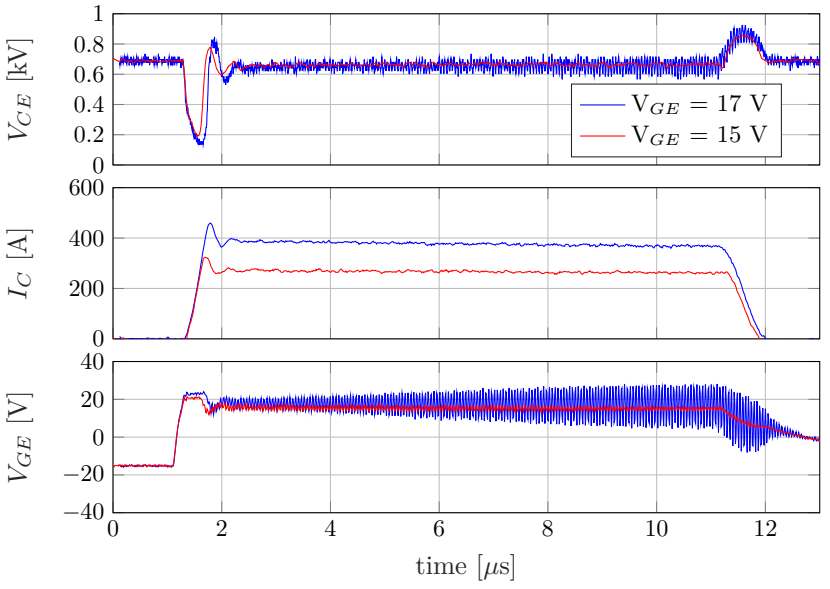

Figure 2.14: *Gate voltage effect on the short-circuit oscillations of a 3.3-kV SPT$^+$ planar IGBT.*

needs to be considered when dealing with oscillations. The applied gate-emitter voltage mainly affects the injection of electrons from the MOS-channel, it will be higher at V_{GE} = 17 V than at V_{GE} = 15 V. The downside of operating the device at a low gate-emitter voltage for mitigating the oscillations is that conduction losses will be increased. Once again, it seems that the excess carrier distribution profile of the IGBT is associated with the root cause of the oscillations. Further investigations with finite-element simulations will be presented in Chapter 3, demonstrating why oscillations are no longer observed at low V_{GE}.

2.3 Short-Circuit Operation of Multi-Chip IGBT Modules

In this section, the short-circuit performance of multi-chip IGBT modules is experimentally investigated by using the non-destructive tester shown in Fig. 2.2. In the following, it will be demonstrated that multi-chip IGBT modules also show oscillations under short-circuit conditions. The short-circuit test method was performed by increasing the short-circuit pulse width after each successful experiment in steps of 100 ns until the amplitude of the gate-voltage oscillations became larger than 30 V. This limit has been set to save the device from a possible gate-oxide breakdown. Different IGBT manufacturers, packaging designs and testing conditions such as temperature, DC-link voltage and gate-voltage will be varied in order to determine the IGBT's oscillation dependence.

2.3.1 Comparison among different manufacturers

One of the first concerns was to understand whether the oscillation mechanism is common to the IGBT design or particularly seen for a given manufacturer with a special device technology. To that end, three commercial 1.7-kV/ 1-kA IGBT power modules from three different manufacturers have been chosen arbitrary, named manufacturer A, B and C. The experimental results presented in the following have been published by the author of this Ph.D. thesis in [54]. The IGBT chip technology employed on the three manufacturers is based on the Trench Field-Stop design [55]. The picture of the IGBT power module is shown in Fig. 2.15 together with its circuit schematic. The IGBT module has a half-bridge configuration and it consists of 6 sections in parallel to achieve the rated 1 kA current capability. Each section contains two IGBT chips and two free-wheeling diodes for the upper and lower arms. To perform the short-circuit type 1, the gate terminal of the upper-arm IGBTs has been connected with a gate driver from Concept and the lower-arm IGBTs have been shorted.

Fig. 2.16 shows the short-circuit waveforms for manufacturer A and B, in which the gate voltage oscillates as soon as the IGBT enters the de-saturation region [54]. The

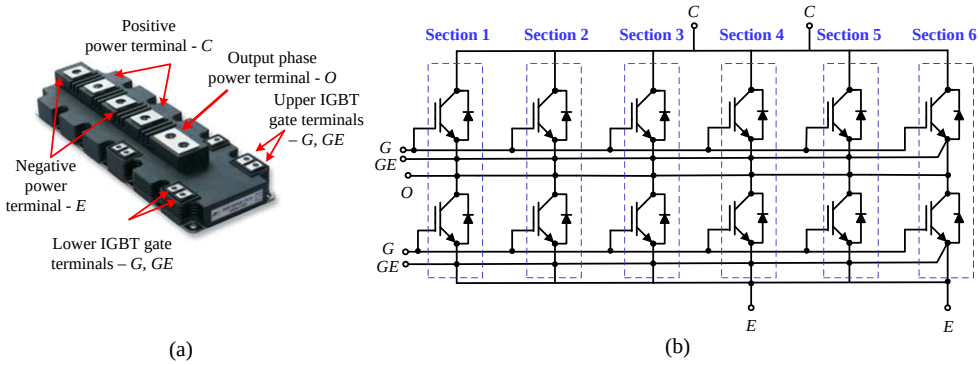

Figure 2.15: *The 1.7-kV/ 1-kA IGBT power module investigated to compare different manufacturer's short-circuit performance: (a) packaging geometry and terminals, (b) the half-bridge internal structure [47].*

gate-voltage oscillation amplitude reaches in a few microseconds 25 V for manufacturer A. On the other hand, the gate voltage oscillation amplitude for manufacturer B is slightly smaller, i.e., 15.2 V, for the same DC-link voltage and short-circuit pulse width as manufacturer A. Both IGBT power modules show similar oscillation frequency, about 20 MHz. As it can be seen in Fig. 2.16, the shape is not sinusoidal but a composition of different frequencies in the MHz range, probably because several of the 6-paralleled IGBT chips are oscillating.

Fig. 2.17a shows the short-circuit waveforms when the IGBT power module from manufacturer C is tested under the same conditions as manufacturers A and B. The oscillation phenomenon is no longer observed. Higher DC-link voltages are applied ranging from 400 V up to 900V. The short-circuit waveforms at 900 V DC-link voltage can be seen in Fig. 2.17b. Nevertheless, there is no evidence of unstable operation [54]. The outcome of these experiments demonstrate that manufacturer C has a higher short-circuit robustness. The downside is that the IGBT power module shows slower switching speed as a result of increased gate internal resistances. This leads to higher energy losses in contrast with manufacturers A and B.

2.3.2 Influence of testing conditions on the oscillations

Previously, it has been demonstrated that the short-circuit operation of single-chip IGBT modules has a strong dependency on the working conditions. The combination of low collector-emitter voltage V_{CE}, high gate-emitter voltage V_{GE} and low temperature has been proven to be adverse for the short-circuit robustness of the IGBT, since gate oscillations are typically seen. In order to demonstrate that multi-chip IGBT power modules exhibit a similar trend, experimental tests varying the same operating condi-

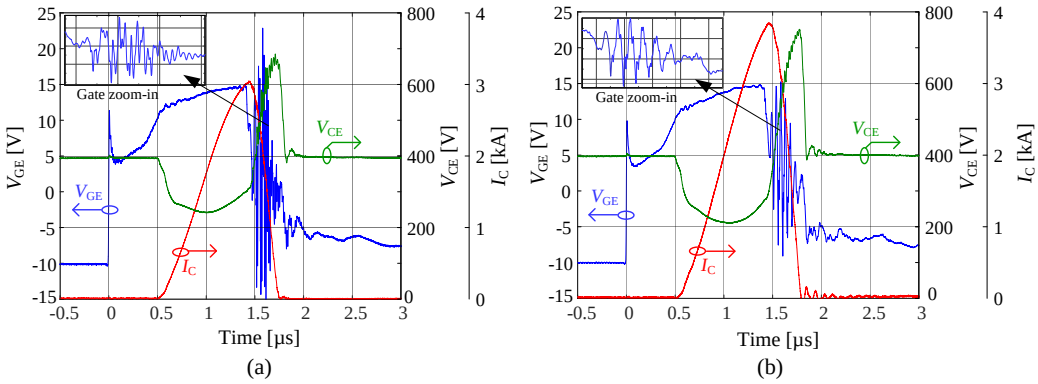

Figure 2.16: *Short-circuit oscillation phenomena observed in the 1.7-kV/ 1-kA IGBT power module: (a) manufacturer A, and (b) manufacturer B. Testing conditions: V_{CE} = 400 V; V_{GE}= 15V; T = 25 °C [54].*

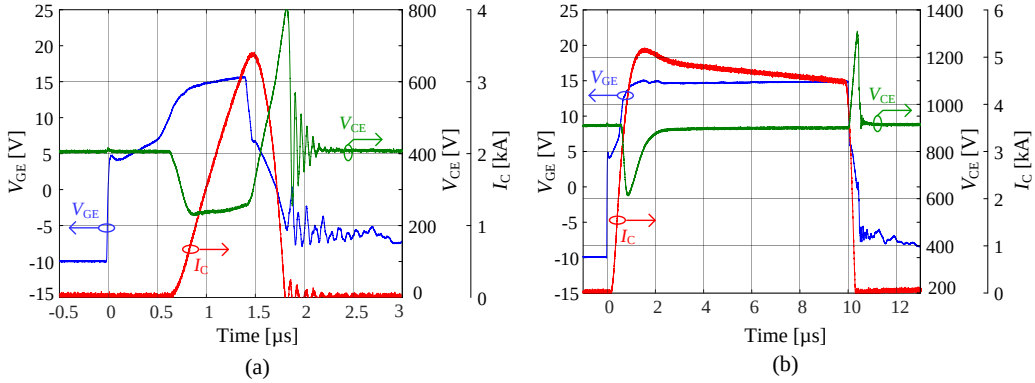

Figure 2.17: *Short-circuit test of a 1.7-kV/ 1-kA IGBT power module from manufacturer C: (a) 400 V/ 1.4 µs , and (b) 900 V/ 10 µs. Testing conditions: V_{GE}= 15V; T = 25 °C [54].*

tions will be performed.

2.3.2.1 Temperature effect

The 1.7-kV/ 1-kA IGBT power module from manufacturer B has been tested under short-circuit type 1, as a function of different temperature conditions. Fig. 2.18 shows the comparison of the short-circuit waveforms under two starting case temperatures

of 50°C and 80°C [13]. Two effects can be observed here, the first one is related to the gate voltage oscillation characteristic, which converges or diverges repeatedly but finally becomes damped with increasing time. It can be noticed that the self-heating of the IGBT during the short-circuit pulse has a great influence on the oscillations, since the amplification mechanism is mitigated. One of the reasons could be related with the short-circuit current evolution during the short-circuit pulse. The current value decreases with increased device temperature due to lower channel mobility; thus, it can be inferred that the oscillation phenomenon is strongly dependent on the current density inside the IGBT.

The second effect is related to the short-circuit starting temperature. The IGBT power module tested at $50°C$ clearly shows higher oscillation amplitude in contrast with the same IGBT power module tested at $80°C$. It can be seen in Fig. 2.18, that the short-circuit current peak is lower at higher temperatures, confirming that the short-circuit current level is taking part as a driving factor. Indeed, the oscillations start

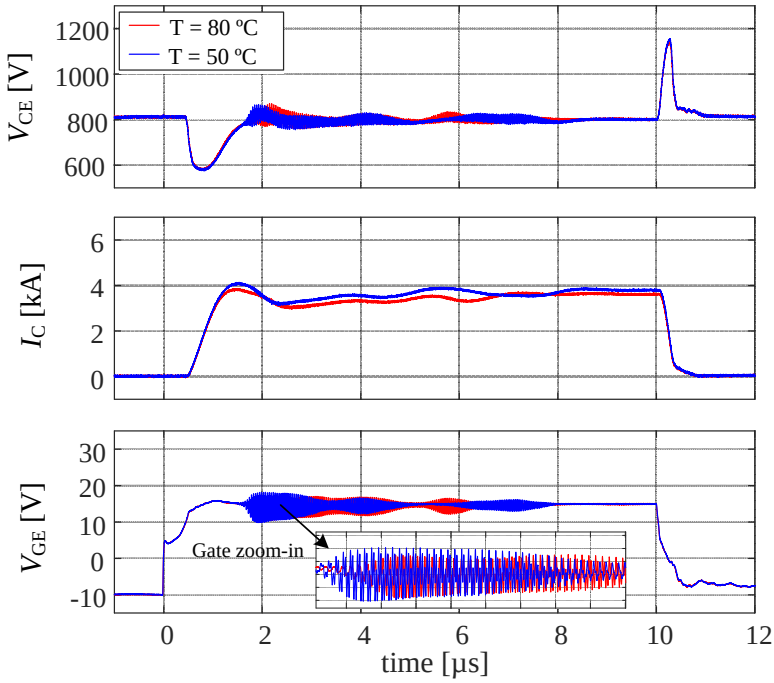

Figure 2.18: *Temperature effect on the short-circuit oscillations of the 1.7-kV/ 1-kA IGBT module from manufacturer B. Testing conditions:* V_{GE} *= 15V;* V_{CE} *= 800V.*

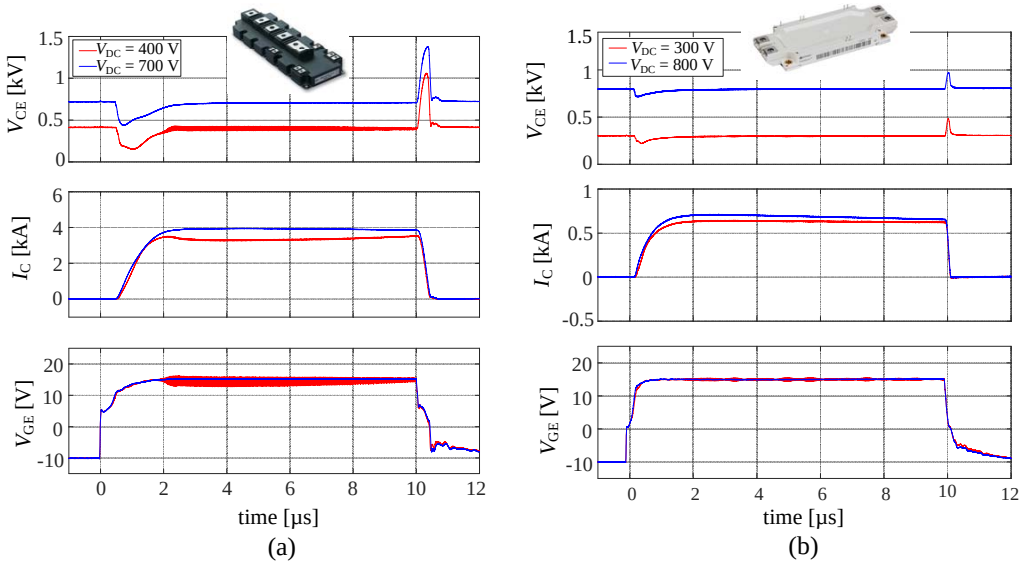

Figure 2.19: *Influence of the applied DC-link voltage on the short-circuit oscillation occurrence: (a) the 1.7-kV/ 1-kA IGBT module (lower arm tested) and (b) the 1.7-kV/ 150 A IGBT power module. Testing conditions: V_{GE}= 15V; T = 25 °C [13].*

earlier with higher short-circuit currents.

From the experimental results, it can be understood that higher temperatures, hence lower collector currents, have a remarkable effect on the short-circuit oscillatory characteristic, helping to attenuate the oscillation. The role of the temperature will be studied in detail by means of TCAD device simulations.

2.3.2.2 DC-link voltage effect

For single-chip IGBTs, it has been demonstrated that the low applied DC-link voltage is the major enabler for triggering the short-circuit oscillations. Once again, a similar behavior is recognized when a multi-chip IGBT power module is tested under short circuit.

Fig. 2.19a shows the short-circuit waveforms of the 1.7-kV/ 1-kA IGBT power module tested under two different voltages of 400 V and 700 V. It is clear that the short-circuit oscillations occur at lower DC-link voltages, while a clean short-circuit characteristic is observed at higher DC-link voltages. A similar behaviour is recognized when another type of IGBT power module, rated at 1.7-kV/ 150-A, is tested at DC-link voltages ranging from 200 V up to 800 V. It can be understood from Fig. 2.19b that

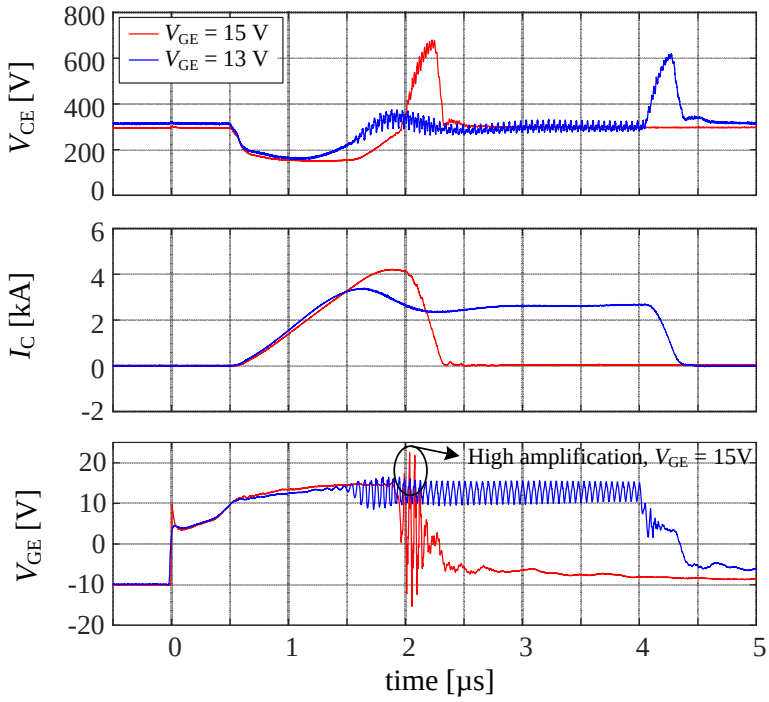

Figure 2.20: *Gate voltage dependence on the short-circuit oscillations of the 1.7-kV/ 1-kA IGBT module from manufacturer B. Testing conditions: V_{CE}= 300V; T = 25° C [13].*

the oscillations occur only for low DC-link voltages. This dependency indicates that the electric field distribution inside of the IGBT is a keystone for understanding the short-circuit failure mechanism, as it will be shown later in Chapter 4.

2.3.2.3 Gate voltage effect

To the same extent, the gate voltage has been modified in order to investigate whether the same correlation as for single-chip IGBTs exists for multi-chip IGBT power modules. Fig. 2.20 shows the advantage of lowering the gate driving voltage from 15 V to 13 V, in agreement with the results from single-chip IGBTs. While the gate oscillations are not very critical for a gate voltage of 13 V, the results at V_{GE} = 15 V compromise the short-circuit robustness of the device. In Fig. 2.20, it is highlighted that a higher amplification is observed for V_{GE} = 15 V, which is above the maximum

positive gate voltage quoted in the datasheet.

2.3.3 Layout influence on the oscillation phenomenon

In practical applications, many failures of power semiconductor devices are caused by parasitic effects [53]. Therefore, it is important that the layout inside of the power module has a low stray inductance, especially in the commutation path. One of the motivations for minimizing the commutation stray inductance is to guarantee small voltage overshoots during the IGBT turn-off, whose amplitude must be below the maximum voltage rating of the device. On the other hand, reducing the inductance is not always desirable, especially in the gate loop. For instance, a reduction of the emitter inductance leads to fast turn-on/turn-off transients that could result in loss of synchronized switching among the IGBT chips connected in parallel.

In short-circuit conditions, the stray inductance influence can even be more critical for the device operation. For instance, the work presented in [13, 54], has demonstrated that the IGBT short-circuit robustness is compromised due to a weak performance in terms of critical oscillations. To better understand the layout influence on the short-circuit oscillations, the 1.7-kV/ 1-kA IGBT module has been modified in a way that two sections and one section have been tested instead of the six parallel sections, forming part of the whole module. The housing package and the layout internal arrangement of the IGBT power module investigated in this section is depicted in Fig. 2.15. The aim is to investigate whether the internal package layout is playing any role on the short-circuit instability. Additionally, three different DCBs (Direct Copper Bonded) substrates with variations on the stray inductance distribution have also been tested under short-circuit, to demonstrate its dependence on the oscillation behavior.

2.3.3.1 Short-circuit assessment of a modified version of the 1.7-kV/ 1-kA IGBT module

Fig. 2.21a shows the experimental short-circuit waveforms of two parallel sections of the 1.7-kV/ 1-kA IGBT module. The gate measuring points can be observed in Fig. 2.22, and the comparison between section 1 and section 2 gate voltage measurements can be observed in Fig. 2.21c. The amplitude of the oscillations were of the same level between the two chips, but each chip oscillated in opposite phases, with similar frequency range as the original module having six sections in parallel - about 20 MHz [54]. A clear indication that lower DC-link voltages drive the IGBT easily into the unstable operation is once more demonstrated. Further experiments on the two parallel sections, as well as one single section can be found in [54], indicating that oscillations do not occur at higher DC-link, for instance for voltages raging from 400 V up to 900 V.

On the other hand, Fig. 2.21b shows the short-circuit results of one section, having a single-chip IGBT, which has been tested at the same conditions as before. The oscillations were not observed on the gate voltage. Two possibilities can be derived here:

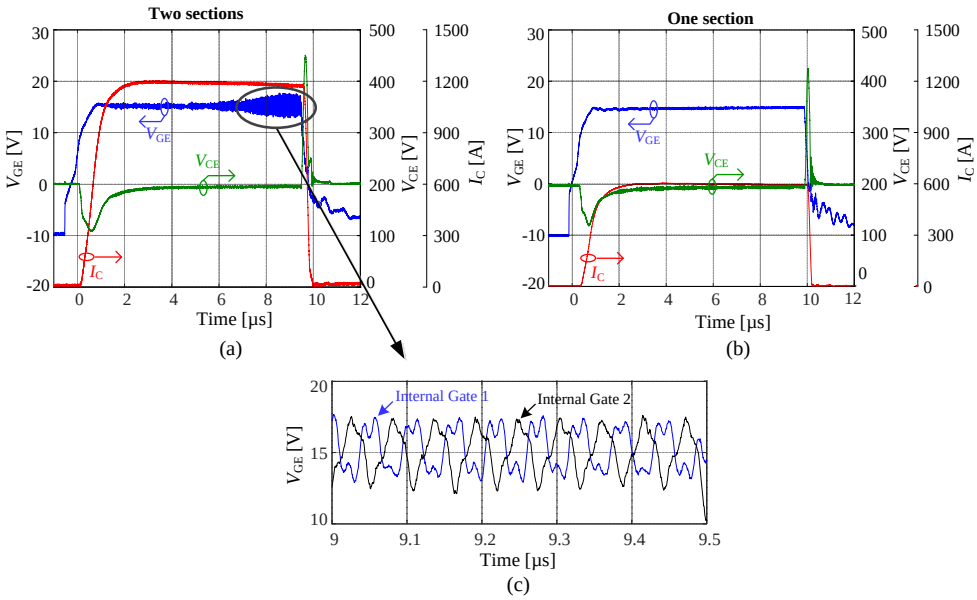

Figure 2.21: *Layout influence on the oscillation behaviour with a modified version of the 1.7-kV/ 1-kA IGBT module: (a) two sections in parallel, (b) one single section, and (c) gate voltage zoom-in. Testing conditions: V_{DC} = 200 V, T = 25°C [54].*

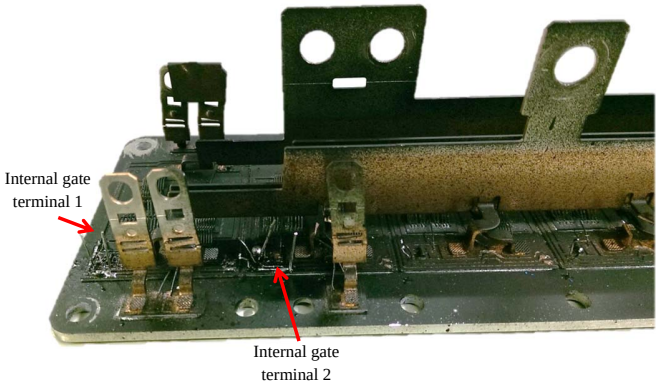

Figure 2.22: *Picture of the 1.7-kV/ 1-kA open module showing the gate terminal measuring points for the two DCB sections.*

(a) the layout has been correctly optimized to mitigate the short-circuit instability, and (b) the oscillation behavior is more prone to occur for paralleled IGBTs than single IGBTs. However, this latter hypothesis has to be rejected, as the experimental tests on single-chip IGBTs have proved that oscillations are inherent to the device itself.

2.3.3.2 DCB substrate layout variations

In order to study the effects of the stray inductance variations, it is necessary to apply different layout solutions to understand which parameters must be minimized. For simplicity, a single DCB substrate of the 1.7-kV/ 1-kA IGBT power module will be studied. Each DCB substrate represents a half-bridge configuration, having two IGBTs and two anti-parallel diodes (upper-arm an lower-arm), which are switched alternately. In multi-chip IGBT modules, the emitter inductance L_e typically shares fractions between

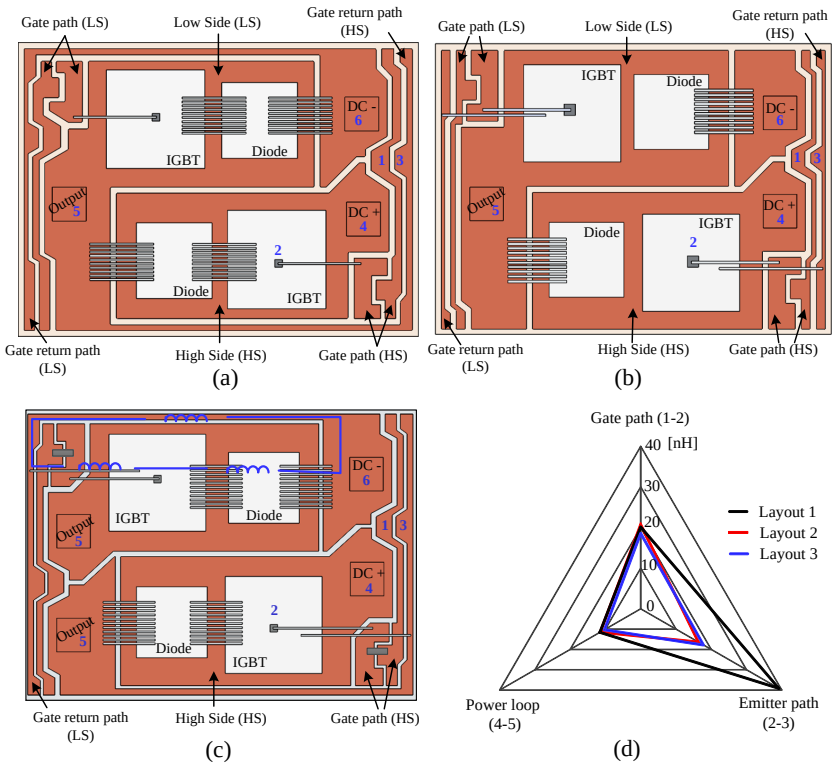

Figure 2.23: *Comparison among the three DCB substrates: (a) Layout 1, (b) Layout 2, (c) Layout 3, and (d) the extracted stray inductance by Q3D at 100 kHz [56].*

the gate and power loop, to guarantee balanced current sharing among the paralleled DCBs. The effect under normal operation is that the IGBT switching speed can be slowed down preventing over-current and over-voltage transients at the expense of increased power losses. In contrast, the influence of L_e on the oscillation phenomenon is not clear. On this basis, three different DCB layouts have been proposed, with particular focus on the optimization of the emitter inductance value for higher short-circuit robustness.

The selected designs are illustrated in Fig. 2.23 [56]. The geometries have been drawn in SolidWorks and then exported to Q3D for extracting the AC self and mutual inductances. The design target has been focused first, on the reduction of the emitter inductance. Layout 1 corresponds with the industry standard package of the 1.7-kV/ 1-kA IGBT power module. In this case, the emitter inductance L_e shares a common path between the gate loop and the power loop. For example, the gate current and the collector current both flow through the emitter bond wires and then split their paths to the gate-return DCB trace or to the power terminal, respectively. On the other hand, Layout 2 aims at decoupling the gate loop from the power loop with an additional bond wire from the IGBT emitter to the gate trace. In this way, a smaller emitter inductance is achieved. An hybrid design could be Layout 3, in case that excessive over-voltage or

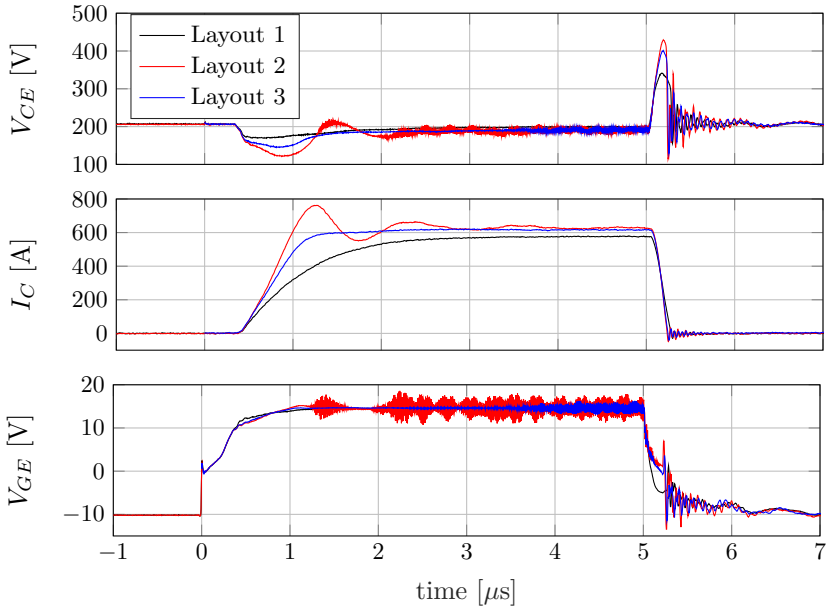

Figure 2.24: *Emitter stray inductance influence on the short-circuit oscillations.*

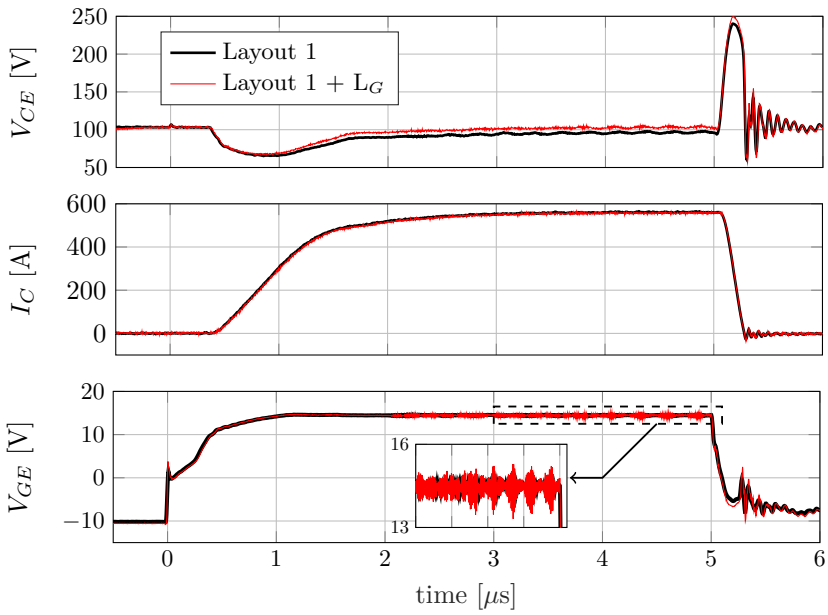

Figure 2.25: *Gate stray inductance influence on the short-circuit oscillations.*

too fast commutations are not suitable for a given application. Layout 3 has the same geometry as Layout 1; the only difference is the extra bond wire from the emitter IGBT to the gate trace forming a triangle of inductances (see Fig. 2.23c).

Fig. 2.23d compares the extracted stray inductances from the three proposed layouts by using AnSYS Q3D extractor. According to Fig. 2.23, the points 1-2 and 2-3 are the gate and gate-emitter paths of the high side IGBT. The points 4-5 represent the main power path. Since the high-side IGBT will be tested under short-circuit, only the stray inductance calculation of the high side is given. From the simulated results, it can be concluded that the emitter inductance has been effectively minimized, therefore the effect of L_e on the short-circuit performance can be experimentally demonstrated.

Fig. 2.24 exemplifies the experimental short-circuit results performed on the high-side IGBTs with the three DCB substrate designs. A higher commutating di/dt is noticed in Fig. 2.24 for Layout 2, in contrast with Layout 1, having the largest emitter inductance. The influence of a small emitter inductance gives rise to an overshoot of the collector current I_C together with a larger collector voltage drop. The combination of low collector-emitter voltage and high collector current seems to be the recipe for the occurrence of the gate oscillations, which also comes with a higher amplification.

It must be noted that the short-circuit experimental results in Fig. 2.24 show that

Layout 1 has no evidence of critical oscillations and one may think that oscillations will not be triggered when the whole IGBT power module is tested. Nevertheless, the original IGBT power module has uneven gate inductance distribution. For instance, section 1 is the closest to the external gate terminal (i.e., low gate inductance) and section 6 is the furthest (i.e., large gate inductance). With the goal of understanding the influence of the gate inductance L_g, Layout 1 is tested with a larger gate wiring cable. The result is obvious in Fig. 2.25, higher gate inductance designs lead to the the occurrence of oscillations.

2.4 Conclusion of this chapter

Instabilities in single-chip IGBTs and multi-chip IGBT power modules have been observed when they are exposed to a short-circuit type 1 event. It has been found that gate voltage oscillations can be observed for both planar and trench cell designs, however, they disappear when the diode function is introduced on both IGBT cell designs to fabricate a reverse-conducting IGBT, named here as the Bimode Insulated Gate Transistor (BIGT). Additionally, it has been demonstrated that there are some conditions playing a key role, either as a triggering condition or as a parameter involved in the instability:

- **Internal layout.** The inductance involving the commutation loop and the gate loop worsens the stability of the device. On the contrary and differently from the expected, a relatively large emitter inductance helps to slow down the switching transient in order to achieve a clean short-circuit waveform.
- **Temperature.** The thermal evolution during the short-circuit condition significantly contributes to the stability of the device. Also, it has been proven that at high temperatures, the amplification behavior is minimized.
- **DC-link voltage**. Gate oscillations are best seen at low DC-link voltages, in most of the cases, oscillations disappear at high DC-link voltages. This reveals that the electric field strength inside of the IGBT at low collector voltages plays a key role in the instability mechanism.
- **Short-circuit current.** The oscillation sets in as a function of the short-circuit current density. The results indicate that the IGBT exhibits oscillations when the applied gate-emitter voltage is increased, which is associated with high current densities. This, in turn, means that the MOS-channel is injecting a larger amount of electrons.
- **Carrier profile distribution.** The excess carriers inside of the IGBT play an essential role on the oscillation instability mechanism. This has been confirmed

with experiments on IGBTs having high-injection-efficiency emitters and BIGTs. The effect of the excess carrier concentration profile has been modified in a way that the short-circuit oscillations have been mitigated.

Chapter 3

TCAD Sensitivity Study of Short Circuit Oscillations in IGBTs

In this chapter, the short-circuit oscillations observed in modern IGBTs will be reproduced by means of mixed-mode device simulations. A 3.3-kV planar IGBT half-cell is employed to show how the IGBT behaves in terms of electric field variations and charge distribution, under different operating conditions and layouts. The trends observed here are needed later, in order to explain the root cause of the short-circuit instability.

3.1 IGBT Designs for 2-D Device Simulations

The simulations in this chapter have been performed using a 3.3-kV SPT (Soft-Punch Through) planar IGBT model [50]. According to the experimental results, both trench and planar cells present oscillations during their short-circuit operation. Firstly, we have focused on carrying a sensitivity analysis on the oscillating behaviour's dependence for the planar IGBT cell, mainly because of two reasons: (a) compromise between computation time and accuracy, and (b) the planar concept makes easier the understanding of the electric field variations and carrier profile distributions. Nevertheless, a brief introduction to the 3.3-kV trench IGBT model is also given here, since simulations with this model will be shown in Chapter 4.

Fig. 3.1 shows the structure of the 3.3-kV planar and trench IGBT cells, which have been calibrated to fit the real characteristics of the tested devices. The origin of the structure is located in the upper left corner, and therefore, the vertical and horizontal cuts will be done with respect to this origin. The trench IGBT cell has been

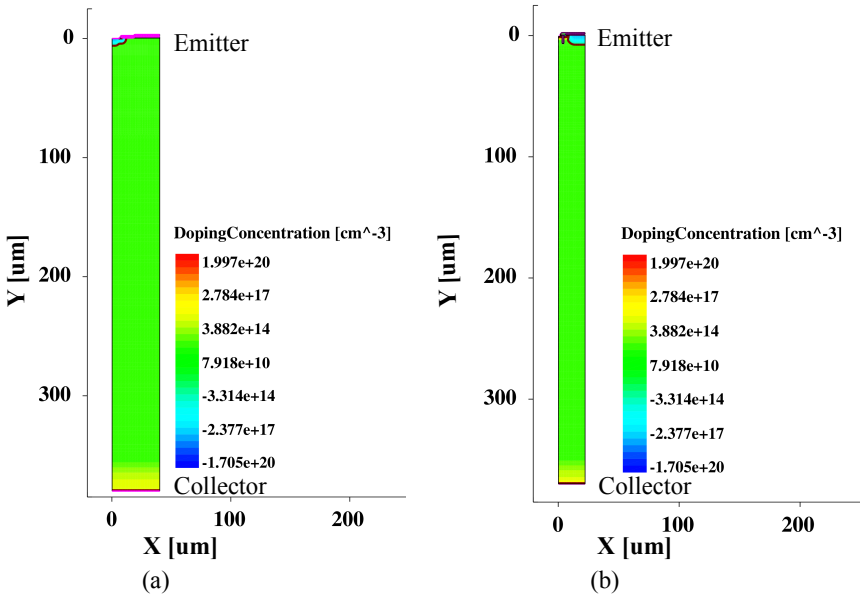

Figure 3.1: *The 3.3-kV IGBT half-cells used for the simulations: (a) the Soft-Punch Through (SPT) planar IGBT and (b) the Enhanced-Trench (ET) IGBT.*

implemented with the n-enhancement layer concept, for reducing the on-state losses without compromising the turn-off losses. Additionally, a lightly doped p-well region is adopted in order to reduce the effective input capacitance and optimize the region between active cells [57].

3.2 The Current-Voltage Characteristic of the IGBT

The simulated output characteristic of the 3.3-kV planar and trench IGBTs with a gate voltage of 15 V is illustrated in Figs. 3.2a and 3.2b, respectively. The graph shows the total current together with the ratio of the electron and hole currents. This ratio is of particular importance because it gives the value of the bipolar gain of the IGBT (J_h/J_e). The bipolar gain for the planar and trench IGBTs is 0.6 and 0.7, respectively. As observed in Figs. 3.2a and 3.2b, the saturation current increases with increasing collector-emitter voltages, mainly caused by the bipolar gain increase due to a deeper field penetration into the buffer with increasing collector-emitter voltages.

The output characteristic of an IGBT has two well-distinguished operation regions, the on-state or saturation region region, where the IGBT normally operates, and the

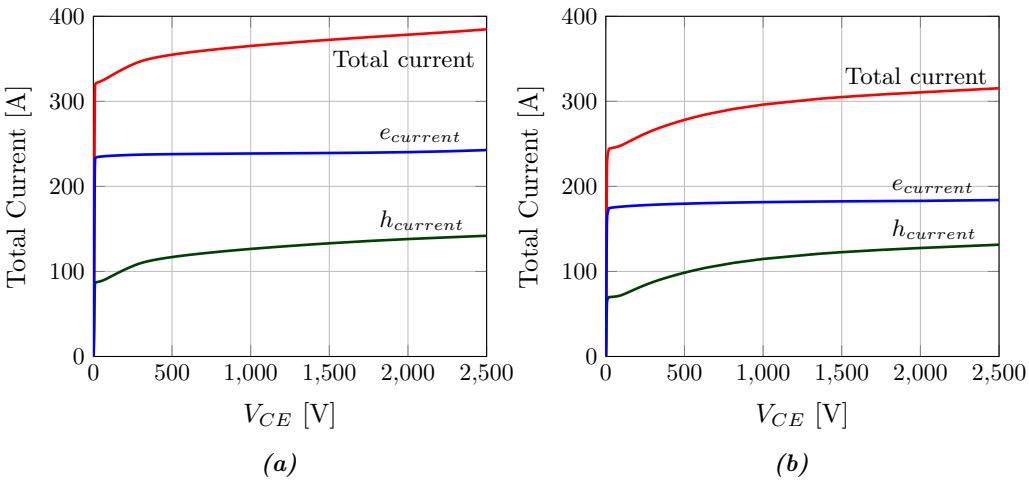

Figure 3.2: *The I-V characteristic at V_{GE} = 15 V together with the electron and hole currents: (a) the SPT planar IGBT and (b) the ET-IGBT.*

active transistor or desaturation region, where the IGBT operates under a short-circuit fault [11]. From the point of view of understanding the charge distribution and the electric field of the IGBT under a short-circuit event, the planar IGBT is evaluated in the active transistor region at different collector voltages of 1000 V, 1500 V, 2000 V and 2500 V. Fig. 3.3 shows the 2-D effects on the electron density at depths lower than 100 μm, together with a vertical cut along the maximum current density at x = 15 μm, illustrating the electric field and electron velocity. Two mechanisms are worth to be pointed out: (a) the injected carriers strongly dominate over the electric field shape in the n-base, and therefore the IGBT exhibits a rotated electric field, whose peak is located at the collector side. This happens because the effective charge N_{eff} becomes negative, and (b) the electron density and thus the current is not homogeneously distributed at the surface of the IGBT, the primary cause for this effect is the weak carrier storage effect between adjacent cells. It is worth to mention that the carrier storage effect becomes weaker with increasing V_{CE}, and thus, the electron density flow is narrower at higher V_{CE}, as it can be observed in Fig. 3.3. One of the reasons for the asymmetrical carrier distribution can be found by looking at the electron velocity quantity. For relatively low collector voltages, such as 1000 V and 1500 V, the electron velocity is proportional to the electric field. This relationship gives rise to low electron velocities at the emitter side and high electron velocities at the collector side (see Fig. 3.3). When a higher collector-emitter voltage is applied, such as 2500 V, the electron velocity becomes close to saturation and more homogeneous across the vertical direction of the IGBT, coinciding with a weaker carrier storage effect as the electron velocity increases

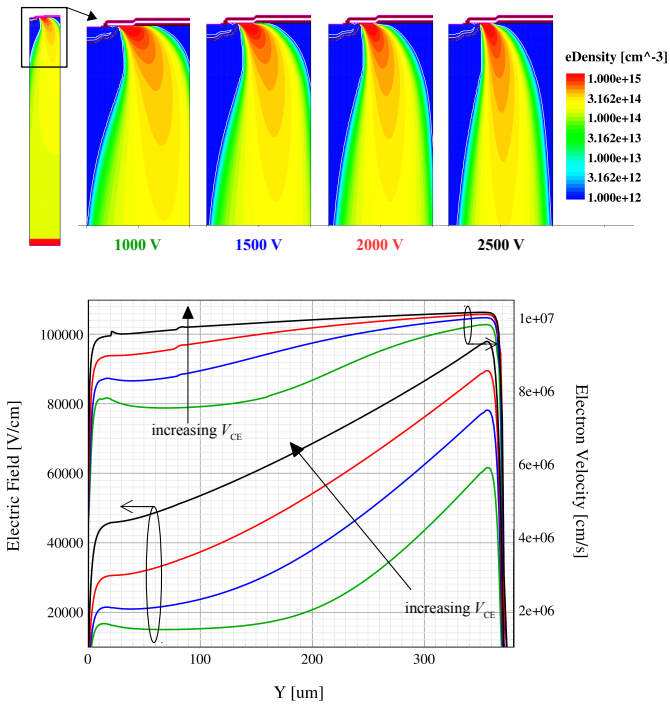

Figure 3.3: *The 2-D electron density distribution of the planar IGBT together with a vertical cut at $x = 15$ μm illustrating the electric field and electron velocity evolutions with increasing collector voltage according to Fig. 3.2a.*

in the emitter side.

For the considered trench IGBT, a similar approach has been followed in order to illustrate the behavior of the device in the active transistor region. The trench IGBT has been evaluated at different collector voltages of 350 V, 500 V, 1000 V and 1500 V. Fig. 3.4 shows the 2-D effects on the electron density at depths lower than 100 μm, together with a cut along the region where the current density is the highest (x = 1 μm). It is worth noting that the considered trench IGBT differs from the conventional planar IGBT in the carrier profile at the emitter side, which is higher for trench cells. This is beneficial to achieve a symmetrical carrier distribution along the n-base. Yet, the carrier storage effect at the emitter is still evident for the considered trench IGBT, which varies according to the applied collector voltage. With increasing V_{CE}, the electron flow is narrower, similarly to the planar IGBT performance. On the other hand, the trench IGBT does not suffer from the drawbacks coming from the strong negative effective

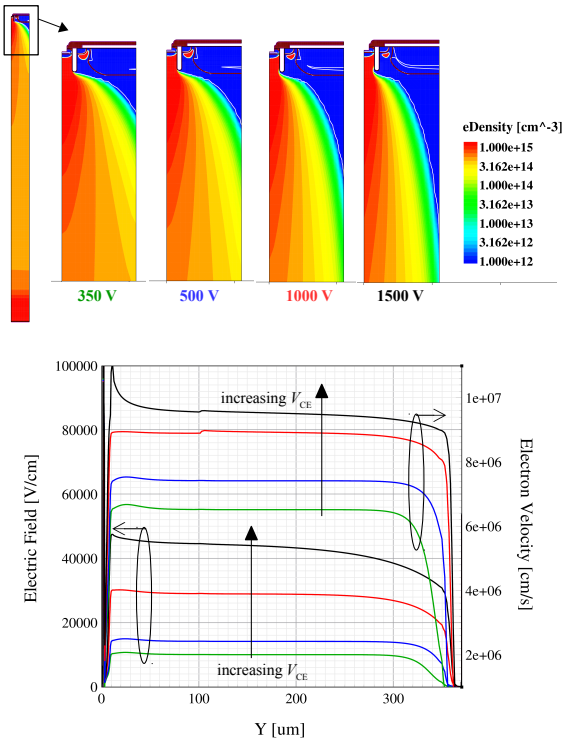

Figure 3.4: *The 2-D electron density distribution of the trench IGBT together with a vertical cut at $x = 1$ µm illustrating the electric field and electron velocity evolutions with increasing collector voltage according to Fig. 3.2b.*

charge causing the electric field to rotate. Instead, the trench IGBT exhibits the well-known triangular electric field shape. In this case, the electron velocity gradually varies as a function of the collector voltage, as discussed before, but it is more homogeneous across the n-base of the trench IGBT, i.e., it has a flat characteristic.

3.3 The Turn-on Process under Normal and Short-Circuit Operation

The turn-on process of the IGBT under normal and short-circuit conditions will be compared and analysed in order to highlight the main differences. The studied fault is a short circuit type 1 or Hard Switching Fault (HSF), which happens at the DUT's turn-

on. The IGBT turn on is evaluated taking into consideration the circuit and the internal device physics. To that end, the 3.3-kV planar IGBT cell is implemented in TCAD to perform mixed-mode simulations. Fig. 3.5 shows the simulated electrical waveforms of the turn-on process, together with the turn-on in the IGBT's output characteristic, for both normal and short-circuit modes. The normal turn-on process can be divided into 4 phases, however, the short-circuit turn-on process has to be divided into 3 phases because there is no miller effect phase. Furthermore, in Fig. 3.6, the evolution of the IGBT for both normal and short-circuit modes, in terms of electron and hole carrier distributions together with the electric field variations, help to understand the differences from the internal physics' point of view.

- **Phase 1 (t_0 to t_1):** The first phase is the same for both normal and short-circuit modes. The phase is initiated when a positive gate voltage is applied to the gate-emitter terminal. A constant gate current i_g is injected and begins to charge the input capacitance C_i. Since the gate-voltage value is lower than the threshold voltage, the collector current is still zero. The gate-emitter voltage increases according to:

$$V_{GE}(t) = V_{GG} \cdot \left(1 - e^{-\frac{t}{R_g C_i}} \right) \tag{3.1}$$

  During this phase, the collector-emitter voltage is high, which means that the depletion capacitance is smaller than the oxide capacitance. Therefore, the gate-collector capacitance C_{gc} is much smaller than the gate-emitter capacitance C_{ge}, and therefore, the gate current is mainly charging C_{ge}.

- **Phase 2 (t_1 to t_2):** At this point V_{GE} reaches the threshold voltage and the collector current i_c starts to increase with a slope depending on the inductance of the power loop path. This phase is observed for both normal and short circuit modes, with the difference that the d_{ic}/dt is higher for the short-circuit condition due to the low inductive power loop path. The equations governing this period can be deduced by applying Kirchhoff's Voltage Law (KVL) to the power and gate loops, resulting in:

$$V_{CE}(t) = V_{DC} - L_c \cdot \frac{d_{ic}}{dt} - L_e \cdot \left(\frac{d_{ic}}{dt} + \frac{d_{ig}}{dt} \right) \tag{3.2}$$

$$V_{GE}(t) = V_{GG} - L_g \cdot \frac{d_{ig}}{dt} - R_g \cdot i_g(t) - L_e \cdot \left(\frac{d_{ic}}{dt} + \frac{d_{ig}}{dt} \right) \tag{3.3}$$

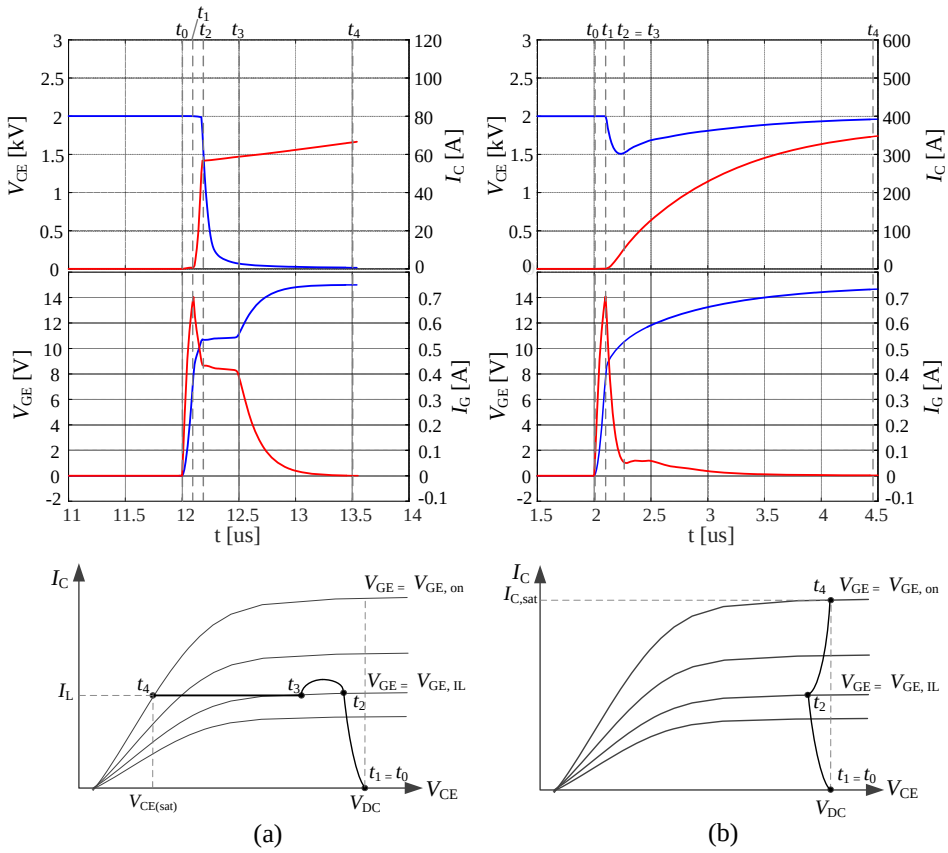

Figure 3.5: *The IGBT turn-on switching waveforms together with the representation in the IGBT's output characteristics: (a) normal turn-on process, and (b) short-circuit type 1 turn-on.*

During the normal turn-on process, the collector voltage does not drop as much as during the short-circuit process, thus, the electric field for t = 12.1 μs in Fig. 3.6 is larger than the one observed for the short circuit turn-on process at t = 2.15 μs.

- **Phase 3 (t_2 to t_3):** During this phase a constant gate-emitter voltage, named the Miller plateau, is observed only under normal turn-on conditions. During normal turn-on, the collector-emitter voltage V_{CE} continues to fall towards the collector-emitter saturation voltage $V_{CE,sat}$, at a lower rate as a consequence of a

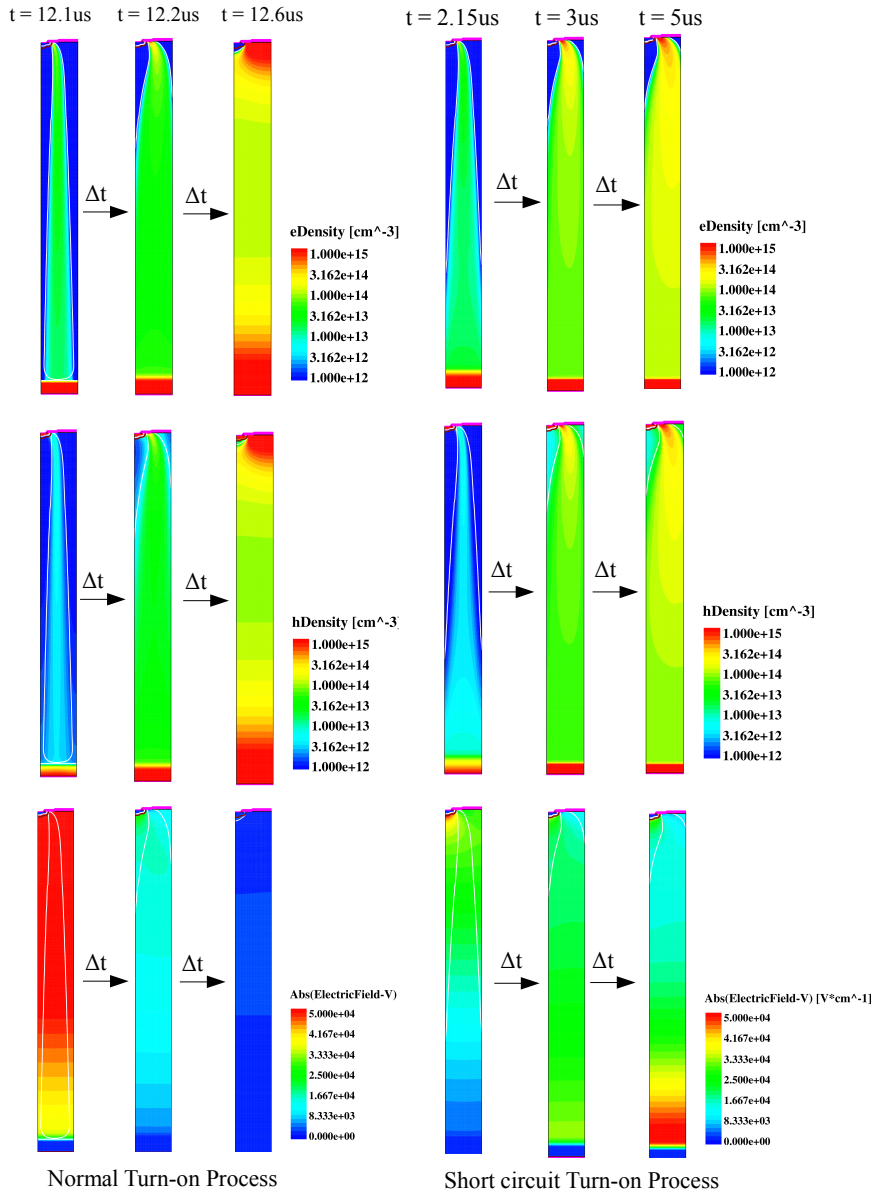

Figure 3.6: *The electron and hole density distribution in a planar IGBT at different instants during the turn-on process under normal and short-circuit modes: phase 2, (t = 12.1 μs and t = 2.15 μs), phase 3 (t = 12.2 μs) and phase 4 (t = 12.6 μs and t = [3 μs, 5 μs]).*

larger gate-collector capacitance C_{gc}. The gate current i_g is now charging C_{gc} and hence, the gate-emitter voltage remains constant. During short-circuit conditions, the V_{CE} value slightly drops, therefore, the non-linear gate-collector capacitance remains small compared to the oxide capacitance. The carrier profile and electric field distributions during this phase can be observed in Fig. 3.6 at the time instant t = 12.2 μ s. The Miller effect does not appear during short-circuit conditions, thus this phase is not observed and V_{GE} continues rising.

- **Phase 4 (t_3 to t_4):** For the normal turn-on process, the IGBT operates in the saturation region and the collector-emitter voltage V_{CE} reaches the $V_{CE,sat}$. The gate-emitter voltage becomes unclamped and continues to rise to sustain the load current i_c. At the same time, the gate current i_g decreases to zero flowing through C_{ge} and C_{gc}. During short-circuit, both the collector current and the collector-emitter voltage are high. The IGBT works in the desaturation region of the IGBT's output characteristic and the collector current is limited to a value that depends on the applied gate-emitter voltage.

  In Fig. 3.6 is illustrated that under normal conditions during phase 4 (i.e., t = 12.6 μs), the resulting electric field becomes very low across the whole n-base, as a consequence of the small collector voltage. The carrier density is higher at the emitter and the collector sides, basically due to the lower electric fields in these regions and so the electron velocities. This leads to current flow lines which tend to spread in the x-direction. The situation is different during short-circuit, the IGBT has to withstand a large electric field across the n-base, whose shape is dictated by the high electron injection and hole carriers. As a consequence, the electric field peak moves from the emitter side of the IGBT, at t = 2.15 μs, to the collector side of the IGBT, at t = 5 μs.

3.4 Simulation of the Short Circuit Oscillations

In the event of a short circuit, the IGBT has to withstand a high voltage V_{CE} and a high current I_C at the same time. Especially in IGBTs, being high-injection level devices, the built-in electric field strongly depends on the distribution of the injected carriers in the n-base. Fig. 3.6 shows the 2-D effects of a planar IGBT cell in terms of electron and hole distributions together with the corresponding electric field in the short-circuit mode. For making the study more clear, a cut along the vertical direction is made in Fig. 3.7, based on the results at t = 5 μs. The graph shows the electron, hole and doping concentrations together with the resulting blocking and short-circuit electric field variations. The electric field during blocking conditions is only determined by the doping concentration of the n-base, corresponding with the well-known triangular shape, also observed under normal switching conditions. However, the electric field during short-circuit conditions has a completely different shape. In Fig. 3.7 is noticed

that the electron and hole carrier concentrations are dominant over the background doping of the n-base, i.e. they are one order of magnitude higher than the doping concentration of the n-base (high-injection level). Even if the doping of the n-base is much lower than the electron and hole concentrations, the difference between them is comparable to the n-base doping concentration. This is crucial to understand the shape of the electric field. Referring to Poisson's equation (3.4), and being the effective charge concentration, $N_{eff} = N_D + h - e$, the electric field per unit width can be calculated as ($N_A = 0$):

$$\frac{dE}{dx} = \frac{q_e}{\varepsilon_s}\left(N_D - N_A + h - e\right) \tag{3.4}$$

As soon as the effective charge in the n-base becomes negative, the electric field slope changes its sign and rotates. Therefore, the electric field peak initially located at the emitter of the IGBT (blocking conditions), transfers to the collector of the IGBT during the short-circuit turn-on. This situation is commonly known as the Kirk effect, firstly investigated in BJTs and later observed in IGBTs under high current and high voltage conditions [12]. The balance between the doping concentration and the injected carriers depends on the current density of the device, the bipolar gain of the IGBT and the carrier drift velocity, which it is proportional to the electric field strength.

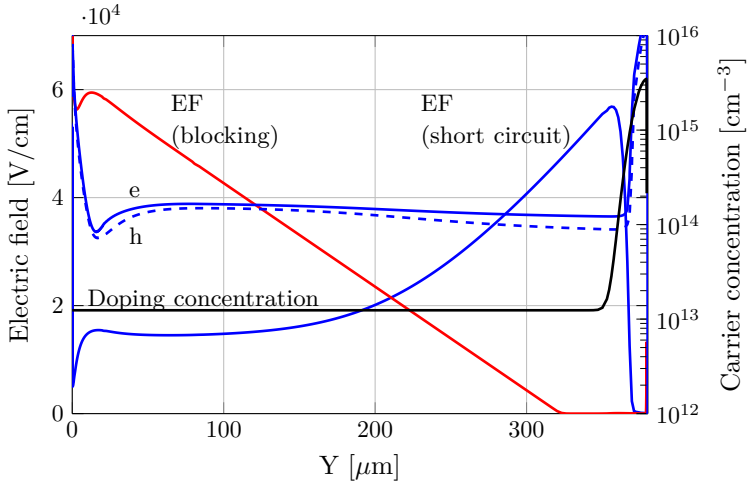

Figure 3.7: *Simulated electric field (EF) and carrier concentrations (e - electron and h - hole) during short-circuit operation along a cut in the vertical direction (see Fig. 3.6). The blocking electric field is reported for comparison.*

So far, the device has been analysed under a short circuit simulation where oscillations cannot be seen. In order to investigate the internal mechanisms occurring during such oscillations, the external circuit parameters are varied in order to find the conditions at which oscillations can be observed. Afterwards, other parameters such as DC-link voltage, temperature and gate voltage are varied to validate the correlation between the simulations and the real operation of the device.

3.4.1 Layout influence

The oscillation phenomenon has been thought to be as a consequence of uneven stray inductance between the parallel chips or cells, however, the oscillations during short-circuit even appear for a single IGBT cell. This has been demonstrated through experiments in Chapter 2. Fig. 3.8 shows the circuit configuration used for the finite-element short-circuit simulations. Four stray elements have been included: gate inductance L_g, emitter inductance L_e, collector inductance L_C and gate resistance R_g.

The effect of the parasitic inductance is evaluated by means of varying the external stray elements included in the circuit of Fig. 3.8. Device simulations have been done with one parameter varied at a time, keeping the rest of the parameters at their reference values. The reference values have been selected as $L_C = 1200$ nH, $L_g = 40$ nH, $L_e = 10$ nH and $R_g = 1\ \Omega$, which are coherent with the values that can be found in real devices.

The stray inductance in the commutation path, L_C, affects the IGBT short-circuit turn-on process in three ways:

- With higher collector inductance L_C, an increased undershoot across the collector-

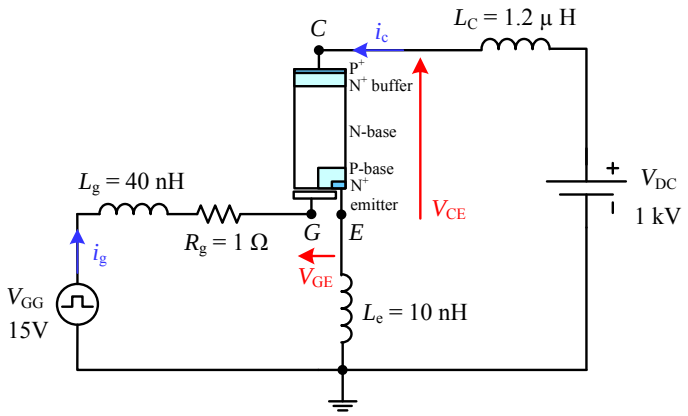

Figure 3.8: *Circuit for the finite-element short-circuit simulations of the 3.3-kV planar IGBT half-cell [58].*

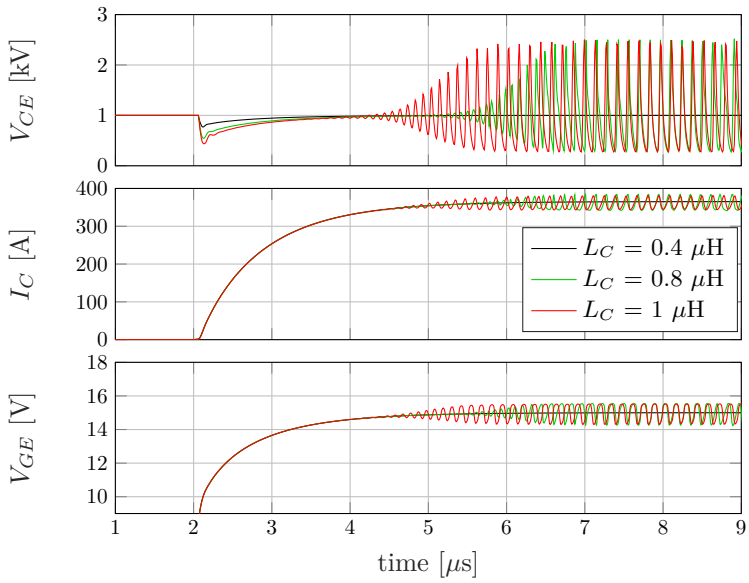

Figure 3.9: *Short-circuit simulation showing the oscillation dependency as a function of the collector inductance (L_e = 10 nH, L_g = 40 nH and R_g = 1 Ω).*

emitter voltage can be observed in Fig. 3.9.

- The lesser stray collector inductance L_C, the more robust is the IGBT against short-circuit oscillations. Fig. 3.9 indicates that the 3.3-kV planar IGBT does not oscillate if the collector inductance is 0.4 μH or below (L_e = 10 nH, L_g = 40 nH and R_g = 1 Ω).
- The oscillation frequency increases with decreasing L_C, being 9 MHz for L_C = 0.8 μH and 7 MHz for L_C = 1 μH.

The effect of the gate stray inductance is evaluated by simulating three different values of 20 nH, 50 nH and 70 nH. The stray inductance in the gate path, L_g, affects the IGBT short-circuit turn-on process in three ways:

- The lesser stray gate inductance L_g, the more robust is the IGBT against short-circuit oscillations. Fig. 3.10 indicates that the 3.3-kV planar IGBT does not oscillate, if the gate inductance is 20 nH or below (L_e = 10 nH, L_C = 1200 nH and R_g = 1 Ω).
- The amplitude of the oscillations varies as a function of the stray gate inductance value. The more gate inductance there is, the higher the oscillation amplitude.

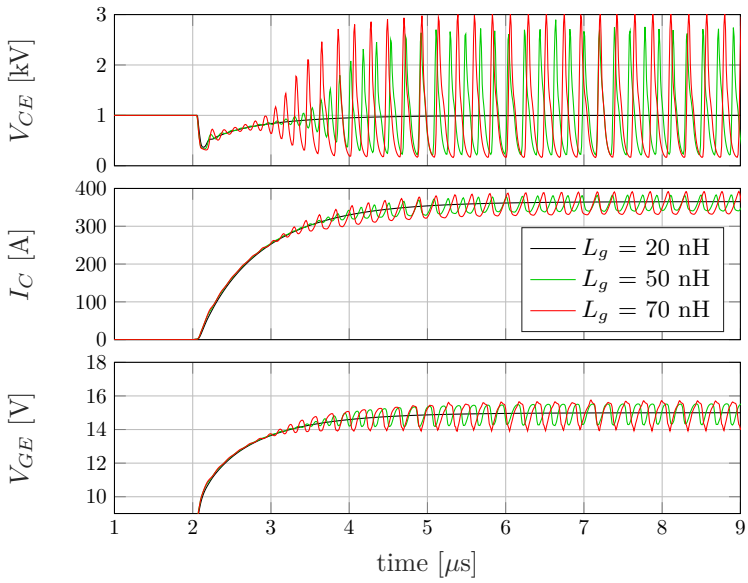

Figure 3.10: *Short-circuit simulation illustrating the oscillation dependency as a function of the gate inductance (L_e = 10 nH, L_C = 1200 nH and R_g = 1 Ω).*

- The oscillation frequency increases with decreasing L_g, being 5 MHz for L_g = 50 nH and 4.34 MHz for L_g = 70 nH.

The effect of the emitter inductance is a little complex because it takes part in both gate and commutation paths. Three different emitter stray inductances of 3 nH, 10 nH and 15 nH are chosen to demonstrate its dependency with the oscillation mechanism. The stray inductance in the emitter L_e, affects the IGBT short-circuit turn-on process in four ways:

- With higher emitter inductance L_e, the device switching speed will become much slower, as it is observed in Fig. 3.11. The IGBT turn-on is easier to control with high L_e values, especially when several devices need to be connected in parallel in a synchronized way. However, higher switching losses are introduced.
- The more stray emitter inductance L_e, the more robust is the IGBT against short-circuit oscillations. Fig. 3.11 indicates that the 3.3-kV IGBT presents oscillations delayed with time, as long as the emitter inductance is increased.
- As explained before, the amplitude of the oscillations varies as a function of the stray gate inductance value L_g. Since the emitter inductance is part of the gate

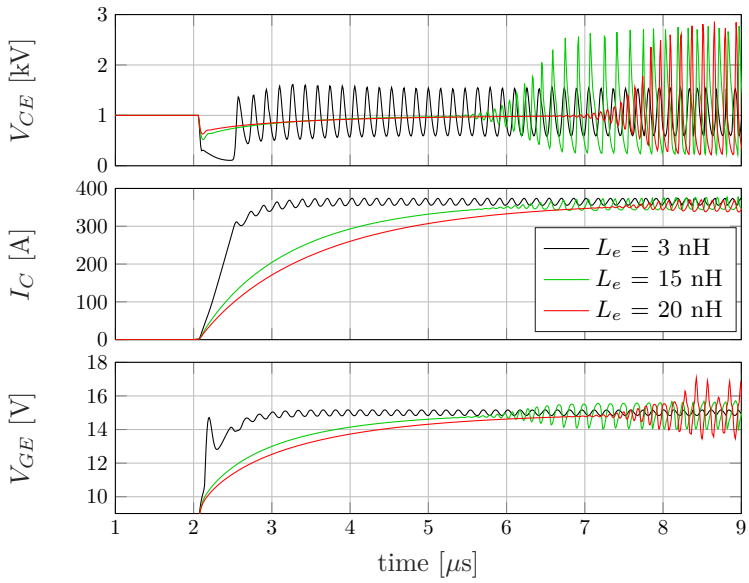

Figure 3.11: *Short-circuit simulation illustrating the oscillation dependency as a function of the emitter inductance (L_g = 40 nH, L_g = 40 nH and R_g = 1 Ω.)*

path, higher stray emitter inductance results also in higher oscillation amplitude, though, occurring later in time.

- The oscillation frequency slightly increases with increasing L_e, being 7.04 MHz for L_e = 20 nH, 6.57 MHz for L_e = 10 nH and 6.25 MHz for L_e = 0.3 MHz

3.4.2 DC-link voltage effect

The short-circuit waveforms of the planar IGBT at two different DC-link voltages of 1 kV and 2 kV are shown in Fig. 3.12. The IGBT exhibits a clean short-circuit waveform at a high DC-link voltage of 2 kV, however, some oscillations with frequency of 8 MHz can be observed at a 1 kV DC-link voltage. The physical mechanisms taking place in the IGBT can be better understood by looking at the electric field and the carrier profile distributions in the n-base region. For that reason, a cut along the vertical direction of the IGBT has been made. The cut position has been selected at x = 30 μm because we would like to look at the carrier accumulation between adjacent cells during the short-circuit event. Later, it will be demonstrated that the charge distribution profile in this region is very important to understand the root cause of the oscillation mechanism.

The IGBT has been evaluated at different time instants during the short-circuit turn

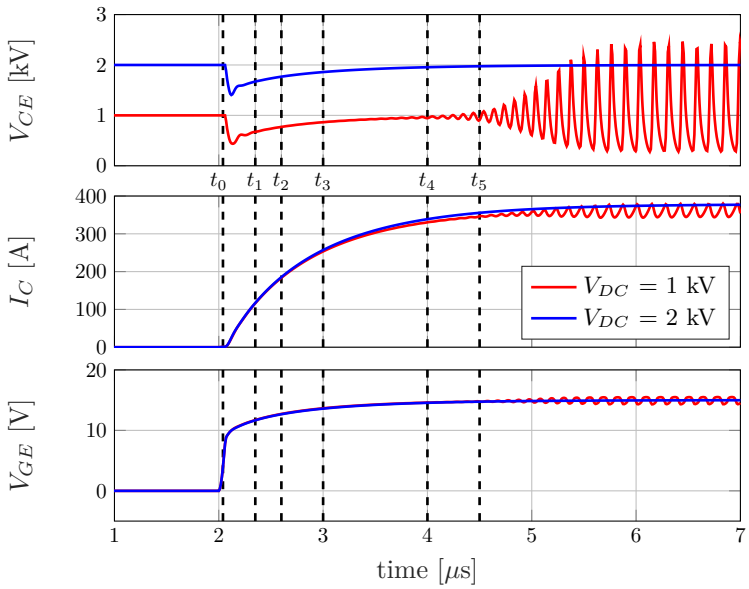

Figure 3.12: *Short-circuit simulations of a 3.3-kV IGBT at different DC-link voltages.*

on, as pointed out in Fig. 3.12, that is just before the device starts to self-oscillate. In this way, it is possible to understand which quantities are the ones leading the device into an oscillatory mode. The resulting electric field and electron carrier concentration are observed in Fig. 3.13. From the graphs in Fig. 3.13, it can be observed the transition from blocking state into short-circuit state, and how the positioning of the field peak gradually transfers from the emitter to the collector of the IGBT. By comparing the results at 2 kV and 1 kV, it is clear that a low collector voltage results in a lower electric field strength, which becomes even smaller at depths below 200 μm. It is also noted that at low DC-link voltages, the electrons tend to accumulate at the surface of the IGBT resulting in a carrier accumulation effect between adjacent cells. For example, in Fig. 3.13, the excess electron carriers are closer to the emitter of the IGBT at 1 kV DC-link voltage (red lines), different from the results at 2 kV (blue lines). This charge storage effect is vital to understand the root cause of the oscillation mechanism.

3.4.3 Gate voltage effect

The short-circuit waveforms at two different gate voltages of 15 V and 13 V are shown in Fig. 3.14. By reducing the gate driving voltage, the short circuit current at which

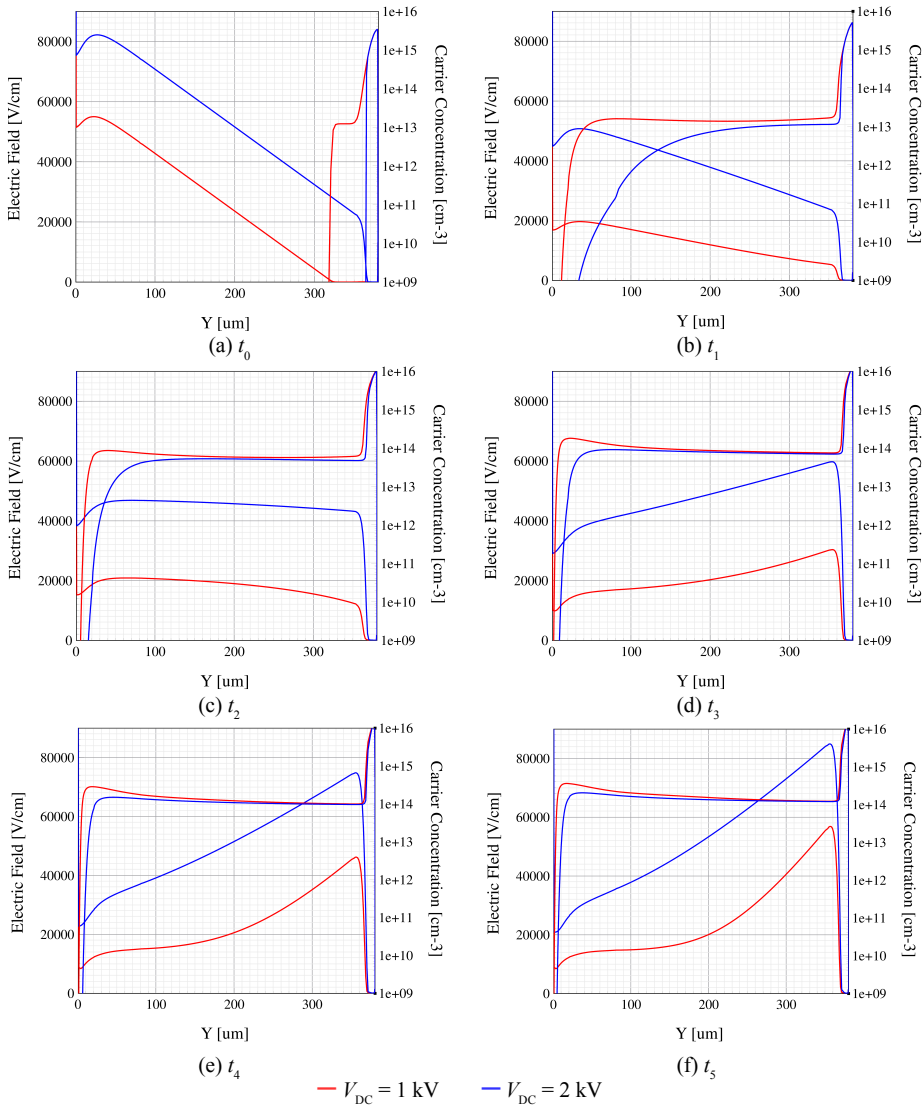

Figure 3.13: *Simulated electric field and electron concentration at different time instants along a cut in the vertical direction of the IGBT at $x = 30$ μm. Operating conditions can be observed in Fig. 3.12.*

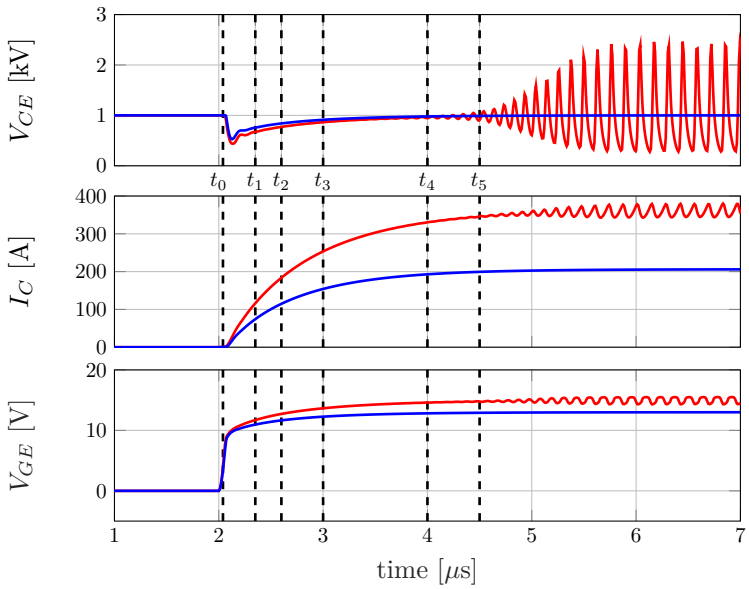

Figure 3.14: *Short-circuit simulations of a 3.3-kV IGBT at different gate voltages.*

the device operates is smaller, in agreement with the output IV-characteristics of the IGBT. This trend is beneficial to increase the short-circuit ruggedness, as the simulations indicate that the oscillations disappear. The physical mechanisms taking place inside of the IGBT are better understood through a cut along the vertical direction of the IGBT, as observed in Fig. 3.15. The graphs correspond with different time instants according to Fig. 3.14. One may note in Fig. 3.15, that the amount of electrons is slightly smaller at $V_{GE} = 13$ V due to the lower current density, this, in turn, has a strong impact on the electric field shape. The charge balance and electric field distributions as a function of the current density have been reported in [**?**]. The author defines a critical electric field, E_{cc}, so that if the electric field is higher than E_{cc}, N_{eff} decreases with increasing electron current density (i.e., this behavior can be observed at the collector of the IGBT). In contrast, if the electric field is lower than E_{cc}, N_{eff} will increase with increasing electron current density (i.e., this behavior can be observed at the emitter of the IGBT). This is reason why the electric field at the emitter of the IGBT is weaker (i.e., N_{eff} increases) with increasing current density at $V_{GE} = 15$ V.

Additionally, the resulting low electric field at the surface of the IGBT at high V_{GE}, coincides with electrons getting closer to the emitter side. This turns out in a more evident carrier accumulation effect (PiN effect), if compared with the results at low V_{GE}, where oscillations are not observed. The simulation results presented here

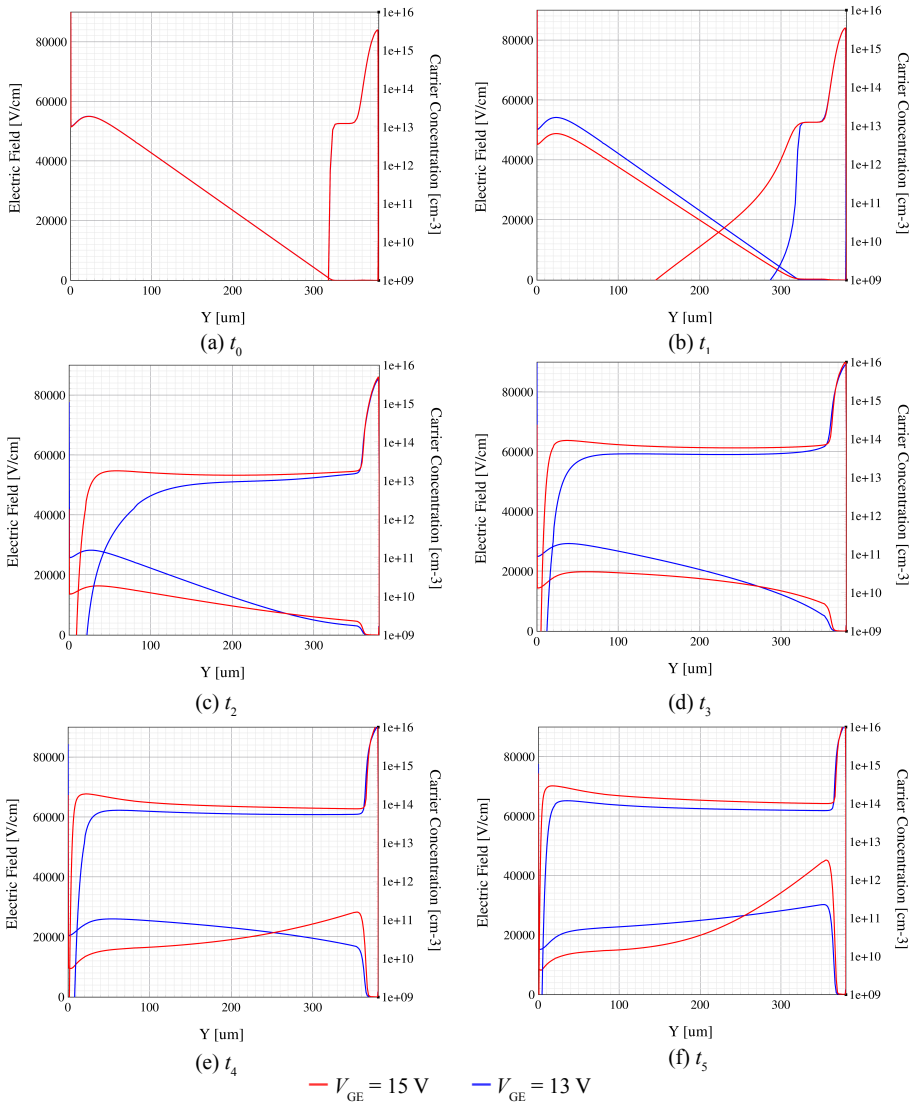

Figure 3.15: *Simulated electric field and electron concentration at different time instants along a cut in the vertical direction of the IGBT at $x = 30$ µm. Operating conditions can be observed in Fig. 3.14.*

demonstrate that the physical trends leading to oscillations are the same as the ones observed when the DC-link voltage is varied.

3.4.4 Temperature effect

In order to investigate the temperature-related effects on the short-circuit oscillations, isothermal simulations have been performed at different temperatures. The self-heating of the IGBT during the short-circuit pulse has not been taken into account. It is or course possible, but not worth at this stage, as a coarse analysis is needed here. The result is that the decreasing channel mobility effect causing the decrease in collector current during the short-circuit pulse is not modelled.

Fig. 3.16 shows the simulated short circuit waveforms of the 3.3-kV planar IGBT as a function of two temperatures (25°C and 100°C). It can be noted that the starting time of the oscillation happens earlier at higher temperatures, while the oscillations have the same amplitude. The reason can be better understood by looking at the evolution of the physical parameters of the IGBT, such as the electric field and the electron carrier concentration, in Fig. 3.17. The graphs correspond with different time instants according to Fig. 3.16. Once again, note that the simulation at T = 100 °C has an electric field shape which rotates earlier in time, if compared with the results at T =

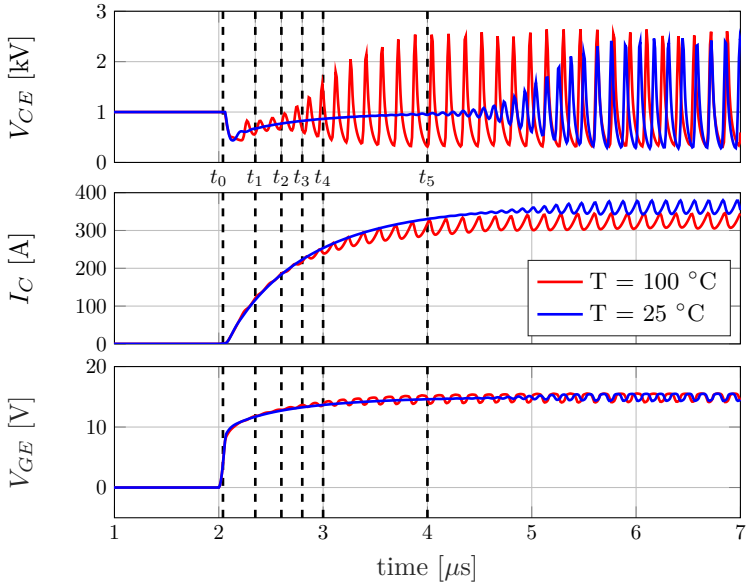

Figure 3.16: *Short-circuit simulations of a 3.3-kV IGBT at different temperatures.*

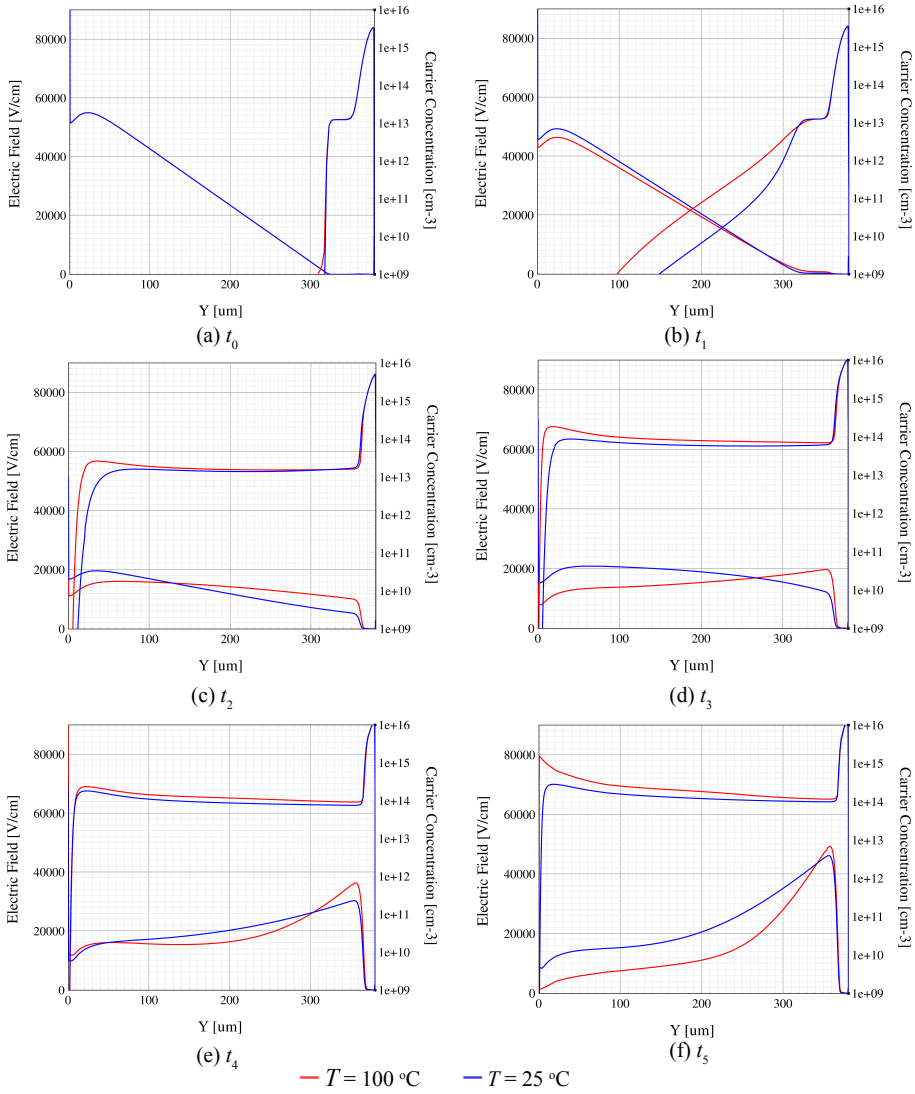

Figure 3.17: *Simulated electric field and electron concentration at different time instants along a cut in the vertical direction of the IGBT at $x = 30$ µm. Operating conditions can be observed in Fig. 3.16.*

25°C. At high temperatures and for a collector voltage of 1000 V, the electric field at the surface of the IGBT is lower, which it is associated with a greater amount of electrons between adjacent cells, and thus, with the occurrence of oscillations.

3.5 Discussion of the Physical Mechanisms Leading to Oscillations

In the previous section, a detailed analysis has been provided on the effects of the external circuit stray elements and the IGBT operating conditions. The simulation results indicate that the operating conditions strongly affect the amount and position of the holes and electrons in the n-base, and thus, the shape of the electric field is remarkably influenced. In the following, the physical mechanisms leading to oscillations are summarized, which are further supported by the simulation results:

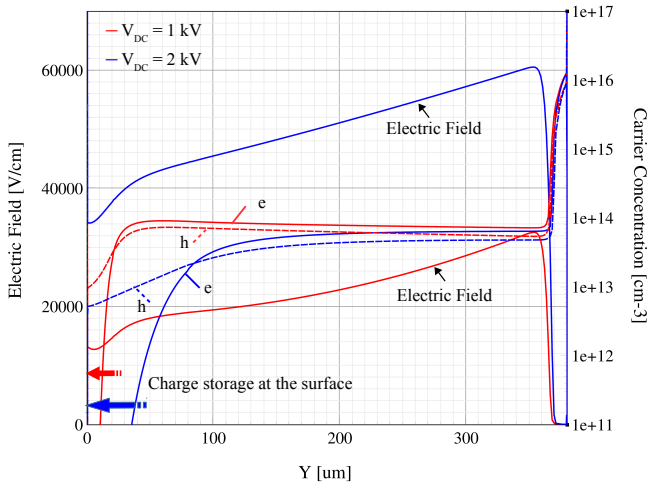

Figure 3.18: *Simulated electric field and carrier concentrations during short-circuit operation along a cut in the vertical direction of the IGBT at $x = 30\ \mu m$. Working conditions at $t = 3\ \mu s$ (see Fig. 3.12) [58].*

1. The IGBT during short circuit presents a rotated-field (Kirk Effect) due to the low n-base doping and high-level carrier injection features, inherent of IGBTs. The high electron injection, about 1 order of magnitude above the background doping of the n-base, modifies the effective charge and becomes negative ($N_{eff} = N_D + h - e$). This evidence is confirmed in Figs. 3.18, 3.19 and 3.20, where the

amount of electrons prevail over the amount of holes and the background doping concentration, which is $1 \cdot 10^{13}\ cm^{-3}$.

2. The IGBT presents an inhomogeneous electron density distribution on the emitter side, as previously reported in Fig. 3.3. It is interesting to observe that electrons tend to accumulate at the emitter side when the electric field is below a given value, at depths below 100 μm. Because the IGBT exhibits an electric field shape which peaks at the collector and not at the emitter as it is supposed to, an excess of electrons is observed between adjacent cells. This behavior is highlighted in Figs. 3.18, 3.19 and 3.20 with red arrows. The charge-storage effect is correlated with the occurrence of oscillations. For instance, in Fig. 3.18, the electron density is nearer the surface at a low DC-link voltage of 1 kV (oscillatory mode), different from the results at 2 kV (non-oscillatory mode). The same trend is also noticed in Figs. 3.19 and 3.20.

3. At low electric fields, the drift velocity is proportional to the electric field as it occurs when the device operates at 1000 V DC-link voltage. On the contrary, at high electric fields, the drift velocity becomes close to saturation and therefore not field dependent. The electron drift velocity at low field conditions is given by:

$$v_e(E) = \mu_e(E) \cdot E \tag{3.5}$$

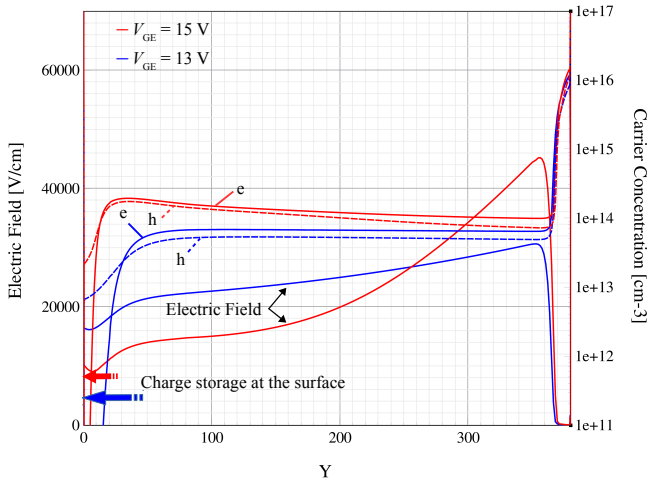

Figure 3.19: *Simulated electric field and carrier concentrations during short-circuit operation along a cut in the vertical direction of the IGBT at $x = 30\ \mu m$. Working conditions at $t = 4\ \mu s$ (see Fig. 3.14) [58].*

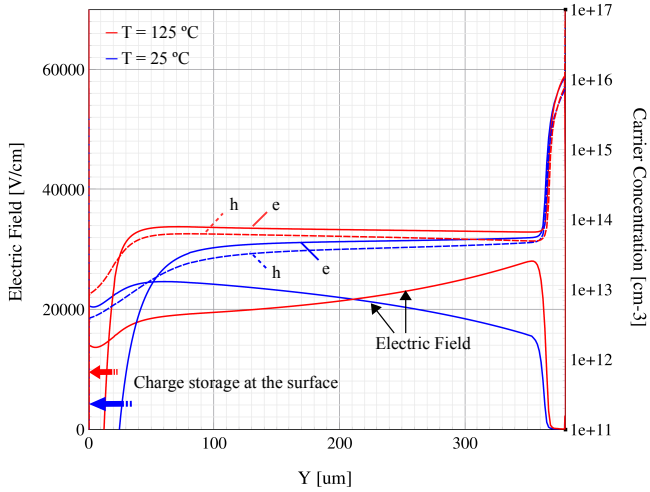

Figure 3.20: *Simulated electric field and carrier concentrations during short-circuit operation along a cut in the vertical direction of the IGBT at $x = 30\ \mu m$. Working conditions at $t = 2.6\ \mu s$ (see Fig. 3.16) [58].*

The relation between the current density and the electron carriers moving at their drift velocity is given as:

$$J_e = q \cdot N \cdot v_e(E) \tag{3.6}$$

This equation helps to understand that for a constant collector current, and therefore a constant electron current density, the low electron velocity observed at the emitter of the IGBT can only result in an excess of electrons. This explains the observed electron accumulation effect between adjacent cells. Figs. 3.21, 3.23, and 3.25, prove that the operating conditions where the IGBT oscillates show a low carrier velocity at the emitter side associated with charge-storage effects, basically driven by the electric field shape across the n-base of the IGBT. In contrast, Figs. 3.22, 3.24, and 3.26, demonstrate that as soon as the electrons move faster at the emitter of the IGBT, which is function of the electric field strength, the charge-storage effect is not observed and oscillations are not triggered for $V_{GE} = 13$ V and $V_{DC} = 2$ kV, or come later in time as for the case when T = 100°C.

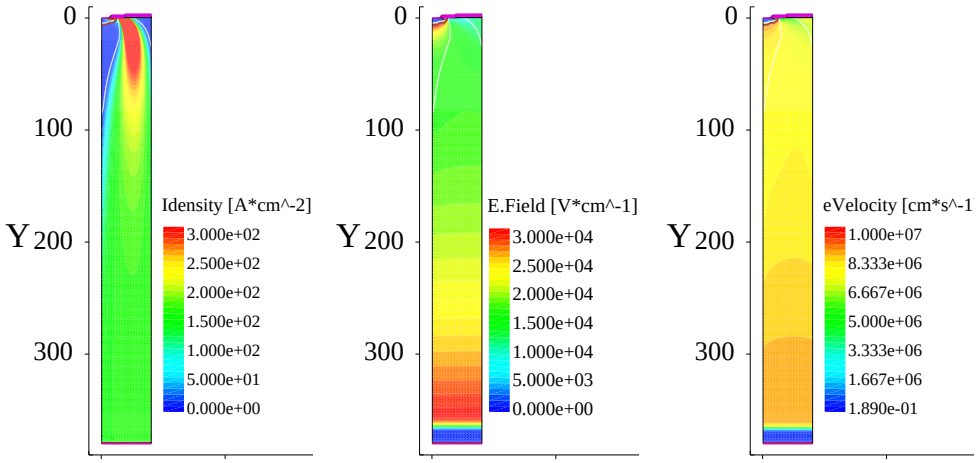

Figure 3.21: *Simulated current density, electric field and electron velocity at V_{DC} = 1 kV, for t = 3 µs (see Fig. 3.12).*

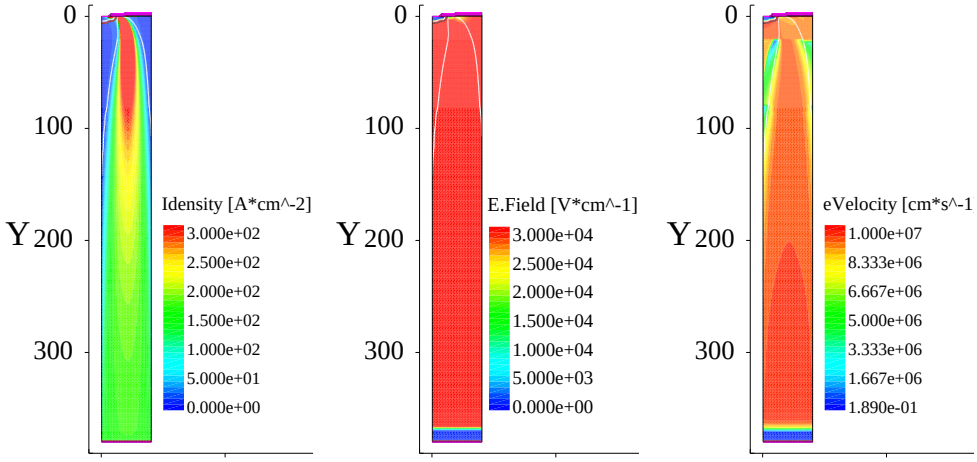

Figure 3.22: *Simulated current density, electric field and electron velocity at V_{DC} = 2 kV, for t = 3 µs (see Fig. 3.12).*

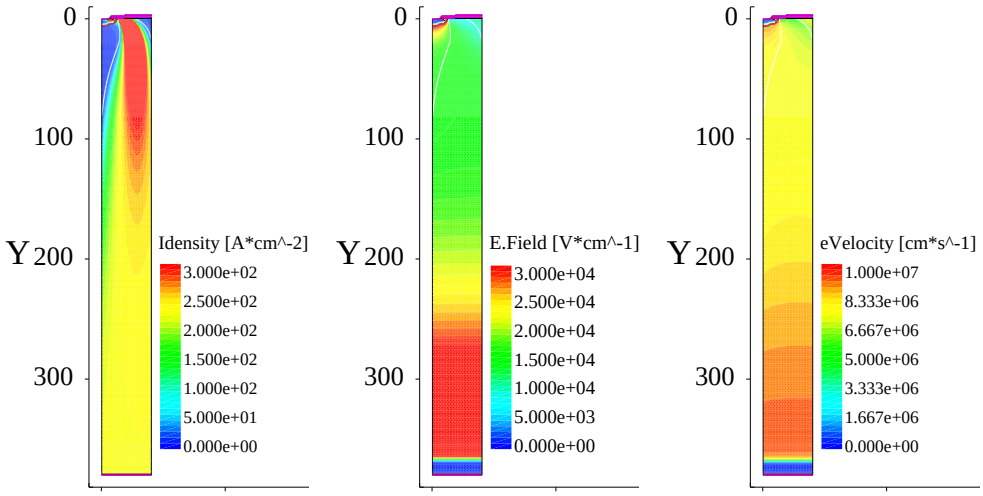

Figure 3.23: *Simulated current density, electric and electron velocity at V_{GE}= 15 V, for t = 4 µs (see Fig. 3.14).*

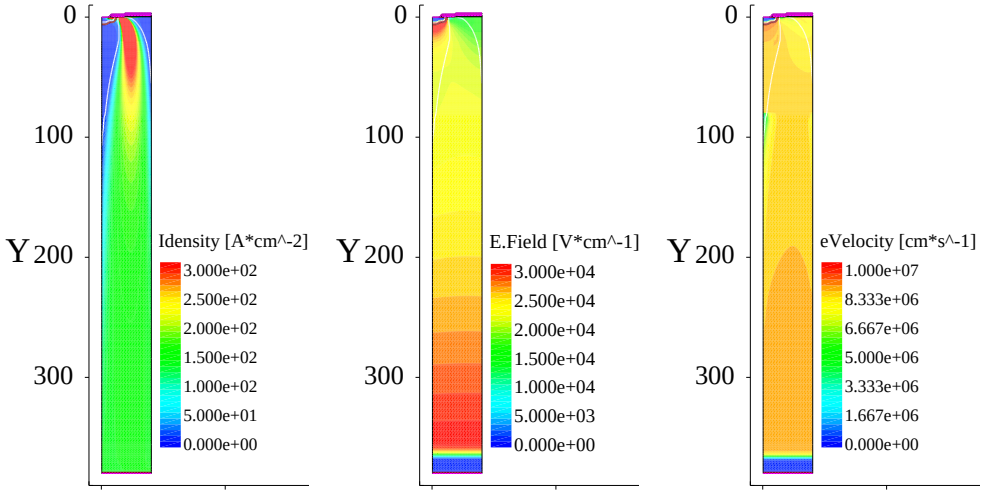

Figure 3.24: *Simulated current density, electric and electron velocity at V_{GE}= 13 V, for t = 4 µs (see Fig. 3.14).*

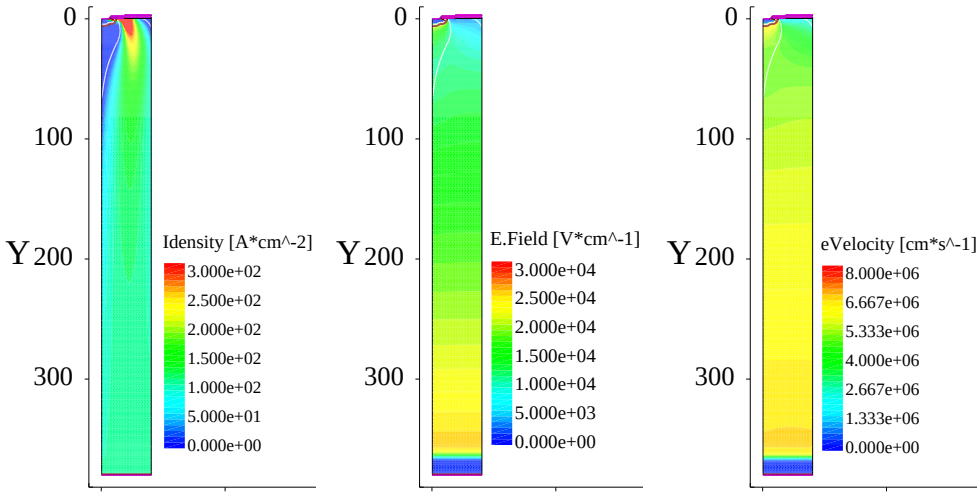

Figure 3.25: *Simulated current density, electric field and electron velocity at $T = 25\ ^\circ C$, for $t = 2.6\ \mu s$ (see Fig. 3.16).*

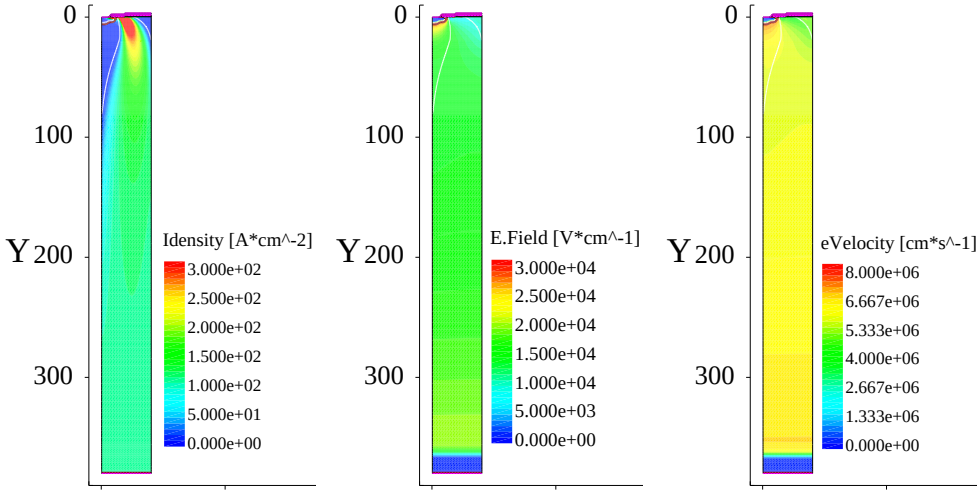

Figure 3.26: *Simulated current density, electric field and electron velocity at $T = 100\ ^\circ C$, for $t = 2.6\ \mu s$ (see Fig. 3.16).*

3.6 Conclusion of this Chapter

In this chapter, the complex short-circuit oscillation mechanism has been simulated with both circuit and device analysis. A sensitivity analysis has been performed, demonstrating that the simulations show the same key enabling factors as the experiments, i.e. layout influence and condition parameters (V_{CE}, V_{GE} and T). It has been found that the oscillations can only occur when the electric field at the emitter of the IGBT becomes weak, particularly because of the Kirk Effect.

The block diagram in Fig. 3.27 helps to understand the trends prior the device starts to self-oscillate. As soon as the collector voltage decreases, the electric field drops and the carrier velocities follow the same pattern as the electric field, which means that they also decrease. This relationship is more crucial at the emitter of the IGBT, because the electric field is rotated and especially at the emitter the electric field is very weak. In the short-circuit mode, the collector current is determined by its saturated value, which can be assumed to be constant. Therefore, a low carrier velocity results in higher carrier densities associated with charge-storage effects at the emitter. If the charge-storage effect becomes stronger with short-circuit time and does not become fixed, oscillations will be observed.

In order to prevent the short-circuit oscillations, one should avoid, as much as possible, the low electron velocity at the emitter of the IGBT, which is function of the electric field amplitude. One should guarantee that the electric field is strong enough at the emitter, in order to avoid the low electron velocity, causing electron accumulation effects. This is confirmed through Figs. 3.18, 3.19 and 3.20, where higher electric fields at the emitter are associated with a more robust short-circuit operation without oscillations [58].

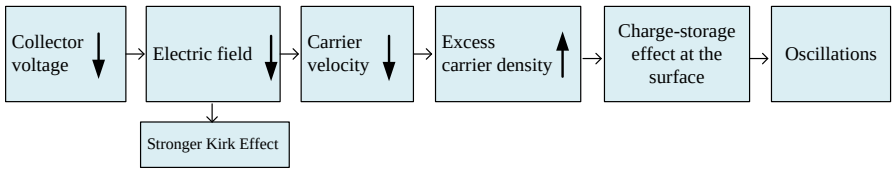

Figure 3.27: *Relation between electric field distribution and charge storage effect observed prior to short-circuit oscillations.*

Chapter 4

The Short Circuit Oscillation Phenomenon in IGBTs

In this chapter, the short-circuit oscillation mechanism in IGBTs in investigated through the use of two different IGBT cell structures based on a planar and a trench-gate designs. The root cause of oscillations can be explained in terms of device capacitive effects coming from both carrier distribution profile and electric field fluctuations. The 2-D effects during one oscillation cycle reveal that the gate capacitance varies according to the strength of electric field near the emitter, which in turn leads to charge-storage effects associated with the low carrier velocity in this region. Additionally, the hypothesis of the time-varying capacitance is validated and solutions are given to the problem by increasing the electric field strength at the emitter fo the IGBT.

4.1 Introduction

Based on the experimental results presented in Chapter 2, and the sensitivity study discussed in Chapter 3, some initial conclusions about the root cause of the short circuit oscillations can be made. A necessary condition for driving the IGBT into an oscillatory mode seems to be the weak electric field observed at the surface of the IGBT. The gradient of the electric strength dE/dy is function of the effective charge concentration in the n-base, $N_{effective}$, which becomes negative at depths below y = 100 μm. The consequence of a weak electric field is that the carrier drift velocities, which are linearly proportional to the applied electric field, become substantially smaller at the surface of the IGBT. This low carrier velocities lead to charge-storage effects at the surface of the IGBT [59]. So far, the physical mechanisms taking place during each oscillation cycle have not been explained, neither the root cause for the self-sustained oscillations. These

two aspects will be addressed in this chapter.

4.2 Physical Mechanisms during Short Circuit

To analyze the physical mechanisms taking place during the oscillations, mixed-mode device simulations have been performed with the following set of circuit parameters: gate inductance of 40 nH (L_g), emitter inductance of 10 nH (L_e), collector inductance of 1200 nH (L_C), and gate resistance of 1 Ω (R_g). These parameters have been chosen in agreement with the values that one can find in real devices, but also taking into account the results from the sensitivity analysis carried out in Chapter 3, where the layout influence on the occurrence of the oscillations has been discussed. To make the study more thorough, the performance of two different IGBT designs (i.e., trench-gate and planar) are compared, demonstrating the validity of the hypothesis. Figs. 4.1 and 4.2 demonstrate that the oscillation phenomenon can be reproduced via mixed-mode device simulations for both planar and trench IGBT designs. This is of particular importance in order to identify which parameters influence the short-circuit process and later justify the root cause of such oscillations.

When comparing the results from the experiments and the simulations, it can be noted that the amplitude of the oscillation rapidly increases in a few microseconds for both gate and collector voltage waveforms. For a better understanding of the processes, it can be assumed that the collector current remains constant, where a 2% and 10% maximum variation is observed for the experiments and simulations, respectively. Note

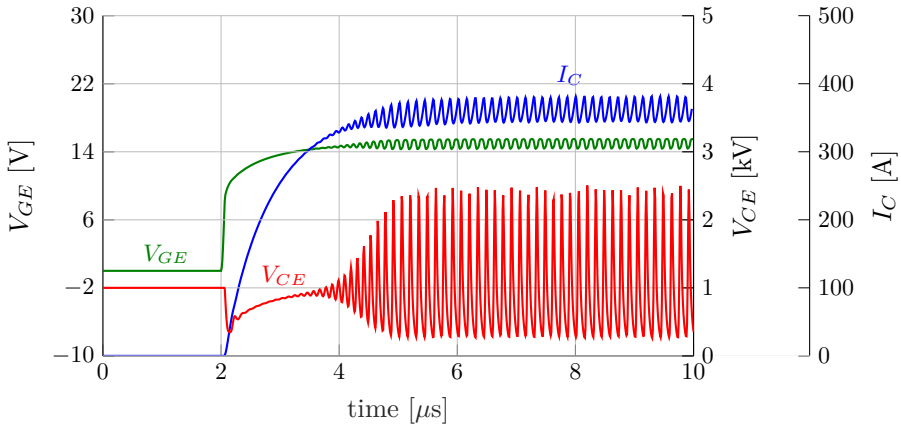

Figure 4.1: *Short-circuit simulation of a SPT 3.3-kV planar IGBT at V_{DC} = 1 kV, showing oscillations after t = 3 μs.*

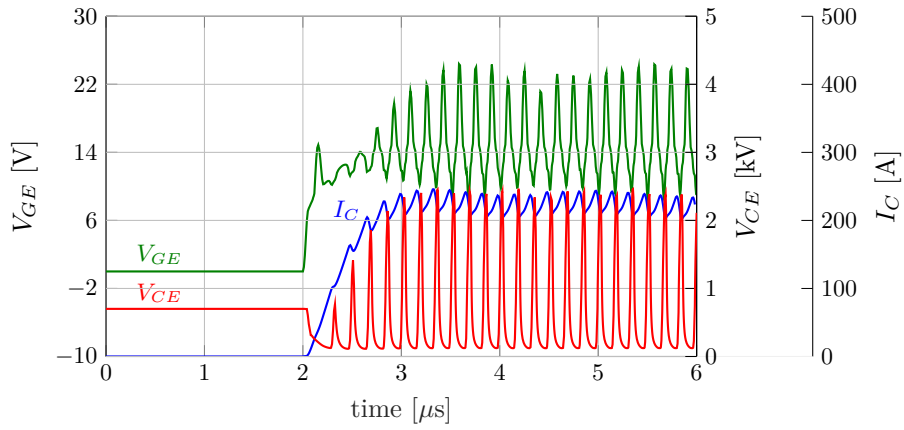

Figure 4.2: *Short-circuit simulation of a SPT 3.3-kV Enhanced-Trench IGBT at V_{DC} = 700 V, showing oscillations during the turn-on process.*

that the oscillation frequency from both experiments and simulations are in the MHz range. A better match of the oscillation frequency between simulations and experiments can be accomplish by further adjusting the device capacitances and the circuit stray inductances. The analysis of the short-circuit oscillations has been addressed by looking at the physical mechanisms taking place inside of the IGBT during one oscillation cycle. First, the IGBT has been evaluated when the oscillations are constant in amplitude in order to discard the dynamic effects, and second, the IGBT is further evaluated when the oscillations are firstly observed and its amplitude is increasing with time.

4.2.1 Simulations during the oscilations

A closer examination of Fig. 4.1 between the time instants 5.1 μs and 5.45 μs can be obtained in Fig. 4.3, where the phase-shift relation of each electrical parameter is shown (i.e., V_{CE}, I_C, i_g and V_{GE}). In this graph, the gate current and the calculated instantaneous input capacitance are added with respect to Fig. 4.1. The instantaneous input capacitance is calculated from i_g and V_{GE} through the formula, $C_i = i_g \times dt/dV_{GE}$. The interaction of the device internal physical mechanisms with the main circuit parameters is investigated by looking at the electric field and the carrier distribution profiles during one oscillation cycle, as shown in Fig. 4.4. The main difference is that when V_{CE} decreases, that is phase A in Fig. 4.3 corresponding to the time instants t_0, t_1, t_2 and t_3, the IGBT builds a dense electron charge near the emitter coinciding with a weak electric field at the emitter (see Fig. 4.4). On the other hand, during phase B, corresponding to the time instants t_4 and t_5, V_{CE} increases and the electric field comes

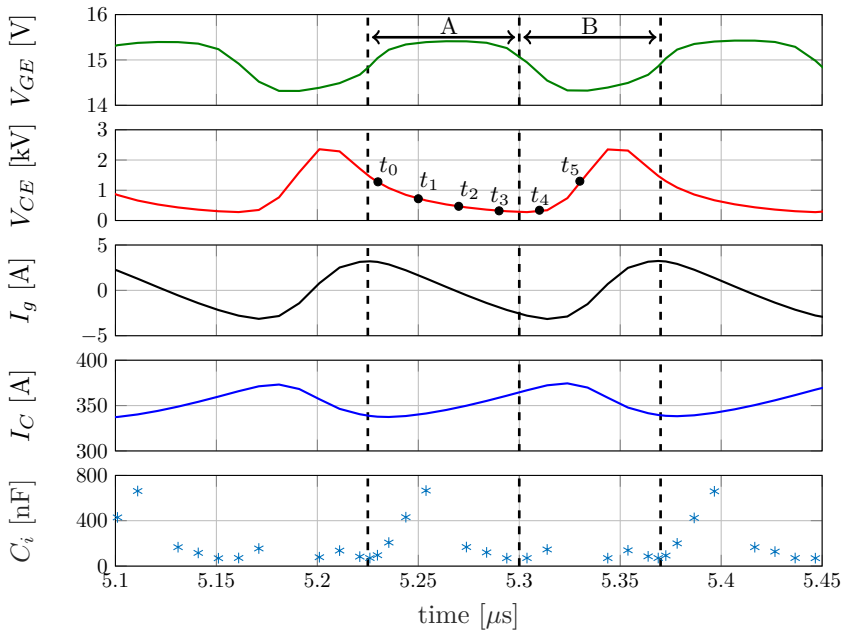

Figure 4.3: *Time-zoom of Fig. 4.1 showing the two phases (A and B) taking place during one oscillation cycle, together with the corresponding instantaneous gate capacitance C_i.*

back to its typical triangular shape. As a consequence, the electron accumulation region at the emitter of the IGBT is no longer observed (see Fig. 4.4)

Based on this insight, it is important to note that the IGBT exhibits a large variation of the input capacitance, which results from the position of the excess carriers inside the n-base of the IGBT. To reach a firm conclusion, one oscillation cycle is divided into two phases: phase A or charge-storage phase and phase B or voltage build-up phase. The 2-D effects together with the cuts along the vertical direction of the IGBT will demonstrate the correlation between the electrical waveforms and the internal physical mechanisms for both trench and planar IGBT cell designs.

4.2.1.1 Phase A: charge-storage phase

During this phase, a carrier accumulation effect appears at the surface of the IGBT coinciding with an increase of the input capacitance. The gate-emitter voltage V_{GE} takes higher values than 15 V, i.e., the value of the positive gate bias voltage. This, in turn, causes the collector voltage V_{CE} to drop for sustaining the nearly constant collector

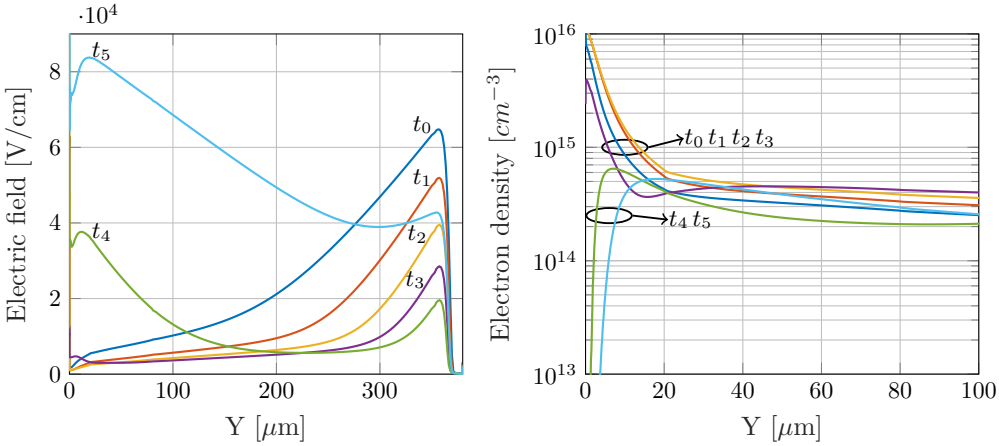

Figure 4.4: *Electric field variation (left) and electron density profile (right) in the planar IGBT at the time instants illustrated in Fig. 4.3.*

current. The carrier accumulation effect is observed as soon as V_{CE} drops, which it is eventually associated with a decrease of the electric field. In short-circuit conditions, the electric field has been found to be weak near the emitter as a consequence of the Kirk effect. This implies that the carrier drift velocity, which is linearly proportional to the electric field, will follow the same pattern as the electric field, i.e., carriers move slower at the emitter and faster at the collector. The observed charge-storage effect is in agreement with the assumption of constant collector current, implying that a lower electron velocity near the emitter can only result in a higher electron density according to $J_n = qnv_n$. This behavior is confirmed in Fig. 4.5 for the planar IGBT cell. Similarly, the trench IGBT cell has been evaluated when the collector voltage is low, the 2D plots observed in Fig. 4.6 reveal the same trend.

From the external circuit point of view, the gate current waveform in Fig. 4.3 indicates that two mechanisms take place during phase A: (i) a charge period (positive i_g) - the gate capacitance has a large value when the capacitor is charged up; this means that the energy initially stored in the gate inductance is now transferred to a larger gate capacitance. Then, the dV_{GE}/dt slows down because the capacitance increases. Once the current reaches zero, the capacitance is charged beyond the gate driver voltage (V_{GG} =15V) and it starts discharging, reversing the current through the inductance; (ii) a discharge period (negative i_g) - the voltage across the large capacitance starts falling as the current through the gate inductance begins to rise. Therefore, the energy stored in the capacitance is now transferred to the inductance. During this transition, the gate capacitance changes its value from a high value to a lower one causing V_{GE} to rapidly decrease.

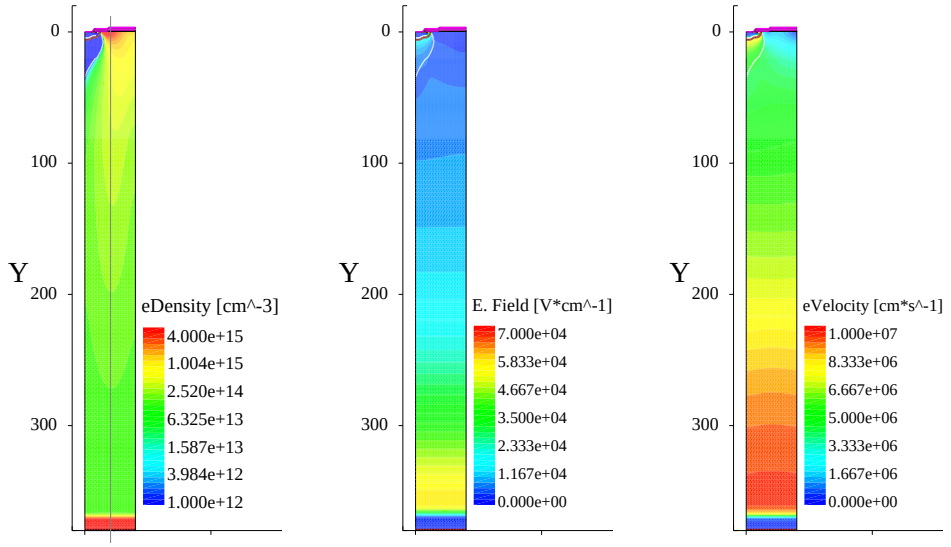

Figure 4.5: *The 3.3-kV planar IGBT during phase A. Left: electron density; middle: electric field; right: electron velocity. The cut line for Fig. 4.9 is highlighted.*

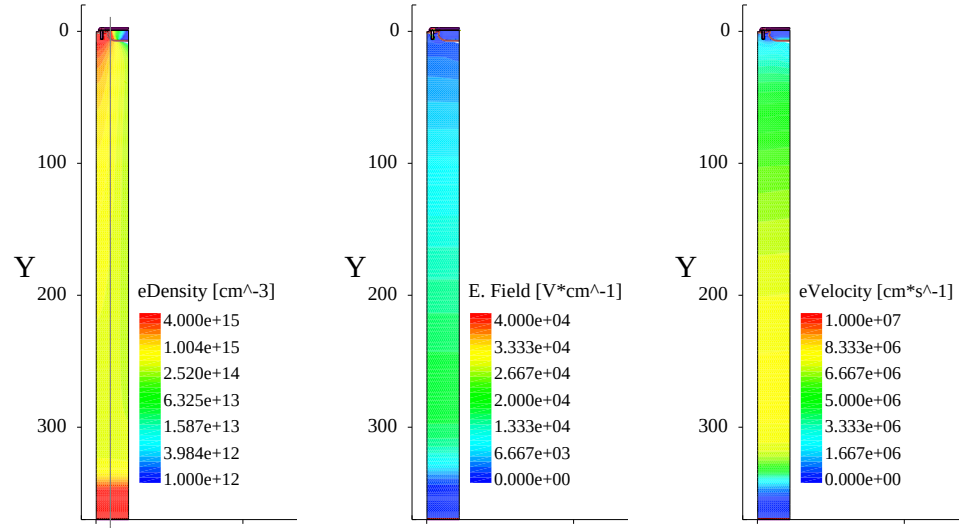

Figure 4.6: *The 3.3-kV trench IGBT during phase A. Left: electron density; middle: electric field; right: electron velocity. The cut line for Fig. 4.10 is highlighted.*

4.2.1.2 Phase B: voltage build-up phase

During this phase, the electron accumulation region at the surface of the IGBT disappears coinciding with a smaller value of input capacitance. Because of V_{GE} decrease, at nearly constant collector current, V_{CE} starts increasing and sweeps out the excess carrier concentration near the emitter. With a higher V_{CE}, the electric field builds up across the n-base of the IGBT, which in turn implies an increase in the electron velocity. A higher electron velocity, especially at the emitter of the IGBT, where in phase A was pretty low, produces a reduction in the electron density counteracting the Kirk Effect. As a consequence, the rotated electric field comes back to its well-known triangular shape. This is confirmed in Figs. 4.7 and 4.8 for both planar and trench devices. By looking at the gate current, the input capacitance charges and discharges during phase B, but now the capacitance has a small value.

4.2.1.3 Comparison between phase A and phase B

In summary, the evolution of the IGBT during the short-circuit oscillations varies between two situations, as demonstrated with the 2-D device plots - phase A and phase B. A better insight of these two mechanisms is gained through a vertical cross-section of the IGBT cell in Figs. 4.9 and 4.10, for both planar and trench IGBTs. Hence, the differences in electric field and electron density profiles can be better compared. In order to help the understanding of the reader, the two situations are additionally represented in Fig. 4.11.

1. In phase A, a rotated-field associated with electron accumulation effects at the emitter of the IGBT, which coincides with a high capacitance value, is observed as a consequence of the low carrier velocity. This is evidenced in Figs. 4.9 and 4.10 for the planar and the trench IGBT cells.

2. In phase B, a non-rotated field associated with holes prevailing over electrons, showing no charge-storage effects, is observed as a consequence of the high V_{CE} leading to a high carrier velocity. This is evidenced in Figs. 4.9 and 4.10 for both planar and trench IGBT cells.

Under these conditions, the IGBT presents a time-varying gate capacitance changing according to the electric field shape and the excess electron carrier concentration profile near the emitter of the IGBT. This is in fact, the basis of a parametric oscillation where the capacitor behaves as an active element. This concept is explained hereafter in this chapter.

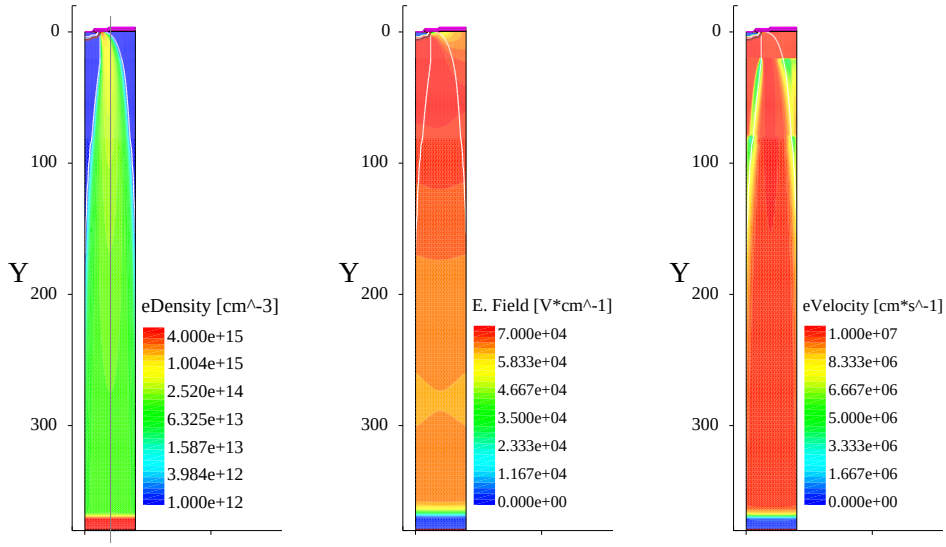

Figure 4.7: *The 3.3-kV planar IGBT during phase B. Left: electron density; middle: electric field; right: electron velocity. The cut line for Fig. 4.9 is highlighted.*

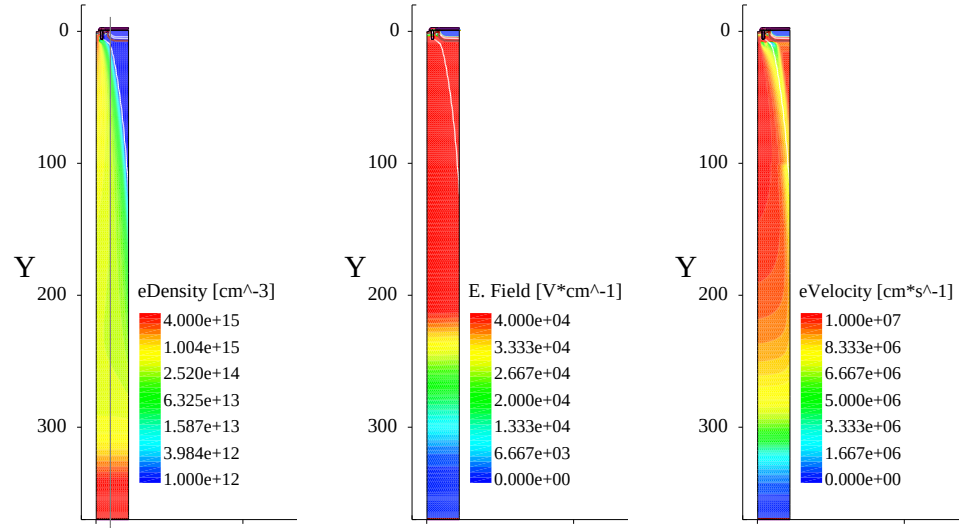

Figure 4.8: *The 3.3-kV trench IGBT during phase B. Left: electron density; middle: electric field; right: electron velocity. The cut line for Fig. 4.10 is highlighted.*

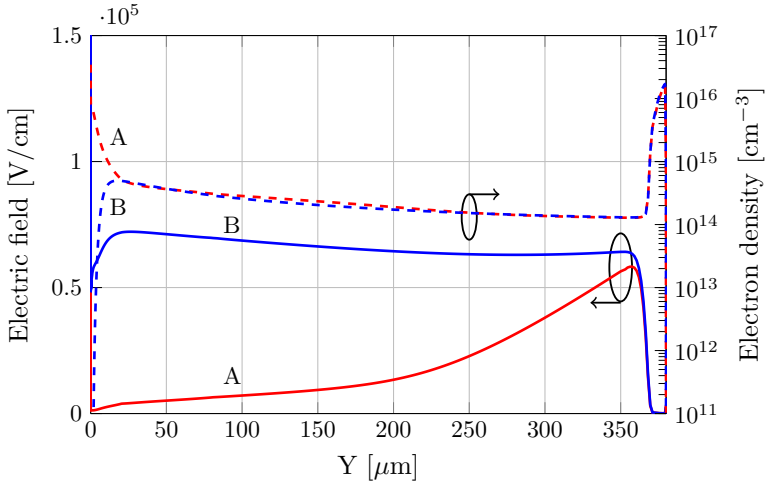

Figure 4.9: *Simulated electric field and electron density of the planar IGBT during phases A and B along the vertical cut observed in Figs. 4.5 and 4.7 .*

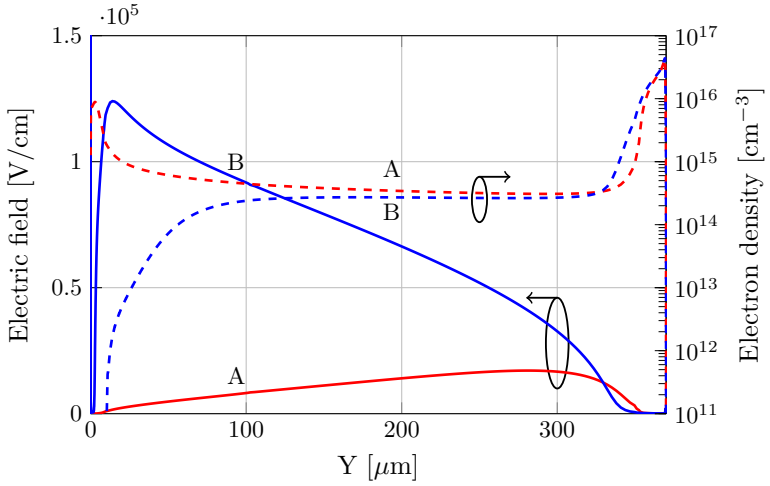

Figure 4.10: *Simulated electric field and electron density of the trench IGBT during phases A and B along the vertical cut observed in Figs. 4.6 and 4.8.*

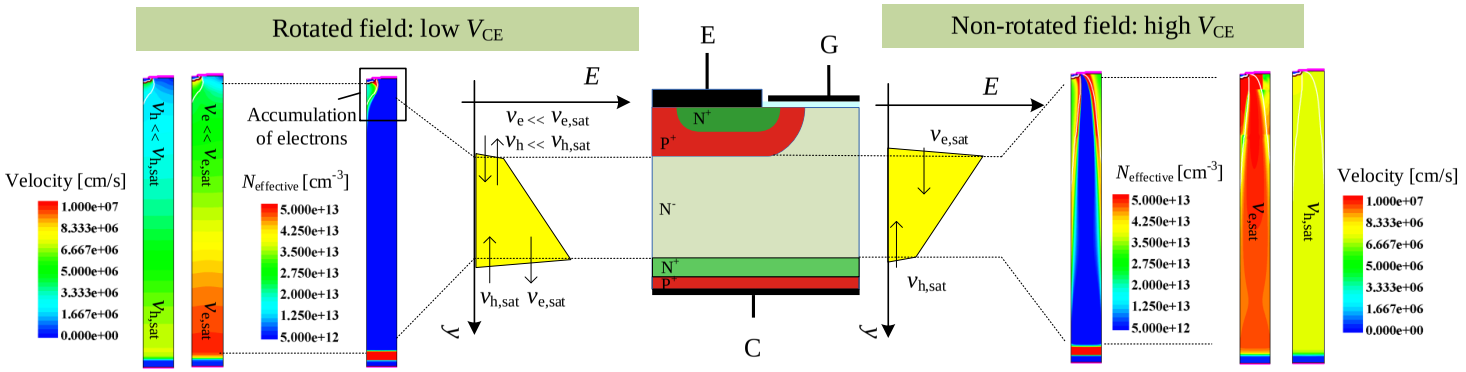

Figure 4.11: *Schematic together with 2-D plots of the two mechanisms (i.e., phase A and phase B) occurring during oscillations: v_e - electron velocity, v_h - hole velocity, $N_{effective}$ - effective charge concentration, E - electric field, and $v_{e,sat}$, $v_{h,sat}$ - electron and hole saturation velocities.*

4.2.2 Simulations at the beginning of the oscillations

In the following, the device is evaluated when the oscillations are diverging with time, rather than being constant in amplitude as before. One difference from before is that the oscillation amplitude experienced by the IGBT is smaller. Therefore, the electric field distortions and carrier profile distributions may differ from the ones presented before. To illustrate this, a time-zoom of Fig. 4.1 between the time instants 3.9 μs and 4.15 μs can be observed in Fig. 4.12. This graph closely resembles the phase-shift relation between each electrical parameter as shown in Fig. 4.3. Also, the instantaneous input capacitance is continuously varying; the highest capacitance value is observed when V_{CE} falls, on the contrary, the lowest values can be seen when V_{CE} rises.

The IGBT is evaluated at the time instants highlighted in Fig. 4.12. The electric field and the carrier distribution profile are plotted in Fig. 4.13. By looking at the time instants t_0, t_4 and t_5, it is evident that the electric field at the emitter is strongly associated with a low electron charge density in this region, that is essentially the reason why the input capacitance value is smaller. The opposite situation exists with regard to the time instants t_1, t_2 and t_3. In this case, the voltage across the device is lower and the area under the electric field must be reduced. This turns out in a weaker electric field at the emitter of the IGBT, associated with a charge-storage effect and a capacitance increase. In summary, it can be concluded that the same behaviour is observed at the beginning of the oscillations, though, the collector voltage is not sufficiently high to increase the carrier drift velocities for counteracting the charge-storage effects and thus the Kirk Effect.

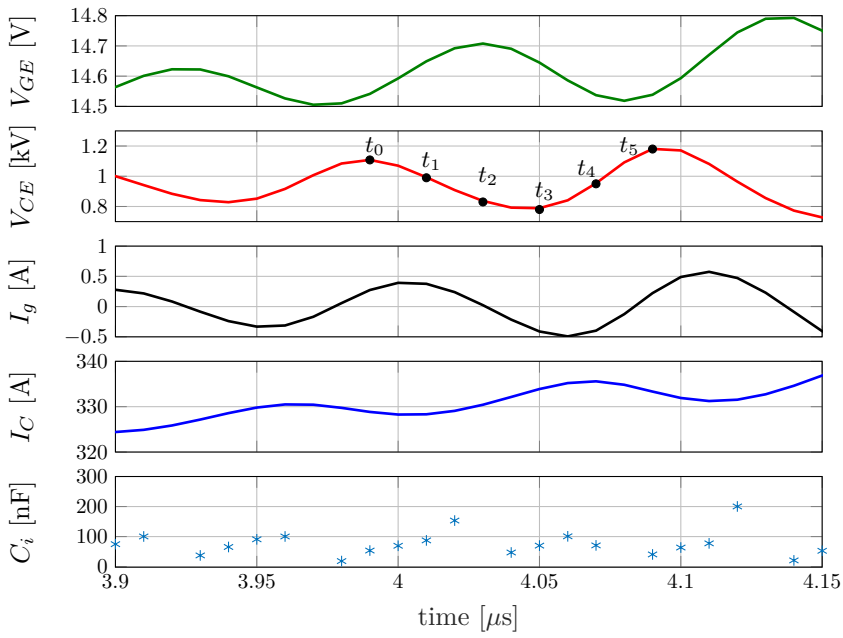

Figure 4.12: *Time-zoom of Fig. 4.1 showing the two phases (A and B) taking place during one oscillation cycle, together with the corresponding instantaneous gate capacitance C_i.*

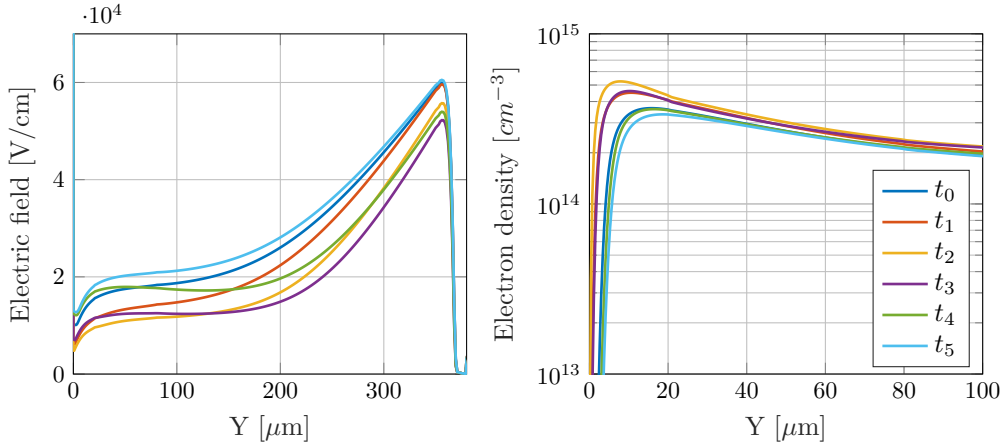

Figure 4.13: *Electric field variation (left) and electron density profile (right) in the planar IGBT at the time instants illustrated in Fig. 4.12.*

4.3 Parametric Oscillations in IGBTs

The results from the mixed-mode simulations have demonstrated that during the oscillations, the instantaneous input capacitance behaves as a time-varying element. Based on this observation, the oscillating gate capacitance together with the series-connected gate resonance circuit gives rise to an energy transfer between the IGBT's input capacitance and the gate inductance. The amplification behaviour arises from the capacitance variation in time, rather than the IGBT cell behaving as an amplifier. This type of amplification has been studied in other fields, and it is commonly known as a parametric oscillation. One example, which gained great popularity in the microwave design, consists on the implementation of a parametric amplifier with a varactor, whose non-linear variable capacitor element is used to amplify [60].

The non-linear equations describing the IGBT model together with the external circuit take a complex form; on the other hand, the interpretation of such an amplifying phenomenon is more obvious through simulations. Therefore, this latter approach is adopted in the following. To validate the proposed hypothesis, a PSpice simulation has been built in order to justify how oscillations can diverge with time. Fig. 4.14 shows the circuit implemented in PSpice, where the gate circuit is represented with resistive/inductive elements connected in series with two capacitors. One fixed capacitor representing the lower value, and a switched one, mimicking the capacitance variation in case of charge accumulation. The voltage across the two capacitances is ensured to be the same with the regulated voltage supply ($V(A) = V(A')$). The gate inductance value has been selected in agreement with the value from the TCAD simulation (i.e., 40 nH), a small resistor is included to simulate circuit losses and the values of the two capacitances have been selected one 50% larger than the other.

With the results from the TCAD simulations, it has been discovered that the gate

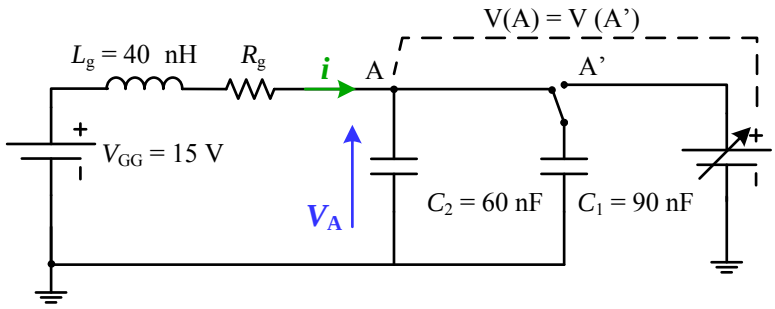

Figure 4.14: *PSpice simulation using switched capacitors to model the amplification behaviour observed in IGBTs during short circuit.*

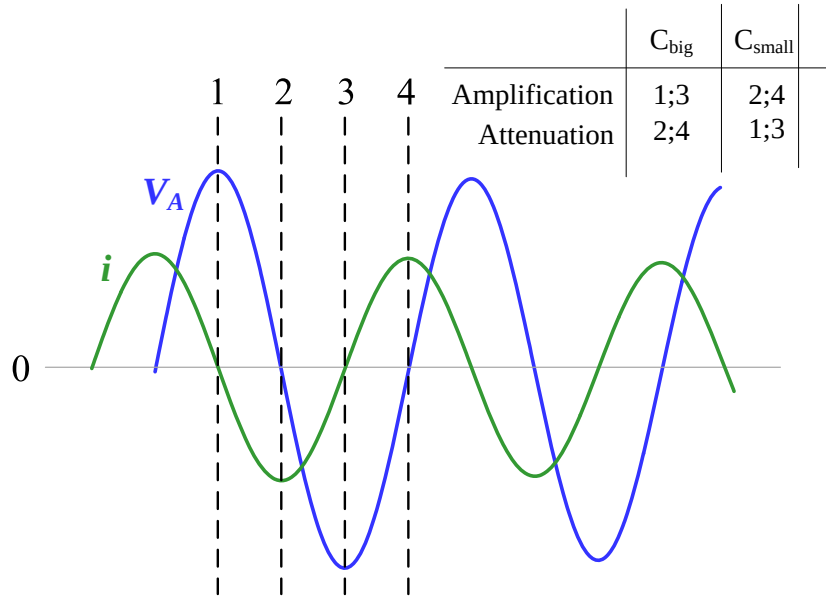

Figure 4.15: *Current and voltage waveforms of a typical LC circuit showing the time instants at which the capacitors need to be changed.*

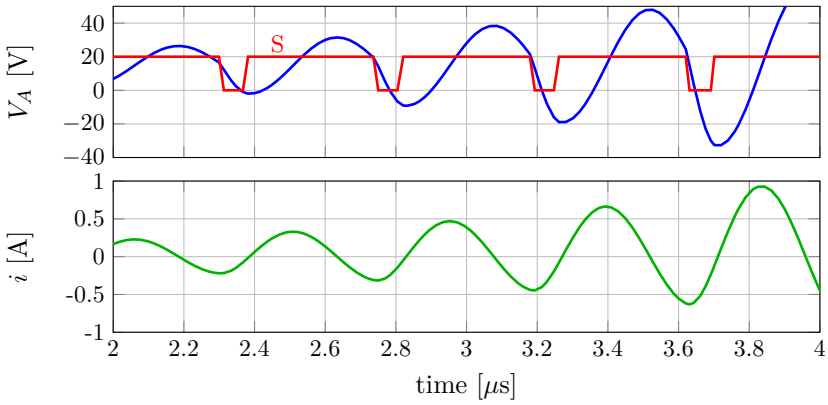

Figure 4.16: *Simulation of oscillations diverging with time. The function S, multiplied by 20, represents the switching between the low (S=0) and high capacitance (S=1).*

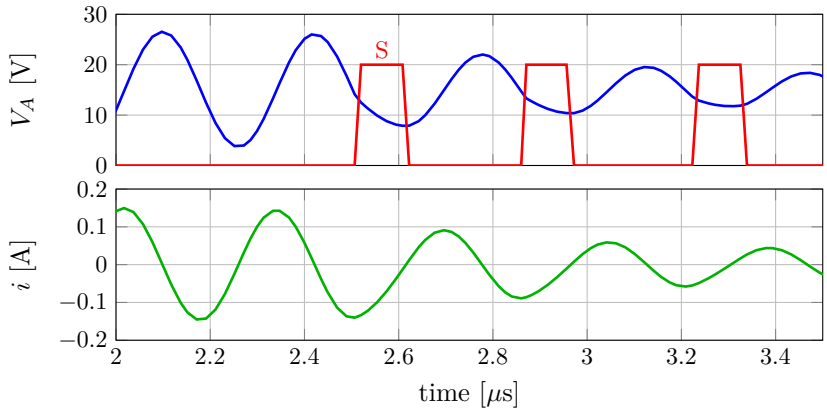

Figure 4.17: *Simulation of oscillations attenuated with time. The function S, multiplied by 20, represents the switching between the low (S=0) and high capacitance (S=1).*

capacitance varies in time as a result of the electric field variations inside the n-base of the IGBT. As a result of the capacitance variation (i.e., inflow and outflow of energy), the gate voltage oscillates increasing its amplitude in time. Based on this insight, the gate voltage oscillation phenomena can be modeled by alternatively switching two capacitances, carefully selecting the time instants at which the capacitors need to be changed.

The time switching instants are very crucial to have an amplification or attenuation of the signal, hence, the graph in Fig. 4.15, which represents the current and voltage waveforms of an LC circuit, will help to explain the concept. During one oscillation period, there are four energy transfers between the inductor and the capacitor, represented in Fig. 4.15 as 1, 2, 3 and 4. At the time instants 1 and 3, the current in the circuit is zero, this means that no energy is stored in the inductor and the capacitance is fully charged. At the time instants 2 and 4, we have the opposite situation; the current reaches its maximum value, thus, the capacitance is discharged and the energy is stored in the inductance. Hence, for a capacitance that varies periodically, the maximum energy increase in the circuit occurs if the capacitance is changed from a small to a big value at the time instants 1 and/or 3, and it is changed again to a small value at the time instants 2 and/or 4. It is particularly important that the capacitance has a large value when all or most of the total energy is stored in the capacitance. Thus, later in time, when all the energy is stored in the inductance and the capacitance is switched to a small value, the voltage signal will be amplified because the same energy has to be stored in a smaller capacitance. With the aim of representing the capacitance variation observed with the device simulations in Fig. 4.3, the highest and lowest capacitance

values are selected at the time instants 3 and 2, respectively. The use of a variable capacitance that reacts non-linearly with the mentioned time sequence is highly effective. A non-linear oscillatory behaviour, whose amplitude increases with time is demonstrated in Fig. 4.16. The current i and the voltage V_A are shown, as well as the function S that represents the switching between the low and high capacitance values, where the higher value of S corresponds with the big capacitance.

To prove that the selected timings are crucial, the opposite situation is simulated in PSpice. In this case, the capacitance is changed to a large value when the energy is stored in the inductance (i.e., point 2) and switched to a small capacitance when the inductance has no energy (i.e., point 3). As expected, Fig. 4.17 demonstrates that the signal is attenuated.

The oscillation frequency of the PSpice simulation, which is basically an LC circuit, is about 2.25 MHz. The oscillation frequency can be analytically calculated as follows:

$$f = \frac{1}{2 \cdot \pi \sqrt{LC}} = \frac{1}{2 \cdot \pi \sqrt{40e-9 \cdot 90e-9}} = 2.65MHz \tag{4.1}$$

This means that in order to obtain a similar oscillation frequency as the TCAD simulations, the capacitance must be smaller than the selected value. However, the value of the capacitance itself does not interfere with the hypothesis presented here, as long as the capacitance has a time-varying characteristic.

To sum up, in the TCAD simulations, the capacitance varies as a result of the electric field variation and charge profile distribution; in the PSpice simulation the capacitance variation is controlled with a voltage supply, i.e., S function in Fig. 4.15. The transition from low to high capacitance is done when the energy is being transferred from the capacitance to the inductance. This, in turn, causes the dV_A/dt to slow down because the capacitance increases in agreement with the results from the TCAD simulation. On the other hand, the transition from the high to low capacitance is done when the energy is transferred back to the capacitance, thus the voltage V_A increases its amplitude because a higher energy has to be stored in a smaller capacitance.

4.4 Design Features for Improved Short Circuit Robustness

The mechanism leading to the occurrence of oscillations is the weak electric field gradient at the emitter side of the IGBT. In order to adjust the electric field across the n-base in a way that it is beneficial for mitigating the short-circuit oscillations, two design measures are proposed in the following. The effectiveness of the proposed design solutions is validated by means of mixed-mode device simulations for the 3.3-kV planar IGBT cell.

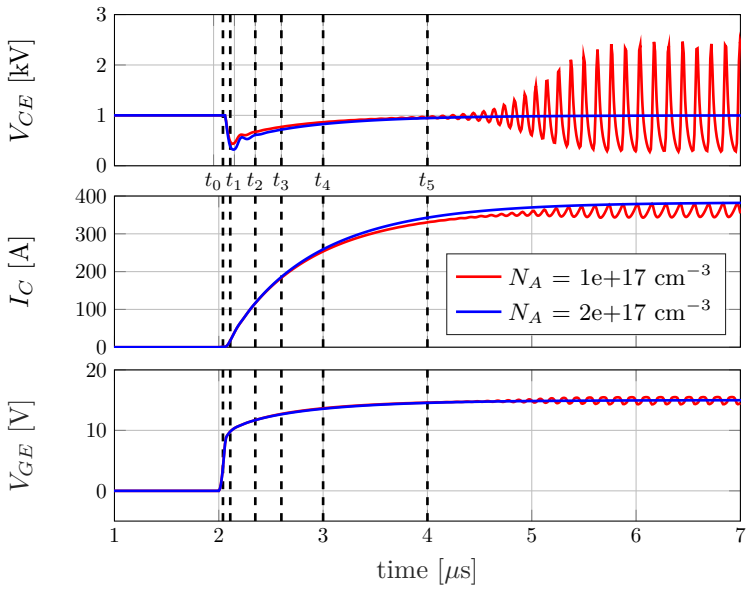

Figure 4.18: *Short-circuit simulations of the 3.3-kV IGBT at V_{CE} = 1000 V, with different collector doping concentrations.*

4.4.1 Collector dependence

One option to make the electric field stronger at the surface of the IGBT is to vary the emitter efficiency, $\gamma_{emitter}$, by changing the hole injection from the IGBT. This can be done by increasing the peak doping concentration of the p^+ collector. By increasing $\gamma_{emitter}$, the amount of holes injected will be higher and the net effective charge $N_{effective}$ will also increase ($N_{effective}$ = N_D + h - e). As a consequence, the electric field peak at the collector decreases due to the higher injection of holes, this means that the electric field strength at the emitter side must increase to compensate for the loss of area under the electric field curve at the opposite side of the cell, to support the same collector voltage. The result is that the Kirk Effect is counterbalanced.

Fig. 4.18 shows the short-circuit simulations of a 3.3 kV planar IGBT by employing different collector doping concentrations of 1e+17 cm^{-3} and 2e+17 cm^{-3}. It is evident that the method of increasing the collector peak doping concentration is effective in eliminating the oscillations. The electric field and electron density distributions have been evaluated at the time instants highlighted in Fig. 4.18, to better understand the validity of the adopted method. By looking at the waveforms in Fig. 4.19, higher emitter efficiencies in IGBTs result in stronger electric fields at the surface of the IGBT. This means that the carrier drift velocity, which is field dependent for low electric

fields, is higher at the surface when compared with the results having a peak collector concentration of 1e+17 cm^{-3}. The benefit is that the higher drift velocity at the emitter reduces the possibility of charge-storage effects, which could turn the input capacitance into a time-varying element. As can be seen in this case, the higher collector current is not necessarily important, but the shape of the electric field and thus the carrier profile distribution is crucial to determine whether the IGBT will oscillate or not.

4.4.1.1 On-state and turn-off losses

The improvement of the short-circuit robustness, typically comes with some compromises with respect to normal operation. By increasing the hole injection, the carrier distribution profile is modified in a way that the IGBT builds up a denser plasma near the collector. This means that turn-off losses will considerably increase.

Fig. 4.20 presents the typical forward characteristics at V_{GE} = 15 V, for the two IGBT designs having different collector doping doses. It is observed that for the nominal current of 50 A, the IGBT with the highest collector doping concentration shows a smaller on-state voltage, about 20 % reduction, in the on-state curve. The easiest way to understand this is by looking at the carrier distribution profiles and electric field shape of the two IGBT designs, when the collector current is 50 A. Fig. 4.21 shows a vertical cut along the highest current density region, demonstrating that a denser carrier concentration, especially near the collector, is observed. This lowers the resistivity of the n-base leading to smaller on-state voltage.

Additionally, the turn-off losses have been evaluated by means of mixed-mode simulations at the nominal conditions, that is 1800 V collector voltage and 50 A collector current. The gate resistance and the load inductance have been chosen as 10 Ω and 2400 nH, respectively. The results from the TCAD simulation alongside with the calculated turn-off power loss are shown in Fig. 4.22. As expected, by increasing the peak collector doping concentration, a higher turn-off tail current is observed, which increases the turn-off losses of the IGBT and therefore the heat generated.

4.4.2 Surface-buffer layer solution

The gradient of the field dE/dy over the region near the emitter, can be increased by inserting an n-doped buffer layer. With this method, the carrier distribution is adjusted in a way that, the negative effective charge previously observed during short circuit, becomes now positive (N_{eff}>0). The surface-buffer layer has been effectively employed by means of simulations in the 3.3-kV planar IGBT. However, this method is accompanied by a decrease of the device blocking capability. In order to select a design for an optimum trade-off between maximum blocking capability and short-circuit oscillation mitigation, the depth and doping level of this layer has been investigated.

Fig. 4.23 compares the doping profiles of four versions: (a) the standard 3.3-kV planar IGBT without the surface-buffer layer, (b) the 3.3-kV planar IGBT with an n^+

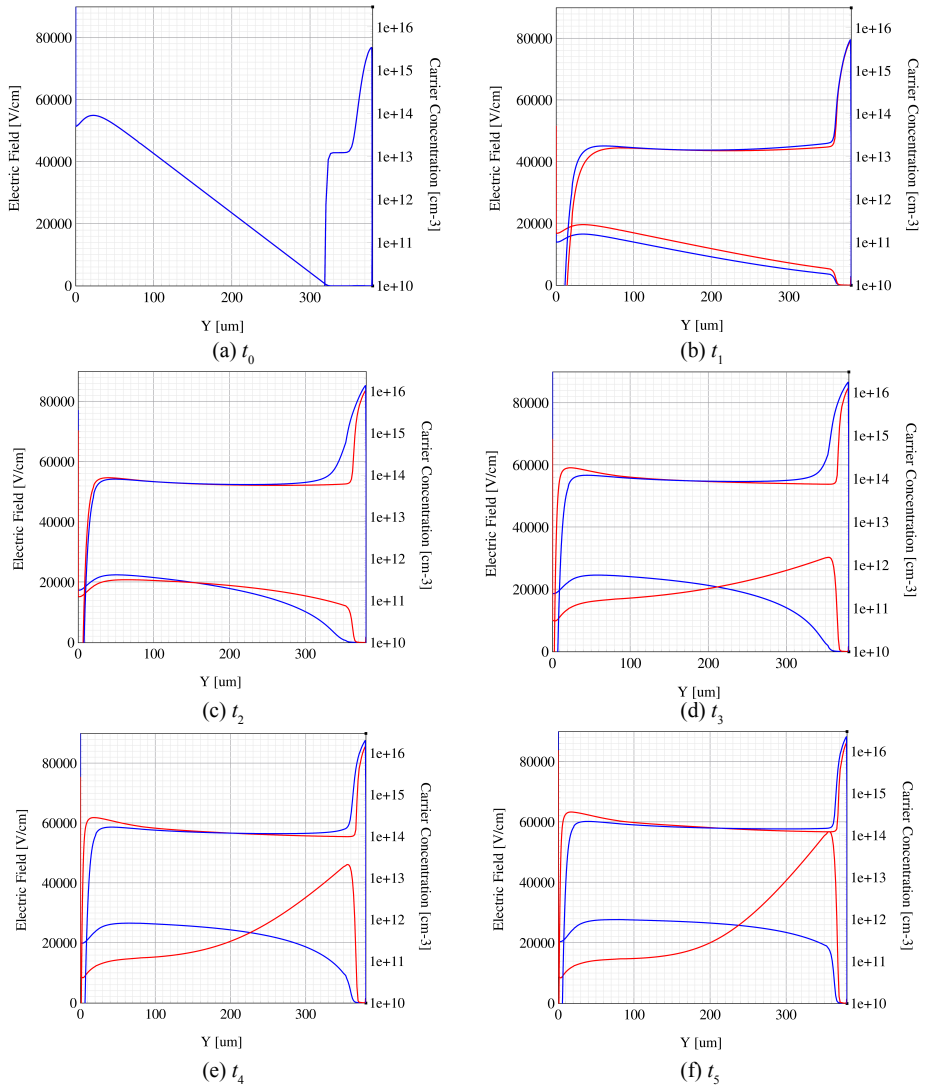

Figure 4.19: *Simulated electric field and electron concentration at different time instants along a cut in the vertical direction of the IGBT at $x = 30\ \mu m$. Operating conditions can be observed in Fig. 4.18.*

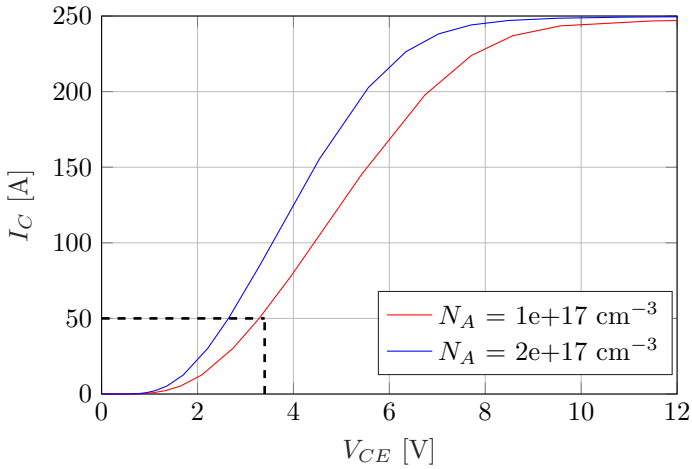

Figure 4.20: *Static characteristics of the 3.3-kV planar IGBT as a function of the peak collector doping concentration.*

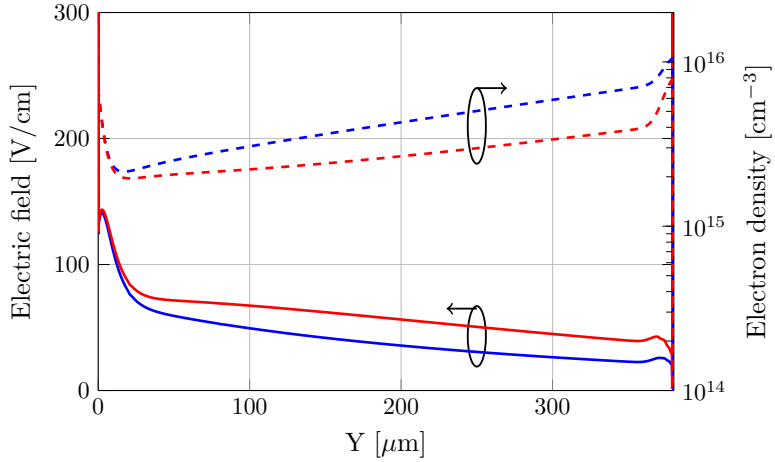

Figure 4.21: *Simulated electric field and electron density of the 3.3-kV planar IGBT as a function of the peak collector doping concentration. N_A = 1e+17 cm^{-3} (red lines) and N_A = 2e+17 cm^{-3} (blue lines).*

doping level of 8e+13 cm^{-3} over a depth of 100 μm, (c) the 3.3-kV planar IGBT with an n^+ doping level of 2.5e+13 cm^{-3} over a depth of 100 μm, and (d) the 3.3-kV planar

IGBT with an n^+ doping level of 8e+13 cm^{-3} over a depth of 50 μm. To illustrate the doping profile differences among the four versions, a vertical cut has been done between adjacent cells or pin-region, with the purpose of avoiding the p-base and n-source layers, which have been kept unmodified.

Short-circuit simulations have been done to prove that the n-doped buffer layer is valid to mitigate the oscillations. Fig. 4.24 shows the comparison between the standard planar IGBT, which exhibits oscillations, while the IGBT employing a surface-buffer layer no longer oscillates. As can be seen in this case, the selected design has the highest doping level and also the deepest design. A further comparison in terms of short-circuit oscillation occurrence between the three versions, is provided to justify which design gives the more robust operation during short circuit.

Fig. 4.25 shows the simulated voltage and current waveforms at the same conditions and with the same stray elements for the three surface-buffer layer designs. Apparently,

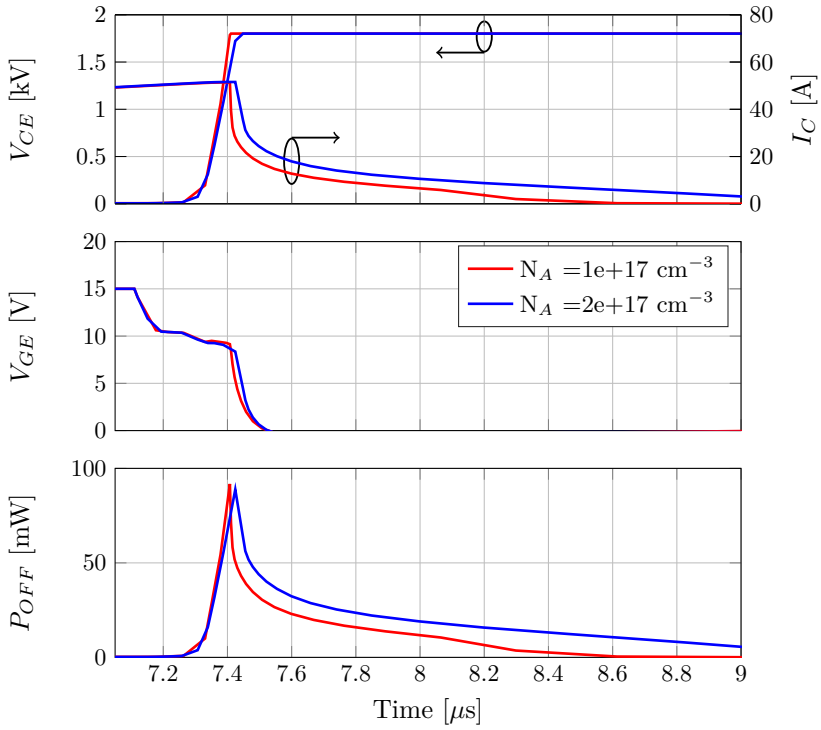

Figure 4.22: *Simulated turn-off current and voltage waveforms of the 3.3-kV IGBT with different emitter efficiencies. The turn-off power loss is also calculated.*

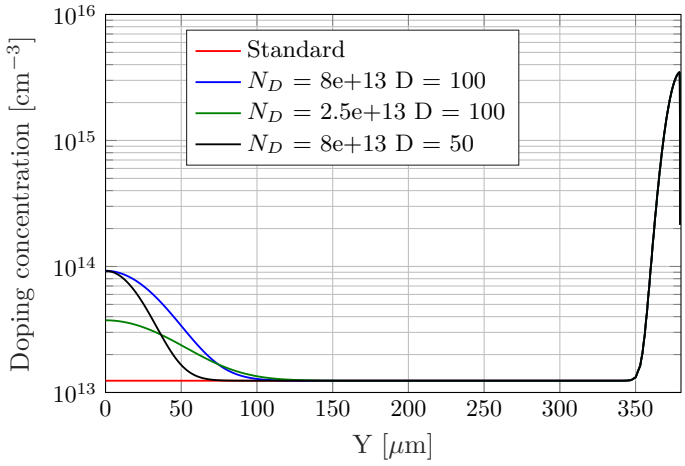

Figure 4.23: *Doping profile comparison between a standard 3.3-kV planar IGBT and the same IGBT with three surface buffer layer design versions. N_D is the doping level and D is the depth of the n^+ layer.*

the three versions result in an improved short-circuit performance without undesirable oscillations. A closer look can be obtained in Fig. 4.26, where a small oscillation is noted when a shallower or low n^+ doping levels are employed. This small oscillation can remarkably be amplified, if a higher stray inductance exist in the gate circuit, e.g. in this case a 40 nH gate inductance has been used. This statement is in agreement with the experimental results in Chapter 2 and the sensitivity analysis carried out on the gate inductance by means of TCAD simulations in Chapter 3. It can be concluded that the best design is the one having a higher doping level (i.e., 8e+13 cm^{-3}) over a depth of 100 μm, which effectively reduces the possibility of having oscillations. Therefore, this design will be considered hereafter, when comparing the static and dynamic performances with respect to the standard IGBT.

4.4.2.1 The electric field and charge balance during short circuit

In order to study the effects of both device and operating condition parameters, mixed-mode simulations showing the electric field and charge balance distributions during short circuit are presented. Fig. 4.27 shows a cut along the vertical direction of the IGBT comparing the physical quantities between the standard IGBT and the one including the selected surface-buffer layer. The time instant at which the cut has been done is just before the oscillations are triggered for the standard IGBT, i.e., t = 3 μs in Fig. 4.24. The figure shows the electric field (solid line) together with the electron

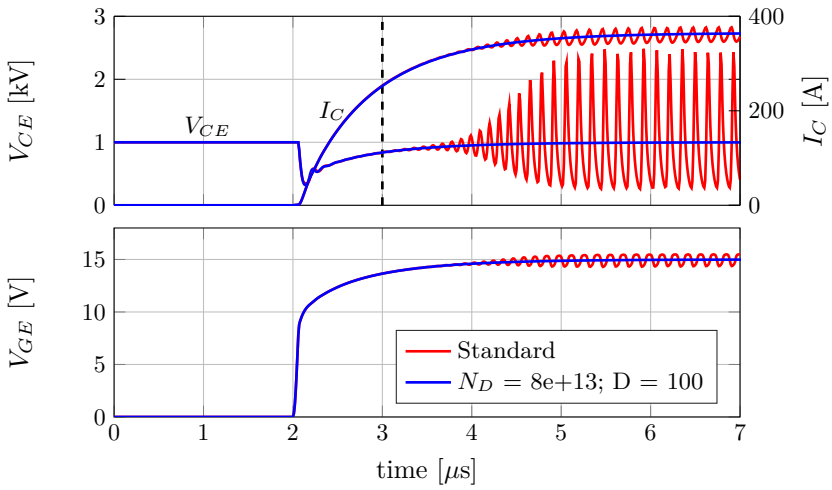

Figure 4.24: *Short-circuit simulation illustrating the voltage and current waveforms of the standard IGBT and the one including the surface-buffer layer.*

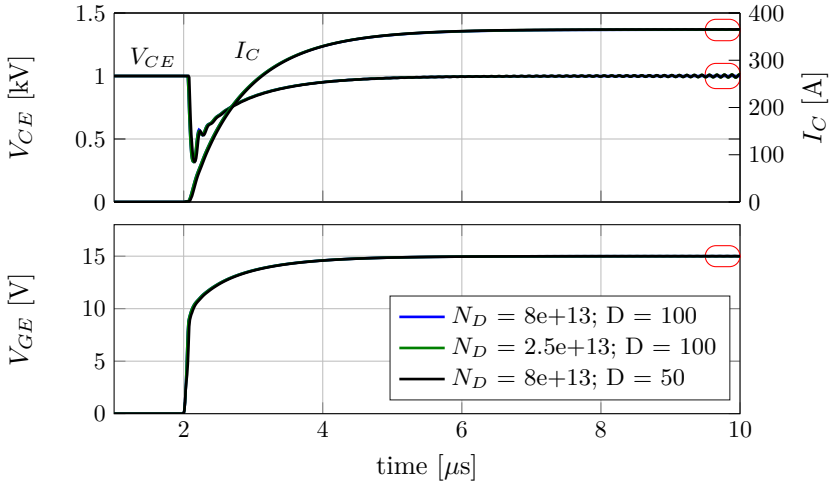

Figure 4.25: *Short-circuit simulations of the three investigated designs. The red circles indicate the zoomed regions represented in Fig. 4.26. N_D is the doping level and D is the depth of the n^+ layer.*

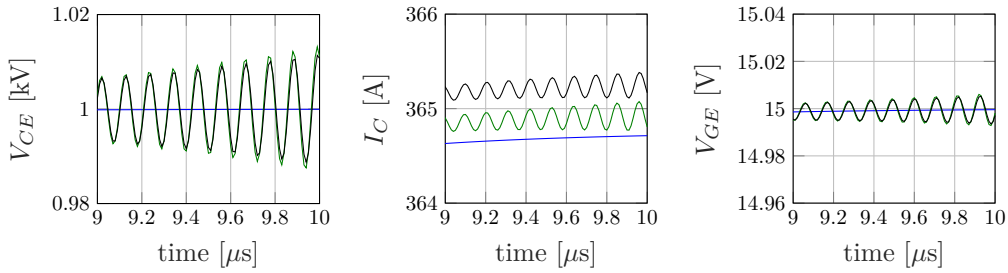

Figure 4.26: *Zoomed view of the voltage and current waveforms in Fig. 4.25: collector voltage (left), collector current (middle) and gate voltage (right).*

carrier profile (dashed line), where the electric field is effectively increased at the emitter side, by employing the surface buffer n-doped layer. In this case, the electron density is smaller at the surface, as the stronger electric field pushes the carriers out from the emitter side into the middle of the n-base region. In this way, the electric field does not strongly depend on the injected electrons from the MOS-channel, the background doping concentration is more dominant, and the electric field does not vary with increasing short-circuit time (the capacitance becomes fixed).

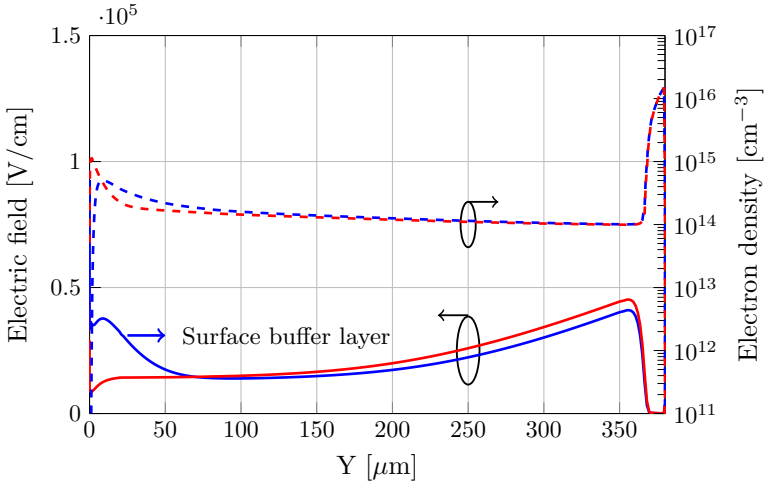

Figure 4.27: *Simulated electric field and electron density of the standard IGBT (red line) and the IGBT with the surface-buffer layer design (blue line), at the time instant highlighted in Fig. 4.24.*

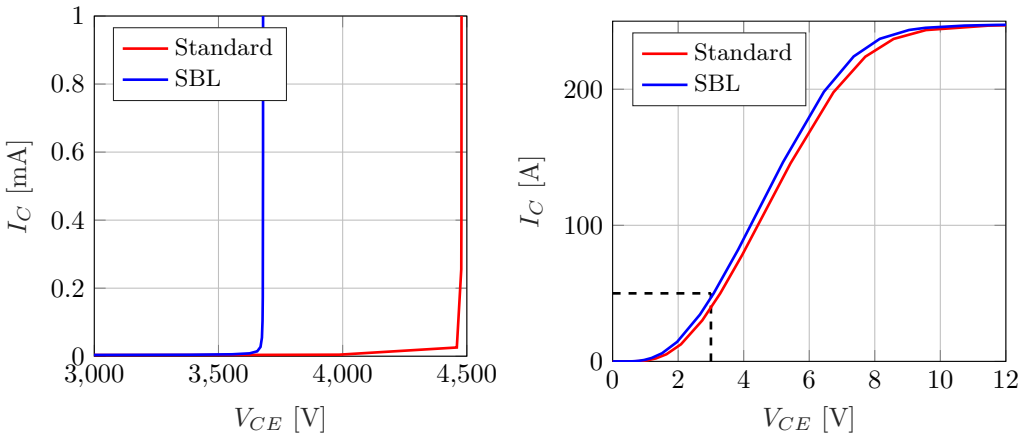

Figure 4.28: *Simulated forward blocking capability (V_{GE} = 0 V) (left) and typical I-V forward characteristic (V_{GS} = 15 V) of the standard IGBT and the one employing the Surface-Buffer Layer, SBL (right).*

4.4.2.2 Blocking capability

After having discussed the benefits of the n^+ surface-buffer layer, the typical off-state I-V characteristics (V_{GE} = 0V) of the standard and the proposed IGBT designs are evaluated. Fig. 4.28 compares the forward blocking characteristics of these devices at 25°C through TCAD simulations. It can be understood that for the standard 3.3-kV planar IGBT, after V_{CE} = 4,460 V, a sharp increase of the collector current is observed. The breakdown voltage is substantially larger than the rated blocking voltage of the IGBT, allowing for a large margin to guarantee the correct operation of the IGBT up to 3.3 kV, without any initiation of breakdown mechanisms. On the other side, the proposed IGBT including the Surface-Buffer Layer (SBL) is accompanied with a reduced blocking capability of 3,700 V, which may not be acceptable for the real application. In short, when compared to the standard IGBT, the adopted SBL design has proven to mitigate the short-circuit oscillations, but it comes with a 17% reduction in breakdown voltage for the most aggressive SBL design.

4.4.2.3 On-state and turn-off losses

The trade-off curve between on-state losses and turn-off losses, typically named as the technology curve, has been evaluated by means of TCAD simulations. Fig. 4.28 compares the typical forward characteristics (V_{GE} = 15 V), for both standard and Surface-Buffer Layer (SBL) IGBT designs. From this graph, one can appreciate that for a collector current of 50 A, which is the nominal current of the 3.3-kV IGBT, the IGBT

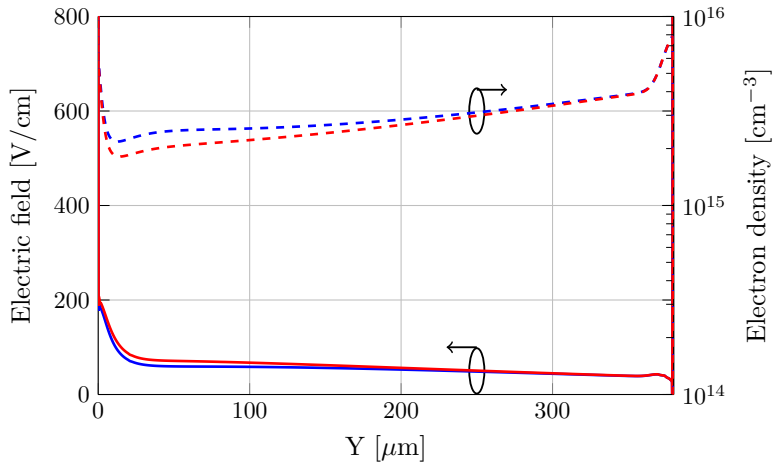

Figure 4.29: *Simulated electric field and electron density during on-state for the standard 3.3. kV planar IGBT (red line) and with the SBL design (blue line).*

with the SBL design shows a smaller voltage drop, about 6% reduction, in the on-state curve. The reason for this can be observed in Fig. 4.29, where a denser electron density, especially at the emitter of the IGBT, can be observed when the SBL design is adopted. Note that the conduction losses in the IGBT are controlled by the carrier distribution in the whole thickness of the device, thus the observed higher plasma density, justifies why the on-state losses are reduced.

To evaluate the turn-off losses, mixed-mode device simulations have been performed under a DC-link of 1800 V (i.e., the nominal voltage of the IGBT) and collector current of 50 A. The gate resistance and the load inductance have been chosen as 10 Ω and 2400 nH, respectively. The results from the TCAD simulation along with the calculated turn-off power losses are shown in Fig. 4.30. Here, it can be observed that the SBL design contributes insignificantly to the turn-off losses. The reason for having similar turn-off losses can be justified by looking at the excess carrier at the collector side, simulated in Fig. 4.29. Since the excess carriers are of the same level for both devices, the tail current at turn-of is not modified. The overall result is that the proposed new design brings a favorable technology curve, when compared to the equivalent standard IGBT.

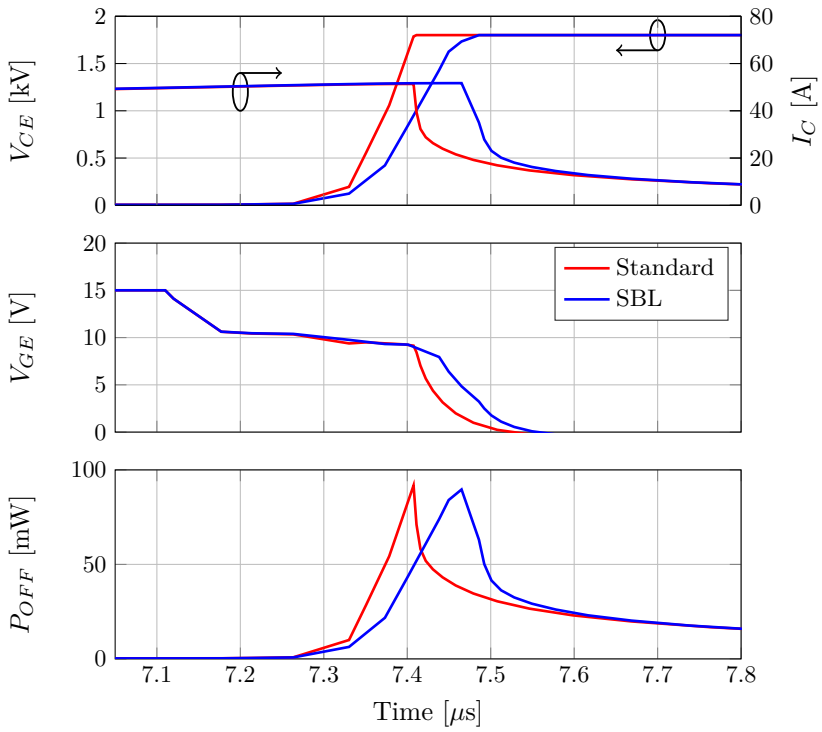

Figure 4.30: *Simulated turn-off current and voltage waveforms of the 3.3-kV IGBT with the standard and SBL design. The turn-off power loss is also calculated.*

4.5 Conclusion of this Chapter

In this chapter, a detailed study of the short-circuit oscillation phenomenon limiting the ruggedness of IGBTs has been provided. Firstly, the short circuit performance of a planar and a trench IGBT cell has been simulated, confirming that the oscillations can be observed for both topologies. Secondly, it has been found that the carrier drift velocities have a strong impact on the charge balance of the IGBT, especially at low DC-link voltages when oscillations are typically observed. During a short circuit event at a low DC-link voltage, the electric field strength in the n-base will be low, and especially weaker at the emitter of the IGBT, mainly due to the observed Kirk Effect. The drift velocities will be in a range where they are not saturated, and thus field dependent, which in turn causes electron accumulation effects at the emitter of the IGBT, due to the substantially lower electron drift velocity in this region. As a major achievement

of this work, it is possible to relate the electric field distortions to gate capacitance variations, and associate the capacitance variation with charge-storage effects occurring at the surface of the IGBT, arising from the low carrier velocities. On the other hand, at high DC-link voltages, the carrier drift velocities become close to its saturation value across the n-base, which means that the charge-storage effect is no longer present, thus, the input capacitance becomes fixed.

It has been pointed out for the first time that a parametric oscillation takes place during the IGBT short circuit, whose time-varying element is the Miller capacitance, leading to an amplification mechanism. This hypothesis has been validated through a PSpice model, showing the typical behavior of parametric oscillators. Finally, it can be concluded that the proposed solutions i.e., the increase of the emitter efficiency and the adoption of an n-doped surface-buffer layer, have proven to be effective in IGBTs for bringing about the desired increase in the electric field at the emitter, resulting in an increase of the carrier velocity, which prevents capacitance variations.

Chapter 5

The Short-Circuit Performance in SiC Power MOSFETs

This chapter presents the experimental tests on the short-circuit withstanding capability of SiC power MOSFETs. The outcome of these results is important to understand which are the failure mechanisms and challenges that need to be faced, in order to further improve the SiC MOSFET robustness against severe conditions. The Short-Circuit Safe Operation Area (SCSOA) of today's discrete and multi-chip power modules for SiC MOSFETs will also be presented.

5.1 Introduction

Recently, the SiC power MOSFET has been launched into the market with ratings up to 1700 V for both discrete and multi-chip modules. While this new technology must overcome a number of challenges, there is no question that SiC MOSFETs are the most promising option for high-voltage applications. They provide low switching losses in combination with low conduction losses at high temperatures, alongside reduction in the size of the power electronic system [61]. This rises a competition between the SiC MOSFET and the widely used silicon IGBT. One of the key performance requirements for a new technology to be accepted is its robustness against severe overloads, where SiC MOSFETs are lagging behind. For example, the capability to withstand short circuit conditions, though not a normal condition but a frequent one, must be guaranteed to avoid downtimes and maintenance costs. Nowadays, discrete SiC MOSFET devices have proven to withstand short circuit conditions to some extent, a few of them up to

10 μs at half of the breakdown voltage and at room temperature [62–68]. The situation is more chaotic for SiC MOSFET power modules, in which several chips are arranged in parallel and the current imbalance between the paralleled chips are the stumbling block [69]. Thus, the aim of this chapter is to show the short-circuit withstand capability of state-of-the-art SiC MOSFETs for both discrete and multi-chip modules. Through this study, it is possible to identify failure precursor parameters, which help in two ways: (i) a prognostic methodology can be developed to predict the failure of the device, and (ii) hypothesis about the failure mechanism can be formulated, thus, the next steps in improving the short-circuit robustness in SiC MOSFETs can be established.

5.2 Short-Circuit Operation of Single-Chip SiC MOSFETs

The short-circuit behaviour of single-chip SiC MOSFET devices is experimentally investigated by using the non-destructive tester shown in Fig. 2.2. The tests have been carried out on 1200 V SiC MOSFETs, having two different nominal currents of 36 A and 90 A. All the experiments have been performed with the same gate-source voltage of V_{GS} = -5V/ 20V and gate resistance of R_g = 10 Ω. The short circuit failure was determined by increasing the short circuit pulse after each successful test in steps of 100 ns until failure. Different bias voltages from 200 V up to 800 V have been applied and case temperatures from 25°C up to 150°C.

5.2.1 Short-circuit assessment of 1.2 kV/ 36 A SiC MOSFET

Fig. 5.1 shows the short-circuit voltage and current waveforms of a 1.2-kV/ 36-A SiC MOSFET (C2M0080120D) for a low bias voltage of 400 V at a case temperature of 25°C. In these conditions, not the nominal ones, the SiC MOSFET is able to survive short-circuit pulse durations up to 10 μs. The results provide an initial insight into two failure precursors: (i) the occurrence of turn-off tail currents, highlighted in Fig. 5.1, and (ii) the gate-source voltage drop with increasing short circuit time, also highlighted in Fig. 5.1. The turn-off tail current amplitude increases for short-circuit pulses up to 5 μs, but after that, its amplitude appears to be clamped (e.g., 45 A), regardless the increasing short-circuit pulse and thus temperature. Previous works have attributed the turn-off tail currents to the amount of hole carriers thermally generated, that increases up to values for which the leakage current is high enough to cause a sufficiently large voltage drop across the n-source/p-body junction, leading to the activation of the parasitic *npn* BJT [43]. On the other hand, the gate-source voltage drop, about 0.5 V lower from its positive gate bias, suggests that a large leakage current is flowing through the gate, indicating that a gate-oxide degradation is present. The gate voltage drops more with increasing short-circuit pulses, which in turn means that it is function of the temperature

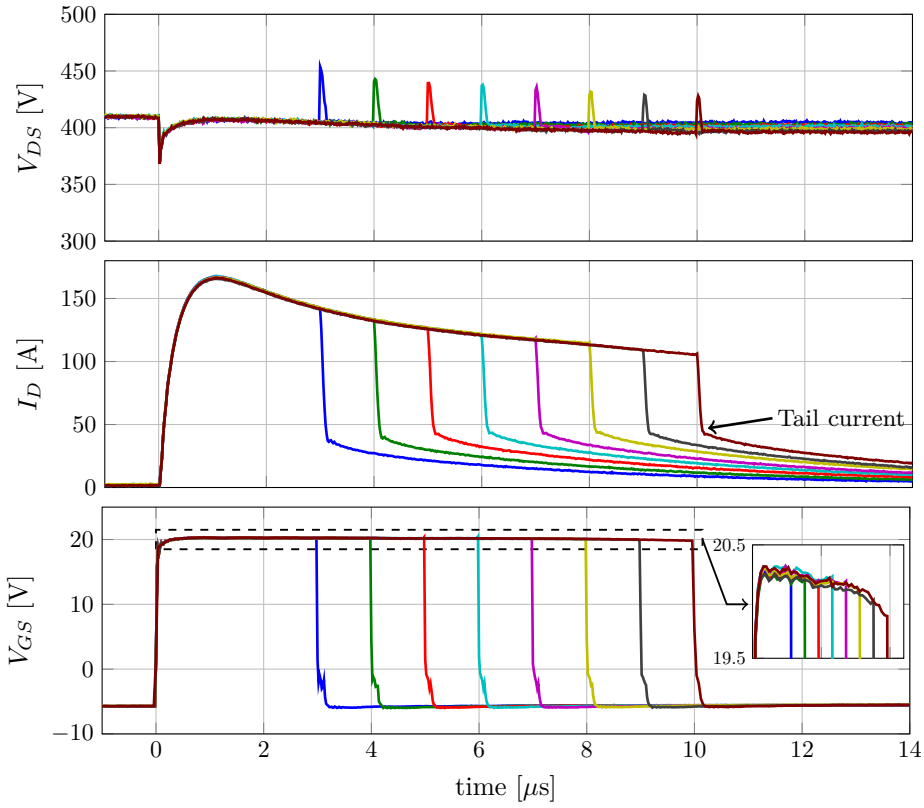

Figure 5.1: *Short-circuit tests of a 1.2 kV/ 36 A SiC MOSFET with V_{DS} = 400 V and T_{case} = 25 °C.*

of the device. The gate-oxide reliability has always been an issue in SiC MOSFETs, as it can be found in the literature [68, 70]. However, there is no conclusive theory about the failure mechanism and how to redesign the cell to make the gate-oxide more robust.

Furthermore, the results of the short-circuit tests carried out at 400 V bias voltage and at higher case temperatures of 25°C, 75°C, 100°C and 150°C of the 1.2 kV/ 36 A SiC MOSFET are observed in Fig. 5.2. The device survives 10 μs short-circuit, revealing the same failure precursors as before, i.e., turn-off tail currents and gate-source voltage fall at the end of the pulse. It is noticed that the short-circuit current peak decreases with increasing case temperatures, in agreement with the negative dependence between the channel mobility and temperature [11]. It is worth to mention that the current tail amplitude does not increase further as the case temperature is increased, however, the

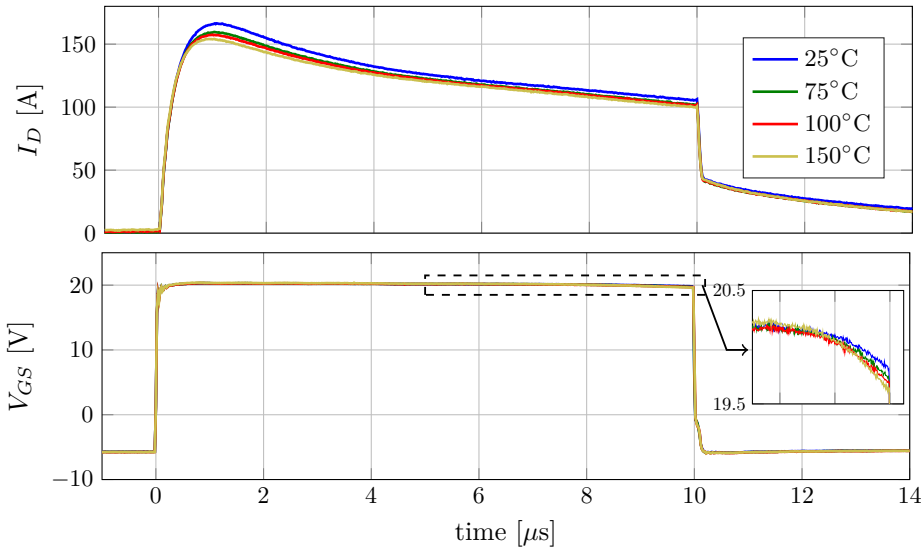

Figure 5.2: *Short-circuit tests of a 1.2 kV/ 36 A SiC MOSFET with V_{DS} = 400 V and t_{sc} = 10 μs at four case temperatures.*

gate-source voltage drops even more with increasing temperatures.

When the drain-source voltage is set to 600 V, the 1.2 kV/ 36 A SiC MOSFET fails within 5 μs at 25°C case temperature. As it can be seen in Fig. 5.3, the device is apparently able to turn off the short-circuit current, but after 1.5 μs, the drain current suddenly increases out of control, leading to the destruction of the device. The root cause of this delayed failure is unknown, but it seems that it is related with some sort of thermal instability due to hot-spot formation and local increase of temperature. This positive feedback leads to device destruction by thermal runaway [45].

During a second round of tests with the 1.2 kV/ 36 A SiC MOSFET, another type of failure mechanism has been observed. Fig. 5.4 shows a series of short-circuit tests, where the 1.2 kV/ 36 A SiC MOSFET fails within 7.2 μs at 600 V DC-link voltage and case temperature of 150°C. The last short-circuit pulses (i.e., t_{sc} = 6 μs and t_{sc} = 7 μs), indicate an important reduction of the gate-source voltage as well as drain current. It is observed that a gate-oxide degradation mechanism takes place leading to a permanent damage of the device, i.e., not reversible. Based on these results, it seems that high temperatures under high DC-link voltages can easily degrade the gate structure. It is a great advantage that the device shows an ageing indicator through the reduction of V_{GS}, this means that V_{GS} or I_D parameters can be monitored to early predict the failure of the device.

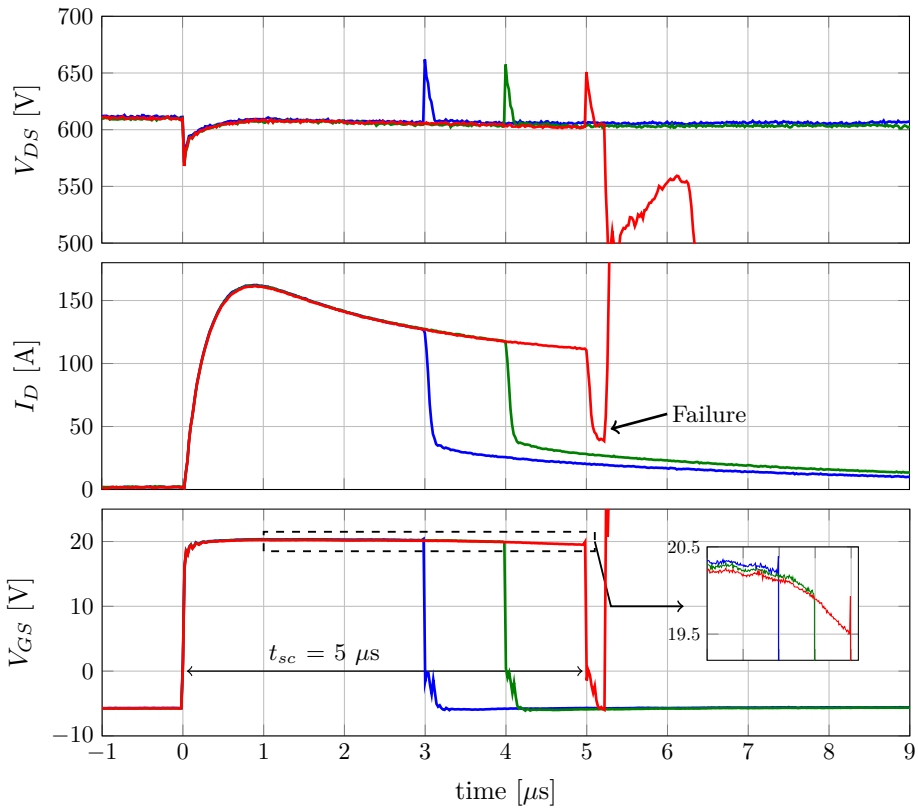

Figure 5.3: *Short-circuit failure of the 1.2 kV/ 36 A SiC MOSFET within 5 µs at 600 V DC-link voltage and 25° C case temperature.*

5.2.2 Short-circuit assessment of the 1.2 kV/ 90 A SiC MOSFET

In addition to the results presented before, further short-circuit tests have been performed for another family of 1.2 kV SiC MOSFETs, whose nominal current is 90 A (C2M0025120D). In Fig. 5.5, the short-circuit waveforms are presented with a DC-link voltage of 400 V and case temperature of 150°C. The 1.2 kV/ 90 A SiC MOSFET withstands short-circuit pulse durations up to 10 μs, at the expense of selecting a low DC bus voltage to fulfil with the expected short-circuit withstanding capability needed, thus the gate driver is able to protect the device. The results reveal that turn-off tail currents are also present for the 1.2 kV/ 90 A SiC MOSFET, whose amplitude increases with short-circuit pulse lengths up to 7 μs. The maximum tail current amplitude seems to stabilize about 100 A, approximately the nominal current of the device, and it does

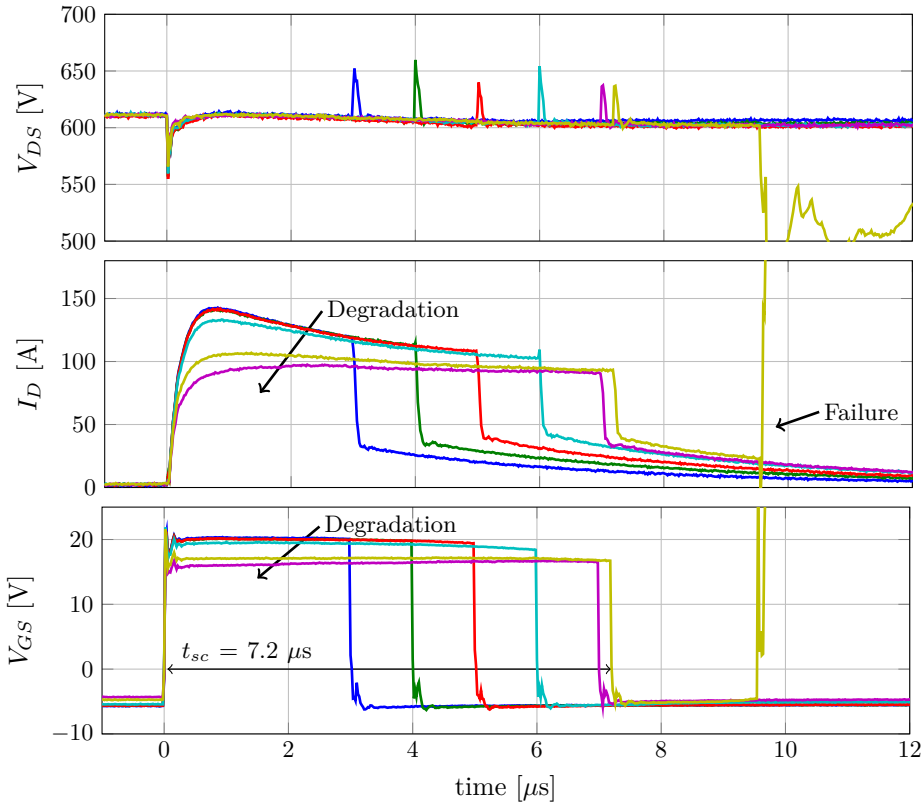

Figure 5.4: *Short-circuit failure of the 1.2 kV/ 36 A SiC MOSFET within 7.2 μs at 600 V DC-link voltage and 150° C case temperature.*

not further increase with short-circuit pulses longer than 7 μs. In addition, the gate-source voltage slightly falls at the end of the 10 μs pulse, however, the voltage drop in this case is only 0.26 V, substantially less than the voltage drop observed for the 1.2 kV/ 36 A SiC MOSFET devices.

To assess the short-circuit dependence of the 1.2 kV/ 90 A SiC MOSFET with temperature, the DC-link voltage has been kept at 400 V and the short-circuit time to 10 μs, while four different case temperatures of 25°C, 75°C, 100°C and 150°C are applied. The results in Fig. 5.6 reveal that the peak saturation current, reached at about 2 μs, strongly depends on the initial case temperature. It is observed that the higher the case temperature is, the lower the saturation current peak. This feature is beneficial for the stability of the device, especially for parallel configurations involving

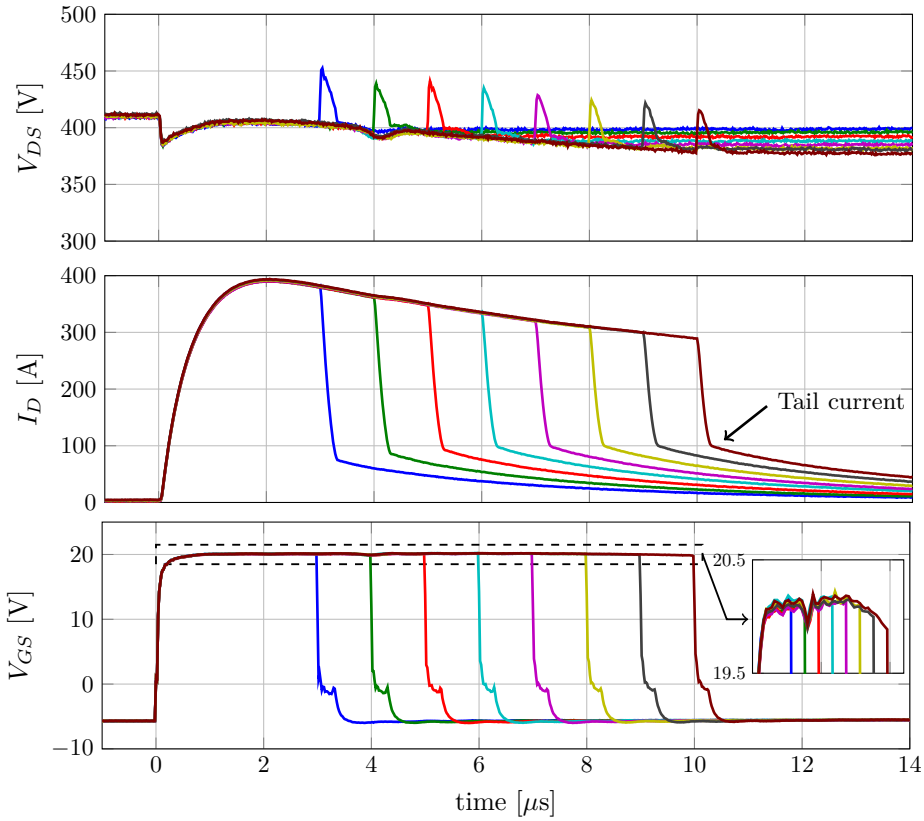

Figure 5.5: *Short-circuit tests of a 1.2 kV/ 90 A SiC MOSFET with V_{DS} = 400 V and T_{case} = 150 °C..*

many chips in parallel to achieve a higher current capability. Thanks to this negative temperature coefficient, the cells heating up more will draw less current, counteracting unbalanced heat distribution among paralleled chips and ensuring good current sharing. It is worth to mention this because the SiC MOSFET power modules tested later contain SiC MOSFET chips that have the same current and voltage ratings as the 1.2 kV / 90 A SiC MOSFET device presented here. When it comes to gate-oxide reliability, the gate-source voltage decrease becomes more critical as the case temperature increases, which means that a higher gate leakage current is expected as the temperature of the chip increases.

With the aim of approaching the nominal voltage of the device, a higher DC-link voltage of 600 V is chosen, while the case temperature is varied. Fig. 5.7 shows the

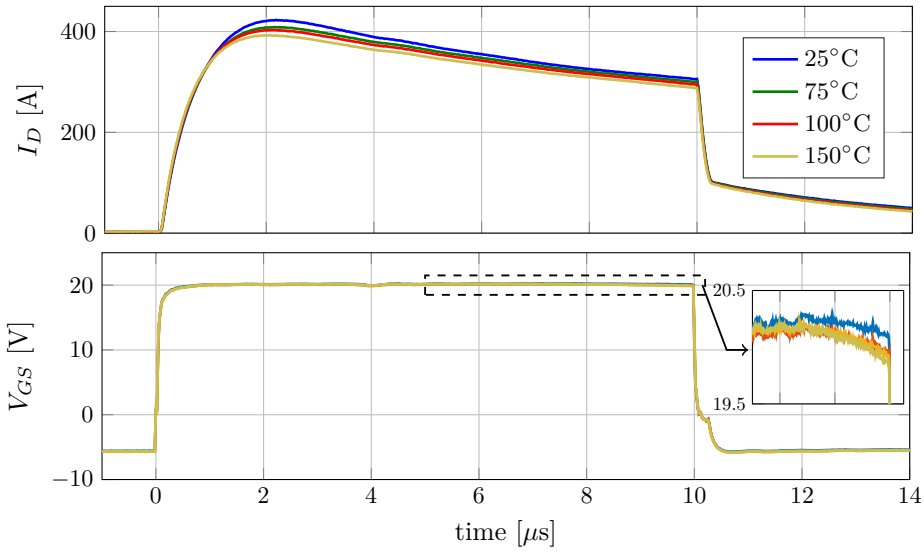

Figure 5.6: *Short-circuit tests of a 1.2 kV/ 90 A SiC MOSFET with V_{DS} = 400 V and t_{sc} = 10 μs at four case temperatures.*

performance of the 1.2 kV/ 90 A SiC MOSFET demonstrating that it survives a short-circuit condition up to 4 μs at 600 V and T_{case} = 150°C. However, during the last test at 150°C, the strong decrease in the gate-source voltage indicates that the gate-oxide insulation material may be damaged, which means that the point of no return has been reached. Beyond this point, it can be assumed that the device will catastrophically fail, as previously demonstrated in Fig. 5.4. Thus, the short-circuit test activity is not continued for higher DC-link voltages or longer pulses.

5.3 Short-Circuit Operation of Multi-Chip SiC MOSFET Power Modules

In recent years, several SiC MOSFET power modules have emerged into the market with current capabilities up to 400 A, principally driven by the challenging requirements for high power density and integration from the automotive industry [71]. One of the limitations of paralleling SiC MOSFET dies is the packaging technologies employed, but also the wide spread in SiC MOSFET parameters, e.g. threshold voltage, and the strong positive thermal coefficient of these devices [72, 73].

In this section, the results of the short-circuit robustness of SiC MOSFET power

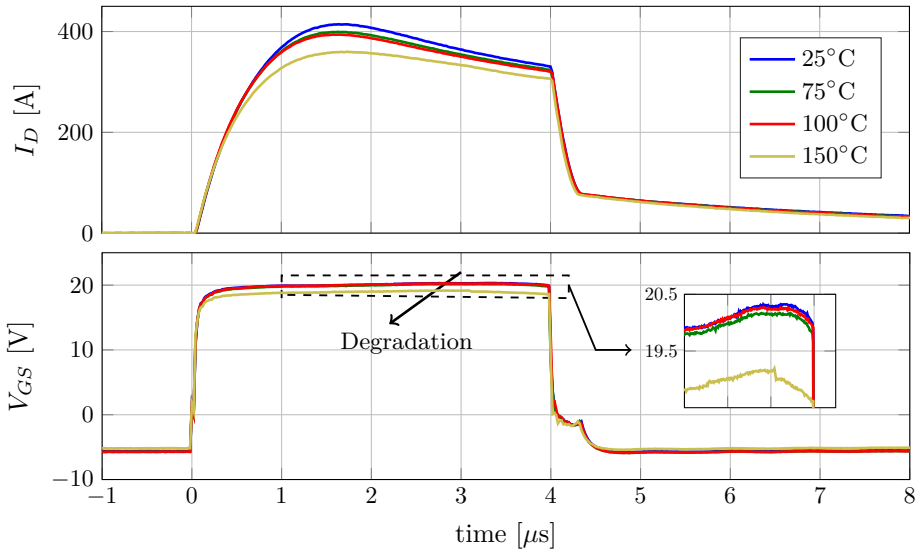

Figure 5.7: *Short-circuit tests of a 1.2 kV/ 90 A SiC MOSFET with V_{DS} = 600 V and t_{sc} = 4 μs at four case temperatures.*

modules will be discussed, some of these results have previously been presented in [69]. All the experiments have been performed with the same gate-source voltage of V_{GS} = -5V/ 20V and gate resistance of R_g = 10 Ω. Two SiC MOSFET power modules from different manufacturers rated at 1.2 kV are tested under different DC-link voltages and pulse durations until failure. The investigated devices normally fail during the turn-off transient or a few μs after the device successfully turns off the short-circuit current.

5.3.1 Short-circuit assessment of the 1.2 kV/ 300 A SiC power module

The short-circuit performance of the 1.2 kV/ 300 A SiC MOSFET (CAS300M12BM2) has been experimentally investigated. Fig. 5.8 shows two short-circuit events with increasing pulse durations for a bias voltage of 600 V and case temperature of 25°C. It can be observed that the device survived a single short-circuit pulse duration of 2.5 μs, however, the pulses were gradually increased until a short-circuit pulse of 3.2 μs causes the device failure. The SiC MOSFET power module is able to turn off the short-circuit current, but after 2 μs, the current increases out of control, this behaviour is typically known as a thermal runaway failure. Therefore, this is a clear indication that self-heating and thermal instability effects play a role in the failure mechanism. The

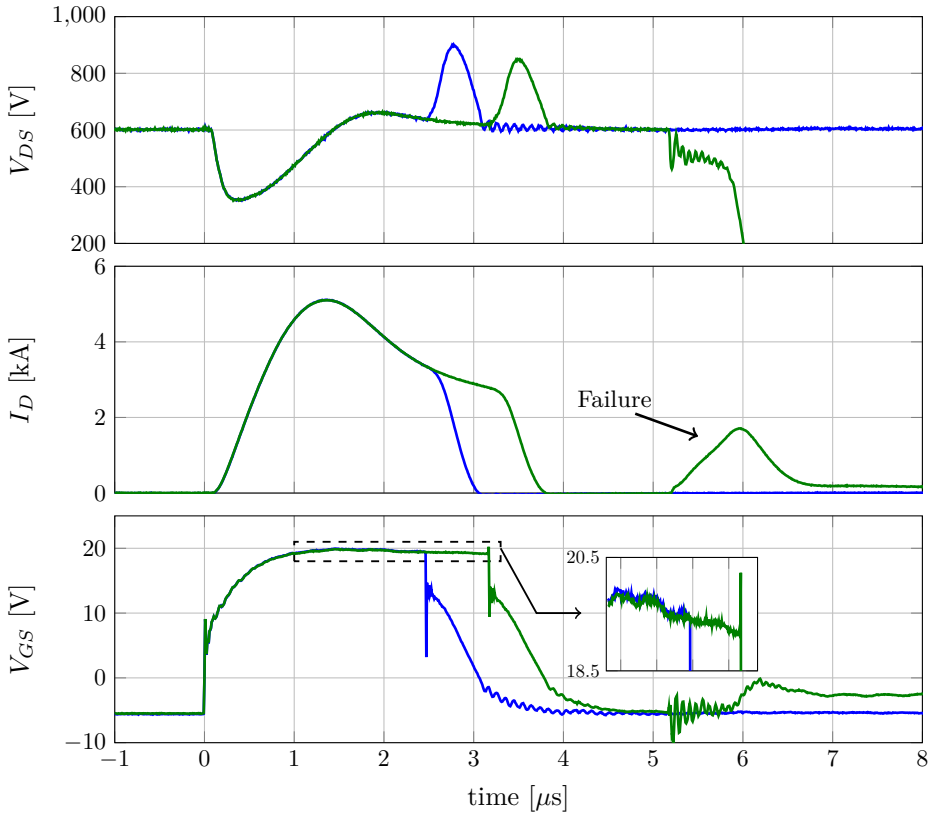

Figure 5.8: *Short-circuit failure of the 1.2 kV/ 300 A SiC power module within 3.2 μs at V_{DS} = 600 V and T = 25°C [69].*

significant decrease of drain current during the short-circuit event demonstrate that a self-heating effect takes place, however the thermal instability leading to the destruction of the device is not known. Previous studies on discrete devices have identified through finite-element TCAD simulations, that a thermal runaway failure is possible due to high off-state drain leakage current, which may cause the activation of the parasitic *npn* BJT. Nevertheless, the turn-off tail currents previously observed for discrete devices are not appreciated here, which means that a current imbalance between paralleled chips would be more likely as the failure root cause.

Another failure mechanism has been observed during the short-circuit testing of a second 1.2 kV/ 300 A SiC MOSFET power module. Fig. 5.9 shows that the device successfully passes the test for a pulse duration of 4.7 μs, with a bias voltage of 500 V

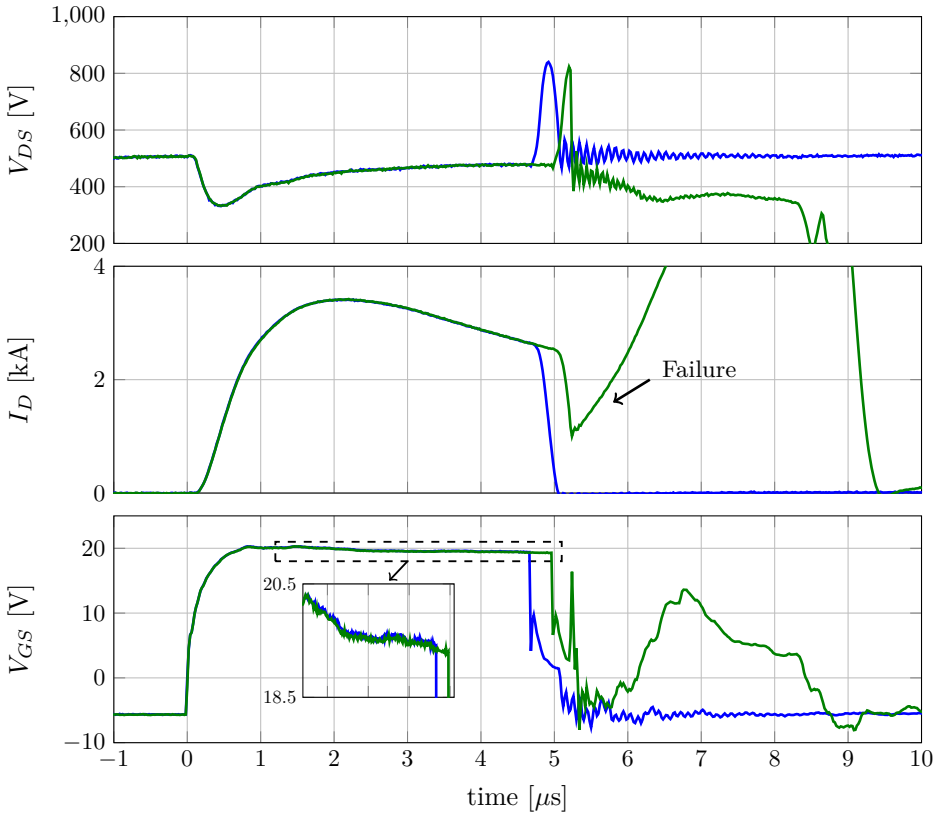

Figure 5.9: *Short-circuit failure of the 1.2 kV/ 300 A SiC power module within 5 μs at V_{DS} = 500 V and T = 25°C [69].*

and case temperature of 25°C. A longer pulse of 5 μs causes the device sudden destruction while it is turning off, implying again some sort of thermal instability mechanism. Similarly as before, it is worth to point out that the gate-oxide reliability is always compromised during short-circuit conditions, since a gradual reduction of the gate voltage has been observed. This could be interpreted as an increase in the gate leakage current, which becomes more critical with higher DC-link voltages and higher temperatures.

5.3.2 Short-circuit assessment of the 1.2 kV/ 180 A SiC power module

To the same extent, the short-circuit performance of the 1.2 kV/ 180 A has been evaluated (BSM180D12P2C101). Fig. 5.10 shows a series of short-circuit tests for a bias voltage of 800 V and case temperature of 25°C. This graph shows the two important failure precursors observed in SiC MOSFETs. Firstly, a tail current during turn-off is appreciated, whose amplitude progressively increases with the pulse length. Indeed there is no sign of turn-off tail current for pulse durations lower than 5 μs. This clearly indicates that the tail current is function of the temperature and, in this case, regardless of the drain-source voltage. Secondly, the degradation of the gate-oxide is confirmed by

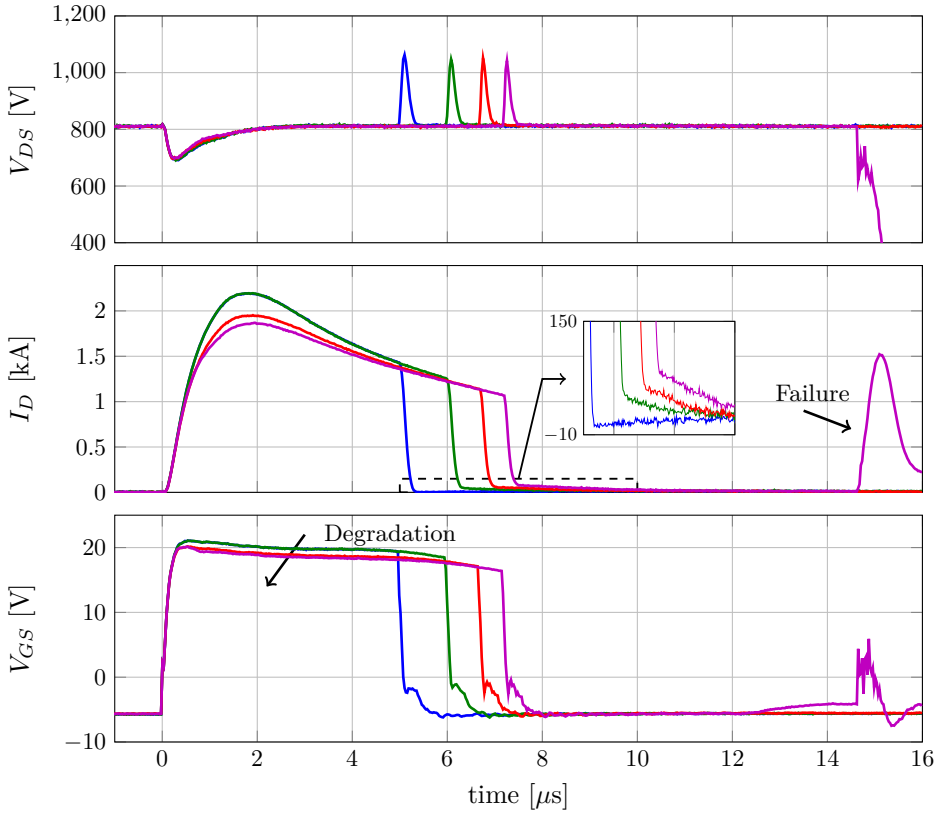

Figure 5.10: *Short circuit failure of the 1.2 kV/ 180 A SiC power module within 7.2 μs at V_{DS} = 800 V and T = 25°C [69].*

looking at the gate-source voltage waveform. A voltage reduction for pulses longer than 6 μs indicate that the gate-oxide insulation material has been damaged and the point of no return has been reached. Finally, the device presents a thermal runaway failure when a short-circuit pulse of 7.2 μs is applied.

5.4 Short-Circuit Safe Operation Area Identification Criterion

Based on the experimental results on SiC MOSFETs under short-circuit conditions, two different failure precursors have been identified, both reducing the short-circuit capability of SiC power modules and discrete devices. The two failure precursors are the tail currents at turn-off associated with drain-leakage current increase at high temperatures and the gate-oxide degradation in the form of gate voltage fall at the end of the pulse (reversible damage) or positive bias gate voltage reduction (permanent damage). The lower short-circuit withstanding capability of SiC power modules raises new challenges at the gate drive level, in which the protection circuit needs to rapidly detect the fault condition and protect the device within very short times, i.e. 2 μs. In view of this need, two short-circuit safety criteria have been formulated: (i) the short circuit current-based criterion, and (ii) the gate-voltage based criterion. The methodology of these two criteria have been presented in [69].

5.4.1 Short circuit current-based criterion

The excessive temperatures reached inside the SiC MOSFET cell can trigger thermal instabilities, which lead to hot spot formation and consequently sudden destruction of the device. During short-circuit, it is observed that a negative dependence between the short-circuit current and the junction temperature exist. As the self-heating effect is more important because of longer short-circuit pulses, the short-circuit current further decreases towards the end of the pulse. The idea is to monitor the drain current level by ensuring that it does not fall below a given value, which corresponds with the maximum allowable junction temperature that the device can withstand before failure takes place. For example, in Fig. 5.8, the critical temperature value which leads to thermal runaway corresponds with a drain current value of 3 kA, measured at the end of the pulse. In order to prevent such a failure, the device can be turned off earlier, which guarantees that the temperature of the device will be lower than the critical one. Based on this insight, the method consists to turn-off the short-circuit current if this one falls below a selected limit, for example 4 kA for the 1.2 kV/ 300 A SiC power module and 1.5 kA for the 1.2 kV/ 180 A SiC power module [69].

Figs. 5.11 and 5.12 demonstrate that this approach is helpful to operate the device in a safe way when the short circuit current-based criterion is applied at different DC-link

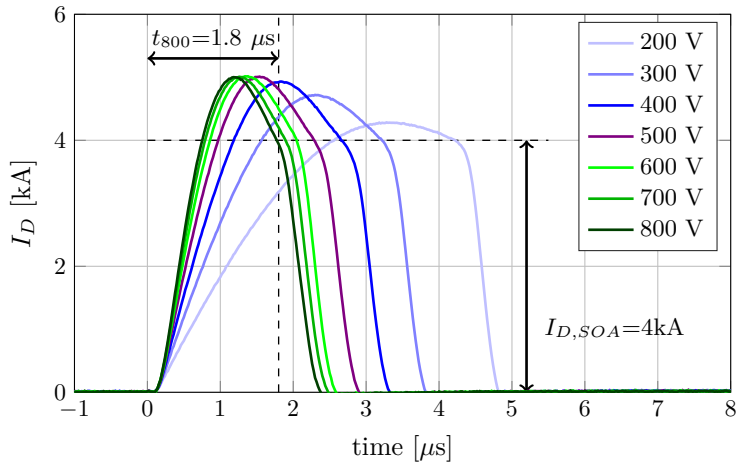

Figure 5.11: *Validation of the short circuit current-based criterion for the 1.2 kV/ 300 A SiC MOSFET at different DC-link voltages for SOA characterization [69].*

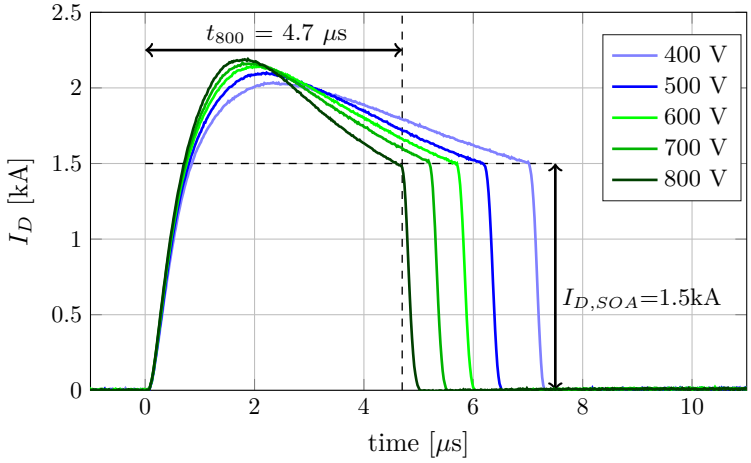

Figure 5.12: *Validation of the short circuit current-based criterion for the 1.2 kV/ 180 A SiC MOSFET at different DC-link voltages for SOA characterization [69].*

voltages. In all the cases, the device is turned off when the short-circuit current reaches the selected limit, without any sign of delayed failures after turn off. One observation is that, as the DC-link voltage is increased, the pulse length becomes shorter due to

the larger dissipated power. Therefore, the gate driver is challenged to detect the short circuit condition and protect the device within 1.8 μs at 800 V for the 1.2 kV/ 300 A SiC power module. On the other hand, the 1.2 kV/ 180 A SiC power module featured higher robustness against short circuit conditions, therefore the device can survive safely a short circuit of 4.7 μs for a bias voltage of 800 V.

5.4.2 Gate voltage-based criterion

The failure mode involving the breakdown of the gate oxide is the most common reported in the literature. The sudden increase in the junction temperature coming from the huge heat generation during the short-circuit event, seems to be critical for the gate-oxide reliability. Especially under high DC-link voltages, where the electric fields inside of the device are larger. Based on the short circuit failures related with the degradation of the gate oxide, another approach is proposed that has been presented in [69]. The method consists to monitor the gate voltage waveform in order to detect whether the the gate voltage falls below a certain value. This voltage drop is associated with the gate leakage current level that the device can withstand before the failure occurs. In order to early predict and therefore avoid gate-oxide breakdown failures, a gate voltage drop corresponding to 100 mA gate current is selected, e.g. 0.5 V/5 Ω.

The validation of the gate voltage-based criterion is demonstrated in Figs. 5.13 and 5.14 for the 1.2 kV/ 300 A and the 1.2 kV/ 180 A SiC power modules, respectively. The method consists to turn-off the short-circuit current if the gate leakage current increases above 100 mA, corresponding to a voltage drop of 0.5 V from its positive gate bias of 20 V (R_g = 5 Ω). The experimental results demonstrate that the proposed method is effective for various DC-link voltages, revealing that both SiC MOSFETs are able to survive short-circuit events, when the gate voltage-based criterion is applied. It is important to highlight that at low DC-link voltages (i..e, 200 V and 300 V), the gate voltage is quite flat, without any sign of voltage drop within the 10 μs short circuit.

5.4.3 Short-circuit safe operation area

The Short-Circuit Safe Operation Area (SCSOA) of the two SiC MOSFET power modules will be presented. The SCSOA has been formulated based on the two original short circuit criteria previously formulated: (a) the short circuit current-based criterion, $I_{D,SOA}$ and (b) the gate voltage-based criterion, $V_{G,SOA}$. Fig. 5.15 illustrates the SCSOA as a function of the drain-source voltage and short-circuit time, for a case temperature of 25°C. The gate voltage-based criterion seems to be the least restrictive one, though at high DC-link voltages becomes the most crucial. The most restrictive criterion is selected as the final SCSOA of the device, this is highlighted with a dashed line in Fig. 5.15. The maximum short circuit time of the tested 1.2 kV SiC discrete devices, rated at 36 A and 90 A, is also reported. The purpose is to have a reference to compare the SCSOA between power modules and discrete devices.

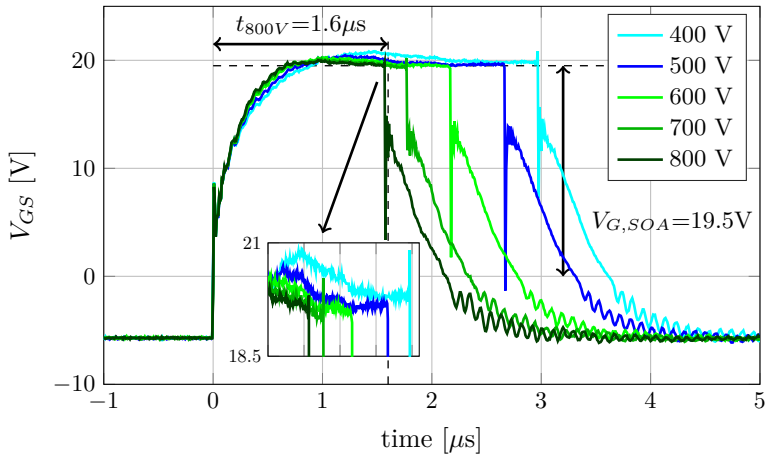

Figure 5.13: *Validation of the gate voltage-based criterion for the 1.2 kV/ 300 A SiC MOSFET at different DC-link voltages for SOA characterization [69].*

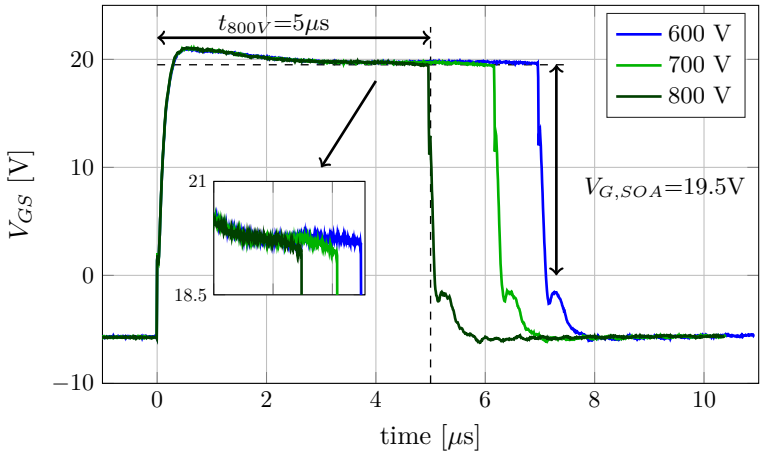

Figure 5.14: *Validation of the gate voltage-based criterion for the 1.2 kV/ 180 A SiC MOSFET at different DC-link voltages for SOA characterization [69].*

It is worth to point out that SiC MOSFET power modules are yet to reach the typical short-circuit withstanding time of 10 μs, which in turn sets a need to either improve the device robustness, or alternatively, employ new gate driver design solutions. For example, if both SiC MOSFET modules are operated at 600 V bias voltage (i.e., half of

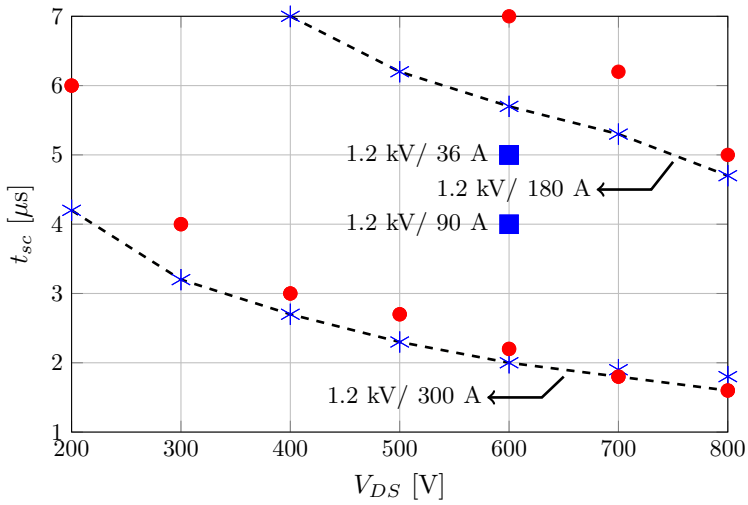

Figure 5.15: *Short circuit SOA (dashed line) of the two SiC power modules based on the two proposed criteria at T= 25° C. $I_{D,SOA}$ (blue asterisk) - short circuit current-based criterion and $V_{G,SOA}$ (red dots) - gate voltage-based criterion. The short circuit withstanding capability of the 36 A and 90 A SiC MOSFETs is reported for comparison [69].*

its breakdown voltage), the gate driver must limit the pulse durations within 5.8 μs for the 1.2 kV/ 180 A DUT and within 2 μs for the 1.2 kV/ 300 A DUT, which becomes especially challenging due to the higher switching frequencies in SiC devices and their interaction with the noisy environment. Additionally, SiC-based semiconductors have superior thermal properties than silicon, however the device itself is subjected to extreme thermal stresses, and, in particular during short circuit. The reason can be found in the high cell densities that are typically employed to ensure a low on-resistance. The drawback is that improvements in the short-circuit robustness (i.e., lower saturation current) will come at the expense of increases in conduction losses [11].

5.5 Conclusions of this Chapter

In this chapter, the short-circuit performance of SiC power MOSFETs is presented for both discrete and power modules, rated at 1.2 kV. The aim was to investigate the short-circuit failure mechanisms and limitations of state-of-the-art SiC MOSFETs. The results have revealed that two failure modes have been observed in this work, which must be understood in order to operate the devices at high temperatures, while not

compromising their reliability. The first failure mechanism is characterized by a sudden drain current increase, either during the DUT's turn-off or a few microseconds after turn-off. As a failure precursor, a large tail current appears, which may be associated with the activation of the parasitic *npn* BJT, as stated in the literature. Further investigations must be done about this failure type, firstly to understand the root cause and secondly to give a solution to the problem.

The second failure mechanism is characterized by a gradual gate voltage degradation, causing irreversible damages, appearing more often under high DC-link voltages and high temperature operations. As a failure precursor, the gate voltage drops a few μs after the beginning of the short circuit, which becomes more evident with longer pulses and higher DC-link voltages. This voltage drop is associated with a leakage current flowing between the gate and source terminals, due to degradation of the gate-oxide material properties. But once more, further investigations must be done to localize the weak point, in order to redesign the device cell to make it more robust against short-circuit events.

Finlay, two short-circuit criteria have been adopted, which rely on temperature-dependent indicators, such as the short-circuit current level and the gate-voltage drop at the end of the short-circuit pulse. A new guideline has been proposed in order to depict the SCSOA of SiC MOSFETs, revealing that discrete devices may survive short-circuit conditions to some extent. However, SiC power modules may need a new rethinking of the package design and probably also at device level, to compete with the well-established Si IGBT.

Chapter 6

Conclusions and Suggestions for Future Research

This chapter summarizes the results, which have been accomplished throughout this Ph.D. project. Moreover, the research areas where future work is needed will be highlighted.

6.1 Summary

The main research objective of this thesis was to investigate the instability mechanisms occurring in power semiconductor devices under short-circuit conditions. In particular, this project has mainly focused on the root cause of the high-frequency gate voltage oscillations in IGBTs. This goal has been achieved by using a combination of measurements of medium and high-voltage IGBTs with different technologies (i.e., planar, trench and BIGT) on discrete devices and also on power modules. Finite-element device simulations have been carried out with a 3.3-kV IGBT half-cell to reproduce the short-circuit oscillations for the first time. This is beneficial in order to identify how the IGBT evolves during each oscillation cycle and finally propose an hypothesis to justify the root cause of such an amplifying behaviour. This has been accomplished by studying the factors that influence the occurrence of such instabilities, which are typically attributed to the internal physics of the device.

Chapter 1 gives an introduction to the project motivation and the background in short-circuit instabilities for both silicon IGBTs and silicon carbide power MOSFETs. The problem formulation, project objectives and limitations of this work have been discussed.

In *Chapter 2*, a thorough investigation about the short circuit performance of sil-

icon IGBTs is presented, especially focusing on the gate voltage oscillations limiting the robustness of IGBTs. Results widely corroborate that gate voltage oscillations can typically be observed for both planar and trench IGBT cell designs. These oscillations take place a few microseconds from the short-circuit beginning, whose diverging amplitude may provoke a gate-oxide breakdown. Furthermore, the influence of the testing conditions and/or external circuit variations have been addressed, making possible the identification of key parameters playing a role, either as a triggering condition or as a parameter involved in the instability, i.e., DC-link voltage, circuit layout, temperature, short-circuit current and carrier profile distribution.

In *Chapter 3*, the short-circuit oscillations have been simulated for the first time with the help of both circuit and device analysis. A sensitivity analysis has been performed, varying different parameters and investigating its influence on the short-circuit oscillation behavior. Therefore, it is possible to establish a correlation between the outcome of the simulations and the experiments. By looking at the internal evolution of the IGBT, it has been discovered that the oscillations can only occur when the electric field at the emitter of the IGBT becomes weak (Kirk Effect). This confirms that the root cause of the oscillations can be explained with focus on the device charge-storage effect resulting from both electric field and carrier velocity variations.

In *Chapter 4*, a detail analysis on the short-circuit oscillations has been given. The conclusion is that, during a short circuit event at a low DC-link voltage, the electric field strength in the n-base will be low, and especially weaker at the emitter of the IGBT, mainly due to the observed Kirk Effect. The drift velocities will be in a range where they are not saturated, and thus field dependent, which in turn causes electron accumulation effects at the emitter of the IGBT, due to the substantially lower electron drift velocity in this region. As a major achievement of this work, it is possible to relate the electric field distortions to gate capacitance variations, and associate the capacitance variation with charge-storage effects occurring at the surface of the IGBT, arising from the low carrier velocities. On the other hand, at high DC-link voltages, the carrier drift velocities become close to saturation across the whole n-base, which means that the charge-storage effect is no longer present, thus, the input capacitance becomes fixed. Finally and as the major discovery of this work, it has been pointed out for the first time that a parametric oscillation takes place during the IGBT short circuit, whose time-varying element is the Miller capacitance, leading to an amplification mechanism.

In *Chapter 5*, the short-circuit assessment of SiC power MOSFETs is presented for both discrete and power modules. The results have revealed that a thermal instability takes place after a few microseconds from the short-circuit beginning, leading to most of the cases to gate-oxide damage. Additionally, a current tail has been observed and characterized in respect to the temperature and the drain voltage, whose occurrence is related to the aforementioned thermal instability. Two short-circuit criteria have been adopted, which rely on temperature-dependent indicators, such as the short-circuit current level and the gate-voltage drop at the end of the short-circuit pulse. A new

guideline has been proposed in order to depict the SCSOA of SiC MOSFETs, revealing that discrete devices may survive short-circuit conditions to some extent. However, SiC power modules may need a new rethinking of the package design and probably also at device level, to compete with the well-established Si IGBT.

6.2 Main Contributions

Based an all the work done, the main contributions can be summarized as:

1. **Experiments demonstrate that the IGBT short-circuit robustness strongly depends on the external circuit and testing conditions.**
   Based on the outcome from the experiments, it can be concluded that the short-circuit oscillations are occurring in both single-chip IGBTs and multi-chip IGBT modules. Different technologies have been tested, such as the Enhanced-Planar IGBT implemented on the Soft Punch-Through (SPT) buffer concept, the Enhanced-Trench IGBT implemented on the Soft Punch-Through (SPT) buffer concept, and the Bi-mode Insulated Gate Transistor (BIGT) on both planar and trench-gate topologies. While the IGBT technologies show an oscillatory behaviour under short circuit, the BIGT concept seems to solve the problem, since oscillations are no longer observed. Analysing the IGBT performance under a short circuit, they all have in common the following features: (1) the gate-voltage oscillations tend to disappear or become mitigated at high DC-link voltages, low gate-emitter voltages and high temperatures, and (2) the gate voltage oscillations tend to disappear or become mitigated with low gate inductance, low stray collector inductance and slower transients, which can be regulated with the gate resistance of the emitter stray inductance.

2. **TCAD short-circuit simulations have reproduced the oscillatory behaviour.**
   Finite-Element simulations have been performed by taking into account both circuit and device analysis. A sensitivity analysis has been performed, demonstrating that the simulations show the same key enabling factors as the experiments, with respect to the occurrence of the oscillations. The simulations demonstrate that under short-circuit conditions, the electric field peak moves towards the collector, thus becoming weak at the emitter. This results in a low carrier drift velocity at the emitter and therefore an excess carrier density is observed leading to a charge-storage effect. In Chapter 3 is demonstrated that the testing conditions resulting in higher electric fields at the emitter (i.e., high V_{CE}, low V_{GE}), correspond with a more robust short-circuit operation without oscillations.

3. **The IGBT presents a time-varying input gate capacitance during the short-circuit oscillations.**

By looking at the physical mechanisms happening during each oscillation cycle, it has been understood that the electric field variations can be related with gate input capacitance fluctuations periodically with time. Basically, the carrier drift velocities have a strong impact on the charge balance of the IGBT, especially at low DC link voltages since they are field dependent. The capacitance variation with time has been associated with charge-storage effects occurring at the surface of the IGBT, due the low carrier velocity in this region. Thus, the capacitance increases and decreases depending on the electric field strength at the emitter of the IGBT. If the electric field is strong enough at the emitter of the IGBT, the carrier drift velocity becomes saturated and the charge-storage effect, responsible for the capacitance variation, is not observed.

4. **The IGBT is prone to parametric oscillations under short-circuit conditions.**
   Based on the results from the mixed-mode simulations, one can hypothesize that the amplification behaviour arises from the capacitance variation in time, rather than the IGBT cell behaviour as an amplifier. The validation of this theory has been presented in Chapter 4, where a PSpice simulation has been built with two capacitances changing with time in order to justify how oscillations can diverge with time. The gate voltage oscillation phenomena has been modelled by alternatively switching two capacitances and carefully selecting the time instants at which the capacitors need to be changed, showing the typical behaviour or a parametric oscillator.

5. **The short-circuit robustness of SiC MOSFETs is limited by gate-oxide degradation and thermal runaway failures.**
   State-of-the art SiC power MOSFETs have been experimentally tested for both discrete and power modules. In Chapter 5, it has been found that the short-circuit withstanding capability of SiC MOSFETs is lower than silicon-based IGBT devices. Two failure modes have been mainly observed, which are temperature-related: (a) gate voltage drop pointing out gate-oxide degradations and (b) turn-off tail currents leading to thermal runaway failures. Both failure modes compromise today's SiC MOSFET devices, however a conclusive theory about its root cause has not been formulated in this work.

6.3 Proposals for Future Work

Below, the most important areas where future work is still needed are summarized:

1. **Oscillation mitigation.**
   The most important achievement of this thesis was the discovery of the short-circuit oscillations root cause, whose hypothesis can be correlated to the experi-

mental short-circuit oscillation dependencies. In order to mitigate the occurrence of the oscillations, some solutions have been proposed: From the layout point of view, the reduction of gate and collector stray inductances has been proposed, however, it may not be feasible to achieve such low stray inductances in real applications. From the testing conditions point of view, it has been suggested to operate the device at high DC-link voltage, low gate voltage and high temperatures, but all of these measures have drawbacks from the device SOA (Safe Operation Area) perspective and also increased losses. From the device point of view, two solutions have been proposed: increase of emitter efficiency and the use of an n-doped Surface-Buffer Layer. Both solutions prove that oscillations can be mitigated, however, some drawbacks must be considered, such as increase in switching losses for the first solution and a reduced blocking capability for the second one. Further research must be done in order to find the optimum trade-off between short-circuit robustness and reliable operation under normal conditions.

2. **Temperature estimation under short circuit.**
   In order to simulate the real temperature under short-circuit operation, simulations including self-heating effects must be necessary to better understand the oscillation behaviour dependency with the temperature distribution inside of the IGBT. This would help to achieve the current densities that can be found in the real device.

3. **Short-circuit failure mechanism in SiC power MOSFETs.**
   The experimental tests presented in Chapter 5 indicate that the short-circuit robustness of SiC MOSFETs is nowadays compromised due different failure modes. Further research must be done on the understanding of such failures modes in order to improve the reliability of this emerging technology. To address this, the development of a SiC MOSFET model suited for finite-element device simulations is suggested, as well as the development of electro-thermal simulations in order to investigate temperature-related failure mechanisms.

Chapter 7

Appendix

This appendix includes the command files which have been used for the TCAD simulations in this thesis. Both IGBT cells have been created in Sentaurus Structure Editor GUI inlcuding the geometrical device structure and the doping profiles for the device. The tool for running the simulations was Sentaurus Device Simulation and a sample of the three different files that have been used is given in the following.

- Quasistationary I-V curve.
- Mixed-mode device simulation for short circuit.
- Transient device simulation - Double Pulse Test (DPT).

Quasistationary I-V Curve

```
electrode {
        { name = "cathode" Voltage = 0.0}
        { name = "anode" Voltage = 0.0 }
        { name = "gate" Voltage = 0.0}
}
plot {  Doping
        Potential Edensity Hdensity
        ElectricField/vector
        eCurrent/vector hCurrent/vector totalCurrent/vector
        eLifeTime hLifeTime
        eAvalanche hAvalanche Avalanche
        eMobility hMobility
        eDriftVelocity hDriftVelocity
        eVelocity hVelocity
        eSaturationVelocity hSaturationVelocity
        SRHRecombination AugerRecombination
}
file {
         Grid= "igbt_msh.tdr"
         Doping= "igbt_msh.tdr"
         Parameters= "lifetime.par"
         Parameters= "mobility.par"
         output  = "LC_cal_A1e17_Vce2500V_Vge0V_300K_des.log"
         plot    = "LC_cal_A1e17_Vce2500V_Vge0V_300K_des.dat"
         current = "LC_cal_A1e17_Vce2500V_Vge0V_300K_des.plt"
         save    = "LC_cal_A1e17_Vce2500V_Vge0V_300K_des.sav"
}
physics {
        areafactor= 2.85e6
        temperature=300
        EffectiveIntrinsicDensity(slotboom)
        Recombination (
                SRH (
                        DopingDependence
                        TemperatureDependence
                )
                Auger
         Avalanche(VanOverstraeten GradQuasiFermi)
        )
        Mobility ( phumob(phosphorus)
                HighFieldSaturation
                 NormalElectricField
        )
}
math {  extrapolate
        digits=5
        derivatives
        avalderivatives
        relerrcontrol
        errref(electron)=1E9
        errref(hole)=1E9
```

```
        NumberOfThreads = 2
        iterations = 12
}
solve {
        coupled(iterations=100){ poisson  }
        coupled { poisson electron hole }
        QuasiStationary
      (
        MaxStep=0.1 MinStep=1e-9 InitialStep=1e-4
        Goal{ name = "anode" voltage=2500 }
            increment = 1.5
            decrement = 3
      )
      {
        coupled (digits=5 iterations=10 )
        { poisson electron hole }
         plot (
              FilePrefix="LC_cal_A1e17_Vge0V_300K"
              Time = (0.002; 0.004; 0.02; 0.03; 0.04; 0.14; 0.2; 0.4; 0.6; 0.8)
              * 5V; 10V; 50V; 75V; 100V; 350V; 500V; 1000V; 1500V; 2000V
              NoOverwrite
               )
      }
}
```

Mixed-Mode Device Simulation for Short Circuit

```
plot {    Doping
          ElectricField/vector Potential
          eDensity hDensity
          SpaceCharge
          totalCurrent/vector eCurrent/vector hCurrent/vector
          DisplacementCurrent
          Avalanche eAvalanche hAvalanche
          eLifeTime hLifeTime
          Temperature
          SRHRecombination AugerRecombination
          eVelocity hVelocity
          TotalHeat
 }
math {   RelErrcontrol
          NoAutomaticCircuitContact
          Transient = BE
          derivatives
          avalderivatives
          NumberOfThreads = 3
}
physics {
          areafactor= 2.85e6
          Thermodynamic
          AnalTEP
          temperature=300
```

```
        EffectiveIntrinsicDensity(slotboom)
        Recombination (
                SRH (
                        DopingDependence
                        TemperatureDependence
                  )
                Auger
         Avalanche(VanOverstraeten GradQuasiFermi)
                )
        Mobility (
                 phumob(phosphorus)
                HighFieldSaturation
                 NormalElectricField
                        )
}
dessis IGBT {
 electrode {
        { name = "cathode" Voltage = 0.0}
        { name = "anode" Voltage = 1000.0}
        { name = "gate" Voltage = 0.0}
  }


 File { }
  physics {
        AreaFactor = 2.85e6
    }
}
System {
        Vsource_pset v1 (Vdc_high Vdc_low)  {dc = 1000.0}
        Inductor_pset ls (Vdc_high I_anode) {inductance = 1.2e-6}


        IGBT I1 (cathode=I_cath, anode=I_anode, gate=I_gate)
        Inductor_pset lc (I_cath Vdc_low){inductance = 10e-9}
        Resistor_pset rg (Vg_high Vg_high2) {resistance=1}
        Inductor_pset lg (Vg_high2 I_gate) {inductance = 40e-9}
        set(Vdc_low=0)
        Vsource_pset vg (Vg_high Vdc_low)  {pulse = (0 15 2e-6 1e-7 1e-7 1e-5 1)}
        plot "SC_300K_1000V_15V_1200nH_Le10n_Lg40n_R1.plt" (
    time() i(I1 I_cath) v(I_gate I_cath) v(I_anode I_cath) i(I1 I_gate) i(I1 I_anode)
    )
 }
solve {   coupled (digits=4 Iterations=100) {circuit}
          coupled (digits=4 Iterations=20 notdamped=50) {
                circuit poisson contact electron hole}
Transient (
         MaxStep=1e-8 MinStep=1e-12 InitialStep=1e-9
         InitialTime=0 FinalTime=10e-6
          Increment = 1.5 Decrement = 2
       )
       {
            coupled (digits=4 iterations=12 notdamped=50)
```

```
        {circuit poisson contact electron hole
        }
    plot (FilePrefix="SC_300K_1000V_15V_1200nH_40n_10n_R1_des"
      Time = (2.04e-6; 2.07e-6; 2.11e-6; 2.35e-6; 2.6e-6; 3.05e-6; 4e-6; 5e-6; 6e-6)
          NoOverwrite
    )
    }
  }
```

Transient Device Simulation - Double Pulse Test (DPT)

```
file {
 Output= "@log@"
}
 !(
  set DG     0       ;#-- quantum corr is on, when 1
  set Hydro  0       ;#-- hydro       is on, when 1
  set Thermo 0       ;#-- thermal     is on, when 1

  set PULSE "(0.0    0
          1.0e-7 0
          1.1e-7 15
          @<7e-6 + 1.1e-7>@ 15
          @<7e-6 + 1.2e-7>@ 0
          @<7e-6 + 1.2e-7 + 5e-6>@ 0
          @<7e-6 + 1.3e-7 + 5e-6>@ 15
          @<2*7e-6 + 1.3e-7 + 5e-6>@ 15
          @<2*7e-6 + 1.4e-7 + 5e-6>@ 0
          @<2*7e-6 + 1.4e-7 + 2*5e-6>@ 15
          @<3*7e-6 + 1.4e-7 + 2*5e-6>@ 0
          1.0    0)"

          set EQN0      "Poisson Electron Hole"
           set EQN1      "Poisson Electron Hole Circuit Contact"
          set HYDROEQ    "eTemperature hTemperature"
          set THEQ      "Temperature"
          set DGEQ      "eQuantumPotential"
  if {$Hydro} {
          set EQNS     "$EQN1 $HYDROEQ"
          set DF       "CarrierTempDrive"
  } else {
          set EQNS     "$EQN1"
          set DF       "GradQuasiFermi"
  }
  if {!$DG} {set DGEQ " "}
  set EQNS  "$EQNS $DGEQ"

  if {!$Thermo} {set THEQ " "}
  set EQNS  "$EQNS $THEQ"
)!
```

```
plot {    Doping
          ElectricField/vector Potential
          eDensity hDensity
          SpaceCharge
          totalCurrent/vector eCurrent/vector hCurrent/vector
          DisplacementCurrent
          Avalanche eAvalanche hAvalanche
          eLifeTime hLifeTime
          Temperature
          SRHRecombination AugerRecombination
          eVelocity hVelocity
          TotalHeat
 }
math {  RelErrcontrol
          NoAutomaticCircuitContact
           Transient = BE
          derivatives
          avalderivatives
}
physics {
          areafactor= 2.85e6
          Thermodynamic
          AnalTEP
          temperature=300
          EffectiveIntrinsicDensity(slotboom)
          Recombination (
                    SRH (
                              DopingDependence
                              TemperatureDependence
                      )
                    Auger
           Avalanche(VanOverstraeten GradQuasiFermi)
                    )
          Mobility (
             phumob(phosphorus)
             HighFieldSaturation
                       NormalElectricField
                              )
}
dessis IGBT {
  electrode {
          { name = "cathode" Voltage = 0.0}
          { name = "anode" Voltage = 0.0}
          { name = "gate" Voltage = 0.0}
    }
File {
          Grid= "igbtNdrift3_msh.tdr"
          Doping= "igbtNdrift3_msh.tdr"
          Parameters= "lifetime.par"
          Parameters= "mobility.par"
          plot= "DPT_des.dat"
          current    = "DPT_des.plt"
}
```

```
physics {
        AreaFactor = 2.85e6
    }
}
System {
        IGBT trans (cathode=s  gate=g anode=d)
        Vsource_pset vd  (nd 0)  { dc = 0 }
        Vsource_pset vs  (s 0)   { dc = 0 }
        Vsource_pset vg  (ng 0)  { pwl = !( puts $PULSE )! }
        Diode_pset dd (d nd) { }   # Resistive Load
        Inductor_pset ld (nd d)  { inductance = 2.5e-4 }   # Inductive Load
        Resistor_pset rg (ng g)  { resistance = 10 }   # Gate Resistance
        Set (0=0)
        Initialize (g=0, d=0)
        plot "Transient_des.plt" (time() v(g) v(d) v(nd) v(ng) i(rd nx) i(rg g))
}
Solve {
        *- Creating initial guess:
        Coupled { poisson }
        Coupled(Iterations=100 LineSearchDamping=1e-4){ Poisson !(puts -nonewline $DGEQ)! }
        Coupled(Iterations=100 LineSearchDamping=1e-4){ Poisson !(puts -nonewline $DGEQ)! Electron Hole }
        *- Ramp Drain
        Unset(d)
        Quasistationary (
                InitialStep=1e-3 MinStep=1e-5 MaxStep=0.5
                Increment=1.45 Decrement=2.1
                Goal { Parameter= vd.dc Value=1800 }
  ){ Coupled { !(puts -nonewline $EQN1)! } }
                Coupled { !(puts -nonewline $EQNS)! }
        NewCurrentPrefix="Trans_"
  Transient (
        InitialTime=0 FinalTime= 13.5e-06
        InitialStep=1e-8 MinStep=1e-15 MaxStep=1e-4
        Increment= 1.35 Decrement= 2.1
        ){ Coupled { !(puts -nonewline $EQNS)! }
    }
}
```

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