Control and Optimization of Modular Multilevel Cascaded Statcom Converters for Offshore Wind Application

Tanaka, Takaaki

Publication date:
2018

Document Version
Publisher's PDF, also known as Version of record

CONTROL AND OPTIMIZATION OF MODULAR MULTILEVEL CASCADED STATCOM CONVERTERS FOR OFFSHORE WIND APPLICATION

BY
TAKAAKI TANAKA

DISSERTATION SUBMITTED 2018

AALBORG UNIVERSITY
DENMARK

CONTROL AND OPTIMIZATION OF MODULAR MULTILEVEL CASCADED STATCOM CONVERTERS FOR OFFSHORE WIND APPLICATION

by

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Dissertation submitted to Faculty of Engineering and science

at Aalborg University in 2018

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PhD Series:	Faculty of Engineering and Science, Aalborg University
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ISSN (online): 2446-1636
ISBN (online): 978-87-7210-363-1

Published by:
Aalborg University Press
Langagervej 2
DK – 9220 Aalborg Ø
Phone: +45 99407140
aauf@forlag.aau.dk
forlag.aau.dk

Printed in Denmark by Rosendahls, 2018

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Takaaki Tanaka was born in Kyoto, Japan in 1987. He received the B.E. degree in electrical engineering from National Institute of Technology, Maizuru College, Kyoto, Japan, in 2010 and the M.E. degree in electrical engineering from Nagaoka University of Technology, Niigata, Japan, in 2012. From 2012, he is a researcher at the Corporate R&D Headquarters, Fuji Electric, Co., Ltd., Tokyo, Japan.

Mr. Tanaka was a visiting researcher with the Center of Reliable Power Electronics (CORPE) at Aalborg University, Aalborg, Denmark from December 2015 to November 2017. His research interests include power electronics and its applications such as in renewable energies, transportation, reliability, power density, WBG devices and circuit architecture. He is a member of the Institute of Electrical and Electronics Engineers (IEEE) and the Institute of Electrical Engineers of Japan (IEEJ).

ENGLISH SUMMARY

The capacity for renewable energy generation has continued to grow in the last decade, and it is expected to become 2.5 TW in 2020. In accordance with constructions of large-scale renewable energy generation systems such as solar photovoltaic and wind power plants, stricter grid codes under both normal operation and grid fault conditions are demanded by Transmission System Operators (TSO) in most countries.

Large-scale offshore wind power generation is significantly growing and becoming one of the major renewable energy sources in Europe with strong wind and shallow sea areas, because of the advantages such as constant and high wind velocity as well as extensive offshore sites, which reduces the generation cost. However, the generated electrical power has to be transmitted to the Point of Common Coupling (PCC) onshore by long-distance submarine cables, which arise a large amount of reactive power if a Medium to High Voltage Alternating Current (MVAC-HVAC) transmission system is selected. In order to compensate enough reactive power and to satisfy the grid codes, SVC or STATCOMs have to be installed on the onshore side of the wind power plant.

The Modular Multilevel Cascade Converters (MMCC) family are promising solutions in the case of high-voltage and high-power STATCOM applications. They have significant advantages, compared to the conventional two-level or three-level voltage source converters, such as lower harmonic distortions, transformer-less configuration at medium voltage level, and modular/ redundant design. Nevertheless, voltage-balancing for a large number of DC-link capacitors in converter cells are still challenging to be achieved for MMCCs, especially under asymmetrical grid faults. In addition, the principal dc-link capacitor voltage ripple with second-order at grid frequency in each converter cell makes the required capacitor size large compared to the conventional converters.

Many authors have proposed useful control schemes and design methods for each type of MMCC solutions until now. However, the optimum MMCC solution for the STATCOM application is still an open question because a comprehensive comparison between each type of MMCC solution has not been done. In addition to the total cost and volume of the MMCC solutions, the asymmetrical reactive power delivering capability under grid faults becomes more and more important for the STATCOM application. Furthermore, it seems that capacitor voltage ripple reduction methods for the MMCC solutions have not been considered enough yet.

This thesis clarifies the performances of potentially used four configurations of the MMCC family with SSBC, SDBC, DSCC, and DSBC for the STATCOM in large-scale offshore wind power plants, with special focus on asymmetrical Low Voltage

Ride Through (LVRT) capability under grid faults. Then, a capacitor voltage ripple reduction method by using a third harmonic zero-sequence current for one type of MMCC-SDBC is proposed and the benefits have been verified.

All achievements in this thesis have been validated by a practical designed 80 MVar/ 33 kV MMCC based STATCOM simulation result. These contributions have also been published in 2 journal papers and 4 conference papers.

DANSK RESUME

Den installerede kapacitet af den vedvarende energi-systemer er fortsat voksende og den forventes at blive 2,5 TW i 2020. I lyset af den stigen kapacitet af store vedvarende energiproduktionssystemer såsom solcelle- og vind-kraftværker bliver der specificeret stadig strengere tilslutnings-krav af Transmission System Operators (TSO) i de fleste lande både under normal drift og ved net-fejl.

Storskala vindkraftproduktion til havs vokser markant og bliver en af de største vedvarende energikilder i Europa, der har glimrende vindforhold og samtidig lav-vands havområder, hvilket giver fordele såsom konstant og høj vindhastighed, hvilket reducerer prisen for den producerede energi. Den genererede elektriske energi skal dog overføres til land via lange kabler i havet, og typisk er det baseret på vekselspændings-teknologien (AC). For at kompensere tilstrækkelig for den reaktive effekt, der opstår på grund af kablerne og for at tilfredsstille net-kravene, skal SVC'ere eller STATCOMs installeres på onshore side af vindkraftværkerne.

Den Modulære Multi-level Cascaded Converter (MMCC) omformer familie er en lovende løsning i tilfælde af høj-spænding og høj-effekt STATCOM applikationer. Konverterne i denne familie har betydelige fordele i forhold til de konventionelle effekt-omformere, som er baseret på to eller tre niveau omformer-systetmer, idet de har lavere harmonisk forvrængning, er en transformer fri konfiguration på mellem-spændingsniveau og har samtidig et modulært / redundant design. Ikke desto mindre er spændingsbalanceringen i sådanne konvertere med et stort antal DC-kondensatorer i konverter-cellerne stadig en udfordring for MMCC'erne, især under asymmetriske net-fejl. Hertil kommer at kondensatorerne har en spændings-variation af anden harmonisk, som gør den nødvendige kondensator-størrelse relativ stor i forhold til de konventionelle omformere.

Mange har indtil nu foreslået forskellige kontrol systemer og design-metoder for hver type of MMCC-løsningerne. Den optimale MMCC-løsning til STATCOM-applikationen er dog stadig et åbent spørgsmål, idet en detaljeret sammenligning mellem hver type MMCC-løsning endnu ikke er blevet udført. Ud over de samlede omkostninger og volumen af MMCC-løsningerne bliver den asymmetriske reaktive strømafgivelsesevne under net-fejl en mere og mere vigtig parameter for STATCOM-applikationerne. Endvidere ser det ud til, at kondensator spændings-variationen i MMCC løsningerne ikke er blevet studeret nok endnu.

Denne PhD afhandling sammenligner fire potentielt anvendelige konfigurationer af MMCC-familien, som er SSBC, SDBC, DSCC og DSBC, som skal agere som STATCOM i store offshore vindkraftværker med særlig fokus på drift under asymmetriske lave spændinger (LVRT), som typisk opstår under net-fejl. Der foreslås også en kondensator spændings-variations reduktionsmetode, der kan i

praksis reducere kondensator størrelsen med 20 % og dette realiseres ved at anvende en harmoniske nul-sekvensstrøm og dette princip er specielt velegnet i typen MMCC-SDBC. En detaljeret design er udført i afhandlingen, såvel som utallige simuleringer er udført til at underbygge den foreslåede metode.

Alle resultater i denne afhandling er blevet afprøvet på en praktisk designet 80 MVar / 33 kV MMCC baseret STATCOM model. Resultaterne er udover i PhD-afhandlingen blevet offentliggjort i 2 tidsskriftsartikler (IEEE) og 4 konferenceartikler.

ACKNOWLEDGEMENTS

This thesis is a summary of the collaboration research project entitled "Control and Optimization of Modular Multilevel Cascade STATCOM Converters for Offshore Wind Application". The research work is supported by the 2-year study abroad program of Fuji Electric Co., Ltd., Japan. Acknowledgements are given to the company as well as Aalborg University, who provided me a research environment in Denmark.

This research project was carried out under the supervision of Prof. Frede Blaabjerg and Prof. Huai Wang from the Department of Energy Technology, Aalborg University, Denmark, and Prof. Ke Ma from the Department of Electrical Engineering, Shanghai Jiao Tong University, China. I would like to show my deepest gratitude to them, for their professional and precise advice with their open-mindedness and earnestness during the collaboration research. Their supervision affects my research style, which I do believe will continuously support me in my future career.

I would like to say thank you to all my colleagues from the Department of Energy Technology for the warm environment. Best wishes to my friend - Changwoo Yoon, Yu-Hsing Chen, Yanfeng Shen, Haoran Wang, Uimin Choi, Hammam Soliman, Zhongxu Wang, Hamid Soltani, and all the other friends. The life hence became more interesting and colorful. My appreciations are extended to John K. Pedersen, Tina Larsen, Corina Busk Gregersen, Eva Janik and Casper Jørgensen for their assistance in different ways.

I would also like to acknowledge with much appreciation to Prof. Toshihisa Shimizu, Tokyo Metropolitan University, Japan, Prof. Jun-ichi Itoh, Nagaoka University of Technology, Japan, and Dr. Yasushi Matsumoto, Fuji Electric Co., Ltd, for introducing me to my supervisors, and Dr. Akio Toba, Fuji Electric Co., Ltd, for kind understanding of my Ph.D. study.

Last but not least, I am deeply thankful to my parents and my sister for their endless love and support.

Takaaki Tanaka

September, 2018

Tokyo, Japan

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CHAPTER 1. INTRODUCTION

1.1. BACKGROUND AND MOTIVATION

1.1.1. MARKET – OFFSHORE WIND POWER GENERATION

Globally, renewables are the largest electrical power source of net additions to power capacity over the medium term. They account for 62% of the expansion by 2020 and grow faster than fossil fuels and nuclear. Second to the hydropower, the wind power generation has the largest share in renewable energy source, and has continued to grow in the last decade, with a 532 GW installed capacity, including 20 GW from offshore wind turbines, by the end of 2018 as shown in Figure 1-1 [1].

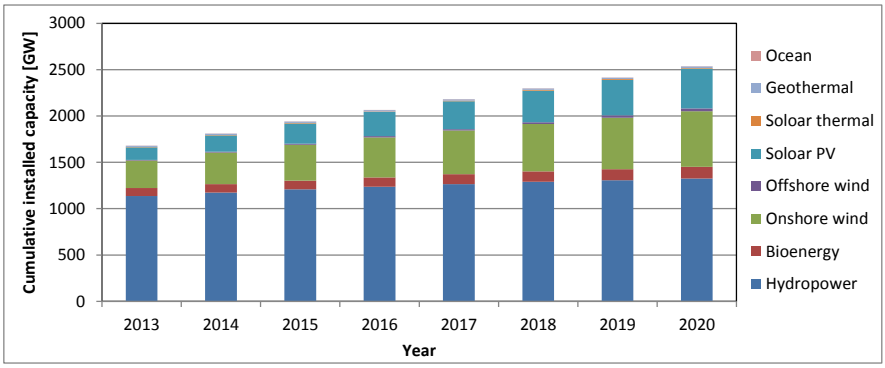


Figure 1-1 World renewable electricity capacity and forecast.

Large-scale offshore wind power generation is significantly growing (see Figure 1-2) and become one of the major renewable energy sources in Europe, which is having strong wind and shallow sea areas and giving the advantages of constant and high wind velocity as well as Europe also has extensive offshore areas. All together will reduce the generation cost of wind energy [1], [2].

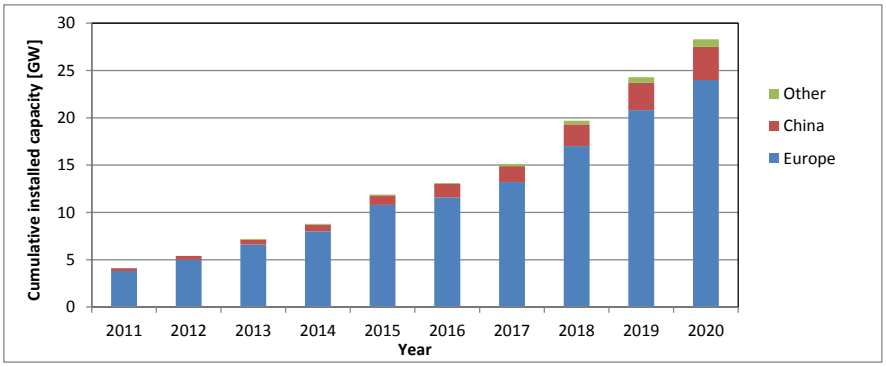


Figure 1-2 Offshore wind power capacity and forecast by region.

1.1.2. MODERN LARGE-SCALE OFFSHORE WIND POWER PLANTS

Offshore wind turbine plants can be placed close to and in long distance to shore. Figure 1-3 plots large-scale offshore wind power plants constructed between 2010 and 2015, depending on the power capacity and electrical transmission distance [3]. The power capacity range of each offshore wind power plant seems to be between a hundred and up to a thousand MW and even more in some areas. The electrical transmission distance from the offshore wind farm to Point of Common Coupling (PCC) located at the onshore side seems to be in the range from a few km to 200 km. It is noted that two types of electrical transmission system exist, which are Alternating Current (AC) transmission system, and Direct Current (DC) transmission system, which have been selected when considering the cost of the transmission system. It highly depends on the transmission distance and other site conditions such as water depth and also transmission system voltage. The break-even distance seems to be around 100 km as far as the recent existing projects. The system configurations of the two types offshore wind power plants are described as follows.

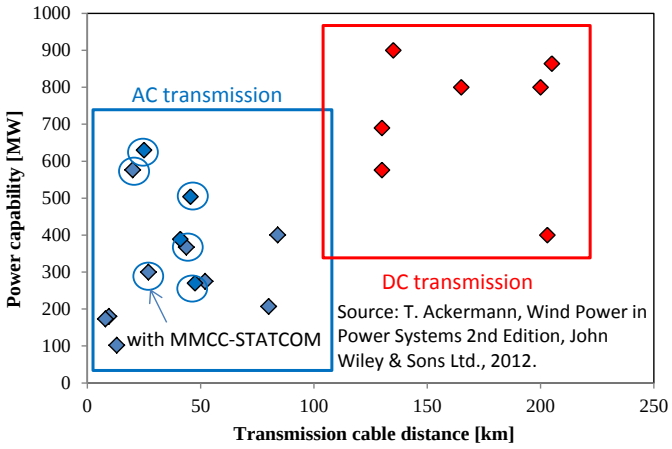
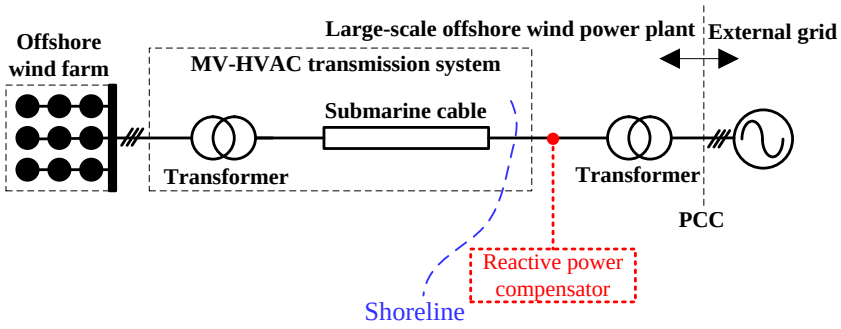


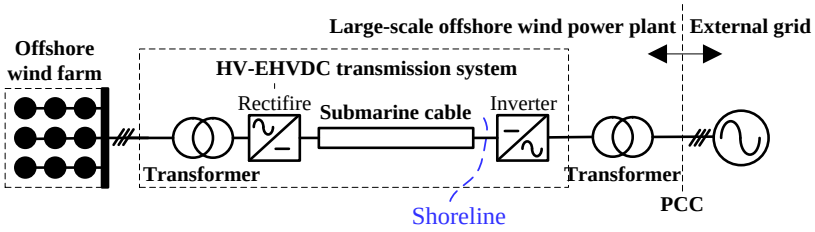
Figure 1-3 Offshore wind power plants constructed from 2010 to 2015 with different transmission systems.

Figure 1-4 (a) shows the system configuration of a typical offshore wind power plant with AC transmission system, which voltage range typically becomes Medium Voltage to High Voltage (MV-HV). The generated active power in offshore wind turbines are transmitted to the PCC by MV-HVAC transmission system with submarine cables. In order to obtain as high voltage as possible between one side and another side, transformers are installed in the offshore wind power plant. It is noted that, where the submarine cable has a long distance, reactive power compensation is required.

Figure 1-4 (b) shows the system configuration of a typical offshore wind power plant with a DC transmission system, which voltage range typically becomes High Voltage to Extra High Voltage (HV-EHV). The generated active power in the offshore wind farm is transmitted to the PCC by HV-EHVDC transmission system with long distance submarine cables, which does not cause reactive power. Therefore, when the distance of the transmission system is longer, the DC transmission system has been selected although it requires expensive AC/DC converter (Rectifier) and DC/AC converter (Inverter).



(a) Offshore wind power plant with AC transmission system



(b) Offshore wind power plant with DC transmission system

Figure 1-4 System configurations of typical offshore wind power plants.

In this thesis, the offshore wind power plant with long distance HVAC transmission system is in focus. Lot of cases exist of this plant type, and typically the reactive power compensator is installed to compensate a large amount of reactive power arisen by the impedance from long distance submarine cables, and also in order to satisfy the grid code. Figure 1-5 shows various types of reactive power compensators for offshore wind power plant. A brief explanation of each type is introduced as follows [2], [4]:

(a) Shunt reactor/Static condenser: The inductor or capacitor is connected in parallel to the grid, which can compensate lead/lag reactive power, respectively. In case of offshore wind power plant, the shunt reactor may be connected to compensate the reactive power arisen by large amount of parasitic capacitance in the long distance submarine cables. It is obviously that it cannot change the compensation amount of the reactive power, although the compensating reactive power to be required changes with each moment.

(b) Static Var Compensator (SVC): SVC can compensate both lead/lag reactive power variably by control of the switching timing of the Thyristor. However, the SVC gives a lot of low-order harmonic currents to the grid by the switching operation of the thyristor, which requires a large amount of passive filters. In addition, when the grid voltage drop by short-circuit grid fault, the reactive power compensation capability of the SVC is significantly reduced, although the reactive power delivering capability under grid fault should according to recent grid codes for large scale offshore wind power plant.

(c) Static Synchronous Compensator (STATCOM): STATCOM could have the highest performance, but it is a more expensive reactive power compensator compared to the three types, which is constructed by Voltage Source Converter (VSC). It can also induce both lead/lag reactive power variably with very fast response and with very small low-order harmonic currents. Then, the reactive power compensation capability does not decrease even if grid voltage drops by a short-circuit grid fault. It is noted that, when the asymmetrical grid fault happens, one type of VSC has a limitation to deliver the reactive current, but it is much better than the SVC.

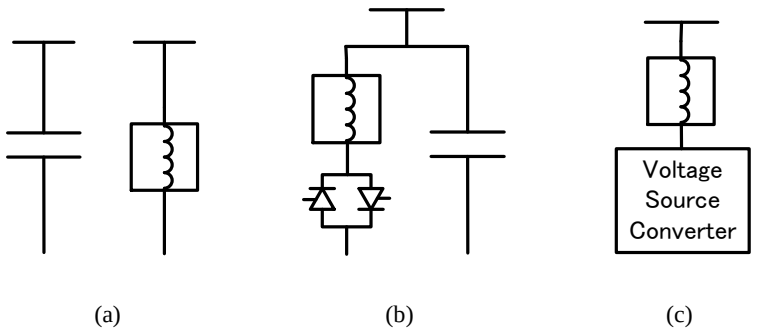


Figure 1-5 Reactive power compensators. (a) Shunt reactor/Static condenser. (b) Static Var Compensator (SVC). (c) Static Synchronous Compensator (STATCOM).

The STATCOM has become the preferable solution for the offshore wind power plant with long distance HVAC transmission system, and it has been selected in some existing offshore wind power plants as shown in Figure 1-3.

1.1.3. STATCOM TECHNOLOGY FOR OFFSHORE WIND POWER PLANTS

Figure 1-6 shows three types of potentially used high voltage and high power STATCOMs for offshore wind power application. It is noted that the circuit configuration is depicted as a per phase circuit configuration in the figure for simple explanations, but it is a three-phase system in the actual systems. The rated power and voltage for the STATCOM application become several tens of MVar and several tens of kV, respectively. Self-turn-off power devices such as Insulated Gate Bipolar Transistor (IGBT) and Integrated Gate Commutated Turn-off thyristor (IGCT) have been used for the STATCOMs [5]. The symbol of the power device is depicted as an IGBTs. Table 1-1 summarizes the characteristics of each circuit configuration. The details of each circuit configuration are explained as follows.

The circuit configuration (a): The reactive power is controlled by a traditional voltage source using two-level (or neutral point clamped three-level [6]) converter. In order to increase the rated voltage of the converter, the IGBT devices are connected in series. It seems that this solution is the cheapest solution. However, depending on the required rated voltage, the series connection counts of the number of IGBT increases. When only one IGBT device in an arm is broken, the STATCOM cannot operate anymore. This may practically be a problem.

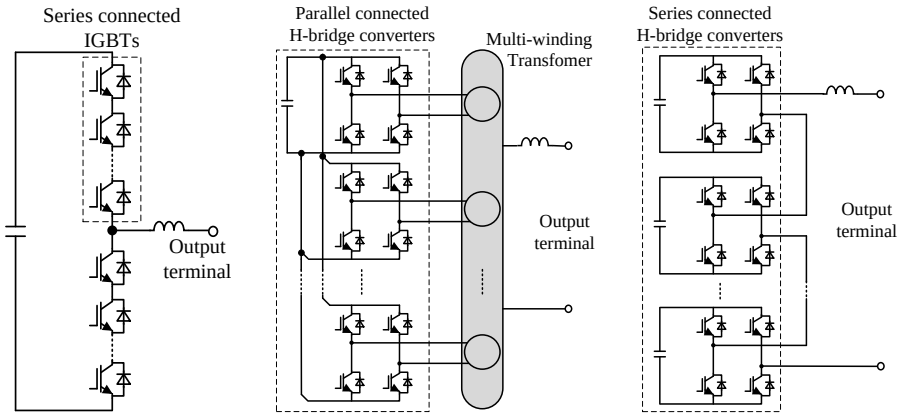
The circuit configuration (b) [7]*:* The ac sides of the single-phase converters such as H-bridge converter having common dc-link terminals are connected to each winding of the input side of the multiplex transformer, where the transformer multiplexes each converter voltage in series. In this result, the output voltage of the multiplex transformer can obtain a high voltage with multi-level waveforms, which will reduce the amount of necessary harmonic filter. However, the multiplex transformer is very expensive and heavy. It is noted that, by redundantly designing the number of the single phase converters, this configuration can continue its operation even if one of the single phase converters is broken.

The circuit configuration (c) [8, 9, 10, 11, 12]*:* Single-phase converters such as H-bridge converters are directly connected in series in order to increase the system rated voltage. This circuit configuration also gains multi-level voltage waveforms, and also redundant operation. However, as only this circuit configuration becomes galvanic isolated of each dc-link terminal of the single-phase converter, each dc-link capacitor voltage has the double frequency voltage ripple at the source frequency, which increases the dc-link capacitor size. In addition, this circuit configuration has a limitation for asymmetrical Fault Ride Through operation, which performance is highly required in recent grid codes as described in the next section.

Nowadays, the circuit configuration in (c) becomes the mainstream solution for the STATCOM, because of significant advantages compared to the conventional

configuration (a) and (b) as it is mentioned above, like lower harmonic distortions, multiplex transformer-less configuration, and modular/ redundant design. Nevertheless, in addition to the capacitor size, voltage-balancing for a large number of DC-link capacitors in the converter cells are still challenging to be achieved for MMCCs, especially under asymmetrical grid faults [4], [13], [14], [15].

Based on this comparison, the MMCC solutions are selected for further study.



(a) Series-connected switches solution (b) Multi-winding transformer solution (c) MMCC solution

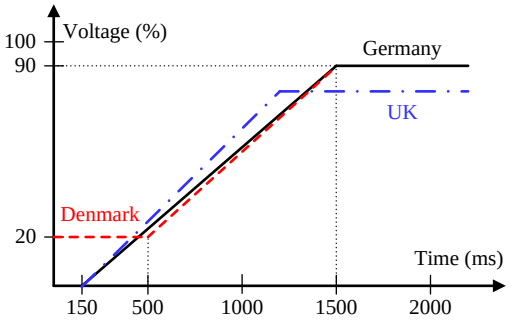
Figure 1-6 Candidates for high voltage and high power STATCOM configuration for offshore wind power plant (Per-phase circuit is depicted).

Table 1-1 Characteristics of each circuit configuration in Figure 1-6 for the STATCOM application.

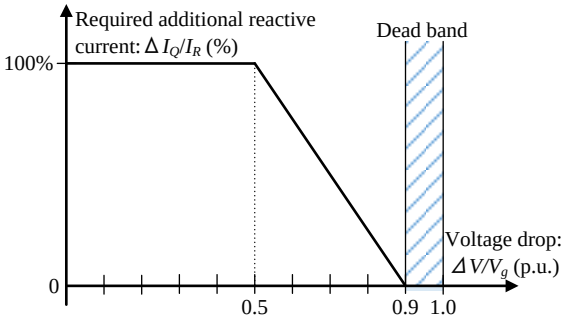
	(a) Series-connected switches solution	(b) Multi-winding transformer solution	(c) MMCC solution
Cost	+++	+	++
- Harmonic filter	Medium	Small (multi-level voltage)	Small (multi-level voltage)
- Multiplex transformer	No	Yes	No
- DC-link capacitor	Small	Small	Large (low frequency voltage ripple by identical DC-link)
Redundancy operation	No	Yes	Yes
Asymmetrical Fault Ride Through operation	+++	+++	++

1.1.4. FAULT RIDE THROUGH REQUIREMENTS

Besides the normal operation, the Transmission System Operators (TSOs) in different countries have issued strict grid supporting requirement for the growing large-scale renewable power plants under grid fault, which is specified in Figure 1-7 [16], [17]. According to the grid codes, the offshore wind power plant has to keep the operation regarding the voltage sag under grid fault as shown in Figure 1-7 (a), and in the case of German and Danish grid codes, it should be able to inject additional reactive current to support the recovery of grid voltage sag which is also shown in Figure 1-7 (b). It is noted that recent grid codes are not requiring negative-sequence reactive current injection, which contributes to recover asymmetrical grid fault voltages. The detail of the negative-sequence current injection can only be found only in Germany grid code as an option for the moment [18]. Therefore, Fault Ride Through capability of the STATCOM becomes more and more important.



(a) LVRT requirement by different countries.



(b) Additional reactive current requirements during LVRT

Figure 1-7 Reactive power requirements of large-scale generating plants under grid fault (low voltage ride through) [19].

1.2. RESEARCH QUESTIONS AND OBJECTIVES

This thesis focuses on the promising MMCC-based STATCOM solution for the rapidly growing offshore wind application. The following issues are qualified in this thesis, which has become open questions.

1. *Which type of MMCC solutions is the best to be in the offshore wind power plants operating as STATCOM? This question gives the following objectives in the thesis.*

   - ✓ Specifications and the component sizing of potentially four types of MMCC solutions for the STATCOM application are compared. The total cost and volume are of interest based on the total power semiconductor chip area and total energy stored in the passive components.
   - ✓ Mathematical formulation of the STATCOM based on the MMCC solutions under asymmetrical compensation operation is developed, which contributes to the quantitative understanding of the performance limitation and circuit behavior for the Fault Ride Through (FRT) operation.
   - ✓ The FRT capacity focusing on the MMCC solutions need to be compared under different grid faults scenarios with the consideration of actual device limitations.
   - ✓ The most attractive MMCC solution for the STATCOM application should be suggested based on the obtained results.

2. *Exist there any dc-link capacitor reduction method for the MMCC solutions?*

   - ✓ A dc-link capacitor voltage ripple reduction method for MMCC-based STATCOM should be proposed.
   - ✓ Also dc-link capacitor volume reduction effect by applying the developed method should be estimated.

1.3. LIMITATIONS ON THIS STUDY

Due to the large efforts to prepare the MMCC systems in practice, experimental setups are not developed in this thesis. However, this thesis proposes mathematical models and computer simulation models of the four types of the MMCC-based STATCOMs. The simulation models are carefully designed and they are based on a practical 80 MVar/33 kV STATCOM model. The realistic cell counts, power modules, and control strategies are taken as much as possible into account in order to clarify the research objectives.

1.4. OUTLINE OF THE THESIS

The Ph. D. dissertation consists of six chapters, which are introduced as follows:

Chapter 1: Introduction

The background and motivation for the research are first presented. Then, the objective of the research is described as well. Finally, the outline of this dissertation is described.

Chapter 2: Modeling and control of the MMCC solutions for offshore wind STATCOM Application

As preparatory for the study, the system configuration of the typical offshore wind power plant, grid fault scenarios, and also the fundamental control scheme of the potentially used configurations of the MMCC solutions for the STATCOM application are summarized. Then, specifications and the component sizing of each type of practical 80 MVar / 33 kV scaled MMCC-STATCOM are carefully designed and compared.

Chapter 3: Theoretical operation of MMCC family under asymmetrical reactive power compensation

The mathematical formulation for the STATCOM based on the MMCC solutions under asymmetrical compensation operation is developed, which contributes to the quantitative understanding of the performance limitation and also the circuit behavior under asymmetrical grid fault operation.

Chapter 4: Performance benchmark of the MMCC solutions

The electro-thermal stresses of the actual power modules used in each type of the MMCC with practical controls are analyzed in detail. The asymmetrical reactive power capacity focusing on the MMCC solutions is compared under different scenarios of grid faults, with the consideration of device temperature limits and voltage saturation. The most attractive MMCC solution for the STATCOM application is suggested based on the obtained results.

Chapter 5: DC-link Capacitor Voltage Ripple Reduction Method for an MMCC-SDBC

This chapter proposes a capacitor voltage ripple reduction method by using a third harmonic zero-sequence current for Modular Multilevel Cascade Converter (MMCC) with Single Delta Bridge Cells (SDBC). A practical case study on an 80 MVar/ 33 kV MMCC-SDBC based STATCOM is used to demonstrate the method. The impact of the third harmonic zero-sequence current level of the capacitor oscillation reduction and the electro-thermal stresses on the IGBT modules are investigated. An optimal parameter of the current level is obtained by compromising the above two performance factors. The capacitor bank volume is also estimated and compared.

Chapter 6: Conclusions

This chapter gives a summary, the main findings, and conclusion of this study. Topics for future research are also listed.

At the end of the thesis, the published papers during the Ph.D. study period are attached.

1.5. LIST OF PUBLICATIONS

A list of journal papers related to the thesis, which have been published or submitted until now, is given as follows:

[J1] T. Tanaka, H. Wang, K. Ma, and F. Blaabjerg, "Asymmetrical Fault Ride Through Capability of a STATCOM based on Modular Multilevel Cascade Converters," *IEEE Trans. Power Electron.* (in press)

[J2] T. Tanaka, H. Wang, and F. Blaabjerg, "DC-link Capacitor Voltage Ripple Reduction Method of an MMCC-SDBC by Third Harmonic Zero-sequence Current Injection," *IEEE Trans. Ind. Appl.* (under review)

A list of conference papers related to this thesis is given as follows.

[C1] T. Tanaka, H. Wang, K. Ma, F. Blaabjerg, "Reactive Power Compensation Capability of a STATCOM based on Two Types of Modular Multilevel Cascade Converters for Offshore Wind Application," in *Proc. IEEE ECCE Asia*, pp.326 - 331, Jun. 2017.

[C2] T. Tanaka, H. Wang, K. Ma, F. Blaabjerg, "Low Voltage Ride Through Performance of a STATCOM based on Modular Multilevel Cascade Converter Family for Offshore Wind Application," in *Proc. IEEE ECCE*, pp. 4879 - 4886, Oct. 2017.

[C3] T. Tanaka, H. Wang, K. Ma, F. Blaabjerg, " Low Voltage Ride Through Capability of a STATCOM based on Modular Multilevel Cascade Converters for Offshore Wind Application," *IEEE eT&D workshop*, Nov. 2017.

[C4] T. Tanaka, H. Wang, F. Blaabjerg, " A DC-link Capacitor Voltage Oscillation Reduction Method for a Modular Multilevel Cascade Converter with Single Delta Bridge Cells (MMCC-SDBC)," in *Proc. IEEE ECCE Asia*, pp. 2604 – 2610, May 2018.

CHAPTER 2. MODELING AND CONTROL OF THE MMCC SOLUTIONS FOR OFFSHORE WIND STATCOM APPLICATION

As preparatory for the study, this chapter summarizes the system configuration of a typical offshore wind power plant including reactive power requirements, grid fault scenarios, and fundamental control scheme of the potentially used configurations of the MMCC solutions for the STATCOM application. Then, specifications and the component sizing of each type of practical 80 MVar / 33 kV scaled MMCC-STATCOM are carefully designed. The total cost and volume are compared based on the total amount of power semiconductor chip area and total energy stored in the passive components.

2.1. TYPICAL OFFSHORE WIND POWER PLANT AND SYSTEM FAULT SCENARIOS [J1]

2.1.1. SYSTEM CONFIGURATION [19]

Figure 2-1 shows the system configuration of a typical offshore wind power plant and an MMCC-based STATCOM. The generated active power from the offshore wind farm needs to be provided to the Point of Common Coupling (PCC) as *Bus* A (400 kV in this case) by an HVAC transmission system (220 kV in this case) with long distance submarine cables. Reactive power induced by the submarine cable is typically compensated by the full-scale converters of wind turbines, the shunt reactor, and the STATCOM connected to *Bus* B via a delta-star transformer. Other power generators and loads besides the wind power plant may also be connected to *Bus* A.

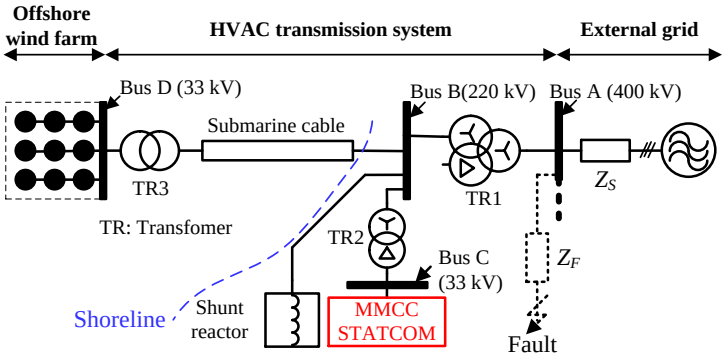


Figure 2-1 A typical offshore wind power plant with an MMCC-STATCOM and shunt reactor [19].

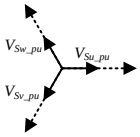
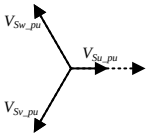
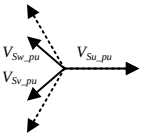
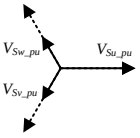
2.1.2. REACTIVE CURRET REQUIREMENT

In order to compensate reactive power arisen by long-distance submarine cable and satisfy the grid codes, a STATCOM may be installed in offshore wind power plant. In addition, as mentioned in section 1.1.4, the offshore wind power plant has to keep the operation regarding the voltage sag under grid fault, and in the case of some countries it should be able to inject additional reactive current to support the recovery of the grid voltage sag. The reactive current reference is only defined as positive-sequence component because today's grid codes do not require negative-sequence current to compensate for the asymmetrical grid fault voltage recovery.

2.1.3. GRID FAULT SCENARIOS [19]

Table 2-1 shows the representative grid fault voltage phasors and vectors corresponding to the three-phase-to-ground fault, single-phase-to-ground fault, phase-to-phase short-circuit fault and two-phase-to-ground fault [20], [21]. Here, V_{Su_pu}, V_{Sv_pu}, and V_{Sw_pu} are each phase voltage standardized on *Bus* A by the rated voltage. It is assumed that the short-circuit faults happen somewhere on a feeder with the line impedance Z_F to *Bus* A (PCC) in Figure 2-1. The line impedance from the PCC to the grid with a higher voltage level is Z_s. A voltage dip severity D is determined by the ratio of the Z_s and Z_F with positive-, negative- and zero-sequence impedances. In order to simplify the grid fault scenarios, the dip severity D is considered as a real part only. More details are explained and classified in [22], [23].

Table 2-1 Phasor diagram and vector definitions of different grid fault scenarios on PCC (*BUS* A) [19]

Fault types	Phasor diagram definitions	Vector definitions
(a) Three-phase-to-ground fault		$\dot{V}_{Su\_pu} = D$ $\dot{V}_{Sv\_pu} = -\frac{1}{2}D - j\frac{\sqrt{3}}{2}D$ $\dot{V}_{Sw\_pu} = -\frac{1}{2}D + j\frac{\sqrt{3}}{2}D$
(b) Single-phase-to-ground fault		$\dot{V}_{Su\_pu} = D$ $\dot{V}_{Sv\_pu} = -\frac{1}{2} - j\frac{\sqrt{3}}{2}$ $\dot{V}_{Sw\_pu} = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$
(c) Phase-to-phase short-circuit fault		$\dot{V}_{Su\_pu} = 1$ $\dot{V}_{Sv\_pu} = -\frac{1}{2} - j\frac{\sqrt{3}}{2}D$ $\dot{V}_{Sw\_pu} = -\frac{1}{2} + j\frac{\sqrt{3}}{2}D$
(d) Two-phase-to-ground fault		$\dot{V}_{Su\_pu} = 1$ $\dot{V}_{Sv\_pu} = -\frac{1}{2}D - j\frac{\sqrt{3}}{2}D$ $\dot{V}_{Sw\_pu} = -\frac{1}{2}D + j\frac{\sqrt{3}}{2}D$

In this thesis, three asymmetrical grid-fault scenarios are chosen to be studied as shown in Table 2-1 (b), (c) and (d), where the asymmetrical grid fault voltage on *Bus* A propagated to *Bus* B, the *Bus* A and *Bus* B voltages do not appear significant different due to the used neutral point grounded wye-wye-delta transformer TR1. However, the voltage on *Bus* B shows different characteristics, when it is propagated to *Bus* C, which is seen by the STATCOM due to the used delta-wye transformer TR2. Table 2-2 shows the asymmetrical grid fault scenarios on *Bus* C corresponding to each grid fault. The V_{dq}^{+}, V_{dq}^{-} and V^{0} are positive-, negative and zero-sequence component of the voltage on dq domain, respectively, which are defined as scenarios used in this thesis.

Table 2-2 Sequence voltage amplitude definition of different grid fault scenarios on *Bus* C [19]. (The V_S is the rated voltage on *Bus* C.)

Fault types	Each sequence voltage vector
(b) Single-phase-to-ground fault	$\begin{bmatrix} V_{dq}^{+} \\ V_{dq}^{-} \\ V^{0} \end{bmatrix} = V_S \begin{bmatrix} \frac{D}{3}+\frac{2}{3} \\ \frac{D}{6}-\frac{1}{6}+j\left(\frac{D}{2\sqrt{3}}-\frac{1}{2\sqrt{3}}\right) \\ 0 \end{bmatrix}$
(c) Phase-to-phase short-circuit fault	$\begin{bmatrix} V_{dq}^{+} \\ V_{dq}^{-} \\ V^{0} \end{bmatrix} = V_S \begin{bmatrix} \frac{D}{2}+\frac{1}{2} \\ -\frac{D}{4}+\frac{1}{4}+j\left(-\frac{\sqrt{3}D}{4}-\frac{\sqrt{3}}{4}\right) \\ 0 \end{bmatrix}$
(d) Two-phase-to-ground fault	$\begin{bmatrix} V_{dq}^{+} \\ V_{dq}^{-} \\ V^{0} \end{bmatrix} = V_S \begin{bmatrix} \frac{2}{3}D+\frac{1}{3} \\ -\frac{D}{6}+\frac{1}{6}+j\left(-\frac{D}{2\sqrt{3}}+\frac{1}{2\sqrt{3}}\right) \\ 0 \end{bmatrix}$

2.2. COMPARISON OF KEY DEVICES FOR EACH TYPE OF THE MMCC-BASED STATCOM [J1]

An 80 MVar / 33 kV case study for a practical STATCOM application is chosen in this thesis. Figure 2-2 shows the potentially used circuit configurations for the STATCOM based on MMCC. The MMCC with Single Star Bridge Cells (SSBC) has a star connection constructed by H-bridge converters. The MMCC with Single Delta Bridge Cells (SDBC) has a delta connection constructed by H-bridge converters. The MMCC with Double Star Chopper Cells (DSCC) and Double Star B ridge Cells have two star connections constructed by chopper converters and H-bridge converters, respectively. The difference of the connection type and cell configuration in the MMCC solutions show different cell counts and rated cell current when the output voltage and current of the MMCC solutions are designed to have the same value.

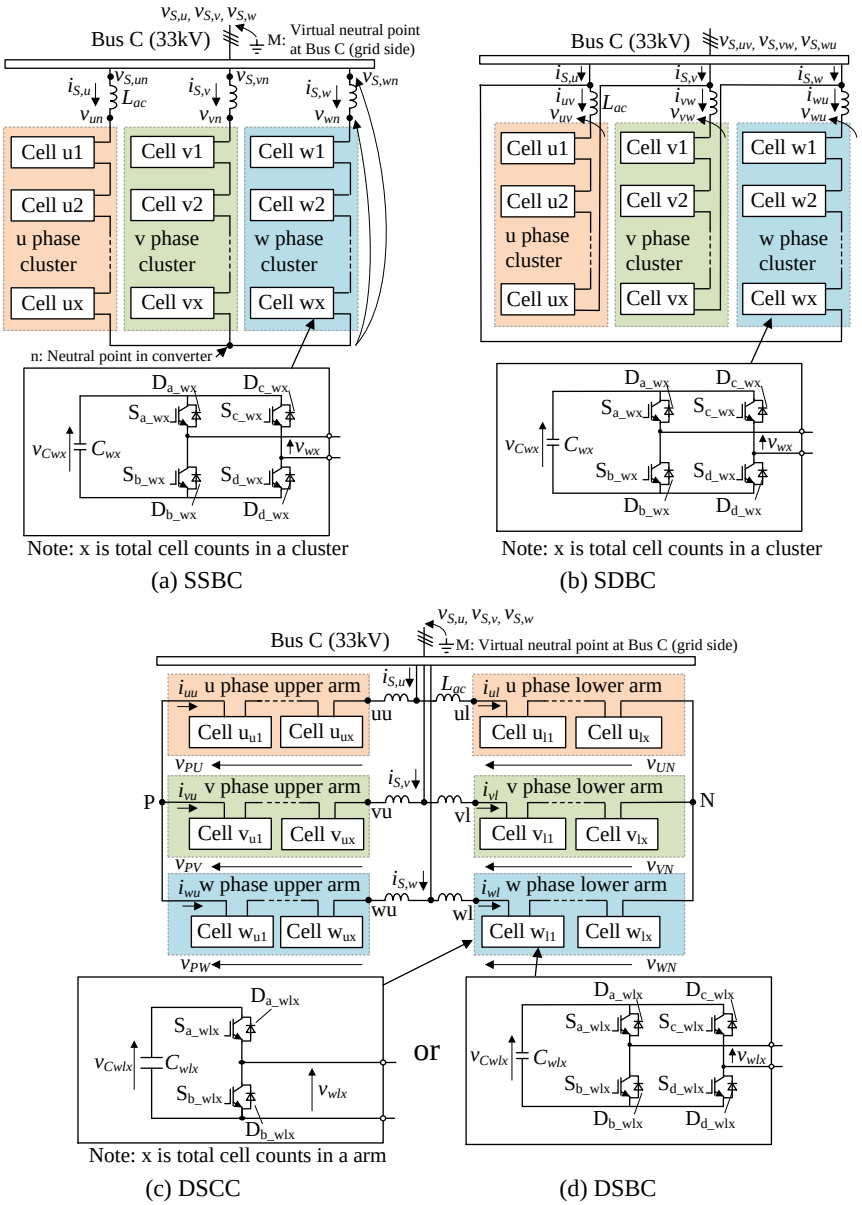


Figure 2-2 Circuit configurations of the MMCC family for a STATCOM application [19].

Table 2-3 shows the specifications, the cell numbers and key components for the specific application. The design procedure is given from next page.

Table 2-3 The MMCC specifications for the case study **[19]**

Circuit type of MMCC	SSBC	SDBC	DSCC	DSBC
Rated power Q_r	±80 MVA			
Rated line-to-line voltage V_s	33 kVrms (Source angular frequency ω_s : 2π×50 rad/s)			
Rated DC-link voltage each cell $V_{C,dc}$	2600 Vdc			
Nominal output voltage each cell	AC 1450 Vrms DC 0 Vdc		AC 725 Vrms DC 1300 Vdc	AC 1450 Vrms DC 0 Vdc
Equivalent switching frequency f_{eq_sw}	10 kHz (with Phase Shift PWM)			
Number of total cells N_{cell}	39 (13 cells/cluster)	69 (23 cells/cluster)	156 (26 series/arm)	78 (13 series/arm)
Number of total switching devices N_{sw}	156	276	312	312
Rated output current of each cell I_r	1400 Arms	808 Arms	700 Arms	700 Arms
Carrier frequency f_c	380 Hz	215 Hz	190 Hz	190 Hz
Total energy stored in interconnection inductor E_L	15 kJ (L_{ac} = 2.6 mH)	15 kJ (L_{ac} = 7.8 mH)	15 kJ (L_{ac} = 5.2 mH)	15 kJ (L_{ac} = 5.2 mH)
Total energy stored in dc-link capacitor E_C	1.6 MJ (C_x = 12 mF)	1.6 MJ (C_x = 7.0 mF)	6.3 MJ (C_x = 12 mF)	1.6 MJ (C_x = 6.0 mF)
IGBT module	MBN1500FH45F (4500V/1500A)	MBN900D45A (4500V/900A)	MBN800H45E2 (4500V/800A)	MBN800H45E2 (4500V/800A)

2.2.1. BASIC STRUCTURE AND POWER SEMICONDUCTOR DEVICES [19]

The rated DC-link voltage $V_{C,dc}$ of each converter cell in the four types of MMCC solutions are designed to be the same at 2600 Vdc where the widely used 4.5 kV IGBT modules are selected for each converter cell in this thesis. The nominal output AC voltage of each converter cell in the SSBC, SDBC and DSBC is designed at 1450 Vrms with the nominal modulation factor α_n = 0.8. The margin of the modulation factor (0.2) is determined by the voltage drop of the output impedance, current control dynamics, pulse width limitation due to dead time, and also in order to achieve modular redundancy. However, the circuit configuration of the converter cell for the DSCC is a chopper converter, which cannot output negative voltage. Because +/- output voltage is also required for the DSCC based STATCOM, the output voltage in each chopper converter cell is superimposed with the half value of the rated DC-voltage (i.e. 1300 Vdc). When the above design guideline is followed, the nominal output AC voltage of each converter cell in the DSCC becomes 725 Vrms AC with the nominal modulation factor for the AC component α_n = 0.8.

Table 2-4 The key equations for the design of the MMCC solutions [19].

	SSBC	SDBC	DSCC	DSBC
The cell converter counts N_{cell}	$\frac{\sqrt{6}V_s}{\alpha_n V_{C,dc}}$	$\frac{3\sqrt{2}V_s}{\alpha_n V_{C,dc}}$	$\frac{4\sqrt{6}V_s}{\alpha_n V_{C,dc}}$	$\frac{2\sqrt{6}V_s}{\alpha_n V_{C,dc}}$
Rated output current of each cell I_r	$\frac{Q_r}{\sqrt{3}V_s}$	$\frac{Q_r}{3V_s}$	$\frac{Q_r}{2\sqrt{3}V_s}$	
The interconnection inductance L_{ac}	$\frac{Z_{pu}V_s^2}{\omega_S Q_r}$	$\frac{3Z_{pu}V_s^2}{\omega_S Q_r}$	$\frac{2Z_{pu}V_s^2}{\omega_S Q_r}$	
The DC-link capacitance of each cell C_x	$\frac{\sqrt{2}\alpha Q_r}{2\sqrt{3}\omega_S \Delta V_{C,pu} V_{C,dc} V_s}$	$\frac{\sqrt{2}\alpha Q_r}{6\omega_S \Delta V_{C,pu} V_{C,dc} V_s}$	$\frac{\sqrt{2}Q_r}{2\sqrt{3}\omega_S \Delta V_{C,pu} V_{C,dc} V_s}$	$\frac{\sqrt{2}\alpha Q_r}{4\sqrt{3}\omega_S \Delta V_{C,pu} V_{C,dc} V_s}$
Total energy stored in dc-link capacitor E_C	$\frac{\alpha Q_r}{2\alpha_n \Delta V_{C,pu}\omega_S}$		$\frac{2Q_r}{\alpha_n \Delta V_{C,pu}\omega_S}$	$\frac{\alpha Q_r}{2\alpha_n \Delta V_{C,pu}\omega_S}$

V_S: Rated line-to-line Voltage, α_n: Nominal modulation factor, $V_{c,dc}$: Rated DC-link voltage each cell, Q_r: Rated reactive power, Z_{pu}: Normalized impedance, ω_s: Source angular frequency, α: modulation index of each cell converter, $\Delta V_{c,pu}$: Normalized DC-link capacitor voltage ripple.

The cell converter counts N_{cell} of the MMCC solutions with SSBC, SDBC, DSCC and DSBC are expressed by the equations in Table 2-4, respectively, where V_S is the rated line to line voltage at *Bus* C, α_n is the nominal modulation factor for the AC component, and $V_{C,dc}$ is the rated DC-link voltage. N_{cell} of each MMCC solution is determined by the ratio between grid voltage and the dc-link capacitor voltage of each cell converter, the difference of connection type of each MMCC such as star, delta, or double star, and the difference of the cell converter configuration such as H-bridge or chopper converter. Then, total number of switching devices N_{sw} for each MMCC topology is derived by each cell converter configuration and N_{cell}.

The rated output currents I_r in each cell among the MMCC solutions are also expressed by the equations in Table 2-4, respectively. The current ratings of the IGBT modules in each of the cell converter among the MMCC solutions are selected depending on the I_r. It is worth to note that the N_{sw} and N_{cell} among the MMCC solutions are different. However, the equivalent total power semiconductor chip area calculated by the total IGBT module counts, the current capacity of each IGBT module and the rated voltage of each IGBT module, which strongly influence the total cost of the STATCOM, seems approximately to have the same values.

2.2.2. MODULATION TYPE AND FREQUENCIES FOR PWM [19]

Phase-shift PWM modulation is chosen because of the advantage that the electro-thermal stresses of the IGBT modules and capacitors are equally distributed among the cells in the same cluster (or arm). The equivalent switching frequency of the MMCC f_{eq_sw} is designed to be the same at 10 kHz. In this thesis, the carrier frequency f_c of the MMCC solutions with SSBC and SDBC are 380 Hz and 215 Hz, respectively. The carrier frequency f_c of the MMCC solutions with DSCC and DSBC are the same being 190 Hz. It is noted that f_c of each MMCC solution should not be an integer multiple of the fundamental frequency in order to avoid diverging the capacitor voltages among the cells, when f_c is below several hundred Hz [24], [25].

2.2.3. INTERCONNECTION INDUCTANCE [19]

In this case study, the L_{ac} is designed as 6 % of the normalized impedance Z_{pu} based on 33 kV and 80 MVA operating condition of converter. In this design rule, the L_{ac} of the MMCC solutions with SSBC, SDBC, DSCC and DSBC are calculated by the equations in Table 2-4. The total energy stored in the whole interconnection inductor E_L has the same value among the MMCC solutions in this designed case, which in practical will strongly influence the total volume of the STATCOM.

2.2.4. DC-LINK CAPACITANCE [19]

The DC-link capacitance of each cell C_x is designed as the capacitor voltage ripple scaled by the rated DC-link voltage $V_{c,dc}$ (2600 V). The voltage ripple $\Delta V_{c,pu}$ is designed to be 10% below the nominal rated operation. The relationship between the voltage ripple and the capacitance C_x of the MMCC solutions with SSBC, SDBC, DSCC and DSBC are also expressed by the equations given in Table 2-4 based on an averaging model, respectively [26], [27]. Here, α is a modulation factor of a cell, which is set to be α =1 and it is assumed to be the largest voltage ripple in this case study. The total energy stored in all dc-link capacitors E_C among the MMCC solutions can be expressed as

$$E_C = \frac{N_{cell}}{2} C_x V_{C,dc}^2 \tag{2.1}$$

After N_{cell}, C_x and I_r as shown in Table 2-4, are substituted for (2.1), the E_C among the MMCC solutions are updated to the formulation as shown in Table 2-4. It is noted that E_C for SSBC, SDBC and DSBC is the same. However, the E_c of the DSCC is 4 times larger than the others because of the used chopper cells. As an example, where E_C of the DSCC are compared with the DSBC, both the N_{cell} and the C_x of the DSCC become twice higher than the DSBC because of the used chopper cells with the output voltage including the superimposed half value of the rated dc-voltage $V_{C,dc}$. It should be noted that the E_C depends greatly on the total size of the MMCC converter.

2.3. CONTROL STRATEGY FOR THE MMCC-BASED STATCOMS

The modulation scheme for the MMCC with SSBC, SDBC, DSCC and DSBC are selected to be the widely-used Phase Shift PWM, because of the advantage that the electro-thermal stresses of the power devices and capacitors are equally distributed among the cells in the same cluster (or arm) [28].

Figure 2-3 shows the overall control block for the MMCC STATCOM solutions, which consist of output current control block, Phase Locked Loop (PLL) block, overall voltage control block for the dc-link capacitor in cell converters, and the dc-link capacitor voltage balancing control block for each cell converter. Here, the reference of positive-sequence reactive current $I^{+}_{S,q,ref}$ is given from the central control of the wind power plant under normal operation. In this result, the STATCOM has two operating modes which are inductive operation in the case of $I^{+}_{S,q,ref} < 0$ and capacitive operation in the case of $I^{+}_{S,q,ref} > 0$. When a grid fault happens, the additional amount of $I^{+}_{S,q,ref}$ may be required due to a recent published grid code of Transmission System Operators (TSOs) [17]. The $I^{-}_{S,d,ref}$ and $I^{-}_{S,q,ref}$ are set to be zero value according to the mentioned recent grid codes. The detail of each control block is described below.

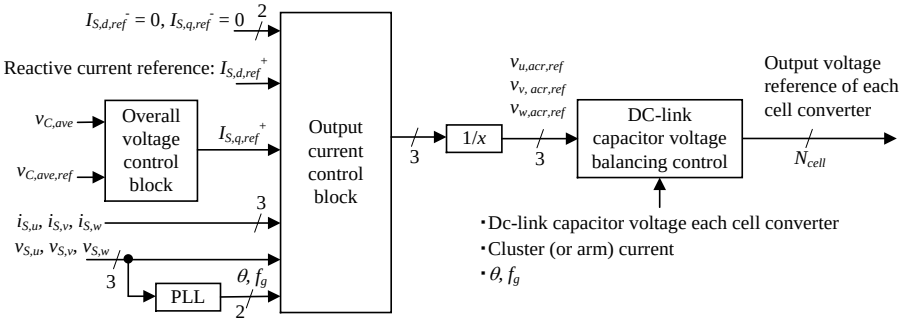


Figure 2-3 Overall control block for the MMCC STATCOM solutions.

2.3.1. OUTPUT CURRENT CONTROL BLOCK

Figure 2-4 shows the output current control block for the MMCC-STATCOM solutions. This control function controls the positive- and negative-sequence output current $I_{s,d}^{+}$, $I_{s,q}^{+}$, $I_{s,d}^{-}$, $I_{s,q}^{-}$ of the MMCC-STATCOM solutions on dq frame to the reference values $I_{s,d,ref}^{+}$, $I_{s,q,ref}^{+}$, $I_{s,d,ref}^{-}$, $I_{s,q,ref}^{-}$, by a dual-frame control scheme with a sequence decoupling using a notch filter [29, 30, 31].

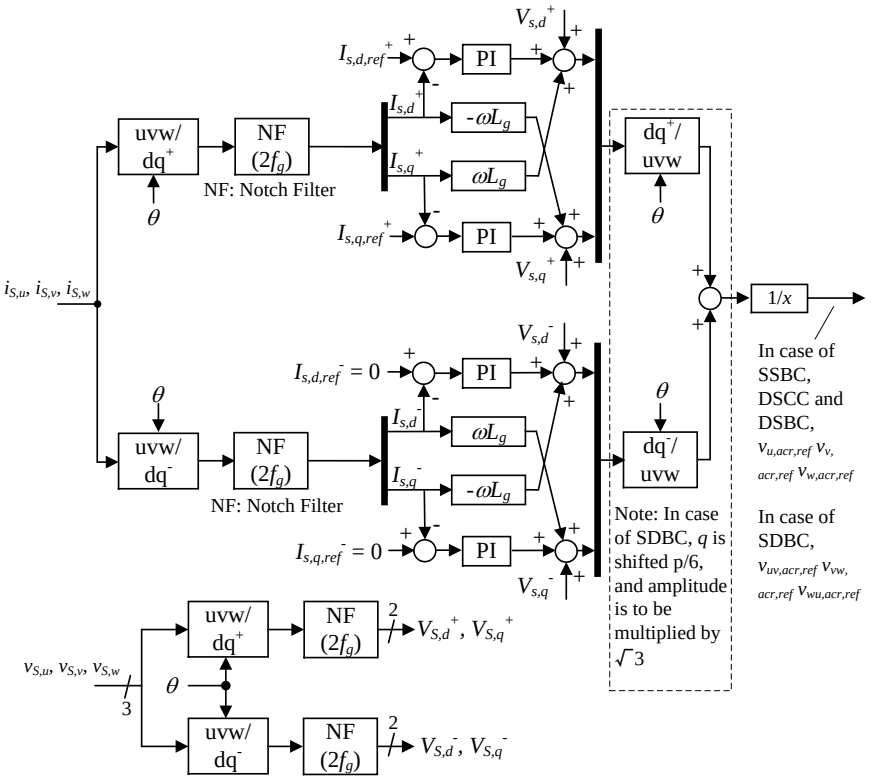


Figure 2-4 Output current control block diagram for the STATCOMs used in the thesis.

2.3.2. PHASE LOCKED LOOP (PLL) BLOCK

The frequency and phase angle of the grid voltage is detected by the PLL block [31], [32]. The standard position of the phase angle is set to be along the d-axis of the positive-sequence grid voltage.

2.3.3. OVERALL VOLTAGE CONTROL BLOCK

The average value $v_{c,ave}$ of all dc-link capacitor voltages in the MMCC is controlled to the designed value $v_{c,ref}$ by using positive-sequence active current, where the reference value $i_{s,q,ref}^{+}$ is produced by the overall voltage control block as shown in Figure 2-5. This control scheme is the same among the four types of the MMCC.

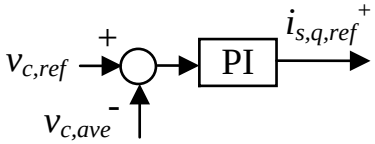


Figure 2-5 Overall voltage control block diagram for dc-capacitors.

2.3.4. DC-LINK CAPACITOR VOLTAGE BALANCING CONTROL BLOCK

As a common issue among all MMCC types, the dc-link capacitor voltage in each cell converter has to be kept within the designed value by activating the dc-link capacitor voltage balancing control, which strategy is shown in Figure 2-6 [33, 34, 35, 36, 26, 37, 38, 39]. The control strategy could be separated into the following three functions.

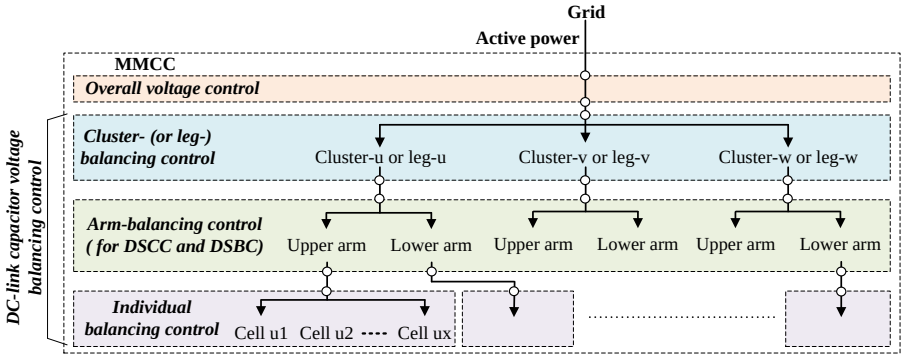


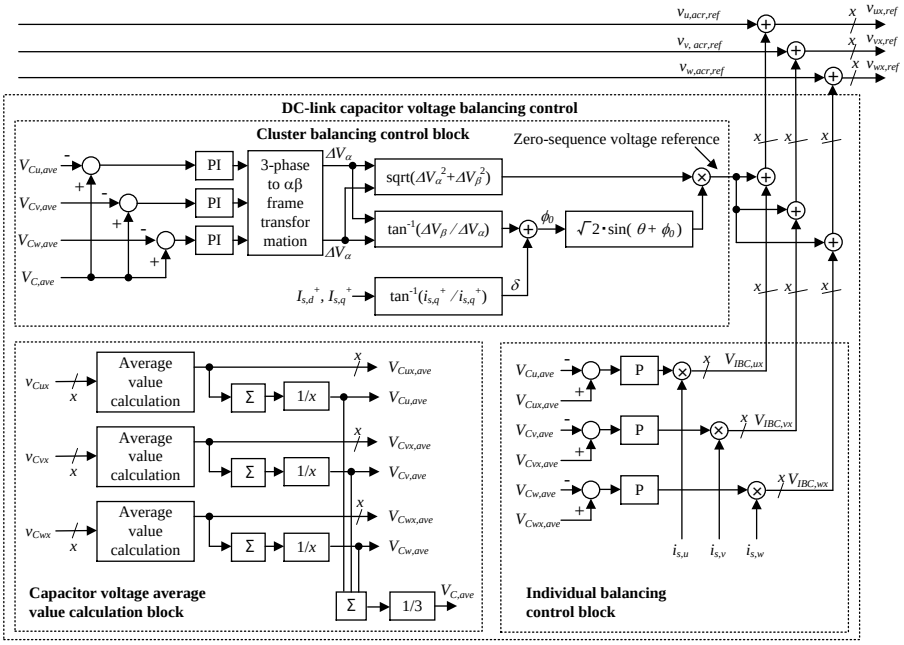
Figure 2-6 Power flow of the dc-link capacitor voltage control for the MMCC solutions.

Cluster- (or leg-) balancing control function: The average values of the dc-link capacitor voltage among clusters or legs are equalized by this function. Especially, when asymmetrical voltage sag by the grid fault happens, the dc-link capacitor voltage between cluster (or leg) becomes principally unbalanced. In order to suppress the voltage unbalance between the phases, zero-sequence AC voltage for SSBC [35, 36], zero-sequence AC current for SDBC [26], circulating DC current for DSCC and DSBC [37, 38, 39] are injected, respectively.

Arm-balancing control function: This function is applied for the DSCC and DSBC, which equalizes the average value of the dc-link voltage in each arm. The third harmonic circulating current injection method is chosen in this thesis, which can perfectly operate both symmetrical and asymmetrical output conditions [39].

Individual balancing control function: The dc-link capacitor voltage difference of each cell converter in a cluster or arm is balanced by this function. This function slightly varies the on-state duration of the IGBT in cell converters in a cluster or arm according to the dc-link voltage differences of the cell converters.

In this thesis, the capacitor voltage control method is selected [36] for SSBC, [26] for SDBC, [39] for DSCC and DSBC, where the control block diagrams are depicted in Figure 2-7, Figure 2-8 and, Figure 2-9, respectively. Special focus is on the Cluster- (or leg-) balancing control function, which function is influent to Asymmetrical Low Voltage Ride Through operation.

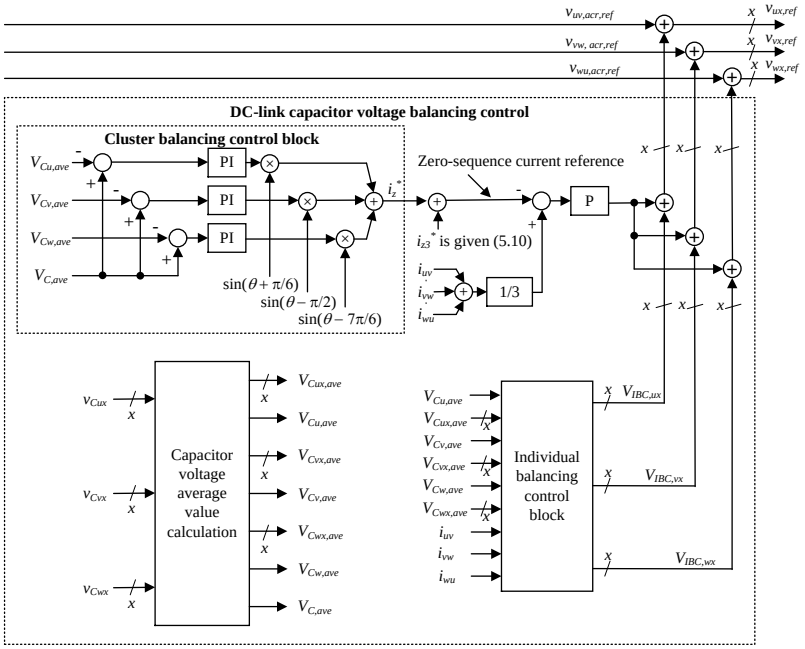


Capacitor voltage average value calculation block: The dc-link capacitor voltage ripple is eliminated in this block. Then, the average values of the dc-link capacitor voltage in each cluster and in all cell capacitors are calculated, respectively.

Cluster balancing control block: The zero-sequence AC voltage reference for cluster balancing control is produced from the voltage difference between the dc-link capacitor averaging voltages in each cluster.

Individual balancing control: In order to balance the dc-link capacitor voltage in each cluster, the superimposed voltage reference for each cell converter is calculated.

Figure 2-7 DC-link capacitor voltage balancing control block for MMCC-SSBC [36].



Capacitor voltage average value calculation block: The dc-link capacitor voltage ripple is eliminated in this block. Then, the average values of the dc-link capacitor voltage in each cluster and in all cell capacitors are calculated, respectively.

Cluster balancing control block: The zero-sequence AC current reference for cluster balancing control is produced from voltage difference between the dc-link capacitor averaging voltages in each cluster.

Individual balancing control: In order to balance the dc-link capacitor voltage in each cluster, the superimposed voltage reference for each cell converter is calculated.

Figure 2-8 DC-link capacitor voltage balancing control block for MMCC-SDBC [26].

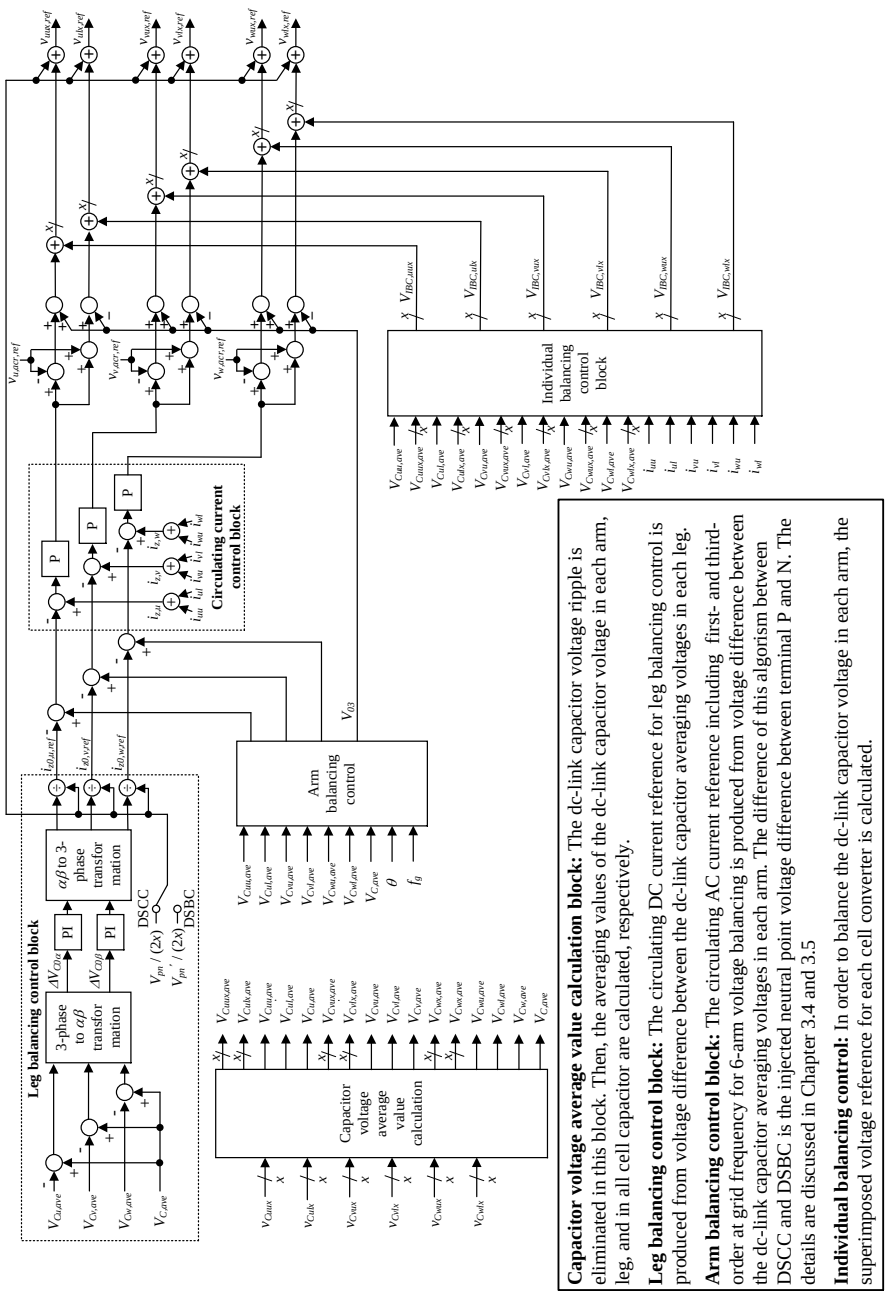


Figure 2-9 DC-link capacitor voltage balancing control block for MMCC-DSCC and DSBC [39].

2.4. THERMAL MODELING FOR THE POWER DEVICES [19]

The electrical losses and junction temperatures on each power semiconductor module are studied by doing thermal simulation function in PLECS. The electrical losses of the power semiconductor modules consist of the conduction loss of the IGBTs, turn on / off loss of the IGBTs, conduction loss of the Diodes, and recovery loss of the Diodes in the power modules. The electrical loss parameters are depending on the flowing currents, applied voltages and junction temperatures which are selected from the datasheets for the power modules. The thermal network between the power semiconductor chip and heatsink for power module are modeled by Foster RC network as shown in Figure 2-10. The thermal parameter, absolute maximum junction temperature $T_{j\text{-}max}$ of each IGBT module and the information of power semiconductor chip used in each power module is summarized in Table 2-5 [40]. It is informed that the $T_{j\text{-}max}$ for the SSBC is higher than other power modules because the generation of power semiconductor chip is newer. In this result, the rated current of the power module is increased 25% while keeping the total power semiconductor chip area. Here, p_S is power loss of the IGBT chip; p_D is power loss of Diode chip; T_{S_j} is junction temperature of IGBT; T_{D_j} is junction temperature of Diode; T_c is the case temperature in the power semiconductor module; T_h is heat sink temperature; $R_S(j\text{-}cn)$, $\tau_D(j\text{-}cn)$, $R_S(j\text{-}cn)$ and $\tau_D(j\text{-}cn)$ are the thermal parameters for the Foster RC network of the power semiconductor module (n:1-4). The heat sink temperature based on liquid cooling system is considered to have a constant value at 60 ˚C in this simulation study as the temperature of the heatsink is normally controlled to be much lower and more stable compared with the junction temperature in a properly designed converter system. Also 60 ˚C is considered to be a worst case for the overall system.

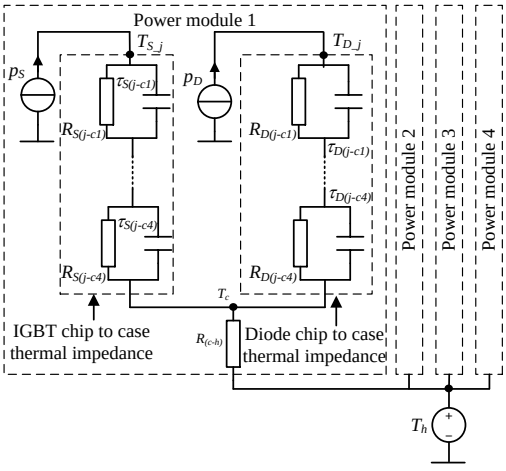


Figure 2-10 Thermal network model between power semiconductor chip and heat sink on each cell converter [19].

Table 2-5 Thermal parameter of each IGBT module (Hitachi) for the MMCC-STATCOM.

	SSBC	SDBC	DSCC	DSBC
Model	MBN1500FH45F (4500V/1500A)	MBN900D45A (4500V/900A)	MBN800H45E2 (4500V/800A)	
Generation	F-version	D-version	E-version	
Technology	Trench IGBT	Planer IGBT	Planer IGBT	
$T_{j\text{-}max}$	150˚C	125˚C	125˚C	
$R_{S(j\text{-}c1)}$ [K/W]	5.59×10^{-3}	5.24×10^{-3}	8.05×10^{-3}	
$R_{S(j\text{-}c2)}$ [K/W]	1.38×10^{-3}	1.61×10^{-3}	2.47×10^{-3}	
$R_{S(j\text{-}c3)}$ [K/W]	1.28×10^{-3}	1.56×10^{-3}	2.39×10^{-3}	
$R_{S(j\text{-}c4)}$ [K/W]	2.45×10^{-4}	8.64×10^{-5}	1.31×10^{-4}	
$R_{D(j\text{-}c1)}$ [K/W]	8.66×10^{-3}	1.05×10^{-2}	1.61×10^{-2}	
$R_{D(j\text{-}c2)}$ [K/W]	7.55×10^{-4}	3.18×10^{-3}	4.91×10^{-3}	
$R_{D(j\text{-}c3)}$ [K/W]	1.84×10^{-3}	3.13×10^{-3}	4.76×10^{-3}	
$R_{D(j\text{-}c4)}$ [K/W]	2.46×10^{-4}	1.71×10^{-4}	2.61×10^{-4}	
$\tau_{S(j\text{-}c1)}$, $\tau_{D(j\text{-}c1)}$ [sec]	1.83×10^{-1}	1.63×10^{-1}	1.63×10^{-1}	
$\tau_{S(j\text{-}c2)}$, $\tau_{D(j\text{-}c2)}$ [sec]	3.34×10^{-2}	2.71×10^{-2}	2.71×10^{-2}	
$\tau_{S(j\text{-}c3)}$, $\tau_{D(j\text{-}c3)}$ [sec]	6.04×10^{-3}	6.12×10^{-3}	6.11×10^{-3}	
$\tau_{S(j\text{-}c4)}$, $\tau_{D(j\text{-}c4)}$ [sec]	1.67×10^{-3}	8.66×10^{-4}	8.61×10^{-4}	

2.5. SUMMARY

This chapter has given the system configuration of a typical offshore wind power plant, its reactive power requirement, specified grid fault scenarios, the output current control scheme, and dc-link capacitor voltage control method of the potentially used four types of MMCCs. Then, specifications and the component sizing of each type of practical 80 MVar / 33 kV scaled MMCC-STATCOM are carefully designed and compared. The equivalent total power semiconductor chip area and the total energy stored in the interconnection inductor, which strongly influence the total cost and total volume of the STATCOM, tunes out to have approximately the same values. However, the total energy stored E_C in the dc-link capacitors for DSCC is 4 times larger than the other MMCCs with SSBC, SDBC and DSBC. It should be noted that the E_C depends greatly on the total volume of the STATCOM. The above specifications and design will be used in the following chapters.

CHAPTER 3. THEORETICAL OPERATION OF MMCC FAMILY UNDER ASYMMETRICAL REACTIVE POWER COMPENSATION [J1]

In this chapter, the mathematical formulation for the STATCOM based on the MMCC solutions under asymmetrical compensation operation is developed. This analysis contributes to the understanding of the limitation of the asymmetrical compensation capability of the MMCC solutions. The asymmetrical three-phase systems are solved by using vector representation as the method seems to be the most elegant to use according to previous works [41, 42, 43].

3.1. DEFINITION OF THE GRID FAULT VOLTAGE AND CURRENT ON BUS C [19]

The grid voltages and currents on *Bus* C as mentioned in Figure 2-1 are defined as

$$\begin{cases} v_{S,u} = V_S^+ \sin(\omega_S t) + V_S^- \sin(\omega_S t + \phi_{vn}) \\ v_{S,v} = V_S^+ \sin\left(\omega_S t - \frac{2\pi}{3}\right) + V_S^- \sin\left(\omega_S t + \phi_{vn} + \frac{2\pi}{3}\right) \\ v_{S,w} = V_S^+ \sin\left(\omega_S t + \frac{2\pi}{3}\right) + V_S^- \sin\left(\omega_S t + \phi_{vn} - \frac{2\pi}{3}\right) \end{cases} \quad (3.1)$$

$$\begin{cases} i_{S,u} = I_S^+ \sin(\omega_S t + \phi_{ip}) + I_S^- \sin(\omega_S t + \phi_{in}) \\ i_{S,v} = I_S^+ \sin(\omega_S t + \phi_{ip} - 2\pi/3) + I_S^- \sin(\omega_S t + \phi_{in} + 2\pi/3) \\ i_{S,w} = I_S^+ \sin(\omega_S t + \phi_{ip} + 2\pi/3) + I_S^- \sin(\omega_S t + \phi_{in} - 2\pi/3) \end{cases} \quad (3.2)$$

where V_S^+ is the amplitude of positive-sequence voltage, V_S^- and ϕ_{vn} are the amplitude and phase angle of negative-sequence voltage, I_S^+ and ϕ_{ip} are the amplitude and phase angle of positive-sequence current, I_S^- and ϕ_{in} are the amplitude and phase angle of negative-sequence current, respectively. After a dq transformation of (3.1) and (3.2), the grid voltage $\dot{V}_{S,dq}^+, \dot{V}_{S,dq}^-$ can be expressed as

$$\begin{cases} \dot{V}_{S,dq}^+ = V_{S,d}^+ + jV_{S,q}^+ \\ \dot{V}_{S,dq}^- = V_{S,d}^- + jV_{S,q}^- \end{cases} \quad (3.3)$$

The $V_{S,d}^+, V_{S,q}^+, V_{S,d}^-$, and $V_{S,q}^-$ are detected by a dual-frame dq transformation scheme in an actual current controller as shown in Figure 2-4. It is noted that the $V_{S,q}^+$ has a zero value because the standard phase is set to be the d-axis of the positive-sequence grid voltage due to the PLL.

Similarly, the grid current $\dot{I}_{S,dq}^{+}, \dot{I}_{S,dq}^{-}$ on *Bus* C can be expressed as

$$\begin{cases} \dot{I}_{S,dq}^{+} = I_{S,d}^{+} + jI_{S,q}^{+} \\ \dot{I}_{S,dq}^{-} = I_{S,d}^{-} + jI_{S,q}^{-} \end{cases} \tag{3.4}$$

The $I_{S,d}^{+}, I_{S,q}^{+}, I_{S,d}^{-}$ and $I_{S,q}^{-}$ are supplied by the STATCOM. These reference values $I_{S,d,ref}^{+}, I_{S,q,ref}^{+}, I_{S,d,ref}^{-}$ and $I_{S,q,ref}^{-}$ can be defined as

$$\begin{cases} I_{S,d}^{+} = I_{S,d,ref}^{+} \equiv 0 \\ I_{S,q}^{+} = I_{S,q,ref}^{+} \\ I_{S,d}^{-} = I_{S,d,ref}^{-} \\ I_{S,q}^{-} = I_{S,q,ref}^{-} \end{cases} \tag{3.5}$$

where $I_{S,d,ref}^{+}$ is set to be zero because of reactive power compensation operation. The $I_{S,q,ref}^{+}$ is given from the central controller of the wind power plant under normal operation. In this result, the STATCOM has two operating modes, which are inductive operation in the case of $I_{S,q,ref}^{+} < 0$ and capacitive operation in the case of $I_{S,q,ref}^{+} > 0$. When a grid fault happens, an additional amount of $I_{S,q,ref}^{+}$ may be required due to a recent published grid code of Transmission System Operators (TSOs) [17]. The $I_{S,d,ref}^{-}$ and $I_{S,q,ref}^{-}$ are set to be zero value according to the mentioned recent grid codes.

3.2. MMCC-SSBC WITH ZERO-SEQUENCE AC VOLTAGE [19]

When the zero-sequence AC voltage with the same frequency as the phase-cluster current is injected, the zero-sequence voltage and the cluster current formulate the different active power between the clusters in the MMCC-SSBC. This phenomenon is used for the dc-link capacitor voltage balancing control between the phase-clusters under asymmetrical grid fault conditions, which value is solved as follows.

Each phase-cluster voltage of the MMCC-SSBC including the Back Electromotive Forces of the interconnection inductor L_{ac} can be expressed as

$$\begin{bmatrix} \dot{V}_{S,un} \\ \dot{V}_{S,vn} \\ \dot{V}_{S,wn} \end{bmatrix} = \begin{bmatrix} \dot{V}_{S,u} \\ \dot{V}_{S,v} \\ \dot{V}_{S,w} \end{bmatrix} + \dot{V}^{0} \tag{3.6}$$

where $\dot{V}_{S,u}, \dot{V}_{S,v}$ and $\dot{V}_{S,w}$ are the grid voltage on *Bus* C, $\dot{V}^{0}$ is the zero-sequence voltage of the MMCC-SSBC, which is the voltage difference between point n and M as shown in Figure 2-2 (a). The $\dot{V}^{0}$ is defined as

$$\dot{V}^{0} = x_{SSBC} + jy_{SSBC} \tag{3.7}$$

where the x_{SSBC} is real part of the $\dot{V}^0$, the y_{SSBC} is imaginary part of the $\dot{V}^0$. The $\dot{V}_{S,u}, \dot{V}_{S,v}$ and $\dot{V}_{S,w}$ can be expressed as

$$\begin{bmatrix} \dot{V}_{S,u} \\ \dot{V}_{S,v} \\ \dot{V}_{S,w} \end{bmatrix} = \begin{bmatrix} \dot{V}^+_{S,dq} + \dot{V}^-_{S,dq} \\ \dot{V}^+_{S,dq} e^{-j2\pi/3} + \dot{V}^-_{S,dq} e^{j2\pi/3} \\ \dot{V}^+_{S,dq} e^{j2\pi/3} + \dot{V}^-_{S,dq} e^{-j2\pi/3} \end{bmatrix}$$

$$= \begin{bmatrix} \left(V^+_{S,d} + V^-_{S,d}\right) + j\left(V^-_{S,q}\right) \\ \left(-\frac{1}{2}V^+_{S,d} - \frac{1}{2}V^-_{S,d} - \frac{\sqrt{3}}{2}V^-_{S,q}\right) + j\left(-\frac{\sqrt{3}}{2}V^+_{S,d} + \frac{\sqrt{3}}{2}V^-_{S,d} - \frac{1}{2}V^-_{S,q}\right) \\ \left(-\frac{1}{2}V^+_{S,d} - \frac{1}{2}V^-_{S,d} + \frac{\sqrt{3}}{2}V^-_{S,q}\right) + j\left(\frac{\sqrt{3}}{2}V^+_{S,d} - \frac{\sqrt{3}}{2}V^-_{S,d} - \frac{1}{2}V^-_{S,q}\right) \end{bmatrix} \tag{3.8}$$

The grid currents $\dot{I}_{S,u}, \dot{I}_{S,v}, \dot{I}_{S,w}$ at *Bus* C can be expressed as

$$\begin{bmatrix} \dot{I}_{S,u} \\ \dot{I}_{S,v} \\ \dot{I}_{S,w} \end{bmatrix} = \begin{bmatrix} \dot{I}^+_{S,dq} + \dot{I}^-_{S,dq} \\ \dot{I}^+_{S,dq} e^{-j2\pi/3} + \dot{I}^-_{S,dq} e^{j2\pi/3} \\ \dot{I}^+_{S,dq} e^{j2\pi/3} + \dot{I}^-_{S,dq} e^{-j2\pi/3} \end{bmatrix}$$

$$= \begin{bmatrix} \left(I^-_{S,d}\right) + j\left(I^+_{S,q} + I^-_{S,q}\right) \\ \left(\frac{\sqrt{3}}{2}I^+_{S,q} - \frac{1}{2}I^-_{S,d} - \frac{\sqrt{3}}{2}I^-_{S,q}\right) + j\left(-\frac{1}{2}I^+_{S,q} + \frac{\sqrt{3}}{2}I^-_{S,d} - \frac{1}{2}I^-_{S,q}\right) \\ \left(-\frac{\sqrt{3}}{2}I^+_{S,q} - \frac{1}{2}I^-_{S,d} + \frac{\sqrt{3}}{2}I^-_{S,q}\right) + j\left(-\frac{1}{2}I^+_{S,q} - \frac{\sqrt{3}}{2}I^-_{S,d} - \frac{1}{2}I^-_{S,q}\right) \end{bmatrix} \tag{3.9}$$

The instantaneous active powers p_u, p_v, p_w of each phase-cluster of the MMCC-SSBC including the L_{ac} can be expressed as

$$\begin{bmatrix} p_u \\ p_v \\ p_w \end{bmatrix} = \begin{bmatrix} \frac{1}{2}\Re\left[\dot{V}^*_{S,un} \cdot \dot{I}_{S,u}\right] \\ \frac{1}{2}\Re\left[\dot{V}^*_{S,vn} \cdot \dot{I}_{S,v}\right] \\ \frac{1}{2}\Re\left[\dot{V}^*_{S,wn} \cdot \dot{I}_{S,w}\right] \end{bmatrix} \tag{3.10}$$

where $\dot{V}^*_{S,un}$ is the complex conjugate of the $\dot{V}_{S,un}$. By using (3.10), the $\dot{V}^0$ in order to make $p_u = p_v = p_w$, can be solved by

$$\dot{V}^0 = \frac{V_{S,d}^+\left(I_{S,d}^- I_{S,d}^- - I_{S,q}^- I_{S,q}^- - I_{S,q}^+ I_{S,q}^-\right) + V_{S,d}^- I_{S,q}^+\left(I_{S,q}^+ + I_{S,q}^-\right) + V_{S,q}^- I_{S,q}^+ I_{S,d}^-}{\left(I_{S,q}^+ I_{S,q}^+ - I_{S,d}^- I_{S,d}^- - I_{S,q}^- I_{S,q}^-\right)}$$

$$+j\frac{V_{S,d}^+\left(I_{S,d}^- I_{S,q}^- + I_{S,d}^- I_{S,q}^- - I_{S,q}^+ I_{S,d}^-\right) + V_{S,q}^- I_{S,q}^+\left(I_{S,q}^- - I_{S,q}^+\right) - V_{S,d}^- I_{S,q}^+ I_{S,d}^-}{\left(I_{S,q}^+ I_{S,q}^+ - I_{S,d}^- I_{S,d}^- - I_{S,q}^- I_{S,q}^-\right)} \tag{3.11}$$

Each phase-cluster converter output voltage $\dot{V}_{un}$, $\dot{V}_{vn}$, $\dot{V}_{wn}$ can be expressed as

$$\begin{bmatrix}\dot{V}_{un}\\ \dot{V}_{vn}\\ \dot{V}_{wn}\end{bmatrix} = \begin{bmatrix}\dot{V}_{S,un}\\ \dot{V}_{S,vn}\\ \dot{V}_{S,wn}\end{bmatrix} - \begin{bmatrix}\dot{V}_{L,u}\\ \dot{V}_{L,v}\\ \dot{V}_{L,w}\end{bmatrix} \tag{3.12}$$

where $\dot{V}_{L,u}, \dot{V}_{L,v}\ and\ \dot{V}_{L,w}$ are the Back Electromotive Forces of the L_{ac}. The $\dot{V}_{L,u}, \dot{V}_{L,v}$ and $\dot{V}_{L,w}$ can be expressed as

$$\begin{bmatrix}\dot{V}_{L,u}\\ \dot{V}_{L,v}\\ \dot{V}_{L,w}\end{bmatrix} = j\omega_S L_{ac}\begin{bmatrix}\dot{I}_{S,u}\\ \dot{I}_{S,v}\\ \dot{I}_{S,w}\end{bmatrix}$$

$$= -\omega_S L_{ac}\begin{bmatrix} I_{S,q}^+ + I_{S,q}^- - jI_{S,d}^- \\ \left(-\frac{1}{2}I_{S,q}^+ + \frac{\sqrt{3}}{2}I_{S,d}^- - \frac{1}{2}I_{S,q}^-\right) + j\left(-\frac{\sqrt{3}}{2}I_{S,q}^+ + \frac{1}{2}I_{S,d}^- + \frac{\sqrt{3}}{2}I_{S,q}^-\right) \\ \left(-\frac{1}{2}I_{S,q}^+ - \frac{\sqrt{3}}{2}I_{S,d}^- - \frac{1}{2}I_{S,q}^-\right) + j\left(\frac{\sqrt{3}}{2}I_{S,q}^+ + \frac{1}{2}I_{S,d}^- - \frac{\sqrt{3}}{2}I_{S,q}^-\right)\end{bmatrix} \tag{3.13}$$

where the resistance of L_{ac} is neglected because the resistance is much smaller than the total impedance given by the inductance. Then the maximum phase-cluster peak voltage V_{max_pu} between the three-phases normalized by the rated peak phase grid voltage $\sqrt{2/3}V_S$ can be expressed as

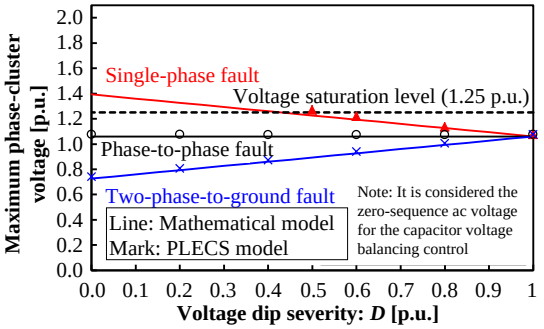
$$V_{max\_pu} = \frac{max(|\dot{V}_{un}|,|\dot{V}_{vn}|,|\dot{V}_{wn}|)}{\sqrt{\frac{2}{3}}V_s} \tag{3.14}$$

The maximum phase-cluster r.m.s current I_{max_pu} between the three phases is normalized by the rated phase current $\sqrt{2}I_r$ of the STATCOM can be expressed as

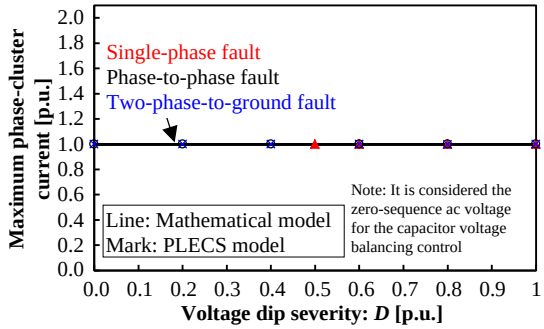
$$I_{max\_pu} = \frac{max(|i_u|,|i_v|,|i_w|)}{\sqrt{2}I_r} \tag{3.15}$$

Figure 3-1 shows with line graphs calculated result of the normalized maximum phase-cluster peak voltage and r.m.s current of the MMCC-SSBC under different types of grid fault scenarios as a function of the voltage dip severity *D* by using (3.14) and (3.15). The I_q^+ is set to be the rated phase current value as $\sqrt{2}I_r$. The grid voltage is given by the mentioned Table 2-2. The normalized inductance of the L_{ac} is

set to be 6% with reference to the model mentioned in Table 2-3. In the case of a single-phase fault, the maximum-phase-cluster peak voltage reaches the voltage saturated level of the designed STATCOM when D = 0.45. On the other hand, the maximum-phase-cluster r.m.s. current does not increase as a function of grid fault conditions. The marks in Figure 3-1 shows the simulation results by using PLECS software, which conditions are given in Chapter 4.1. The calculated values correspond reasonably well with the PLECS simulations based on the given STATCOM configuration.



(a) Maximum-phase-cluster peak voltage



(b) Maximum-phase-cluster r.m.s. current

Figure 3-1 Maximum-phase-cluster output of the MMCC-SSBC corresponding to various grid fault scenarios [19].

3.3. MMCC-SDBC WITH ZERO-SEQUENCE AC CURRENT [19]

When the zero-sequence AC current with the same frequency as the cluster output voltage is injected, the zero-sequence current and the cluster output voltage will formulate different active powers between the clusters in the MMCC-SDBC. This phenomenon is used for the dc-link capacitor voltage balancing control among the phase-clusters under asymmetrical grid fault conditions, which values are solved as follows.

For the configuration of MMCC-SDBC, the phase-cluster current $\dot{I}_{uv}, \dot{I}_{vw}, \dot{I}_{wu}$ can be expressed as

$$\begin{bmatrix} \dot{I}_{uv} \\ \dot{I}_{vw} \\ \dot{I}_{wu} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} \dot{I}^{+}_{S,dq} e^{j\pi/6} + \dot{I}^{-}_{S,dq} e^{-j\pi/6} \\ \dot{I}^{+}_{S,dq} e^{-j\pi/2} + \dot{I}^{-}_{S,dq} e^{j\pi/2} \\ \dot{I}^{+}_{S,dq} e^{j5\pi/6} + \dot{I}^{-}_{S,dq} e^{-j5\pi/6} \end{bmatrix} + \dot{I}^{0}$$

$$= \begin{bmatrix} \left(x_{SDBC} - \frac{I^{+}_{S,q}}{2\sqrt{3}} + \frac{I^{-}_{S,q}}{2\sqrt{3}} + \frac{I^{-}_{S,d}}{2} \right) + j \left(y_{SDBC} + \frac{I^{+}_{S,q}}{2} + \frac{I^{-}_{S,q}}{2} - \frac{I^{-}_{S,d}}{2\sqrt{3}} \right) \\ \left(x_{SDBC} + \frac{\sqrt{3} I^{+}_{S,q}}{3} - \frac{I^{-}_{S,q}}{3} \right) + j \left(y_{SDBC} + \frac{\sqrt{3} I^{-}_{S,d}}{3} \right) \\ \left(x_{SDBC} - \frac{I^{+}_{S,q}}{2\sqrt{3}} + \frac{I^{-}_{S,q}}{2\sqrt{3}} - \frac{I^{-}_{S,d}}{2} \right) + j \left(y_{SDBC} - \frac{I^{+}_{S,q}}{2} - \frac{I^{-}_{S,q}}{2} - \frac{I^{-}_{S,d}}{2\sqrt{3}} \right) \end{bmatrix} \quad (3.16)$$

where $\dot{I}^{0}$ is the zero-sequence current circulating in the MMCC-SDBC. The $\dot{I}^{0}$ can be expressed as

$$\dot{I}^{0} = x_{SDBC} + j y_{SDBC} \quad (3.17)$$

where x_{SDBC} is real part of the $\dot{I}^{0}$, the y_{SDBC} is imaginary part of the $\dot{I}^{0}$. Each line-to-line voltage $\dot{V}_{S,uv}, \dot{V}_{S,vw}, \dot{V}_{S,wu}$ of the MMCC-SDBC including the Back Electromotive Forces of the L_{ac} can be expressed as

$$\begin{bmatrix} \dot{V}_{S,uv} \\ \dot{V}_{S,vw} \\ \dot{V}_{S,wu} \end{bmatrix} = \sqrt{3} \begin{bmatrix} \dot{V}^{+}_{S,dq} e^{j\pi/6} + \dot{V}^{-}_{S,dq} e^{-j\pi/6} \\ \dot{V}^{+}_{S,dq} e^{-j\pi/2} + \dot{V}^{-}_{S,dq} e^{j\pi/2} \\ \dot{V}^{+}_{S,dq} e^{j5\pi/6} + \dot{V}^{-}_{S,dq} e^{-j5\pi/6} \end{bmatrix}$$

$$= \begin{bmatrix} \frac{\sqrt{3}}{2} \left\{ \left(\sqrt{3} V^{+}_{S,d} + \sqrt{3} V^{-}_{S,d} + \sqrt{3} V^{-}_{S,q} \right) + j \left(V^{+}_{S,d} - V^{-}_{S,d} + \sqrt{3} V^{-}_{S,q} \right) \right\} \\ \sqrt{3} \left\{ -V^{-}_{S,q} + j \left(-V^{+}_{S,d} + V^{-}_{S,d} \right) \right\} \\ \frac{\sqrt{3}}{2} \left\{ \left(V^{-}_{S,q} - \sqrt{3} V^{+}_{S,d} - \sqrt{3} V^{-}_{S,d} \right) + j \left(V^{+}_{S,d} - V^{-}_{S,d} - \sqrt{3} V^{-}_{S,q} \right) \right\} \end{bmatrix} \quad (3.18)$$

The zero-sequence current circulating in the MMCC-SDBC $\dot{I}^0$ in order to make the instantaneous active powers between the phase-clusters to have the same value can be expressed as follows [23]:

$$\dot{I}^0 = \frac{I_{S,q}^+\left(V_{S,d}^-V_{S,d}^- - V_{S,d}^-V_{S,d}^+ - V_{S,q}^-V_{S,q}^-\right) + I_{S,q}^-V_{S,d}^+\left(V_{S,d}^+ - V_{S,d}^-\right) - I_{S,d}^-V_{S,d}^+V_{S,q}^-}{\sqrt{3}\left(V_{S,d}^-V_{S,d}^- - V_{S,d}^+V_{S,d}^+ + V_{S,q}^-V_{S,q}^-\right)} + j\frac{I_{S,q}^+\left(V_{S,d}^-V_{S,q}^- + V_{S,d}^-V_{S,q}^- + V_{S,d}^+V_{S,q}^-\right) + I_{S,d}^-V_{S,d}^+\left(V_{S,d}^+ + V_{S,d}^-\right) - I_{S,q}^-V_{S,d}^+V_{S,q}^-}{\sqrt{3}\left(V_{S,d}^-V_{S,d}^- - V_{S,d}^+V_{S,d}^+ + V_{S,q}^-V_{S,q}^-\right)} \tag{3.19}$$

Each phase-cluster converter output voltage $\dot{V}_{uv}$, $\dot{V}_{vw}$, $\dot{V}_{wu}$ of the MMCC-SDBC can be expressed as

$$\begin{bmatrix}\dot{V}_{uv}\\ \dot{V}_{vw}\\ \dot{V}_{wu}\end{bmatrix} = \begin{bmatrix}\dot{V}_{S,uv}\\ \dot{V}_{S,vw}\\ \dot{V}_{S,wu}\end{bmatrix} - \begin{bmatrix}\dot{V}_{L,uv}\\ \dot{V}_{L,vw}\\ \dot{V}_{L,wu}\end{bmatrix} \tag{3.20}$$

where $\dot{V}_{L,uv}, \dot{V}_{L,vw}$ and $\dot{V}_{L,wu}$ are the Back Electromotive Forces of the L_{ac}. The $\dot{V}_{L,uv}, \dot{V}_{L,vw}$ and $\dot{V}_{L,wu}$ can be expressed as

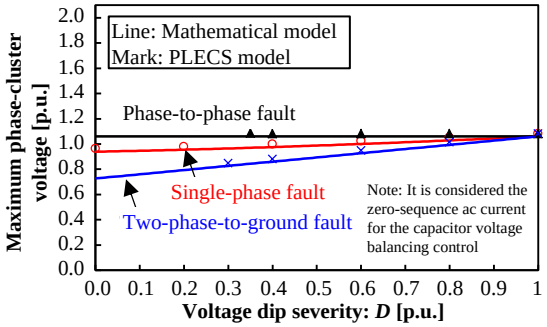
$$\begin{bmatrix}\dot{V}_{L,uv}\\ \dot{V}_{L,vw}\\ \dot{V}_{L,wu}\end{bmatrix} = j\omega_S L_{ac}\begin{bmatrix}\dot{I}_{S,uv}\\ \dot{I}_{S,vw}\\ \dot{I}_{S,wu}\end{bmatrix}$$

$$= -\omega_S L_{ac}\begin{bmatrix}\left(y_{SDBC} + \frac{I_{S,q}^+}{2} + \frac{I_{S,q}^-}{2} - \frac{I_{S,d}^-}{2\sqrt{3}}\right) + j\left(-x_{SDBC} + \frac{I_{S,q}^+}{2\sqrt{3}} - \frac{I_{S,q}^-}{2\sqrt{3}} - \frac{I_{S,d}^-}{2}\right)\\ \left(y_{SDBC} + \frac{\sqrt{3}I_{S,d}^-}{3}\right) + j\left(-x_{SDBC} - \frac{\sqrt{3}I_{S,q}^+}{3} + \frac{I_{S,q}^-}{3}\right)\\ \left(y_{SDBC} - \frac{I_{S,q}^+}{2} - \frac{I_{S,q}^-}{2} - \frac{I_{S,d}^-}{2\sqrt{3}}\right) + j\left(-x_{SDBC} + \frac{I_{S,q}^+}{2\sqrt{3}} - \frac{I_{S,q}^-}{2\sqrt{3}} + \frac{I_{S,d}^-}{2}\right)\end{bmatrix} \tag{3.21}$$

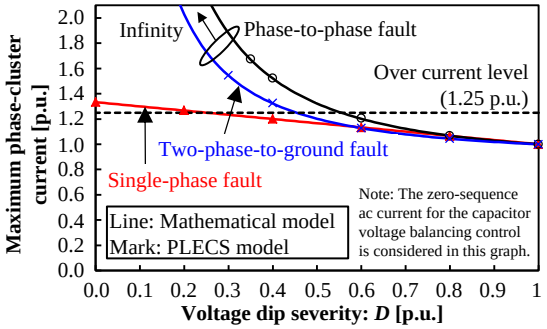
where the resistance of L_{ac} is neglected. The maximum-phase-cluster peak voltage and r.m.s. current of the MMCC-SDBC can be calculated in the same way as the MMCC-SSBC

Figure 3-2 shows with line graphs the normalized maximum-phase-cluster peak voltage and r.m.s. current of the MMCC-SDBC under different types of grid fault scenarios in respect to the voltage dip severity D. The I_q^+ is set to be the rated phase current value as $\sqrt{2}I_r$. The grid voltage is given in Table 2-2. The normalized inductance of L_{ac} is set to be 6% with reference to the model mentioned in Table 2-3. It is noted that the maximum-phase-cluster peak voltage does not increase at different grid fault conditions. The maximum-phase-cluster r.m.s. current increases rapidly when $D < 0.5$ under the phase-to-phase short-circuit fault and two-phase-to-

ground fault, and reach the over current level (1.25) decided by the maximum junction temperature of the IGBT model, which will be discussed in more detail in the next chapter. When *D* approaches 0 under these faults, the current approaches to infinity value while the denominator of the (3.19) is close to zero. When *D* is zero under these fault voltages, there is no solution to the zero-sequence current, and it is claimed to be the major problem of the MMCC-SDBC for the STATCOM application [34], [43]. The marks in Figure 3-2 indicate the simulation results using the PLECS software and the conditions are given in the Chapter 4.1. The calculated values correspond reasonably well with the PLECS simulation results based on the practical scaled STATCOM model.



(a) Maximum phase-cluster peak voltage



(b) Maximum phase-cluster r.m.s. current

Figure 3-2 The Maximum-phase-cluster output of the MMCC-SDBC corresponding to various grid fault scenarios [19].

3.4. MMCC-DSCC WITH CIRCULATING DC CURRENT [19]

The DSCC has two neutral points P and N in each single star connection as shown in Figure 2-2 (c). The differential voltage V_{PN} between P and N is normally 50 % of the rated dc-link voltage of each converter cell in the DSCC in order to output the AC voltage using the chopper converter cells. When the circulating dc current is injected in each leg of the DSCC, the circulating current and the V_{PN} formulate the independent active power between the legs in the MMCC-DSCC. This phenomenon is used for the dc-link capacitor voltage balancing control among the legs under asymmetrical grid fault conditions, which value is solved in the following.

The instantaneous active power in the αβ0 frame $p_{S,\alpha}$, $p_{S,\beta}$, $p_{S,0}$ of the MMCC-DSCC arising by asymmetrical reactive power supply can be expressed as

$$\begin{bmatrix} p_{S,\alpha} \\ p_{S,\beta} \\ p_{S,0} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}\begin{bmatrix} \frac{1}{2}\Re\left[\dot{V}_{S,u}^{*} \cdot \dot{I}_{S,u}\right] \\ \frac{1}{2}\Re\left[\dot{V}_{S,v}^{*} \cdot \dot{I}_{S,v}\right] \\ \frac{1}{2}\Re\left[\dot{V}_{S,w}^{*} \cdot \dot{I}_{S,w}\right] \end{bmatrix} \tag{3.22}$$

where $\dot{V}_{S,u}, \dot{V}_{S,v}$ and $\dot{V}_{S,w}$, are the same as, the $\dot{I}_{S,u}$, $\dot{I}_{S,v}$ and $\dot{I}_{S,w}$ are the same as (3.9). It is noted that the $p_{S,\alpha}$ and $p_{S,\beta}$ are the instantaneous active power imbalances among the phases. The $p_{S,0}$ shows the instantaneous active power of the three-phase MMCC-DSCC. Normally, each converter cell of the MMCC-DSCC has injected a dc-bias voltage with 50% of modulation factor in order to output AC (+/-) voltage using chopper cells where the dc-bias voltage appears to be the differential voltage V_{PN} between the P and N terminal. The V_{PN} can be expressed as

$$V_{PN} = 2\sqrt{\frac{2}{3}}V_s\alpha_{mgn} \tag{3.23}$$

where α_{mgn} is the ratio between the maximum converter output voltage and rated grid voltage and it is used as design margin. The circulating currents of each of the leg $i_{z,u}$, $i_{z,v}$, $i_{z,w}$ can be expressed as

$$\begin{bmatrix} i_{z,u} \\ i_{z,v} \\ i_{z,w} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} i_{uu} + i_{ul} \\ i_{vu} + i_{vl} \\ i_{wu} + i_{wl} \end{bmatrix} \tag{3.24}$$

Based on (3.22) and (3.23), the circulating currents to cancel out the instantaneous active power imbalance among the phases arises due to the asymmetrical reactive power output operation that can be expressed as

$$\begin{bmatrix} i_{z,u} \\ i_{z,v} \\ i_{z,w} \end{bmatrix} = \frac{1}{V_{PN}}\begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} P_{S,\alpha} \\ P_{S,\beta} \end{bmatrix} \tag{3.25}$$

The AC component of each arm output voltages $\dot{V}_{PU,ac}$, $\dot{V}_{PV,ac}$, $\dot{V}_{PW,ac}$, $\dot{V}_{NU,ac}$, $\dot{V}_{NV,ac}$ and $\dot{V}_{NW.ac}$ can be expressed as

$$\begin{bmatrix} \dot{V}_{PU,ac} \\ \dot{V}_{PV,ac} \\ \dot{V}_{PW,ac} \\ \dot{V}_{UN,ac} \\ \dot{V}_{VN,ac} \\ \dot{V}_{WN,ac} \end{bmatrix} = \begin{bmatrix} -\dot{V}_{S,u} \\ -\dot{V}_{S,v} \\ -\dot{V}_{S,w} \\ \dot{V}_{S,u} \\ \dot{V}_{S,v} \\ \dot{V}_{S,w} \end{bmatrix} - \begin{bmatrix} \dot{V}_{L,uu} \\ \dot{V}_{L,vu} \\ \dot{V}_{L,wu} \\ \dot{V}_{L,ul} \\ \dot{V}_{L,vl} \\ \dot{V}_{L,wl} \end{bmatrix} \tag{3.26}$$

where $\dot{V}_{L,uu}, \dot{V}_{L,vu}, \dot{V}_{L,wu}, \dot{V}_{L,ul}, \dot{V}_{L,vl}$ and $\dot{V}_{L,wl}$ are the Back Electromotive Forces of the L_{ac}. The $\dot{V}_{L,uu}$, $\dot{V}_{L,vu}$, $\dot{V}_{L,wu}$, , $\dot{V}_{L,ul}$, $\dot{V}_{L,vl}$ and $\dot{V}_{L,wl}$ can be expressed as

$$\begin{bmatrix} \dot{V}_{L,ul} \\ \dot{V}_{L,vl} \\ \dot{V}_{L,wl} \end{bmatrix} = -\begin{bmatrix} \dot{V}_{L,uu} \\ \dot{V}_{L,vu} \\ \dot{V}_{L,wu} \end{bmatrix} = j\frac{\omega_S L_{ac}}{2}\begin{bmatrix} \dot{I}_{S,u} \\ \dot{I}_{S,v} \\ \dot{I}_{S,w} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} \dot{V}_{L,u} \\ \dot{V}_{L,v} \\ \dot{V}_{L,w} \end{bmatrix} \tag{3.27}$$

where the resistance of the L_{ac} is neglected. The $\dot{V}_{L,u}, \dot{V}_{L,v}$ and $\dot{V}_{L,w}$ were given in (3.13). The maximum arm output peak voltage V_{max_pu} between the arm-converters normalized by the rated grid voltage $\sqrt{2/3}V_S$ can be expressed as

$$V_{max\_pu} = \frac{V_{PN} + max\left(\left|\dot{V}_{PU,ac}\right|, \left|\dot{V}_{PV,ac}\right|, \left|\dot{V}_{PW,ac}\right|, \left|\dot{V}_{UN,ac}\right|, \left|\dot{V}_{VN,ac}\right|, \left|\dot{V}_{WN,ac}\right|\right)}{\sqrt{\frac{2}{3}}V_s} \tag{3.28}$$

Each arm output r.m.s. current $i_{uu,rms}$, $i_{vu,rms}$, $i_{wu,rms}$, $i_{ul,rms}$, $i_{vl,rms}$ and $i_{wl,rms}$ can be expressed as

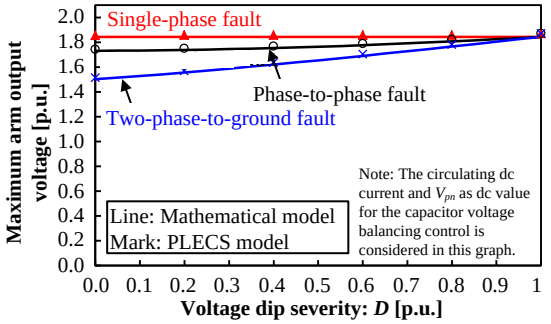
$$\begin{bmatrix} i_{uu,rms} \\ i_{vu,rms} \\ i_{wu,rms} \end{bmatrix} = \begin{bmatrix} i_{ul,rms} \\ i_{vl,rms} \\ i_{wl,rms} \end{bmatrix} = \begin{bmatrix} \sqrt{\left(\frac{\left|\dot{I}_{S,u}\right|}{\sqrt{2}}\right)^2 + \left(\frac{i_{z,u}}{2}\right)^2} \\ \sqrt{\left(\frac{\left|\dot{I}_{S,v}\right|}{\sqrt{2}}\right)^2 + \left(\frac{i_{z,v}}{2}\right)^2} \\ \sqrt{\left(\frac{\left|\dot{I}_{S,w}\right|}{\sqrt{2}}\right)^2 + \left(\frac{i_{z,w}}{2}\right)^2} \end{bmatrix} \tag{3.29}$$

The maximum arm output r.m.s current I_{max_pu} normalized by the rated arm current $1/2I_r$ of the STATCOM can be expressed as

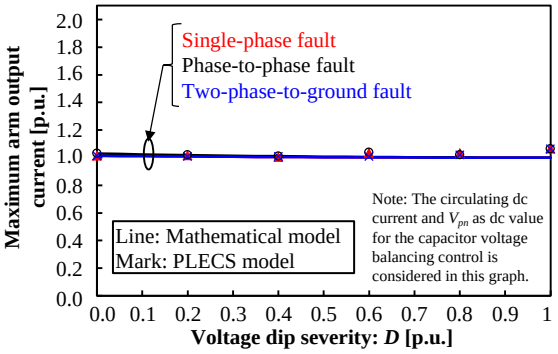
$$I_{max\_pu} = \frac{max\left(i_{uu,rms}, i_{vu,rms}, i_{wu,rms}\right)}{I_r/2} \tag{3.30}$$

Figure 3-3 shows with line graphs the calculated result of the normalized maximum arm output peak voltage and r.m.s. current of the MMCC-DSCC under different types of grid fault scenarios regarding the voltage dip severity D by using (3.28) and (3.30). The I_q^+ is set to be the rated phase current value as $\sqrt{2}I_r$. The grid voltage is given by the mentioned Table 2-2. The normalized inductance of L_{ac} is set to be 6%,

the α_{mgn} is set to be 1.127 with reference to the practical scale model as mentioned Table 2-3. It is noted that the maximum arm output peak voltage and r.m.s current do not increase significantly under different grid fault conditions. The marks in Figure 3-3 plot the simulation result using the PLECS software, where the simulation conditions are given in Chapter 4.1. The calculated values correspond reasonably well with the PLECS simulation values based on the practical scaled STATCOM model.



(a) Maximum arm output peak voltage



(b) Maximum arm output r.m.s. current

Figure 3-3 Maximum arm output of the MMCC-DSCC corresponding to various grid fault scenario [19].

3.5. MMCC-DSBC WITH CIRCULATING DC CURRENT [19]

The operation principle of the MMCC-DSBC is almost the same as the MMCC-DSCC. The only difference is the amplitude of the V_{PN}. In the case of the MMCC-DSBC, each of the arms is able to supply AC (+/-) voltage without the V_{PN} because of the used H-Bridge converter cells. However, due to the voltage balancing control, the V'_{PN} is required, which can be expressed as

$$V'_{PN} = \alpha_{DSBC} V_{PN} \tag{3.31}$$

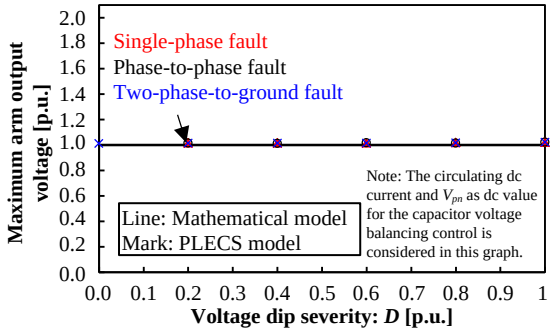
where α_{DSBC} is the amplitude ratio of the differential voltage between terminal P and N of the DSCC to the DSBC. The injectable α_{DSBC} is normally less than 20% in order to avoid the voltage saturation when the DSBC is designed practically. The maximum value of the α_{DSBC} considering the grid fault condition can be expressed as

$$\alpha_{DSBC} = \frac{\sqrt{\frac{2}{3}} V_s \alpha_{mgn} - \max\left(|\dot{V}_{PU,ac}|, |\dot{V}_{PV,ac}|, |\dot{V}_{PW,ac}|, |\dot{V}_{UN,ac}|, |\dot{V}_{VN,ac}|, |\dot{V}_{WN,ac}|\right)}{\sqrt{\frac{2}{3}} V_s \alpha_{mgn}} \tag{3.32}$$

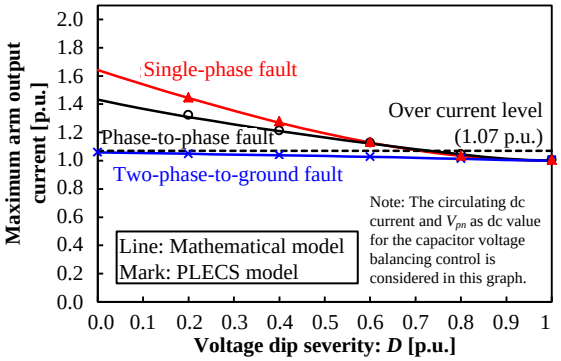
where $\dot{V}_{PU,ac}, \dot{V}_{PV,ac}, \dot{V}_{PW,ac}, \dot{V}_{UN,ac}, \dot{V}_{VN,ac}$ and $\dot{V}_{WN,ac}$ were mentioned in (3.26). It is noted that the circulating dc current of the DSBC becomes larger than the DSCC because the $V_{PN}{}'$ for the DSBC becomes smaller than the DSCC. The maximum arm output voltage and current can be solved in the same way as the MMCC-DSCC.

Figure 3-4 with line graphs show the calculated result of the normalized maximum arm output peak voltage and r.m.s. current of the MMCC-DSBC under the different types of grid fault scenarios in respect to the voltage dip severity *D*. The I_q^+ is set to be the rated phase current value as $\sqrt{2}I_r$. The grid voltage is given in Table 2-2. The normalized inductance of L_{ac} is set to 6%, the α_{mgn} is set to be 1.127 with reference to the practical scaled model given in Table 2-3. The marks are the practical scaled simulation results, which test conditions will be shown in the next chapter. It is noted that the maximum arm peak voltage tracks 1 p.u. by the injected V'_{PN} as being the designed maximum value. The maximum arm r.m.s. current increases moderate in respect to *D*, but reaches the over current level (1.07), which is decided by the over junction temperature of the IGBT module, which is discussed in next chapter. The arm current becomes larger than the DSCC because of a lower V'_{PN}. The over current level becomes lower than the SDBC because the current distribution between the IGBT modules in a converter cell increases by the injected dc voltage and current for the capacitor voltage balancing method. The marks in Figure 3-4 show the simulation results using PLECS software, which conditions are given in

Chapter 4.1 next chapter. The calculated values correspond reasonably well with the PLECS simulation results based on a practical scale STATCOM model.



(a) Maximum arm output peak voltage



(b) Maximum arm output r.m.s. current

Figure 3-4 Maximum arm output of the MMCC-DSBC corresponding to various grid fault scenario [19].

3.6. SUMMARY

In this chapter, the asymmetrical three-phase systems for the MMCC-based STATCOMs are analyzed and solved based on vector representation. Because of different cluster- (or leg-) balancing control principles, the performance limitation and circuit behavior between the MMCC solutions are different under asymmetrical compensation. The SSBC with a zero-sequence voltage injection method shows a voltage stress increase when the voltage dip severity is serious. The SDBC, DSCC, and DSBC with zero-sequence current or circulating current injection increase the current with different levels under asymmetrical grid fault conditions. It is noted that the current of the DSCC increases by only a few % with the most serious grid fault condition. In the case of the SDBC, when the voltage dip severity approaches the most serious condition, the current will approach to an infinity value. In the case of DSBC, the current amplitude increases by maximum 60% under the most serious grid fault condition. These results show the possibility to compromise the reactive power compensation capability with different degrees in fault ride through mode.

CHAPTER 4. PERFORMANCE BENCHMARK OF THE MMCC SOLUTIONS [J1]

In this chapter, the electro-thermal stresses of the actual power modules used in each type of the MMCC with practical controls are analyzed in detail. The asymmetrical reactive power capacity focusing on the MMCC solutions is compared under different scenarios of grid faults, with the consideration of device temperature limits and voltage saturation. The most attractive MMCC solution for the STATCOM application is suggested based on the obtained results.

4.1. ELECTRICAL AND THERMAL SIMULATION MODELING [19]

The LVRT capability of a STATCOM, which is based on the MMCC with SSBC, SDBC, DSCC and DSBC is simulated by using the software PLECS. Three types of grid fault voltages are studied in Chapter 2.1, then the voltage vector as shown in Table 2-2 is applied directly on *Bus* C in Figure 2-1. The specifications of the MMCC with SSBC, SDBC, DSCC and DSBC are assembled based on the parameters given in Table 2-3. The reactive current reference is set to rated 1 p.u. of the positive-sequence as the recent grid codes do not require negative sequence current to compensate for the asymmetrical grid voltage. The control scheme of each type of MMCC has been described in Chapter 2.3. The thermal model for the power devices have been discussed in Chapter 2.4.

4.2. ELECTRICAL AND THERMAL SIMULATIONS OF THE MMCC-SSBC [19]

Figure 4-1 shows the key waveforms of the MMCC-SSBC under single-phase-to-ground fault with a dip severity *D* of 0.5 p.u.. It can be seen that the peak value of the voltage reference increases by maximum 22% maximum on the w-phase cluster under the single-phase-to-ground fault in order to able inject zero-sequence voltage to balance the DC-link capacitor voltages of the converter cells. Here, the zero-sequence voltage reference v^*_{zero} of each cell converter is equivalent to (4.1) when all capacitor voltages are balanced, where v^*_{u1}, v^*_{u1}, and v^*_{u1} are the cell converter output voltage reference of u1, v1, and w1 cell, respectively.

$$v^*_{zero} = \frac{v^*_{u1} + v^*_{v1} + v^*_{w1}}{3} \tag{4.1}$$

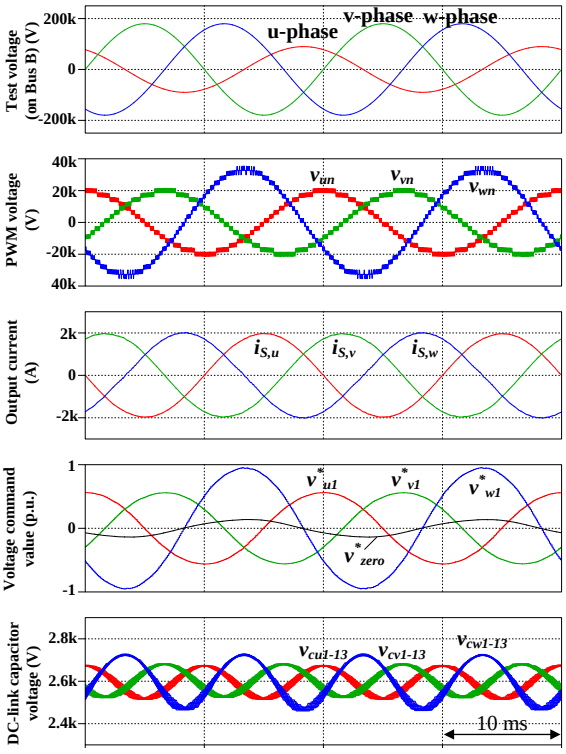
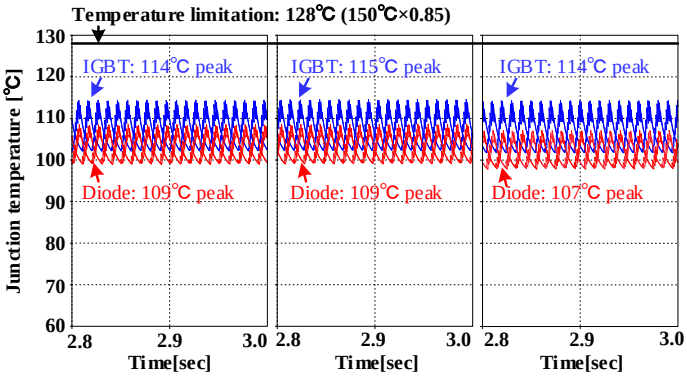


Figure 4-1 Key waveforms of the MMCC-SSBC under single-phase fault with a dip severity *D* of 0.5 p.u [19].

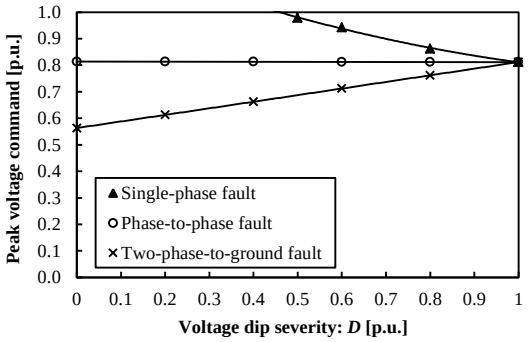
Figure 4-2 shows the junction temperatures of four IGBTs and diodes in each cell of u1, v1, and w1 under the same simulation conditions. The peak junction temperature of the IGBT and Diode are the same, 115˚C and 109˚C respectively among the different cluster cells. The temperatures are below the limit of 128 ˚C when considering a 15 % margin for the IGBT modules where the absolute maximum rating of the junction temperature is defined by the manufacturers (see Table 2-5).



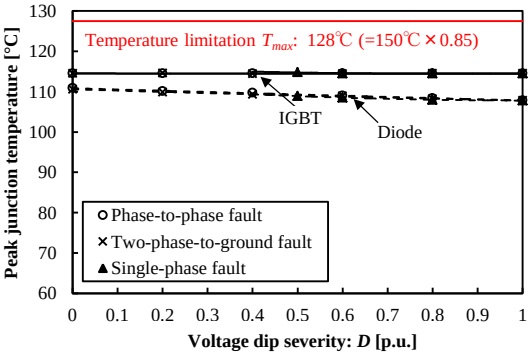
(a) u1-cell (b) v1-cell (c) w1-cell

Figure 4-2 Thermal distribution of the MMCC-SSBC under single-phase fault with dip severity *D* of 0.5 p.u. [19]

Figure 4-3 shows the maximum peak voltage command and the peak junction temperature of the IGBT and Diode among the cells in respect to the dip severity D under various grid fault scenarios. It can be seen that the peak voltage command saturates with a single-phase-to-ground fault at D = 0.5 p.u.. The maximum peak junction temperature of the IGBT and Diode are approximately 115 °C and 109 °C, respectively, regardless of the grid conditions.



(a) Peak voltage command



(b) Peak junction temperature

Figure 4-3 Electrical-thermal simulations of the MMCC-SSBC at different dip severities [19].

4.3. ELECTRICAL AND THERMAL SIMULATIONS OF THE MMCC-SDBC [19]

Figure 4-4 shows the simulated key waveforms of the MMCC-SDBC under phase-to-phase fault with a dip severity D = 0.4 p.u. as an example. It can be noted that the peak value of the cluster current increases by maximum 52% at the v and w cluster under the phase-to-phase fault in order to inject zero-sequence current i_{zero} to balance the DC-link capacitor voltages of the converter cells. Here, the injected zero-sequence current is equivalent to (4.2).

$$i_{zero} = \frac{i_{uv} + i_{vw} + i_{wu}}{3} \tag{4.2}$$

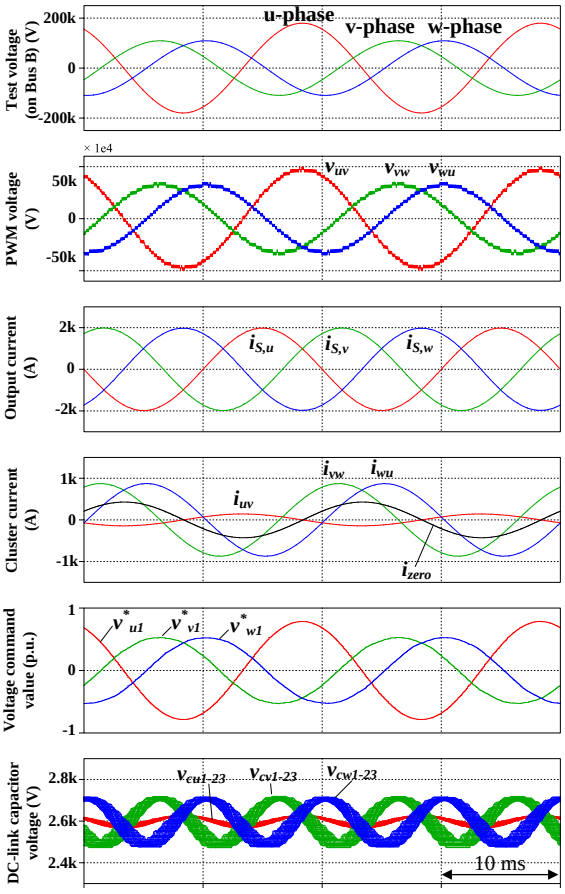
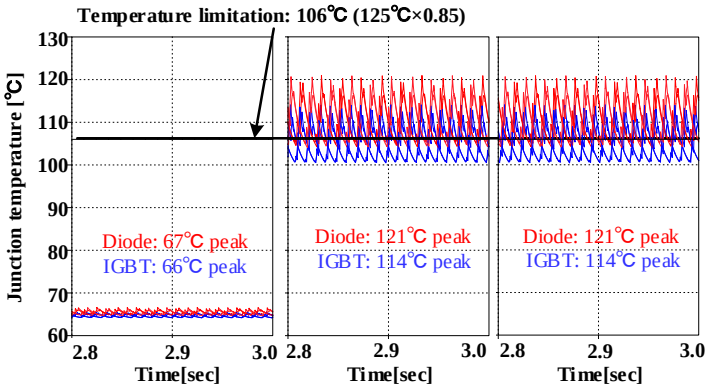


Figure 4-4 Key waveforms of the MMCC-SDBC under phase-to-phase fault with a dip severity D of 0.4 p.u. [19]

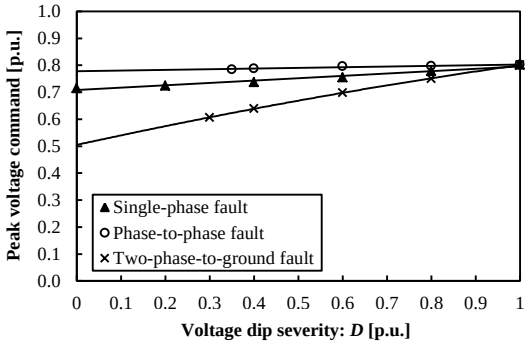
Figure 4-5 shows the junction temperatures of four IGBTs and diodes in the cells u1, v1 and w1 under the same condition. The peak junction temperatures increase to maximum 121˚C and 114˚C at the diodes and IGBTs of the v1 and w1 cells. These temperatures are above the limit of 106˚C by considering a 15 % margin for the IGBT modules with the absolute maximum rating of the junction temperature which is defined by the manufacturer (see Table 2-5).



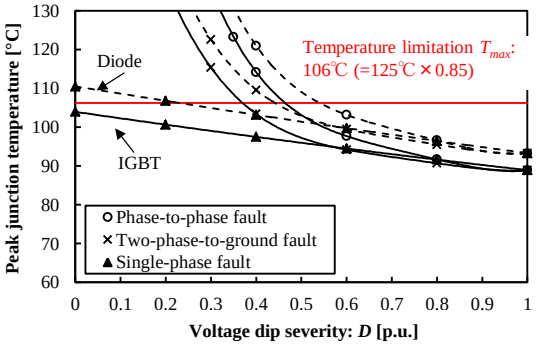
(a) u1-cell (b) v1-cell (c) w1-cell

Figure 4-5 Thermal distribution of the MMCC-SDBC under phase-to-phase fault with a dip severity *D* of 0.4 p.u [19].

Figure 4-6 shows the maximum peak voltage command and peak junction temperature among the cells for different dip severities *D* under various grid fault scenarios. It can be seen that the peak voltage command does not saturate in various grid fault scenarios. The peak junction temperatures increase quickly with phase-to-phase fault and two-phase-to-ground fault conditions and reach an upper temperature limit of 106˚C when the voltage dip is 0.55 and 0.45 p.u., respectively.



(a) Peak voltage command



(b) Peak junction temperature

Figure 4-6 Electrical-thermal simulations of the MMCC-SDBC at different dip severities [19].

4.4. ELECTRICAL AND THERMAL SIMULATIONS OF THE MMCC-DSCC [19]

Figure 4-7 shows the simulated key waveforms of the MMCC-DSCC under the phase-to-phase fault with a dip severity D = 0 p.u.. It can be noted that the arm currents (i.e. i_{uu}, i_{ul}, i_{vu}, i_{vl}, i_{wu}, and i_{wl}) contain both half value of the output phase current and the circulating DC current i_{Zu}, i_{Zv} and i_{Zw} for the dc-link capacitor voltage balancing under asymmetrical grid fault conditions. Here, the circulating current is equivalent to

$$i_{Zu} = \frac{i_{uu} + i_{ul}}{2},\ i_{Zv} = \frac{i_{vu} + i_{vl}}{2},\ i_{Zw} = \frac{i_{wu} + i_{wl}}{2} \tag{4.3}$$

It is noted that the r.m.s. value of the arm current increases by only a few % under the phase-to-phase fault.

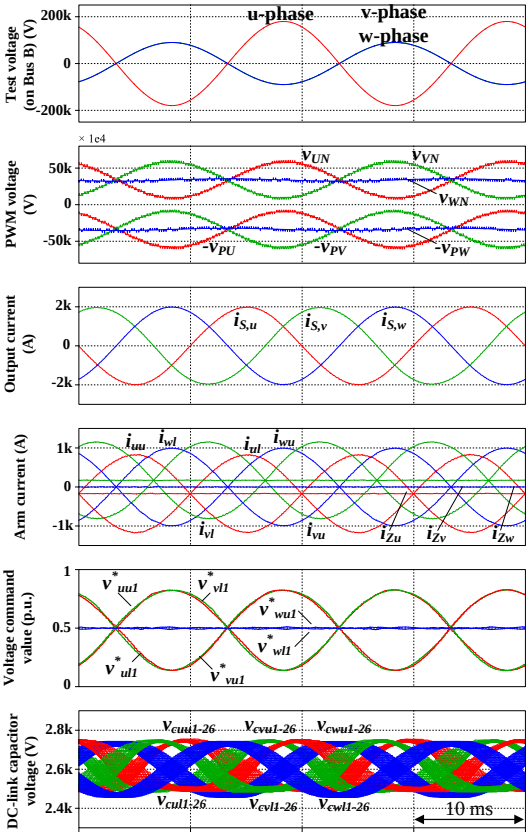


Figure 4-7 Key waveforms of the MMCC-DSCC under phase-to-phase fault with a dip severity D of 0 p.u. [19]

Figure 4-8 shows the junction temperatures of IGBTs and diodes in the chopper converter cells uu1, vu1, wu1, ul1, vl1 and wl1 under the same condition. The junction temperatures are widely distributed among the arms compared with the other MMCC types because the chopper converter cells are used with different modulation index among the arms. The peak junction temperature increases to maximum 104 ˚C at the diodes of u1 cells. This temperature is below the limit of 106˚C by considering a 15 % margin for the IGBT modules by using the absolute maximum rating of the junction temperature defined by the manufacturer (see Table 2-5).

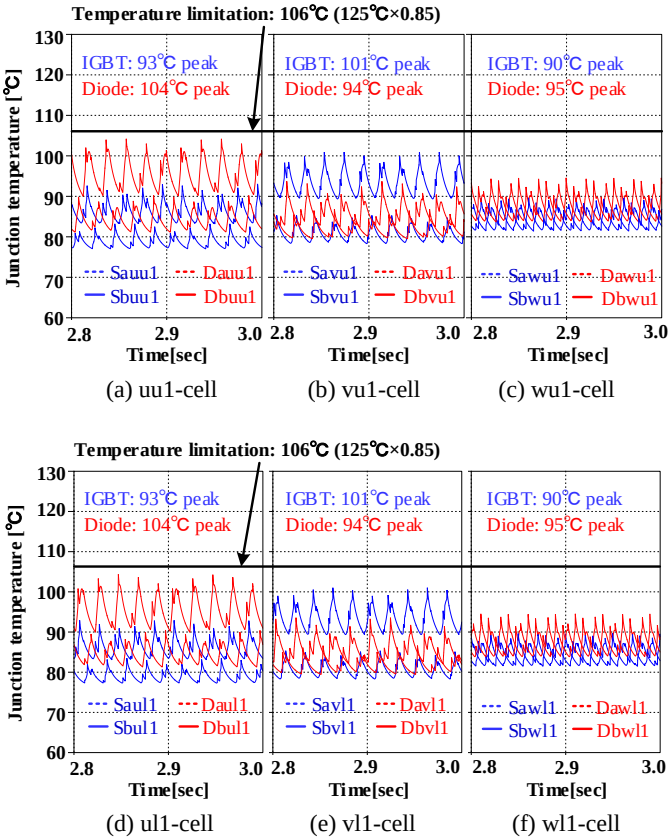
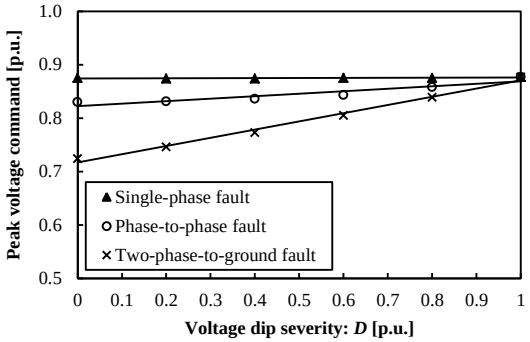
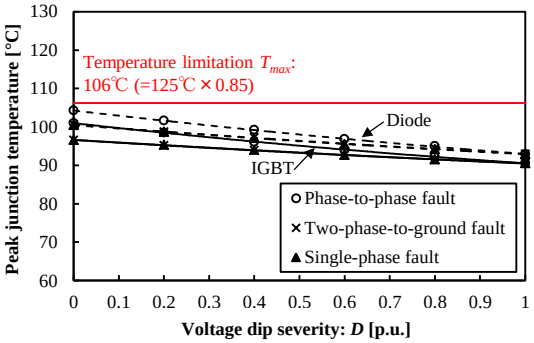


Figure 4-8 Thermal distribution of the MMCC-DSCC under phase-to-phase fault with a dip severity *D* of 0 p.u. [19]

Figure 4-9 shows the maximum peak voltage command value and peak junction temperature among the arms regarding the voltage dip severity *D* under various grid fault scenarios. It can be noted that the peak voltage command does not saturate in the various grid fault scenarios. The peak junction temperature does not reach the temperature limitation in the various grid fault scenarios.



(a) Peak voltage command



(b) Peak junction temperature

Figure 4-9 Electrical-thermal simulations of the MMCC-DSCC at different dip severities [19].

4.5. ELECTRICAL AND THERMAL SIMULATIONS OF THE MMCC-DSBC [19]

Figure 4-10 shows the simulated key waveforms of the MMCC-DSBC under the single-phase-to-ground fault with a dip severity D = 0.4 p.u.. It can be noted that the arm currents and PWM output voltage of each arm contain the dc component as well as the DSCC. However, the amplitude of the PWM output voltage with dc-component is smaller than the DSCC because of avoiding the voltage saturation of each cell output voltage command. In this result, the circulating DC current increases for the capacitor voltage balancing control.

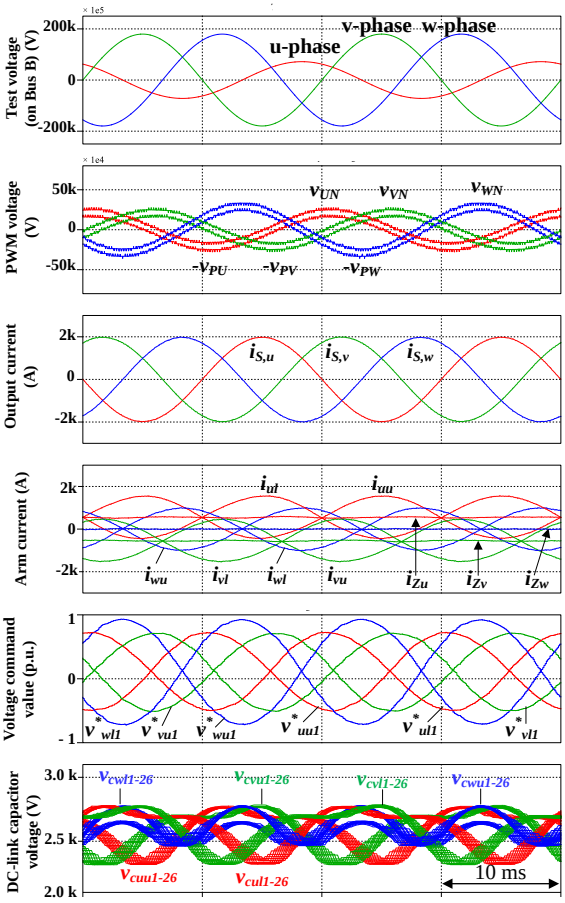


Figure 4-10 Key waveforms of the MMCC-DSBC under single-phase-to-ground fault with a dip severity D of 0.4 p.u [19].

Figure 4-11 shows the junction temperatures of IGBTs and diodes in the H-bridge converter cells uu1, vu1, wu1, ul1, vl1 and wl1 under the same conditions. The junction temperatures are widely distributed among the arms compared with the MMCC-DSBC because in addition to different circulating current among phases, the H-bridge converter cells are used with different modulation index among the arms. The peak junction temperature increases to maximum 104 ˚C at the diodes of uu1 cells. This temperature is below the limit of 106˚C by considering a 15 % margin for the IGBT modules with the absolute maximum rating of junction temperature, which is defined by the manufacturer (see Table 2-5).

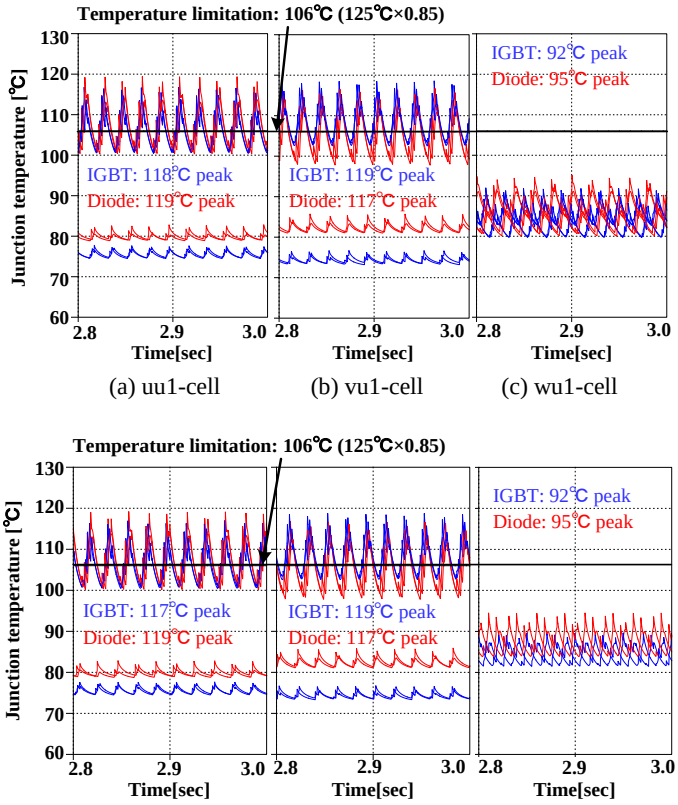
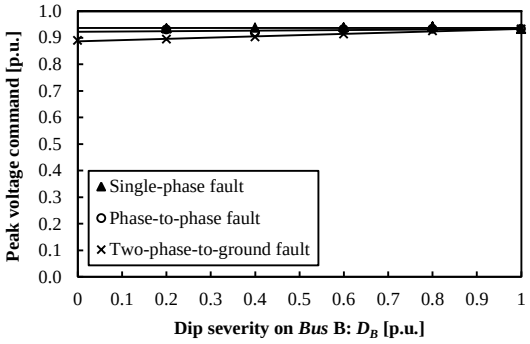
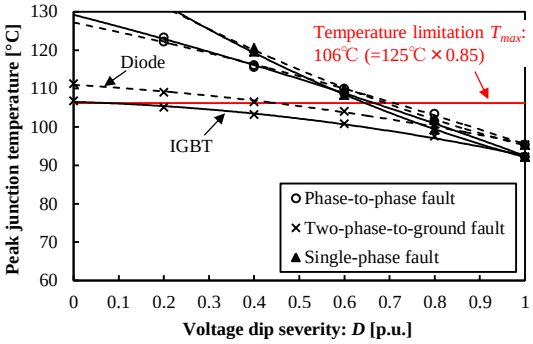


Figure 4-11 Thermal distribution of the MMCC-DSBC under single-phase-to-ground fault with a dip severity *D* of 0.4 p.u. [19]

Figure 4-12 shows the maximum peak voltage command value and peak junction temperature among the arms regarding dip severity *D* under various grid fault scenarios. It can be noted that the peak voltage command keeps the same value under various grid fault conditions with the different voltage dip severity because the V'_{PN} is injected maximum value to minimize the amplitude of the circulating DC current. The peak junction temperatures exceed the limit in value, when *D* is lower than 0.6. However, the slope is moderate compared with the SDBC.



(a) Peak voltage command



(b) Peak junction temperature

Figure 4-12 Electrical-thermal simulations of the MMCC-DSBC at different dip severities [19].

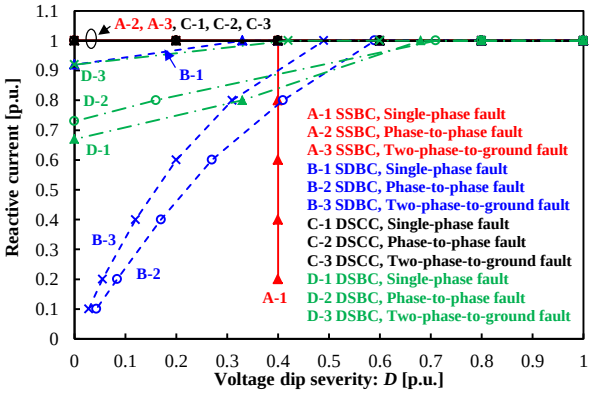
4.6. PERFORMANCE COMPARISON BETWEEN THE MMCC FAMILY [19]

Figure 4-13 (a) shows the reactive current compensation capability for the MMCC solutions with SSBC, SDBC, DSCC and DSBC in order to enable a proper voltage-balancing between the cell converters under the different dip severity *D* with various grid faults. The compensation capability limits of the MMCC family are determined by the modulation index saturation point and the maximum junction temperature. Figure 4-13 (b) and (c) show the peak voltage command and peak junction temperature of the IGBT modules in the whole converter cells corresponding to the operating conditions giving Figure 4-13 (a). The peak voltage command and junction temperature are normalized by instantaneous dc-link voltage for each cell converter and the temperature limitation value is decided by the manufacturer as mentioned in the 4.2, 4.3 and 4.4. The MMCC family can continue to supply the rated reactive current when the dip severity of the grid voltage is higher than 0.7 p.u., but the reactive current compensation capability shows different characteristics for a dip severity lower than 0.7 p.u. as discussed below.

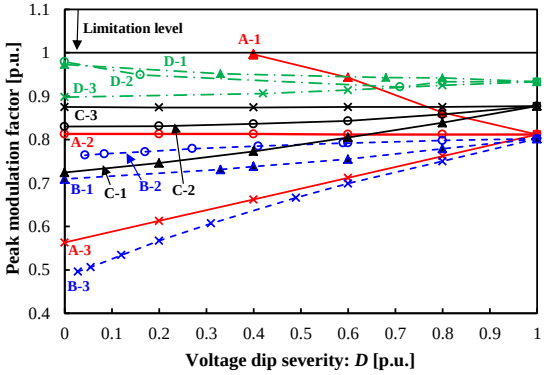
1) The MMCC-SSBC: It reveals that the SSBC can supply the rated reactive current under phase-to-phase fault and two-phase-to-ground fault condition regardless of the dip severity. However, the reactive current capability decreases steeply at a voltage dip severity of 0.4 p.u. for single-phase-to-ground fault and it cannot operate anymore even if the current derating is activated because of the saturation of peak voltage command by the zero-sequence AC voltage injection. It seems that this characteristic is a problem in practical use.

2) The MMCC-SDBC: The SDBC can supply the reactive current by a few percentages of reactive current derating under single-phase-to-ground fault to avoid over junction temperature by a slightly increased zero-sequence AC current. The SDBC can also keep the operation under phase-to-phase short circuit fault and two-phase-to-ground fault by larger reactive current derating, which characteristics seem to be better than the SSBC. However, the required zero-sequence current is dramatically increased toward infinity when the voltage dip severity approaches zero under the phase-to-phase short circuit fault and two-phase-to-ground fault, as mentioned theoretically in Chapter 3.3.

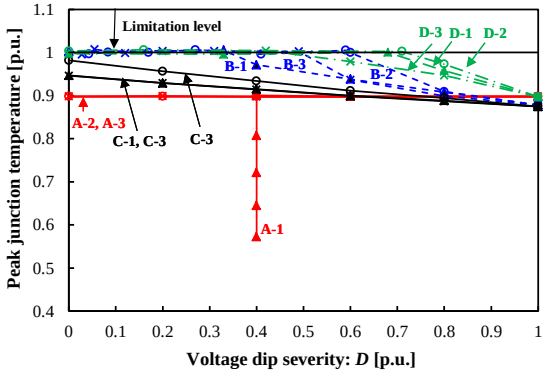
3) The MMCC-DSCC: The DSCC is injecting circulating DC current among the legs, which have two degrees of freedom and can balance the DC-link capacitor voltages under asymmetrical grid fault conditions. The amplitude of the circulating DC current becomes smaller than the zero-sequence AC current for the SDBC, which has only one degree of freedom. In this result, the DSCC can supply the reactive current under all grid fault scenarios without reactive current derating in this case.



(a) Reactive current capability



(b) Voltage command according to the reactive current



(c) Junction temperature according to the reactive current

Figure 4-13 Reactive current compensation capability of the MMCCs for different dip severities [19].

4) The MMCC-DSBC: The dc-link capacitor voltage balancing method for the DSBC is similar to the DSCC. However, the amplitude of the circulating DC current on the DSBC will have a larger value compared with the DSCC in compensation for lower injectable DC voltage capability between terminal P and N. The DSBC can keep the operation under all grid fault scenarios with a maximum of 35% current derating to avoid an over junction temperature, which characteristics is worse than the DSCC, but much better than the SSBC and SDBC.

Table 4-1 summarizes asymmetrical Low Voltage Ride Through capability as well as the key component sizes of the MMCC solutions for the STATCOM application, which are obtained from Figure 4-13 and Table 2-3, respectively.

Table 4-1 Performance comparison between the MMCC-STATCOM solutions.

	SSBC	SDBC	DSCC	DSBC
Total power semiconductor chip area [p.u.] (Total device counts [p.u.])	**1** (1)	**1** (1.7)	**1** (2)	**1** (2)
Total energy stored in interconnection inductor [p.u.] (Total device counts [p.u.])	**1** (1)	**1** (1)	**1** (2)	**1** (2)
Total energy stored in dc-link capacitor [p.u.] (Total device counts [p.u.])	**1** (1)	**1** (1.7)	**4** (4)	**1** (2)
Asymmetrical Low Voltage Ride Through Capability	+	+	+++	++

4.7. SUMMARY

This paper investigates the asymmetrical Low Voltage Ride Through (LVRT) capability of a practical 80 MVar / 33 kV scale MMCC based STATCOM having potentially used four configurations which are called the SSBC, SDBC, DSCC, and DSBC in large scale offshore wind power plants.

The practical designed SSBC and SDBC are not able to handle Low Voltage Ride Through operating conditions under some of the grid faults because of the dc-link capacitor voltage control. The DSCC can keep the operation in all grid fault scenarios for the whole voltage dip severity without any current derating. However, the total volume of the MMCC-DSCC seems larger than other MMCC solutions because the total energy stored in the capacitors becomes larger by using chopper converter cells. The DSBC can keep the operation in all grid fault scenarios for the whole dip severity with a maximum of 35% current derating in this case study. The total cost and volume of the DSBC seems similar to SSBC and SDBC because of similar total power semiconductor chip area and total energy stored of the passive components. The present result suggests that the DSBC is the most attractive solution for the STATCOM application of the MMCC family.

CHAPTER 5. A DC-LINK CAPACITOR VOLTAGE RIPPLE REDUCTION METHOD FOR AN MMCC-SDBC [J2]

This chapter proposes a capacitor voltage ripple reduction method by using third harmonic zero-sequence current for a Modular Multilevel Cascade Converter (MMCC) with Single Delta Bridge Cells (SDBC). A practical case study on an 80 MVar/ 33 kV MMCC-SDBC based STATCOM is used to demonstrate the method. The impact of the third harmonic zero-sequence current level of the capacitor ripple reduction and the electro-thermal stresses on IGBT modules are investigated. An optimal parameter of the current level is obtained by compromising the above two performance factors. The required capacitance as well as capacitor bank volume are reduced by 20 % by applying the proposed method.

5.1. INTRODUCTION [44]

A common disadvantage of each MMCC topology is the dc-link capacitor voltage ripple having a second-order at the grid frequency in each cell converter. To suppress the capacitor voltage ripple below a certain value, the capacitor size becomes larger. In addition, when the carrier frequency of each cell converter for a PWM is designed to be lower than a few hundred Hz, the capacitor voltage ripple significantly increases due to the impact of the harmonic components of the carrier frequency, which is the practical case [24], [25].

Several capacitor voltage ripple reduction methods for an MMCC with Double Star Chopper Cells (DSCC) have been presented [27, 45, 46, 47, 48, 49, 50]. These methods reduce the voltage ripple by injecting a circulating current with second-order at the grid frequency. It is noted that these papers do not consider the impact of the carrier frequency to the capacitor voltage ripple, as stated previously and this influence cannot ignore where the carrier frequency is lower than a few hundred Hz.

On the other hand, any voltage ripple reduction methods for other MMCC solutions with Single Star Bridge Cells (SSBC) and Single Delta Bridge Cells (SDBC) have not been proposed. Here, the SSBC and SDBC could inject zero-sequence voltage and zero-sequence current, respectively, instead of the circulating current, so there is a possibility to suppress the capacitor voltage ripple using these zero-sequence components in both the SSBC and SDBC.

In this chapter, the capacitor voltage ripple reduction method for one type of MMCC such as a Single Delta Bridge Cells (SDBC) is proposed. Firstly, the capacitor

voltage ripple reduction effect by using the proposed third harmonic zero-sequence current injection method is analyzed considering the impact of the low carrier frequency. Secondly, the electrical losses and junction temperatures of each power semiconductor switch regarding the amplitude of the injected third harmonic zero-sequence current are simulated based on the case study model. Third, the optimum third-harmonic zero-sequence current to reduce the capacitor voltage ripple is presented. Finally, the capacitor bank is designed for each case considering the required capacitance and reliability. The capacitor bank volume reduction effect by applying the proposed method is finally discussed.

5.2. THE THEORETICAL BEHAVIOR OF THE DC-LINK CAPACITOR VOLTAGE [44]

Table 5-1 shows the detailed specification of the MMCC-SDBC for this case study. Phase-shift PWM modulation is chosen because of the advantage that the principal electro-thermal stresses of the IGBT modules and capacitors are equally distributed among the cells in the same cluster.

Here, the dc-link capacitor voltage of each cell-converter in the MMCC-SDBC with the conventional condition and the proposed voltage ripple reduction method is analyzed theoretically.

Table 5-1 The detailed specification of the MMCC-SDBC [44].

Rated power Q_r	±80 MVA
Nominal grid voltage V_s	33 kVrms
Nominal cell DC-side voltage V_{Cref}	2600 Vdc
Nominal cell AC-side voltage v_x	1450 Vrms
Equivalent switching frequency f_{eq_sw}	10.35 kHz
Rated line current I_r	808 Arms
Carrier frequency f_c	225 Hz
Grid frequency f_g	50 Hz
Interconnection inductor L_{ac}	7.8 mH (6%)
Dc-link capacitance each cell C_x	7.0 mF
IGBT module (rated 4500 V / 900 A)	MBN900D45A
Expected lifetime	20 years or more

5.2.1. CONVENTIONAL OPERATION [44]

Figure 5-1 shows with a solid line the conventional operation waveforms of the u1-cell converter as an example. When the MMCC-SDBC is in steady state and each dc-link capacitor voltage is balanced, the output voltage reference of each cell in the u-phase cluster e_{m_u} is given by

$$\begin{aligned} e_{m\_u} &= M_a \sin\theta_m + e_{m\_z} \\ M_a &\equiv \frac{\sqrt{2}\left(V_s \pm \omega_s L_{ac} I/\sqrt{3}\right)}{\left(N_{cell}/3\right)V_{Cref}} \end{aligned} \tag{5.1}$$

with the modulation factor: M_a, the phase angle of the u-phase cluster voltage: θ_m, each cell output voltage of the zero-sequence component: e_{m_z}, the nominal grid voltage: V_s, the grid frequency: ω_s, the inductance of each phase-cluster AC inductor: L_{ac}, the phase current at the PCC: I, the total cell number: N_{cell}, the dc-link voltage reference of each cell converter: V_{Cref}. The e_{m_z} has zero value in this condition. It is noted that the polarity of the voltage drop of the AC inductor depends on leading/lagging of the STATCOM output current.

The e_{c_u1} is the carrier signal of the u1-cell converter. The ϕ_{c_u1} is the phase delay of the e_{c_u1} from the e_{m_u}, which has a zero value in Figure 5-1. Each phase delay ϕ_{c_un} of the other cell converters in the u-phase cluster is given by

$$\phi_{c\_un}\Big|_{n=1,2\cdots,N_{cell}/3} = 2\pi\frac{n-1}{N_{cell}/3} + \phi_{c\_u\_ini} \tag{5.2}$$

with the number of the optional cell in the u-phase cluster: n, the initial phase of the u1-cell: $\phi_{c\_u\_ini}$. As an example, in case of the u1-cell, the phase delay ϕ_{c_u1} was set to be 0 with $n = 1$ and $\phi_{c\_u\_ini} = 0$.

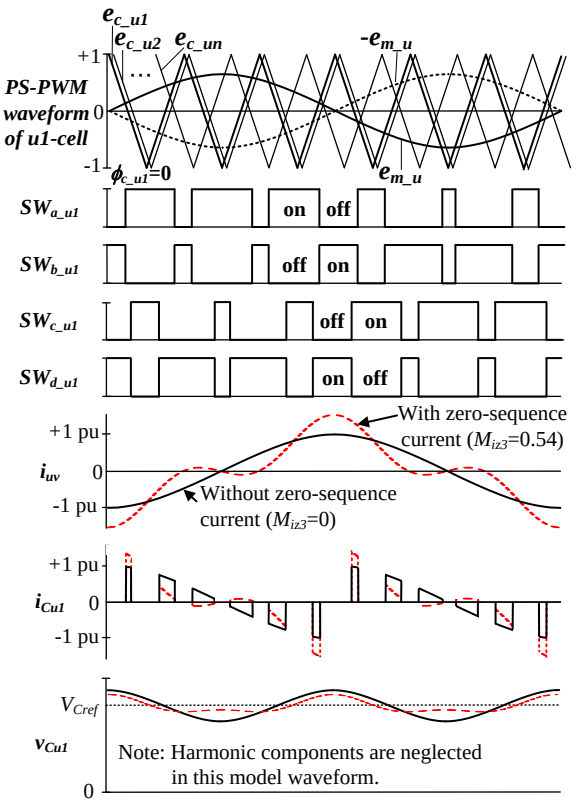


Figure 5-1 The PWM waveforms and current in the u1-cell for the MMCC-SDBC circuit [44].

The switching functions SW_{a_u1}, SW_{b_u1}, SW_{c_u1} and SW_{d_u1} define the on/off states of the power semiconductor switches S_{a_u1}, S_{b_u1}, S_{c_u1} and S_{d_u1}, respectively, which is determined by the PS-PWM of the e_{m_u1} and the e_{c_u1} by neglecting the dead time duration.

The u1-cell output current, as well as u-phase cluster current i_{uv}, is defined as

$$i_{uv} = \sqrt{\frac{2}{3}} I \sin\left(\theta_m + \phi_{pf}\right) + i_{zero} \tag{5.3}$$

where ϕ_{pf} is the power factor of the MMCC-SDBC, i_{zero} is the zero-sequence current. It is noted that the zero-sequence current i_{zero} is controlled to zero value where all capacitor voltages are balanced.

The dc-link capacitor current i_{Cu1} of the u1-cell is given by using the switching

functions as follows:

$$i_{Cu1} = -i_{uv}\left(SW_{a\_u1} - SW_{c\_u1}\right) \tag{5.4}$$

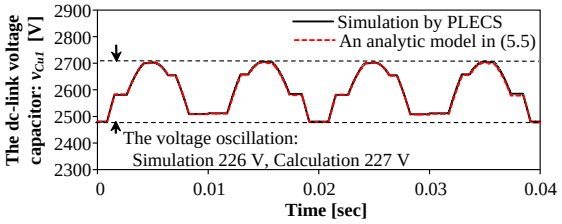
By integrating (5.4), the dc-link capacitor voltage v_{cu1} of the u1-cell is expressed by (5.5) with the initial value of v_{cu1}: V_{Cu1_ini}.

$$v_{Cu1} = -\frac{1}{C}\int i_{Cu1}dt + V_{Cu1\_ini} = -\sqrt{\frac{2}{3}}\frac{IM_a}{4\omega_m C}\sin\left(2\omega_m t + \phi_{pf}\right)$$

$$+\frac{1}{C}\int\sqrt{\frac{2}{3}}I\sin\left(\omega_m t+\phi_{pf}\right)\sum_{n=1}^{\infty}\frac{4}{n\pi}\cos\left(\frac{n\pi}{2}\right)\sin\left[\frac{n\pi}{2}\left\{M_a\sin\omega_m t + M_{a3}\sin\left(3\omega_m t-\phi_{iz3}+\frac{\pi}{2}\right)\right\}\right]\cos\left(n\omega_c t - n\phi_c\right)dt + V_{Cu1\_ini}$$

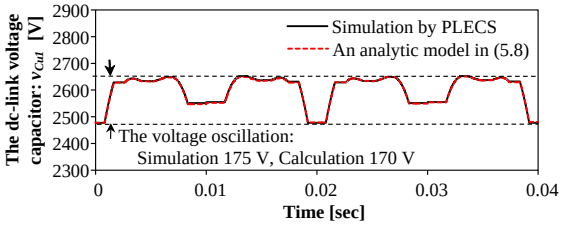
(5.5)

Figure 5-2(a) plots the v_{Cu1} based on the analytic ac model (5.5) and the simulations, respectively, under with ϕ_{C_u1} = - 3.11 rad, V_{Cu1_ini} = 2480 V as an example. The analytic ac model corresponds reasonably well with the simulation result.



Note: M_a = 0.827 p.u., M_{a3} = 0 p.u. ϕ_{C_u1} = -3.11 rad, V_{c_ini} = 2480 V

(a) Conventional operation as the M_{iz3} = 0 p.u.



Note: M_a = 0.827, M_{a3} = 0.0702 p.u. ϕ_{C_u1} = -3.11 rad, V_{c_ini} = 2477 V

(b) Proposed operation with M_{iz3} = 0.5 p.u.

Figure 5-2 The u1-cell capacitor voltage waveforms [44].

5.2.2. PROPOSED CAPACITOR VOLTAGE RIPPLE REDUCTION METHOD [43]

Figure 5-1 shows with a solid line the conventional example. The i_{zero} is normally controlled to be zero value where all capacitor voltages are balanced. However, it is possible to output an optional value. A third harmonic zero-sequence current which has the same angle and amplitude among the three phase clusters to be able to reduce the dc-link capacitor voltage ripple is considered in the next.

The i_{zero} is defined as

$$i_{zero} = \sqrt{\frac{2}{3}} I M_{iz3} \sin\left(3\theta_m + \phi_{iz3}\right) \tag{5.6}$$

where M_{iz3} is the amplitude ratio of the i_{zero} at the output phase r.m.s. current I, ϕ_{iz3} is the phase difference from θ_m.

In order to inject the i_{zero}, each cell converter requires additional output voltage. The additional output-voltage reference e_{m_z} is given by

$$e_{m\_z} = M_{a3} \sin\left(3\theta_m + \frac{\pi}{2} + \phi_{iz3}\right), \; M_{a3} = \frac{\sqrt{6}\omega_m L_{ac} I M_{iz3}}{(N_{cell}/3) V_{Cref}} \tag{5.7}$$

With regard to (5.1), (5.3), (5.4), (5.6) and (5.7), the v_{Cu1} injected by the i_{zero} can be written as (5.8).

$$\begin{aligned} v_{Cu1} = & -\sqrt{\frac{2}{3}} \frac{I M_a}{4\omega_m C} \left\{ \sin\left(2\omega_m t + \phi_{pf}\right) - M_{iz3} \sin\left(2\omega_m t + \phi_{iz3}\right) + \frac{M_{iz3}}{2} \sin\left(4\omega_m t + \phi_{iz3}\right) \right\} \\ & + \sqrt{\frac{2}{3}} \frac{I M_{a3}}{4\omega_m C} \left\{ \sin\left(2\omega_m t - \phi_{iz3} + \frac{\pi}{2} - \phi_{pf}\right) - \frac{1}{2} \sin\left(4\omega_m t - \phi_{iz3} + \frac{\pi}{2} + \phi_{pf}\right) - \frac{M_{iz3}}{3} \cos\left(6\omega_m t + \frac{\pi}{2}\right) \right\} \\ & + \sqrt{\frac{2}{3}} \frac{I}{C} \int \left\{ \sin\left(\omega_m t + \phi_{pf}\right) + M_{iz3} \sin\left(3\omega_m t + \phi_{iz3}\right) \right\} \sum_{n=1}^{\infty} \frac{4}{n\pi} \cos\left(\frac{n\pi}{2}\right) \sin\left[\frac{n\pi}{2} \left\{ M_a \sin \omega_m t + M_{a3} \sin\left(3\omega_m t - \phi_{iz3} + \frac{\pi}{2}\right) \right\} \right] \\ & \cos\left(n\omega_c t - n\phi_{c\_u1}\right) dt + V_{Cu1\_ini} \end{aligned} \tag{5.8}$$

The M_{iz3} and ϕ_{iz3} are considered to reduce the dc-link capacitor voltage by using (5.8). For the sake of simplicity, only the first term in (5.8) is in focus here. It is noted that the third and fourth term in (5.8) is the harmonic component associated with the carrier frequency f_c. Because the M_{a3} is much smaller than M_a, the second term in (5.8) is much smaller than the first term. It is obvious that, when ϕ_{iz3} is ϕ_{pf}, the ripple of v_{Cu1} by the double frequency of the f_g can be suppressed in response to the M_{iz3}.

Figure 5-2 (b) shows the v_{Cu1} based on the analytic model (5.8) and the simulations, respectively, under which ϕ_{C_u1} = - 3.11 rad, V_{Cu1_ini} = 2477 V and used in an example. These waveforms correspond reasonably well. The error of the voltage ripple amplitude of the v_{Cu1} is 3%.

5.2.3. DC-LINK CAPACITOR VOLTAGE RIPPLE [43]

The capacitor voltage ripple Δv_{Cu1} of the u1-cell is calculated with numeric calculations using equation (5.9) substituted (5.5) or (5.8), which period is the least common multiples among f_g and f_c.

$$\Delta v_{Cu1} = \max\left(v_{Cu1}\right) - \min\left(v_{Cu1}\right) \tag{5.9}$$

Figure 5-3 shows with a dot line the plot of the capacitor voltage ripple in respect to the M_{iz3} based on the analytical model (5.9) with ϕ_{c_u1} = -3.11 rad. The other condition is the same as Figure 5-2. The circle shows the Δv_{Cu1} based on the simulation with the same condition of the dot line. These results correspond reasonably well with the maximum error of the Δv_{Cu1} = 3.7% at M_{iz3} = 0.6. The capacitor voltage ripple of the other cells can also be calculated by using the same equation (5.8) with different ϕ_{c_un}. The maximum and minimum capacitor voltage ripple Δv_{c_max} and Δv_{c_min} in respect to the ϕ_{c_un} are plotted by solid lines, respectively. As an example, the capacitor voltage ripple is reduced by 24 % by injecting the M_{iz3} of 0.5 p.u.

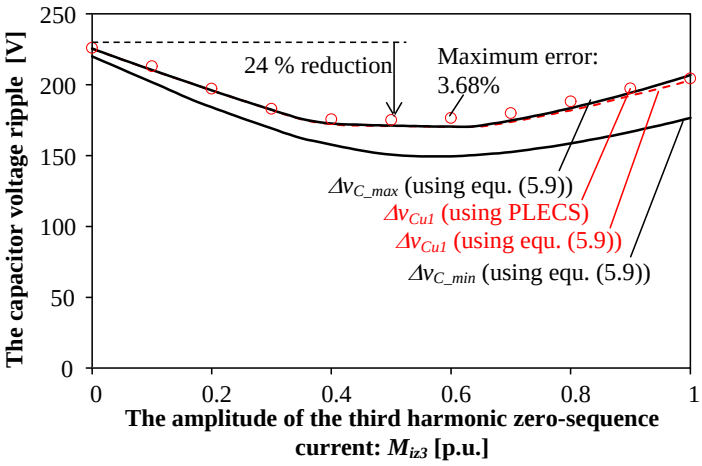


Figure 5-3 The u1-cell capacitor voltage oscillation in respect to the amplitude ratio M_{iz3} [44].

5.3. POWER SEMICONDUCTOR LOSSES AND JUNCTION TEMPERATURES [43]

The electrical and thermal simulations of the IGBT modules in the MMCC-SDBC regarding the M_{iz3} are implemented by using the simulation software PLECS. The specification of the MMCC - SDBC is shown in Figure 2-2 (b) and Table 5-1. The reactive current reference $i_{d,ref}$ is set to be the rated 1 p.u. The third harmonic current reference i_{z3}^* can be defined by (5.10), which current is controlled by using the block diagram as shown in Figure 2-8.

$$i_{z3}^* = M_{iz3}\sqrt{\frac{i_{d,ref}^2+i_{q,ref}^2}{3}}\sin\left(3\theta_m + \phi_{pf}\right) \tag{5.10}$$

The power loss and junction temperature of each power module are also simulated by using PLECS. The simulation model used is mentioned in Chapter 2.4.

Figure 5-4 shows the total semiconductor losses and electrical efficiency of the MMCC-SDBC with respect to the M_{iz3}. It is noted that the total semiconductor losses increase when M_{iz3} is above 0.3 p.u., because the r.m.s. value of each cluster current increases. However, the total semiconductor losses are slightly reduced when M_{iz3} is below 0.3 because of the V_{ce} - I_c characteristics of the used bipolar devices.

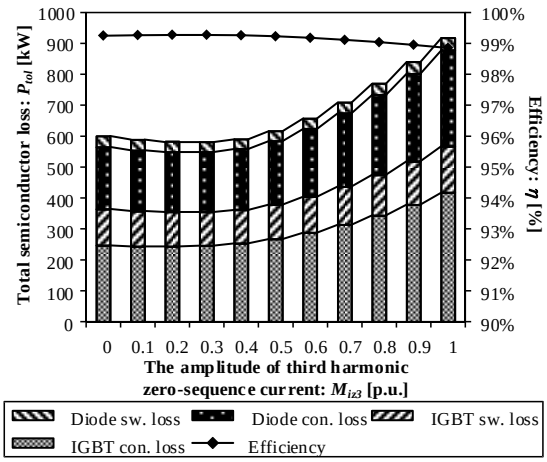


Figure 5-4 The total semiconductor losses of the 80 MVar MMCC-SDBC [44].

Figure 5-5 shows the instant peak and average junction temperature of the IGBT and Diode, where the maximum thermal stress among the 276 modules with respect to M_{iz3} are shown. It is noted that the average junction temperature exhibits similar trends as the total losses. On the other hand, the peak junction temperature increases as a function of the M_{iz3} because the peak value of the phase-cluster current increases regarding of the M_{iz3}.

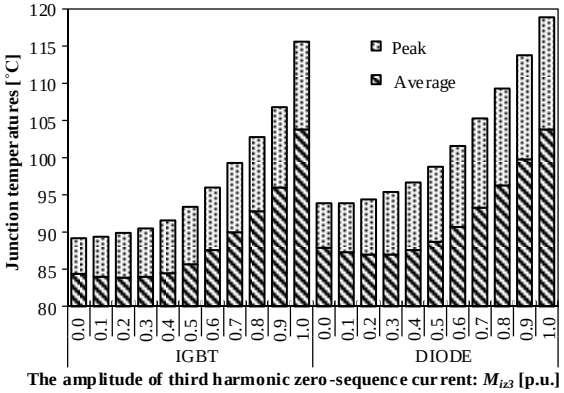


Figure 5-5 The junction temperature of an IGBT and Diode, which is chosen to be the maximum in all switches of the MMCC-SDBC [44].

Figure 5-6 shows the total semiconductor losses and the capacitor voltage ripple regarding the M_{iz3} standardized at the zero value of the M_{iz3}. The M_{iz3} is selected to be 0.4 p.u. where the capacitor voltage ripple could be reduced to a maximum without any total power semiconductor loss increase compared with the conventional method ($M_{iz3} = 0$).

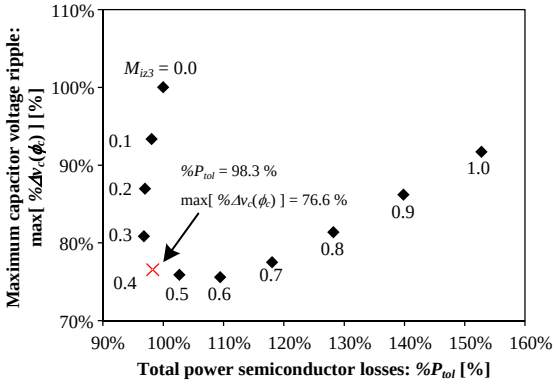
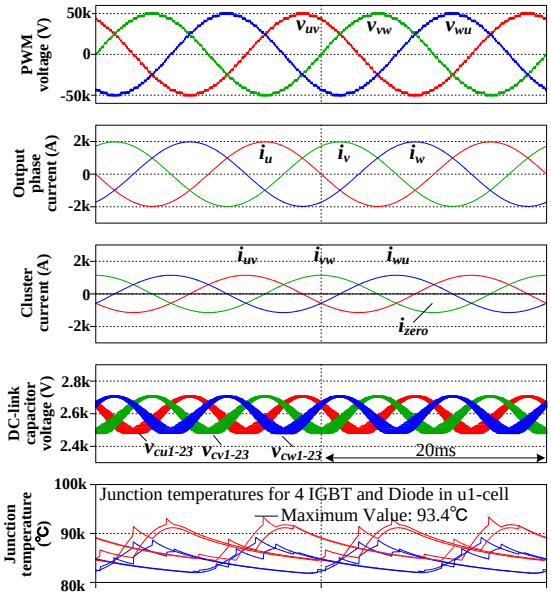
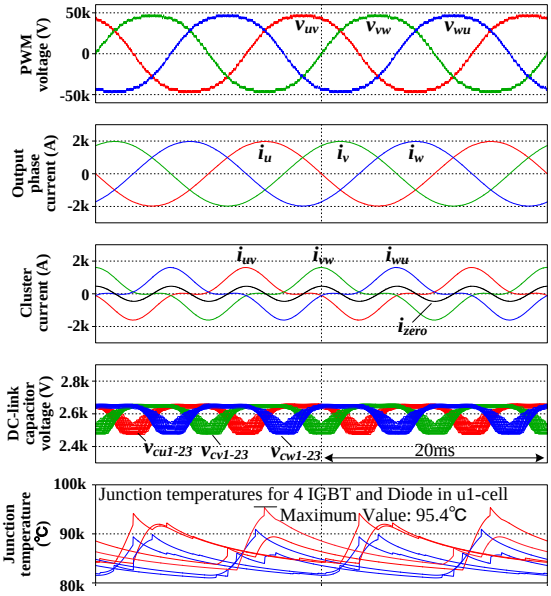


Figure 5-6 The total semiconductor loss and the capacitor voltage ripple as a function of M_{iz3} at rated 80 MVar operation [44].

Figure 5-7 shows the electrical and thermal simulation waveforms with M_{iz3} = 0 (the conventional operation) and M_{iz3} = 0.4 (the proposed operation), respectively. The output phase currents for these cases are controlled adequately. It is noted that the total harmonic distortion of the output phase current with conventional M_{iz3} = 0 and proposed M_{iz3} = 0.4 are almost the same, which are 0.35% and 0.4%, respectively. The maximum peak modulation factors of each converter cell with M_{iz3} = 0 and 0.4 are 0.80 pu and 0.76 pu, respectively. In other words, the modulation factor could be reduced 0.04 pu by injecting third harmonic zero-sequence current with M_{iz3} = 0.4. The peak value of the cluster current for the proposed case increases by 40 % because of the third harmonic zero-sequence current injected. In this result, the peak junction temperature of the power module in u1-cell increases 2 K. The other junction temperatures in the other cell converters have similar values because of the selected Phase Shift PWM modulation technique. The capacitor voltage ripple for the proposed case is decreased by 20 %. These waveforms show no evidence of abnormalities.



(a) The conventional operation (M_{iz3} = 0)



(b) The proposed operation (M_{iz3} = 0.4)

Figure 5-7 Key simulation waveforms of the MMCC-SDBC operating at rated 80 MVar and M_{iz3} = 0, 0.4 [44].

5.4. CAPACITOR BANK DESIGN [43]

The final purpose of the proposed capacitor voltage ripple reduction method is to reduce the entire capacitor bank size. Surely, the required capacitance is reduced by applying the proposed method, but the current through the capacitor bank is changed by the injected third harmonic zero-sequence current. The capacitor bank size depends not only on the required capacitance but also on the current ripple through the capacitor bank [51], [52]. In order to clarify the capacitor bank size reduction effect of the proposed method, the capacitor bank is designed in this section.

5.4.1. CAPACITOR BANK STRUCTURE [43]

Table 5-2 shows the target specification of the capacitor bank for the MMCC-SDBC having the specification given by Table 5-1. The type of the dc-link capacitor is selected to be metalized polypropylene film capacitor (MPPF-Cap), which is commonly chosen for the medium and high voltage class MMCC solutions because of high reliability [53], [5]. The capacitance of the dc-link capacitor bank with the conventional operation and the proposed method are set to be 7 mF and 5.4 mF, respectively, where the capacitor voltage ripples are suppressed to be less than 10%.

Table 5-2 Target specification of the capacitor bank in an MMCC-SDBC model [44].

	Conventional method	Proposed method
Capacitor type	Metallized polypropylene film capacitor	
Rated dc voltage	2600 Vdc	
Capacitance	7 mF or more	5.4 mF or more
Expected life time	20 years or more	
Ambient temperature	60 °C	

Figure 5-8 shows the proposed dc-link capacitor bank structure. The capacitor bank is constructed by series and parallel connection of an MPPF-Cap. Table 5-3 shows the capacitor bank specification of both the conventional and the proposed case. The capacitor bank is selected to use 560 μF, 1300 Vdc, Type 947C MPPF-Cap from Cornell Dubilier [54]. In order to overcome the applied dc voltage to the capacitor bank, the series connection number is designed to be 2 for both cases. For providing the capacitor bank with the required capacitance, the parallel counts of the conventional and the proposed case are designed to be 25 and 20, respectively. It is noted that the capacitor bank volume is reduced by 20% by applying the proposed method in this case study.

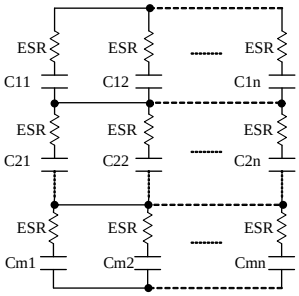


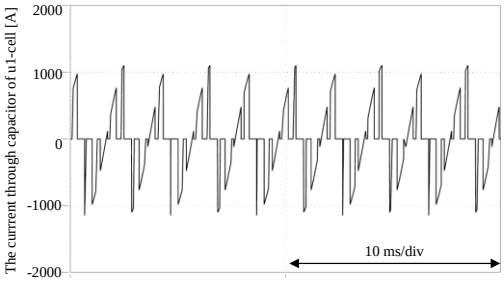
Figure 5-8 The capacitor bank structure for a cell [44].

Table 5-3 The capacitor bank specification [44].

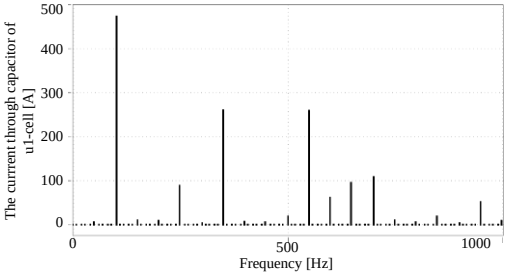
	Conventional case	Proposed case
Used capacitor	560 μF, 1300 Vdc, 85 °C, Type 947C Polypropylene Film DC-Link Capacitors from Cornell Dubilier (MPPF)	
Series connection count: *m*	2	2
Parallel connection counts: *n*	25	20
Total count: *m*×*n*	50	40
Total capacitance	7.00 mF	5.60 mF
Rated voltage	2600 Vdc	
Total capacitor volume	0.111 m^3	0.089 m^3

5.4.2. THERMAL STRESS OF EACH MPPF-CAP. [43]

The hot spot temperatures of the dc-link capacitors under the conventional and proposed condition are calculated, which have to be kept below the rated temperature determined by the manufacturer. Figure 5-9 and Figure 5-10 show the current waveforms through the dc-link capacitor bank of the u-1 cell and an FFT analysis with or without the proposed method. The simulation conditions are the same as shown in Figure 5-7. By applying the proposed method, the main current ripple component as the double fundamental frequency is reduced by 33% and distributed to higher frequency components. The r.m.s. values of the current through the capacitor bank in the conventional and the proposed case are 473 Arms and 426 Arms, respectively.

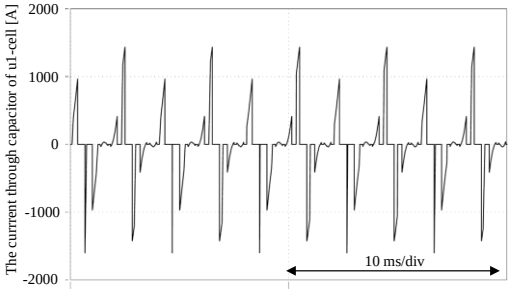


(a) Current waveform through the capacitor bank (473 Arms)

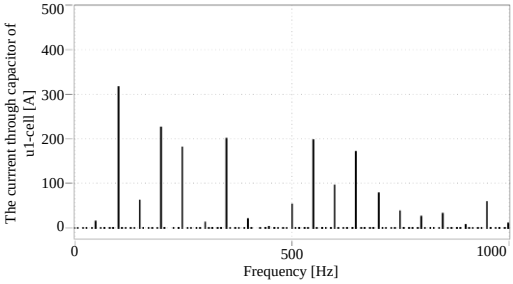


(b) FFT analysis

Figure 5-9 The current through the capacitor bank for the conventional case [44].



(a) Current waveform through the capacitor bank (426 Arms)



(b) FFT analysis

Figure 5-10 The current through the capacitor bank using the proposed method [44].

In order to simplify the calculations, it is assumed that the current through each individual capacitors in the capacitor bank is balanced. The power loss of each capacitor is given by

$$P_{loss} = \sum_f ESR(f) \cdot I_C^2(f) \tag{5.11}$$

where *ESR*(*f*) is the Equivalent Series Resistance of the capacitor regarding the frequency *f*, I_C is the r.m.s. current through each capacitor in respect to *f*. The core temperature of the capacitor is given by

$$T_C = T_a + P_{Loss} \cdot R_{th} \tag{5.12}$$

where T_a is the ambient temperature around the capacitor and it is assumed to be 60 °C in this case, R_{th} is the thermal resistance of the capacitor at 3 K/W in this case.

Table 5-4 shows the P_{loss} and T_c of the individual capacitor between the conventional and proposed case. The power loss and hot spot temperature of the proposed capacitor case become slightly higher than the conventional case in order to be reduced a parallel number of the capacitors. However, because the ESR of the film capacitors have a small value, the core temperatures of the used capacitor for both cases become lower than its absolute temperature of 85 °C.

Table 5-4 Power loss and hot spot temperature of each capacitor [44].

	Conventional case	Proposed case
Power loss	1.11 W	1.36 W
Hot spot temperature	63.3 °C	64.1 °C

5.4.3. EXPECTED LIFETIME OF THE CAPACITOR BANK [43]

Generally, MPPF-Caps have very long lifetime under controlled operating conditions including the applied dc-voltage, the core temperature of the capacitor and the humidity compared with Aluminum Electrolytic Capacitors, which have wear out failure modes. For such kind of components, it is important to estimate the reliability by using its lifetime model. In this chapter, the lifetime of the capacitor bank under the conventional and proposed case is estimated by using the provided information from the capacitor manufacturer.

A widely used capacitor lifetime model applicable for film capacitor is as follows [55]:

$$L = L_0 \times \left(\frac{V}{V_0}\right)^{-n} \times 2^{\frac{T_0 - T}{k}} \tag{5.13}$$

where L is the lifetime under the thermal and electrical stress T and V, L_o is the lifetime under the reference temperature T_0 and the nominal voltage V_0. The coefficients k and n are temperature dependent constants and the voltage stress constant, respectively. The parameters L_0, T_0, n, and k for the used capacitor are obtained from the provided lifetime curve fitting as, 200000, 66 °C, 19.4, and 3.9, respectively.

Actually, there is a probability on a lifetime of individual capacitors, which is taken into considered as given below [56]. It is assumed that the variation of the lifetime obeys the normal distribution. The cumulative distribution function (CDF) for the normal distribution can be calculated by

$$F(t) = \frac{1}{2}\left\{1 + erf\left(\frac{t-\mu}{\sigma\sqrt{2}}\right)\right\} \tag{5.14}$$

where μ is the mean of the distribution, σ is the standard deviation, erf is the error function. The μ is determined by the expected lifetime calculated by (5.13). The σ is determined by considering ±10% variation with a 95% confidence interval (CI).

It is assumed that all the considered devices are connected in series in the reliability model, i.e., any capacitor in the capacitor bank failure will lead to system failure. Then the capacitor bank wear-out failure $F_{CB}(t)$ can be calculated by

$$F_{CB}(t) = 1 - \prod(1 - F_i(t)) \tag{5.15}$$

where $F_i(t)$ is the CDF of an individual capacitor used in constructing the capacitor bank.

Figure 5-11 shows the probability curves of wear-out failures of the capacitor bank for the conventional and the proposed case. It is noted that the lifetime B_5 is to fail

5% of the total amount of capacitor bank for the conventional and proposed case, which are 31.0 years and 27.2 years, respectively. The expected lifetime of the proposed case is slightly shorter than the conventional case, because of the slightly higher capacitor temperature due to reduced capacitor number. The B_5 of both cases satisfy the target which is expected to be longer than 20 years, as mentioned in Table 5-2.

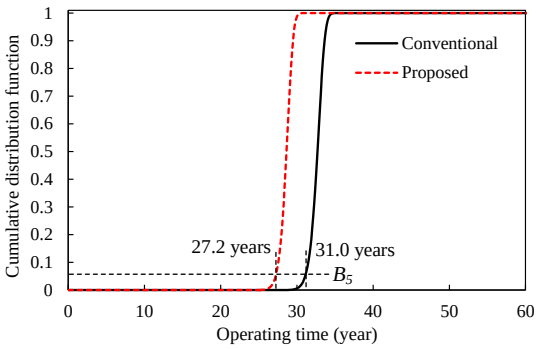


Figure 5-11 Probability curves of wear-out failure for the capacitor banks [J2].

5.5. SUMMARY

In this chapter, a capacitor voltage ripple reduction method for an MMCC-SDBC by injecting a third harmonic zero-sequence current is proposed. The capacitor voltage ripple is analyzed, considering the impact of the harmonics by the practical low carrier frequency. The electrical loss and junction temperature of each power semiconductor switch regarding the amplitude of the zero-sequence current M_{iz3} are analyzed. In the case study, the capacitor voltage ripple maximum is reduced by 23 % at M_{iz3} = 0.4 p.u without increasing the total power semiconductor losses for the proposed method. The capacitor bank volume is also reduced 20 % by applying the proposed method.

CHAPTER 6. CONCLUSIONS

The main conclusions of this study are addressed in this chapter.

6.1. SUMMARY OF THESIS

The Modular Multilevel Cascade Converter (MMCC) has become a promising solution for medium voltage class STATCOM applications since it was presented in the middle of the 1990s. However, there are still open questions in the point of view of practical use, arisen from its unique architecture having galvanic isolated dc-link capacitors for each converter cell, and they are qualified in this study based on a practical case study on an 80 MVar / 33 kV scale STATCOM used in a large scale offshore wind power plant. Following have been studied:

(1) Asymmetrical Reactive Power Capability of Modular Multilevel Cascade Converter (MMCC) based STATCOMs

This study clarifies the performances of four configurations of the MMCC family with SSBC, SDBC, DSCC, and DSBC for the STATCOM in large scale offshore wind power plants, with special focus on the asymmetrical Low Voltage Ride Through (LVRT) capability under grid faults. From Chapter 2 to Chapter 4, the sizing of the key components, number of cells, electro-thermal analysis, mathematical analysis under asymmetrical reactive power output condition considering the dc-link capacitor voltage balancing control, and reactive current capability of an practical 80 MVar / 33 kV scale MMCC based STATCOM are presented.

The practical designed SSBC and SDBC have limitations in the Low Voltage Ride Through operation under some of the grid fault conditions because of the dc-link capacitor voltage control. The DSCC can keep the operation in all grid fault scenarios for the whole voltage dip severity without any current derating. However, the total volume of the MMCC-DSCC seems larger than other MMCC solutions, because the total energy stored in the capacitors becomes larger for using chopper converter cells. The DSBC can keep the operation in all grid fault scenarios for the whole dip severity with a maximum of 35% current derating in this case. The total cost and volume of the DSBC seems similar to SSBC and SDBC because of the same total power semiconductor chip area and total energy stored of the passive components. The present result suggests that the DSBC could be the most attractive solution for the STATCOM application for the MMCC family.

(2) A DC-link Capacitor Voltage Ripple Reduction Method for a Modular Multilevel Cascade Converter

A common disadvantage of each MMCC topology compared with the conventional topology is that a dc-link capacitor voltage ripple of second-order of the grid frequency exists in each cell converter. This study proposes a capacitor voltage ripple reduction method for one type of MMCC as a Single Delta Bridge Cells (SDBC) by injecting the third harmonic zero-sequence current. In Chapter 5, an analytic model of the dc-link capacitor voltage, the electrical loss and junction temperature of each power semiconductor switch, the optimum third-harmonic zero-sequence current level, and the capacitor bank design are presented and also considering the reliability. The capacitor voltage ripple could be reduced by 23 % without increasing the total power semiconductor losses for the proposed method. The capacitor bank volume is also reduced 20 % by applying the proposed method.

6.2. CONTRIBUTIONS

The major contributions of this Ph. D. study are described below;

(1) Asymmetrical Reactive Power Capability of Modular Multilevel Cascade Converter (MMCC) based STATCOMs

- ✓ The mathematical formulation for the STATCOM based on the potentially used four types of the MMCC solutions under asymmetrical compensation operation is developed, which contributes to quantitative understanding of the performance limitation and circuit behavior under the asymmetrical compensation.

- ✓ Specifications and the component sizing of each type of practical 80 MVar / 33 kV scaled MMCC-STATCOM are carefully designed and compared. After that, the electro-thermal stresses of the actual power modules used in each type of the MMCC with practical controls are analyzed in detail. The asymmetrical reactive power capacity focusing on the MMCC solutions is compared under different scenarios of grid faults, with the consideration of the device temperature limits and voltage saturations. Based on the obtained result, the most attractive MMCC solution for the STATCOM application is achieved, which is the MMCC-DSBC.

(2) A DC-link Capacitor Voltage Ripple Reduction Method for a Modular Multilevel Cascade Converter

- ✓ A dc-link capacitor voltage ripple reduction method by using third harmonic zero-sequence current for one type of MMCC with Single Delta Bridge Cells (SDBC) is proposed.

- ✓ The analytic model of the capacitor voltage considering the proposed third harmonic zero-sequence current injection and the impact of the low carrier frequency is developed, which quantitatively contribute to show the capacitor voltage ripple reduction effect.

- ✓ The optimum third-harmonic zero-sequence current to reduce the capacitor voltage ripple is determined by compromising the power semiconductor loss and the capacitor voltage ripple.

- ✓ The capacitor bank of each case is designed considering the required capacitance and reliability, to clarify the capacitor bank volume reduction effect by applying the proposed method. The required capacitance as well as the capacitor bank volume is reduced by 20 % by applying the proposed method.

6.3. FUTURE WORK

Some future interesting topics from the point of view of the author derived from this Ph.D. study are noted as follows;

- ➢ In order to validate the obtained result in this thesis experimentally, the practical test system is built.

- ➢ The development of the total system simulation model is an interesting topic, in order to design the optimum size of the STATCOM of the offshore wind power plant.

- ➢ Total system reliability calculation of the whole offshore wind power plant including wind turbines and the STATCOM are interesting topics.

- ➢ The investigation of asymmetrical reactive current injection capability of the MMCC based STATCOM under grid fault conditions by both positive- and negative-sequence reactive current injection becomes also an interesting topic,

which is the most advanced requirement emerging in an European country specified as an optional code.

- An impact analysis of the asymmetrical reactive current injection by the MMCC-based STATCOM to the faulty grid on the offshore wind farm area is an interesting topic because some types of wind turbines have a limitation to keep the operation under serious faulty grid voltages, which may need to be improved.

- A dc-link capacitor voltage ripple reduction method of an MMCC with Single Star Bridge Cells (SSBC) has not been proposed yet. There is a possibility to reduce the dc-link capacitor voltage by using zero-sequence voltage as well as zero-sequence current of the MMCC-SDBC.

Literature list

[1] IEA, Renewable Energy Medium-Term Market Report 2015, IEA Publications, 2015.

[2] F. Blaabjerg and M. Guerrero, "Smart Grid and Renewable Energy Systems," in *Proc. Electrical Machines and Systems (ICEMS)*, 2011, pp. 1-10.

[3] T. Ackermann, "Wind Power in Power Systems", 2nd Edition, West Sussex: John Wiley & Sons Ltd., 2012.

[4] M. Claus, S. Mcdonald, P. Cahill, D. Retzmann, M. Pereira and K. Uecker, "Innovative VSC Technology for Integration of "Green Energy" - without Impact on System Protection and Power Quality," in *Proc. CIRED International Conference on Electricity Distribution*, 2011, pp. 1-4.

[5] K. Sharifabadi, L. Harnefors, H. Nee, S. Norrga and R. Teodorescu, "Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems", Wiley-IEEE Press, 2016.

[6] A. Nabae, I. Takahashi and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, Vols. IA-17, no. 5, pp. pp. 518-523, Sep./Oct. 1981.

[7] S. Mori, K. Matsuno, T. Hasegawa, S. Ohnishi, M. Takeda, M. Seto, S. Murakami and F. Ishiguro, "Development of a large static VAr generator using self-commutated inverters for improving power system stability," *IEEE Trans. Power Syst.*, vol. 8, no. 1, pp. pp. 371-377, Feb. 1993.

[8] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (MMCC)," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3119-3130, Nov. 2011.

[9] H. Akagi, "Multilevel Converters: Fundamental Circuits and Systems," *Proceedings of the IEEE*, vol. 105, no. 11, pp. 2048-2065, Nov. 2017.

[10] F. Z. Peng and J. Wang, "A Universal STATCOM with Delta-Connected Cascade Multilevel Inverter," in *Proc. IEEE Power Electronics Specialists*

Conference, 2004, pp. 3529-3533.

[11] F. Z. Peng, J. Lai, J. W. McKeever and J. VanCoevering, "A Multilevel Voltage-Source Inverter with Separate DC Sources for Static Var Generation," *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1130-1138, Sep. 1996.

[12] R. Marquardt and A. Lesnicar, "A new modular voltage source inverter topology," in *Proc. IEEE EPE*, 2003, pp. 1-10.

[13] M. Pereira, D. Retzmann, M. Wiesinger and G. Wong, "SVC PLUS: An MMC STATCOM for Network and Grid Access Applications," in *Proc. IEEE Trondheim PowerTech*, 2011, pp. 1-5.

[14] J. Glasdam, "Harmonics in Offshore Wind Power Plants Employing Power Electronic Devices in the Transmission System", Aalborg University, 2015, Ph.D. thesis.

[15] B. Ronner, P. Maibach and T. Thurnherr, "Operational experiences of STATCOMs for wind parks," *IET Renewable Power Generation*, vol. 3, no. 3, pp. 349-357, 2009.

[16] F. Blaabjerg , D. M. Ionel, "Renewable Energy Devices and Systems with Simulations in MATLAB® and ANSYS®", 1st Edition, CRC Press, 2017.

[17] K. Ma, M. Liserre and F. Blaabjerg, "Operating and Loading Conditions of a Three-Level Neutral-Point-Clamped Wind Power Converter Under Various Grid Faults," *IEEE Trans. Ind. Appl.*, vol. 50, pp. 520-530, Jan./Feb. 2014.

[18] T. Neumann, T. Wijnhoven, G. Deconinck and I. Erlich, "Enhanced Dynamic Voltage Control of Type 4 Wind Turbines During Unbalanced Grid Faults," *IEEE Trans. Energy Convers.*, vol. 30, no. 4, pp. 1650-1659, Dec. 2015.

[19] T. Tanaka, K. Ma, H. Wang and F. Blaabjerg, "Asymmetrical Fault Ride Through capability of a STATCOM based on Modular Multilevel Cascade Converters," *IEEE Trans. Power Electron.*, 2018 (in press).

[20] CIGRE/CIRED/UIE Joint Working Group C4.110, Voltage Dip Immunity of Equipment and Installations, CIGRE, 2010.

[21] IEC 61000-4-34, Electromagnetic compatibility (EMC) - Part 4-34: Testing and measurement techniques - Voltage dips, short interruptions and voltage

variations immunity tests for equipment with input current more than 16 A per phase. IEC, 2009.

[22] M. H. Bollen, Understanding Power Quality Problems, New York, US: John Wiley & Sons Ltd., 2000.

[23] R. Teodorescu, M. Liserre , P. Rodriguez, Grid Converters for Photovoltaic and Wind Power Systems, New York, US: John Wiley & Sons Ltd., 2011.

[24] K. Ilves, L. Harnefors, S. Norrga and H.-P. Nee, "Analysis and Operation of Modular Multilevel Converters With Phase-Shifted Carrier PWM," *IEEE Trans. Power Electron.,* vol. 30, no. 1, pp. 268-283, Jan. 2015.

[25] E. Behrouzian, M. Bongiorno and R. Teodorescu, "Impact of Switching Harmonics on Capacitor Cells Balancing in Phase-Shifted PWM-Based Cascade H-Bridge STATCOM," *IEEE Trans. Power Electron.,* vol. 32, no. 1, pp. 815-824, Jan. 2017.

[26] M. Hagiwara, R. Maeda and H. Akagi, "Negative-Sequence Reactive-Power Control by a PWM STATCOM Based on a Modular Multilevel Cascade Converter (MMCC-SDBC)," *IEEE Trans. Ind. Appl.,* vol. 48, no. 2, pp. 720-729, Mar.-Apr. 2012.

[27] A. Marzoughi, R. Burgos, D. Boroyevich and Y. Xue, "Analysis of capacitor voltage ripple minimization in modular multilevel converter based on average model," in *Proc. IEEE COMPEL,* 2015, pp. 1-7.

[28] Y. J. Ota, Y. Shibano, N. Niimura and H. Akagi, "A Phase-Shifted-PWM D-STATCOM Using a Modular Multilevel Cascade Converter (SSBC)—Part I: Modeling, Analysis, and Design of Current Control," *IEEE Trans. Ind. Appl.,* vol. 51, no. 1, pp. 279-288, Jan./Feb. 2015.

[29] H. Song and K. Nam, "Dual Current Control Scheme for PWM Converter Under Unbalanced Input Voltage Condition," *IEEE Trans. Ind. Electro.,* vol. 46, no. 5, pp. 953-959, Oct. 1999.

[30] J. Svensson, M. Bongiorno and A. Sannino, "Practical Implementation of Delayed Signal Cancellation Method for Phase-Sequence Separation," *IEEE Trans. Power Del.,* vol. 22, no. 1, pp. 18-26, Jan. 2007.

[31] P. Rodriguez, A. V. Timbus, R. Teodorescu, M. Liserre and F. Blaabjerg, "Flexible Active Power Control of Distributed Power Generation Systems

During Grid Faults," *IEEE Trans. Ind. Electro.*, vol. 54, no. 5, pp. 2583-2592, Oct. 2007.

[32] J. Svensson, M. Bongiorno and A. Sannino, "Practical Implementation of Delayed Signal Cancellation Method for Phase-Sequence Separation," *IEEE Trans. on Power Delivery*, vol. 22, no. 1, pp. 18-26, 2007.

[33] R. E. Betz, T. Summers and T. Furney, "Symmetry Compensation using a H-Bridge Multilevel STATCOM with Zero Sequence Injection," in *Proc. of IEEE IAS Annual Meeting*, 2006, pp. 1724-1731.

[34] E. Behrouzian and M. Bongiorno, "Investigation of Negative-Sequence Injection Capability of Cascaded H-Bridge Converters in Star and Delta Configuration," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1675-1683, Feb. 2017.

[35] T. Kikuma and M. Takasaki, "A Method Unbalance Compensation on Y-connection Modular Multilevel Converter (Japanese)," *IEEJ Trans. Ind. Appl.*, vol. 132, no. 12, pp. 1159-1166, 2012.

[36] Y. Ota, Y. Shibano, N. Niimura and H. Akagi, "A Phase-Shifted PWM D-STATCOM Using a Modular Multilevel Cascade Converter (SSBC)—Part II: Zero-Voltage-Ride-Through Capability," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 289-296, Jan.-Feb. 2015.

[37] M. Hagiwara, R. Maeda and H. Akagi, "Negative-Sequence Reactive-Power Control by the Modular Multilevel Cascade Converter Based on Double-Star Chopper-Cells (MMCC-DSCC)," in *Proc. IEEE ECCE*, 2010, pp. 3949-3954.

[38] M. Guan and Z. Xu, "Modeling and Control of a Modular Multilevel Converter-Based HVDC System Under Unbalanced Grid Conditions," *IEEE Trans. Power Electron.*, vol. 27, no. 12, pp. 4858-4867, Dec. 2012.

[39] J. Jung, S. Cui, Y. Lee and S. Sul, "A Cell Capacitor Energy Balancing Control of MMC-HVDC under the AC Grid Faults," in *Proc. IEEE ECCE-Asia*, 2015, pp. 1-8.

[40] Website of Hitachi Power Semiconductor Device, Ltd., "Product Lineup of 4500V-IGBT module," [Online]. Available: http://www.hitachi-power-semiconductor-device.co.jp/en/products/igbt/4500v/index.html. [Accessed 6 10 2018].

[41] Z. He, F. Ma, Q. Xu, Y. Chen, C. Li, M. Li, J. M. Guerrero and A. Luo, "Reactive Power Strategy of Cascaded Delta-Connected STATCOM Under Asymmetrical Voltage Conditions," *IEEE Journal of Emerg. and Selec. Topics in Power Electron.*, vol. 5, no. 2, pp. 784 - 795, Jun. 2017.

[42] P. Sochor, N. M. L. Tan and H. Akagi, "Low-Voltage-Ride-Through Control of a Modular Multilevel Single-Delta Bridge-Cell (SDBC) Inverter for Utility-Scale Photovoltaic Systems," *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 4739 - 4751, June 2018.

[43] P. Wu, Y. Chen and P. Cheng, "The Delta-Connected Cascaded H-Bridge Converter Application in Distributed Energy Resources and Fault Ride Through Capability Analysis," *IEEE Trans. Ind. Appl.*, vol. 53, no. 2, pp. 4665-4672, Sep./Oct. 2017.

[44] T. Tanaka, H. Wang and F. Blaabjerg, "DC-link capacitor voltage ripple reduction method of an MMCC-SDBC by third harmonic zero-sequence current injection," in *Proc. IEEE ECCE Asia*, 2018, pp. 2604-2610.

[45] H. H. Parikh, R. S. M. Loeches, G. Tsolaridis, R. Teodorescu, L. Mathe and S. Chaudhary, "Capacitor voltage ripple reduction and arm energy balancing in MMC-HVDC," in *Proc. IEEE EEEIC*, 2016, pp. 1-6.

[46] H. Kim, S. Kim, Y. Chung, D. Yoo, C. Kim and K. Hur, "Operating Region of Modular Multilevel Converter for HVDC With Controlled Second-Order Harmonic Circulating Current: Elaborating P-Q Capability," *IEEE Trans. on Power Delivery*, vol. 31, no. 2, pp. 493-502, Apr. 2016.

[47] K. Li, C. Li, F. C. Lee, M. Mu and Z. Zhao, "Precise Control Law of MMC and Its Application in Reducing Capacitor Voltage Ripple by Injecting Circulating Current," in *Proc. International Conference on Electrical Machines and system (ICEMS)*, 2015, pp. 371-377.

[48] C. D. Townsend, R. Aguilera, P. Acuna, G. Konstantinou, J. Pou and G. C. Goodwin, "Capacitance Minimization in Modular Multilevel Converters: Using Model Predictive Control to Inject Optimal Circulating Currents and Zero-Sequence Voltage," in *Proc. IEEE SPEC*, 2016, pp. 1-6.

[49] M. A. Perez and S. Bernet, "Capacitor Voltage Ripple Minimization in Modular Multilevel Converters," in *Proc. International Conference on Industrial Technology (ICIT)*, 2015, pp. 3022-3027.

[50] J. Pou, S. Ceballos, G. Konstantinou, V. G. Agelidis, R. Picas and J. Zaragoza, "Circulating Current Injection Methods Based on Instantaneous Information for the Modular Multilevel Converter," *IEEE Trans. Ind. Electron.,* vol. 62, no. 2, pp. 777-788, Feb. 2015.

[51] H. Wang and F. Blaabjerg, "Reliability of Capacitors for DC-Link Applications in Power Electronic Converters — An Overview," *IEEE Trans. Ind. App.,* vol. 50, no. 5, pp. 3569-3578, Sep./Oct 2014.

[52] Y. Song and B. Wang, "Survey on Reliability of Power Electronics System," *IEEE Trans. Power Electron.,* vol. 28, no. 1, pp. 591-604, Jan. 2013.

[53] V. Najmi, J. Wang, R. Burgos and D. Boroyevich, "High Reliability Capacitor Bank Design for Modular Multilevel Converter in MV Applications," in *Proc. IEEE ECCE*, 2014, pp. 1051-1058.

[54] Website of Cornell Dubilier Company, "Type 947C Polypropylene, DC Link Capacitors," [Online]. Available: http://www.cde.com/resources/catalogs/947C.pdf. [Accessed 6 10 2018].

[55] S. G. Parler, "Deriving life multipliers for electrolytic capacitors," *IEEE Power Electron. Soc. Newsl.,* vol. 16, no. 1, pp. 11-12, Feb. 2004.

[56] Y. Shen, A. Chub, H. Wang, D. Vinnikov, E. Liivik and F. Blaabjerg, "Wear-out Failure Analysis of an Impedance-Source PV Microinverter Based on System-Level Electro-Thermal Modeling," *IEEE Trans. Ind. Electron.,* 2018 (in press).

[57] T. Tanaka, H. Wang, K. Ma and F. Blaabjerg, "Reactive Power Compensation Capability of a STATCOM based on Two Types of Modular Multilevel Cascade Converters for Offshore Wind Application," in *Proc. IEEE ECCE Asia*, 2017, pp. 326 - 331.

[58] T. Tanaka, H. Wang, K. Ma and F. Blaabjerg, "Low Voltage Ride Through performance of a STATCOM based on Modular Multilevel Cascade Converter family for Offshore Wind Application," in *Proc. IEEE ECCE*, 2017, pp. 4879 - 4886.

[59] T. Tanaka, H. Wang, K. Ma and F. Blaabjerg, "Low Voltage Ride Through Capability of a STATCOM based on Modular Multilevel Cascade Converters for Offshore Wind Application," in *IEEE eT&D Workshop*, 2017.

ISSN (online): 2446-1636
ISBN (online): 978-87-7210-363-1

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