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Switching Behavior, Thermal Modeling, and Reliability Assessment

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BY
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SiC-Based 1.5-kV Photovoltaic Inverter: Switching Behavior, Thermal Modeling, and Reliability Assessment

Ph.D. Dissertation

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Abstract

Power electronic converter based on silicon carbide (SiC) devices is one of the most promising technologies for a breakthrough in renewable generation systems. Owing to its wide band-gap (WBG) characteristics, the SiC features several superiorities compared to its silicon (Si) counterpart, e.g., the increased electric field, the higher thermal conductivity, and the greater melting point. Among the application areas of SiC devices, the emerging 1.5-kV photovoltaic (PV) inverter is one of the most popular applications over the last five years. However, the broad adoption of SiC devices in emerging 1.5-kV PV inverters is still facing several reliability uncertainties. Although manufacturers have been working promptly to enhance the robustness of their SiC power devices, efforts from the application perspective are still highly demanded in several aspects.

First, owing to the high di/dt and dv/dt during the switching transient, the SiC metal-oxide-semiconductor field-effect-transistor (MOSFET) can suffer unfavorable switching behaviors, e.g., critical switching oscillations and voltage overshoots, which lead to a catastrophic breakdown in the early phase of operation. Moreover, this switching-behavior challenge becomes even more considerable in the emerging 1.5-kV PV inverter application, where three-level topologies are commonly adopted. Hence, it is highly demanded to have a switching-behavior investigation in 1.5-kV SiC-based inverters and identify the potential solution.

Secondly, the state-of-the-art thermal models fail to ensure an acceptable level of accuracy (especially in high operating temperatures), since the temperature effect on thermal performance is omitted. As the SiC device's thermal profile is closely related to several failure mechanisms, falsely predicting the junction temperature can lead to thermal runaway or accelerated degradation in both short-term and long-term operations. Therefore, a modified thermal model and its modeling methodology with improved accuracy will be needed to realize a highly reliable SiC-based PV inverter.

Thirdly, the long-term wear-out reliability of SiC MOSFETs is still threatened by the issue of die-solder fatigue inside the module, as the Young's modulus of SiC material is two times greater than Si. It has been reported

that the thermal-mechanical lifetime of SiC device with standard solder is only 1/3 of Si. Nevertheless, this lifespan deduction has not been considered in state-of-art reliability assessments and design-for-reliability cases. In this perspective, a reliability assessment considering this solder fatigue effect for the 3L-ANPC 1.5-kV PV inverter is highly demanded to evaluate how much system-level lifetime deduction can be expected.

To address the reliability issues as mentioned above, this Ph.D. project works on the following three aspects of SiC-based 1.5-kV PV inverters – switching behaviors, thermal modeling, and wear-out assessment.

Subsequently, the switching behaviors of SiC MOSFETs in a 1.5-kV three-level active-neutral-point-clamped (3L-ANPC) PV inverter are studied in a comprehensive way to identify the unfavorable switching behaviors. The issues of multi-frequency switching oscillation and the induced drain-source voltage overshoot are investigated, and the reliability-critical SiC device and root-cause parasitic component are identified accordingly. Specific design considerations are concluded to aid the design for more reliable SiC-based PV inverters with 1.5-kV dc input.

One critical point regarding an accuracy-level enhanced thermal model lies in taking the temperature effect into account. In this regard, the temperature-dependent thermal properties of several SiC power module package materials are integrated into a finite-element-method (FEM) based thermal simulation. On this basis, a temperature-dependent Cauer-type thermal model is extracted, where some of its thermal resistance and capacitance are characterized as temperature-dependent by linear polynomials. It can be concluded that the junction-heatsink thermal resistance is increased by over 10% under high junction temperatures (200 °C) by taking the temperature effect in to account.

Regarding the wear-out assessment of SiC-based 1.5-kV PV inverter, special efforts are paid on identifying a convincing lifetime model for solder-joints in the SiC power module. Based on available power cycling data and simulation results, a die-solder lifetime model is extrapolated. With the electrical and thermal models already built and validated, a mission-profile-based wear-out assessment procedure is conducted to predict the accumulated failure rate due to the wear-our of SiC modules within a lifespan of thirty years. On this basis, the wear-out reliability performance considering the SiC solder-joint wear-out can be concluded.

Dansk Resumé

Effektelektroniske omformere baseret på Silicium-Carbid (SiC) er en af de mest lovende teknologier i elektriske systemer til vedvarende energi. På grund af SiCs brede båndgapsegenskaber (WBG) har SiC flere fordele sammenlignet med det konventionelle anvendte silicium (Si). Eksempler på forbedringer er det forøget elektriske felt, en højere termisk ledeevne og et højere smeltepunkt. Blandt anvendelsesområderne af SiC-enheder er den nye 1,5 kV solcelle (PV) vekselretter en af de mest anvendte applikationer. Dog står den udbredte anvendelse af SiC-enheder i nye 1,5 kV PV-konvertere stadig over for flere pålidelighedsusikkerheder. Selvom producenterne arbejder med at forbedre robustheden af deres elektriske SiC-omformere, er pålideligheden fra applikationsperspektivet stadig meget ukendt i flere aspekter.

Som det første, grundet høje di/dt og dv/dt for SiC metal-oxid-halvleder-felt-effekt-transistor (MOSFET), opleves der ugunstige skifteadfærd under skiftende transienter af transistorerne. Dette medfører f.eks. kritiske oscillationer og uønskede spændingsoverskridelser, der kan føre til et katastrofalt nedbrud i den tidlige fase af komponentens livstid. Desuden bliver udfordringen omkring denne skifteadfærd endnu mere betydelig i den nye 1,5 kV PV-vekselretter, hvor tre-niveau typologier oftest anvendes. Det er derfor særdeles vigtigt, at der foretages en adfærdsundersøgelse af skiftende transistorer i 1,5-kV SiC-baserede vekselrettere, samt at potentielle løsninger på pålideligheds-problemet identificeres.

For det andet er moderne termiske modeller ikke i stand til at sikre et acceptabelt niveau af nøjagtighed (især ved høje driftstemperaturer), da temperatureffekten på den termiske ydeevne udelades. Da SiC-enhedens termiske profil er tæt relateret til flere fejlmekanismer, kan forkert forudsigelse af overgangs temperaturen føre til en termisk overophedning eller accelereret nedbrydelse af komponenten. Derfor vil en modificeret termisk model og dens modellerings-metodologi med forbedret nøjagtighed være nødvendig for at realisere en yderst pålidelig SiC-baseret PV-vekselretter.

Som et tredje element, trues den langsigtede pålidelighed af SiC MOSFETs af problemer med lodningstræthed inde i modulet, da Young's modulus af

SiC-materialet er to gange større end det for Si. Det er rapporteret, at den termisk-mekaniske levetid for SiC-enheder med standardlodning kun er 1/3 af det der kan forventes for Si. Ikke desto mindre er dette levetidsfradrag ikke taget i betragtning i avancerede pålidelighedsvurderinger og applikationer hvor der designes for høj pålidelighed. I dette perspektiv kræves der en pålidelighedsvurdering, hvor effekten af lodningen for en 3L-ANPC 1,5 kV PV-vekselretter undersøges, samt for at evaluere, hvor stort et levetidsfradrag der kan forventes på systemniveau.

For at tackle pålidelighedsproblemerne som nævnt ovenfor, arbejder dette ph.d. projektet med tre aspekter af SiC-baserede 1,5-kV PV-omformere, nemlig skifteadfærd, termisk modellering og slidvurdering.

Derefter foretages der et omfattende studie af skifte egenskaberne af SiC MOSFETs i en 1,5 kV 3L-ANPC PV-vekselretter for at identificere den ugunstige skifteadfærd. Spørgsmål vedrørende multi-frekvens oscillationer og den inducerede transistor overspænding er undersøgt, og den pålidelighedskritiske SiC-enhed er identificeret. Specifikke designovervejelser er givet for at forbedre designet af mere pålidelige SiC-baserede PV-vekselrettere med et 1,5 kV dc input.

Et vigtigt punkt vedrørende en forbedret termisk model med en høj nøjagtighed ligger i at tage temperatur effekten i betragtning. I dette henseende er de temperaturafhængige termiske egenskaber for flere SiC moduler integreret i en finit-element-metode (FEM) baseret termisk simulering. På dette grundlag forslåes en temperaturafhængig termisk model af Cauer-typen, hvor noget af dens termiske modstand og kapacitet er karakteriseret som temperaturafhængige lineære polynomier. Det kan konkluderes, at den overordnede termiske modstands fra modul-indre til kølelegeme kan hæves med mere end 10% under høje temperaturforhold (200 °C) ved at inkludere denne temperatureffekt.

Hvad angår slidvurderingen af SiC-baseret 1,5 kV PV-vekselrettere, gøres der en særlig indsats for at identificere en overbevisende levetidsmodel for loddeforbindelser i SiC-modulet. Baseret på tilgængelige data for effektcykler og simuleringsresultater, ekstrapoleres en levetidsmodel. Med de elektriske og termiske modeller foreslået i dette projekt, udføres en missionprofil baseret vurderingsprocedure for at forudsige den akkumulerede fejlhyppighed på grund af slid på SiC-moduler inden for en levetid på tredive år. På dette grundlag kan pålidelighedens præstation konkluderes med SiC-loddesamlinger taget i betragtning.

Contents

Thesis Details

Thesis Title: SiC-Based 1.5-kV Photovoltaic Inverter: Switching Behavior, Thermal Modeling, and Reliability Assessment

Ph.D. Student: Mengxing Chen

Supervisors: Prof. Frede Blaabjerg, Aalborg University, Denmark
Prof. Huai Wang, Aalborg University, Denmark
Prof. Xiongfei Wang, Aalborg University, Denmark

The main body of this thesis consists of the following papers:

Publications in Refereed Journals

J1. **M. Chen**, D. Pan, H. Wang, X. Wang, and F. Blaabjerg, "Investigation of Switching Oscillations for Silicon Carbide MOSFETs in Three-Level Active Neutral-Point-Clamped Inverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. PP, no. 99, pp. 1-15, 2020, Early Access.

J2. **M. Chen**, H. Wang, D. Pan, X. Wang, and F. Blaabjerg, "Thermal Characterization of Silicon Carbide MOSFET Module Suitable for High-Temperature Computationally-Efficient Thermal-Profile Prediction," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. PP, no. 99, pp. 1-12, 2020, Early Access.

J3. **M. Chen**, Z. Shen, H. Wang, X. Wang, and F. Blaabjerg, "Reliability Assessment of SiC MOSFETs in Three-Level Active Neutral-Point-Clamped Inverters Considering Die-Solder Degradation," *IEEE Trans. Power Electron.*, 2020, Status: to be Submitted.

Publications in Refereed Conferences

C1. **M. Chen**, D. Pan, H. Wang, X. Wang, F. Blaabjerg, and W. Wang, "Switching Characterization of SiC MOSFETs in Three-Level Active Neutral-Point-Clamped Inverter Application," in *Proc. 2019 10th Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, May 2019, pp. 1793-1799.

C2. **M. Chen**, H. Wang, F. Blaabjerg, X. Wang, and D. Pan, "A Temperature-Dependent Thermal Model of Silicon Carbide MOSFET Module for Long-Term Reliability Assessment," in *Proc. 2018 IEEE 4th Southern Power Electronics Conference (SPEC)*, Dec. 2018, pp. 1-7. (Best Paper Award)

C3. **M. Chen**, T. Zhu, D. Pan, H. Wang, X. Wang, and F. Blaabjerg, "Loss Analysis of SiC-Based Three-Level Active Neutral-Point-Clamped Inverters under Different Modulation Schemes," in *Proc. 2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, Status: In Press.

This thesis has been submitted for assessment in partial fulfillment of the Ph.D. degree. The thesis is a summary of the outcome from the Ph.D. project, which is documented based on the above publications. Parts of the results are used directly or indirectly in the extended summary of the thesis. The co-author statements have been made available to the assessment committee and are also available at the Faculty of Engineering and Science, Aalborg University.

Preface

This Ph.D. thesis is a summary of the Ph.D. project "Highly Efficient and Reliable SiC-based Photovoltaic Inverters", which was conducted at the Department of Energy Technology, Aalborg University, Denmark. This Ph.D. project is sponsored by Innovation Fund Denmark under grant 5185-00006B (HER-SiC project). I would like to express my gratitude to both institutions for their enduring supports. Also, I would like to thank our project partners, Harbin Institute of Technology (HIT) and Global Energy Interconnection Research Institute (GEIRI), for their continued supports.

I would like to sincerely thank my supervisor Professor Frede Blaabjerg for his patient instruction and valuable suggestions during this Ph.D. project. He is such a generous mentor who always provides me with infinite guidance and support during my academic career in Aalborg. I would also like to express the deepest gratitude to my co-supervisor Professor Huai Wang, who always offers me professional and patient advice regarding theoretical analyzing, paper drafting, and experimental testing. Likewise, I would like to sincerely thank my co-supervisor Professor Xiongfei Wang. He always provides me with enthusiasm advising and warmth encouragement.

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Mengxing Chen
Aalborg University, August 29, 2020

Report

Chapter 1

Introduction

1.1 Background

As a wide band-gap (WBG) material, the SiC exhibits several superiorities compared to its silicon (Si) counterpart, e.g., the enhanced electric field, the greater electron velocity, and the higher thermal conductivity and melting point, as exhibited in Fig. 1.1 [1]. The material properties of SiC enable practical power devices with blocking voltages an order of magnitude of the possibility in Si, improved dynamic behavior, extended operating temperature range, and significantly reduced energy losses [2, 3]. One of the most prevalent devices is the SiC metal-oxide-semiconductor field-effect-transistor (MOSFET) as it meets the requirement of 1.2–3.3 kV blocking voltage for several applications, e.g., photovoltaic (PV) converters [4], uninterruptible power supplies (UPS) [5, 6], locomotive power converters [7], and electric vehicles [8, 9].

Among these application areas, the SiC-based photovoltaic (PV) inverter is one of the most interesting research topics in the last five years [3, 4, 10–13], where improvements in the conversion efficiency and power density have been reported. As the world demands more renewable and sustainable energies, the SiC power device market for PV applications keeps increasing over recent years, as it is exhibited in Fig. 1.2 [14]. The compound annual growth rate (CAGR) of SiC power devices in PV applications is anticipated to be 11% from the year 2017 to 2023, and its market size is expected to reach 100 million US Dollars upon the year 2023.

Despite the dramatic market demand, the broad adoption of SiC MOSFET in PV inverters is still facing reliability and robustness challenges, as summarized in Table 1.1. It is noted that the SiC MOSFET suffers various reliability issues, e.g., over-voltage breakdown [15], power-cycling capability [16–19], electro-thermal instability [20, 21], short-circuit robustness [22–25], GOX re-

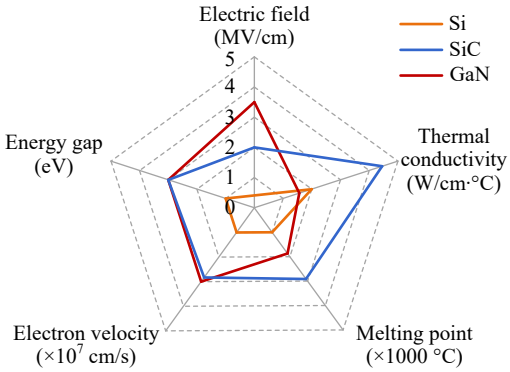


Fig. 1.1: Benchmark of material properties among Si, SiC, and GaN. [1]

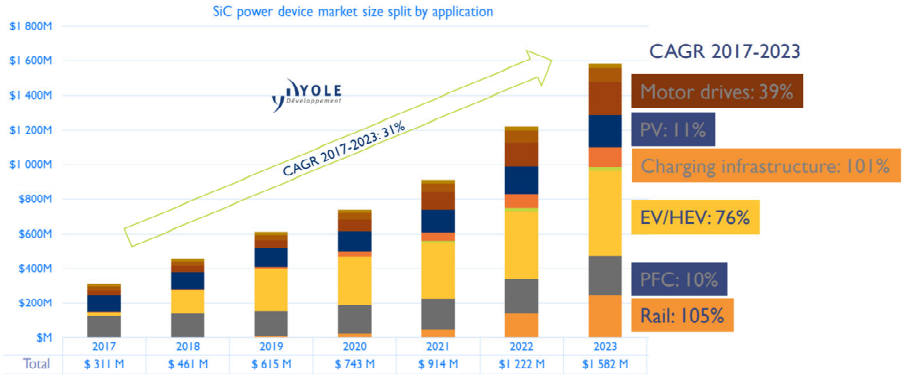


Fig. 1.2: SiC power device market share and compound annual growth rate (CAGR) split by applications. [14]

liability [18, 26, 27], threshold instability [28], and body-diode degradation [29]. In order to tackle these challenges, the device manufacturers have been working promptly to improve the robustness of their SiC power devices. For instance, the GOX of SiC MOSFET has exhibited a lifetime comparable with that of the Si insulated-gate bipolar transistor (IGBT), as it is reported in [18]. Also, novel interconnection technologies, e.g., aluminum-copper (AlCu) ribbon and silver (Ag) sintering, have seen applications in industrial prototypes to enhance their power cycling capabilities [19]. Even though, efforts from the application perspective are still highly demanded to improve the robustness and reliability of SiC-based power converters. To maximize the PV energy yields, it is generally required that the commercial PV inverters should achieve a useful lifetime of twenty years. A future lifetime target for reliable PV inverters shall be thirty years. It is still questionable if the SiC-based PV inverters are able to achieve an useful lifetime of twenty years.

Table 1.1: Reliability issues, failure mechanisms, and critical stressors of SiC MOSFET.

Reliability issues	Critical failure mechanisms	Stressors
Over-voltage breakdown [15]	Thermal runaway, PD	V_{ds}, T_{jm}
Power-cycling capability [16–19]	Solder-joint wear-out	ΔT_j, T_{jm}
Electro-thermal instability [20, 21]	Thermal runaway	T_{jm}
Short-circuit robustness [22–25]	Thermal runaway, GOX damage	T_{jm}
GOX reliability [18, 26, 27]	Extrinsic failure, over-heat	V_{gs}, T_{jm}
Threshold instability [28]	Trapped electrons	V_{gs}
Body-diode degradation [29]	Crystal defect (stacking fault)	I_f

GOX: gate oxide, PD: partial discharge, V_{ds}: drain-source voltage, T_{jm}: mean junction-temperature, ΔT_j: junction-temperature swing, V_{gs}: gate-source voltage, I_f: diode forward current.

Several reliability challenges for SiC-based PV inverters still exist from the application perspective, as listed below:

- **Challenge I – switching-behavior uncertainty:**
  Owing to the high di/dt and dv/dt during switching transients, the SiC device can suffer unfavorable switching behaviors. More critically, the emerging PV inverter commonly adopts a 1.5-kV dc-link with three-level (3L) inverters to diminish PV-power transmission losses. Integrating the fast-switching SiC MOSFETs into 3L inverters worsens their switching characteristics (e.g., critical voltage overshoots, excessive switching losses, and multiple switching-oscillation components) and may lead to immediate failure and performance degradation of the power semiconductor [30–32].

- **Challenge II – thermal uncertainty:**
  The thermal performance of a power semiconductor device is closely related to its reliability. It is noted from Table 1.1 that the mean junction-temperature T_{jm} and the junction-temperature swing ΔT_j are two of the most significant stressors to a variety of critical failure mechanisms. However, the state-of-art thermal models and their characterization methodologies fail to provide sufficient accuracy for SiC power devices, especially under high-temperature operating conditions.

- **Challenge III – wear-out uncertainty:**
  Up till now, one of the most significant failure mechanisms limiting the long-term reliability of SiC power modules is the solder-joint wear-out. As the Young's modulus of SiC is two times greater than that of Si (meaning that SiC is two times stiffer than Si), the SiC solder-joints suffer substantial mechanical stress during the long-term power cycling operations. It has been reported that the thermal-mechanical lifetime of the SiC device is only 1/3 of Si [17, 19]. However, this lifetime reduction

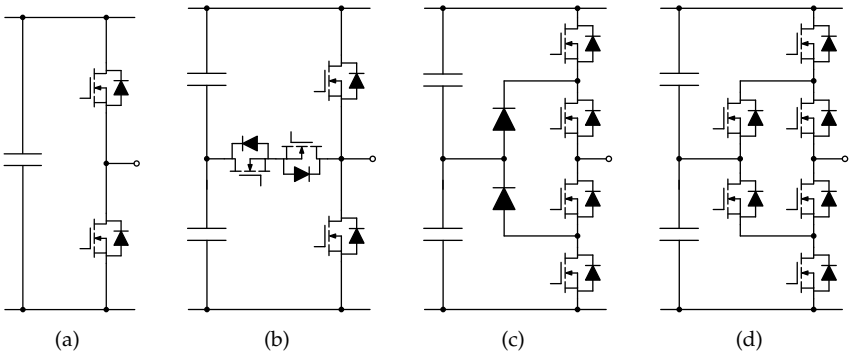


Fig. 1.3: Prevalent 3-phase PV inverter topologies for 1.5-kV dc-link voltage. (a) Two-level half-bridge (2L-HB). (b) Three-level T-type neutral-point-clamped (3L T-type NPC) [37]. (c) Three-level diode neutral-point-clamped (3L-DNPC) [38]. (d) Three-level active neutral-point-clamped (3L-ANPC) [39].

has not been addressed in the design and lifespan-expectation of SiC-based power converters.

1.1.1 Topologies for PV Inverter with a 1.5-kV DC-Link

As the PV panels with 1.5-kV insulation capability have been commercialized in recent years, one of the most significant trends in emerging commercial- and utility-scale PV plants is the extension of the maximum dc voltage to 1.5 kV [33]. It is reported in [34] that the increase of dc voltage to 1.5 kV leads to a reduction of 15–85% in conductor mass, as well as a reduction of 25–60% in combiner boxes, depending on PV array sizes and configurations. It is worth to note that the maximum input voltage of the PV inverter can reach 1.5 kV, which matches the maximum open-circuit voltage of the PV array. During operation, the maximum-power-point (MPP) voltage can operate from 880 V to 1450 V or 850 V to 1350 V, as defined by SMA Solar Technology AG [35] and ABB AG [36], respectively.

The prevalent PV inverter topologies are exhibited in Fig. 1.3. The two-level half-bridge [2L-HB, see Fig. 1.3(a)] and three-level T-type neutral-point clamped [3L T-type NPC, see Fig. 1.3(b)] topologies may only be applicable in 1-kV PV systems. Compared with the 2L-HB, the 3L architectures bring several merits. The volume and and cost of the ac-side filter can be designed to be much lower [40], and the system leakage current can be significantly reduced due to a lower dv/dt [40]. However, as each of the main switches in 2L-HB and 3L T-type NPC topologies bears the whole dc-link voltage during blocking state, the 1.5-kV inverter based on 2L-HB and 3L T-type NPC topologies can not guarantee a sufficient voltage margin for commercial 1.7-

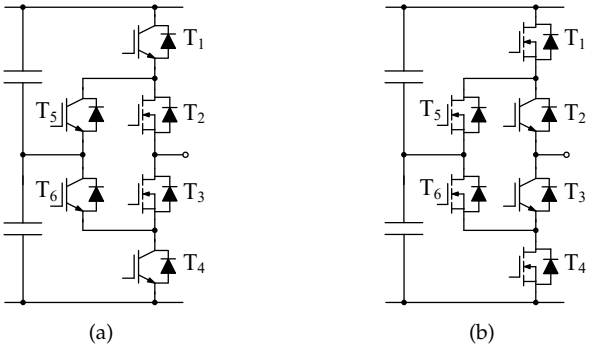


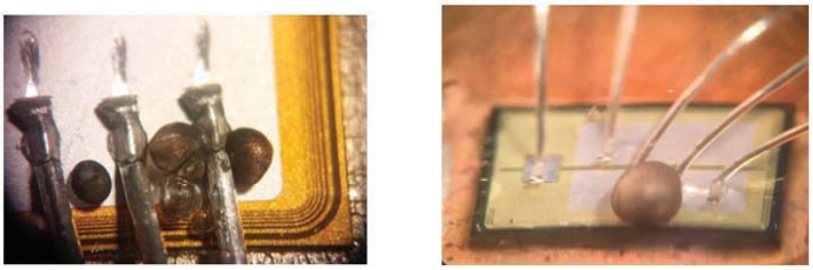
Fig. 1.4: Two types of hybrid 3L-ANPC inverter architectures using both Si IGBTs and SiC MOSFETs. (a) Type I: inner mode. (b) Type II: outer mode.

kV power devices.

On the other hand, the three-level diode neutral-point-clamped [3L-DNPC, see Fig. 1.3(c)] and three-level active neutral-point-clamped [3L-ANPC, see Fig. 1.3(d)] topologies can assure a sufficient voltage margin with commercial 1.2-kV Si IGBTs and SiC MOSFETs, making them competently qualified for PV inverters with the 1.5-kV dc-link voltage. Compared with the 3L-DNPC, the 3L-ANPC inverter is able to re-distribute the power-loss and heat stresses among different semiconductor devices [39].

Over the recent years, the applications of SiC MOSFETs in 3L-ANPC inverters are presented in the literature with enhancement in efficiency and power-density [4, 41–44]. Except for fully utilizing SiC MOSFETs in a 3L-ANPC inverter phase-leg [as exhibited in Fig. 1.3(d)], implementing two types of hybrid 3L-ANPC architectures with both SiC MOSFETs and Si IGBTs [as demonstrated in Figs. 1.4(a) and 1.4(b)] reduces the cost while still maintains the superiority brought by SiC MOSFETs [4, 42–44]. In specific, the type I shown in Fig. 1.4(a) only implements inner switches T_2 and T_3 as SiC MOSFETs (high-frequency switching), while other switches are implemented using Si IGBTs (line-frequency switching). The type II [see Fig. 1.4(b)], on the other hand, uses SiC MOSFET with high-frequency-switching for devices T_1, T_4, T_5, and T_6, while the inner switches T_2 and T_3 are implemented using Si IGBTs with line-frequency-switching.

Considering the above-mentioned merits of SiC-based 3L-ANPC inverters in 1.5-kV PV applications, the world's leading PV-system manufacturer, SMA Solar Technology AG, has successfully launched a 1.5-kV, 150-kW PV inverter based on the hybrid 3L-ANPC topology shown in Fig. 1.4(a) [45]. It is expected that using the 3L-ANPC topology with SiC MOSFETs will be a significant trend in future 1.5-kV PV systems.



(a) (b)

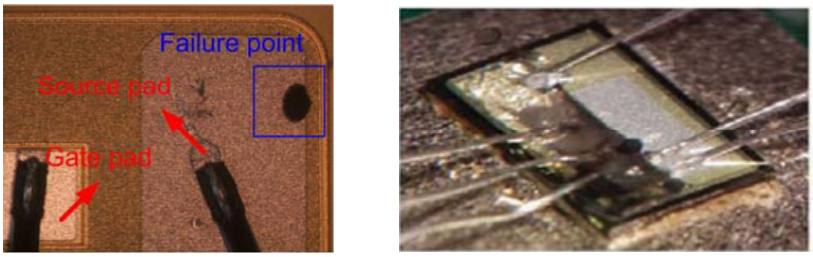
Fig. 1.5: Over-voltage failure samples of SiC MOSFET modules [20]. (a) Sample I. (b) Sample II.

1.1.2 Switching Behaviors of SiC MOSFETs in 1.5-kV 3L-ANPC Inverter

Although the SiC-based 3L-ANPC inverter exhibits a significant application potential in 1.5-kV PV systems, the switching behaviors of SiC MOSFETs in 3L-ANPC inverters still have not been fully revealed. The fast-switching SiC MOSFETs may suffer unfavorable switching behaviors in 3L-ANPC inverters, e.g., critical switching oscillations, voltage overshoots, and excessive switching losses, which may lead to an over-voltage breakdown of the SiC power device (by thermal runaway or partial discharge). Two failure samples of SiC MOSFET caused by transient over-voltage are exhibited in Fig. 1.5.

Differing from the switching characteristics in discrete-devices and 2L-HB configurations [46–53], the switching characteristics of SiC MOSFETs in 3L-ANPC inverters are more sophisticated, as they can be significantly affected by multiple commutation modes and line-frequency devices [31, 54, 55]. The three representative commutation modes, i.e., the full mode, outer mode, and inner mode, of the 3L-ANPC inverter were studied in [39]. The typical commutation loops and characteristics related with the three commutation types were investigated in [54, 55]. Most recently, the extra junction capacitance and the capacitive loop induced by low-frequency switches are illustrated in [31]. Owing to various commutation loops and high slew rates, the fast-switching of SiC MOSFET in 3L-ANPC inverters engenders unfavorable switching behaviors, e.g., critical voltage overshoots, excessive switching losses, and multiple switching-oscillation components.

In [30], the over-voltage issue of SiC MOSFET in 3L-ANPC inverters was introduced for the outer and inner modes. A model for the over-voltage issue was proposed in [32], which only studies the outer-mode mechanism. Despite the studies mentioned above, the comprehensive understanding regarding the switching oscillations with multiple frequency components closely related to the SiC-based 3L-ANPC inverter remains unexplained. A com-



(a) (b)

Fig. 1.6: Failure samples of SiC MOSFET modules caused by high temperature. (a) Failure sample under single-event unclamped inductive switching (UIS) [59]. (b) Failure sample under long-term over temperature [20].

prehensive study of the switching behaviors (e.g., overshoots, oscillations, and switching losses) with these three typical ANPC commutation modes is highly demanded since the performance of the switching is dependent on commutation modes.

1.1.3 Thermal Characterization of SiC MOSFET Module

As discussed in Table 1.1, the mean junction temperature T_{jm} and junction-temperature swing ΔT_j are two of the most significant stressors to a variety of critical failure mechanisms of SiC MOSFET [56]. Compared with the Si IGBT, the SiC MOSFET can be more easily damaged by a single over-temperature event, e.g., the short-circuit and unclamped inductive switching (UIS), owing to its GOX weakness and compact die size. On the other hand, the solder-joint degradation of the SiC die can be two times faster than the Si IGBT during the long-term thermal cycling process, due to the high stiffness of SiC [16–19]. Moreover, other reliability issues, e.g., the time-dependent dielectric breakdown, inter-layer dielectric erosion, and electrode delamination, can be triggered under a long-term high-temperature operating condition [57]. To guarantee the reliability of the SiC MOSFET module during its life-span, a high-precision thermal model and its characterization methodology for the temperature-profile prediction within a wide temperature range are strongly demanded. Thereafter, a reliability investigation methodology shall be used to transfer the temperature data to a variety of reliability characteristics [56, 58].

Nowadays, one of the most general methodologies regarding thermal estimations of power devices is to conduct the circuit-level thermal simulation using these resistor-capacitor (RC) lumped thermal models [60, 61], i.e., the Foster-type and Cauer-type. In specific, the Foster-type RC lumped thermal model [the Foster model, as illustrated in Fig. 1.7(a)] can usually be accessed

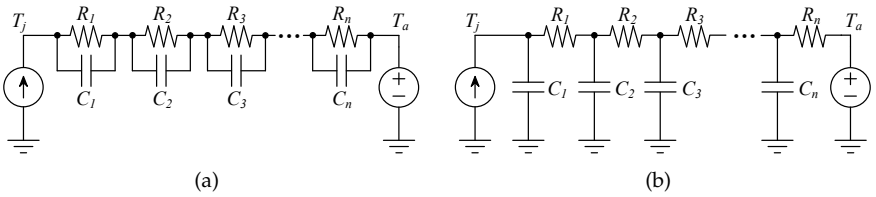


Fig. 1.7: Two types of prevailing RC lumped thermal models. (a) Foster model. (b) Cauer model.

from the datasheet of power semiconductor devices, which are obtained from the transient-thermal-impedance curve characterized by experiments. The Cauer-type thermal model [the Cauer model, as exhibited in Fig. 1.7(b)], on the other hand, can be built based on the knowledge of geometry and material properties of the power semiconductor device [62]. These two types of RC lumped thermal models have found their applications for long-term thermal-profile evaluations of SiC MOSFETs in several works [63–66].

However, the RC lumped thermal models are commonly characterized under a fixed temperature with constant thermal resistance and capacitance values. The precision under high-temperature circumstance is unwarranted. The thermal conductivities and heat capacities of the SiC die and peripheral materials can shift dramatically with local-temperature variations due to free electrons and lattice vibration. To address the aforementioned issue, a temperature-dependent thermal model for the Si IGBT module was proposed in [67]. It was also validated that omitting the temperature effect of Si IGBT's thermal model can lead to significant junction-temperature estimation errors. Nevertheless, the temperature effects of peripheral materials other than the Si IGBT die, especially the ceramic substrate, were not characterized [67]. A SiC MOSFET thermal model having a particular focus on the die area was studied in [68], and the temperature-dependent thermal properties of SiC were considered. Yet, the temperature-dependent thermal performance of the whole power module remains unexplored.

1.1.4 Wear-out of SiC MOSFET Based Inverter

Regarding the long-term power cycling reliability of the SiC device, one of the most crucial failure mechanisms is the solder-joint wear-out. Due to contact of different packaging layers with different coefficients of thermal expansion (CTE), the solder material (e.g., Sn-Ag-Cu as die-solder or baseplate-solder) can suffer from dramatic thermo-mechanical stresses during the long-term power cycling. As the Young's modulus of SiC is two times greater than that of Si (meaning that SiC is two times stiffer than Si), the solder layer beneath the SiC die will degrade two times faster than that of Si. As it is

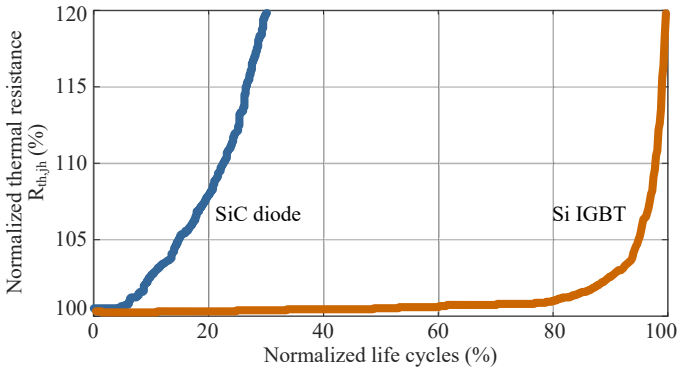


Fig. 1.8: Comparison of normalized thermal resistance degradation for SiC Schottky barrier diode (SBD) and Si IGBT measured during the power cycling test. [16]

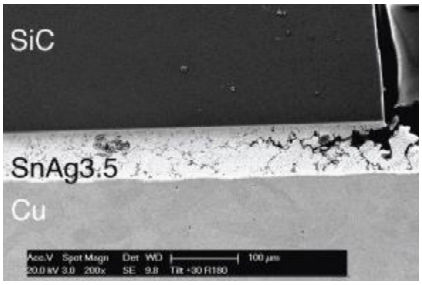


Fig. 1.9: Scanning electron microscope image of a cracked SiC die-solder in cross-section view [19].

demonstrated in Fig. 1.8, the power cycling lifetime of a SiC diode is only 1/3 of Si IGBT, assuming the end-of-life criteria to be a 20 % increase of the thermal resistance $R_{th,jh}$ [16]. A scanning electron microscope (SEM) image shows that the solder layer beneath a SiC die to crack from the die edge, where the strain energy during power cycling is concentrated [19].

Although the novel Ag sintering technology can solidify the die-attach reliability in SiC-based power modules, its application in practical power electronic converters is still constrained by high costs. For some cost-sensitive applications, e.g., PV inverters, the SiC MOSFET modules with standard solder materials (e.g., the Sn-Ag-Cu) still dominate the SiC market. However, this lifetime deduction caused by the solder degradation has not been addressed in the lifespan-evaluation of SiC-based power converters [65, 69]. Moreover, a useful power cycling lifetime model of the SiC module with standard soldering technology is still under research.

1.2 Project Motivation

1.2.1 Research Questions

As discussed in previous sub-chapters, the broad application of the SiC power device in 1.5-kV PV inverter systems is still restricted by its reliability uncertainties in different aspects (as listed in Table 1.1). Although the manufacturers have been working promptly to enhance the robustness of their SiC power devices, efforts from the application perspective are even more demanding to realize more reliable SiC-based power electronic converters. Concerning this point, the Ph.D. project works with the reliability challenges from a power electronic system's viewpoint.

Therefore, the overall research question for this Ph.D. project is defined as follows:

- **Q0:** How to ensure twenty years of a useful lifetime for SiC-based 1.5-kV PV inverters?

To answer this overall research question, we need to be aware that the SiC-based 1.5-kV PV inverter can face numerous reliability challenges during its whole lifespan. Three of the most critical ones are switching-behavior uncertainty, thermal uncertainty, and wear-out uncertainty, as discussed in Chapter 1.1. Based on the justifications mentioned above, the following research questions are considered in this Ph.D. project:

- **Q1:** Will the 3L-ANPC topology bring reliability challenges to SiC MOSFETs in terms of their potential unfavorable switching behaviors?
- **Q2:** How to improve the power-stage design to address the reliability challenge brought by switching behaviors?
- **Q3:** How to characterize the thermal behaviors of SiC power modules with an improved accuracy level throughout the full temperature range?
- **Q4:** Is there any power-cycling lifetime model available for SiC MOSFET modules with standard the soldering and wire-bonding technology?
- **Q5:** What amount of lifetime expectation will be concluded if a two-times faster solder-layer degradation process is considered for SiC MOSFET modules.

1.2.2 Research Objectives

Motivated by the research questions mentioned above, this Ph.D. project aims to achieve the following research objectives:

- **O1 – Switching-behavior investigation:**
  To answer Q1 and Q2, a comprehensive investigation of switching behaviors for SiC MOSFETs in 3L-ANPC topologies shall be conducted in this dissertation. The reliability-critical components need to be found based on a parasitic model of the 3L-ANPC phase-leg. The switching behaviors of SiC MOSFETs need also to be tested under a 1.5-kV PV inverter prototype.

- **O2 – Temperature-dependent thermal model with computational efficiency:**
  To answer Q3, a temperature-dependent thermal model shall be developed in this Ph.D. project, which should consider the temperature effect and provide an enhanced accuracy level. Meanwhile, a high computational efficiency should be guaranteed to make the proposed thermal model suitable for long-term reliability assessment.

- **O3 – Wear-out reliability assessment considering die-solder wear-out:**
  To answer Q4 and Q5, a power cycling lifetime model considering die-solder degradation effects of SiC MOSFET need to be identified. Then a mission-profile-based reliability investigation should be conducted to assess the wear-out reliability of SiC-based 1.5-kV PV inverter. The wear-out failure probability of different SiC MOSFETs under three typical 3L-ANPC commutation modes are to be found and concluded accordingly.

These research objectives are achieved in the same order throughout this dissertation, based on the published journal and conference papers. The published papers are provided in the appendix of the dissertation.

1.3 Project Limitations

Several scientific limitations of this Ph.D. project are listed as follows:

- **L1:** The overall reliability performance and assessment can be more complicated with multiple failure mechanisms and stressors involved (see Table 1.1). This Ph.D. project covers the packaging-related wear-out failure mechanisms, while other reliability-limiting factors, e.g., the humidity and cosmic ray, are not considered.

- **L2:** The switching-behaviors of SiC MOSFETs are studied based on a 3L-ANPC inverter demonstrator, where the switching characteristics are specified. Different values of switching metrics, e.g., amplitudes of overshoots and oscillation frequencies, might be witnessed if a re-designed 3L-ANPC inverter prototype is tested.
- **L3:** To build the proposed temperature-dependent Cauer-type thermal model, the knowledge of temperature-dependent thermal property and power-module geometry is mandatory.
- **L4:** The lifetime model extrapolated in this Ph.D. project can only predict the lifetime of the SiC MOSFET module with conventional interconnection technologies, i.e., using the Sn-based solder and Al bond wires.
- **L5:** The reliability assessment of SiC MOSFETs is conducted based on the mission profile sampled in one specific location, i.e., Arizona, USA. The failure probability figures may not be applicable for SiC-based 3L-ANPC inverters operating at other installation sites.

1.4 Thesis Outline

This Ph.D. dissertation consists of two parts: **Report** and **Selected Publications** (Journals: J, Conference: C), as illustrated in Fig. 1.10. The **Report** summarizes the research outcomes during the Ph.D. project, which is based on both journal and conference publications presented in the **Selected Publications** part. The **Report** is divided into five chapters, and the research objectives O1, O2, and O3 are discussed in Chapters 2, 3, and 4, respectively. A brief introduction of chapter contents and their corresponding publications are summarized as follows:

- **Chapter 1 – Introduction**
  Chapter 1 reviews the background of the SiC device and its reliability challenges in several aspects for the 1.5-kV PV application. Then, the motivations (i.e., research questions and objectives) and limitations of this Ph.D. project are derived in Chapter 1.
- **Chapter 2 – Switching-behavior investigation of SiC MOSFETs in 1.5-kV 3L-ANPC inverter**
  Aiming to identify and address the reliability challenges caused by unfavorable switching behaviors, a comprehensive investigation of switching performance for SiC MOSFET in 3L-ANPC inverters is conducted in Chapter 2. It is figured out that the inner SiC devices can suffer severe voltage overshoots, and multiple switching-oscillation components

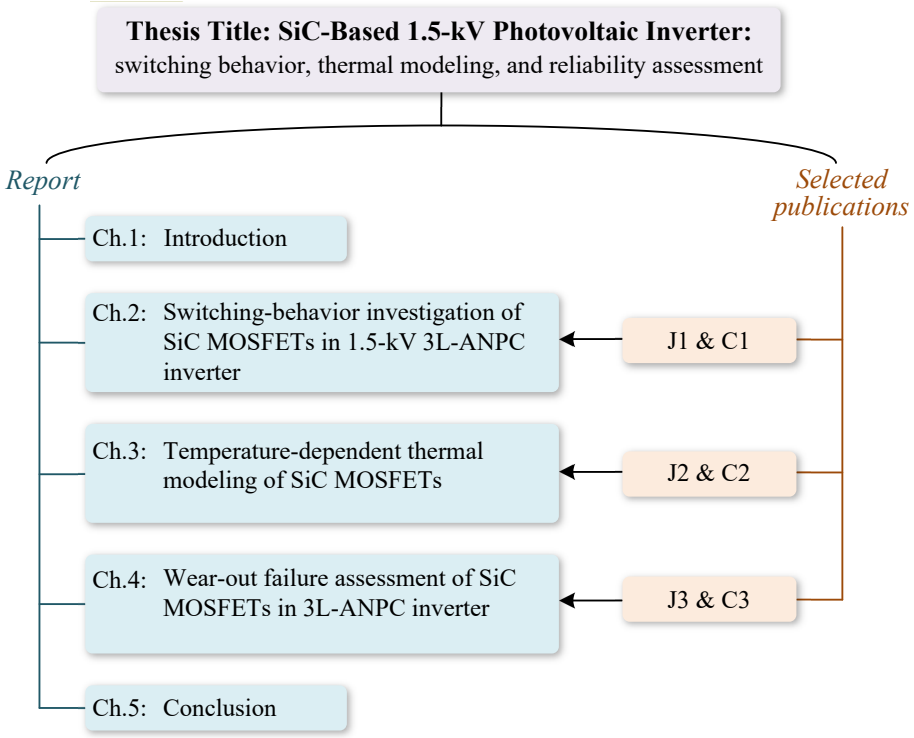


Fig. 1.10: The outline of this Ph.D. thesis, and the relationship between the **Report** and **Selected Publications**. J: journal, C: conference.

are induced due to the 3L-ANPC topology. Then, the critical parasitic components are identified to achieve reliability improvements in SiC-based 1.5-kV 3L-ANPC inverters.
Based on publications: J1, C1

- **Chapter 3 – Temperature-dependent thermal modeling of SiC MOSFET**
  This chapter focuses on improving the precision of the SiC MOSFET thermal model under the full temperature range. A temperature-dependent Cauer-type thermal model and its FEM based modeling methodology are proposed in Chapter 3. Moreover, a temperature-sensitive electrical parameter (TSEP) based transient-thermal-impedance characterization method is introduced to validate the proposed thermal model under the full temperature range of a SiC MOSFET module.
  Based on publications: J2, C2

- **Chapter 4 – Wear-out failure assessment of SiC MOSFETs in 3L-**

ANPC inverter
In Chapter 4, a die-solder lifetime model for the SiC MOSFET module is extrapolated. A mission-profile-based wear-out assessment for the SiC-based 1.5-kV 3L-ANPC inverter is conducted based on the electro-thermal model. The wear-out failure probabilities of different SiC MOSFETs are identified accordingly, and the reliability-critical devices under each commutation mode are identified.
Based on publications: J3, C3

- **Chapter 5 – Conclusion**
  The contributions of this Ph.D. project are summarized, and future research perspectives are expected.

1.5 List of Publications

The research dissemination during the Ph.D. study is shown below in the forms of journal papers and conference publications. Parts of them are used in the Ph.D. thesis, i.e., J1, J2, J3, C1, C2, and C3.

Journal Papers:

J1. **M. Chen**, D. Pan, H. Wang, X. Wang, and F. Blaabjerg, "Investigation of Switching Oscillations for Silicon Carbide MOSFETs in Three-Level Active Neutral-Point-Clamped Inverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. PP, no. 99, pp. 1-15, 2020, Early Access.

J2. **M. Chen**, H. Wang, D. Pan, X. Wang, and F. Blaabjerg, "Thermal Characterization of Silicon Carbide MOSFET Module Suitable for High-Temperature Computationally-Efficient Thermal-Profile Prediction," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. PP, no. 99, pp. 1-12, 2020, Early Access.

J3. **M. Chen**, Z. Shen, H. Wang, X. Wang, and F. Blaabjerg, "Reliability Assessment of SiC MOSFETs in Three-Level Active Neutral-Point-Clamped Inverters Considering Die-Solder Degradation," *IEEE Trans. Power Electron.*, 2020, Status: to be Submitted.

Conference Papers:

C1. **M. Chen**, D. Pan, H. Wang, X. Wang, F. Blaabjerg, and W. Wang, "Switching Characterization of SiC MOSFETs in Three-Level Active Neutral-Point-Clamped Inverter Application," in *Proc. 2019 10th Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, May 2019, pp. 1793-1799.

C2. **M. Chen**, H. Wang, F. Blaabjerg, X. Wang, and D. Pan, "A Temperature-Dependent Thermal Model of Silicon Carbide MOSFET Module for Long-Term Reliability Assessment," in *Proc. 2018 IEEE 4th Southern Power Electronics Conference (SPEC)*, Dec. 2018, pp. 1-7. (Best Paper Award)

C3. **M. Chen**, T. Zhu, D. Pan, H. Wang, X. Wang, and F. Blaabjerg, "Loss Analysis of SiC-Based Three-Level Active Neutral-Point-Clamped Inverters under Different Modulation Schemes," in *Proc. 2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, Status: In Press.

- **M. Chen**, H. Wang, H. Wang, F. Blaabjerg, X. Wang, and D. Pan, "Reliability Assessment of Hybrid Capacitor Bank Using Electrolytic- and Film-Capacitors in Three-Level Neutral-Point-Clamped Inverters," in *Proc. 2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2019, pp. 2826-2832.
- D. Pan, **M. Chen**, X. Wang, H. Wang, F. Blaabjerg, and W. Wang, "EMI Modeling of Three-Level Active Neutral-Point-Clamped SiC Inverter Under Different Modulation Schemes," in *Proc. 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, Busan, Korea (South), 2019, pp. 1-6.
- D. Pan, **M. Chen**, X. Wang, H. Wang, F. Blaabjerg, and W. Wang, "Precise Inductor Current Ripple Distribution of Three-Level Active Neutral-Point-Clamped Inverter," in *Proc. 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, Busan, Korea (South), 2019, pp. 1952-1959.

Chapter 2

Switching-Behavior Investigation of SiC MOSFETs in 1.5-kV 3L-ANPC Inverter

2.1 Brief Introduction

As discussed in Chapter 1.1.1, the 3L-ANPC topology exhibits a superior application potential in 1.5-kV PV systems compared to its counterparts, as a sufficient voltage margin and active loss and thermal distribution can be realized. Considering the merits of applying the 3L-ANPC topology and SiC devices, it is expected that using 3L-ANPC topology with SiC MOSFETs will be a significant trend in future 1.5-kV PV systems [45]. However, fast-switching SiC MOSFETs in 3L-ANPC inverters can induce unfavorable switching behaviors, e.g., critical switching oscillations, voltage overshoots, and excessive switching losses, which engenders reliability challenges (i.e., over-voltage breakdown and partial discharge) to the SiC-based 3L-ANPC inverters.

Compared with the switching characteristics of SiC MOSFETs in discrete or half-bridge configurations [46–53], the switching behavior of SiC MOSFET in the 3L-ANPC inverter can be much more complicated, as line-frequency devices can induce a secondary switching loop. Furthermore, the 3L-ANPC inverter features three representative commutation types, i.e., the full mode, outer mode, and inner mode, and each mode exhibits distinguished switching behavior [**J1**].

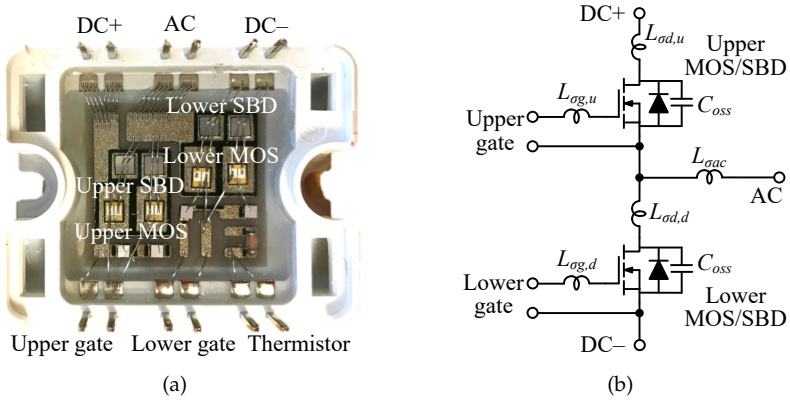


Fig. 2.1: SiC MOSFET module APTMC120AM55CT1AG (made by Microsemi). (a) Photograph from top-side. (b) Circuit diagram. Source: **[J1]**.

Considering the aforementioned reliability challenges in terms of unfavorable switching behaviors, this chapter presents a comprehensive study of the switching characteristics of SiC MOSFETs in 1.5-kV 3L-ANPC inverters under the three representative commutation modes. The analyses are conducted based on a parasitic model extracted from finite-element-method (FEM) simulations. The theoretical findings are validated experimentally through double-pulse test (DPT) results.

2.2 Parasitic Modeling of SiC-based 3L-ANPC Phase-Leg

2.2.1 Half-bridge SiC MOSFET Module

The half-bridge SiC MOSFET module (APTMC120A-M55CT1AG made by Microsemi) is used as a forming element of the 3L-ANPC phase-leg. The device is rated at 1200 V and 42 A specified at the case temperature of 80 °C [70]. The top-side image and circuit diagram are depicted in Figs. 2.1(a) and 2.1(b), respectively. It is noted in Fig. 2.1(a) that two pairs of SiC MOSFET dies as well as their anti-parallel Schottky barrier diode (SBD) dies are packed in the half-bridge module, as noted to be the upper and lower MOS/SBDs in Fig. 2.1(b).

To connect SiC dies with module's electrical terminals, copper traces and bond wires are used in the module housing. This unavoidably introduces parasitic inductance and affects the commutation behaviors. Then, these parasitic-inductance components induced by copper traces and bond wires

Table 2.1: Values of parasitic components of the SiC MOSFET module (extracted at 1 MHz). Source: **[J1]**.

Category		Symbol	Inductance (nH)	Resistance (mΩ)
AC terminal		$L_{\sigma ac}$	6.0	1.0
Upper device	gate	$L_{\sigma g,u}$	9.4	6.5
	drain+source	$L_{\sigma d,u}$	10.0	3.7
Lower device	gate	$L_{\sigma g,d}$	12.0	8.7
	drain+source	$L_{\sigma d,d}$	12.9	3.8
PCB trace		$L_{\sigma clp}$	5.2	1.0
		$L_{\sigma inv}$	34.1	5.6
Busbar		$L_{\sigma bus}$	3.6	—

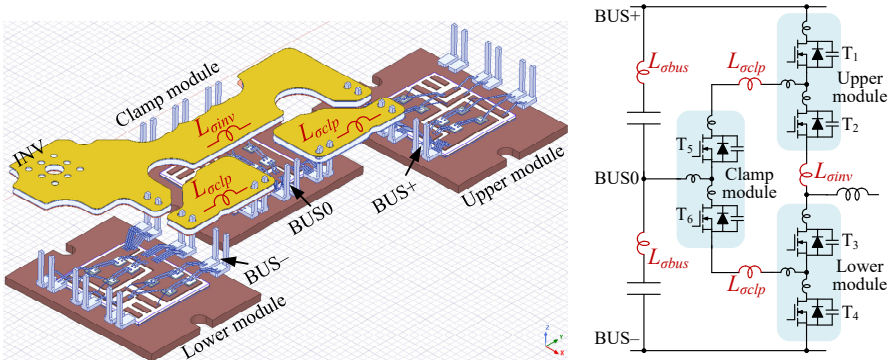
are extracted using finite-element method (FEM) simulations (ANSYS/Q3D), as given in Fig. 2.1(b). The components $L_{\sigma d,x}$ and $L_{\sigma g,x}$ ($x = u$ or d) represent the parasitic inductance located at the drain and gate terminals of the SiC MOSFET die, respectively. Moreover, $L_{\sigma ac}$ is the parasitic inductance contributed by the module's AC terminal. These inductance values and their related series resistances are summarized in Table 2.1, and it can be seen that their values can vary (from 6.0 nH to 12.9 nH) due to geometry variations.

2.2.2 3L-ANPC Phase-Leg

Utilizing the aforementioned half-bridge SiC MOSFET module, a 3L-ANPC phase-leg is built, as illustrated in Fig. 2.2(a). Three half-bridge modules are used, which are denoted as the upper module, clamp module, and lower module. A four-layer PCB busbar is implemented to interconnect the three SiC MOSFET modules, and the parasitic circuit diagram demonstrating the layout is exhibited in Fig. 2.2(b). Accordingly, the 3L-ANPC phase-leg can withstand a dc-link voltage of 1.5 kV (with a sufficient voltage margin) using commercial 1.2-kV SiC MOSFETs.

Nevertheless, the PCB routing also brings excessive parasitic inductances to the ANPC phase-leg. More specifically, the components $L_{\sigma clp}$ and $L_{\sigma inv}$ denote the PCB inductance induced by the clamping branch and inversion branch, respectively, as they are marked in both Figs. 2.2(a) and 2.2(b). FEM simulations are also performed on the PCB busbar to extract the values of $L_{\sigma clp}$ and $L_{\sigma inv}$, which are also exhibited in Table 2.1. It can be seen that the clamping branch features a low inductance value ($L_{\sigma clp}$ = 5.2 nH). In contrast, the inversion branch features a relatively significant inductance value ($L_{\sigma inv}$ = 34.1 nH) due to its longer geometry [as shown in Fig. 2.2(a)].

Moreover, another part of the parasitic inductance comes from the 1.5-kV capacitor bank. Both the capacitor's equivalent-series-inductance (ESL) and



(a) (b)

Fig. 2.2: Layout and circuit diagram of the 3L-ANPC phase-leg. (a) Physical layout from top-side. (b) Simplified parasitic model–circuit diagram. Source: **[J1]**.

Table 2.2: Switching states of the 3L-ANPC inverter [39].

States	T_1	T_2	T_3	T_4	T_5	T_6
–	0	0	1	1	1	0
0L2	0	0	1	0	0	1
0L1	1	0	1	0	0	1
0F	0	1	1	0	1	1
0U1	0	1	0	1	1	0
0U2	0	1	0	0	1	0
+	1	1	0	0	0	1

the routing inductance of busbar should be considered in the loop. Hence, the PCB busbar is specifically designed to minimize the routing inductance [71]. To simplify, the capacitor's ESL and the busbar's routing inductance are unified as $L_{\sigma bus}$ in Fig. 2.2(b), which is estimated as being 3.6 nH. Having the knowledge of parasitic components in the 3L-ANPC phase-leg, the three commutation modes and their corresponding switching circuits will be analyzed in the following sub-chapters.

2.3 Analyses of Commutation Modes

2.3.1 Switching States

The switching states will first be demonstrated before introducing the commutation modes of the 3L-ANPC inverter, as summarized in Table 2.2.

For the "–" state, switches T_3 and T_4 conduct the phase current to the neg-

ative bus-rail (i.e., BUS–). Meantime, the switch T_5 also conducts to balance the voltage sharing between switches T_1 and T_2. Similarly, switches T_1, T_2, and T_6 conduct during the "+" state to realize the positive bus-rail output. Moreover, by turning on switches T_3 and T_6, the phase current can be conducted to the neutral point in both directions through the lower neutral path. The switch T_1 can be in either ON or OFF state, leading to lower-clamping states "0L1" or "0L2", respectively. Analogously, the phase current can also be conducted via the upper neutral-path by turning on switches T_2 and T_5 simultaneously. The switch T_4 can be in either ON or OFF state, leading to dual upper-clamping states, "0U1" or "0U2", respectively. Alternatively, the phase current can be conducted via both the upper and lower neutral paths by turning on switches T_2, T_3, T_5, and T_6 simultaneously, which is known as the full state "0F".

Accordingly, different commutation options can take place between a single active state (either "+" or "–") and one clamping state ("0L1", "0L2", "0U1", "0U2", or "0F"). The three representative commutation modes (i.e., the full mode, outer mode, and inner mode) of the 3L-ANPC phase-leg will be analyzed as follows.

2.3.2 Full-Mode Commutation

The full-mode commutation contains commutation transitions "– $\leftrightarrow$ 0F" and "+ $\leftrightarrow$ 0F" for the negative and positive ac line-cycles, respectively. In short, the commutation transition for the negative line-cycle (i.e., "– $\leftrightarrow$ 0F") will be analyzed in this work. Figs. 2.3(a) and 2.3(b) present the gate signals and circuit diagrams during the full-mode commutation, respectively. During the negative line-cycle (i.e., $V_{an} < 0$), switch T_4 is modulated to be sinusoidal, while switches T_2 and T_6 are switched complementarily. Accordingly, the phase current will commutate between the active phase-arm and both the upper and lower neutral paths, forming dual switching loops nominated as the main loops I and II in Fig. 2.3(b) **[J1]**.

To reveal the commutation mechanisms, the equivalent switching circuits during full mode are investigated. Figs. 2.4(a) and 2.4(b) demonstrate the equivalent switching circuits during "0F $\rightarrow$ –" and "– $\rightarrow$ 0F" (i.e., the turn-on and turn-off transients of T_4), respectively. The components L_{lpx} and R_{lpx} represent the parasitic inductance and resistance of switching loops I and II (x = 1 and 2), respectively. The components L_{cm} and R_{cm} denote the common loop inductance and resistance enclosed by loops I and II. Besides, R_{on} and $C_{oss,Tx}$ are the on-state resistance and output capacitance of SiC MOSFETs, respectively. The values of these parasitic components are summarized in Table 2.3, which are obtained based on the parasitic model.

During the transition "0F $\rightarrow$ –" (i.e., the turn-on transient of T_4), the output capacitance of T_6 and T_2 (i.e., $C_{oss,T6}$ and $C_{oss,T2}$) are charged via main

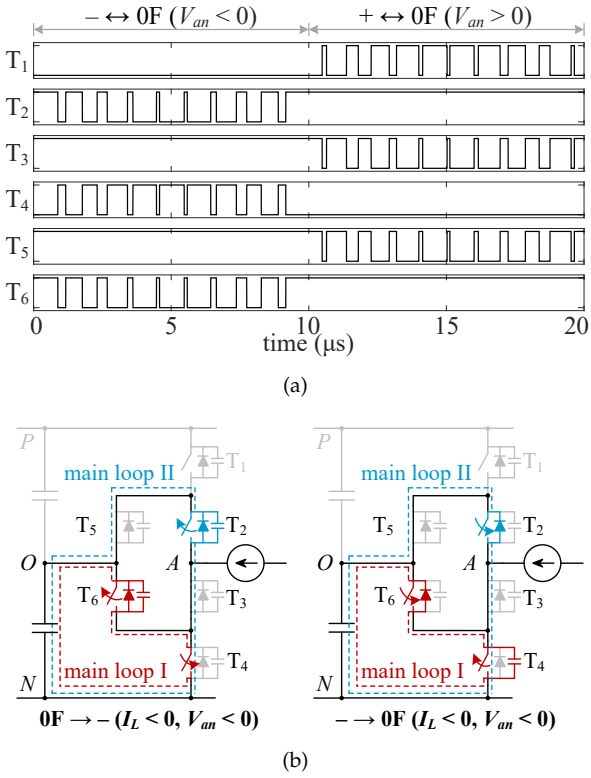


Fig. 2.3: Gating voltages and commutation diagrams during the full mode. (a) Gating voltages. (b) Commutation diagrams for transitions "0F → –" and "– → 0F". Source: **[J1]**.

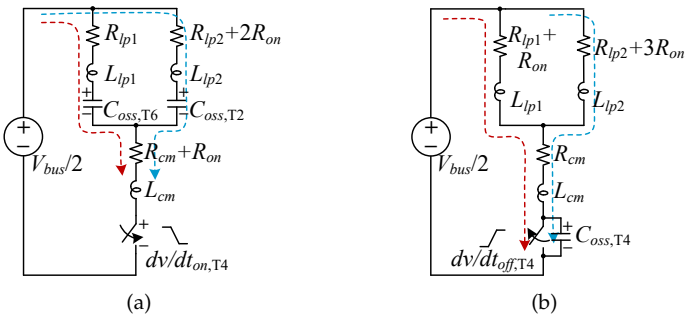


Fig. 2.4: Full-mode equivalent switching circuits. (a) Transition "0F → –". (b) Transition "– → 0F". Source: **[J1]**.

loops I and II, respectively. Multi-frequency switching oscillations will exist for the transition "0F → –". Moreover, switch T_2 is expected to experi-

Table 2.3: Switching-loop parasitic parameters. Source: [**J1**].

Symbol	Inductance (nH)	Resistance (mΩ)	Capacitance (pF)
L_{lp1}, R_{lp1}	24.1	5.8	–
L_{lp2}, R_{lp2}	78.2	18.8	–
L_{lp3}, R_{lp3}	40.8	10.4	–
L_{cm}, R_{cm}	22.5	4.8	–
R_{on}	–	49	–
$C_{oss,Tx}$ (x = 1–6)	–	–	270 @ 500 V

ence a more significant voltage overshoot than T_6 as L_{lp2} is greater than L_{lp1}. Impedance characteristic of the equivalent switching circuit for "0F $\rightarrow$ –" is depicted in Fig. 2.5(a). Dual switching-oscillation components with different frequencies are identified in Fig. 2.5(a) as $f_{osc1}^{0F\rightarrow-}$ = 49.4 MHz and $f_{osc2}^{0F\rightarrow-}$ = 29.4 MHz, which are dominated by loops I and II, respectively. The two oscillation frequencies can also be obtained by letting the imaginary part of the circuit impedance to be zero:

$$f_{osc1,osc2}^{0F\rightarrow-} = \frac{1}{2\pi}\cdot\sqrt{\frac{L_{lp1}+L_{lp2}+2L_{cm}\pm\sqrt{\left(L_{lp1}-L_{lp2}\right)^2+2{L_{cm}}^2}}{2C_{oss}\cdot\left(L_{lp1}L_{lp2}+L_{lp1}L_{cm}+L_{lp2}L_{cm}\right)}}. \tag{2.1}$$

During the transition "– $\rightarrow$ 0F" (i.e., when T_4 is switched off), the output capacitance of T_4 is charged by the load current. After T_4's drain-source voltage reaches $V_{bus}/2$, the oscillation is triggered via the conduction path established by loops I and II, as shown in Fig. 2.4(b). It is expected that turning T_4 off will not introduce severe switching-oscillation and voltage-overshoot issues since the total loop inductance is not significant considering the paralleling effect:

$$L_{tot}^{-\rightarrow0F} = \frac{L_{lp1}L_{lp2}}{L_{lp1}+L_{lp2}} + L_{cm} \tag{2.2}$$

where, $L_{tot}^{-\rightarrow0F}$ is the equivalent loop inductance during "0F $\rightarrow$ –", which is estimated to be 40.9 nH. Then, a single switching-oscillation component $f_{osc}^{-\rightarrow0F}$ = 47.9 MHz is identified according to:

$$f_{osc}^{-\rightarrow0F} = \frac{1}{2\pi\cdot\sqrt{L_{tot}^{-\rightarrow0F}\cdot C_{oss}}}. \tag{2.3}$$

This is confirmed by the impedance analysis presented in Fig. 2.5(b).

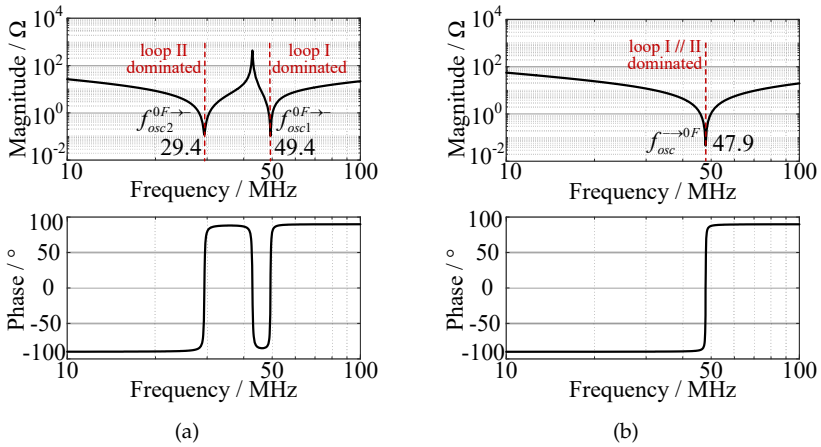


Fig. 2.5: Impedance curves of equivalent switching circuits during the full-mode commutation. (a) Magnitude and phase characteristics for "0F → –". (b) Magnitude and phase characteristics for "– → 0F". Source: **[J1]**.

2.3.3 Outer-Mode Commutation

The outer mode is composed of commutations "– ↔ 0L2" and "+ ↔ 0U2" for the negative and positive line periods, respectively. Figs. 2.6(a) and 2.6(b) illustrate the gate signals and commutation diagrams during the outer mode. During the negative line-cycle (i.e., $V_{an} < 0$), switch T_4 is operated identically with its modulation pattern during the full-mode commutation, while only T_6 is switched complementary. Simultaneously, switch T_5 is modulated identically with T_4 to balance the voltage sharing between T_1 and T_2. Accordingly, the phase current will commutate between the active phase-arm and its neighboring neutral path (e.g., the lower neutral path during $V_{an} < 0$), and the loop I is found to be the major commutation loop **[J1]**. Furthermore, the switching operation of T_5 will charge and discharge the device output capacitance of T_2 and T_1, which leads to double capacitive loops, i.e., the capacitive (capaci.) loop II (or II') and capaci. loop III in Fig. 2.6(b). Even though no actual phase current flows through these two capacitive loops, critical switching oscillations and voltage overshoots may be introduced in outer-mode switching circuits.

Figs. 2.6(a) and 2.6(b) illustrate the equivalent switching circuits of the outer transitions "0L2 → –" and "– → 0L2", respectively. R_{lp3} and L_{lp3} denote the parasitic resistance and inductance of the capacitive loop III, respectively. During the transition "0L2 → –", the output capacitances of $C_{oss,T6}$ and $C_{oss,T2}$ shall be charged via the main loop I and capacitive loop II, respectively. Additionally, the output capacitance of switch T_1 (i.e., $C_{oss,T1}$) is

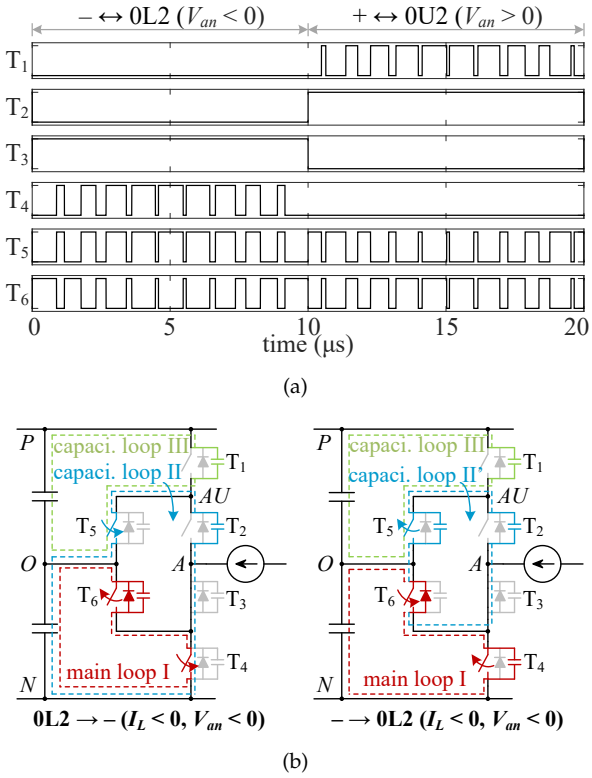


Fig. 2.6: Gating voltages and commutation diagrams during the outer mode. (a) Gating voltages. (b) Commutation diagrams for transitions "0L2 → –" and "– → 0L2". Source: **[J1]**.

also charged through the loop III owing to the conduction of switch T_5. Nevertheless, the capacitive loop III does not alter commutation behaviors of the main switches involved in the main loop I and capaci. loop II. Hence, the switching behavior of outer-mode commutation "0L2 → –" duplicates that of the transition "0F → –", and the dual switching-oscillation components can be obtained by:

$$f_{osc1,osc2}^{0L2\rightarrow-} = f_{osc1,osc2}^{0F\rightarrow-}$$
$$\frac{1}{2\pi}\cdot\sqrt{\frac{L_{lp1}+L_{lp2}+2L_{cm}\pm\sqrt{\left(L_{lp1}-L_{lp2}\right)^2+2L_{cm}{}^2}}{2C_{oss}\cdot\left(L_{lp1}L_{lp2}+L_{lp1}L_{cm}+L_{lp2}L_{cm}\right)}} \tag{2.4}$$

where, $f_{osc1}^{0L2\rightarrow-}$ and $f_{osc2}^{0L2\rightarrow-}$ are calculated to be 29.4 MHz and 49.4 MHz, respectively. This can also be validated through the impedance curve of the equivalent switching circuit exhibited in Fig. 2.8(a).

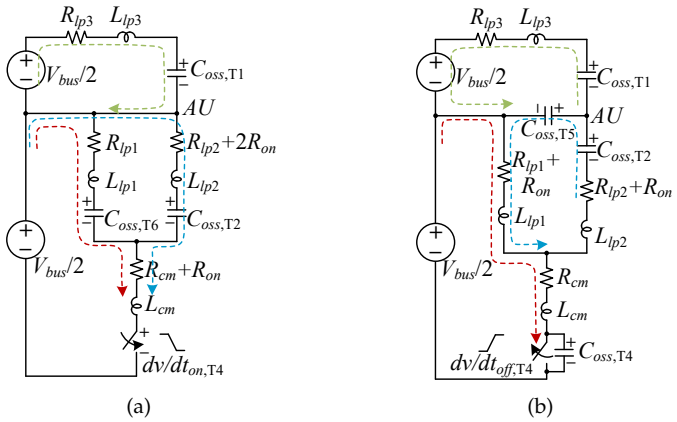


Fig. 2.7: Outer-mode equivalent switching circuits. (a) Transition "0L2 → –". (b) Transition "– → 0L2". Source: **[J1]**.

The switching behavior for the transition "– → 0L2" is more complicated compared to others since the three loops, i.e., the main loop I, capacitive loops II', and III, all take effects. Even though, it is expected that there will not be significant switching oscillations and voltage overshoots on switch T_4, as the main loop I with relatively low inductance is actively involved. Fig. 2.8(b) shows the circuit impedance analysis of the transition "– → 0L2", and dual oscillation components of $f_{osc1}^{-\rightarrow 0L2}$ = 34.3 MHz and $f_{osc2}^{-\rightarrow 0L2}$ = 51.8 MHz can be determined, which can also be obtained from the calculations:

$$f_{osc1,osc2}^{-\rightarrow 0L2} = \frac{1}{2\pi}\cdot\frac{1}{2}\cdot\sqrt{\frac{L_a^{-\rightarrow 0L2} \pm \sqrt{\left(L_a^{-\rightarrow 0L2}\right)^2 - 24\cdot\left(L_b^{-\rightarrow 0L2}\right)^2}}{C_{oss}\cdot\left(L_b^{-\rightarrow 0L2}\right)^2}} \tag{2.5}$$

where

$$L_a^{-\rightarrow 0L2} = 5L_{lp1} + 2L_{lp2} + 3L_{cm} \tag{2.6}$$

$$L_b^{-\rightarrow 0L2} = \sqrt{L_{lp1}L_{lp2} + L_{lp1}L_{cm} + L_{lp2}L_{cm}}\,. \tag{2.7}$$

2.3.4 Inner-Mode Commutation

The inner-mode commutation features commutation transitions "– ↔ 0U1" and "+ ↔ 0L1" for the negative and positive line-cycles, respectively. Figs.

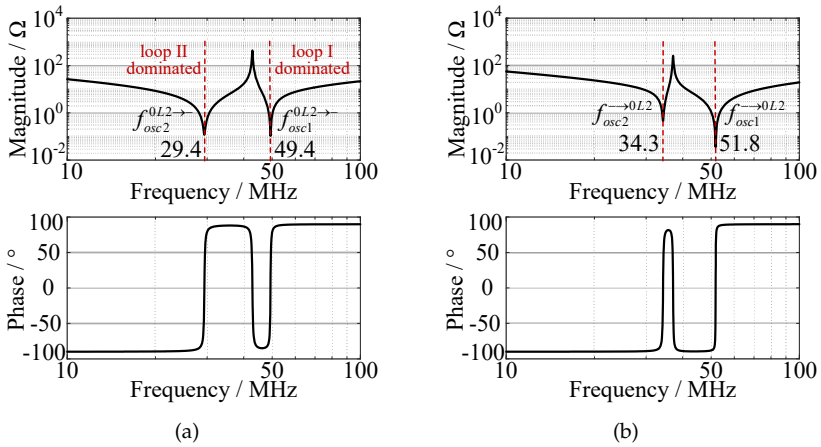


Fig. 2.8: Impedance curves of equivalent switching circuits during the outer-mode commutation. (a) Magnitude and phase characteristics for "0L2 → –". (b) Magnitude and phase characteristics for "– → 0L2". Source: **[J1]**.

2.9(a) and 2.9(b) illustrate the gating voltages and commutation diagrams during the inner mode operation, respectively. It can be seen from Fig. 2.9(a) that only inner switches T_2 and T_3 are modulated to be sinusoidal, while the gating signals of other switches alter each half line-cycle. The phase current switches between T_2 and T_3. Being different from the other two commutation modes, the inner mode involves a single switching loop, i.e., the main loop II shown in Fig. 2.9(b).

The equivalent switching circuits during inner-mode commutations "0U1 → –" and "– → 0U1" are demonstrated in Figs. 2.10(a) and 2.10(b), respectively, which resemble that of the two-level converter [50]. As a single switching loop is featured, only one switching-oscillation component with $f_{osc}^{-\leftrightarrow 0U1}$ = 30.5 MHz can be identified for both inner transitions "0U1 → –" and "– → 0U1" in Fig. 2.11. This oscillation component can be identified by:

$$f_{osc}^{-\leftrightarrow 0U1} = \frac{1}{2\pi \cdot \sqrt{L_{tot}^{-\leftrightarrow 0U1} \cdot C_{oss}}} \tag{2.8}$$

$$L_{tot}^{-\leftrightarrow 0U1} = L_{lp2} + L_{cm} \tag{2.9}$$

where $L_{tot}^{-\leftrightarrow 0U1}$ (= 100.7 nH) denotes the loop inductance in total for the inner-mode commutation. It can be expected that both the inner switches T_2 and T_3 will suffer dramatic switching oscillations and voltage overshoots since its switching loop is relatively long and contains four devices.

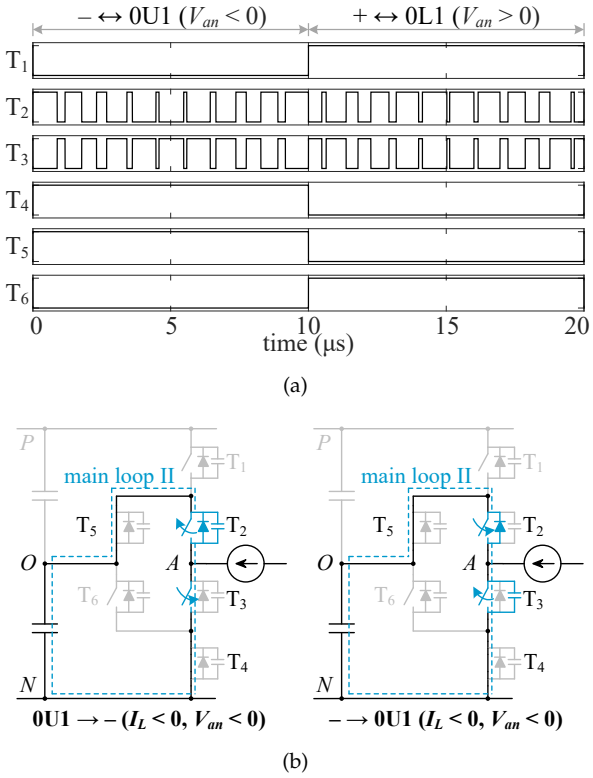


Fig. 2.9: Gating voltages and commutation diagrams during the inner mode. (a) Gating voltages. (b) Commutation diagrams for transitions "0U1 → –" and "– → 0U1". Source: **[J1]**.

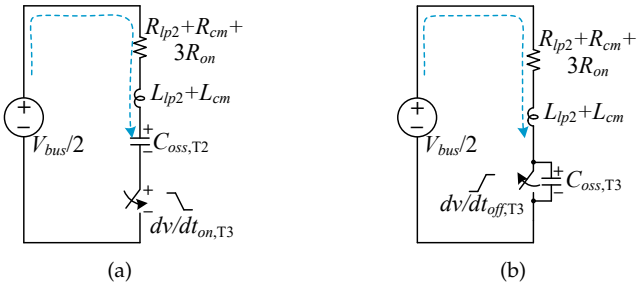


Fig. 2.10: Inner-mode equivalent switching circuits. (a) Transition "0U1 → –". (b) Transition "– → 0U1". Source: **[J1]**.

A summary of the switching-loops involved and their corresponding oscillation frequencies for each commutation mode are presented in Table 2.4.

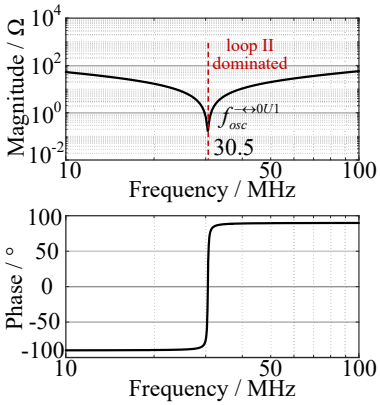


Fig. 2.11: Impedance curves of equivalent switching circuits during the inner-mode commutation. Source: **[J1]**.

Table 2.4: Summary of commutation loops and associated frequencies of oscillations. Source: **[J1]**.

Commutation modes	Loops involved	Symbols	Oscillation frequencies
Full	Main I, II	$f_{osc1}^{0F\rightarrow -}$, $f_{osc2}^{0F\rightarrow -}$	29.4 & 49.4 MHz
		$f_{osc}^{-\rightarrow 0F}$	47.9 MHz
Outer	Main I and capaci. II, III	$f_{osc1}^{0L2\rightarrow -}$, $f_{osc2}^{0L2\rightarrow -}$	29.4 & 49.4 MHz
		$f_{osc1}^{-\rightarrow 0L2}$, $f_{osc2}^{-\rightarrow 0L2}$	34.3 & 51.8 MHz
Inner	Main II	$f_{osc}^{-\leftrightarrow 0U1}$	30.5 MHz

Owing to the multiple loops, the full mode and outer mode are characterized by multiple switching-oscillation components. Nevertheless, the inner mode exhibits only one oscillation component owing to its single switching loop.

2.4 Double-Pulse Test (DPT) and Result Analysis

2.4.1 Test Setup Introduction

To validate the theoretical analyses presented in previous sub-chapters, DPTs are conducted on the 1.5-kV 3L-ANPC inverter prototype using SiC MOSFETs. The power stage is implemented according to the design demonstrated in Chapter 2.2. A top view of the 1.5-kV SiC-based 3L-ANPC inverter prototype is exhibited in Fig. 2.12.

The basic principle of the DPT is referred to [72]. In this work, the basic

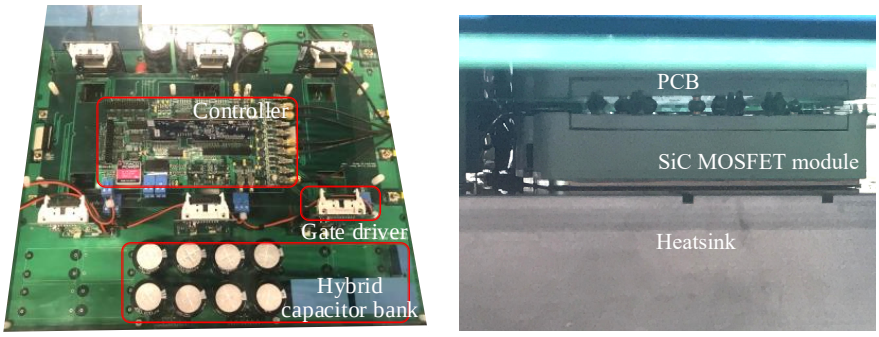


Fig. 2.12: Photograph of the 1.5-kV SiC-based 3L-ANPC inverter protopype. (a) Top-view. (b) Lateral-view of the SiC MOSFET module. Source: **[J1]**.

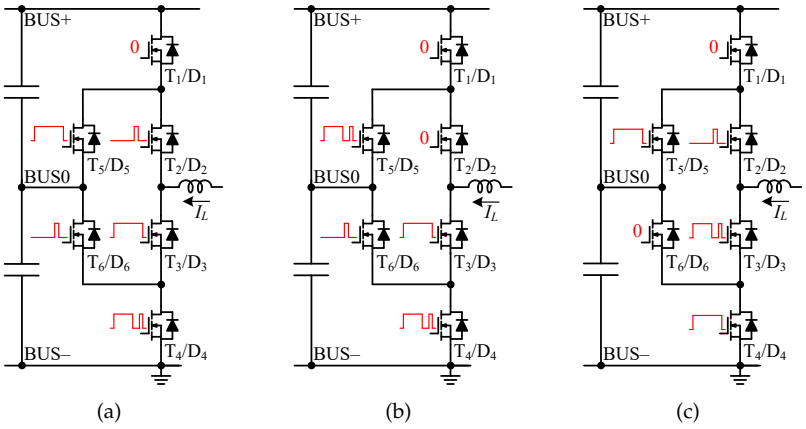


Fig. 2.13: DPT circuits of the 3L-ANPC phase-leg under the three representative commutation modes. (a) The full mode "– ↔ 0F". (b) The outer mode "– ↔ 0L". (c) The inner mode "– ↔ 0U1". I_L: load current. Source: **[J1]**.

DPT principle is extended to 3L-ANPC inverters, where the gating signals are assigned to all six SiC MOSFETs of the 3L-ANPC phase-leg during the DPT. The configurations of gating pulses for full-mode, outer-mode, and inner-mode commutations during the tests are depicted in Figs. 2.13(a), 2.13(b), and 2.13(c), respectively **[J1]**. It is noted that the oscilloscope and the BUS– rail are grounded and commutation for negative cycles, i.e., "– ↔ 0F", "– ↔ 0L", and "– ↔ 0U1" are studied.

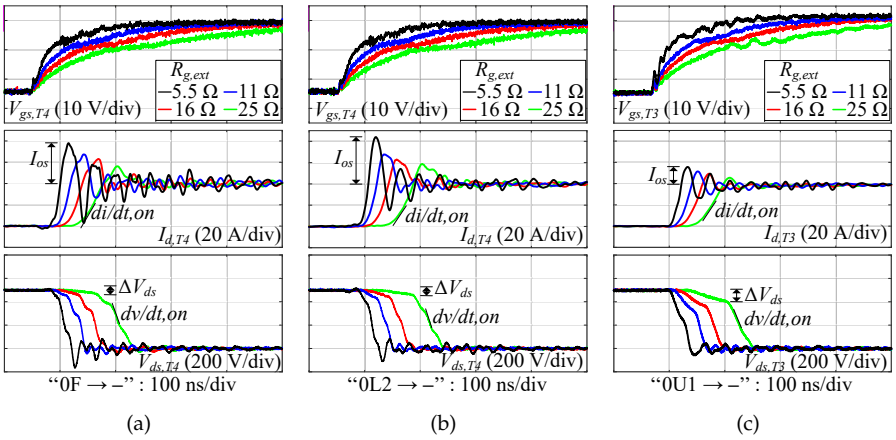


Fig. 2.14: Turn-on waveforms of three commutation modes under the conditions of V_{bus} = 1000 V, I_L = 40 A, $R_{g,ext}$ = 5.5 Ω, 11 Ω, 16 Ω, and 25 Ω, and $C_{gs,ext}$ = 3.3 nF. (a) Full mode turn-on waveforms of $V_{gs,T4}$, $I_{d,T4}$, and $V_{ds,T4}$. (b) Outer mode turn-on waveforms of $V_{gs,T4}$, $I_{d,T4}$, and $V_{ds,T4}$. (c) Inner mode turn-on waveforms of $V_{gs,T3}$, $I_{d,T3}$, and $V_{ds,T3}$. Source: **[J1]**.

2.4.2 Transient Switching Waveforms

The DPT is conducted under the condition of V_{bus} = 1000 V and I_L (load current) = 40 A. It is noted that the testing voltage of V_{bus} = 1000 V is in the reasonable maximum-power-point-voltage range of the 1.5-kV PV inverter [35, 73]. An external gate-source capacitance of $C_{gs,ext}$ = 3.3 nF is installed to mitigate the parasitic turn-on issue [74, 75]. Additionally, different external-gate-resistance values, i.e., $R_{g,ext}$ = 5.5 Ω, 11 Ω, 16 Ω, and 25 Ω, are tested to reveal the commutation behaviors with different commutation speeds. The turn-on and turn-off waveforms of main switches captured during the DPT (i.e., T_4 for the full mode and outer mode, and T_3 for the inner mode) are exhibited in Figs. 2.14 and 2.15, respectively. The electrical waveforms obtained with $R_{g,ext}$ = 5.5 Ω, 11 Ω, 16 Ω, and 25 Ω are plotted as in black, blue, red, and green, respectively **[J1]**.

It can be seen that, during the main-switch turn-on transients, the full-mode and outer-mode commutations exhibit excessive drain-current overshoots compared with the inner mode. This can be induced by their secondary switching loops and the additional output capacitances involved. For the turn-off transients, the inner-mode commutation exhibits a critical switching oscillation on its main switch T_3, which is introduced by its larger loop inductance L_{lp2}. On the other hand, switch T_4 features a mitigated switching oscillation and voltage overshoot during full-mode and outer-mode commutations [see Figs. 2.15(a) and 2.15(b)].

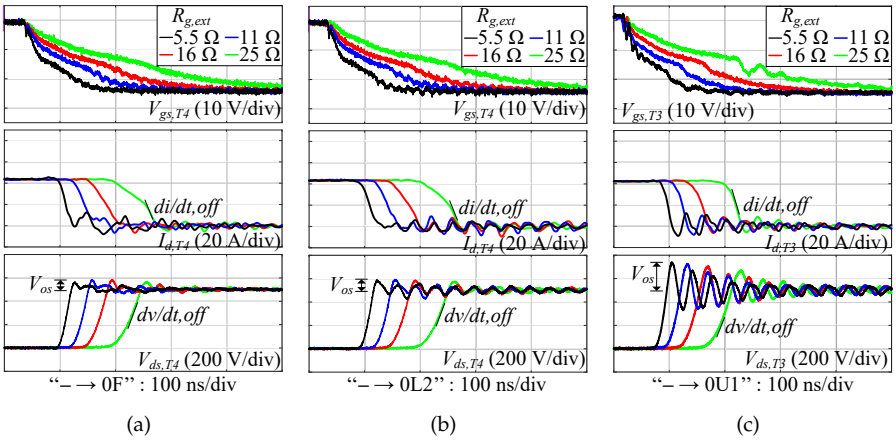


Fig. 2.15: Turn-off waveforms of three commutation modes under the conditions of V_{bus} = 1000 V, I_L = 40 A, $R_{g,ext}$ = 5.5 Ω, 11 Ω, 16 Ω, and 25 Ω, and $C_{gs,ext}$ = 3.3 nF. (a) Full mode turn-off waveforms of $V_{gs,T4}$, $I_{d,T4}$, and $V_{ds,T4}$. (b) Outer mode turn-off waveforms of $V_{gs,T4}$, $I_{d,T4}$, and $V_{ds,T4}$. (c) Inner mode turn-off waveforms of $V_{gs,T3}$, $I_{d,T3}$, and $V_{ds,T3}$. Source: [**J1**].

2.4.3 Result Analysis – Multi-Frequency Switching Oscillation

To validate the multi-frequency switching-oscillation phenomena in the 3L-ANPC inverter (as discussed in Chapter 2.3), multiple fast Fourier transform (FFT) analyses are performed on drain-source voltage waveforms for the identification of switching-oscillation frequencies.

Figs. 2.16(a) and 2.16(b) present the time-domain waveforms of drain-source voltages of switches T_2 and T_6 as well as their frequency spectrums during the full-mode transition "0F → –". It is obtained that a single device can have double oscillation components, owing to the mutual-interference between paralleled switching loops, i.e., main loops I and II. Specifically, both $V_{ds,T2}$ and $V_{ds,T6}$ contain dual oscillation frequencies at 30.1 MHz and 50.5 MHz during the analyzed FFT interval. Moreover, $V_{ds,T2}$ exhibits a more significant voltage overshoot than $V_{ds,T6}$, which is dominated by the low-frequency switching-oscillation component (at 30.1 MHz). For the "– → 0F" transition, i.e., the transient when T_4 is turned off , the voltage overshoot of $V_{ds,T4}$ is relived compared with those exhibited on $V_{ds,T2}$ and $V_{ds,T6}$, which can be concluded from Fig. 2.17. This can be explained by that the total loop inductance during "– → 0F", i.e., $L_{tot}^{-\rightarrow 0F}$ discussed in Chapter 2.3, can be regarded as the parallel inductance of loops I and II. Additionally, three switching-oscillation components can be identified from $V_{ds,T4}$, where the 34.9 MHz and 60.1 MHz ones are induced by asymmetrical reverse-recovery of T_2 and T_6. For the full-mode commutations "0F → –" and "– → 0F", the

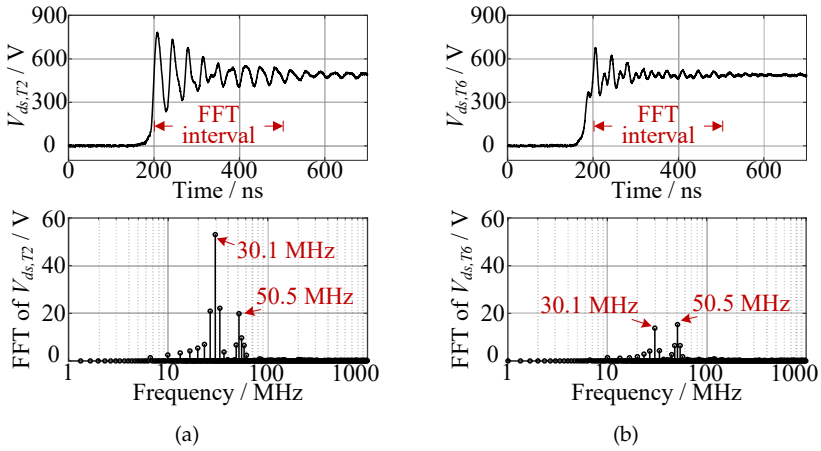


Fig. 2.16: FFT analysis of the full-mode transition "0F → –" with V_{bus} = 1000 V, I_L = 40 A, $R_{g,ext}$ = 5.5 Ω, and $C_{g,ext}$ = 3.3 nF. (a) $V_{ds,T2}$ during "0F → –". (b) $V_{ds,T6}$ during "0F → –". Source: **[J1]**.

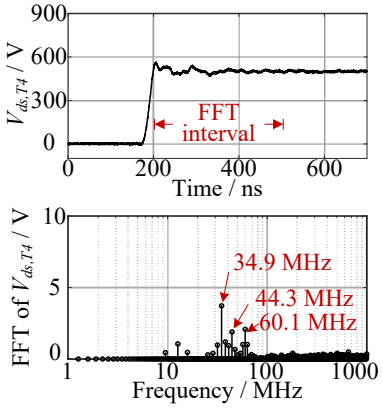


Fig. 2.17: FFT analysis of $V_{ds,T4}$ for the full-mode transition "– → 0F" with V_{bus} = 1000 V, I_L = 40 A, $R_{g,ext}$ = 5.5 Ω, and $C_{g,ext}$ = 3.3 nF. Source: **[J1]**.

oscillation frequencies obtained from FFT are summarized in Table 2.5, where limited frequency errors (less than 3.6 MHz) between theory and experiment can be found.

As it is already predicted in Chapter 2.3, the outer-mode commutation "0L2 → –" features a similar multi-frequency oscillation characteristic as the full-mode commutation "0F → –". Two oscillation components at 29.9 MHz and 49.9 MHz are found from the frequency spectrum of $V_{ds,T6}$, as shown in Fig. 2.18(a). In Fig. 2.18(b), two oscillation components of 32.8 MHz and 52.4 MHz are identified from the frequency spectrum of $V_{ds,T4}$ during "– → 0L2",

Table 2.5: FFT results of device drain-source voltages in comparison with theoretical oscillation frequencies. Source: **[J1]**.

Commutation types		V_{ds} studied	Measured Oscillations	Theoretical Oscillations	Theoretical errors
Full	"0F → –"	$V_{ds,T2}$	30.1 & 50.5 MHz	29.4 & 49.4 MHz	0.7 & 1.1 MHz
		$V_{ds,T6}$	30.1 & 50.5 MHz	29.4 & 49.4 MHz	0.7 & 1.1 MHz
	"– → 0F"	$V_{ds,T4}$	44.3 MHz	47.9 MHz	3.6 MHz
Outer	"0L2 → –"	$V_{ds,T6}$	29.9 & 49.9 MHz	29.4 & 49.4 MHz	0.5 MHz
	"– → 0L2"	$V_{ds,T4}$	32.8 & 52.4 MHz	34.3 & 51.8 MHz	1.5 & 0.6 MHz
Inner	"0U1 → –"	$V_{ds,T2}$	29.7 MHz	30.5 MHz	0.8 MHz
	"– → 0U1"	$V_{ds,T3}$	28.3 MHz	30.5 MHz	2.2 MHz

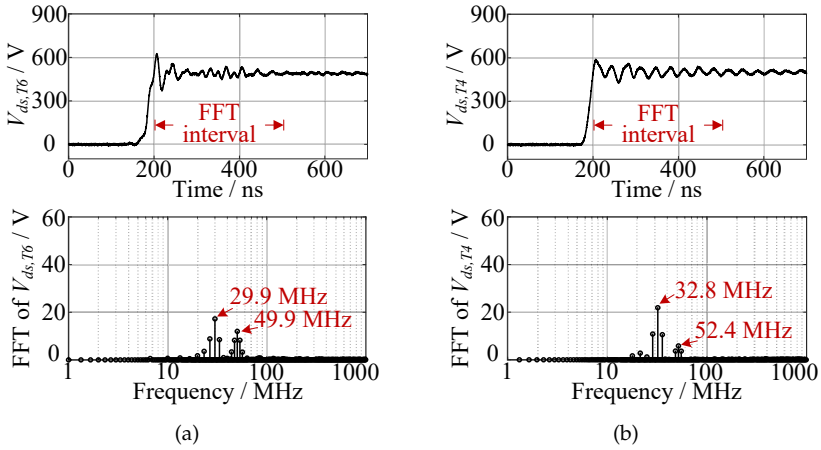


Fig. 2.18: FFT analysis of the outer-mode transitions "0L2 → –" and "– → 0L2" with V_{bus} = 1000 V, I_L = 40 A, $R_{g,ext}$ = 5.5 Ω, and $C_{g,ext}$ = 3.3 nF. (a) $V_{ds,T6}$ during "0L2 → –". (b) $V_{ds,T4}$ during "– → 0L2". Source: **[J1]**.

both of which are slightly higher than the ones obtained from the transients "0F → –" and "0L2 → –". Moreover, the measured oscillation frequencies by FFT during outer-mode commutations also match with theoretical derivations with limited frequency error (less than 1.5 MHz), as listed in Table 2.5.

Regarding the inner mode, the FFT results of $V_{ds,T2}$ during "0U1 → –" and $V_{ds,T3}$ during "– → 0U1" are presented in Figs. 2.19(a) and 2.19(b), respectively. Only a single oscillation component is identified in each inner-mode commutation, as 29.7 MHz and 28.3 MHz in Figs. 2.19(a) and 2.19(b), respectively. This also matches the theoretical assumption proposed in Chapter 2.3. Nevertheless, the oscillation magnitude, i.e., the voltage overshoot, exhibited

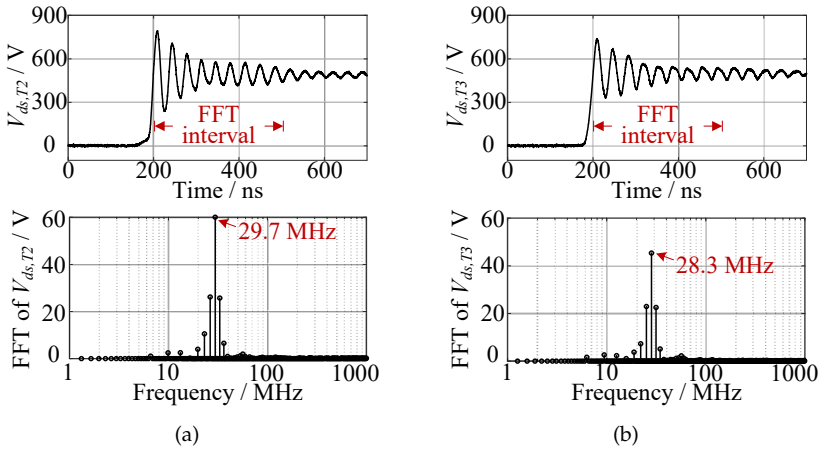


Fig. 2.19: FFT analysis of the inner-mode transitions "0U1 → –" and "– → 0U1" with V_{bus} = 1000 V, I_L = 40 A, $R_{g,ext}$ = 5.5 Ω, and $C_{g,ext}$ = 3.3 nF. (a) $V_{ds,T2}$ during "0U1 → –". (b) $V_{ds,T3}$ during "– → 0U1". Source: [**J1**].

on $V_{ds,T2}$ and $V_{ds,T3}$ are significant. A more detailed comparison of voltage overshoot magnitude will be given in the following sub-chapter.

2.4.4 Result Analysis – Voltage Overshoots, Current Overshoots, and Capacitive Charge

A comparison of drain-source voltage overshoots for the three commutation modes is exhibited in Fig. 2.20. The switches T_2 and T_3 (applicable for inner mode) bears the most significant voltage overshoots since loop II encloses them with larger parasitic inductance. It is noted that although no phase-current commutates through T_2 during the outer mode, it still suffers a critical voltage overshoot with a comparable magnitude. Also, operating T_6 in full mode will cause a slightly higher overshoot magnitude that in the outer mode.

A comparison of another representative switching characteristic, the drain-current overshoot, is depicted in Fig. 2.21(a). Although the transient current overshoot will not cause reliability issues, it can introduce additional turn-on losses. The full mode and outer mode have twice the current overshoot magnitude than the inner mode within the applied $R_{g,ext}$ range from 5.5 Ω to 25 Ω. This dramatic expansion of current overshoot can be explained by the excessive capacitance charge featured by both the full mode and outer mode, since output capacitances of T_2 and T_6 are charged during T_4's turn-on transient. Fig. 2.21(b) gives the total capacitive charges $Q_{oss,tot}$ of the three modes. It is noted that the full mode and outer mode are characterized by

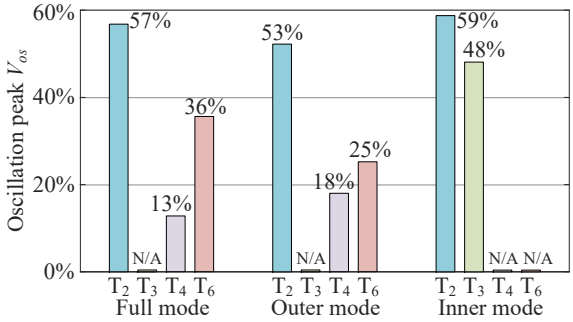


Fig. 2.20: Comparison of oscillation peaks V_{os} in percentage with respect to $V_{bus}/2$. Source: **[J1]**.

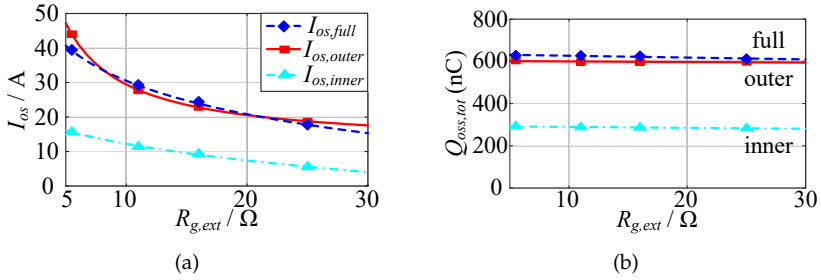


Fig. 2.21: Switch-on drain-current overshoots and total capacitive charges with the DPT condition of V_{bus} = 1000 V and I_L = 40 A. (a) Turn-on drain current overshoots I_{os}. (b) Total capacitive charges $Q_{oss,tot}$. Source: **[J1]**.

twice the $Q_{oss,tot}$ of the inner mode.

2.4.5 Result Analysis – Switching Losses

The turn-on and -off switching energies (E_{on} and E_{off}) of the main switches with $R_{g,ext}$ = 11 Ω are shown in Figs. 2.22(a) and 2.22(b), respectively. Owing to the excessive capacitance charge, the full mode and outer mode have higher switch-on energies compared to the inner mode, e.g., $E_{on,full}$ = 550 μJ and $E_{on,outer}$ = 560 μJ in comparison with $E_{on,inner}$ = 390 μJ under I_d = 40 A. The switch-off energies of full-mode and outer-mode commutations are reduced in comparison with that of the inner mode, as the capacitive charge stored in $C_{oss,T2}$ and $C_{oss,T6}$ can be released for the switch-off transient.

Overall, the total switching energies (i.e., $E_{tot} = E_{on} + E_{off}$) with $R_{g,ext}$ = 5.5 Ω, 11 Ω, 16 Ω, and 25 Ω are depicted in Figs. 2.23(a), 2.23(b), 2.23(c), and 2.23(d), respectively. Under conditions of $R_{g,ext}$ = 11 Ω, 16 Ω, and 25 Ω, the total switching energies of the three commutation types are similar throughout the drain-current range **[J1]**. Nevertheless, the inner mode has

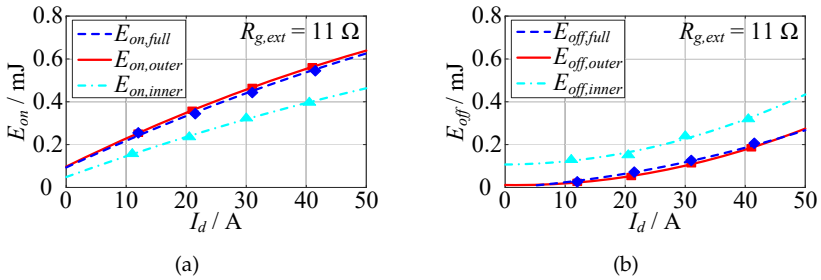


Fig. 2.22: Turn-on and turn-off switching energies of the with V_{bus} = 1000 V, $R_{g,ext}$ = 11 Ω, and $C_{g,ext}$ = 3.3 nF. (a) Turn-on switching energies E_{on}. (b) Turn-off switching energies E_{off}. Source: [**J1**].

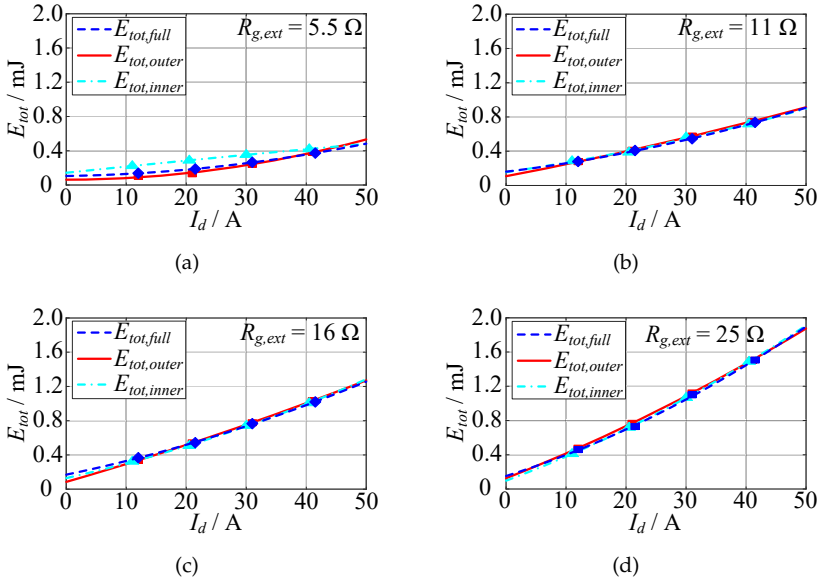


Fig. 2.23: Total switching energies E_{tot} with various $R_{g,ext}$ conditions. (a) $R_{g,ext}$ = 5.5 Ω. (b) $R_{g,ext}$ = 11 Ω. (c) $R_{g,ext}$ = 16 Ω. (d) $R_{g,ext}$ = 25 Ω. Source: [**J1**].

higher total switching energies (by 40–100 μJ) with the condition of $R_{g,ext}$ = 5.5 Ω, because the parasitic inductance of loop II can limit the speed of switching especially, under the condition with a low gate-resistance value.

Table 2.6: Overview of switching characteristics of SiC MOSFETs applied in the 3L-ANPC inverter prototype. Source: [**J1**].

Commutation types		Oscillation frequencies	Critical oscillations	Current overshoots	Switching energies	Capacitive charges
Full	"0F → –"	30.1 & 50.5 MHz	T_2 @ 284 V, 30.1 MHz	39 A	550 μJ	599.8 nC
	"– → 0F"	44.3 MHz	—	—	200 μJ	
Outer	"0L2 → –"	29.9 & 49.9 MHz	T_2 @ 261 V, 29.9 MHz	44 A	560 μJ	599.8 nC
	"– → 0L2"	32.8 & 52.4 MHz	—	—	190 μJ	
Inner	"0U1 → –"	29.7 MHz	T_2 @ 294 V, 27.9 MHz	16 A	390 μJ	299.9 nC
	"– → 0U1"	28.3 MHz	T_3 @ 240 V, 28.3 MHz	—	320 μJ	

2.5 Summary and Design Considerations

To answer the research question **Q1**, this chapter presents a comprehensive study of the switching behaviors of SiC MOSFETs in 1.5-kV 3L-ANPC inverters. An overview of the commutation characteristics of SiC MOSFETs with the three typical commutation modes in 3L-ANPC inverters is given in Table 2.6 [**J1**]. Owing to multiple switching loops during commutation, both the full and outer modes perform dual switching-oscillation components with separate frequencies. On the other hand, the inner mode performs a single oscillation frequency, since one commutation loop is associated.

Then, particular attention should be paid on the low-frequency switching-oscillations with frequency ranging from 28.3 MHz to 30.1 MHz (dominated by the loop II), as they can induce the most critical voltage overshoots on switches T_2 and T_3 during the fast-switching transients. Moreover, the full and outer modes also show other coincidences regarding current overshoot, capacitive charge, and switching energy. Specifically, higher current overshoot magnitude and twice the capacitive charge are observed for the full and outer modes, owing to the secondary switching-loop involved. Moreover, total switching energy of the inner mode is slightly higher than the others, especially under the fast-switching scenarios, e.g., with $R_{g,ext}$ = 5.5 Ω.

To answer the research question **Q2**, the following design considerations can be concluded to achieve a reliability improvement for SiC-based 1.5-kV 3L-ANPC inverters:

- To reduce voltage overshoots exposed to switches T_2 and T_3, efforts are to be focused on reducing the parasitic inductance of loop II. One way is to shorten the loop length of the inversion branch, i.e., the parasitic inductance contributed by $L_{\sigma inv}$ in Fig. 2.2(b).
- Other than designing the 3L-ANPC phase-leg based on half-bridge modules and PCB connections, integrating the six ANPC switches in a single power module housing can be a wise way to significantly exploit

the SiC merits and improve its operating reliability. In this regard, Infineon Technologies AG has successfully launched a SiC-based 3L-ANPC phase-leg module operating with the inner-mode commutation [76].

- The FEM-based analyses, e.g., ANSYS/Q3D, could be used to evaluate the design [**J1**]. Additionally, the magnetic-field cancellation technique can be used to mitigate the parasitic inductance of the commutation loop [71].

- Regarding the full and outer modes, the electromagnetic interference (EMI) filters shall be accurately sized to attenuate the commutation noises at dual oscillation ranges (i.e., 29.9–32.8 MHz and 49.9–52.4 MHz) [**J1**]. Specifically, more design considerations should be focused on the lower frequency range, i.e., 29.9–32.8 MHz, as higher amplitudes of oscillation are observed in this range. Regarding the inner-mode commutation, the design efforts of EMI filters can be specifically focused on the lower frequency range.

Related Publications:

J1. **M. Chen**, D. Pan, H. Wang, X. Wang, and F. Blaabjerg, "Investigation of Switching Oscillations for Silicon Carbide MOSFETs in Three-Level Active Neutral-Point-Clamped Inverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. PP, no. 99, pp. 1-15, 2020, Early Access.

C1. **M. Chen**, D. Pan, H. Wang, X. Wang, F. Blaabjerg, and W. Wang, "Switching Characterization of SiC MOSFETs in Three-Level Active Neutral-Point-Clamped Inverter Application," in *Proc. 2019 10th Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, May 2019, pp. 1793-1799.

Chapter 3

Temperature-Dependent Thermal Modeling of SiC MOSFETs

3.1 Brief Introduction

The mean junction temperature T_m and junction-temperature swing ΔT are known as two of the most important stressors to a variety of critical failure mechanisms in SiC MOSFETs. Although the pure-SiC material features a melting point up to 2830 °C [77], the peripheral packaging materials cannot withstand such high operating temperatures. Compared with the Si IGBT, the SiC MOSFET is even more fragile to high thermal stresses and temperature cycling. The SiC MOSFET can be damaged during short-time over-temperature events owing to its more compact die size and reduced gate-oxide thickness. The die-attach material (i.e., the solder joint in a conventional method) in a SiC MOSFET module will degrade two times faster than a Si-IGBT module during the long-term temperature-cycling, owing to the high stiffness of SiC die. Furthermore, other issues, e.g., the time-dependent dielectric breakdown, inter-layer dielectric erosion, and electrode delamination, can be triggered with a long-term high-temperature operating condition. To ensure the reliability of the SiC-based converter, a thermal model with a high accuracy level is highly demanded.

One of the critical issues for thermal modeling is that the thermal characteristics of several packaging materials may shift significantly with temperature variations; therefore, the thermal model in theory alters. Nevertheless, the state-of-art RC-lumped thermal models for the SiC MOSFET module are commonly calculated based on thermal tests or physical models with fixed

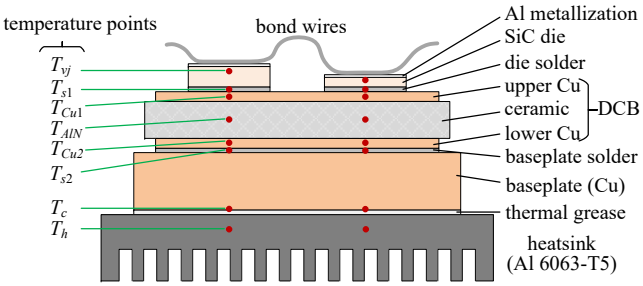


Fig. 3.1: Cross-sectional view of the half-bridge SiC module. Source: [**J2**].

temperature conditions. Subsequently, their accuracy levels for a wide-range (e.g., high temperature) thermal-profile prediction are unwarranted, and the SiC MOSFETs can suffer certain reliability issues due to some significant errors.

To address this reliability issue, a temperature-dependent Cauer-type (RC-lumped) thermal model is studied and proposed in this chapter. Temperature effects on packaging materials' thermal properties are studied and modeled. The proposed model can reflect the temperature effects of thermal properties of each physical packaging layer. This model is suited for a wide temperature range (especially the high-temperature) thermal simulation with a high level of accuracy. Furthermore, the proposed temperature-dependent thermal model is validated through experimental measurements of the junction-heatsink transient thermal impedance within a wide junction temperature range (60.5 °C to 199.6 °C).

3.2 Structure and Thermal Properties of a Commercial SiC MOSFET Module

3.2.1 Structure of SiC MOSFET Module

A cross-sectional diagram of a SiC module is illustrated in Fig. 3.1. The SiC dies are attached (by soldering) on direct copper bonded (DCB) substrate, which includes a ceramic insulation layer (by Al_2O_3, AlN, or Si_3N_4) sandwiched by double copper (Cu) layers [**J2**]. Further, the DCB substrate is soldered on a base plate (by Cu or AlSiC), which is then attached to a heatsink via thermal interface materials and dissipates the heat to the ambient.

Without losing the generality, a commercial SiC MOSFET module (APTMC-120AM55CT1AG from Microsemi) is used as a study case [70]. The top-side view and circuit diagram of the SiC module are illustrated in Fig. 2.1, and the dimensions of various packaging layers inside the SiC module are listed

Table 3.1: Dimensions of various packaging layers of the half-bridge SiC module as shown in Fig. 3.1 [78]. Source: **[J2]**.

Layers	**Size (mm^2)**	**Thickness (mm)**
MOSFET die	2.80×3.00 (per die)	0.18
SBD die	3.08×3.08 (per die)	0.377
MOSFET solder	2.80×3.00 (per die)	0.09
SBD solder	3.08×3.08 (per die)	0.09
Upper copper	28.2×25.54	0.3
Ceramic (AlN)	28.2×25.54	0.63
Lower copper	28.2×25.54	0.3
Baseplate solder	28.2×25.54	0.2
Baseplate	49.46×40.8	2.5
TIM (silicone grease)	49.46×40.8	0.1

in Table 3.1 [78]. The AlN is utilized as the DCB ceramic to achieve the heat-conduction path with a lower thermal resistance.

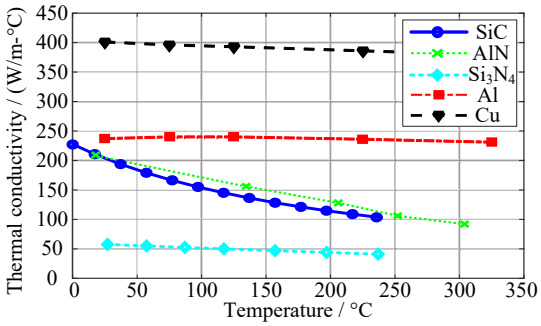
3.2.2 Temperature-Dependent Thermal Properties

The power modules with single-side cooling can be assumed to be adiabatic from both the top and lateral sides. Hence, the thermal characteristics (i.e., thermal conductivity and heat capacity) of packaging materials discussed in Chapter 3.2.1 remarkably affect the overall thermal behavior of the SiC module.

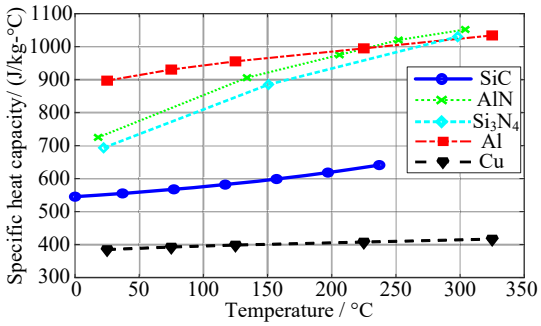
The thermal conductivities and specific heat capacities of multiple packaging layers (i.e., SiC, AlN, Si_3N_4, Al, and Cu) in correspondence with temperature are exhibited in Figs. 3.2(a) and 3.2(b), respectively [79–81]. It is noted that the both SiC's and AlN's thermal conductivities have an extensive dependency on temperature, which decrease with the growth of material temperature. Moreover, the specific heat capacities of SiC, AlN, Si_3N_4, and Al exhibit a positive correlation with material temperatures. After the temperature-dependent thermal conductivities and heat capacities are defined, a thermal model considering the temperature effect can be obtained through FEM simulations.

3.3 Extraction of the Temperature-Dependent Cauer Model

In this work, the Cauer-type RC-lumped thermal model (i.e., the Cauer model) is modified with temperature-dependency to characterize the thermal



(a)



(b)

Fig. 3.2: Thermal properties of module packaging layers in correspondence with material temperature [79–81]. (a) Thermal conductivity. (b) Specific heat capacity. Source: **[J2]**.

behavior of SiC MOSFET, since the Cauer model can reveal the temperature-dependent thermal properties of each physical layer **[J2]**. Fig. 3.3 shows a Cauer model of the SiC MOSFET module, where each packaging layer is represented by a thermal capacitance and a thermal resistance. The temperature-dependent thermal characteristics of different packaging geometries can in physics be revealed via variable thermal resistances and capacitances **[J2]**.

3.3.1 FEM Simulations of SiC MOSFET Module

To derive a temperature-dependent Cauer model, the FEM-based transient thermal simulations using ANSYS/Icepak are conducted in this work. Before the FEM simulations, a 3D model for the studied SiC module is built via Solidworks, where all structural details demonstrated in Fig. 3.1 are replicated. Then, the 3D CAD model is imported to ANSYS/Icepak, and all those temperature-dependent thermal conductivities and heat capacities are programmed in Icepak. The heat-source is set to be the upper-third volume of

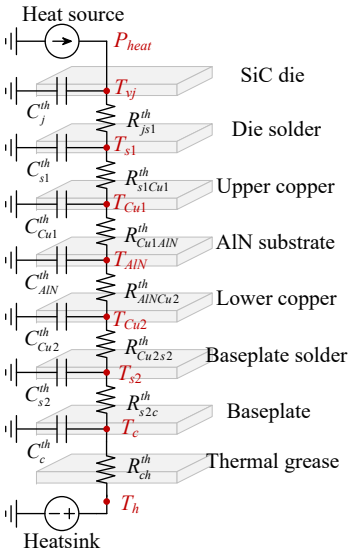
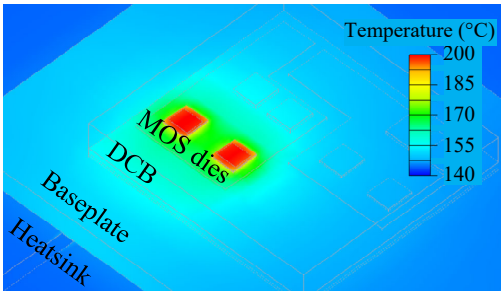


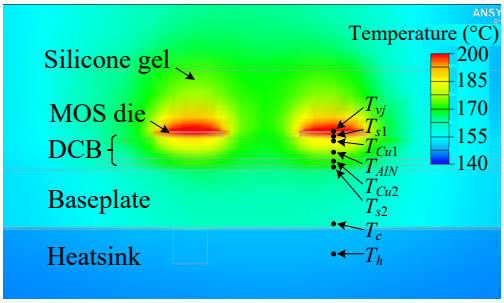
Fig. 3.3: Cauer-type thermal model of the SiC MOSFET module exhibiting physical meanings based on the layout presented in Fig. 3.1. Source: [**J2**].

the SiC-die to better simulate the real heat-distribution scenario inside the die [68, 82]. FEM-simulated thermal distribution of the SiC MOSFET module is demonstrated in Fig. 3.4, where the power module structure can be identified. The procedures to perform the transient thermal simulation are demonstrated as the following:

- The boundary conditions (e.g., the heatsink temperature T_h = 20 °C and heating power P_{heat} = 30 W) and properties of thermal materials are programmed before the thermal simulation.
- For the initial phase of thermal simulations, an invariable heating power P_{heat} is assigned to the SiC MOSFET die until the steady state (equilibrium) is reached.
- Then the heating power is removed in the FEM simulation, and the cooling phase starts. The temperatures at the measurement spots of various packaging layers are recorded, i.e., T_{vj} at the junction, T_{s1} at the die solder, T_{Cu1} at the upper copper, T_{AlN} at the ceramic, T_{Cu2} at the lower copper, T_{s2} at the baseplate solder, T_c at the case, and T_h at the heatsink, as illustrated in Fig. 3.4.
- Multiple simulation runs are then conducted with heatsink temperature variations, i.e., T_h = 50 °C, 80 °C, 110 °C, and 140 °C, and the aforementioned steps are replicated.



(a)



(b)

Fig. 3.4: Simulated temperature distribution under the heatsink temperature of 140 °C and heating power of 30 W per SiC die. (a) Top view. (b) Cross-sectional view. Source: **[J2]**.

It is noted that the virtual junction temperature T_{vj} is specified to be the mean temperature of the die volume in FEM simulations.

3.3.2 Extraction Methodology of Thermal Resistance and Capacitance

After the temperature responses under various temperature conditions are obtained, the values of thermal resistance and capacitance can be calculated. Fig. 3.5 exhibits a generalized Cauer model with multiple layers. The thermal resistances can be obtained by steady-state (thermal equilibrium) temperature measurements:

$$\begin{cases} R^{th}_{k-1,k} = \left(T_{k-1,steady} - T_{k,steady}\right) \Big/ P_{heat} \\ R^{th}_{k,k+1} = \left(T_{k,steady} - T_{k+1,steady}\right) \Big/ P_{heat} \end{cases} \tag{3.1}$$

where $T_{k-1,steady}$, $T_{k,steady}$, and $T_{k+1,steady}$ are the steady-state temperatures of the $(k-1)^{th}$, k^{th}, and $(k+1)^{th}$ measurement points, respectively **[J2]**.

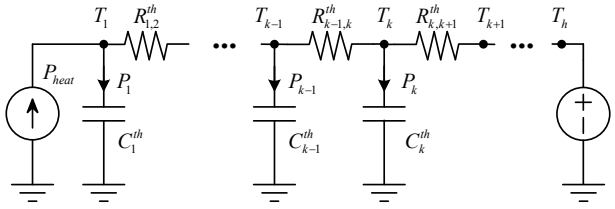


Fig. 3.5: Generalized Cauer-type thermal model with multiple physical layers. Source: **[J2]**.

Afterwards, the k^{th} layer's thermal capacitance is obtained through:

$$C^{th}_k = P_k(t) \Big/ \frac{dT_k(t)}{dt} \tag{3.2}$$

$$\begin{cases} P_k(t) = \frac{T_{k-1}(t)-T_k(t)}{R^{th}_{k-1,k}} - \frac{T_k(t)-T_{k+1}(t)}{R^{th}_{k,k+1}}, k \neq 1 \\ P_k(t) = -\frac{T_k(t)-T_{k+1}(t)}{R^{th}_{k,k+1}}, k = 1 \end{cases} \tag{3.3}$$

where $T_{k-1}(t)$, $T_k(t)$, and $T_{k+1}(t)$ designate the transient temperatures of the $(k-1)^{th}$, k^{th}, and $(k+1)^{th}$ measurement points recorded. Besides, $P_k(t)$ represents the instantaneous power passing through the k^{th} thermal capacitor **[J2]**.

3.3.3 Temperature-Dependent Cauer Model

The obtained thermal resistance values under various heatsink temperatures are represented as a bar-graph exhibited in Fig. 3.6. It can be seen that the thermal resistance components R^{th}_{js1} (junction to die solder), R^{th}_{Cu1AlN} (upper copper to ceramic), and R^{th}_{AlNCu2} (ceramic to lower copper) grow dramatically with the increase of heatsink temperature. In contrast, the thermal resistance contributed by other layers can be regarded as temperature-independent. The overall junction-to-heatsink thermal resistance rises from 0.5221 °C/W to 0.5787 °C/W (by 0.057 °C/W, 11%), as the heatsink temperature rises from 20 °C to 140 °C **[J2]**.

To show the thermal-resistance-temperature correlation via a Cauer model, curve fittings are conducted on R^{th}_{js1}, R^{th}_{Cu1AlN}, and R^{th}_{AlNCu2} with linear polynomial equations [83]:

$$R^{th}_{js1} = (1.2 \times 10^{-4}) \cdot T_{vj} + (4.93 \times 10^{-2}) \tag{3.4}$$

$$R^{th}_{Cu1AlN} = (1.5 \times 10^{-4}) \cdot T_{AlN} + (6.54 \times 10^{-2}) \tag{3.5}$$

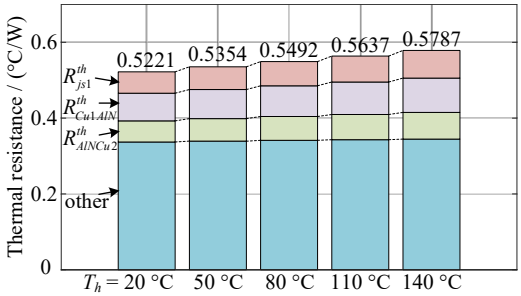


Fig. 3.6: FEM-extracted thermal resistance values under different thermal conditions (T_h = 20–140 °C). Source: **[J2]**.

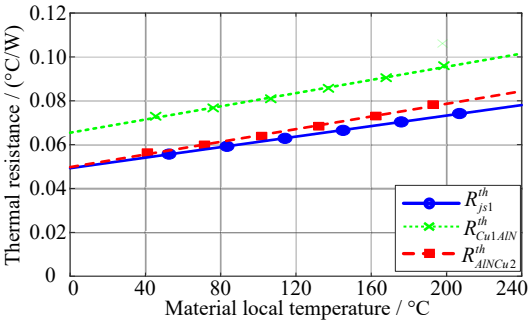


Fig. 3.7: Thermal resistance values (curve fitting) of R^{th}_{js1}, R^{th}_{Cu1AlN}, and R^{th}_{AlNCu2} in correspondence with material local temperature. Source: **[J2]**.

$$R^{th}_{AlNCu2} = (1.4 \times 10^{-4}) \cdot T_{AlN} + (4.98 \times 10^{-2}) \tag{3.6}$$

where T_{vj} and T_{AlN} are the virtual junction temperature and AlN ceramic temperature, respectively. Fig. 3.7 shows the curve fitting results, where acceptable matching precision is achieved using linear polynomial equations. Similarly, the thermal capacitance with a significant temperature dependency, i.e., C^{th}_{AlN}, can be extrapolated by curve fitting [83]:

$$C^{th}_{AlN} = (4.9 \times 10^{-5}) \cdot T_{AlN} + (1.95 \times 10^{-2}). \tag{3.7}$$

Finally, the temperature-dependent Cauer model is obtained, as exhibited in Fig. 3.8. The temperature-dependency mainly exists in components closely associated with the SiC and the AlN ceramic. Subsequently, thermal components R^{th}_{js1}, R^{th}_{Cu1AlN}, R^{th}_{AlNCu2}, and C^{th}_{AlN} are modeled to be temperature-dependent using linear polynomial relations (3.4)–(3.7), while others are modeled as temperature-constant. Then, the proposed temperature-dependent Cauer model is ready for thermal simulations. It is noted that the FEM based modeling methodology discussed in this chapter is not limited to specific

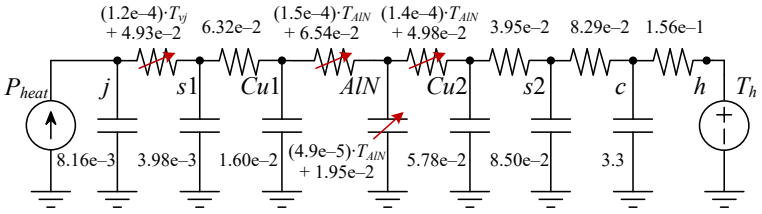


Fig. 3.8: The proposed Cauer-type thermal model with temperature-dependent RC components for the module shown in Fig. 3.1. Source: [**J2**].

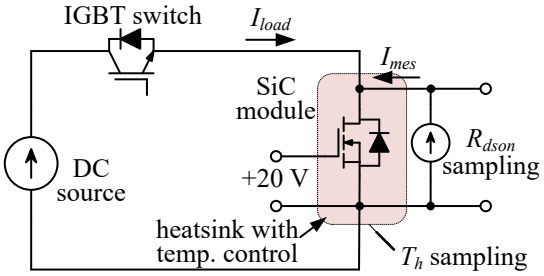


Fig. 3.9: Circuit diagram of the setup for characterization of the transient-thermal-impedance of SiC MOSFETs. Source: [**J2**].

cases, and its application can be extended to the thermal characterization of other types of power modules.

3.4 Experimental Characterization of Transient Thermal Impedance

3.4.1 Experiment Setup

To verify the proposed temperature-dependent Cauer model, experimental measurements of the junction-heatsink transient thermal impedance are performed. Fig. 3.9 demonstrates the circuit diagram of the experimental prototype, which includes a DC power source, an IGBT switch, and a SiC MOSFET module [**J2**]. The SiC MOSFET module is mounted on a temperature-controlled heatsink so that multiple heatsink temperature conditions can be realized. The gate-source voltage of SiC MOSFET maintains 20 V during the experiments, and the module can be heated by the load current (I_{load} = 30 A) supplied by the DC source. Furthermore, the ON/OFF of the load current is controlled by the auxiliary IGBT. A photography of the built experimental setup for the transient-thermal-impedance measurement is presented in Fig. 3.10.

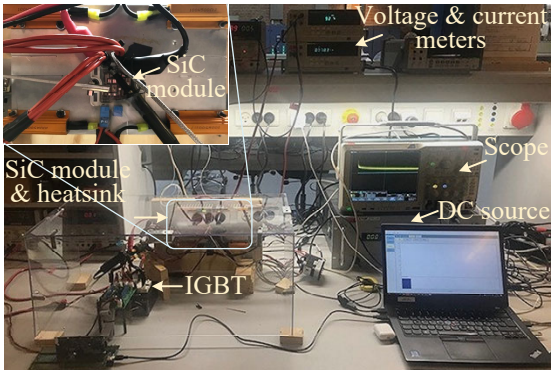


Fig. 3.10: Setup for the experimental characterization of transient-thermal-impedance of SiC MOSFETs. Source: **[J2]**.

3.4.2 Measurement of Transient Thermal Impedance

To measure the virtual junction temperature of the SiC MOSFET, the temperature-sensitive electrical parameter (TSEP) based method is utilized in this work. The on-state resistance R_{dson} of the device is sampled via external probes during the experiments, which indirectly reflects the virtual junction temperature T_{vj} of the SiC MOSFET [84]. Before the primary test, multiple sets of T_{vj}-R_{dson} data are experimentally obtained thanks to the temperature-controlled heatsink, and the following $T_{vj}(R_{dson})$ function can be extrapolated accordingly:

$$T_{vj}\left(R_{dson}\right) = \frac{n_1 \cdot {R_{dson}}^2 + n_2 \cdot R_{dson} + n_3}{R_{dson} + d_1} \tag{3.8}$$

where $n_1 = 1.842$, $n_2 = 66.95$, $n_3 = -4427$, and $d_1 = -14.67$.

Fig. 3.11 illustrates the procedure of transient-impedance measurement and the corresponding thermal responses. During the heating phase, the IGBT is ON, and a load current of $I_{load} = 30$ A constantly heats the SiC MOSFET die until a steady state (thermal equilibrium) is achieved. Then, the IGBT cuts the load current, and the transient temperatures $T_{vj}(t)$ (according to R_{dson}) and $T_h(t)$ are recorded during the cooling phase. Multiple experimental measurements are conducted with a wide range of heatsink temperatures, i.e., $T_h = 35.7\ ^\circ C$, $70.2\ ^\circ C$, $113.3\ ^\circ C$, and $145.8\ ^\circ C$. Table 3.2 exhibits the external conditions and steady-state parameters of various experiments. It is noted that a virtual junction temperature of 199.6 °C is achieved during the experiment. Then, the junction-heatsink transient thermal impedance is calculated according to:

$$Z_{jh}^{th}\left(t\right) = \frac{-\left[T_{vj}\left(t\right) - T_h\left(t\right)\right] + \Delta T_{steady}}{P_{heat}} \tag{3.9}$$

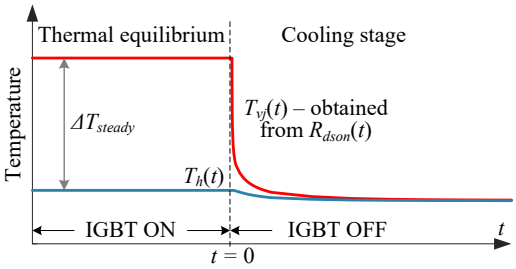


Fig. 3.11: Temperature waveform during the transient-thermal-impedance measurement process. Source: **[J2]**.

Table 3.2: Conditions for multiple experimental measurements: external conditions and steady-state results. Source: **[J2]**.

	Experiment No.			
	Expt 1	**Expt 2**	**Expt 3**	**Expt 4**
Heatsink temperature T_h	35.7 °C	70.2 °C	113.3 °C	145.8 °C
Load current I_{load}	30 A	30 A	30 A	30 A
Junction loss P_{heat}	46.3 W	55.4 W	73.2 W	91.9 W
Virtual junction temperature T_{vj}	60.5 °C	100.2 °C	154.9 °C	199.6 °C

where ΔT_{steady} denotes the steady-state junction-heatsink temperature difference, as marked in Fig. 3.11.

3.4.3 Experimental Results

The measured junction-heatsink transient thermal impedances $Z_{jh}^{th}(t)$ under T_h = 35.7 °C, 70.2 °C, 113.3 °C, and 145.8 °C are shown in Figs. 3.12(a), 3.12(b), 3.12(c), and 3.12(d), respectively. For validation, the thermal impedances of the temperature-dependent Cauer model (calibrated with the experimental conditions) are also plotted as dashed curves in Figs. 3.12(a)–3.12(d). The temperature-dependent Cauer model satisfactorily matches the experimental measurement under various temperature conditions, and steady-state errors of less than 0.9% can be identified for all cases. It is obtained that the proposed temperature-dependent Cauer model estimates the thermal behaviors of a real SiC module with limited errors throughout a broad temperature range. Additionally, it can be seen that the total thermal resistance R_{jh}^{th} is increased by over 10%, i.e., from 0.5287 °C/W to 0.5830 °C/W, as T_{vj} rises from 60.5 °C to 199.6 °C **[J2]**.

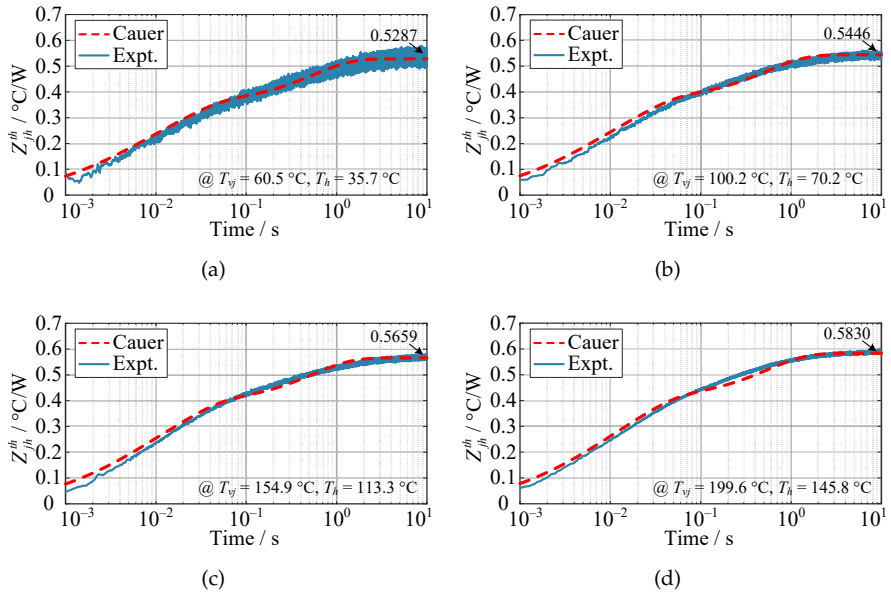


Fig. 3.12: Comparison of transient thermal impedance (junction-heatsink) attained from the experimental measurements and proposed Cauer model under various thermal conditions. (a) T_h = 35.7 °C, I_{load} = 30 A. (b) T_h = 70.2 °C, I_{load} = 30 A. (c) T_h = 113.3 °C, I_{load} = 30 A. (d) T_h = 145.8 °C, I_{load} = 30 A. Expt.: experimental measurement. Cauer: temperature-dependent Cauer model. Source: [**J2**].

3.5 Application of Transient Thermal Simulation

As the temperature-dependent Cauer model has been verified through the experimental measurement, an application case, i.e., thermal estimation with cyclic heating power, is demonstrated in this sub-chapter.

A flowchart for the thermal simulation using the temperature-dependent Cauer-model is illustrated in Fig. 3.13. Since the thermal components R^{th}_{js1}, R^{th}_{Cu1AlN}, R^{th}_{AlNCu2}, and C^{th}_{AlN} are modeled with temperature dependency, their values should be properly calibrated before the transient thermal simulation. A calibration process, including the steady-state iteration of T_{vj} and T_{AlN}, is implemented as shown in Fig. 3.13. After that, transient thermal simulations shall be performed utilizing these RC parameters after a calibration.

One of the most representative heating conditions for a SiC MOSFET can be considered as a periodic power generated by its conduction and switching losses. By simulating the proposed temperature-dependent Cauer model in a circuit simulator, the temperature profiles of junction (T_{vj}) and die-solder (T_{s1}) with a periodic power (square wave with 180 W magnitude, 50% duty cycle, and 50 Hz frequency) can be predicted as exhibited in Figs. 3.14(a) and

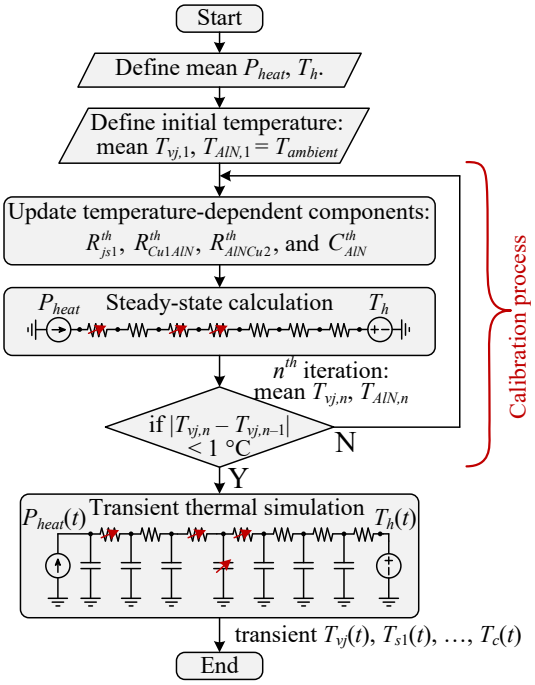


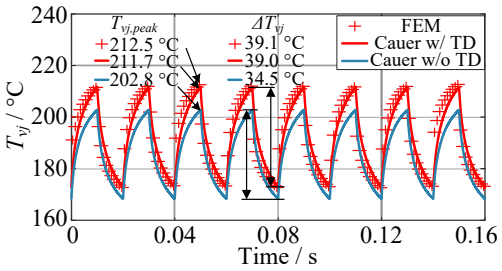
Fig. 3.13: Flowchart for the circuit-level thermal simulation using the temperature-dependent Cauer model. Source: **[J2]**.

3.14(b), respectively **[J2]**. The temperature of heatsink is set to be 140 °C. In order to compare, the T_{vj} and T_{s1} emulated from FEM software and a Cauer model omitting the temperature effects are also shown in Figs. 3.14(a) and 3.14(b).

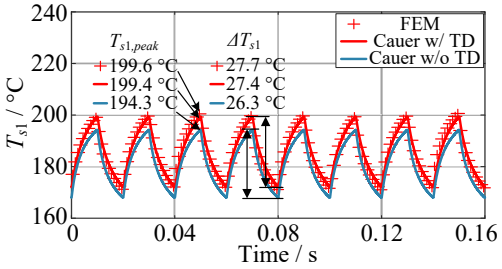
In both Figs. 3.14(a) and 3.14(b), the T_{vj} and T_{s1} calculated by the temperature-dependent Cauer model match well to these emulated by the FEM software. However, a dramatic discrepancy can be found if the temperature dependency of the Cauer model is omitted. The maximum T_{vj} difference between Cauer models with and without the temperature-dependency is found to be 8.9 °C at peak points $T_{vj,peak}$ in Fig. 3.14(a) **[J2]**. Besides, a significant estimation error on ΔT_{vj} can also be obtained from Fig. 3.14(b) as 4.5 °C. Similar observations can be witnessed in Fig. 3.14(b).

3.6 Summary

In order to answer the research question **Q3**, the thermal behavior of a commercial SiC module is characterized in this chapter with an enhanced accuracy level throughout a wide temperature range. It is concluded that



(a)



(b)

Fig. 3.14: Time-domain thermal profiles of the SiC MOSFET module. (a) Cauer-simulated virtual junction temperature T_{vj} with (w/) and without (w/o) the temperature dependency (TD), as well as the T_{vj} recorded from FEM simulations. (b) Cauer-simulated die-solder temperature T_{s1} w/ and w/o the TD, as well as the T_{s1} recorded from FEM simulations. Source: [**J2**].

the temperature-dependent thermal characteristics of various packaging materials (especially the SiC die and AlN ceramic) significantly deteriorate the temperature estimations.

Therefore, a temperature-dependent Cauer model and a FEM-based modeling methodology are proposed in this chapter. The temperature effect on the thermal properties of packaging materials is characterized as polynomial equations so that the proposed thermal model can achieve enhanced computational accuracy throughout a wide temperature range. The performance of the temperature-dependent Cauer model is confirmed through experimental characterizations of the transient thermal impedances.

It can also be observed from the Cauer model that the junction-heatsink thermal resistance is increased by over 10%, with T_{vj} being from 60.5 $^{\circ}C$ to 199.6 $^{\circ}C$ in the study case [**J2**]. An application case indicates a maximum junction-temperature rise of 8.9 $^{\circ}C$ by utilizing the proposed Cauer model. In addition, the calculated junction temperature swing ΔT_{vj} is increased by 4.5 $^{\circ}C$ using the proposed model.

Related Publications:

J2. **M. Chen**, H. Wang, D. Pan, X. Wang, and F. Blaabjerg, "Thermal Characterization of Silicon Carbide MOSFET Module Suitable for High-Temperature Computationally-Efficient Thermal-Profile Prediction," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. PP, no. 99, pp. 1-12, 2020, Early Access.

C2. **M. Chen**, H. Wang, F. Blaabjerg, X. Wang, and D. Pan, "A Temperature-Dependent Thermal Model of Silicon Carbide MOSFET Module for Long-Term Reliability Assessment," in *Proc. 2018 IEEE 4th Southern Power Electronics Conference (SPEC)*, Dec. 2018, pp. 1-7. (Best Paper Award)

Chapter 4

Wear-Out Failure Assessment of SiC MOSFETs in 3L-ANPC Inverter

4.1 Brief Introduction

4.1.1 System Description

The circuit diagram and specifications of a 1.5-kV 25-kW grid-connected 3L-ANPC inverter system are exhibited in Fig. 4.1 and Table 4.1, respectively. The operating maximum-power-point (MPP) voltage, i.e., $V_{dc,mpp}$ could vary from 850 V to 1350 V [36], and the ac-side nominal voltage is configured 600 V. Two groups of dc capacitors (C_{dc} = 1.35 mF) are connected in series to form a three-level dc-link, which consists of both aluminum-electrolytic capacitors (EPCOS B43630A5827) and metalized-polypropylene-film capacitors (EPCOS B32778G8606). The SiC MOSFET module APTMC120AM55CT1 is utilized as the switching devices T_1–T_6. The switching frequency of SiC MOSFETs is selected to be 48 kHz. A photography of the inverter prototype can be found in Fig. 2.12. It is worth to mention that this three-level architecture brings several merits. The volume and and cost of the ac-side filter, e.g., LCL filter, can be designed to be much lower when adopting the 3L-ANPC topology [40]. Moreover, the system leakage current can be significantly reduced due to a lower dv/dt during the operation [40].

It is noted that this chapter focuses on the wear-out reliability assessment of SiC devices, i.e., T_1–T_6, as shown in Fig. 4.1. Since the T_1–T_6 features different thermal loading profiles, i.e., different reliability metrics, the wear-out probability of various switches need to be studied separately in the following

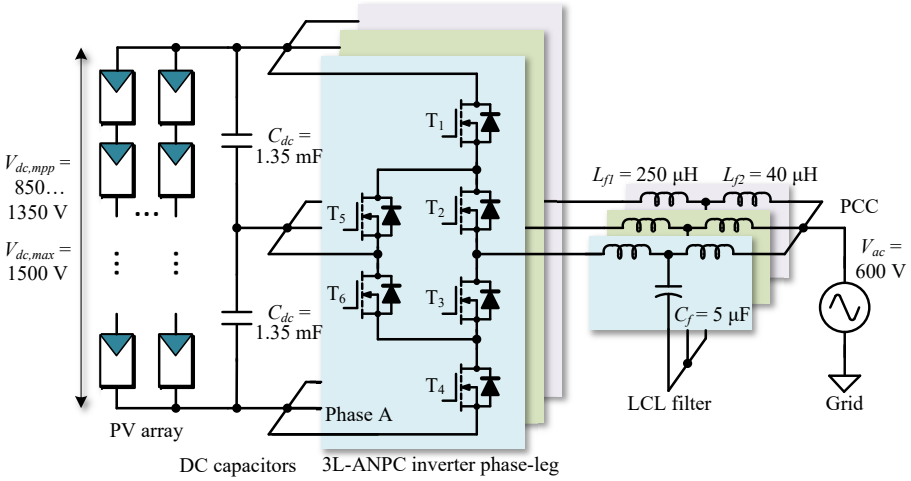


Fig. 4.1: Circuit diagram of the 1.5-kV grid-tied 3L-ANPC inverter system using SiC MOSFETs. Source: [**C3**].

Table 4.1: Specifications of the 1.5-kV 3L-ANPC inverter system. Source: [**J3**].

Parameter	Symbol	Value
Dc MPP voltage	$V_{dc,mpp}$	850...1350 V
Ac nominal voltage (line-line)	V_{ac}	600 V
Rated power	P_{nom}	25 kW
Dc capacitance	C_{dc}	1.35 mF
Converter-side inductance	L_{f1}	250 μH
Grid-side inductance	L_{f2}	40 μH
Filter capacitor	C_f	5 μF
Switching frequency	f_{sw}	48 kHz
Model of SiC MOSFETs	—	APTMC120AM55CT1
Model of dc capacitors	—	B43630A5827 & B32778G8606

sub-chapters.

4.1.2 Reliability Assessment Procedure

The thermal-cycling induced die-solder degradation has been identified as one of the most critical wear-out mechanisms for SiC MOSFETs. To study the wear-out failure probability of the SiC-based 1.5-kV inverter, a mission-profile-based reliability assessment methodology [65, 85–91] is utilized in this work.

The mission-profile-based reliability assessment flowchart is illustrated in

Fig. 4.2. A set of mission profiles, i.e., the solar irradiance SI and ambient temperature T_a, are fed into a PV array and a maximum-power-point tracking (MPPT) model, where the maximum-power-point (MPP) power P_{mpp} can be calculated accordingly. Electro-thermal calculations are then conducted to obtain the power loss P_{loss} and junction temperature T_j profiles of SiC MOSFETs. It is noted that the calculated T_j profile is fed back to the electrical model as the power loss of SiC MOSFET is dependent on its junction temperature profile. Thereafter, a rain-flow sorting algorithm is utilized to count the junction temperature cycling ΔT_j and mean junction temperature T_{jm} of the device. Accordingly, the annual damage D_{mg} of each SiC device can be obtained according to its lifetime model.

Nevertheless, in practice, the electro-thermal and lifetime model parameters may have variations due to manufacturing tolerances. These parametric variations also affect the calculated lifetime metrics, where statistical distributions need to be taken into account. Therefore, a risk analysis, i.e., a Monte-Carlo simulation, can be performed to obtain the lifetime distribution of 10000 samples considering normal distributions of electro-thermal and lifetime model parameters. Then, a Weibull distribution fit can be conducted to derive the probability distribution function (PDF) for each SiC component. Finally, the system-level wear-out probability of the SiC-based inverter bridge can be obtained according to a system reliability model, which consists of a series connection of device-level reliability model. This means that if one SiC MOSFET fails, the inverter system will fail.

4.2 Electro-Thermal and Lifetime Modeling of SiC Devices

4.2.1 Electrical Model of SiC MOSFETs – Switching Losses

In this Ph.D. project, half-bridge SiC MOSFET modules APTMC120AMCT-1AG (from Microsemi) are utilized as building blocks of the 1.5-kV 3L-ANPC phase leg. As mentioned before, the device is rated at 1200 V and 42 A under the case temperature of 80 °C [70]. The detailed structural diagrams of the SiC MOSFET module and 3L-ANPC phage leg are depicted in Figs. 2.1 and 2.2, respectively.

To obtain the practical power-loss characteristics of the SiC MOSFET module, a set of double-pulse tests (DPTs) are conducted with the 3L-ANPC inverter prototype [**J1**]. Multiple DPTs are performed with different external-gate-resistances and drain-currents, i.e., $R_{g,ext}$ = 5.5–25 Ω, I_d = 10–40 A, and V_{dc} = 1000 V. The total switching energies per switching cycle ($E_{tot} = E_{on} + E_{off}$) under full-mode, outer-mode, and inner-mode commutations are exhibited in Figs. 2.23(a)-2.23(d). A curve-fitting process can be performed to

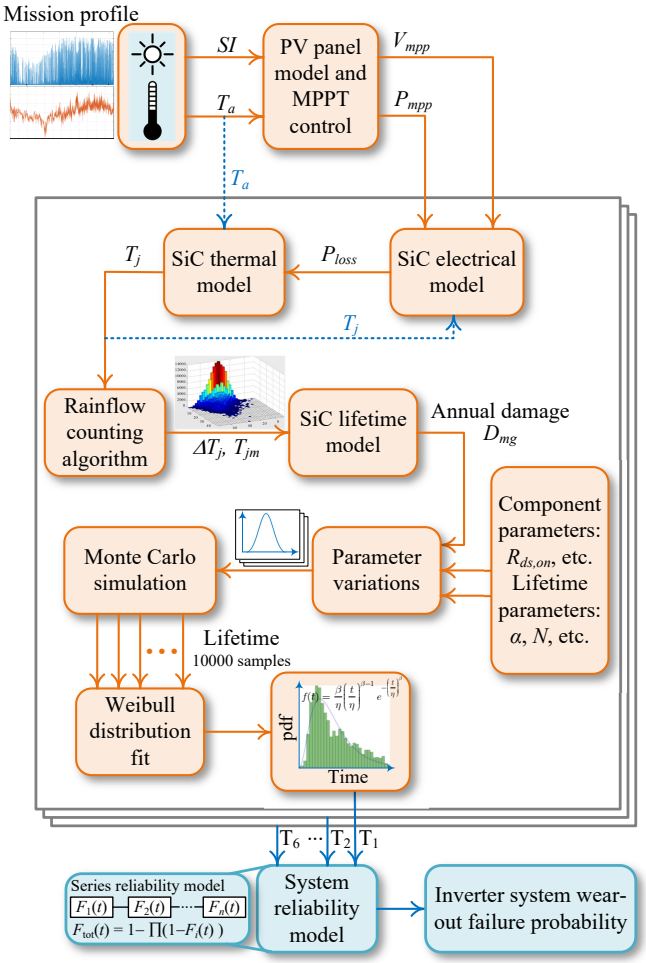


Fig. 4.2: Mission-profile based reliability assessment flow chart for SiC MOSFETs and the whole PV inverter. Source: [**J3**].

extrapolate the total-switching-energy function in the dependence of drain current [92]:

$$E_{tot}(R_{g,ext}, I_d) = E_{on}(I_d) + E_{off}(I_d) = a_1 \cdot I_d^2 + a_2 \cdot I_d + a_3 \tag{4.1}$$

where a_1, a_2, and a_3 are scaling factors obtained by the curve fitting. Then, the averaged switching-loss P_{sw} can be calculated by integrating the total switching energy over a line-frequency cycle:

$$P_{sw,MOS}(R_{g,ext}, P_{op}) = \frac{f_{sw}}{2\pi} \cdot \int_0^{2\pi} E_{tot}[I_d(\omega t)] \cdot d\omega t \tag{4.2}$$

where f_{sw} = 48 kHz is the switching frequency adopted in this work, and P_{op} represents the operating power of the inverter.

4.2.2 Electrical Model of SiC MOSFETs – Conduction Losses

The conduction feature of SiC MOSFETs can be regarded as a drain-source resistance $R_{ds,on}$ in dependence on the junction temperature T_j [92]:

$$R_{ds,on}(T_j) = R_{ds,on}(25^{\circ}C) \cdot (1 + \frac{\alpha_T}{100})^{T_j - 25^{\circ}C} \tag{4.3}$$

where the coefficient α_T is obtained as 0.46 for the SiC MOSFET module adopted in this work. Thereafter, the conduction loss can be written as (4.4):

$$P_{cond,MOS}(T_j, P_{op}) = \frac{1}{2\pi} \cdot \int_0^{2\pi} R_{ds,on}(T_j) \cdot d_{cond}(\omega t) \cdot I_d(\omega t)^2 \cdot d\omega t \tag{4.4}$$

where $d_{cond}(\omega t)$ denotes the instantaneous duty cycle of the SiC device. Then, the total loss of a single SiC MOSFET $P_{tot,MOS}$ can be obtained as:

$$P_{tot,MOS}(R_{g,ext}, T_j, P_{op}) = P_{sw,MOS}(R_{g,ext}, P_{op}) + P_{cond,MOS}(T_j, P_{op}) \,. \tag{4.5}$$

As the total loss $P_{tot,MOS}$ is dependent on $R_{g,ext}$, T_j, and P_{op}, look-up tables of $P_{tot,MOS}$ considering these factors are generated for the reliability assessment process, as shown in Figs. 4.3(a)-4.3(c). For full-mode and outer-mode commutations, switches T_1 and T_4 bear the most critical thermal stresses, as they have both the switching and conduction losses. On the other hand, switches T_2 and T_3 have the greatest loss and thermal stresses during the inner-mode commutation. The detailed analyses in terms of commutation mechanisms of the three commutation modes can be found in Chapter 2.3.

It is noted that the SiC SBDs generates negligible reverse-recovery losses. Moreover, they only conduct during a 200 ns dead time interval per switching cycle (i.e., 20.8 μs with f_{sw} = 48 kHz). The SiC MOSFETs in the 3L-ANPC inverter can be regarded as modulated in a synchronous-rectification mode, where the load current only conducts through the SiC MOSFET. It can be obtained from Fig. 4.4 that the forward voltage of SBD (V_f) is more significant than the on-state drain-source voltage ($V_{ds,on}$) under comparable junction-temperature and conduction-current conditions. Hence, the power losses of SiC SBDs can be omitted compared to these of SiC MOSFETs in 3L-ANPC inverters.

4.2.3 Thermal Model of SiC MOSFETs

As discussed in Chapter 3, the thermal model of the SiC MOSFET module is dependent on the material temperature. The junction-heatsink thermal resistance is increased by more than 10%, with the junction tempera-

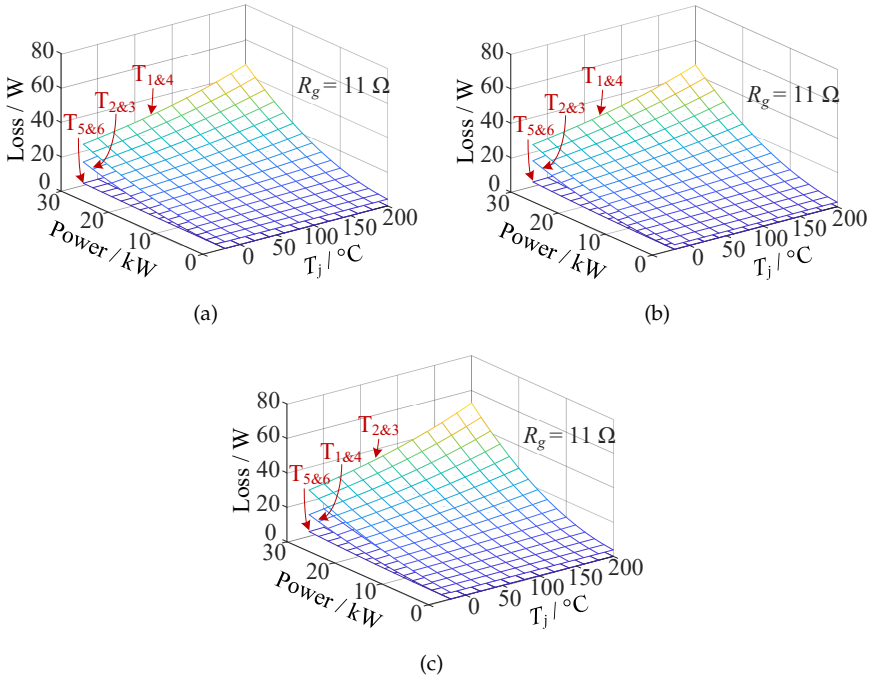


Fig. 4.3: Look-up table for the fast power-loss calculation of SiC MOSFETs with $R_{g,ext}$ = 11 Ω. (a) Full-mode commutation. (b) Outer-mode commutation. (c) Inner-mode commutation. Source: **[J3]**.

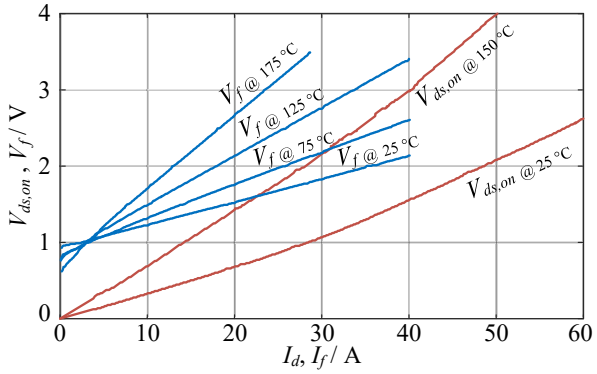


Fig. 4.4: Conduction characteristics of the external SiC SBD and SiC MOSFET: SBD's forward voltage V_f and MOSFET's on-state drain-source voltage $V_{ds,on}$ in correspondence with the conduction current and junction temperature. Source: **[C3]**.

ture being from 60.5 °C to 199.6 °C **[J2]**. To obtain more accurate thermal and lifetime predictions, the temperature-dependent Cauer-type thermal

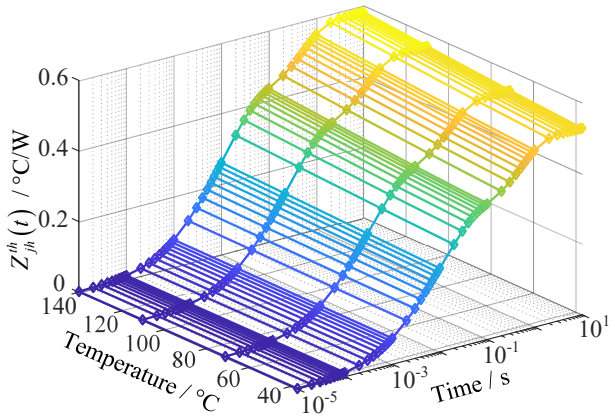


Fig. 4.5: Temperature-dependent junction-heatsink thermal model of SiC MOSFET: transient-thermal-impedance curve.

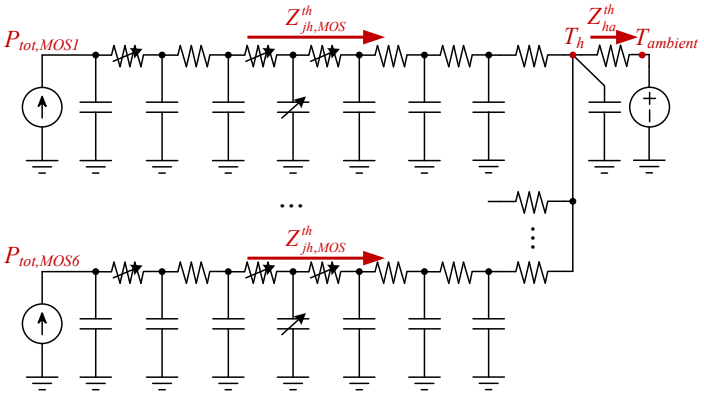


Fig. 4.6: Phase-leg level thermal model of SiC based 3L-ANPC inverter. Source: **[J3]**.

model (Cauer model) obtained in Chapter 3 is used in this Chapter for the thermal-profile prediction, as depicted in Fig. 3.8. The thermal resistances of the junction to die-solder (j-s1), upper DCB copper to ceramic (Cu1-AlN), and ceramic to lower DCB copper (AlN-Cu2) are modeled as temperature-dependent. Accordingly, the magnitude of the junction-heatsink transient thermal impedance can be raised remarkably as the temperature increases, as exhibited in Fig. 4.5.

For the phase-leg level thermal modeling, multiple SiC dies can be regarded as coupled through the common heatsink. As depicted in Fig. 4.6, multiple junction-heatsink thermal paths, i.e., $Z_{jh,MOS}^{th}$ branches, are joint together at the heatsink node. Then the heatsink-ambient thermal impedance can be modeled as a first-order RC network.

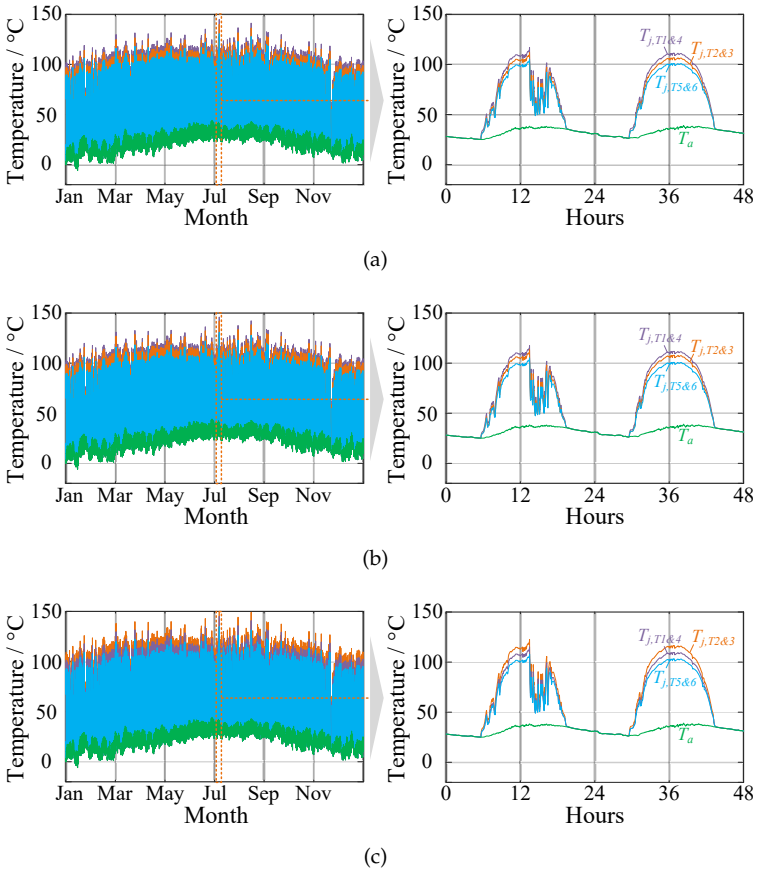


Fig. 4.7: Calculated temperature profile for various SiC components (T_1–T_6) under three typical commutation modes. (a) Full-mode commutation. (b) Outer-mode commutation. (c) Inner-mode commutation. Source: **[J3]**.

Based on the electrical and thermal models proposed in this chapter, the junction-temperature of SiC devices under the three different commutation modes can be obtained. Fig. 4.7 exhibits the calculated one-year temperature profiles with the mission profile captured from Arizona, USA. Moreover, 48-hour zoom-in-views are depicted on the right side. For the full-mode and outer-mode commutations, it can be observed that outer switches T_1 and T_4 are thermal-critical components, as they feature the largest amplitude of the junction-temperature swing ΔT_j. For the inner-mode commutation, on the other hand, inner switches T_2 and T_3 can be identified as devices with the most significant thermal stresses.

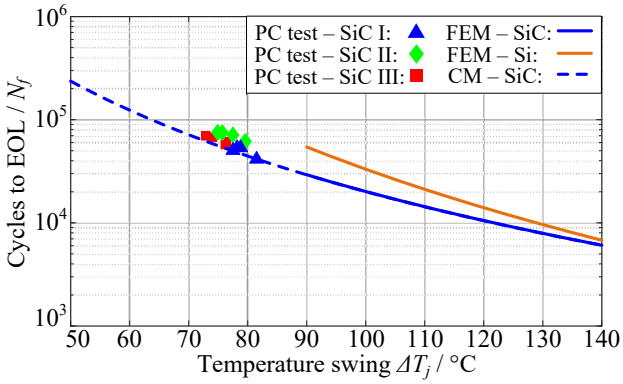


Fig. 4.8: Lifetime benchmark between SiC MOSFET and Si IGBT. Power cycling (PC) test results are presented in [16, 19], and finite-element-method (FEM) simulation results are available in [17]. CM: Coffin-Manson extrapolation–(4.6). Source: **[J3]**.

4.2.4 Lifetime Model of SiC MOSFETs

At present, there is no power-cycling lifetime model published regarding the SiC MOSFET die-solder wear-out issue. Applying the available Si-IGBT's lifetime models [93, 94] to assess the reliability of SiC MOSFETs leads to optimistic lifetime estimations. Nevertheless, power-cycling (PC) test data and finite-element-method (FEM) simulation results regarding the SiC die-solder wear-out issue can be found in [16, 17, 19], which are also depicted in Fig. 4.8. The end-of-life criteria is defined as a transient-thermal-impedance increase of 20%, which is closely related to the solder degradation. It can be observed from FEM results that the life cycles of Si IGBT are greater than that of SiC MOSFET throughout a wide ΔT_j range. The number of cycles N_f to end-of-life of SiC devices can be extrapolated by the Coffin-Manson relation [95]:

$$N_f = \alpha \cdot (\Delta T_j)^{-n} \,. \tag{4.6}$$

By means of curve fitting, the coefficients α and n can be attained as 2.64×10^{11} and 3.559, respectively. The extrapolated Coffin-Manson relation is also depicted in Fig. 4.8, where it matches with the results obtained from PC tests. It is noted that the mean junction temperature T_m could be another reliability stressor to the die-solder degradation, which does not appear in (4.6) due to the limited data collection of T_m. In [16, 19], a T_m range of 95–110 °C is reported for the PC tests of SiC devices. In [17], the T_m is fixed at 90 °C for various FEM simulations.

The Miner's rule is commonly used to accumulate the damages to the

devices [96], where the damage accumulates linearly according to:

$$D_{mg} = \sum_{k} \frac{n_k}{N_{f,k}} \tag{4.7}$$

where n_k denotes the accumulated number of cycles under a specific thermal stress, and $N_{f,k}$ [obtained by (4.6)] is the number of cycles to failure with this thermal-loading condition.

4.3 Analyses of Wear-Out Failure Probability

4.3.1 Annual Damage of Devices

After the number-of-cycles and cycling amplitude of thermal-loading profiles (in Fig. 4.7) are calculated through a rain-flow counting algorithm [97], the lifetime consumptions of various devices can be calculated and accumulated by (4.6) and (4.7). Fig. 4.9 presents the annual accumulated damage of different devices under the three ANPC commutation modes. Except for annual damages obtained by (4.6), the accumulation results by the classic LESIT model [93], which is proposed for Si IGBTs, are also depicted in Fig. 4.9 for damage comparison.

It can be seen that the classic LESIT model may lead to much optimistic lifetime consumption. By considering the SiC die-solder wear-out model (4.6), the annual damages of SiC devices will be raised by 2.2 times ($T_{5\&6}$, full mode) to 6.1 times ($T_{2\&3}$, inner mode), which are dependent on the device studied and the commutation mode. It is also observed that the inner switches T_2 and T_3 under inner-mode commutation have the most significant annual damage, followed by the outer switches T_1 and T_4 during the outer-mode and full-mode commutations.

4.3.2 Monte-Carlo Simulation

In real applications, the lifetime estimations may have considerable uncertainties, which can be induced by both the devices' manufacturing tolerance and variance of lifetime model parameters. On one aspect, the on-state resistance $R_{ds,on}$ of the utilized SiC MOSFET module may vary from 40 mΩ to 49 mΩ under T_j = 25 °C. Accordingly, a ΔT_j error of $\pm$ 8% can be attained based on the electro-thermal simulation discussed in Chapter 4.2. On the other aspect, the coefficient n in (4.6) features a parametric variation of $\pm$ 5%, according to [86, 94].

To investigate the impacts of these parametric uncertainties on the reliability of the 3L-ANPC inverter system, a risk analysis, i.e., Monte-Carlo simulation, is conducted in this Ph.D. project by considering all these parametric variations. As depicted by top-left and top-right curves in Figs. 4.10(a),

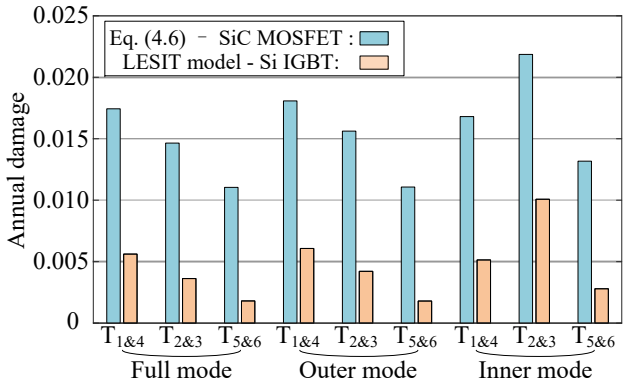


Fig. 4.9: Annual accumulated damage of SiC MOSFETs calculated by two different lifetime models, i.e., Eq. (4.6) and LESIT model, [93]., based on the mission profile in Fig. 4.7. Source: [**J3**].

4.10(b), and 4.10(c), both n and ΔT_j are modeled as subject to normal distributions, which have variations of $\pm$ 5% and $\pm$ 8% within their 99.7% confidence intervals, respectively. After that, a Monte-Carlo calculation on operation lifetime can be conducted with 10000 samples, each of which is implemented based on random values of n and ΔT_j extracted from their normal distributions. Figs. 4.10(a), 4.10(b), and 4.10(c) depict the histograms of wear-out lifetimes of different devices under the three commutation modes, which can be fitted to the Weibull distribution function [98]:

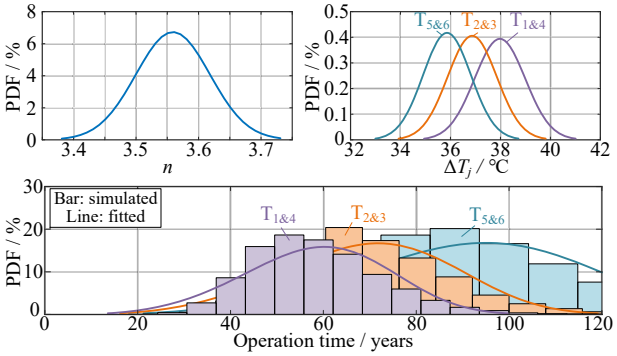
$$f(t) = \frac{\beta}{\eta} \cdot (\frac{t}{\eta})^{\beta-1} \cdot e^{-(\frac{t}{\eta})^{\beta}} \tag{4.8}$$

where $f(t)$ denotes the probability distribution functions (PDF) of the Weibull distribution, and β and η are the shape and scale factors, respectively. The fitted PDF $f(t)$ are also depicted in Figs. 4.10(a), 4.10(b), and 4.10(c), which match satisfactorily with Monte-Carlo simulation results. It is noted that the PDF values up to 120 years only have mathematical meanings, as other failure mechanisms, e.g., humidity induced failure, will appear in real-fields.

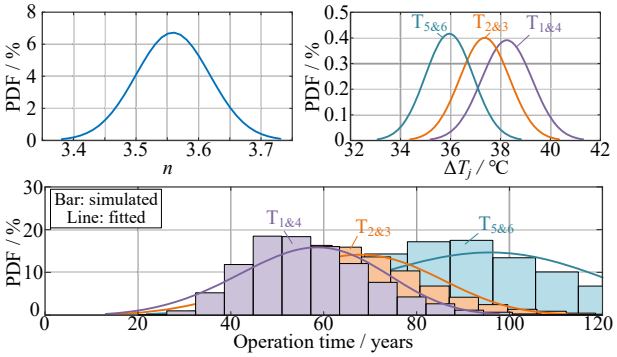
The cumulative distribution function (CDF) of the Weibull distribution, i.e., wear-our failure probability over the operation time t, can be obtained as the integration of the PDF:

$$F(t) = 1 - e^{-(\frac{t}{\eta})^{\beta}} \ . \tag{4.9}$$

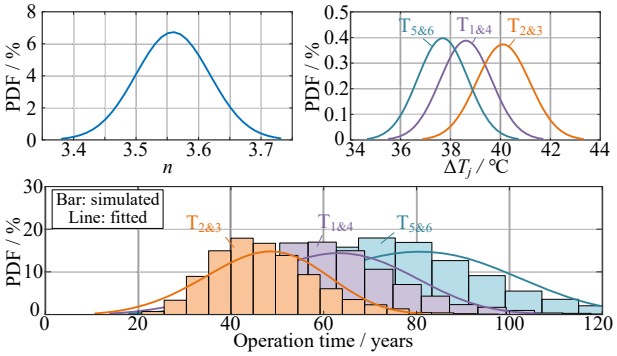
To obtain the system-level reliability function, i.e., the reliability function considering all SiC devices as a inverter system, a series reliability model is considered in this Ph.D. project. It is assumed that any device failure



(a)



(b)



(c)

Fig. 4.10: Probability distribution functions (PDF) of lifetime parameter n, static-state junction-temperature swing ΔT_j, and Monte-Carlo simulated operation time under three typical ANPC commutation modes using the identical mission profile. (a) Full-mode commutation. (b) Outer-mode commutation. (c) Inner-mode commutation. Source: **[J3]**.

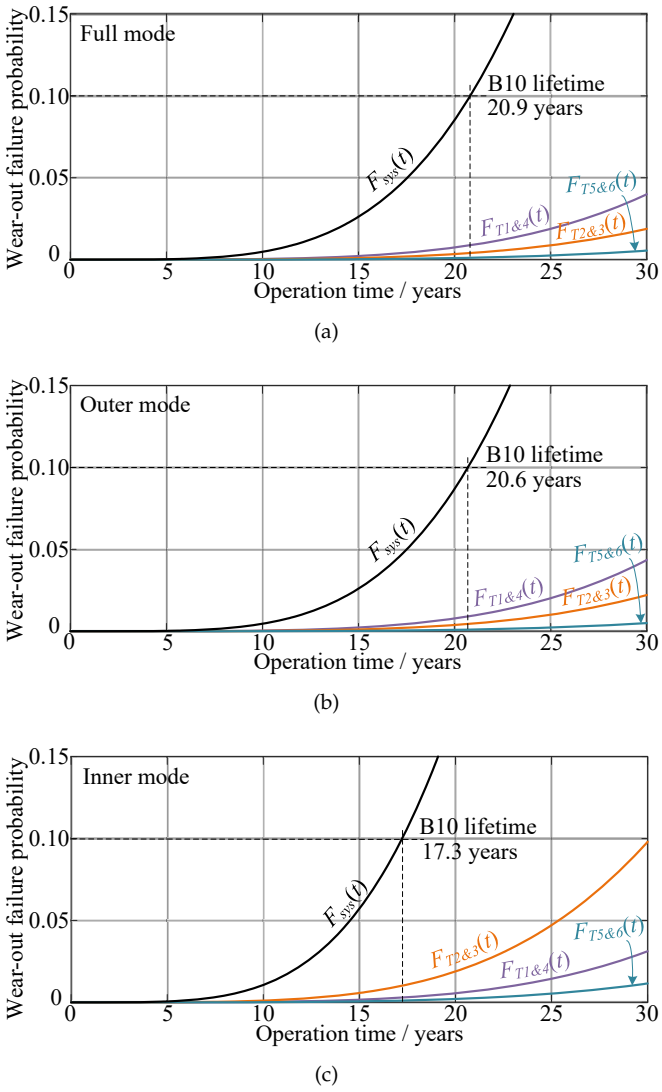


Fig. 4.11: Wear-out probability curve for SiC MOSFETs and inverter system. (a) Full-mode commutation. (b) Outer-mode commutation. (c) Inner-mode commutation. Source: **[J3]**.

introduces the system failure, whose wear-out failure probability $F_{sys}(t)$ is expressed as:

$$F_{sys}(t) = 1 - \prod[1 - F_i(t)] \tag{4.10}$$

where $F_i(t)$ denotes the wear-out failure probability of each SiC MOSFET.

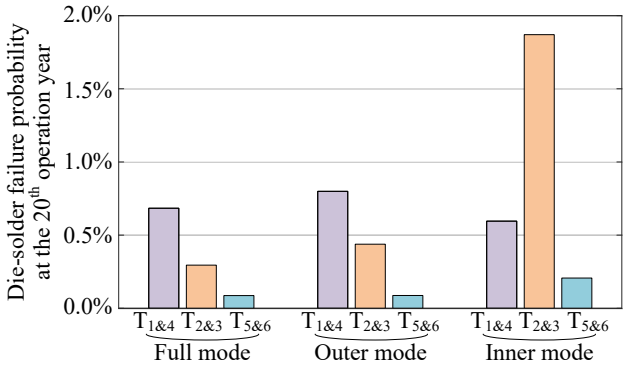


Fig. 4.12: Die-solder failure probability of various devices at the 20^{th} operation year. Source: **[J3]**.

4.3.3 Results Analyses

Fig. 4.11 depicts the wear-out failure probabilities of both system level and component level under the three ANPC commutation modes. The full mode and outer mode exhibit comparable performances in terms of their wear-our failure probabilities, and both of them are able to achieve B10 lifetimes above 20 years. As discussed previously, the reliability-critical components for both the full and outer modes are switches T_1 and T_4, as they suffer both switching and conduction losses.

For the inner-mode commutation, on the other hand, switches T_2 and T_3 can be identified as devices which are more fragile to wear-out failure. Due to a much higher failure rate of T_2 and T_3, the system-level B10 lifetime of inner mode (considering die-solder wear-out) is identified as 17.3 years, which is three years less than these of full mode and outer mode.

The die-solder failure probabilities of various SiC MOSFETs at the targeted 20^{th} operation year are exhibited in Fig. 4.12. Among all components, switches T_2 and T_3 for the inner-mode commutation have the highest failure probability of 1.87%, which is 3.1 to 9.1 times greater than other devices under the inner-mode commutation. For the full-mode and outer-mode commutations, T_1 and T_4 are devices with the most significant die-solder wear-out issues, which feature failure probabilities of 0.68% and 0.80%, respectively.

The analysis results in Fig. 4.11 and Fig. 4.12 can be useful for lifetime prediction and reliability-oriented design of practical SiC-based 3L-ANPC inverters. Nevertheless, it is noted that the reliability-assessment results presented in this Ph.D. project mainly focus on the die-solder wear-out issue of SiC MOSFETs, while the lifetime deduction caused by other failure mechanisms are not considered.

4.4 Summary

To address research questions **Q4** and **Q5**. This chapter studies the wear-out failure reliability of the SiC-based 1.5-kV 3L-ANPC inverter. To specifically answer the research question **Q4**, a lifetime model considering the SiC die-solder wear-out mechanism is developed to attain the more practical reliability characteristics for SiC-based power converters. Moreover, the temperature-dependent Cauer-type thermal model is utilized to improve the prediction accuracy for thermal-loading profiles.

Compared with calculations based on the classical LESIT model, the annual damages of SiC devices calculated by the developed model (considering SiC die-solder wear-out) are raised by 2.2–6.1 times, dependent on the thermal-mechanical stresses and operation modes of various SiC MOSFETs.

A risk analysis using the Monte-Carlo simulation is conducted, and the wear-out probabilities of both components and systems are obtained accordingly. It is identified that T_1 and T_4 are more fragile to wear-out failure for both the full-mode and outer-mode commutations (showing 20-year failure probabilities of 0.68% and 0.80%). At the same time, T_2 and T_3 are the reliability-critical components during the inner-mode commutation, which feature a failure probability of 1.87% at the 20^{th} operation year.

Related Publications:

J3. **M. Chen**, Z. Shen, H. Wang, X. Wang, and F. Blaabjerg, "Reliability Assessment of SiC MOSFETs in Three-Level Active Neutral-Point-Clamped Inverters Considering Die-Solder Degradation," *IEEE Trans. Power Electron.*, 2020, Status: to be Submitted.

C3. **M. Chen**, T. Zhu, D. Pan, H. Wang, X. Wang, and F. Blaabjerg, "Loss Analysis of SiC-Based Three-Level Active Neutral-Point-Clamped Inverters under Different Modulation Schemes," in *Proc. 2020 IEEE 9^{th} International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, Status: In Press.

Chapter 5

Conclusions

This chapter summarizes the methodologies and outcomes achieved in this Ph.D. project. Furthermore, the main contributions of this Ph.D. project are highlighted, and the research perspectives are discussed in this chapter.

5.1 Summary

Power electronic converter based on SiC devices is by far one of the most promising technology for an energy efficiency breakthrough in renewable energy systems. The market size of SiC devices for PV applications is kept booming over the recent years and is expected to reach 100 million US Dollars upon the year 2023. Nevertheless, the application of SiC power devices in the emerging 1.5-kV PV inverters still needs to address several reliability challenges. These include the uncertainties on switching behavior, thermal performance, and wear-out probability. Accordingly, this Ph.D. thesis focuses on addressing these reliability uncertainties faced by the SiC-based 3L-ANPC inverter for 1.5-kV PV applications.

In **Chapter 2**, the switching characteristics of SiC MOSFETs in a 1.5-kV 3L-ANPC inverter are investigated in a comprehensive way to identify the reliability challenges in terms of unfavorable switching behaviors. A parasitic model of the 3L-ANPC phase-leg, including parasitic components contributed by the SiC MOSFET module and PCB routing, is developed to characterize the switching behaviors. The switching oscillations and voltage overshoots featured by three representative ANPC commutation modes are studied, and the overvoltage-critical components are identified accordingly. These theoretical findings are verified through experimental results obtained from DPTs, and other switching behaviors in terms of drain-current overshoots, capacitive charges, and switching energies are also evaluated. Based on the above-mentioned scientific findings, several design considerations are pro-

posed to realize a reliability improvement for the SiC-based 1.5-kV 3L-ANPC inverter.

In **Chapter 3**, a temperature-dependent Cauer-type thermal model and its FEM-based characterization methodology are proposed to improve the accuracy of thermal-profile estimations throughout a wider temperature range. It is figured out that the temperature-dependent thermal properties of various package materials (especially the SiC die and AlN ceramic) can significantly affect the thermal estimations. A FEM simulation with temperature-dependent thermal properties integrated is conducted to extract the Cauer model. It is concluded from the proposed thermal model that the overall junction-heatsink thermal resistance is increased by more than 10%, with a virtual junction temperature T_{vj} being from 60.5 $^{\circ}C$ to 199.6 $^{\circ}C$ in the study case **[J2]**. Furthermore, the performance of the proposed thermal model is validated through multiple experimental measurements of the transient thermal impedances.

In **Chapter 4**, a long-term reliability assessment of the SiC-based 1.5-kV PV inverter considering the wear-out probability of SiC die-solder is conducted. A lifetime model characterizing the SiC die-solder wear-out is extrapolated. The reliability assessment is performed using the mission profile in Arizona, USA, and the reliability metrics of the three representative commutation modes, i.e., full mode, outer mode, and inner mode, are investigated individually. It is found that, by utilizing a newly developed lifetime model, the annual damages of SiC MOSFET are raised by 2.2 to 6.1 times, compared with the calculation based on a classical LESIT model [93]. Moreover, it is identified that devices T_1 and T_4 (see Fig. 4.12) are more fragile to wear-our failure under the full-mode and outer-mode commutations (showing 20-year failure probabilities of 0.68% and 0.80%). At the same time, T_2 and T_3 (see Fig. 4.12) are the reliability-critical components during the inner-mode commutation, which feature a failure probability of 1.87% at the 20^{th} operation year.

5.2 Main Contributions

The main contributions of this Ph.D. project are summarized as follows:

A) Switching-Behavior Investigation of SiC MOSFETs in 1.5-kV 3L-ANPC Inverter

- A parasitic model of the SiC-based 3L-ANPC phase-leg for switching-behaviors characterizations;
- Multi-frequency switching oscillations are modeled for SiC-based 1.5-kV 3L-ANPC inverters, and the mechanisms are identified for different

3L-ANPC commutation modes;

- Design considerations for more reliable 1.5-kV 3L-ANPC inverters with SiC MOSFETs.

B) Temperature-Dependent Thermal Modeling of SiC MOSFETs

- A temperature-dependent Cauer model for thermal-profile prediction of SiC MOSFET modules with enhanced precision throughout a wider temperature range;
- A FEM-based parameter extraction methodology of the Cauer-type thermal model with the consideration of temperature dependency;
- The temperature-sensitive electrical parameter (TSEP) based experimental measurements of transient thermal impedance within a wider temperature range (up to 200 $^{\circ}C$).

C) Wear-Out Failure Assessment of SiC MOSFETs in 3L-ANPC Inverter

- An extrapolated lifetime model of SiC devices considering die-solder degradation;
- A system-level reliability assessment of the 1.5-kV 3L-ANPC inverter is conducted. The lifetime reduction caused by the SiC die-solder is taken into consideration in the evaluation process.
- The wear-out reliability-critical components are identified for the three representative ANPC commutation modes.

5.3 Project Perspectives

Although several aspects of reliability challenges for the SiC-based 1.5-kV PV inverters have been addressed in this Ph.D. project, several scientific challenges remain unresolved. Several research perspectives are listed as follows:

- Regarding SiC switching behaviors, a considerable portion of the parasitic inductance in a commutation loop comes from the power module package. Therefore, optimizing the design of the PCB busbar will not be the ultimate way to mitigate the switching oscillations and voltage overshoots. Instead, integrating all of the SiC MOSFETs of the 3L-ANPC phase-leg into a single module-package would be the future trend [45].

- The lifetime model extrapolated in this Ph.D. project can only predict the service time of the SiC MOSFET module with conventional interconnection technologies, i.e., using the Sn-based solder and Al bond wires. As the interconnection technologies of the SiC power module keep developing, it would be interesting to see how much the system-level lifetime can be extended using the more advanced interconnection technologies.

- The reliability assessment conducted in this Ph.D. project does not consider the reliability metrics of the dc capacitor bank. It would be interesting to see that the reliability performances of both the SiC MOSFET module and dc capacitor bank are considered in future system-level reliability assessment of SiC-based 1.5-kV PV inverters.

- Currently, implementing the hybrid 3L-ANPC architectures with both Si and SiC switches (see Fig. 1.4) in 1.5-kV PV inverters is one effective way to reduce the system cost. It would also be interesting to see system-level reliability assessments and benchmarks on the two types of hybrid architectures given in Fig. 1.4.

- The fault-tolerant operation of the 3L-ANPC inverter can be implemented to enhance the system-level robustness of the SiC-based 1.5-kV PV inverter [99].

- The future design target for the PV interter system might be a thirty-year useful lifetime. This requires reliability improvements on the SiC module interconnection technologies, especially more reliable die-attach methods.

Appendix A

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