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***Abstract*—Control delay plays an important role in the stability of grid-connected voltage source converters (VSCs), and the critical value is one quarter of switching period ($0.25T_{sw}$) based on the passivity-based stability theory. However, the control delay is $1.5T_{sw}$ and $0.75T_{sw}$ for the regular single-sampling and double-sampling pulse width modulation (PWM), respectively, and there will be a large non-dissipative region in the high-frequency range. To tackle this challenge, an enhanced real-time-update PWM is proposed and the control delay can be kept to $0.25T_{sw}$. Moreover, compared with the conventional real-time-update PWM, the duty cycle is not limited and the grid-side current quality is similar. Finally, the simulation verifies the effectiveness of the proposed method.**

Keywords—grid-connected VSCs, current control, passivity, delay, real-time-update PWM.

I. Introduction

LCL-filtered grid-connected voltage source converters (VSCs) are widely used in distributed generation systems, e.g., photovoltaic, wind turbine, and energy storage systems [1]. Nevertheless, with the large-scale penetration of renewable generation, the grid admittance seen from the point of common coupling varies in a wide range, which poses a significant challenge to the VSC-grid interactive stability [2]. For example, even though the alternate-current controller (ACC) is well designed, the system may still be unstable when the phase difference is over 180° at the intersection point between the VSC output admittance and the grid admittance. As an extension of the admittance shaping in the frequency domain, the passivity-based current control is a promising solution to tackle the induced resonances regardless of the grid admittance. However, the pure passivity is impossible to obtain, and the upper boundary of the dissipative region is set to the Nyquist frequency [3].

For the single-loop converter-side current control, a control delay T_d is inevitable in the pulse width modulation (PWM) process, which leads to a non-dissipative region between the critical frequency ($\frac{1}{4T_d}$) and the switching frequency. Hence, the critical control delay should be at least $0.25T_{sw}$, and extra active damping is required for regular single-sampling (SS) and double-sampling (DS) PWM. Capacitor current feedback, capacitor voltage feedforward, or a combination can be used to enhance the passivity, which, however, makes the control system more complicated [3-4]. Another passivity enhancement route is to compensate for the control delay. Various terms are inserted in parallel with the ACC, such as high pass filter [5], biquad filter [6], and a predictive term [7], but their compensation effect in the high-frequency range is limited. Another alternative to reduce the control delay is shifting the sampling instant or the update instant of the PWM. Specifically, shifting the sampling instant can reduce the computation delay, but the aliased low-order harmonics will be introduced due to the sampled non-average value of current [8]. Shifting the update instant of the PWM can optimize the computation delay to zero, and only average value of current at the peak/valley of carrier is used [9-10]. However, due to the considerable code processing time, the control delay may increase when the duty cycle is larger/smaller than a specific value, which again jeopardizes the dissipativity of ACC.

To tackle this challenge, the existing real-time-update (RTU) PWM methods are evaluated, where a control delay analysis is given based on the voltage-second equivalence. Then an enhanced real-time-update (ERTU) PWM using multi-sampling is proposed in this paper. Not only the control delay can always be kept to the critical value $0.25T_{sw}$, but also the burden on the code processing time is released as well. Finally, the proposed method is verified through the simulation.

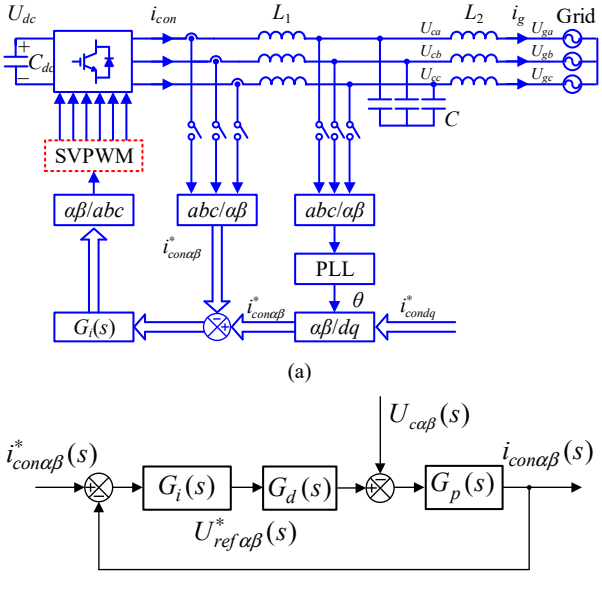

Fig. 1. Single-loop control diagram of a three-phase grid-connected VSC using converter-side current feedback. (a) Diagram of single-loop control, (b) Mathematic model.

II. System Model

The control diagram of a three-phase grid-connected VSC with single-loop converter-side current control is depicted in Fig. 1, where U_{ga}, U_{gb}, U_{gc} are the grid voltages, U_{ca}, U_{cb}, U_{cc} are the filter capacitor voltages, U_{dc} is the dc-link voltage, i_{con} is the converter-side current, i_g is the grid-side current, i^*_{condq} and $i^*_{conαβ}$ are current references in the dq- and $αβ$-frame, L_1 is the converter-side inductance, L_2 is the grid-side inductor, and C is the filter capacitor, respectively. Regarding C and L_2 as

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the grid admittance, only the converter-side inductance needs to be considered and the plant model $G_p(s)$ is

$$G_p(s)=\frac{1}{sL_1}. \tag{1}$$

$G_d(s)$ is the control delay, which is given as

$$G_d(s)=e^{-sT_d}. \tag{2}$$

$G_i(s)$ is the proportional-resonant (PR) controller which is

$$G_i(s)=K_p+K_r\omega_{rc}\frac{s\cos\varphi_g-\omega_g\sin\varphi_g}{s^2+\omega_{rc}s+\omega_g^2} \tag{3}$$

where ω_g, ω_{rc}, φ_g, K_p and K_r are the fundamental angle frequency, the cut-off angle frequency of the resonant controller, the compensation angle of the resonant controller, the proportional gain, and the resonant gain, respectively. Based on Fig. 1(b), the output converter-side current is

$$i_{con}(s)=G_{cl}(s)i_{con}^{*}(s)-Y_o(s)U_c(s) \tag{4}$$

where $G_{cl}(s)$ is the closed-loop transfer function between the reference current and the converter-side current, $Y_o(s)$ is the VSC output admittance.

$$G_{cl}(s)=\frac{G_d(s)G_i(s)}{sL_1+G_d(s)G_i(s)} \tag{5}$$

$$Y_o(s)=\frac{1}{sL_1+G_d(s)G_i(s)}. \tag{6}$$

According to the passivity-based stability theory, a grid-connected VSC can be stabilized if the two constraints are satisfied [3]. First, the closed-loop transfer function $G_{cl}(s)$ should be stable. Usually, the inner stability can be guaranteed by setting a proper bandwidth. Second, the real part of $Y_o(j\omega)$ is non-negative. Since the control delay mainly affects the dissipation in the high-frequency range, the R controller can be temporarily neglected. By substituting '$s=j\omega$' into (6), the real part of VSC output admittance $Re\{Y_o(j\omega)\}$ is given as

$$\mathrm{Re}\{Y_o(j\omega)\}\approx\frac{K_p\cos(\omega T_d)}{(K_p\cos(\omega T_d))^2+(\omega L_1-K_p\sin(\omega T_d))^2}. \tag{7}$$

Then the sign of $Re\{Y_o(j\omega)\}$ is determined by the numerator, and the dissipative region is

$$f_{dissipative}\in(0,\frac{1}{4T_d}). \tag{8}$$

It can be seen that only if the control delay T_d is smaller or equal to $0.25T_{sw}$, the dissipative region can be lifted to the switching frequency. Fig. 2 shows the diagram of regular SS and DS PWM, where the control delay is $1.5T_{sw}$ and $0.75T_{sw}$, respectively. Their non-dissipative regions are given as

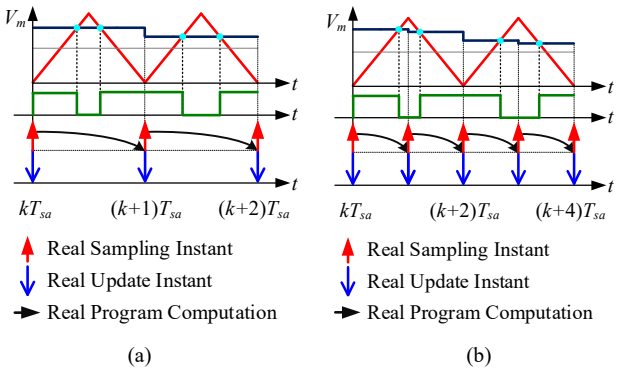

Fig. 2. Regular digital PWM. (a) Single-sampling PWM with one-step computation delay, (b) Double-sampling PWM with one-step computation delay.

$$f_{dissipative\_SS}\in(0,\frac{1}{6}f_{sw}) \tag{9}$$

$$f_{dissipative\_DS}\in(0,\frac{1}{3}f_{sw}). \tag{10}$$

III. Conventional Real-Time-Update PWM

The critical control delay for the dissipation of single-loop ACC is $0.25T_{sw}$, based on this optimization goal, the control delays for the conventional RTU PWM methods are evaluated first. RTU PWM methods using single-sampling include the single-valley-sampling RTU (SVSRTU) PWM and single-peak-sampling RTU (SPSRTU) PWM. Specifically, the average value of current at the peak/valley of the carrier is used for the control, and the calculated duty cycle is loaded in real-time [9-10]. Fig. 3(a) shows the diagram of SVS PWM, based on the voltage-second equivalence, the equivalent update instant is the same as the sampling instant. Then the computation delay is $0T_{sw}$, and only the single-sampling PWM delay $0.5T_{sw}$ remains. The control delay for the SVSRTU PWM is given as

$$\begin{cases} T_{d\_SVSRTU}=\underbrace{0}_{\text{computation delay}}+\underbrace{0.5T_{sw}}_{\text{PWM delay}}=0.5T_{sw} & d\ge d_{cri} \\ T_{d\_SVSRTU}=\underbrace{0.5T_{sw}}_{\text{computation delay}}+\underbrace{0.5T_{sw}}_{\text{PWM delay}}=T_{sw} & d<d_{cri} \end{cases}. \tag{11}$$

However, when the duty cycle is low, as shown in Fig. 3(b), the computation delay increases from 0 to $0.5T_{sw}$, and the control delay increases from $0.5T_{sw}$ to T_{sw}. Based on the geometric principle, the critical duty cycle is determined by the code processing time T_{cp}, which is given as

$$d_{cri}=\frac{2T_{cp}}{T_{sw}}. \tag{12}$$

Substituting (11) to (8), the dissipative region for SVSRTU PWM is given as

$$\begin{cases} f_{dissipative\_SVSRTU}=(0,\frac{1}{2}f_{sw}) & d\ge d_{cri} \\ f_{dissipative\_SVSRTU}=(0,\frac{1}{4}f_{sw}) & d<d_{cri} \end{cases}. \tag{13}$$

It can be seen from (13) that the dissipative region is shrunk when the duty cycle is lower than the critical value.

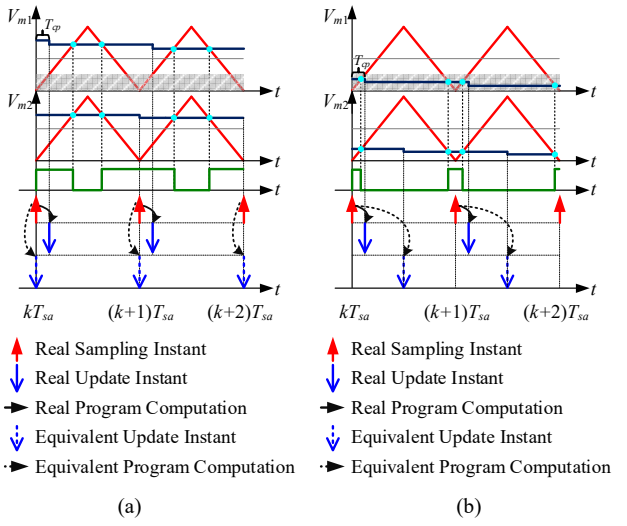

Fig. 3. Single-valley-sampling real-time-upate PWM. (a) Without duty cycle limitation, (b) With duty cycle limitation.

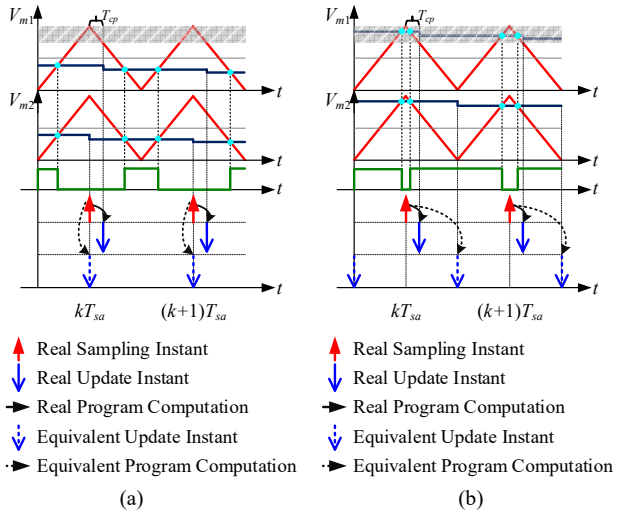

Fig. 4. Single-peak-sampling real-time-update PWM. (a) Without the duty cycle limitation, (b) With the duty cycle limitation.

Compared with the SVSRTU PWM, the sampling instant is located at the peak of the carrier for the SPSRTU PWM. As shown in Fig. 4, the critical duty cycle is

$$d_{cri} = 1 - \frac{2T_{cp}}{T_{sw}}. \tag{14}$$

For the SPSRTU PWM, when the duty cycle is smaller than the critical value, only the single-sampling PWM delay $0.5T_{sw}$ remains and the control delay is given as

$$\begin{cases} T_{d\_SPSRTU} = \underbrace{0}_{\text{computation delay}} + \underbrace{0.5T_{sw}}_{\text{PWM delay}} = 0.5T_{sw} & d \le d_{cri} \\ T_{d\_SPSRTU} = \underbrace{0.5T_{sw}}_{\text{computation delay}} + \underbrace{0.5T_{sw}}_{\text{PWM delay}} = T_{sw} & d > d_{cri} \end{cases}. \tag{15}$$

When the duty cycle is larger than the critical value, the computation delay increases from 0 to $0.5T_{sw}$, and the control delay increases from $0.5T_{sw}$ to T_{sw}. The dissipative region for SPSRTU PWM is given as

$$\begin{cases} f_{dissipative\_SPSRTU} = (0, \frac{1}{2} f_{sw}) & d \le d_{cri} \\ f_{dissipative\_SPSRTU} = (0, \frac{1}{4} f_{sw}) & d > d_{cri} \end{cases}. \tag{16}$$

Combining SVSRTU PWM and SPSRTU PWM, without duty cycle limitation (WDCL) PWM can always maintain the control delay as $0.5T_{sw}$ [3], which is given as

$$T_{d\_WDRL} = \underbrace{0}_{\text{computation delay}} + \underbrace{0.5T_{sw}}_{\text{PWM delay}} = 0.5T_{sw} \tag{17}$$

It can be seen in Fig. 5 that the shaded areas are same in the positive half cycle and negative half cycle of modulation signal. Moreover, the sampling instants will switch between the peak and valley of carrier according to the amplitude of duty cycle. As a result, the dissipation for WDCL PWM can be optimized to $0.5f_{sw}$, which is given as

$$f_{dissipative\_WDRL} = (0, \frac{1}{2} f_{sw}) \tag{18}$$

Note that WDCL PWM cannot strictly be regarded as a single-sampling PWM but as a kind of double-sampling PWM because the sampling instant is switched between the peak and the valley of the carrier. Further, by substituting d_{cri}=0.5 into (12), the maximum allowed computation time for WDCL PWM is $0.25T_{sw}$, which is acceptable for the microprocessors.

Similar to SS RTU PWM, DSRTU PWM can be applied as well [11], where the control delay is $0.25T_{sw}$ when the duty

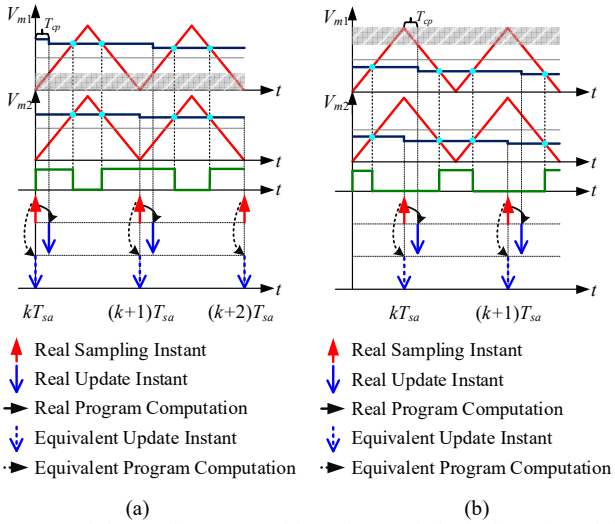

Fig. 5. Real-time-update PWM without duty cycle limitation. (a) Positive half cycle of modulation signal, (b) Negative half cycle of modulation signal.

cycle is smaller than the critical value, as shown in Fig. 6(a). However, when the duty cycle is larger than the critical value (see Fig. 6(b)), DSRTU PWM is the same as the WDCL PWM and the control delay for DSRTU PWM is given as

$$\begin{cases} T_{d\_DSRTU} = \underbrace{0}_{\text{computation delay}} + \underbrace{0.25T_{sw}}_{\text{PWM delay}} \\ \qquad = 0.25T_{sw} \quad \frac{2T_{cp}}{T_{sw}} \le d \le 1 - \frac{2T_{cp}}{T_{sw}} \\ T_{d\_DSRTU} = \underbrace{0}_{\text{computation delay}} + \underbrace{0.5T_{sw}}_{\text{PWM delay}} \\ \qquad = 0.5T_{sw} \quad others \end{cases}. \tag{19}$$

Consequently, the dissipation still cannot be achieved, and the dissipative region is shown as

$$\begin{cases} f_{dissipative\_DSRTU} = (0, f_{sw}) & \frac{2T_{cp}}{T_{sw}} \le d \le 1 - \frac{2T_{cp}}{T_{sw}} \\ f_{dissipative\_DSRTU} = (0, \frac{1}{2} f_{sw}) & others \end{cases} \tag{20}$$

Note that DSRTU PWM can optimize the control delay to the critical delay $0.25T_{sw}$ when the code process time is short enough. For example, if $T_{cp} \le 0.005T_{sw}$, the duty cycle can be in the interval of (0.01, 0.99). In addition, when the duty cycle

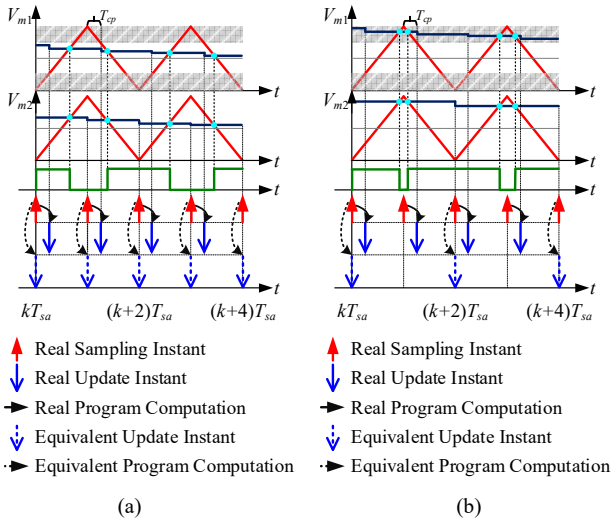

Fig. 6. Double-sampling real-time update PWM. (a) Without the duty cycle limitation, (b) With the duty cycle limitation.

is limited, the control delay can be the same as WDCL PWM. In addition, the maximum allowed computation time decreases from $0.25T_{sw}$ to $0.125T_{sw}$. To summarize, although DSRTU PWM can be a potential candidate to achieve the dissipation below the Nyquist frequency, the requirement for the computation speed of microprocessors is high. Once the duty cycle is limited, the dissipation in the high-frequency range will be jeopardized.

IV. Enhanced Real-Time-Update PWM

To remove the duty cycle limitation of the DSRTU PWM, an ERTU PWM using multi-sampling is proposed in this paper. As shown in Fig. 7(a), the sampling instants are the same as the DSRTU PWM when the duty cycle is lower than the critical value. On the other hand, when the duty cycle is larger than the critical value, the sampling instants are moved to the middle points of the carrier. As shown in Fig. 7(b), the computation delay is $-0.25T_{sw}$ which achieves a phase-leading function. Note that the PWM delay is the same as the SS PWM delay, and the total control delay is $-0.25T_{sw}+0.5T_{sw}=0.25T_{sw}$, which is given as

$$\begin{cases} T_{d\_ERTU\_PWM} = \underbrace{0}_{\text{computation delay}} + \underbrace{0.25T_{sw}}_{\text{PWM delay}} \\ \quad = 0.25T_{sw} \quad \dfrac{2T_{cp}}{T_{sw}} \le d \le 1-\dfrac{2T_{cp}}{T_{sw}} \\ T_{d\_ERTU\_PWM} = \underbrace{-0.25}_{\text{computation delay}} + \underbrace{0.5T_{sw}}_{\text{PWM delay}} \\ \quad = 0.25T_{sw} \quad others \end{cases} \tag{21}$$

Moreover, the negative computation delay concept is inspired by the multi-sampling PWM in [11], which can be regarded as a four-sampling PWM due to the number of used current samples. Consequently, the dissipation can be achieved using single-loop control, which is given as

$$f_{dissipative\_ERTU} = (0,\ f_{sw}) \tag{22}$$

On the other hand, the non-average current is used for the control when the sampling instants are switched to the middle points of the carrier. But the introduced aliased harmonics are minimum compared with the case where the sampling instant is shifted to other points.

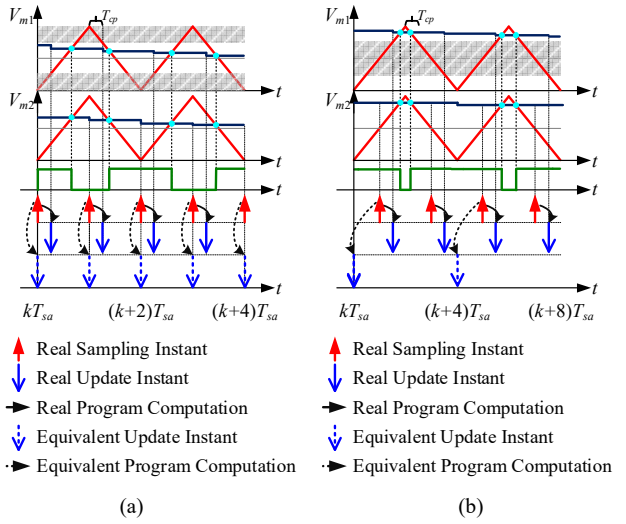

Fig. 7. Enhanced real-time-update PWM with double-sampling. (a) Sampling at Peak/valley point of carrier, (b) Sampling at middle point of carrier.

Especially, when the code processing time is shorter, the duration time using the currents at the middle points of the carrier will be shorter, i.e., the shaded area in Fig. 7(a). Consequently, the aliasing effect caused by the middle points sampling will be weakened. Based on (21), if $T_{cp}=0.25T_{sw}$, ERTU PWM changes back to WDCL PWM. If $T_{cp}=0.125T_{sw}$, the shaded area and the unshaded area in Fig. 7(a) are the same. Therefore, T_{cp} is recommended to $0.0625T_{sw}$ for ERTU PWM, the shaded area occupies 1/4 and the maximum allowed computation time is the same with sixteen-sampling PWM.

TABLE I. Comparison Between Different PWM Methods.

PWM / Index	SVSRTU (see Fig. 3)	SPSRTU (see Fig. 4)	WDCL (see Fig. 5)	DSRTU (see Fig. 6)	MS with an anti-aliasing filter [11]	ERTU (see Fig. 7)
Control delay	$\frac{1}{2}T_{sw}$	$\frac{1}{2}T_{sw}$	$\frac{1}{2}T_{sw}$	$\frac{1}{4}T_{sw}$	$(\frac{1.5}{N}+\frac{1}{4})T_{sw}$	$\frac{1}{4}T_{sw}$
Dissipative region	$(0, \frac{1}{2}f_{sw})$	$(0, \frac{1}{2}f_{sw})$	$(0, \frac{1}{2}f_{sw})$	$(0, f_{sw})$	$(0, \frac{N}{6+N}f_{sw})$	$(0, f_{sw})$
Aliasing	No	No	No	No	No	Small
Duty cycle limitation	Yes	Yes	No	Yes	No	No
Maximum allowed computation time	$\frac{1}{4}T_{sw}$	$\frac{1}{4}T_{sw}$	$\frac{1}{4}T_{sw}$	$\frac{1}{8}T_{sw}$	$\frac{1}{N}T_{sw}$	$\frac{1}{16}T_{sw}$

SVSRTU: Single-valley-sampling real-time-update, SPSRTU: Single-peak-sampling real-time-update, WDCL: Without the duty cycle limitation, DSRTU: Double-sampling real-time-update, MS: Multi-sampling, ERTU: Enhanced real-time-update.

Then the proposed ERTU PWM can not only optimize the control delay to the critical value and achieve the dissipation up the Nyquist frequency, but has also the same computation burden with sixteen-sampling. In addition, ERTU PWM has a constant control delay, which simplifies the system modeling compared with the piecewise control delay in DSRTU PWM. To further clarify the advantage of ERTU PWM, a comparison among various PWM methods is given in Table I, and their priority is given as follows.

(1) If $T_{cp} \le 0.005T_{sw}$, select DSRTU PWM where $T_d = 0.25T_{sw}$ and $d \in (0.01, 0.99)$;

(2) If $0.005T_{sw} < T_{cp} \le T_{sw}/16$, select ERTU PWM where $T_d = 0.25T_{sw}$ and $d \in (0, 1)$;

(3) If $T_{sw}/16 < T_{cp} < T_{sw}/6$, select MS PWM with an anti-aliasing filter where $0.25T_{sw} < T_d < 0.5T_{sw}$ and $d \in (0, 1)$;

(4) If $T_{sw}/6 \le T_{cp} \le 0.25T_{sw}$, select WDCL PWM where $T_d = 0.5T_{sw}$ and $d \in (0, 1)$.

V. Case Studies

To investigate the validity of the proposed method, two cases with different filter capacitances are studied through simulation. Table II gives the parameters of a down-scaled three-phase grid-connected VSC. i^*_{invq} changes from 15 A to −15 A to simulate the duty cycle limitation. For Case 1 with C=3 μF and f_r=2517 Hz, as shown in Fig. 9, the system is not stable with DSRTU PWM because the resonance frequency is located in the non-dissipative region in (20). ERTU PWM can make the system stable instead, which is consistent with the theoretical analysis in Section IV. For case 2 with C=6 μF and f_r=1779 Hz, as shown in Fig. 10, the system can be stable for DSRTU PWM and ERTU PWM, and the grid-side current quality is similar.

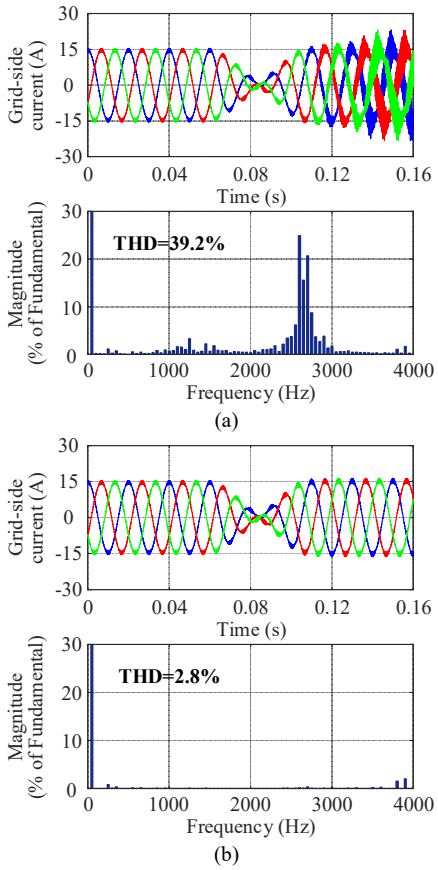

Fig. 8. Simulation results of Case 1 (C=3 μF and f_r=2517 Hz). (a) Double-sampling real-time-update PWM, (b) Enhanced real-time-update PWM.

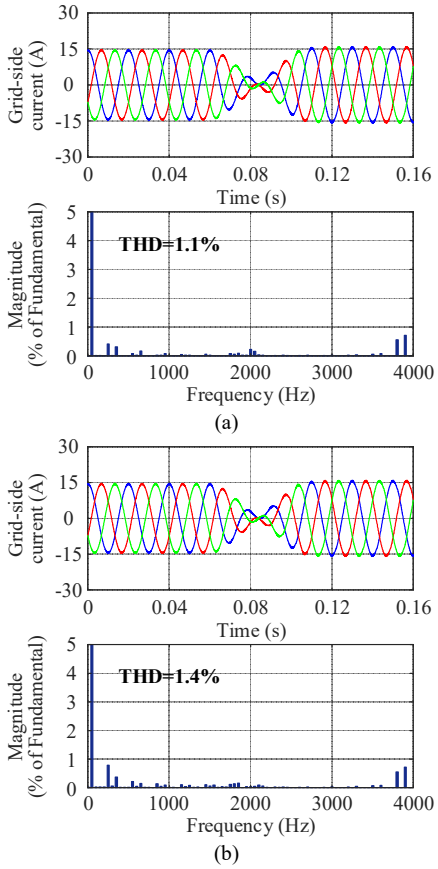

Fig. 9. Simulation results of Case 2 (C=6 μF and f_r=1779 Hz). (a) Double-sampling real-time-update PWM, (b) Enhanced real-time-update PWM.

TABLE II. PARAMETERS OF A THREE-PHASE GRID-CONNECTED VSC

Symbol	Description	Value	Symbol	Description	Value
P_o	Output power	7 kW	U_{grms}	Grid voltage	220 V
U_{dc}	DC-link voltage	700 V	L_1	Converter-side inductance	4 mH
L_2	Grid-side inductance	2 mH	C	Filter capacitance	3/6 μF (Case 1/Case 2)
f_{sw}	Switching frequency	4 kHz	T_{cp}	Computation time	T_{sw} /16
K_p	Proportional coefficient	20	K_r	Resonant coefficient	1000

VI. CONCLUSION

This paper investigates the duty cycle limitation phenomenon when using RTU PWM. It is revealed that the control delay will increase when the duty cycle is larger than the critical value, which jeopardizes high-frequency dissipation. In order to optimize the control delay to the critical value ($0.25T_{sw}$), an enhanced RTU PWM is proposed by switching the sampling instants when the duty cycle is limited. Consequently, the control delay can always be kept to the critical value and the dissipation is achieved up to the Nyquist frequency. Finally, the proposed method is validated through simulation.

REFERENCES

[1] F. Blaabjerg, Y. Yang, D. Yang, and X. Wang, "Distributed power generation systems and protection," *Proc. IEEE*, vol. 105, no. 7, pp. 1311-1331, July 2017.

[2] X. Wang and F. Blaabjerg, "Harmonic stability in power electronic-based power systems: concept, modeling, and analysis," *IEEE Trans. Smart Grid*, vol. 10, no. 3, pp. 2858-2870, May 2019.

[3] L. Harnefors, X. Wang, A. Yepes, and F. Blaabjerg, "Passivity-based stability assessment of grid-connected VSCs-An overview," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 1, pp. 116–125, Mar. 2016.

[4] C. Wang, X. Wang, Y. He, and X. Ruan, "A Passivity-Based Weighted Proportional-Derivative Feedforward Scheme for Grid-Connected Inverters with Enhanced Harmonic Rejection Ability," *IEEE J. Emerg. Sel. Top. Power Electron.*, *early access*, 2022.

[5] X. Wang, F. Blaabjerg, and P. Loh, "Passivity-based stability analysis and damping injection for multiparalleled VSCs with LCL filters," *IEEE Trans. Power Electron*., vol. 32, no. 11, pp. 8922-8935, Nov. 2017.

[6] A. Akhavan, J. C. Vasquez, and J. M. Guerrero, "A simple method for passivity enhancement of current controlled grid-connected inverters," *IEEE Trans. Power Electron*., vol. 35, no. 8, pp. 7735–7741, 2020.

[7] M. Awal, W. Yu, and I. Husain, "Passivity-based predictive-resonant current control for resonance damping in LCL-equipped VSCs," *IEEE Trans. Ind. Appl*., vol. 56, no. 2, pp. 1702–1713, 2020.

[8] D. Pan, X. Ruan, C. Bao, W. Li, and X. Wang, "Capacitor-current-feedback active damping with reduced computation delay for improving robustness of LCL-type grid-connected inverter," *IEEE Trans. Power Electron*, vol. 29, no. 7, pp. 3414-3427, July 2014.

[9] M. Hu, W. Hua, H. Xiao, Z. Wang, K. Liu, K. Cai, and Y. Wang "Fast current control without computational delay by minimizing update latency," *IEEE Trans. Power Electron*., vol. 36, no. 11, pp. 12207–12212, Nov. 2021.

[10] G. Bonanno and L. Corradini, "Digital predictive current-mode control of three-level flying capacitor buck converters," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4697–4710, Apr. 2021.

[11] S. He, D. Zhou, X. Wang, and F. Blaabjerg, "Aliasing suppression of multi-sampled current controlled LCL-filtered inverters," *IEEE Trans. Journal Emerg. Sel. Topics Power Electron.*, vol. 10, no. 2, pp. 2411-2423, April 2022.