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Parallel Connection of Silicon Carbide MOSFETs—Challenges, Mechanism, and Solutions

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***Abstract*—Power semiconductor devices are often connected in parallel to increase the current rating of the power conversion systems. However, due to mismatched circuit parameters or semiconductor fabrication discrepancies, the current of paralleled power semiconductor devices can be unbalanced, which potentially leads to accelerated aging and long-term reliability issues. The fast-switching speed of silicon carbide (SiC) devices aggravates this problem due to its higher sensitivity to parasitic parameters. Numerous efforts have been dedicated to analyzing and addressing the current imbalance issue of paralleling SiC devices. This article comprehensively summarizes and presents state-of-the-art research regarding the current imbalance in paralleled SiC devices. Degree of imbalance is proposed to comprehensively quantify the current mismatch. Starting with mechanism analysis, different types of current imbalance are categorized. Various device parameters and the package layout that impact the current distribution are investigated. The existing solutions including passive methods and active methods are concluded and categorized. This work also incorporates insight into the future development needs of high-power multichip SiC module packaging and driving technologies.**

***Index Terms*—Current imbalance, multichip power module, parallel connection, SiC metal oxide semiconductor field effect transistor (MOSFET).**

I. Introduction

SILICON carbide (SiC) metal oxide semiconductor field effect transistor (MOSFET) devices have been undergoing rapid development in the past decade and a fast growth rate is forecasted in the next two decades due to the booming market of electric vehicles (EVs). SiC MOSFET is considered a preferred option in the EV powertrain inverter application, not only by academia [1], [2] but also by the mainstream automotive industry [3], [4], [5], due to its low device losses, high system efficiency, and most importantly the lower cost at the vehicle level. As the automotive market is enormous and extremely cost-sensitive, SiC MOSFET technology is supposed to enjoy massive investment, rapid technology iteration [6], [7], [8], [9], [10], as well as significant further cost reduction in the next 5–10 years [11], [12], [13]. As a result of technology improvements and cost reduction, other industrial markets, e.g., photovoltaic, energy storage, charging infrastructure [14], traction [15], [16], and power grid, also expect to see a high-level market penetration of SiC devices [17], [18].

Compared with silicon (Si) insulated gate bipolar transistors (IGBTs), SiC MOSFETS s feature several device superiorities: fast switching speed, high operating temperature, high breakdown voltage [19], [20], and linear current–voltage (I–V) properties These device superiorities benefit from both SiC material properties and MOSFET unipolar device structure. The SiC wide band gap (WBG) material property enables higher temperature operation [21] and a higher critical electric field. Currently, the automotive market is pushing the highest operation junction temperature from 175 °C to 200 °C, which is not hurdled by SiC material but mainly by the MOSFET gate oxide reliability [22], [23], [24], [25]. The higher critical electric field of SiC material allows a much higher doping concentration and thinner drift layer, therefore, leading to much lower specific resistance in the drift region [26]. As a consequence, a 1.2 or 1.7 kV unipolar MOSFET device is easily achieved with SiC material but not quite feasible with Si material due to the high specific resistance of the drift region [27]. At present, up to 1.7 kV SiC MOSFET, the epitaxial layer thickness is approximately 1 μm/100 V, while for Si IGBT, the Si wafer thickness is about 10 times larger. The unipolar MOSFET structure naturally leads to a fast-switching speed and a linear I–V property, compared to the bipolar IGBT structure [28], which is beneficial to conduction losses at light load applications. Last but not least, unipolar MOSFET structure also results in a lower switching loss compared to bipolar IGBTs due to the absence of tail current.

While enjoying the aforementioned device superiorities of SiC MOSFETS, there are still several challenges that are impeding SiC MOSFETS from walking over the last mile into massive market applications. From the perspective of material, SiC substrate and epitaxy still have multiple defective issues (micro-pipe, dislocation, stacking fault) [29]. The material defects further impact SiC device properties, yield, as well as the maximum device size of a single chip. The immaturity of manufacturing equipment, process, and device design for SiC devices also results in a larger inconsistency of SiC device parameters. From the device level,

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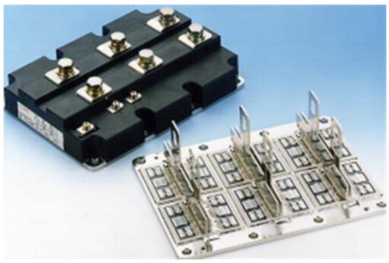


Fig. 1. IGBT-high-current-module with paralleled IGBTs and diodes.

SiC MOSFETS are still confronting the challenges of gate oxide reliability and threshold voltage ($V_{\rm th}$) instability [30], [31], [32]. Along with the fast-switching speed benefit, it also results in high sensitivity to circuit parasitics [33], [34], [35], which poses additional challenges to the design of SiC power semiconductor packaging, gate driver, and power loop circuit layout.

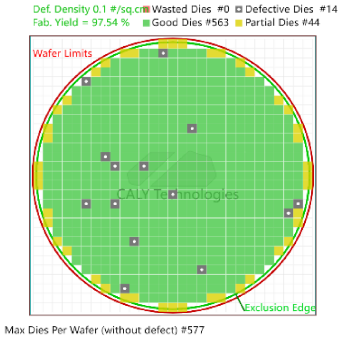
In addition to the SiC material immaturity, device parameters inconsistency, and fast switching speed, the current imbalance among the paralleled SiC MOSFETS has been a practical issue for the high current application of SiC MOSFETS. In normal operating conditions, the current imbalance could lead to thermal imbalance, as well as long-term reliability concerns. Due to the current imbalance, the design margin is normally set to a high level to avoid significant excessive stress on a single device, whereas it means less utilization of the device's full potential and a higher cost.

To tackle the challenges of paralleling SiC MOSFETS, there has been an increasing amount of research work in the last decade. The research works could be classified into two categories: the investigation of the current imbalance mechanism and current sharing methodologies. This article tries to put together state-of-the-art research regarding paralleling SiC MOSFETS comprehensively. First, it explains the reasons why paralleling SiC MOSFETS is more challenging than paralleling Si IGBTs, from material defects to process immaturity and applications: smaller single die size, larger device parameters inconsistency, and faster switching speed [36], [37], [38]. Second, it describes the current imbalance mechanism, including both static and dynamic imbalances. Third, the summary of current imbalance mitigation methodologies is presented. Among the methods, there are passive mitigation methods including circuit layout design optimization and device screening measures, and active methods such as utilizing external passives and active gate drivers [39]. Following the mitigation methods, it gives insights of circuit/multichip power module designs and the application of active gate driver control to minimize the current imbalance. The final section concludes the article.

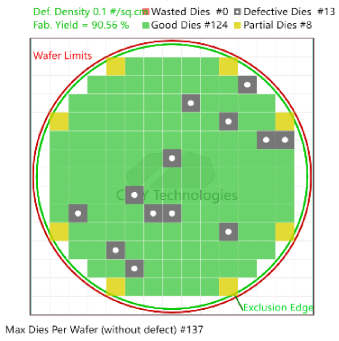
II. Challenges of Paralleling SiC MOSFETs

Paralleling power semiconductors are common at various levels.

1) At the die level, a SiC mosfet chip consists of thousands of semiconductor unit cells connecting in parallel via the drain/source metallization layers and gate runners.



(a)



(b)

Fig. 2. 6-inch wafer for the dies under different sizes. (a) 5 × 5 mm die size. (b) 10 × 10 mm die size.

2) At the module level, paralleling power semiconductor dies in multichip power modules or paralleling discrete devices is a common approach to achieve a high current rating in high-power applications. For instance, the power module in Fig. 1 has a 3600 A rated current with twenty-four IGBT chips and twelve diode chips in parallel.
3) At the circuit level, for some high-current and high-power applications, parallel connection of multiple power modules is also employed to achieve the desired current level.

A. Challenges Associated With Small Dies of SiC MOSFETs

To further increase the current rating of a power device, it is desired to fabricate a larger die. However, several issues hinder the further increase of the die size. There is a design tradeoff between the die size and the yield. Due to SiC material defects and process imperfection, a larger die size normally means lower yield, which in turn results in a higher cost/Ampere. Fig. 2 compares the yield difference between 5 × 5 and 10 × 10 mm die size on a 6-inch wafer, which indicates that the yield is reduced significantly from 97.54% to 90.56% with the same defect density.

Compared to a Si IGBT, it is more challenging to make a large die for a SiC MOSFET. SiC substrate and epitaxial material have higher-level level defects than their Si counterparts due to their material properties [40]. In addition, the SiC MOSFET manufacturing equipment and process control are not as mature as those for Si IGBTs. At present, for lower voltage ($\leq$750 V) Si IGBTs, the maximum current rating of a single IGBT chip is around 300 A with a die size of 10 × 12 mm^2. While for the

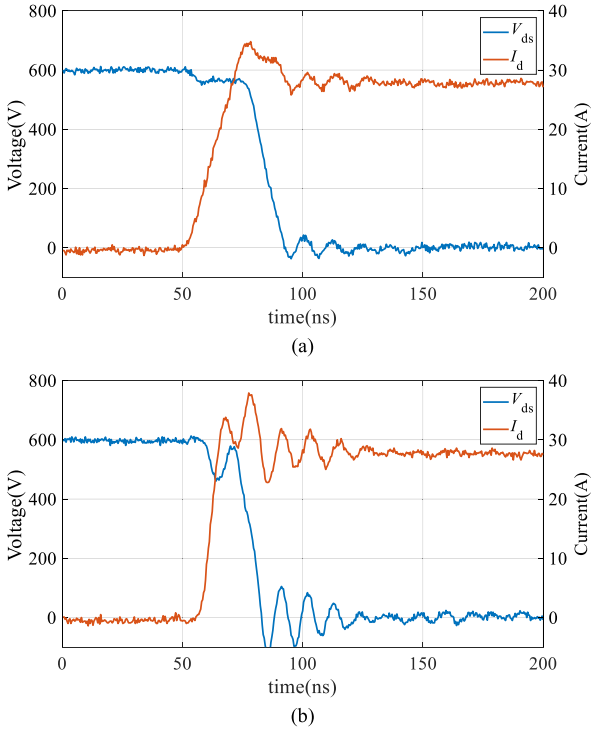


Fig. 3. Comparison of experimental switching waveform under different switching slew rates. (a) Waveform when d*i*/d*t* is 2 A/ns. (b) Waveform when d*i*/d*t* is 6 A/ns.

SiC MOSFETS of the same voltage level, the maximum current rating of a single SiC MOSFET die is approximately 100 A with a 5×5 mm^2 die size. For the same current rating, it is necessary to parallel more SiC MOSFET dies than using Si IGBT. Since more dies are connected in parallel when using SiC MOSFET, the level of device electrical parameters' variations among the paralleled chips can increase. Therefore, it can lead to higher risks of current imbalance [41].

B. Challenges Due to Large Device Parameter Variations

Another challenge for paralleling SiC MOSFETS is also associated with the less maturity of the SiC MOSFET manufacturing process, which not only leads to low yield but also results in a larger variance of the device parameters. Datasheets of SiC MOSFETS specify high variation limits of the characteristics of the chip. The inconsistency of device parameters, e.g., ON-resistance (R_{dson}), transconductance (g_{fs}), and V_{th} could lead to current imbalance during steady state and switching transient.

C. Challenges Due to Fast Switching Speed

In addition to the limited die size and device parameters' inconsistency, the fast-switching speed associated with the unipolar MOSFET structure also needs additional attention. Fast switching speed means high sensitivity to parasitic parameters since it can interact with the parasitic inductance and generate ringings, overshoot, and false-triggering. Fig. 3 is the waveform of the same circuit under different switching speeds [34] which shows that the ringing increases while the d*i*/d*t* increases from 2 to 6 A/ns. In Fig. 3, V_{ds} is the drain–source voltage and I_{d} is the drain current.

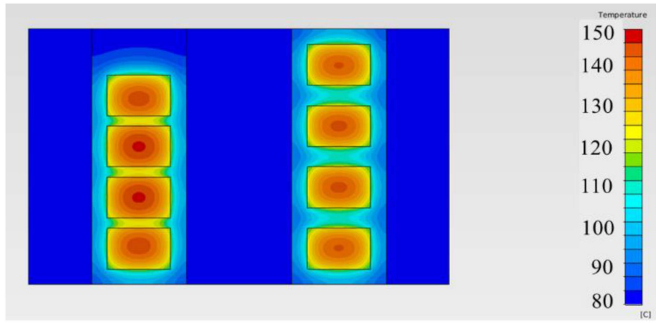


Fig. 4. Thermal performance with different distances among paralleled dies.

D. Challenges From Designing Multidiscipline of Multichip Power Modules

Another challenge for multichip power module design is its highly multidiscipline characteristic. The "optimal" design solution is often a compromised result between various aspects such as electrical, mechanical, thermal, environmental, reliability, and manufacturability [42]. In general, the design principles from different aspects are usually paradoxical. A simple example is that the distance between the paralleled chip is expected to be larger for better thermal performance, but smaller for better electrical performance [43]. Fig. 4 compares the thermal simulation of two groups of paralleled dies with different distances. It is apparent that the four MOSFETS with larger space, i.e., the right ones, have lower junction temperatures but larger stray inductance among the loops.

Apart from the tradeoff from different design principles, the performance from different aspects (e.g., electrical, thermal, mechanical) is highly coupled. For paralleled power devices, the current imbalance among paralleled devices may lead to mismatched thermal distribution, mechanical performance, and finally reliability issues. Consequently, there is no cure-all solution for the optimization of the current imbalance among the paralleled dies. Prior to mitigating the current imbalance, it is necessary to conduct an in-depth investigation into the mechanisms of the current imbalance.

III. Categories of Current Imbalance and Possible Consequences

In general, the current imbalance can be categorized into two types: static and dynamic [44]. Static imbalance can lead to mismatched conduction losses while dynamic imbalance can lead to unequal switching losses and I_{d} peak which are pertinent to the current stress. Herein, Zhao's degree of imbalance concept is introduced.

A. Static Degree of Imbalance

Static imbalance is usually induced by the mismatched ON-state resistance R_{dson}. For power MOSFETS, the current is proportional to the conductance. The current on the kth MOSFET $I_{\mathrm{d}k}$

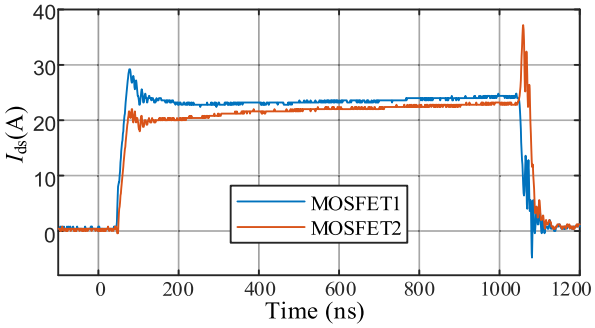


Fig. 5. Experimental waveform of steady-state current imbalance.

is determined by its ON-state-resistance $R_{\mathrm{dson}k}$ as given in the following:

$$I_{\mathrm{d}k} = \frac{1/R_{\mathrm{dson}k}}{1/R_{\mathrm{dson1}} + 1/R_{\mathrm{dson2}} + \ldots 1/R_{\mathrm{dson}-n}} I_{\mathrm{o}}. \quad (1)$$

In (1), n is the total number of MOSFETS in parallel and I_{o} is the total load current. Herein, $I_{\mathrm{o}} = I_{\mathrm{d1}} + I_{\mathrm{d2}} + \ldots I_{\mathrm{d}n}$. A typical waveform of two parallel-connected MOSFETS with the same model number is shown in Fig. 5. It still shows a slightly mismatched static current.

For paralleled MOSFETS, V_{ds} on each MOSFET is equal. According to $V_{\mathrm{ds}} = R_{\mathrm{dson}} I_{\mathrm{d}}$, the MOSFET with lower R_{dson} has higher current I_{d}. Because conduction loss can be calculated with $P_{\mathrm{cond}} = V_{\mathrm{ds}} I_{\mathrm{d}}$, the MOSFET with lower R_{dson} withstands higher conduction losses and junction temperature. The static imbalance is usually not catastrophic due to the positive temperature coefficient of R_{dson}.

To quantify the current imbalance, in this article, *the Degree of Imbalance* (*DoI*) is introduced. *s*DoI which denotes the DoI for static current can be calculated with the following:

$$\begin{aligned} s\mathrm{DoI} = \sum |I_{dj} - I_{dk}| \\ |I_{\mathrm{d1}} - I_{\mathrm{d2}}| + |I_{\mathrm{d1}} - I_{\mathrm{d3}}| + |I_{\mathrm{d1}} - I_{\mathrm{d4}}| + \ldots |I_{\mathrm{d1}} - I_{\mathrm{dn}}| \\ + |I_{\mathrm{d2}} - I_{\mathrm{d3}}| + |I_{\mathrm{d2}} - I_{\mathrm{d4}}| + \ldots |I_{\mathrm{d2}} - I_{\mathrm{dn}}| \\ + \ldots\ldots \\ |I_{\mathrm{d}k} - I_{\mathrm{d}k+1}| + \ldots |I_{\mathrm{d}k} - I_{\mathrm{dn}}| \\ + \ldots\ldots \\ + |I_{\mathrm{d}n-1} - I_{\mathrm{dn}}| \\ = \frac{}{(n-1)(|I_{\mathrm{d1}}| + |I_{\mathrm{d2}}| + \ldots |I_{\mathrm{dn}}|)}. \end{aligned} \quad (2)$$

*s*DoI is an indicator between zero and one. In (2), k and j denote the kth and jth paralleling route respectively and $j \neq k$. n means the number of MOSFETS in parallel. It is an integer no less than 2, i.e., $n \geq 2$. The scenario when s*DoI* equals one is the most extreme condition since all I_{o} is withstood by a single MOSFET and the I_{d} of the other MOSFETS is zero. When sDoI equals zero, the I_{d} on all MOSFETS is completely matched.

B. Dynamic Degree of Imbalance

Dynamic imbalance occurs due to the mismatching switching trajectory which is brought by various factors such as mismatched stray inductance, gate resistance R_{g}, V_{th}, etc. [45]. Theoretically, the dynamic imbalance can be equivalent to the combinations of two special cases: 1) synchronous gate signal and different slew rate; and 2) Asynchronous gate signal and same slew rate. The turn-ON switching profiles of the two special cases are plotted in Fig. 6. M1 and M2 are the two MOSFETS under test. Since the V_{ds} of the paralleled MOSFETS is similar, the switching loss is dominated by I_{d}.

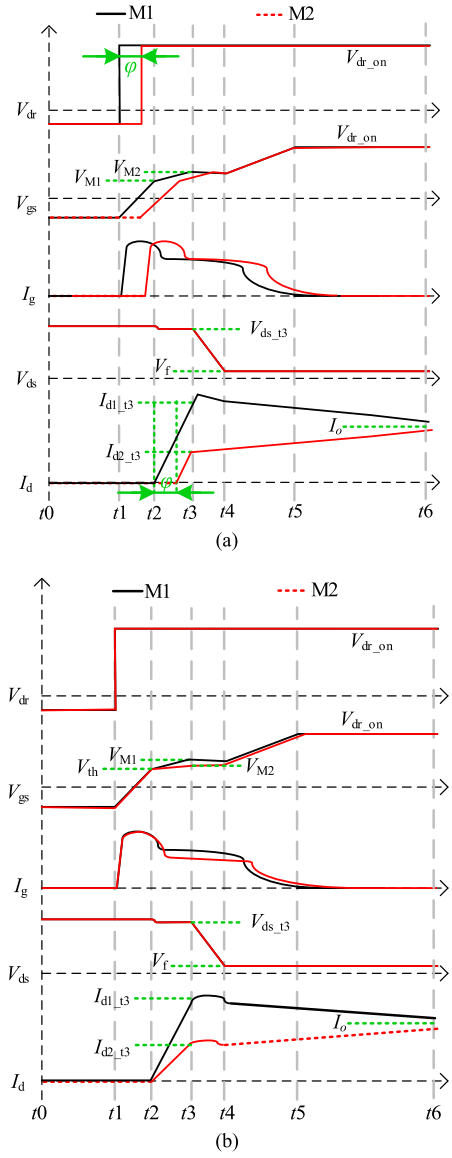


Fig. 6. Turn-ON process of the two special cases of parallel-connected MOSFETS. (a) Asynchronous gate signal and same switching slew rate. (b) Synchronous gate signal and different slew rate [47].

Fig. 6(a) shows the turn-ON process trajectory with an asynchronous gate signal and the same switching slew rate. In this case, two MOSFETS have the same switching slew rate while the gate signal of M1 lags behind M2 for φ. The gate signal lag is usually introduced by the gate driver propagation delay [47]. V_{dr} is the output voltage of the gate driver. Since the turn-ON signal of M1 is earlier than M2, the peak current of M1, i.e., $I_{\mathrm{d1\_t3}}$, is different from that of M2 $I_{\mathrm{d2\_t3}}$. It is apparent that M1 undergoes a higher current than M2. The difference between $I_{\mathrm{d1\_t3}}$ and $I_{\mathrm{d2\_t3}}$ will increase as the delay time φ increases.

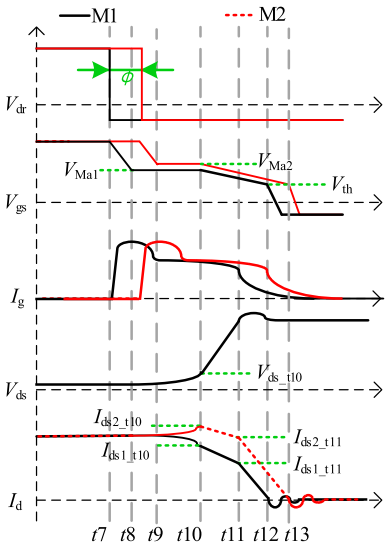


Fig. 7. Turn-OFF process of the two parallel-connected MOSFETs [47].

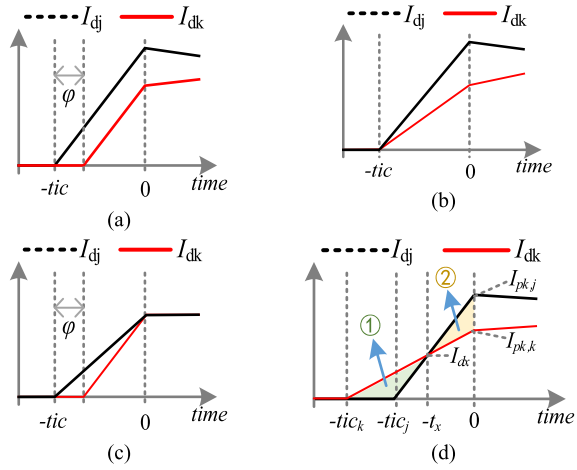


Fig. 8. Turn-ON process of the two paralleled MOSFETs. (a) Nonintersect conditions 1: asynchronous gate signal and same switching slew rate. (b) Nonintersect conditions 2: synchronous gate signal and different switching slew rate. (c) Nonintersect conditions 3: asynchronous gate signal and different switching slew rate. (d) Intersect condition.

If the overshoot current is neglected, $I_{d1\_t3}+I_{d2\_t3} = 2I_o$. The most unbalanced condition occurs when I_{d2_t3} is zero. In this situation, M2 operates in soft turn-ON mode. All the current stress and energy loss are undergone by M1.

Fig. 6(b) shows the turn-ON process trajectory with a synchronous gate signal but a different switching slew rate. In this situation, the I_d of M1 and M2 start to rise at the same time when the while the switching transient of M1 is faster than M2. The different slew rate is introduced by the mismatching electrical parameters of the devices such as C_{gd}, $V_{th,}$ etc. Since M1 switches faster, it withstands higher current stress and overshoot.

The analysis of the turn-OFF process is similar. The two MOSFETS turn OFF with the same switching slew rate while M2 lags behind M1 for φ as plotted in Fig. 7. During the turn-OFF process, M1 withstands less current stress and it operates under quasi-soft-turn-OFF mode. Accordingly, more switching loss is undergone by M2.

Similar to *sDoI*, the concept of dynamic degree of imbalance, i.e., *d*DoI, is introduced as given in (3). Generally, the two variables-of-interest during switching are d*i*/d*t* and peak I_d. Since the V_{ds} is similar, peak I_d indicates the safe-operation while both d*i*/d*t* and peak I_d determine the switching loss. If the d*i*/d*t* and peak I_d of the parallel-connected MOSFETS are equal, it can be claimed that these MOSFETS are balanced. *d*DoI can be defined with the following:

$$d\mathrm{DoI} = \frac{\sum_{j,k=1}^{n}\int_0^{tic}(|I_{dj}-I_{dk}|)\mathrm{d}t}{(n-1)\sum_{j=1}^{n}\int_0^{tic}|I_{dj}|\mathrm{d}t} = \frac{\int_0^{tic}\begin{pmatrix}|I_{d1}-I_{d2}|+|I_{d1}-I_{d3}|+|I_{d1}-I_{d4}|+\ldots|I_{d1}-I_{dn}|\\ +|I_{d2}-I_{d3}|+|I_{d2}-I_{d4}|+\ldots|I_{d2}-I_{dn}|\\ +\ldots\ldots\\ |I_{dk}-I_{dk+1}|+\ldots|I_{dk}-I_{dn}|\\ +\ldots\ldots\\ +|I_{dn-1}-I_{dn}|\end{pmatrix}\mathrm{d}t}{(n-1)\int_0^{tic}(|I_{d1}|+|I_{d2}|+\ldots|I_{dn}|)dt}. \quad (3)$$

In (3), *k* and *j* denote the *k*th and *j*th paralleling route, respectively, and $j \neq k$. $I_{d1} - I_{dn}$ denote the I_d of each MOSFET during current changing substage. *tic* is the duration of drain current rising, i.e., *t*2 to *t*3 in Fig. 6(a). For the turn-OFF process, *tic* starts at the beginning of V_{ds} rising and ends when the total I_d reduces to zero, i.e., *t*10 to *t*13 in Fig. 7.

Considering that the integral is usually difficult to be calculated, (3) can be further simplified. Generally, the current changing process can be linearized to a first-order function [48]. In this case, there are three critical indicators: d*i*/d*t*, *tic*, and start moment. First, the denominator can be simplified as given in the following:

$$\int_0^{tic}(|I_{d1}|+|I_{d2}|+\ldots|I_{dn}|)\,dt = 0.5\left(\left|\frac{\mathrm{d}i_1}{\mathrm{d}t}\right|tic_1^2+\left|\frac{\mathrm{d}i_2}{\mathrm{d}t}\right|tic_2^2\ldots+\left|\frac{\mathrm{d}i_n}{\mathrm{d}t}\right|tic_n^2\right). \quad (4)$$

Second, the simplified calculation of nominator, i.e., $\int_0^{tic}|I_{dk}-I_{dj}|\mathrm{d}t$ is based on the practical condition. Generally, there are two basic conditions: the intersect condition and the nonintersect condition.

Fig. 8(a)–(c) show the current waveform of three typical types of nonintersect conditions which is defined when the I_{dj} and I_{dk} do not intersect in the range of 10%–90% of peak current. In this condition, the integral value can be easily obtained with

$$\int_0^{tic}(|I_{dj}-I_{dk}|)\,\mathrm{d}t = \frac{1}{2}\left|\left|\frac{\mathrm{d}i_j}{\mathrm{d}t}\right|tic_j^2-\left|\frac{\mathrm{d}i_k}{\mathrm{d}t}\right|tic_k^2\right|. \quad (5)$$

Fig. 8(d) shows the current waveform of intersect condition. In this condition, the current I_{dj} and I_{dk} intersect at the point (-t_x, I_{dx}) which locates in the range of 10% to 90% of peak current.

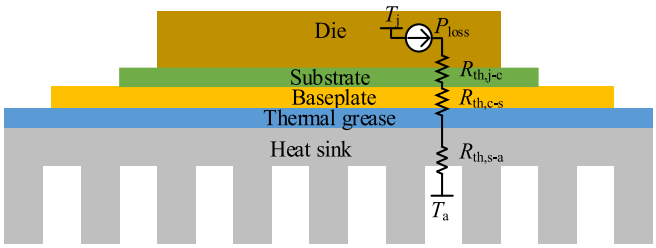


Fig. 9. Thermal network of a bottom-side cooling power device [1].

Peak currents of I_{dj} and I_{dk} are denoted by $I_{pk,j}$ and $I_{pk,k}$, respectively. The calculation of $\int_0^{tic}(|I_{dj}-I_{dk}|)dt$is actually the area of region ① and ② in Fig. 8(d). It can be calculated with the following:

$$\int_0^{tic}\left(|I_{dj}-I_{dk}|\right)\mathrm{d}t = \frac{1}{2}\left(tic_j-tic_k\right)I_{dx}+\frac{1}{2}t_x\left(I_{pk,j}-I_{pk,k}\right). \quad (6)$$

t_x and I_{dx} can be inspected from the oscilloscope. It can be also calculated with di/dt and the current rising time of each current as given in the following:

$$\begin{cases} t_x = \frac{\frac{di_j}{dt}tic_j-\frac{di_k}{dt}tic_k}{di_j/dt-di_k/dt} \\ I_{dx} = \frac{di_j}{dt}\frac{di_k}{dt}\frac{tic_k-tic_j}{di_j/dt-di_k/dt}. \end{cases} \quad (7)$$

C. Thermal Imbalance and Long-Term Reliability

The current mismatch can lead to a thermal imbalance and raise long-term reliability concerns. It can be analyzed as below. The total power loss of a MOSFET can be divided into the conduction loss and switching loss as given in the following [49]:

$$P_{loss} = \frac{V_{ds}^2}{R_{dson}} + f_{sw}\int V_{ds}I_d\mathrm{d}t. \quad (8)$$

From (8), the static current imbalance can lead to mismatched conduction loss which is proportional to the steady-state I_d of the power device. Also, the switching power loss is proportional to the switching frequency and the switching energy loss. The equivalent thermal network of a bottom-side cooling power device can be drawn as shown in Fig. 9 [1].

In Fig. 9, P_{loss} denotes the total power loss of the SiC MOSFET. $R_{th,j-c}$ is the thermal resistance and capacitance from the junction to the case, respectively, which can be found in the Z_{th} plot of the datasheet, while $R_{th,c-s}$ and $C_{th,c-s}$ denote those from the case to the surface of the heatsink. s-a denotes the surface to the ambient thermal impedance. T_a is the ambient temperature of the system and T_c is the temperature of the case. Thus, the calculation of junction temperature T_j of the SiC device can be referred to the following:

$$T_j = P_{loss}\left(R_{th,j-c}+R_{th,c-s}+R_{th,s-a}\right)+T_a. \quad (9)$$

From (9), T_j is proportional to the power loss. Both the mismatching R_{th} and power loss on the parallel-connected MOSFETS can lead to the T_j difference which has a significant impact on lifetime. A simulation study is conducted with a power factor correction (PFC) converter. Two paralleled SiC MOSFETS with different R_{dson} are utilized and their T_j profiles are shown in Fig. 10. The normal operation of an inverter can inevitably introduce a T_j cycle due to the sinusoidal load current. This results in power loss fluctuation and finally the junction temperature fluctuation, i.e., ΔT_j.

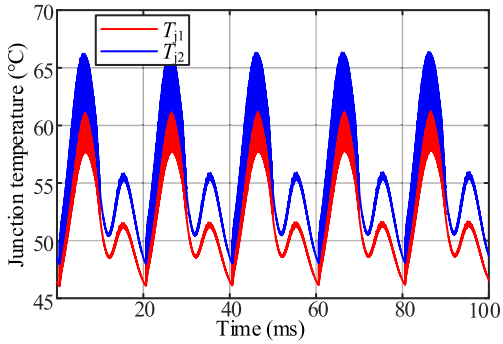


Fig. 10. T_j profile of paralleled SiC MOSFETs in a PFC.

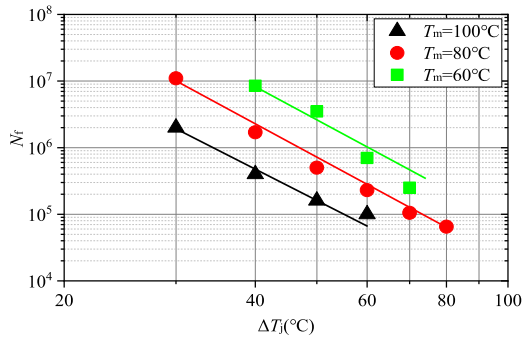


Fig. 11. Relationship between the number of life cycles and junction temperature.

Most failures of the power devices occur on the mechanical parts due to periodical expansion/shrinking. Specifically, the coefficients of thermal expansion of the semiconductor dies, bonding wire, solder and direct bonding copper layer are different [50]. The solder layer between the die and direct bond copper layer and the bonding wires undergo a large periodical force brought by the temperature cycling fluctuation. The accumulated fatigue can result in delamination of the die attach and bonding wire damage [51]. The lifetime power cycles of a power device N_f versus ΔT_j can be quantified with the Coffin–Manson model in the following and plotted in Fig. 11 [52]:

$$N_f = A\cdot(\Delta T_j)^{\alpha}\cdot e^{E_a/(k_B\cdot T_m)}. \quad (10)$$

In (10), A, α, and E_a are defined as the coefficients obtained from experimental results, and k_B which is Boltzmann's constant equals to 1.38×10^{-23} J/K.

When the current imbalance occurs, the mismatched power loss can lead to different T_j on the paralleled MOSFETS [53]. Finally, the MOSFETS that withstand larger ΔT_j in paralleled devices age first and the reliability of the system reduces [54]. Therefore, the current imbalance can speed up the aging process of a system with paralleled devices [55].

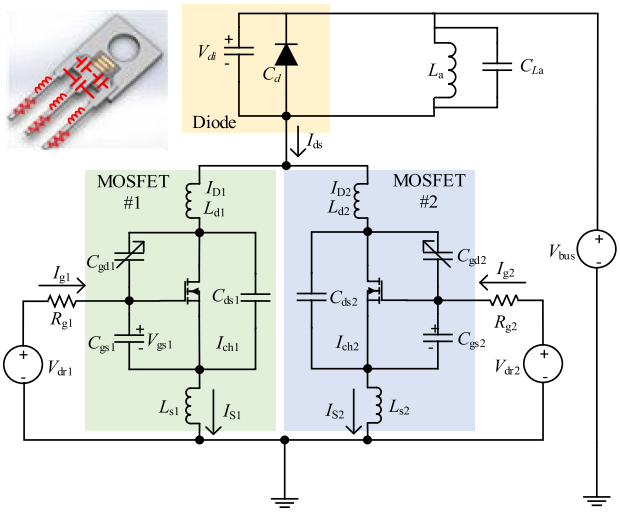


Fig. 12. Equivalent circuit of the parallel-connected power devices.

IV. Mechanism of Current Imbalance

Prior to proposing current sharing strategies, an investigation of the current imbalance mechanism should be conducted. Various parameters that induce the current distribution are usually coupled. This section will discuss the impact of pertinent parameters on the current distribution.

A. Pertinent Parameters

The equivalent circuit of the paralleled power devices is given in Fig. 12 [45]. The parameters in Fig. 12 which have an impact on the current distribution can be categorized into three types: device parameters [55], circuit parameters [56], and status indicators. The intrinsic electric parameters, which are the parameters of the die, are generally determined amid the die fabrication process [57]. It includes the junction capacitance [58], internal gate resistance, transconductance, etc. The external parameters include the parasitic inductance introduced by the package stray, bonding wires, PCB, and cables [59]. The status indicators denote the parameters pertinent to statuses such as T_j, humidity, load current, and dc bus voltage. Some typical parameters can be summarized as shown in Table I. Some equivalent parameters are highly coupled such as V_{th} versus R_{dson}, and T_j versus R_{dson} [60]. Also, some parameters only impact one type of current imbalance. For instance, R_{dson} only affects static current distribution while C_{gs} only influences dynamic distribution. Some parameters such as V_{gs} and T_j can affect both static and dynamic current distribution.

B. Device Parameters Variations

1) R_{dson} Variation: The current on the two paralleled MOSFETS is proportional to the conductance of the MOSFET as given in (1) and their R_{dson} can be calculated with the following:

$$\begin{cases} R_{ds1\_on} = \frac{L}{W\mu_n C_{ox}(V_{gs1}-V_{th1})} \\ R_{ds2\_on} = \frac{L}{W\mu_n C_{ox}(V_{gs2}-V_{th2})}. \end{cases} \quad (11)$$

TABLE I
Typical Parameters That Affect the Current Distribution on Parallel-Connected MOSFET

Category	Variable	Definition
Device parameters	V_{th}	Gate threshold voltage
	C_{gd}	Gate-drain capacitance
	C_{gs}	Gate-source capacitance
	C_{ds}	Drain-source capacitance
	gs	Transconductance
	R_{dson}	On-state resistance
Circuit parameters	V_{dr}	Driver voltage
	L_d	Drain inductance
	L_s	Source inductance
	L_g	Gate inductance
	R_g	Gate resistance
Status indicators	T_j	Junction temperature
	V_{DC}	DC-link voltage
	I_o	Load current

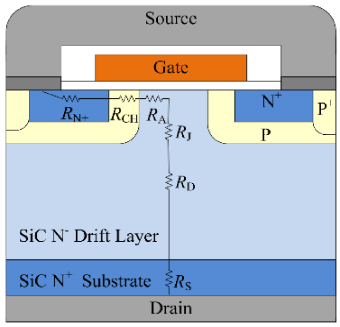


Fig. 13. Components breakdown of SiC MOSFETs R_{dson}.

It is straightforward that the MOSFET with lower R_{dson} shares more current than the one with higher R_{dson}. Generally, higher V_{gs} can reduce R_{dson}, and this is also similar for the third-quadrant mode as claimed in [61]. To better understand the mechanism of static imbalance, an in-depth analysis of R_{dson} should be conducted. As shown in Fig. 13, the R_{dson} of a SiC MOSFET consists of various components.

Among the several components of R_{dson} in Fig. 13, the channel resistance (R_{CH}) has a negative temperature coefficient, while the drift region resistance (R_D) has a positive temperature coefficient. For SiC MOSFETS, higher breakdown voltage normally requires a thicker drift layer, which results in different R_{dson} over temperature behavior. The curves of R_{dson} versus T_j of several commercialized SiC MOSFETS under different voltage ratings are plotted in Fig. 14. Most SiC MOSFETS on the market have positive temperature coefficients of R_{dson} which enable self-balancing of the static currents [62].

For a 650 V SiC MOSFET, R_{CH} can account for more than 50% of the total R_{dson}, while in a 1.7 kV SiC MOSFET, the proportion of R_{CH} can be reduced to be lower than 30%. Therefore, paralleling higher voltage SiC MOSFETS tends to have a stronger self-balancing effect due to the higher temperature coefficient of R_{dson}.

In terms of the temperature coefficient of R_{dson}, there is a tradeoff between the conduction loss and the feasibility of parallel connection. A higher ratio of positive temperature coefficient is beneficial to current balancing for parallel connection

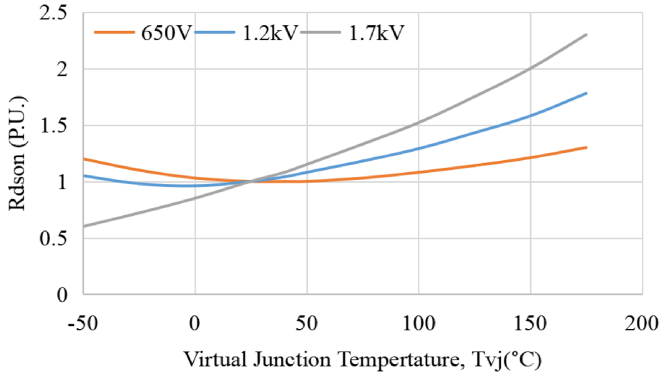


Fig. 14. Normalized $R_{\rm dson}$ versus virtual junction temperature.

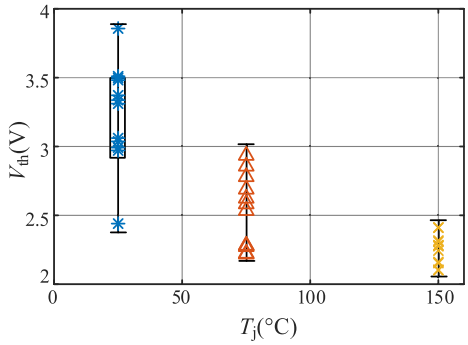


Fig. 15. $V_{\rm th}$ of multiple SiC MOSFETs.

while it leads to a higher conduction loss at elevated junction temperature.

For static current imbalance, the characterization of paralleling SiC MOSFETS is discussed in [63] with $R_{\rm dson}$ variations, which could see the small current difference between the two paralleled SiC MOSFETS with $R_{\rm dson}$ mismatch.

2) V_{th} Variation: $V_{\rm th}$ variation can be introduced in the manufacturing process of the device. As demonstrated in [64], $V_{\rm th}$ can also be shifted under long-term gate stress. Therefore, investigating the impact of $V_{\rm th}$ variation on the current imbalance is critical. Twenty SiC MOSFETS are chosen for testing with a curve tracer. The $V_{\rm th}$ curves are plotted in Fig. 15.

$V_{\rm th}$ variation has a major impact on the dynamic switching current distribution and $R_{\rm dson}$ variation mainly affects the static current sharing [65], which could also be explained with the following equation:

$$I_{\rm d} = g_{\rm fs}(V_{\rm gs} - V_{\rm th})^2. \tag{12}$$

As shown in Fig. 16, in paralleled MOSFETS, the device with lower $V_{\rm th}$ has faster turns-ON and slower turns-OFF, which leads to both higher turn-ON and turn-OFF losses. This happens because it withstands more current stress. Consequently, among the paralleled devices, the $T_{\rm j}$ of the device with lower $V_{\rm th}$ can be higher due to higher switching losses. Moreover, the negative temperature coefficient of $V_{\rm th}$ can lead to a vicious circle and finally a catastrophic result [66].

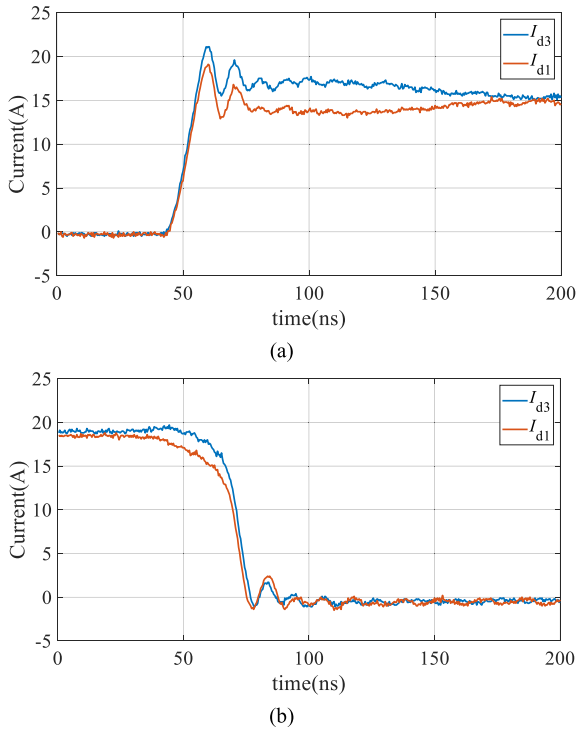


Fig. 16. Experimental dynamic current distribution with $V_{\rm th}$ variation. (a) Turn-ON process. (b) Turn-OFF process.

Compared with the self-balancing feature of $R_{\rm dson}$ variation among paralleled devices, this self-aggravating feature of $V_{\rm th}$ variation could lead to severe $T_{\rm j}$ mismatch and even thermal run-away events.

C. Circuit Parameters Mismatch

1) $L_{\rm d}$ Mismatch: Li et al.[63], [67] claimed that $L_{\rm d}$ has little impact on dynamic current sharing. The reason is that the $I_{\rm d}$ in switching transient is controlled by (12) while $L_{\rm d}$ has no direct impact on $V_{\rm gs}$. Nonetheless, the impact of $L_{\rm d}$ on the current oscillations cannot be neglected.

An experimental study is conducted to validate this impact. Twenty MOSFETS with the same part number are tested with a curve tracer and two MOSFETS, i.e., M1 and M4, with identical parameters are selected for the study. Fig. 17 shows the current waveform of the two paralleled MOSFETS with different $L_{\rm d}$. $I_{\rm d1}$ and $I_{\rm d4}$ in Fig. 17 denote the current of SiC MOSFETS with $L_{\rm d4}$ = 64 nH and $L_{\rm d1}$ = 34 nH, respectively. $I_{\rm d4}$ has a larger ringing over $I_{\rm d1}$. With the analysis in [63], $L_{\rm d}$ has an influence on the current in a short period after turn-ON and turn-OFF. SiC MOSFET with larger $L_{\rm d}$ has a smaller oscillation frequency and a smaller damping factor after turn-ON and turn-OFF. As a result, the SiC MOSFET with larger $L_{\rm d}$ has a larger current overshoot, and the current oscillation amplitude after turn-OFF is also larger.

Additionally, $L_{\rm d}$ has an impact on the static current sharing if the drain current is still changing during the ON-state period. The equivalent circuit of paralleled MOSFETS in ON-state mode is shown in Fig. 18 where L is the load inductance. It can be derived that the ON-state current difference could be calculated

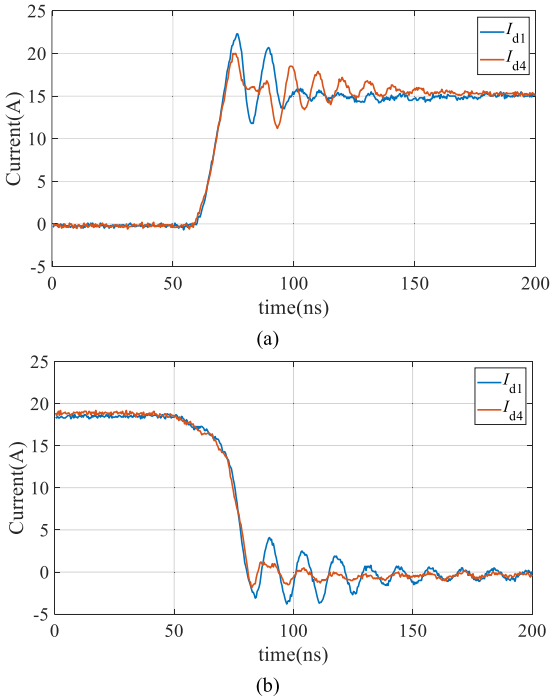


Fig. 17. Experimental switching transient current with different L_d. (a) Turn-ON process. (b) Turn-OFF process.

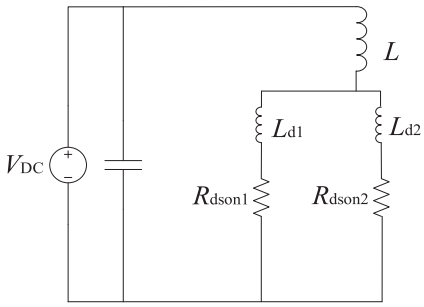


Fig. 18. ON-state equivalent circuit of paralleling two SiC MOSFETs.

with the following:

$$I_{ds1} - I_{ds2} \approx \frac{L_{d2} - L_{d1}}{2R_{dson}} \frac{V_{DC}}{L}. \tag{13}$$

It means that the static current difference can be influenced by four parameters: loop inductance, R_{dson}, load inductor L, and dc-link voltage.

2) L_s Mismatch: In contrast to L_d, L_s mismatch has a significant impact on dynamic current sharing [63] due to its influence on V_{gs}. Analyzing the equivalent circuit in Fig. 12, (14) can be derived. It shows that the channel current is determined by V_{gs} during switching transient while V_{gs} is affected by L_s and source current I_s

$$V_{gs} = V_{dr} - i_g R_g - L_s \frac{dI_s}{dt}. \tag{14}$$

Fig. 19 shows the switching current with L_s mismatch, which demonstrates that larger L_s results in both slower turn-ON and turn-OFF. It means that the MOSFET with larger L_s leads to a smaller turn-ON loss since more current stress is withstood by the MOSFETS which turn ON faster. On contrary, the turn-OFF loss of the MOSFET with larger L_s is higher since the other MOSFET operates in quasi-zero-voltage switching mode.

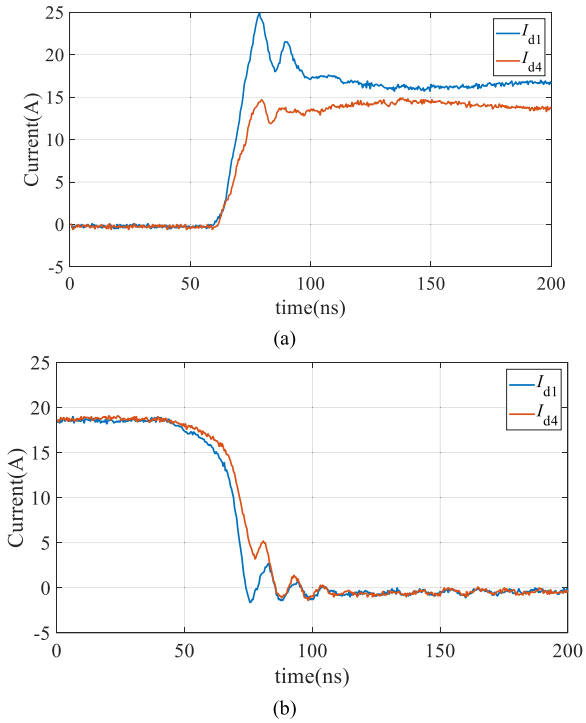


Fig. 19. Experimental current sharing performance of M1 and M4 ($L_{s4} > L_{s1}$). (a) Turn-ON waveform. (b) Turn-OFF waveform.

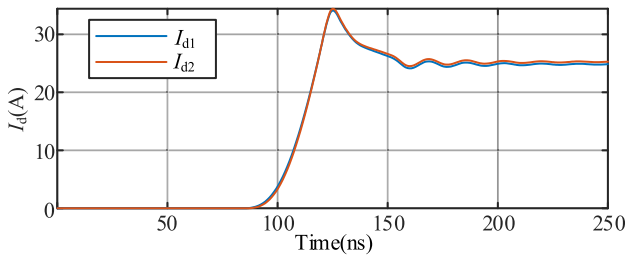


Fig. 20. LTspice Simulation waveform with the impact of L_g on turn-ON transient.

3) L_g Mismatch: L_g mismatch has a small impact on transient current sharing. Even though higher L_g means a slower charging process of V_{gs}, the gate current and its di/dt are normally quite small in switching dynamic. Therefore, its impact on the gate voltage values is not as significant as L_s. LTspice simulation is conducted to study the impact of L_g on switching speed for paralleled MOSFETS. The L_g of M1 is 10 nH, while that of M2 is 50 nH. The I_d curves of both MOSFETS are plotted in Fig. 20. It validates that the impact of L_g mismatch on the current distribution is not critical. However, gate inductance and its mismatch could lead to gate oscillations and instability issues, which is out of the scope of this article and therefore not discussed.

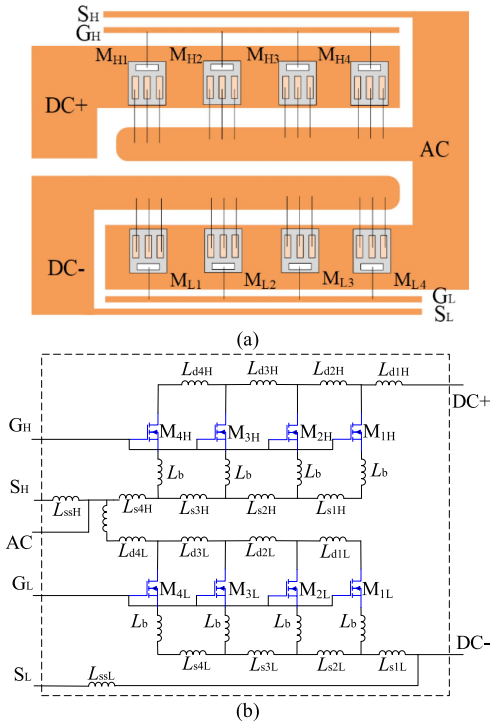


Fig. 21. Power module layouts and their modeling. (a) Package layout. (b) Equivalent circuit.

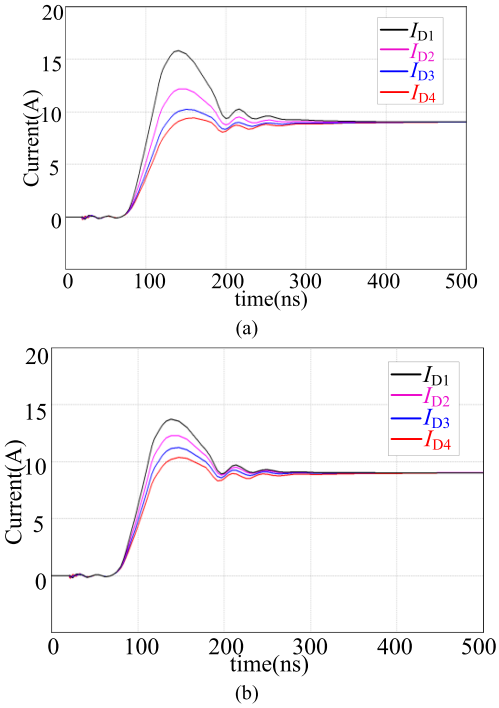


Fig. 22. Simulation result of current waveform of four paralleled MOSFETs. (a) With current coupling effects. (b) Without current coupling effects.

V. Analysis and Modeling of Multichip Power Module Layouts

Section IV analyzes the impact of the electrical parameters mismatch on current sharing. In a multichip power module, there could be more than two devices in parallel. The accurate modeling of the multichip power module layouts is essential to the current sharing analysis.

A typical power module layout is shown in Fig. 21(a), while its equivalent circuit is shown in Fig. 21(b). The gate loop inductance and mutual inductance are not considered since only gate loops are analyzed here. The current distribution among the paralleled SiC MOSFETs with the above layout is analyzed in [63]. It is revealed that the inductance L_{sxL} has a significant impact on dynamic current sharing due to its impact on V_{gs} during the switching transient process. While the impact of L_{dxL} on dynamic current sharing is not critical since V_{gs} during switching transient is not influenced by L_{dxL}. In this layout, the effective value of L_{sxL} and L_{dxL} is around 1–2 nH considering the magnetic coupling effects. With a di/dt of 2 kA/μs, the voltage on the parasitic inductance could be around 2–4 V. While this voltage is not comparable to the drain–source voltage but it has a significant impact on the gate–source voltage which is normally between –5 and 15 V.

A. Current Coupling Effect

Aside from the analysis above, the current coupling effect can exacerbate the current imbalance among the paralleled devices [68]. The current coupling effect means that the current of the paralleled devices affects not only its switching transient current but also the other devices' currents. Dynamic current imbalance among the paralleled SiC MOSFET is because of the device source terminal voltage difference, the root cause of which is due to the voltage on the mismatched inductance. The mismatched inductance voltage is equal to L^{*}di/dt during the switching transient.

Therefore, both the mismatched L and di/dt play pivotal roles. Even though the value of L_{s4L} and L_{s2L} are identical, the di/dt applied on L_{s2L} is more than 3 times that on L_{s4L}. Consequently, the dynamic current imbalance between $\mathrm{M_{L1}}$ and $\mathrm{M_{L2}}$ is larger than the current imbalance between $\mathrm{M_{L3}}$ and $\mathrm{M_{L4}}$. Due to the current coupling effect, the same inductance mismatch leads to different current imbalances, as shown in Fig. 22.

B. Paralleling Dies and Paralleling Half-Bridges

Fig. 23 shows a power module layout as well as the busbar structures, which have six substrates in parallel. Each substrate is an individual half-bridge. In other words, the layout in Fig. 23 is configured with six half-bridges in parallel. The equivalent circuit of this layout is shown in Fig. 24.

The difference between paralleling dies and paralleling half-bridges is the current commutation loop, which further influences the di/dt on the parasitic inductance [69]. As shown in Fig. 24, with paralleled half-bridges, the di/dt on L_{sHx} between the top side paralleled devices is not high, since the current commutation is able to be achieved within the individual half-bridge. While with paralleling dies in Fig. 21, every current commutation between the top switch and the bottom switch leads to full load di/dt on L_{sHx}.

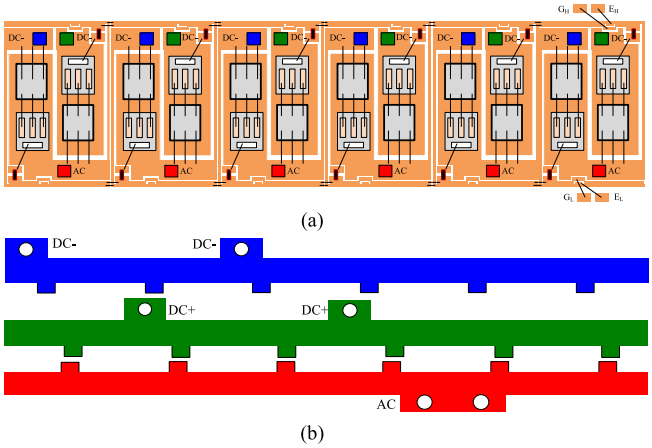


Fig. 23. Power module layout with paralleling half-bridge configurations. (a) Package layout. (b) Bus bar layout.

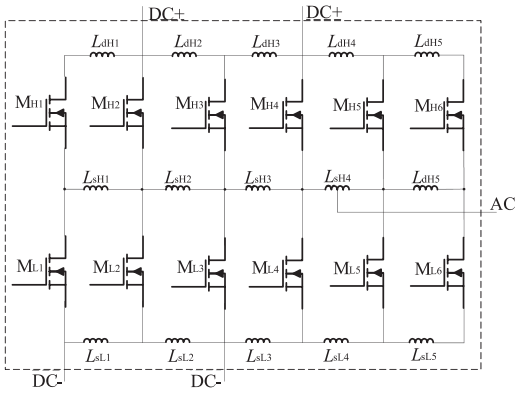


Fig. 24. Modeling of the layout with paralleling half-bridges.

The d*i*/d*t* interacting with parasitic inductance generates voltage among the source terminals of the paralleled SiC MOSFETs. Thus, the potential of each source terminal is different and this is the dominant reason for dynamic current imbalance among the paralleled devices.

The simulation results of current sharing performance with paralleling half-bridges are plotted in Fig. 25. It can be seen that the dynamic current imbalance of the top devices is not high while that of the bottom devices is significant.

C. Auxiliary Source Connections

Auxiliary source connection is extensively applied in multichip power modules. It is revealed that the auxiliary source connection for paralleled devices in a multichip power module cannot fully decouple the power loop and gate loop, which is different with the Kelvin connection of a single device [70]. In order to add auxiliary source connections to the layout in Fig. 21(a), the original layout can be improved as shown in Fig. 26(a), while its equivalent circuit can be drawn in Fig. 26(b).

From Fig. 26, it can be seen that there are more than one current paths between the paralleled source terminals. The impedance of each path determines the current distribution

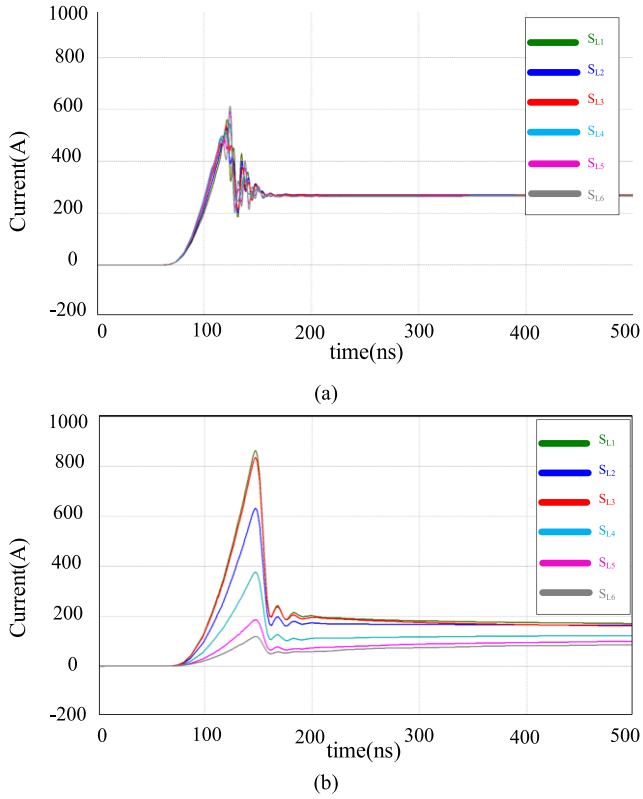


Fig. 25. Simulation result of current sharing performance with paralleling half-bridge configurations. (a) Current waveform of the top devices. (b) Current waveform of the bottom devices.

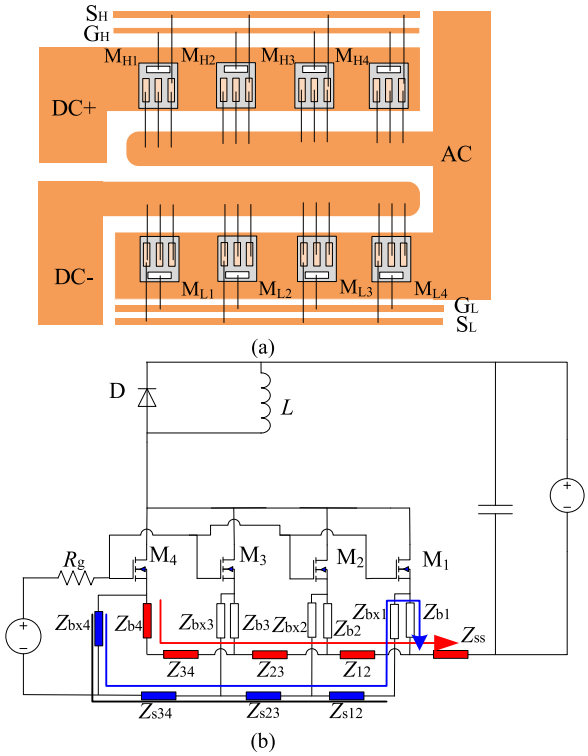


Fig. 26. Power module layout with auxiliary connection and its modeling. (a) Package layout. (b) Equivalent circuit.

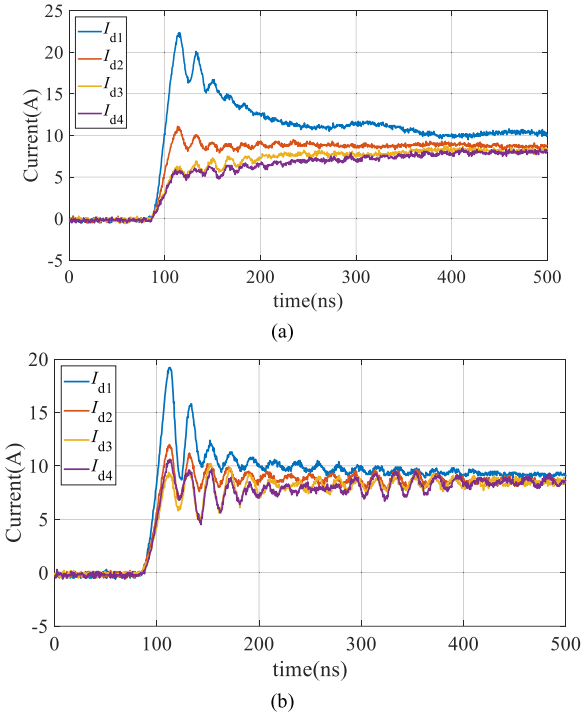


Fig. 27. Experimental Current waveforms in a multichip power module. (a) Without auxiliary source connection. (b) With auxiliary source connection.

among the different paths. The impact of the auxiliary source connections on the dynamic current imbalance can be validated by the experimental results in Fig. 27 [70].

A power module with four identical dies is tested and the waveforms are plotted in Fig. 27. The difference between highest current peak and lowest current peak is 18 A which leads to high DoI. With an auxiliary source connection on the module, the difference can be reduced by half to 9 A.

VI. Solutions of Current Mismatching in Parallel-Connected Devices

Various state-of-the-art methodologies for tackling the current mismatch issue in paralleled devices can be categorized into two major types: passive methods [71] and active methods [72], [73]. Passive methods can minimize the impact of mismatched electrical parameters among loops by optimizing the package/circuit layout or preselection of the chips. Active methods employ auxiliary circuits or component to realize current rebalancing. They include external passive components and external active components. External passive components methodologies can adjust the current distribution via adding passive components in the gate loop or power loop. The external active components methods usually employ adjustable gate driver solutions to dynamically change the device characteristics cycle by cycle. In this section, the research of the aforementioned two methodologies will be illustrated.

A. Passive Methodologies

Passive methodologies can adjust the current distribution via selecting the dies with identical electrical parameters or

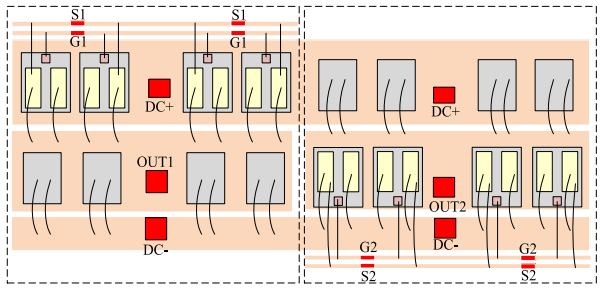


Fig. 28. Improved power module design for dynamic current imbalance mitigation.

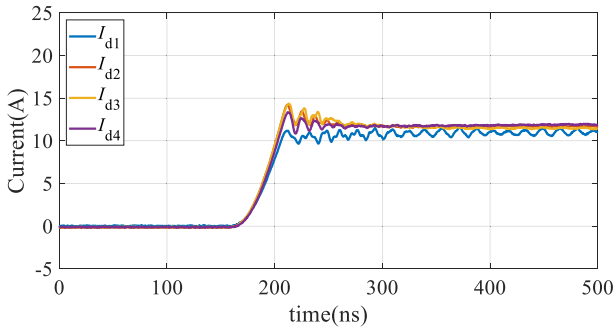


Fig. 29. Experimental dynamic current imbalance mitigation results.

optimizing the hardware layout. From the sequence of the semiconductor device manufacturing process, it can be categorized into the preselection of dies and layout optimization of the circuit.

Preselection of chips means selecting the MOSFET chips in prior to packaging into a module. As demonstrated in Section II, the dies in one wafer usually have different electrical parameters such as $V_{\rm th}$, $R_{\rm dson}$, and $C_{\rm gd}$. For a power module with multiple paralleled dies, the chips with close electrical parameters are selected for a module [74], [75]. Machine learning algorithms are utilized in paper [76] to assist in the SiC die screening for sorting paralleling SiC MOSFET. Device screening strategy is applied in paper [77] to balance the short-circuit current on the paralleling SiC MOSFETs.

The hardware layout includes power module package layout and external circuit layouts such as a bus bar and PCB [78]. The symmetric circuit layout method can eliminate the current imbalance brought by the mismatched parasitics among different current loops. Fig. 28 shows an improved power module layout design. The layout optimization for mitigating the current imbalance is usually conducted by minimizing the following parameters:

1) mismatched $L_{\rm s}$;
2) di/dt across the mismatched $L_{\rm s}$.

Comparing the layout in Figs. 21(a) and 28, it can be concluded that both the mismatched $L_{\rm s}$ and di/dt applied on the mismatched $L_{\rm s}$ are reduced. The experimental results before/after performing the aforementioned improved method are plotted in Fig. 29 [79].

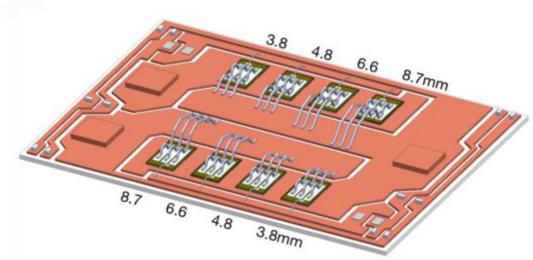


Fig. 30. Substrate layout design with different wire-bonding lengths.

Apart from the previous optimization method, multiple emerging module layouts are summarized in [80] which also figures out the future development direction. Specifically, several design methods for symmetric the module internal layout or bus bar structure are introduced in [79], [81], [82], [81] and [83].

Fig. 30 shows another method to improve the current sharing performance, which inserts additional parasitic inductance by adjusting the length of source wire bonding for the paralleled chips [84]. This approach could potentially mitigate the current imbalance to a certain degree but it also increases the parasitic inductance, which can slow down the switching speed or pose switching oscillations. A method with a similar principle can be found in [85]. To control the parasitics on the connecting wires, copper clips are utilized to supplant bonding wires.

B. Active Methodologies: External Passive Components

An active method in the industry is inserting external passive components into the gate loop or power loop. It can manually adjust the impedance for the circulating current and finally realize current sharing. It is known that the passive components can be categorized into inductors (L), capacitors (C), and resistors (R). Different combinations of passive components can adjust the overall characteristics and finally change the current trajectory and distribution.

Employing external passive components for mitigating the current imbalance is usually conducted by optimizing the following parameters.

1) Static current imbalance: adjust the resistance in the current route.
2) Dynamic current imbalance: change the impedance for circulating current.

A typical inductor-based method is presented in [86], which rebalances I_{d} via connecting a differential mode inductor on the source side as shown in Fig. 31.

When I_{d} is unbalanced, there is an equivalent circulating current between the power loops. The differential mode inductor can increase the impedance for the circulating current, thus the current imbalance is minimized. The mechanism can be further applied on the parallel-connection of power converter as demonstrated in [87] which applies coupled inductor on a resonant pulsed power converter. An RC network connected in the gate loop to suppress the circulation gate current and balance the current in paralleled MOSFET is proposed in [88].

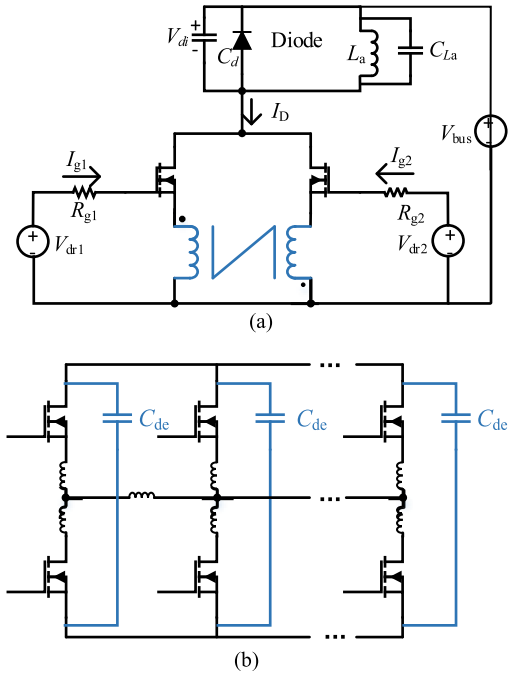


Fig. 31. Several external passives method. (a) Differential mode inductor [86]. (b) Decoupling capacitors on each half-bridge [89].

As analyzed in Section IV-B, paralleling half-bridge has superior current sharing performance over paralleling dies. However, the lower side switch still has current imbalance caused by coupled current. To address this problem, a dynamic current sharing method proposed in [89] optimizes the layout of PCB to enable decoupling capacitors to be located close to the half-bridge. External resistors are added in series with the power MOSFET to adjust the total ON-state resistance [90]. The hybrid component method combines resistors, inductors, or capacitors to implement current sharing. A Kelvin-source resistor and a power source inductor are utilized [91] to mitigate the dynamic current imbalance. It can balance the steady-state I_{d} while also increasing the conduction loss and reducing the overall efficiency. As demonstrated in [92], two switches are applied on the source side of the MOSFET to actively adjust the current distribution and finally realize current sharing. An R–L network connecting in the power loop is proposed to minimize the current imbalance between multiple parallel IGBTs in [93].

C. Active Methodologies: External Active Components

Generally, the aforementioned two methods have a drawback in terms of lack of flexibility. The circuit layout or the passive components cannot be changed in the operating condition, thus they are not appropriate for all conditions. Furthermore, as demonstrated in Section II, V_{th} can change due to variating T_{j} when the converter is operating. Therefore, online current sharing methodologies are desired. Specifically, close-loop control lends its capabilities to be applied in various operating conditions. It is known that adjusting the gate driver parameters can change the slew rate of the power MOSFET [94]. As claimed

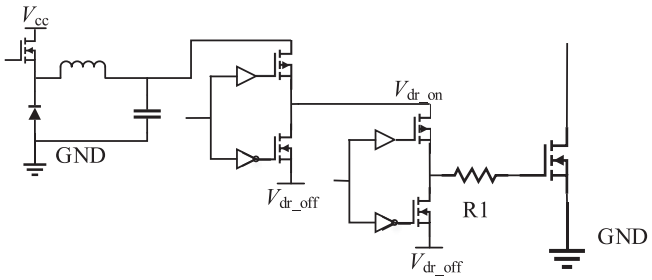


Fig. 32. Circuit topology of the adjustable V_{gs} gate driver [99].

in [39], there are four variables for MOSFET switching trajectory adjustment from the gate side, i.e., gate resistance, gate current, gate voltage, and input capacitance. Thus, to adjust the current distribution, active methodologies are usually implemented by utilizing active gate driver (AGD). AGD is an emerging gate driver technique that can adjust its output dynamically based on real-time operation conditions [95]. Generally, the basic mechanism of using external active components for mitigating the current imbalance can be summarized as follows.

1) *Static current imbalance:* Via actively adjusting the R_{dson} of the MOSFETS, the channel current distribution can be changed.
2) *Dynamic current imbalance:* By actively changing the switching slew rate di/dt or gate signal delay φ, the dynamic current stress on each MOSFET can be tuned.

Static current imbalance can be addressed via adjusting R_{dson}. Since V_{th} and other parameters in (11) are all determined in the midst of die manufacturing, the only adjustable parameter is the normal turn-ON driver voltage V_{dron}. Thus, to change the static current distribution, variable static driver voltage is needed. Also, considering that R_{dson} is also pertinent to T_j which is greatly impacted by the load current, it is preferred to have a turn-ON driver voltage adjusted cycle by cycle. This mechanism is usually employed to suppress ΔT_j and finally maximize the life cycles. Several driver circuits to dynamically change V_{dron} are proposed in [96], [97], and [98]. Via detecting the collector current of an IGBT, it can increase V_{ge} at the load current peak and reduce V_{ge} at the load current valley. In this way, ΔT_j can be minimized and the device long-term reliability is enhanced.

For paralleled MOSFETS, different V_{dron} levels are applied on each MOSFET to compensate for the static current imbalance in [99] and [100]. The V_{dron} adjustment can be implemented by using adjustable power supply with a buck converter as shown in Fig. 32(a) [99]. Also, there are some other circuits such as using digital/analog converter, analog adder circuit, and amplifier circuit.

The dynamic current sharing methods with AGDs are relatively challenging for the sake of the very short switching transient process. Specifically, V_{ds} and I_d changing period occurs during the Miller plateau which can be finished in a couple of nanoseconds. The dV/dt of a SiC MOSFET can increase to over 50 V/ns which means the voltage falling substage can be finished in 10 ns. This is challenging to the design of the active gate driver, particularly for the selection of voltage/current sensors, timing sequence, and topology of the AGD [97].

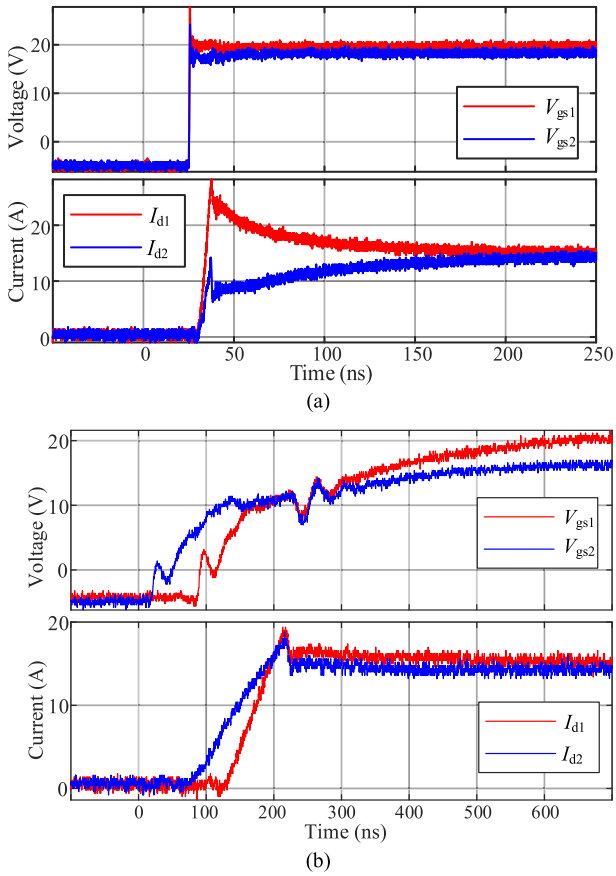


Fig. 33. Experimental results of the parallel-connected device with variable gate voltage AGD. (a) Without AGD. (b) With AGD.

Apart from the slew rate, the switching loss on paralleled MOSFETS is relevant to the gate signal lagging time between the two MOSFETS. Theoretically, the earlier MOSFET withstands higher turn-ON loss and lower turn-OFF loss. As shown in Fig. 33, the transient current waveform of two MOSFETS is not balanced. Via changing the gate lagging time, it can be rebalanced as given in Fig. 33(b). Based on this feature, a common application scenario for AGD is the hybrid switch which is comprised of a Si IGBT with a SiC MOSFET [101]. It is desired to combine the Si IGBT's low conduction loss and SiC MOSFET's low switching loss superiorities [102]. Correspondingly, by means of controlling the gate signal lag between the two devices, the overall power loss can be manually adjusted. SiC MOSFET is desired to turn ON earlier and turn OFF later than the Si IGBT, thus the switching loss is withstood by the SiC MOSFET. Thus, the high switching loss of IGBT can be avoided. The advantage is that the overall power loss can be greatly reduced while the downsides include the higher cost and higher current which may move the SiC MOSFET out of SOA. This method has been presented in [103], [104], [105], and [106] and quantifies the power loss for the hybrid switch under different gate signal delay times.

To realize dynamic current sharing, variable gate current AGD is applied in [107] while this methodology is also employed to balance the voltage in series-connected power MOSFET [108]. Both papers utilize the current mirror circuit and adjustable voltage regulator to change the gate current during the switching

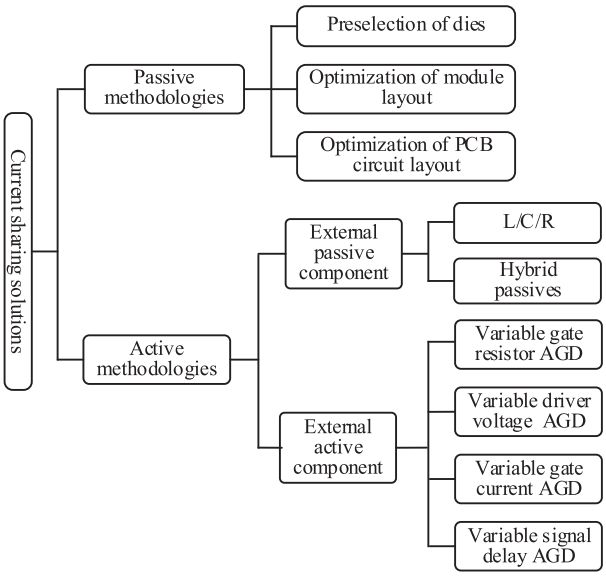


Fig. 34. Summary of the state-of-the-art current sharing methodologies.

transient. Variable gate resistor AGD is employed in [109] to realize dynamic current sharing. The basic operating principle is similar to paper [97]. The capacitor coupling method is utilized in [110] to change the gate current during the switching transient and balance the voltage on series-connected power MOSFET. An adjustable gate signal delay auxiliary circuit for the gate driver is proposed to change the switching stress on paralleled MOSFETS in [111] and [112]. Several variable driver voltage AGD circuitries are introduced in [73] and [113] for the current sharing of paralleled MOSFETS.

D. Conclusions and Insight of Current Sharing Strategies

The state-of-the-art types of current sharing solutions can be summarized in Fig. 34.

Passive methods are generally cost-friendly and no extra component is needed. It can be implemented amid fabrication, thus it is preferred by manufacturers [43]. Via continually improving the die screening strategy and optimizing package layout, the commercialized power modules are approaching ideal switches. However, there are still some challenges from technic and cost aspects hindering the further optimization of the power module.

SiC MOSFETS tends to have the concept of known good die (KGD), which means that the key device parameters could be available. This is helpful for the die screening method to improve the current sharing performance among the paralleled devices in multichip power modules. However, there are still a few challenges. First, among the many device parameters (R_{dson}, V_{th}, g_{fs}, etc.), it needs to choose one parameter or an algorithm to make the die binning or screening. At present, SiC vendors, on the one hand, are trying to improve the device process maturity to reduce the device parameters' tolerance. On the other hand, a practical algorithm for die binning is also under development and estimation. Second, the KGD concept is currently still based on room temperature. High-temperature KGD for mass production is possible but still quite challenging considering the high-temperature oxidation of the metallization, cost, efficiency, etc.

For the multichip SiC power module package, a more effective and intelligent die binning or sorting method is needed for SiC power devices. The binning or sorting should not be carried out according to one specific device parameter. A "comprehensive device parameter" should be developed to reflect the overall device performance, including paralleling performance, reliability, robustness, and cost. In addition, high-temperature, low-cost KGD measurement equipment, and efficient burn-in test equipment are expected for high-temperature device parameters acquisition.

For multichip power module layout design, some guidelines could be given here. As MOSFET is a voltage-controlled device, which means I_{d} is fully controlled by V_{gs} during the switching transient, the design of the multichip module layout is to reduce the differences of V_{gs} for the paralleled devices. Considering that the difference in gate voltage potentials is small, the design principle is to reduce the difference in source voltage potentials. Two executable rules [79] are reducing the mismatched L_{s} and the di/dt applied on the mismatched L_{s}. By following these design rules, the dynamic current imbalance could be significantly suppressed. The increasing penetration of artificial intelligence (AI) algorithms into manufacturing enables the design process to be smarter. Since all SiC dies are tested in advance to packaging, their electrical parameters are known and it allows the preselection to be implemented. Several computer-aided automatic layout generation methods aiming at minimizing the parasitic inductance in the current loop have been introduced in [114], [115], [116], and [117]. More AI-involved layout design will be the future trend of power semiconductor device packaging development.

The active methods are generally the supplementary solutions for situations when the passive methodologies no longer work. For instance, paralleled discrete devices are usually utilized in an electric vehicle since they are cost-efficient compared with using a power module. In these conditions, active methods can be adopted to improve the long-term reliability of the system. First, adding the external passive components can increase the cost and introduce extra parasitics in the loop which may lead to false-triggering, voltage overshoot, or crosstalk noise [118]. Second, AGD is a premature technology due to the very short switching transient of SiC MOSFET which is usually within 100 ns. di/dt of a SiC module can increase to 5 A/ns. The current sensing, signal processing and timing sequence in such a short time are usually challenging [39]. For instance, a variable driver voltage AGD usually changes the driver voltage during the Miller plateau to adjust the switching slew rate. The detection of the Miller plateau and calculation of optimal driver voltage for the Miller plateau is difficult. The commercialized gate driver on the market can be found in [119]. It employs a patented augmented turn-OFF driver voltage profile to suppress the overshoot voltage. However, software configuration is utilized to optimize the turn-OFF process of each SiC MOSFET. Academia has dedicated much effort to the exploration of closed-loop control for AGD including Rogowski coil [120], the voltage on the stray inductance [73], and current transformer [121], [122].

For the active gate driver method, an effective and low-cost device current measurement method or an equivalent device current acquisition method is needed for accurate device current

distribution optimization. Taking one step back, the active gate driver method could be helpful given the junction temperature could be estimated via the TESP method. In most cases, the target is to limit the junction temperature differences either by controlling the steady state or the dynamic current distribution. Therefore, with AGD and junction temperature estimation of each device, the switching speed or the effective R_{dson} could be adjusted by AGD in a thermal time constant. With this, the requirements of device's current measurement are not needed.

VII. Conclusion

This article comprehensively summarizes the state-of-the-art research on paralleling SiC power devices. It starts with the challenges brought by the application of SiC for the paralleling operation. It is followed by a detailed analysis of the current imbalance mechanism among parallel loops. An index *DoI* is proposed to quantify the degree of static and dynamic current imbalance. Various parameters pertinent to the static and dynamic current distribution are categorized into three major types, i.e., the device parameters which are the equivalent parameters inside the dies, the circuit parameters which are parasitics introduced by the package and circuit, and the status indicators such as junction temperature and load current.

Based on the theoretical analysis, the state-of-the-art current sharing methodologies in the industry are summarized. The passive method includes the preselection of dies based on the screening results and package/circuit layout optimization methods. This article also figures out the design criteria of a paralleled devices system. Active current sharing methods include the external passive components and active gate driver solutions are also summarized. Based on the summary of the analyses and solutions, the insight of the current sharing strategies for paralleling SiC MOSFETS is presented.

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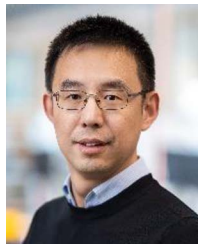

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