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Inverter design for future electrified aircraft propulsion systems under consideration of wear-out failure and random failure

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***Index Terms*—Electrified Aircraft, Reliability, Lifetime, Inverter design.**

***Abstract*—To reduce the wear-out effect and minimize the Single Event Burnout effect of the power semiconductor, several hardware design rules for inverters in electric aircraft propulsion systems are posed and implemented in this work. These strategies include scalable chip area and derated DC-link voltage. It is observed in a short-range reference aircraft case study that these rules could result in a conflict of objectives: reducing the risk of wear-out failure while simultaneously minimizing the risk of random failure. Therefore, it is recommended to consider random failures, wear-out failures, and their mutual impacts in a comprehensive analysis of system reliability. A reliability-oriented design rule is proposed in this work.**

I. INTRODUCTION

Sustainable and energy-efficient aviation with electrified propulsion systems is one of the most promising solutions to achieve net-zero carbon emissions in the next few decades. In order to accomplish these goals, electrified aircraft propulsion systems not only need to be lightweight and highly efficient but also need to demonstrate their reliability to meet stringent aircraft safety requirements [1].

One of the most important indicators for evaluating the component reliability is the failure rate λ, which describes the "proneness to failure" of a component after the time t has elapsed. A typical failure rate curve, known as the bathtub curve, can describe the failure characteristics over the lifetime of a component. The bathtub curve can be mainly divided into three phases: early failure, random failure and wear-out failure. During the early failure phase, failures are primarily induced by design or quality control issues. Performing burn-in tests could be beneficial in reducing these early failures. In the second phase, random failures such as Single Event Burnout effect, over-voltage or over-heating events are dominant. The failure rate during this period is usually assumed to be constant. Due to the wear-out effect of the components, the failure rate of the components increases during the wear-out failure phase, ultimately limiting the useful life of the components and the systems [2]. A widely used indicator for assessing reliability is the B_{x} lifetime, which represents the time when $x\%$ of the device population fails.

In aircraft propulsion applications, the power electronic system needs to be designed to minimize the risks of random failure in order to meet the required target average failure probability per flight hour throughout its useful life [3]. One of the most concerning risks of random failure can be induced by an increased exposure to cosmic radiation at high flight altitudes. Additionally, the wear-out effect must also be taken into account

during the inverter design phase to meet the service life requirement. Most commercial aircraft are expected to have a design life of 25-30 years in service. Minimizing the wear-out effect of the inverter system could also potentially reduce maintenance costs, which typically account for 10-20 percent of aircraft-related operating costs [4]. Among the wear-out mechanisms, thermo-mechanical-related failure is predominant. Particularly for power electronic systems in aircraft propulsion applications, such failure is primarily caused by significant changes in load demand, resulting in substantial junction temperature variations during their mission profiles.

To achieve these objectives, several reliability-oriented design rules can be adopted. In [5] - [6], a scalable modeling method for power semiconductors is introduced, allowing for adjustments to the active chip area, which significantly impacts the wear-out effect of the power semiconductors due to changes in thermo-mechanical stress. Bolotnikov proposes in [7] a reduction in voltage utilization on power semiconductors to reduce the risk of cosmic radiation-induced failures and to achieve the desired failure rate. In [8], the impact of the thermo-management on the cosmic radiation-induced failure of the power converter system was addressed. However, these design rules regarding the reliability of power electronic systems are interrelated and not independent. Previous studies have focused either on reducing the risk of random failures (due to cosmic radiation) or minimizing the wear-out effect of power semiconductors. They overlook the fact that the above mentioned design rules can lead to conflicting reliability objectives in terms of minimizing the risk of random failures and reducing the risk of wear-out failures. Additionally, the evaluation of lifetime is associated with both types of failures. This work addresses these issues through a case study and proposes a system reliability design framework for inverter systems in aircraft propulsion applications.

II. Inverter design under considerations of random device failure

Failure mechanism of power semiconductors due to radiation can be divided into two categories: degradation effects caused by long-time exposure to cosmic radiation (Total Ionizing Dose, TID), and sudden effects caused by single radiation particles (Single Event Effects, SEE). Because the overall radiation dose is only $1-9\ \mu\mathrm{Sv\,h^{-1}}$ for typical flight altitudes, TID effects are of no relevance in aircraft applications. on the other hand SEE can lead to sudden and unpredictable failure of power semiconductors even on ground level. The failure mechanism is based on a single neutron from the natural radiation interacting with the semiconductor material and by that causing damage to the gate structure (Single Event Gate Rupture, SEGR) or leading to a thermal destruction by burnout (Single Event Burnout, SEB). For the latter, electron-hole-pairs are generated by indirect ionization. These will be accelerated by the E-field in the device during voltage blocking, generating more electron-hole-pairs by impact ionization, forming an avalanche. The failure rate is determined by the number of available neutrons and the probability of an interaction between a neutron and the semiconductor material, the so-called *cross section*. Because of that, SEB are a stochastic process, which can not be predicted, justifying the declaration as random failure. As a result, the failure rate directly depends on the number of available neutrons, which in turn exponentially increases with altitude. For a flight altitude of 12 km, the neutron flux increases by approximately 300 times compared to sea level, highlighting the significant impact of radiation-induced failures in aircraft applications. To calculate the failure rate for flight missions, it is essential to have failure data for the power semiconductors used at sea level. These failure data can be obtained by conducting accelerated measurements using artificial neutron beams, as described in [9]. The data are normalized to one square centimeter of chip area to ensure comparability. Due to the stochastic nature of the failure mechanism, a larger chip area will result in a higher failure rate since more semiconductor material is exposed to radiation. Therefore, reducing the chip area can be a viable approach to decrease the failure rate caused by cosmic radiation. However, this needs to be balanced against other reliability requirements, as it will be explained later. Furthermore, it can be demonstrated that a higher blocking voltage will increase the failure rate due to the increased electric field within the device, resulting in a stronger acceleration of electron-hole pairs. The impact of altitude and blocking voltage are summarized in Fig. 1, showing the FIT rate (Failure In Time, one failure per 10^9 hours) per square centimeter of chip area in dependency on the normalized blocking voltage for different altitudes. The failure data is based on measurement of a 1.7 kV SiC-MOSFET presented in [9]. In order to guarantee a certain FIT rate required by the application, a voltage derating is necessary. In summary, both the chip area and the blocking voltage have a high influence on the failure rate due to cosmic radiation and need to be investigated as parameters in the reliability evaluations. It should also be mentioned that the risk induced by cosmic radiation could be

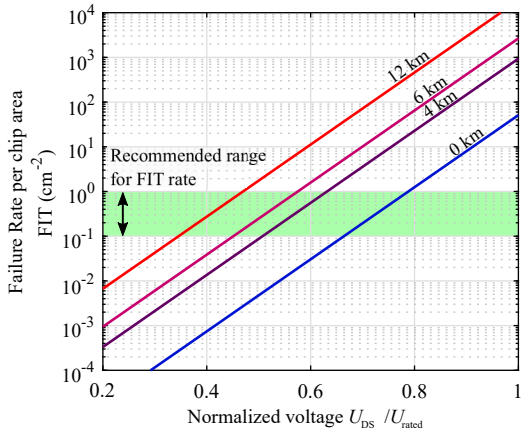

Fig. 1. Example failure rate of a 1.7 kV SiC-MOSFET in dependency on the applied voltage and the flight altitude, normalized to one square centimeter of chip area. Failure data based on [9].

more pronounced for electrified middle-range aircraft and long-range aircraft with potentially higher power propulsion systems. In these cases, the challenges related to chip area, blocking voltage level, and neutron flux density are larger.

In addition to the impact of flight altitude, chip area, and voltage utilization, the junction temperature dependence on the failure rate of IGBT modules induced by the cosmic radiation was investigated in [10]. The test results revealed that a higher junction temperature is beneficial in reducing the Single Event Burnout (SEB) effect for IGBT modules. However, the temperature dependence of SEB for SiC power semiconductors is still unknown [11], and further experimental investigations are needed in this regard. It is important to note that this work does not take into account the temperature dependency on the cosmic ray ruggedness for SiC power components.

III. Inverter Design under Considerations of Wear-Out Failure

To assess the wear-out-related failures of power semiconductors in inverter systems, this work conducts a mission-profile-based evaluation, considering thermo-mechanical stress as the primary cause. Since static parameters do not accurately represent real field operation conditions, Monte-Carlo simulations are utilized to incorporate parameter and load uncertainties into the analysis. The mission-profile-based lifetime evaluation process is depicted in Fig. 2, which will be explained in the following subsection.

A. Mission profile and propulsion system

For the case study, this work adopts the mission profile of a short-range reference aircraft (see Fig. 3).

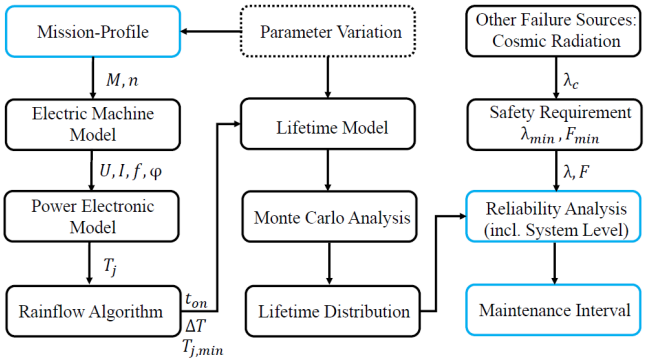

Fig. 2. Mission-profile-based lifetime evaluation

The mission profile is derived based on [12]. Using this mission profile as a basis, the electric drive system will be appropriately sized to meet the power requirements.

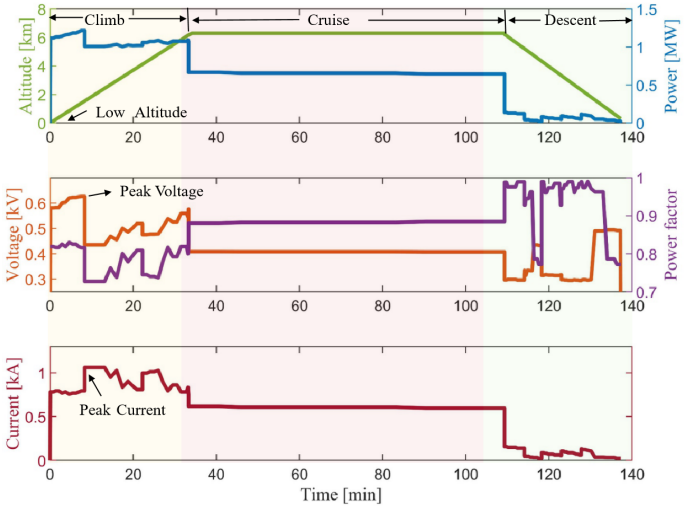

Fig. 3. Typical mission profile for a short range flight with data based on [4]. Top: flight altitude and one motor power. middle: motor voltage and power factor. bottom: current. Most critical for cosmic radiation induced failures is the cruise phase because of the high altitude.

1) Electric motor and propeller: The electric machine was sized based on calculations conducted within the SE^{2}A project to meet the requirements of a suitable propeller. Considering the high torque demand of the propeller, a direct drive system was deemed preferable. In this application, permanent magnet synchronous machines were chosen due to their high torque density and efficiency. To reasonably size the electrical machine for an aircraft, a fractional-slot concentrated winding with direct liquid conductor cooling was selected. This allows particularly high current densities. A current density of $50\,\mathrm{A/mm^2}$ was selected as a suitable compromise,

ensuring an increase in power density while maintaining good efficiency. The rotor is designed with spoke magnets, as these offer good protection against demagnetization and give the highest flux densities. The required voltage, current and power factor of the designed electric motor during the mission profile are depicted in Fig. 3.

2) Inverter system: One of the most promising inverter topologies for short-range aircraft propulsion systems is the active neutral-point-clamped (ANPC) inverter (see Fig. 4). The ANPC inverter has several advantages in terms of reliability for aircraft applications. Compared to a two-level inverter, a three-level inverter allows for the use of power semiconductors with lower blocking voltage capability while maintaining the same DC-link voltage level. This characteristic has the potential to reduce the risk associated with cosmic radiation, particularly considering the high DC-link voltage required to enhance the power density of the inverter system in aircraft applications [13]. Furthermore, less stress will be applied to the isolation system since smaller voltage steps can be achieved with such kind of topology. In case of single device failure, several fault-tolerant operation strategies can be applied to improve the post-fault performance [14], [15].

The selection of the DC-link voltage needs to consider the maximum line voltage during the mission profile (see Fig. 3) and the necessary derated voltage utilization on the power semiconductors to reduce the risk of random failures. In this case study, 1700 V SiC-MOSFET modules from Semikron (production line SEMITRANS 3) are chosen for the ANPC inverter. As a result, the DC-link voltage can vary between 1800 - 2200 V, which corresponds to a power semiconductor voltage utilization range of 0.529 to 0.647. To meet the power requirement, three modules are required to be placed in parallel for each switch position of the ANPC inverter. During system operation, it is assumed that the case temperature can be maintained at approximately 60 degree Celsius in this case study, which is based on the typical cooling system design for electric vehicles [16]. For this case study, a switching frequency of 30 kHz is specified. It is worth noting that for power electronic systems with higher switching frequencies, case temperatures should be kept lower to reduce the risk of wear-out failure.

B. Lifetime prediction

1) Loss model and thermal model: To derive the temperature profile of the power semiconductors for further reliability analysis, the loss model and thermal model of the inverter system need to be built. Compared with a detailed simulation model in PLECS, an analytical model is preferred for its shorter simulation time and flexibility in implementing uncertainty analysis. For the purpose of wear-out related lifetime evaluation, the junction temperature change in the power modules between 8 - 15 K is believed to mainly cause elastic deformation, which has a negligible impact on the lifetime consumption [17]. Therefore, the analytical loss model is considered accurate enough to predict the lifetime of the inverter system.

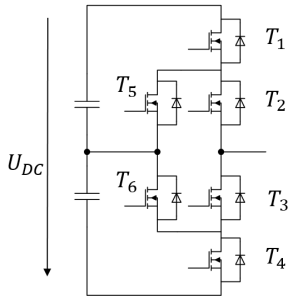

Fig. 4. One phase-leg of an ANPC inverter

TABLE I
BASIC INFORMATION OF THE INVERTER SYSTEM

DC-link voltage	1800 - 2200 V
Maximum phase current	1061 A
Switching frequency	30 kHz
power devices	1700 V SiC-MOSFET modules (Semikron SEMITRANS 3)
Modulation	Split-current PWM (see [13])

The analytical model primarily relies on mission-profile-related information, such as phase current, phase voltage, power factor, modulation index, and the inverter's design parameters, including DC-link voltage, switching frequency, and power semiconductor parameters. Additionally, it is essential to consider the feedback of the junction temperature to the loss model. The loss model and its related temperature profile are highly influenced by the chosen PWM strategy. This work implements the power-splitting PWM (see [13]) due to its high efficiency and balanced thermal distribution among the power semiconductors. The analytical model is validated using the PLECS simulation tool. Fig. 5 illustrates typical junction temperature profiles of the power semiconductors in an ANPC inverter.

2) Rainflow Algorithm: Once the junction temperature profile of each power semiconductor is obtained, the rainflow algorithm can be applied to derive the number

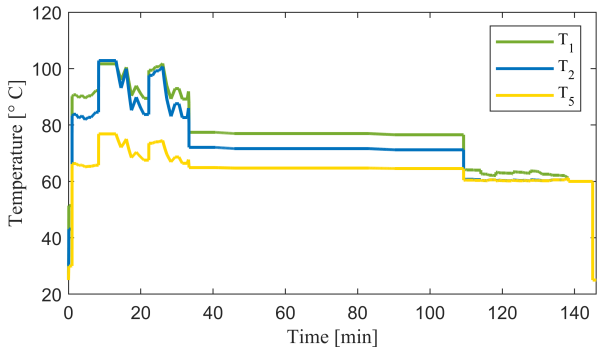

Fig. 5. Junction temperature profile of power semiconductors (T_1, T_2, T_5) in an ANPC-inverter during a mission-profile ($f_{\text{sw}} = 30\text{kHz}$, $U_{\text{DC}} = 2000\text{V}$)

of stress cycles N_{c} for the considered thermal profile, as well as the heating time t_{on} in relation to the cycle time, and the minimum junction temperature for each counted cycle $T_{\text{j,min}}$. These parameters are then utilized in the lifetime model and Miner's rule to calculate the expected lifetime of the components [18].

3) Lifetime model: The lifetime model of the power semiconductors is based on the results of power cycling tests. Various lifetime models were already introduced in previous works [2]. The LESIT lifetime model does not include the parameter of heating time t_{on} [19]. The SEMIKRON model only provides the B15 lifetime [20] (indicating that 15% of the components will fail at the end of the calculated useful life), which is not suitable for propulsion systems in aircraft application with stringent safety requirements. In contrast, the CIPS08 model contains a lot of parameters covering different module technologies. By incorporating the uncertainties given in the CIPS08 model [21], Monte-Carlo simulation can be applied to obtain the lifetime distribution and the corresponding cumulative failure probability. The number of cycles to failure N_f in the CIPS08 model is described as follows:

$$N_f = K \cdot \Delta T_{\text{j}}^{\beta_1} \cdot \exp\left(\frac{\beta_2}{T_{\text{j,min}}}\right) \cdot t_{\text{on}}^{\beta_3} \cdot I^{\beta_4} \cdot U^{\beta_5} \cdot D^{\beta_6} \quad (1)$$

where, ΔT_{j}, $T_{\text{j,min}}$, and t_{on} are the junction temperature swing, the minimum junction temperature of the stress cycle, and the heating time of the chips, respectively. U is related to the rated voltage of the power semiconductors. if a 1700 V SiC-MOSFET is implemented in this case:

$$U = \frac{U_{\text{rated}}}{100} = 1.7\,\text{V} \quad (2)$$

I in ampere and D in micrometer represent current per bond wire and bond wire diameter, respectively. I = 12 A and D = 400 μm are used as static values in this case study according to [22]. The technology factor K is set to be 3.1E+14 (a third of the standard technology factor of IGBT in CIPS08 model) for 1700 V SiC-MOSFETs, which is based on the fact that the power cycling capability is reduced by a factor of 3 - 4 on SiC-devices compared with Si-devices [23]. The thickness factor (0.33) for SiC devices in the SEMIKRON model also indicates a similar trend. It should be mentioned that the adjusted technology factor for SiC-MOSFETs still requires further investigations [24], as the CIPS08 model was primarily designed for IGBT power semiconductors. However, for the purpose of this comparative study, this value is sufficient to be used. Other coefficients $\beta_1 - \beta_6$ are summarized in Table II.

TABLE II
COEFFICIENT FOR CIPS08 LIFETIME MODEL

β_1	β_2	β_3	β_4	β_5	β_6
-4.416	1285	-0.463	-0.716	-0.761	-0.5

4) Miner's rule: Based on Miner's rule, damage accumulation Da of a certain mission-profile can be calculated with $N_{f,i}$ (number of counted cycles at ith cycle condition) and $N_{c,i}$ (number of cycles to failure at ith cycle condition):

$$Da = \sum_{i=1}^{k} \frac{N_{c,i}}{N_{f,i}} \quad (3)$$

If we assume n flight missions per day, the lifetime of the power semiconductors in years Lt can be calculated using the following equation:

$$Lt = \frac{1}{365 \cdot n \cdot Da} \quad (4)$$

In this case, we assume four flight missions per day as a reasonable value for a short-range aircraft.

5) Mont-Carlo Simulation: In practice, the lifetime of the inverter system should be expressed as a probabilistic distribution rather than a deterministic value. By employing Monte-Carlo simulations, the uncertainties associated with the lifetime parameters and thermal stress parameters can be taken into account for lifetime prediction. A 5% parameter variation with a

99% confidence level [19] is assumed in this paper. The lifetime distribution can be fitted using various probability distributions, such as weibull, lognormal, or normal distributions. The goodness of fit can be verified using the Kolmogorov-Smirnov test. In this study, it has been demonstrated that the lognormal distribution provides the best fit. By using the fitted distribution function, it becomes feasible to derive the reliability-related information such as the lifetime and failure rate of the power semiconductors.

C. Impact of reliability design rules on the wear-out failure

1) Impact of voltage derating on the wear-out failure: As mentioned earlier, cosmic radiation at high altitudes can lead to unpredictable Single Event Burnout effects. To reduce the risk of Single Event Burnout effect induced random device failure, necessary voltage derating on the power semiconductor is required. However, it is important to note that such design considerations indirectly affect the thermal stresses experienced by the power semiconductors, which in turn can impact their wear-out effect and the overall lifetime. Therefore, when implementing variable DC-link voltage strategies [25] to reduce random device failures caused by cosmic radiation, it is essential to analyze the potential impact on wear-out failures as well.

To analyse the impact of DC-link voltage on the wear-out effect of the power semiconductors, a range of DC-link voltage values (1800 - 2200 V) is selected for the lifetime evaluation of the ANPC inverter. Other design constraints remained unchanged. Due to the symmetric performance behavior of the ANPC inverter, only T_1, T_2, and T_5 are chosen for further analysis. As depicted in Fig. 6, a reduced DC-link voltage slightly decreases the wear-out related lifetime of T_1 and T_2. This decrease is primarily attributed to higher conduction losses and the resulting higher junction temperature. Since the wear-out effect of T_5 during the first 30 years is not significant due to its low power losses, the impact of varying the DC-link voltage on the wear-out effect of T_5 is considered negligible.

2) Impact of scalable chip size: Minimization of the chip size is one of the methods to reduce the risk of random failure caused by SEB. However, changing the chip size can also impact the thermal behavior of power semiconductors and, consequently, their wear-out effect. A scaling factor can be introduced to investigate the impact of chip size A_{Chip} on the lifetime of the inverter system, as discussed in previous works [5], [6]. It should be noted that the same lifetime model can still be used

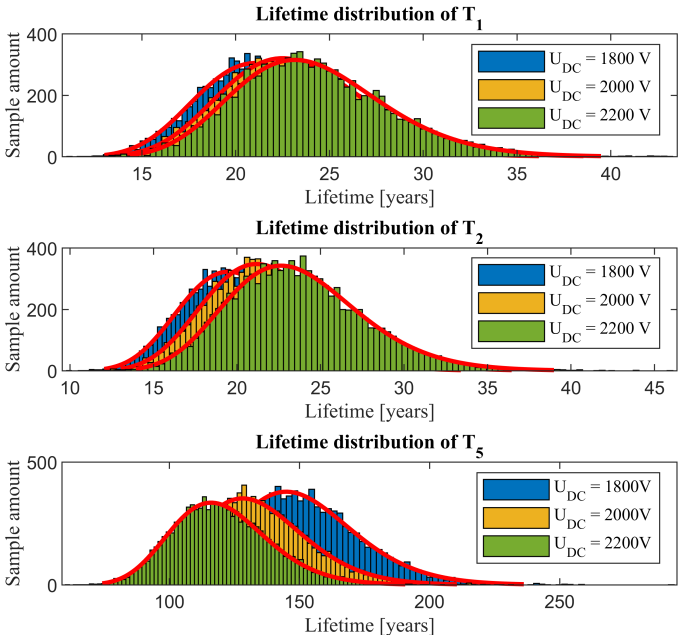

Fig. 6. Impact of DC-Link voltage variation on wear-out related lifetime distribution (power splitting PWM, f=30 kHz, 10000 samples in Monte-Carlo simulation)

for power semiconductors with different chip areas for further investigation, as stated in [20]. The scaling factor is defined as the ratio of the newly defined chip size A_{Chip} to the reference chip size $A_{\text{Chip,Ref}}$:

$$SF = \frac{A_{\text{Chip}}}{A_{\text{Chip,Ref}}} \tag{5}$$

The turn-on-resistance $R_{\text{DS(on)}}$, the thermal resistance R_{th} and the switching energy E_{sw} of the power semiconductors can be described by the following equations:

$$R_{\text{DS(on)}} = \frac{R_{\text{DS(on),Ref}}}{SF} \tag{6}$$

$$R_{\text{th}} = \frac{R_{\text{th,Ref}}}{SF} \tag{7}$$

$$E_{\text{sw}}(SF, U_{\text{DC}}, I, T_{\text{j}}) = E_{\text{s,Ref}}(U_{\text{DC}}, \frac{I}{SF}, T_{\text{j}}) \cdot SF \tag{8}$$

As it can be seen from Fig. 7, the wear-out related lifetime of the power semiconductors with a scaling factor larger than one can be obviously extended, as the thermal stress on the power semiconductors is reduced. However, the increased chip size also leads to an increase in the random failure rate induced by cosmic radiation. This conflict between improving system reliability and the unified analysis of these factors will be discussed in the next paragraph.

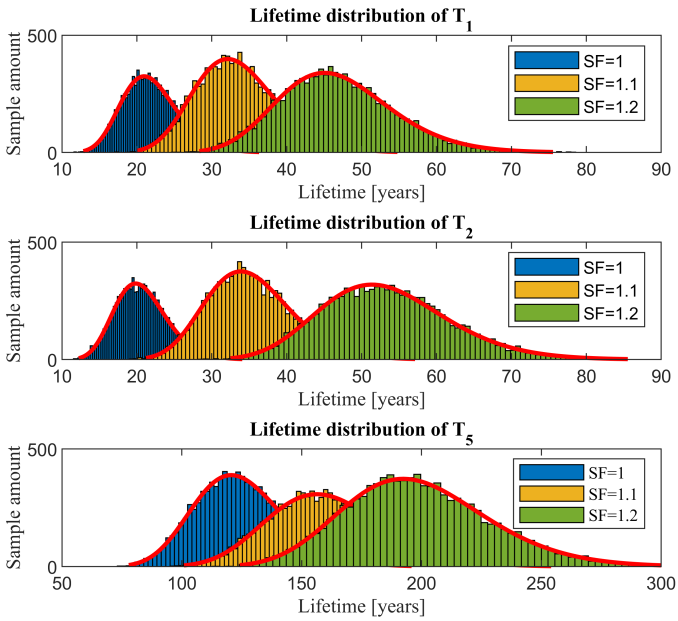

Fig. 7. Wear-out related lifetime distribution of power semiconductors with scalable chip area (power splitting PWM, $U_{\mathrm{DC}} = 2000\,\mathrm{V}$, f=30 kHz, 10000 samples in Monte-Carlo simulation). SF: chip area scaling factor.

IV. System Reliability Analysis

As mentioned earlier, reliability design rules, such as derated voltage utilization and scalable chip size, can lead to a conflict of objectives in terms of reducing the risk of random device failure and decreasing the wear-out effect of power semiconductors (see Table III). Additionally, the B_x lifetime is not only related to wear-out failure probability but also to random failure probability. In such cases, it becomes necessary to conduct an overall system reliability analysis, considering different design parameters and taking into account these two objectives.

TABLE III
Reliability Design Conflict in Power Semiconductors for Aircraft Propulsion Applications

Design parameter	Random failure	Wear-out failure
Chip area ↓	↓	↑
DC-link voltage ↓	↓	T_1↑ T_2↑ T_5↓ in this case
Junction temperature ↓	IGBT ↑ SiC-MOSFET ?*	↓

*: Further experimental investigations are needed

With the aid of Monte-Carlo simulation, the probability density function of failure distribution $f_{\mathrm{w}}(x)$ and its corresponding cumulative failure probability $F_{\mathrm{w}}(x)$, resulting from the wear-out failure of the power semiconductor, can be obtained from the wear-out related lifetime distribution. The wear-out related failure rate λ_{w} of the power semiconductor is defined as follows:

$$\lambda_{\mathrm{w}}(t) = \frac{f_{\mathrm{w}}(t)}{1 - F_{\mathrm{w}}(t)} \tag{9}$$

The failure rate of all the power semiconductors λ_{All} in an ANPC inverter, taking into account the failure rate induced by cosmic radiation λ_{r} and the failure rate due to thermo-mechanical effects λ_{w}, can be calculated as follows:

$$\lambda_{\mathrm{All}}(t) = \lambda_{\mathrm{r}}(t) + \lambda_{\mathrm{w}}(t) \tag{10}$$

with:

$$\lambda_{\mathrm{r}} = 6 \cdot n \cdot A_{\mathrm{T}} \cdot (k_{T_1} \cdot \lambda_{r,pA} + k_{T_2} \cdot \lambda_{r,pA} + k_{T_5} \cdot \lambda_{\mathrm{r,pA}}) \tag{11}$$

and

$$\lambda_{\mathrm{w}}(t) = 6 \cdot n \cdot (\lambda_{\mathrm{w},T_1}(t) + \lambda_{\mathrm{w},T_2}(t) + \lambda_{\mathrm{w},T_5}(t)) \tag{12}$$

where $\lambda_{\mathrm{r,pA}}(t)$ represents the failure rate induced by cosmic radiation per unit chip area, which is dependent on the flight altitude, the rated voltage, and the voltage utilization (see Fig. 1) of the power semiconductor. A_{T} is the chip area, which can be approximately estimated using the fitted curve based on the rated voltage and the area-specific on-resistance from [13] or obtained from the power semiconductor producer. The on-resistance is provided in the datasheet. In this case, 3 parallel (n = 3) SiC-MOSFET modules per switch position are implemented in the case study. Additionally, the failure rate of the power semiconductor induced by cosmic radiation mainly occurs during the blocking state, where the implemented PWM strategy plays a crucial role. In Eq. (11), blocking time ratios ($k_{T_1} = 0.75$, $k_{T_2} = 0.25$, $k_{T_5} = 0.25$) for T_1, T_2, and T_5 are introduced, respectively, based on the blocking times of the implemented current-splitting PWM strategy. As the thermal distribution of power semiconductors in an ANPC inverter is uneven, the wear-out effect on T_1, T_2, and T_5 differs, leading to different wear-out related failure rates ($\lambda_{\mathrm{w},T_1}(t)$, $\lambda_{\mathrm{w},T_2}(t)$, λ_{w,T_5}).

In practical applications, the failure rate requirement is allocated based on the failure rate requirement on the system level. Considering that the current failure rate of a propulsion system for a large passenger aircraft is approximately 1000 FIT, it is crucial to ensure that the failure rate of an inverter system remains below several hundreds FIT. In this case study, we have set the upper

limit of the failure rate of all power semiconductors in an ANPC inverter to be 100 FIT (example see Fig. 8). Due to the stringent aircraft safety requirement, $B_{0.1}$ lifetime is used in the system level reliability analysis (example see Fig. 9). Other subcomponents, such as gate drivers, capacitors, and PCBs, are not included in the reliability analysis.

The reliability analysis in this study incorporates the mutual impact between random failures and wear-out failures within a framework, while considering various design parameters. The wear-out failure and random failure can be considered as subsystems within a serial system reliability analysis. As shown in Table IV and Fig. 11, when the DC-link voltage is kept under 2000 V, increasing the scaling factor leads to an extended lifetime of the power semiconductors. This extension is primarily attributed to the reduction in thermo-mechanical stress, while the failure probability induced by single Event Burnout (SEB) is not the dominant factor. However, when the DC-link voltage exceeds 2000 V, the $B_{0.1}$ lifetime may be limited by the random failure before the wear-out effect occurs. This is due to the increased failure probability caused by Single Event Burnout (SEB) at high voltage utilization (see Fig. 10). As a result, the benefits of reduced wear-out effect resulting from high DC-link voltage become negligible. It should be mentioned that the derived $B_{0.1}$ lifetime in this context does not reflect the degradation of the power semiconductors. As the scaling factor increases, the $B_{0.1}$ lifetime can also be limited by random failures even if the inverter has a low DC-link voltage. A notable example is the inverter design parameters with SF = 1.2 and $U_{\mathrm{DC}} = 1900\,\mathrm{V}$ in Table IV. These results once again emphasize the importance of analyzing system reliability considering both wear-out failure and random failure within a unified framework. Based on the requirement of a $B_{0.1}$ lifetime of 15 years and a failure rate of 100 FIT, the optimal choice to minimize oversizing would be a DC-link voltage of 1900 V and a scaling factor of 1.1, as indicated in Table IV and Fig. 11. It is important to note that in aircraft applications, reliability is not the sole pursuit objective for power electronic systems. Other design objectives such as high efficiency and high power density must also be considered during the inverter design phase. A flowchart illustrating the reliability-oriented design process is proposed in Fig. 12.

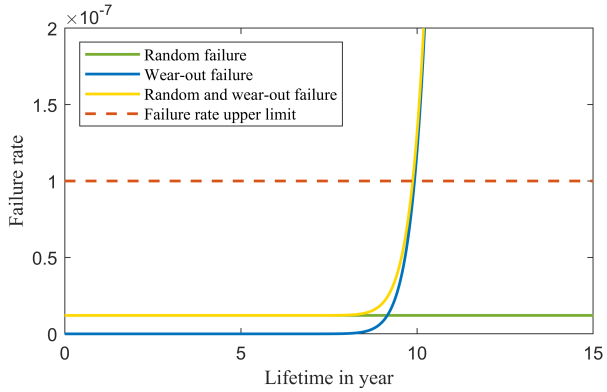

Fig. 8. Failure rate of all power semiconductors in an ANPC inverter ($U_{\mathrm{DC}} = 1900\,\mathrm{V}, SF = 1$)

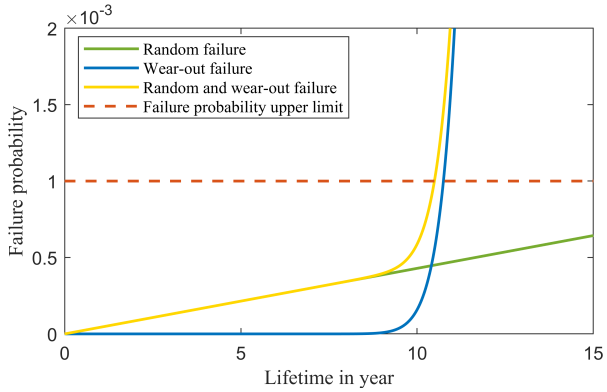

Fig. 9. Failure probability of all power semiconductors in an ANPC inverter ($U_{\mathrm{DC}} = 1900\,\mathrm{V}, SF = 1$). The $B_{0.1}$ lifetime is defined based on a failure probability upper limit of 0.1%.

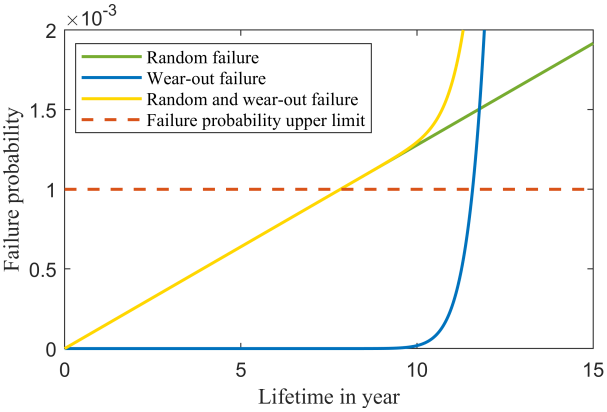

Fig. 10. Failure probability of all power semiconductors in an ANPC inverter ($U_{\mathrm{DC}} = 2100\,\mathrm{V}, SF = 1$), $B_{0.1}$ lifetime is mainly limited by the random failure.

V. Conclusion

This study focuses on the analysis and implementation of several reliability design rules for an ANPC inverter in a short-range electric aircraft propulsion system. The main focus is on the reliability of power semiconductors, which exhibit an objective conflict doing reliability-oriented design. The random device

TABLE IV
$B_{0.1}$ LIFETIME AND 100 FIT RELATED LIFETIME OF THE INVERTER WITH DIFFERENT DESIGN PARAMETERS

U_{DC} [V]	SF	$B_{0.1}$ Lifetime [year]	lifetime limited by λ_{min} [year]
1800	1	10.17	9.47
1900	1	10.56	9.95
2000	1	10.66	10.36
2100	1	7.78*	10.49
1800	1.1	16.94	16.30
1900	1.1	16.96	16.92
2000	1.1	12.32*	17.23
2100	1.1	7.11*	16.30
1800	1.2	24.20	24.30
1900	1.2	19.46*	24.78
2000	1.2	11.26*	24.94
2100	1.2	6.62*	24.78

*: These lifetimes are limited by random failures (e.g.: Fig. 10). Blue marked numbers: lifetimes that satisfy both reliability requirements (λ_{min}, F_{min}) for the given parameters.

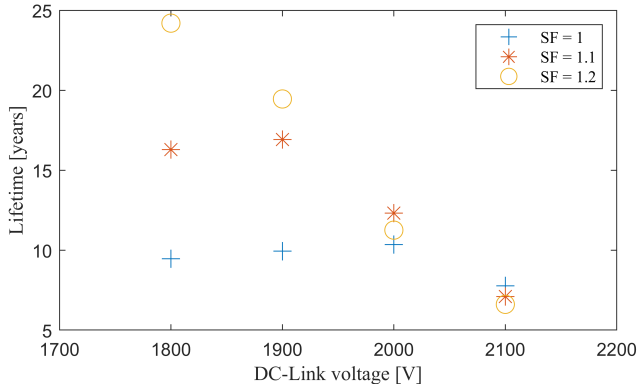

Fig. 11. Lifetime dependency on DC-Link voltage and chip area scaling factor with data based on Table IV

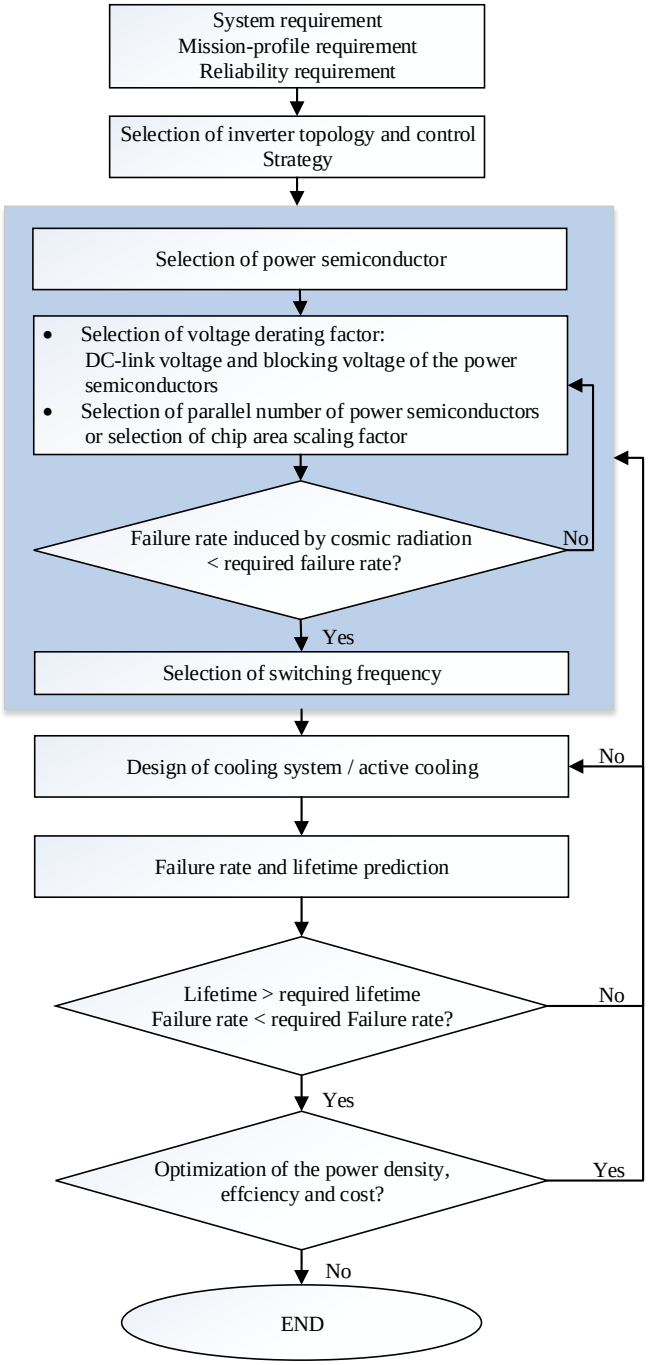

Fig. 12. Reliability-oriented design rules for power semiconductors in an ANPC inverter for aircraft applications

failure rate is determined based on existing test results, while the wear-out effect is analyzed using a mission-profile-based lifetime model. This model incorporates analytical loss and thermal models developed in MATLAB&SIMULINK, which have been validated in PLECS. By employing strategies such as minimizing chip size and reducing voltage utilization of power semiconductors, the risk of random device failure induced by cosmic radiation can be reduced. However, these design rules can lead to increased wear-out effects due to additional thermal stress on the power semiconductors. To achieve the desired reliability objectives and select appropriate inverter design parameters, an overall system reliability analysis method is introduced that takes into account wear-out failure, random failure and their mutual impacts. The case study results demonstrate that increasing the chip area scaling factor can extend the $B_{0.1}$ lifetime, particularly when the DC-link voltage is low. Despite the slight additional wear-out effect associated with derated DC-link voltage, maintaining a low DC-link voltage can still effectively reduce the failure probability

caused by Single Event Burnout (SEB) and prevent it from limiting the $B_{0.1}$ lifetime.

However, it should be mentioned that the analysis does not consider other failure mechanisms of the power semiconductor, such as gate-oxid degradation, bipolar diode degradation, degradation induced by vibration, etc. Furthermore, future work requires more accurate power cycling tests to derive the lifetime model for SiC-MOSFETs with higher blocking voltage.

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