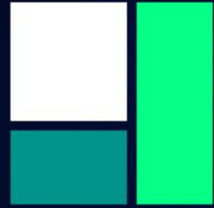


Digital

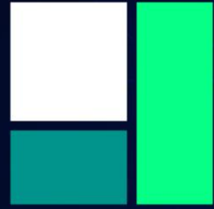
Power Semiconductor Reliability Round Table

October 12, 2023

Powered by:

in cooperation with:

Digital

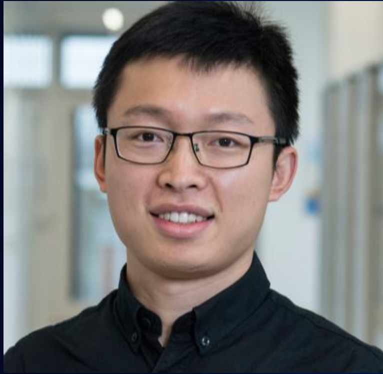


Power Semiconductor
Reliability Round Table

Reproducible Thermal Structure Analysis for SiC MOSFETs

Powered by:

in cooperation with:



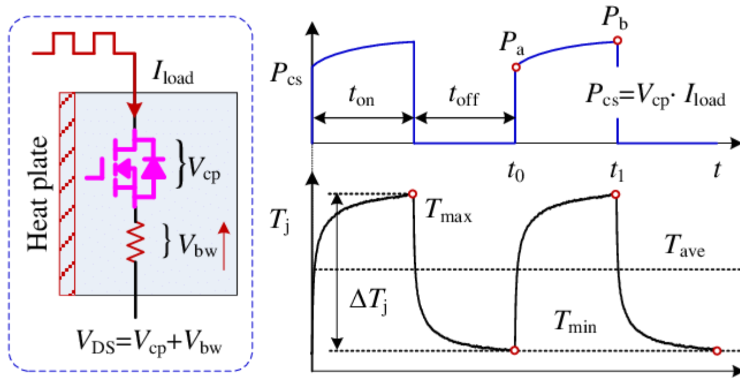
Yi Zhang

Assistant Professor, Aalborg University, Denmark

E-Mail: yiz@energy.aau.dk

Research: reliability modeling, testing, and thermal characterization of power electronics

Thermal characterization during power cycling



Source: H. Luo (2019)

Table 9.3: EOL criteria PC_{sec}

Parameter		**Change from standard value**
Increase of forward voltage	IGBT: $V_{CE,sat}$ MOSFET: V_{DS} Diode: V_F, V_{FSD}	+5% [a]
Increase of thermal resistance	$R_{th,j\text{-}c}$, $R_{th,j\text{-}s}$, $R_{th,j\text{-}f}$ [b] optionally ΔT_{vj}	+20%

[a] Note: See also the notes on the settling process under test conditions

[b] Note: It has to be ensured (e.g. by comparison with Z_{th} curve in the datasheet) that the duration of temperature rise is sufficient for the calculation of static R_{th}, or an additional online R_{th} measurement should be performed without removing the power modules from the test bench, when TIM or a baseplate is part of the DUT.

Source: AQG 324

Why we need to do thermal characterization along power cycling?

- Continuously capture failure mechanisms
- Justify end-of-life

Thermal characterization based on TSEP

Comply standards: JEDEC JESD 51-1, 51-14

Step 1: temperature calibration

Cooling plate

Measured V_{sd}

Temperature (T)

I_{sense}

d

g

s

V

V_{gsoff}

Temperature control unit

Step 2: cooling curve measurement

Current

I_{heat}

Heating

Cooling

I_{sense}

$t = 0$

$V_{sd}(T)$

t

I

V

Electrical transient

Thermal transient

A

t=0

I_{heat}

I_{sense}

V_{gson}

V_{gsoff}

d

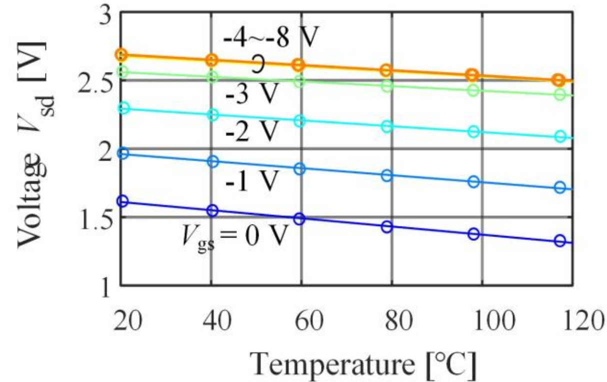
g

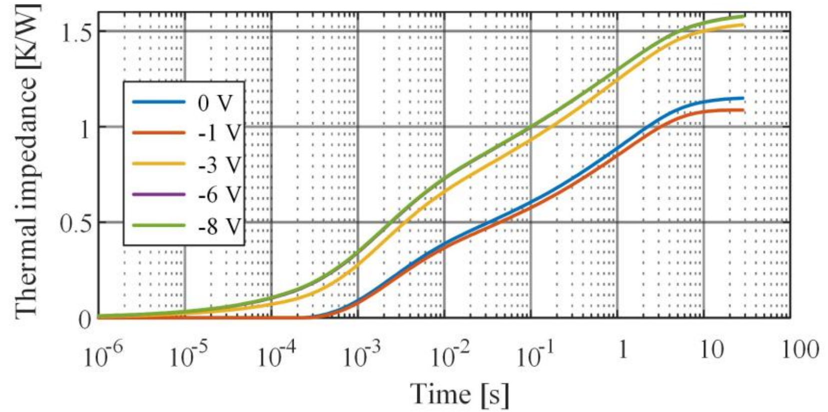
s

V

Temperature control unit

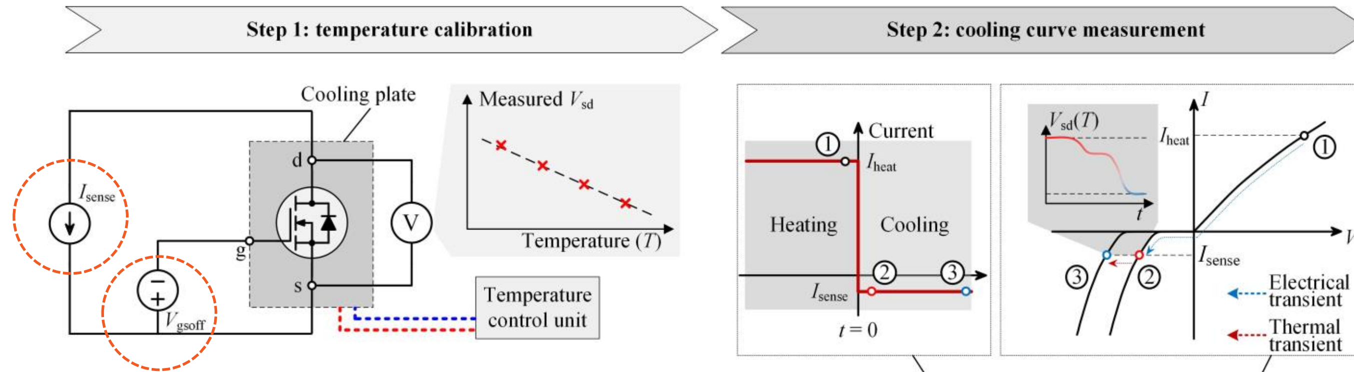
A problem for SiC MOSFETs





- Which is the correct thermal impedance?
- Can obtaining a well-calibrated curve guarantee the acquisition of accurate temperature information?

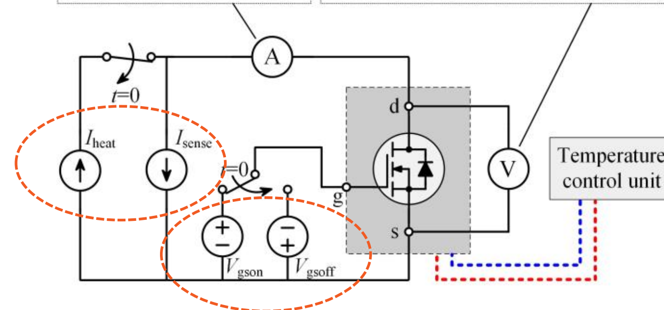
Thermal characterization based on TSEP



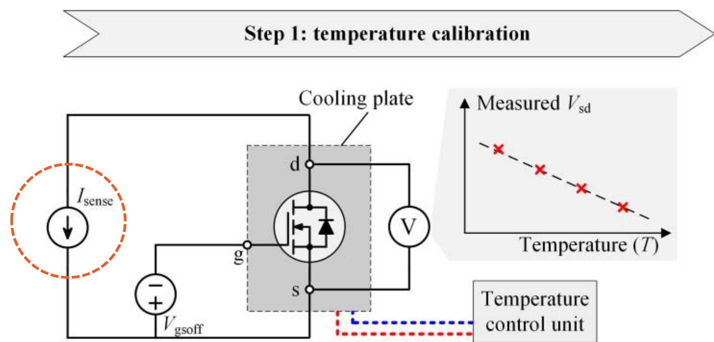
Calibration: build a static relation $V_{sd}=f(T)$

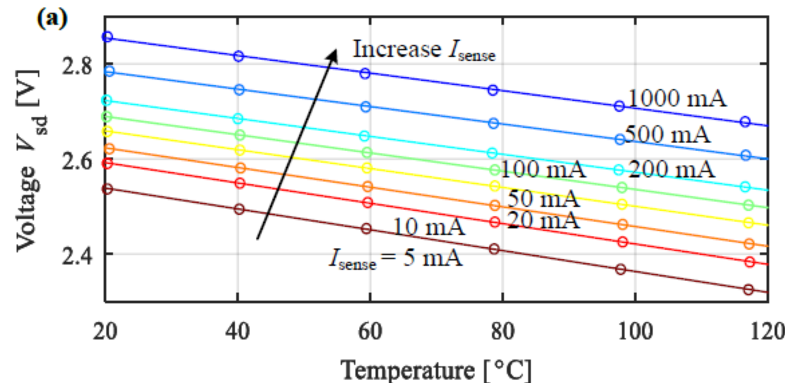
Feasibility? Limitations?

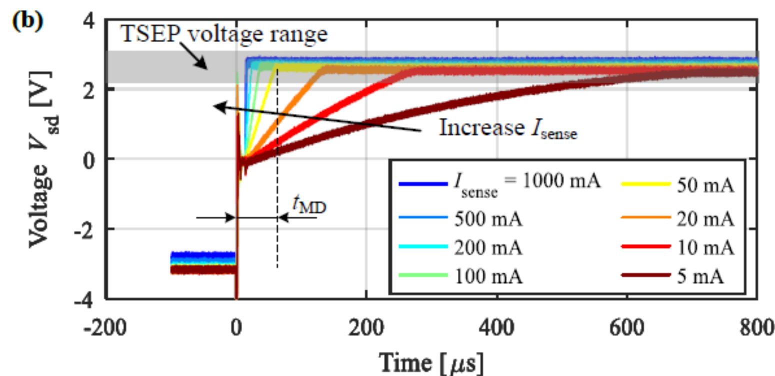
Cooling curve measurement: capture $V_{sd}(t)$ and translated into $T(t)$



Calibration under different sensing current







Sensing current:

- Small enough → self-dissipation
- Large enough → measurable voltage

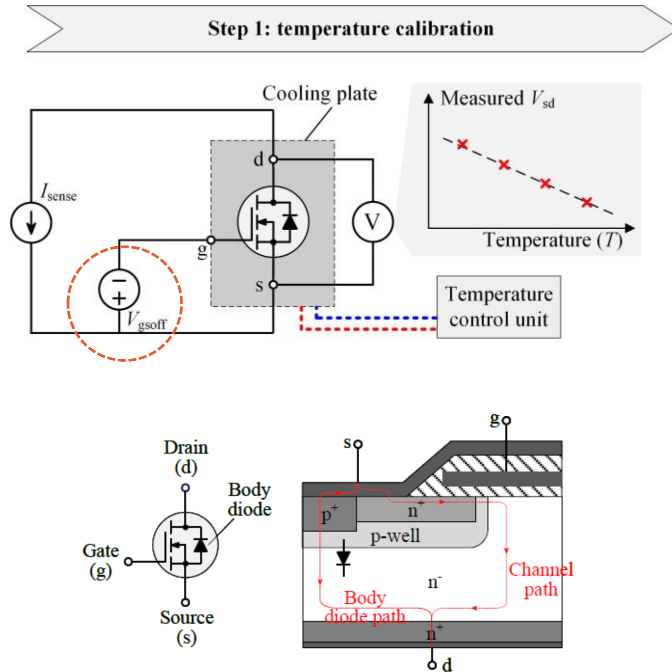
Quantitative criteria to justify testing conditions

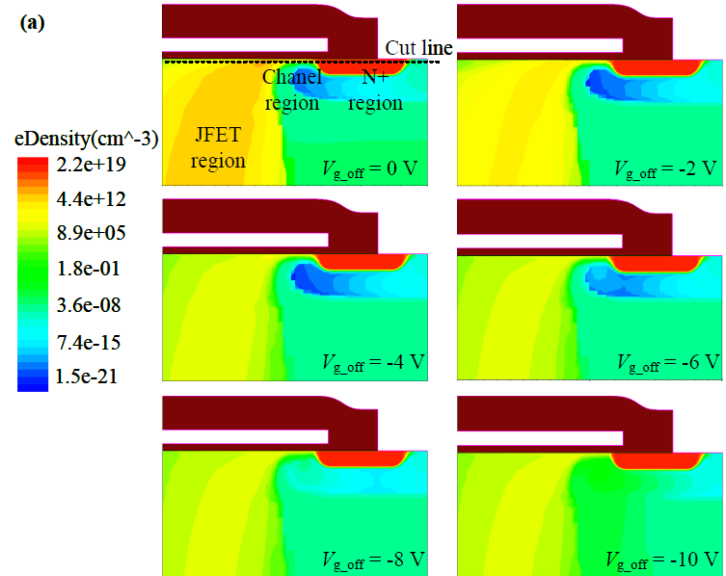
Key indicators

- Linearity $\rho_{\text{linear}} = \left| \frac{\text{cov}(V_{sd}, T)}{\sigma_{V_{sd}} \cdot \sigma_T} \right|$
- Resolution $K_{\text{res}} = \frac{\Delta V_{sd}}{\Delta T}$ [mV/K]
- Self Dissipation Ratio $\eta_{sd} = \frac{P_{sense}}{P_{rate}}$
- Delay time t_{MD}

I_{sense} [mA]	Linearity	Resolution [mV/K]	Self dissipation ratio	t_{MD} [μs]
	$V_{\text{gsoff}} = -6$ V (related to §III-A, III-B)			
5	0.999948	2.192245	0.022%	663
10	0.999945	2.139215	0.045%	268
20	0.999954	2.068415	0.091%	139
50	0.999968	1.983309	0.230%	62
100	0.999995	1.918120	0.467%	42
200	0.999940	1.884273	0.943%	28
500	0.999678	1.835086	2.411%	20
1000	0.999415	1.847177	4.947%	19
	static			*dynamic*

Calibration under different gate voltages

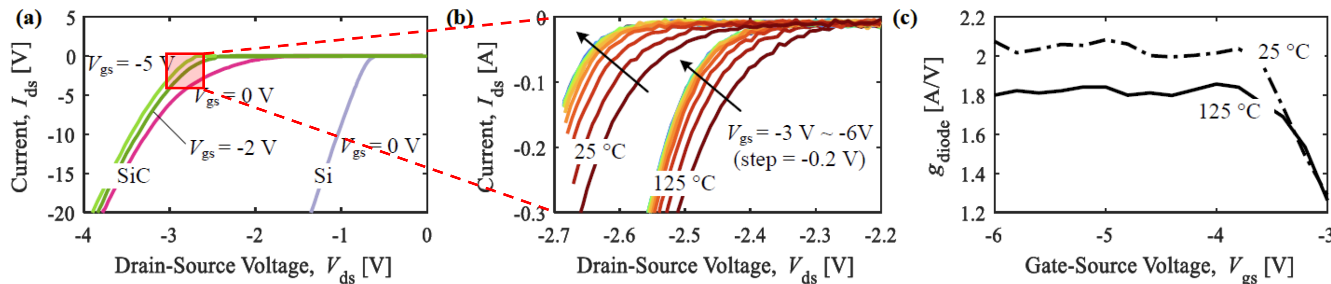




ReliaPEC Group | Aalborg University | Yi Zhang, yiz@energy.aau.dk

Two methods to justify gate voltage

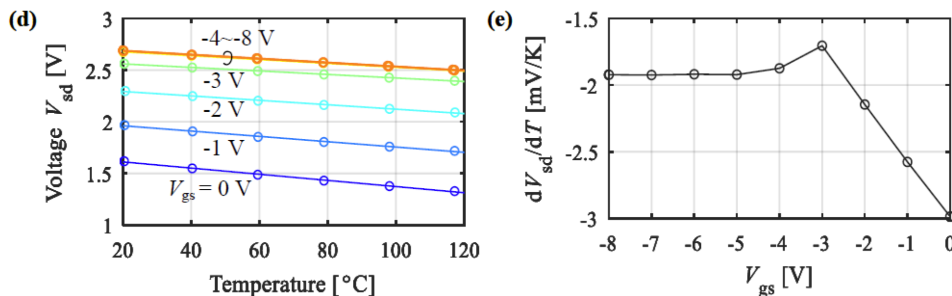
Method 1: Output Characteristics under Sensing Current



$$g_{diode} = \left.\frac{dI_{ds}}{dV_{ds}}\right|_{I_{ds}=I_{sense}}$$

$$\frac{\partial g_{diode}}{\partial V_{gs}} = 0$$

Method 2: Calibration Curves with Varied Gate Voltages



$$\frac{\partial}{\partial V_{gs}}\left[\frac{\partial V_{sd}(T)}{\partial T}\right] = 0$$

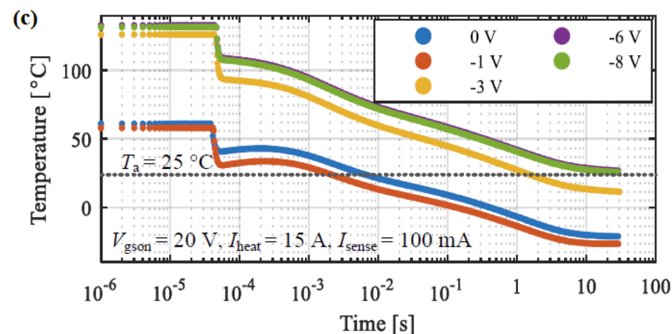
ReliaPEC Group | Aalborg University | Yi Zhang, yiz@energy.aau.dk

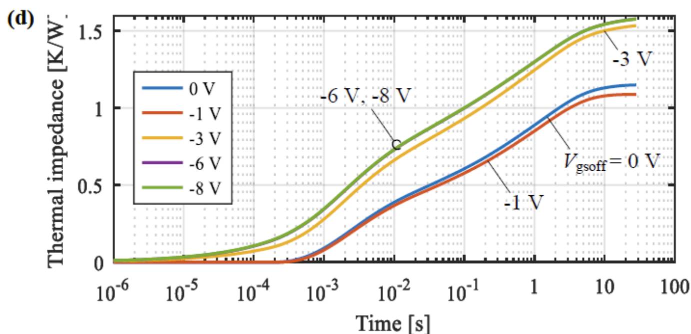
Different SiC MOSFETs

	Device 2	Device 3	Device 4
Determine V_{gsoff}	dV_{sd}/dT [mV/K] vs. V_{gs} [V]; V_{gsoff} = -7 V	V_{gs} [V]; V_{gsoff} = -10 V	V_{gs} [V]; V_{gsoff} = -13 V
Determine I_{sense} (t_{MD})	Voltage V_{sd} [V] vs. Time [μs]; 1000 mA, 500 mA, 200 mA, 100 mA, 50 mA, 20 mA, 10 mA, 5 mA	Time [μs]; 1000 mA, 500 mA, 200 mA, 100 mA, 50 mA, 20 mA, 10 mA, 5 mA	Time [μs]; 1000 mA, 500 mA, 200 mA, 100 mA, 50 mA, 20 mA, 10 mA, 5 mA

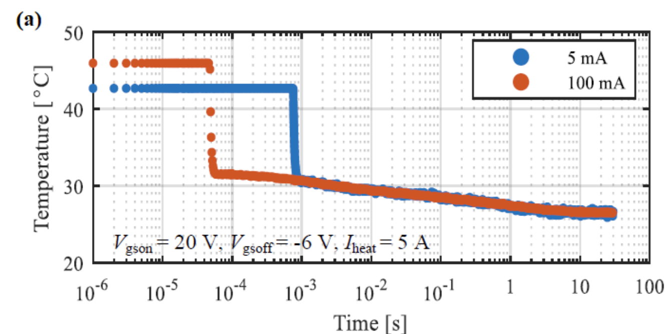
Testing results (1)

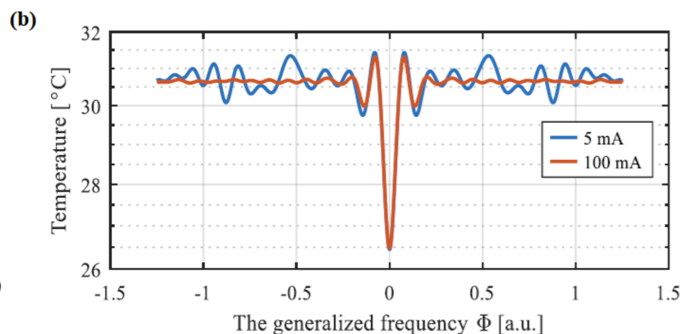
Impact of Gate Turn-Off Voltage





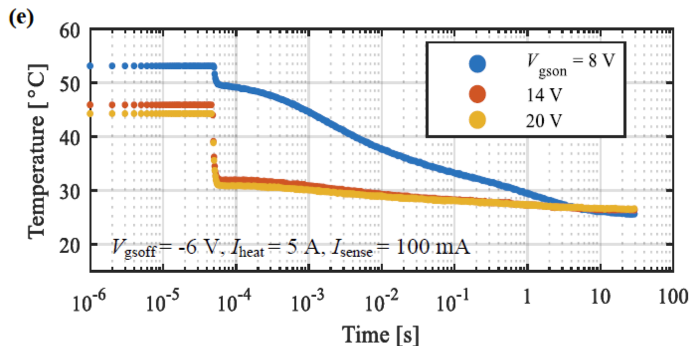
Impact of Sensing Current

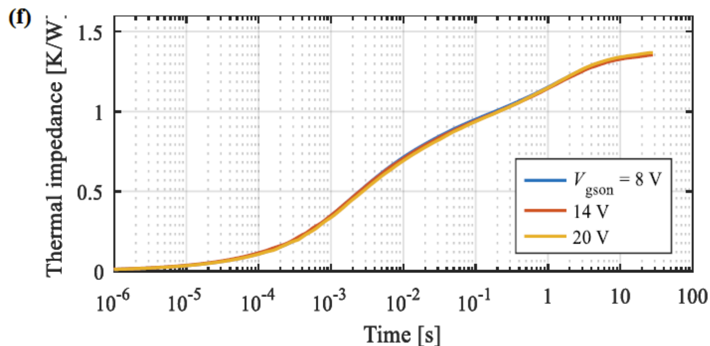




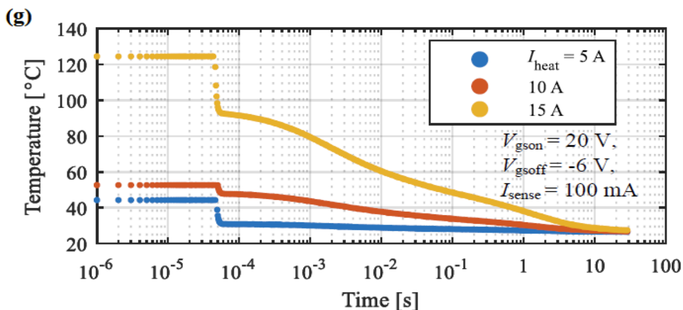
Testing results (2)

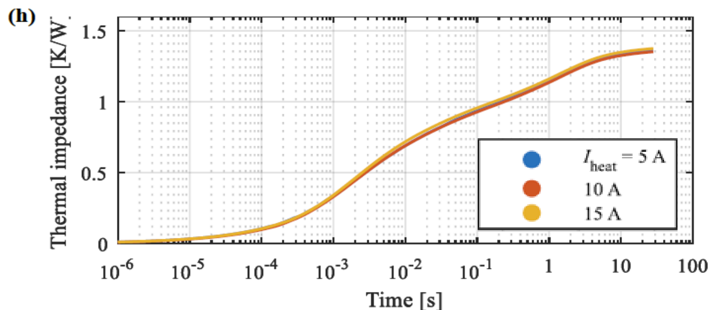
Impact of Gate Turn-On Voltage



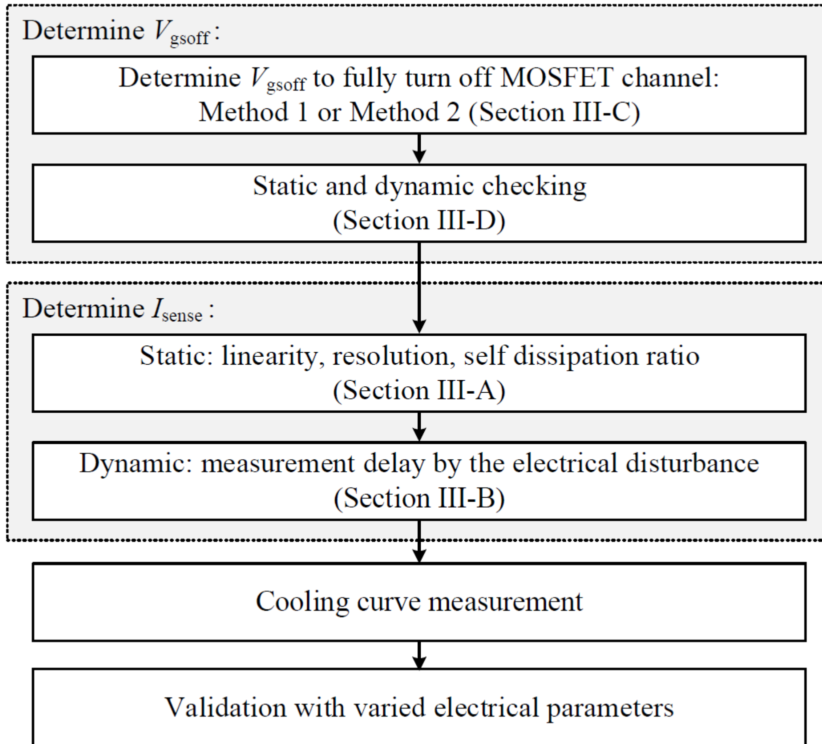


Impact of Heating Current

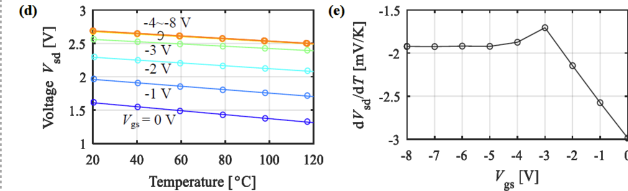


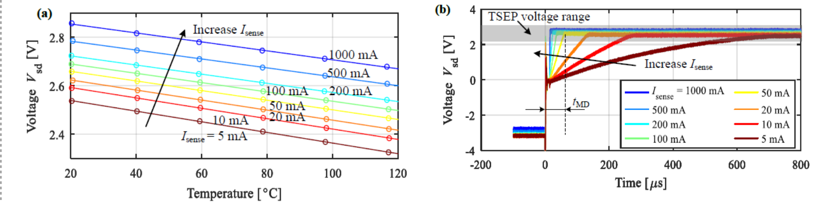


A guideline for SiC thermal characterization



Calibration Curves with Varied Gate Voltages





ReliaPEC Group | Aalborg University | Yi Zhang, yiz@energy.aau.dk

Wrap-up

Lessons from our measurements:

- A well-calibrated Vsd=f(T) cannot guarantee reproducible thermal measurement
- Quantitative methods are necessary to determine proper conditions
  - I_{sense}: four factors in terms of static and dynamic
  - $V_{gs,off}$: two methods find the sufficient gate turn-off voltage
  - $V_{gs,off}$ = -6 V does not apply for all devices
- Careful about the TSEP method! You don't measure temperature directly!

Read more about this work:
Zhang, Y., Zhang, Y., Xu, Z., Wang, Z., Wong, H., Lu, Z. and Caruso, A., 2023, March. "A Guideline for Silicon Carbide MOSFET Thermal Characterization based on Source-Drain Voltage". *In 2023 IEEE Applied Power Electronics Conference and Exposition (APEC)* (pp. 378-385). IEEE.

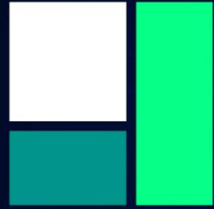
Acknowledgements

- Students: Yichi Zhang, Zhiliang Xu
- Siemens: Hon Wong, Antonio Caruso
- Nexperia: John Wang

DANMARKS FRIE FORSKNINGSFOND
INDEPENDENT RESEARCH FUND DENMARK

Read more about this work:

Zhang, Y., Zhang, Y., Xu, Z., Wang, Z., Wong, H., Lu, Z. and Caruso, A., 2023, March. “A Guideline for Silicon Carbide MOSFET Thermal Characterization based on Source-Drain Voltage”. *In 2023 IEEE Applied Power Electronics Conference and Exposition (APEC)* (pp. 378-385). IEEE.



Digital

Power Semiconductor Reliability Round Table

Thank you!