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***Abstract*—Capacitive parasitic couplings in power electronics systems are gaining increased attention due to the emergence of the wide bandgap devices, with the main challenges being faster switching speeds and increased operating voltage capabilities causing increased voltage slew rate (dv/dt). The high dv/dt induces capacitive displacement currents through the channel of the power semiconductor devices, effectively reducing the switching speed, resulting in an increase in the Volt-Ampere integral, incurring surplus switching energy dissipation. This paper highlights that the parasitic power module gate high side capacitance should be analyzed in parallel to the high-side gate-drain capacitance and thus contributing to the "equivalent" high-side Miller capacitance, slowing down the switching speed of the high-side device compared to the low-side device in the half-bridge power module. Effectively this causes an imbalance in switching energy dissipation between high-side and low-side devices. A combined physics based and behavioural based digital twin simulation is used to evaluate high-side and low-side switching energy dissipation through double pulse testing. Simulations identify a significant increase in turn-on energy on the high-side device compared to the low side device, due to the equivalent high-side Miller capacitance increase. Possible reasons for why such significant deviation in switching energy dissipation between the high-side and low-side devices is unprecedented, are shared from the authors perspectives.**

***Index Terms*—Capacitive couplings; SiC MOSFET; Half-bridge switching dynamics; Miller capacitance; Switching losses; Power module modelling; Digital twin simulations**

I. Introduction

CAPACITIVE couplings in Power Electronics Converters (PECs) have gained increased interest due to the emergence of the Wide Bandgap (WBG) power semiconductor devices [1], [2]. The WBG devices are intrinsically superior to the prevalent Silicon (Si) based power semiconductor components, with higher breakdown voltage, lower on-resistance, faster switching speeds and increased operating temperatures [3]. Because of this, multiple industry segments, e.g. traction [4]–[6], wind [7]–[9] and induction heating industries [10]–[12] are exploiting the advantages of the Silicon Carbide (SiC) power MOSFETs. In prevalent Si-based PEC systems, minimizing parasitic inductance has been of main concern due to high di/dt and slow switching speed (dv/dt) [13]. However, with the fast switching speeds of the SiC devices and the potential to increase operating voltage levels the design regime of modern power converters is shifting towards minimizing parasitic capacitive couplings due to high dv/dt causing high-frequency, high amplitude capacitive displacement currents in the power electronics converter systems [14].

The intrinsic power semiconductor capacitive couplings, their modelling methods and their impact on device transient switching performance, including the Miller region switching dynamics, have been studied in great detail in [15]–[21]. Similarly, the power module layout parasitic capacitive couplings and their impact on the semiconductor switching performance have been studied in [22]–[26]. As these capacitive couplings are often present in the switching power loop of the SiC semiconductor devices, the capacitive displacement currents will be discharging/charging the capacitive couplings through the channel of the power semiconductor devices, which causes additional joule heating of the devices from; 1) An effective reduction in device switching speed which will results in surplus switching losses from the increase of the Volt-Ampere integral [27] and 2) the displacement currents through the channel of the semiconductors, will increase the switched current amplitude and thus incur surplus switching and conduction losses [28]. However, in the both industry and academia the semiconductor switching losses, which are affected by the capacitive couplings, are assumed identical for the high-side and low-side power semiconductors in the half-bridge configured power module [29]–[31].

This paper will show that the high-side and low-side power semiconductor switching losses are not identical in a $10\,\mathrm{kV}$ SiC half-bridge power module, due to higher operating voltage levels and switching speeds and the power module parasitic capacitive couplings affecting the Miller region charging dynamics of the high-side SiC MOSFET. This results in an increase of energy dissipation on the high-side causing an imbalance in semiconductor switching losses with higher losses on the high-side device compared to the low-side device.

The paper is organized as follows. In Sec. II the parasitic capacitive couplings of MOSFET and power module packaging will be modelled, the contributions of different relevant parasitic capacitive couplings on the SiC MOSFET switching dynamics will be illustrated and the impact of the defined "equivalent" Miller capacitance on the MOSFET switching speed will be analytically derived. Through a simulation case study of the $10\,\mathrm{kV}$ SiC MOSFET power module the difference

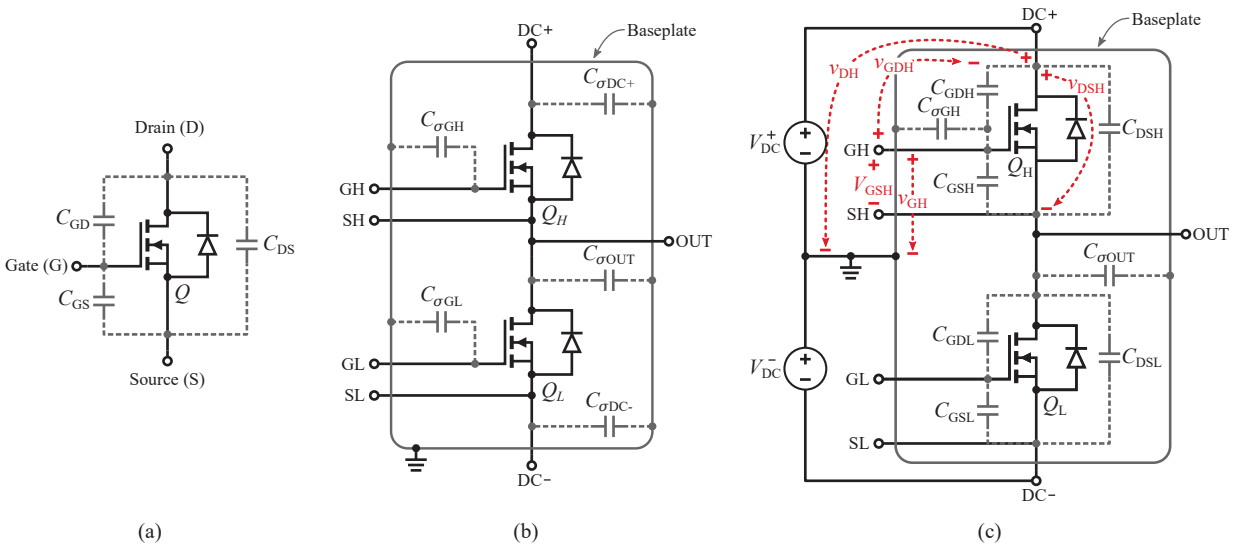

Fig. 1: (a) MOSFET intrinsic capacitive couplings [20]. (b) Half-bridge power module parasitic capacitive couplings [25]. (c) Equivalent MOSFET and half-bridge power module capacitive couplings.

between high-side and low-side equivalent Miller capacitance will be highlighted in Sec. III, where physics based FEM extractions are used for a digital twin model of the 10 kV SiC MOSFET power module. To validate the hypothesis of a turn on energy dissipation imbalance between high-side and low-side MOSFET caused by the shown difference in equivalent Miller capacitance, a sensitivity analysis is presented where the turn-on energy increase is related to the increase in the equivalent high-side Miller capacitance, by sweeping the gate-high capacitance.

II. Half-bridge SiC MOSFET Power Module Modelling

A. Power MOSFET Modelling

The capacitive couplings of a power MOSFET can be modelled using the intrinsic capacitance model, as illustrated in Fig. 1a. The capacitances C_{GD} and C_{DS} are typically modelled as being voltage dependent and C_{GS} is assumed constant. The charging dynamics of the MOSFET is governed by these three capacitances. During turn-on, the Miller region charging dynamics for the MOSFET is being governed by the charging of the gate-drain capacitance which is also referred to as the Miller capacitance. In the Miller region a stationary condition is reached where the gate-source voltage is clamped to the Miller voltage level V_{mil} and the Miller capacitance is charged through the gate. The gate current I_G is thus limited by the gate resistance R_G, yielding a constant gate current as illustrated in (1).

$$I_G = \frac{V_G - V_{mil}}{R_G} \tag{1}$$

During the Miller region C_{GD} and C_{DS} are considered in parallel and thus Kirchhoff's current law dictates that the charging of the drain-source capacitance is forced to follow the charging of the gate-drain capacitance yielding an approximately constant dv/dt on the drain-source voltage until the on-state forward voltage is reached [15].

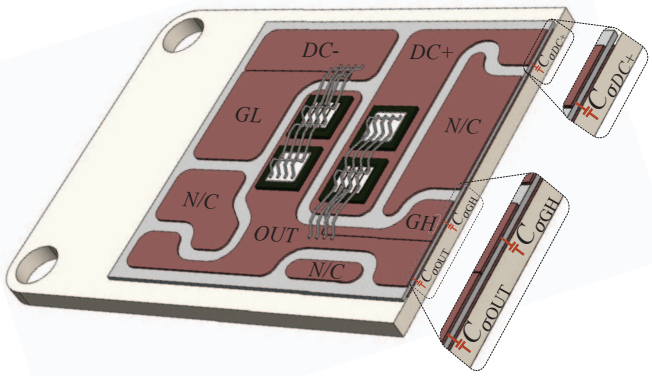

Fig. 2: Power module layout illustrating the DBC islands, the layering of the DBC and the baseplate including a cross-sectional view of the layering illustrating the OUT, DC+ and gate-high parasitic capacitive couplings to the baseplate.

B. Half-bridge Power Module Modelling

In a typical half-bridge power module the isolating ceramic substrate of the Direct Bonded Copper (DBC) results in parasitic capacitive couplings between the baseplate and the top copper islands, as depicted by the cross-sectional view in Fig. 2. The circuit representation of the power module capacitive couplings is given in Fig. 1b. The baseplate is assumed grounded, as is the case in most practical setups.

The capacitances $C_{\sigma DC+}$, $C_{\sigma DC-}$ and $C_{\sigma GL}$ are referred between two approximately constant potentials during switching transition and can thus be analyzed as being fully charged yielding an open-circuit connection in a DC analysis. In

contrast the capacitances $C_{\sigma\text{GH}}$ and $C_{\sigma\text{OUT}}$ will be subject to a high dv/dt during switching transitions as the potential of the half-bridge output terminal is changing between DC- and DC+ during each switching commutation [28].

C. Miller Capacitance Modelling

As the majority of the power module parasitic capacitive couplings are referred between constant potentials, the model in Fig. 1a is simplified and combined with the MOSFET model from Fig. 1b yielding the equivalent MOSFET and power module parasitic capacitive couplings of the half-bridge, as illustrated in Fig. 1c. From the model in Fig. 1c a difference can be observed in capacitive couplings between the gate-high and gate-low terminals due to the inclusion of the gate-high power module capacitance $C_{\sigma\text{GH}}$ on the high-side MOSFET. The gate voltage V_{GH} to ground will govern the capacitive displacement current of the gate-high capacitance $C_{\sigma\text{GH}}$. As for the high-side MOSFET gate-drain capacitance C_{GDH} the voltage governing the capacitive displacement current will be the gate-drain voltage v_{GDH}. From Kirchoff's voltage law in (2) and (3) are derived under the assumption that the gate-source voltage bias is negligible. The respective voltages in (2) and (3) are defined in Fig. 1c, which likewise depicts the polarity conventions used for the derivation.

$$v_{\text{GH}} = V_{\text{GSH}} - v_{\text{DSH}} + V_{\text{DC}}^{+} \approx -v_{\text{DSH}} + V_{\text{DC}}^{+} \tag{2}$$

$$v_{\text{GDH}} = v_{\text{GH}} - v_{\text{DH}} = -v_{\text{DSH}} + V_{\text{DC}}^{+} - V_{\text{DC}}^{+} = -v_{\text{DSH}} \tag{3}$$

The difference in subjected voltage in (2) and (3) is the DC+ bias on the voltage of the gate-high capacitance. With V_{DC}^{+} being a constant voltage, the dv/dt of the drain-source voltage v_{DSH} will be governing the capacitive displacement currents of both of the capacitances $C_{\sigma\text{GH}}$ and C_{GDH}, thus allowing to consider these as being in parallel. Effectively this will impact the Miller region of the high-side MOSFET Q_{H} compared to the low-side MOSFET Q_{L}, which is why the "equivalent" Miller capacitance $C_{\text{eqmil,H}}$ of the high-side is defined a combination of the gate-high capacitance and the gate-drain capacitances, whereas the low-side Miller capacitance will only be C_{GD}, as shown in (4), under the assumption that $C_{\text{GDH}} = C_{\text{GDL}} = C_{\text{GD}}$.

$$C_{\text{eqmil,H}} = C_{\sigma\text{GH}} + C_{\text{GD}} \;>\; C_{\text{eqmil,L}} = C_{\text{GD}} \tag{4}$$

$$\left.\begin{aligned} i_{\text{G}} &= C_{\text{eqmil,H}} \cdot \tfrac{\Delta v_{\text{DSH}}}{\Delta t_{\text{mil,H}}} \\ i_{\text{G}} &= C_{\text{eqmil,L}} \cdot \tfrac{\Delta v_{\text{DSL}}}{\Delta t_{\text{mil,L}}} \end{aligned}\right\} \;\Delta t_{\text{mil,H}} \;>\; \Delta t_{\text{mil,L}} \tag{5}$$

As was explained previously in (1), the charging current of the Miller capacitance during the Miller region is limited by the gate resistor, thus with a fixed gate current amplitude and a fixed DC voltage yielding a fixed change in drain-source voltage ($V_{\text{DC}} = \Delta V_{\text{DS}}$), the increase in equivalent Miller capacitance will directly impact the Δt_{mil} (duration of the Miller region) and thus the slope of the drain-source voltage, which is given in (5). This will cause an imbalance in the switching dynamics of the two MOSFETs with the high-side MOSFET Q_{H} turning on slower than Q_{L} and thus incurring additional losses on the high-side device which can impact life-time and reliability of the half-bridge power module.

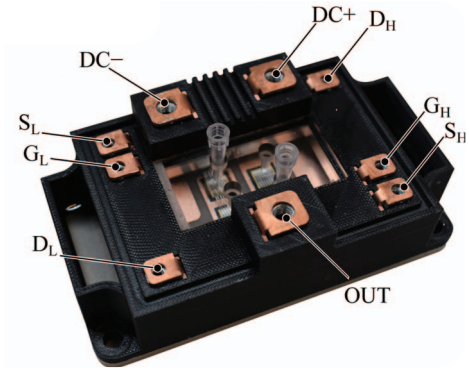

Fig. 3: Case study, SiC MOSFET power module populated with 3rd generation Wolfspeed 10 kV / 17 A dies [25].

To validate the analytically derived analysis of the gate-high capacitance $C_{\sigma\text{GH}}$ impact on the Miller region charging dynamics, the following section presents the simulation study for these charging dynamics using a digital twin model of a laboratory DPT setup.

III. Digital Twin Simulations

For the the simulations of this paper the 10 kV SiC MOSFET power module shown in Fig. 3 will be used as a case study. In [32] a digital twin simulation model of power module from Fig. 3 has been constructed from a combined physics based power module model and a behavioural based MOSFET and diode model. The digital twin SPICE simulation model was validated through comparison between experimental and simulated Double Pulse Test (DPT) utilizing the low-side device of the half-bridge 10 kV SiC MOSFET power module. Further details of the experimental setup, testing procedures and loss analysis are found in [32]. In this paper, the validated SPICE model is utilized to highlight the impact of the gate-high capacitance on the Miller region charging dynamics. In addition, a high-side DPT simulation model is further developed, as illustrated from the schematic in Fig. 4, with both models having a split DC-midpoint. Simulation parameters are given in Table I. The piece-wise-linear models of the MOSFET intrinsic capacitances $C_{\text{ISS}}, C_{\text{OSS}}, C_{\text{RSS}}$ and the external JBS diode intrinsic capacitance C_{T} are depicted by the dashed lines in Fig. 5. Where the capacitance conversion from the capacitances in Fig. 5 to the switching device intrinsic capacitances defined in Table I and Fig. 4 are given as; $C_{\text{DS}} = C_{\text{OSS}} - C_{\text{RSS}} + C_{\text{T}}$, $C_{\text{GS}} = C_{\text{ISS}} - C_{\text{RSS}}$ and $C_{\text{GD}} = C_{\text{RSS}}$.

A. Switching Loss Imbalance

The impact of the gate-high capacitance on the switching dynamics of the high-side device, compared to the low-side device will be illustrated from simulations in this section.

The 2nd turn-on switching waveforms for the two DPT's are shown in Fig. 6 and depicts how the gate-high capacitance $C_{\sigma\text{GH}}$ extends the Miller region of the high-side MOSFET turn-on, compared to the low-side MOSFET turn-on. This

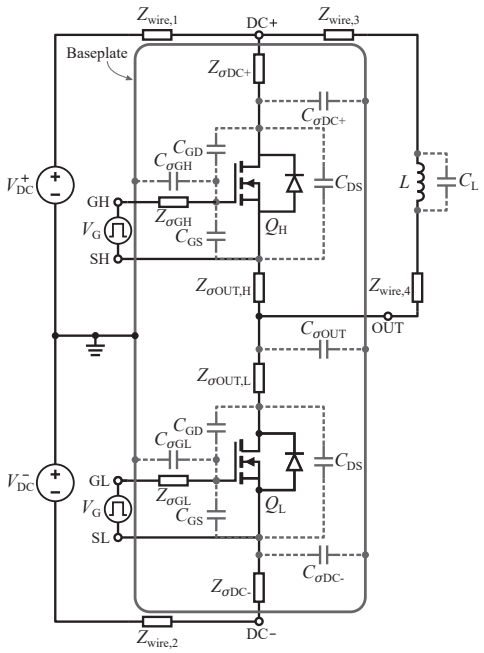

Fig. 4: Circuit schematic illustrating parasitic impedances included in the digital twin model of the DPT setup.

TABLE I: Double pulse test setup simulation parameters.

Load & source parameters			
V_{DC}	±3 kV	C_{DC}	100 µF
V_G^+	20 V	$R_{G,ext}$	20.2 Ω
V_G^-	−5 V	$R_{G,int}$	2.8 Ω
L	49 mH	R_L	6.08 Ω
Parasitic capacitances			
C_{GS}	piece-wise-linear	C_{GD}	piece-wise-linear
C_{DS}	piece-wise-linear		
$C_{\sigma DC+}$	68.1 pF	$C_{\sigma DC-}$	33.91 pF
$C_{\sigma GH}$	12.85 pF	$C_{\sigma GL}$	35.6 pF
$C_{\sigma OUT}$	83.1 pF	C_L	12 pF
Parasitic inductances		**Series resistances**	
$L_{\sigma DC+}$	17.9 nH	R_{DC+}	21.1 mΩ
$L_{\sigma DC-}$	17.9 nH	$R_{\sigma DC-}$	22.6 mΩ
$L_{\sigma GH}$	17.0 nH	$R_{\sigma GH}$	121.5 mΩ
$L_{\sigma GL}$	16.3 nH	$R_{\sigma GL}$	100.7 mΩ
$L_{\sigma OUT,H}$	18.5 nH	$R_{\sigma OUT,H}$	34.7 mΩ
$L_{\sigma OUT,L}$	16.5 nH	$R_{\sigma OUT,L}$	28.2 mΩ
$L_{wire,1}$	50.0 nH	$R_{wire,1}$	12.8 mΩ
$L_{wire,2}$	49.0 nH	$R_{wire,2}$	12.8 mΩ
$L_{wire,3}$	560 nH	$R_{wire,3}$	35.2 mΩ
$L_{wire,4}$	720 nH	$R_{wire,4}$	39.0 mΩ

is clearly shown from a comparison between the switching energy dissipation of the high-side and low-side device, yielding an increase of 27.1 mJ for the high-side MOSFET corresponding to a percentage increase of 76 % in switching energy dissipation for this specific switching event.

B. Gate-High Capacitance Sensitivity Analysis

The gate-high capacitance $C_{\sigma GH}$ will be varied in the simulations with steps of ±5 pF from the original value of 12.85 pF, thus the swept range will be from 2.85 pF-22.85 pF, with the addition of a 0 pF simulation used as a reference. The

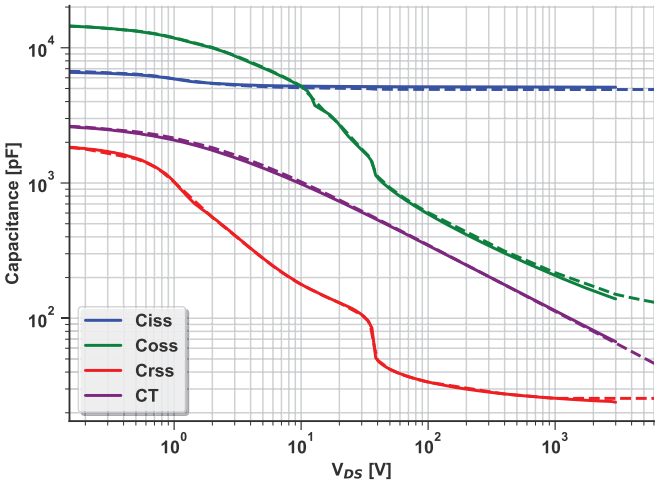

Fig. 5: MOSFET and diode intrinsic capacitances [32].

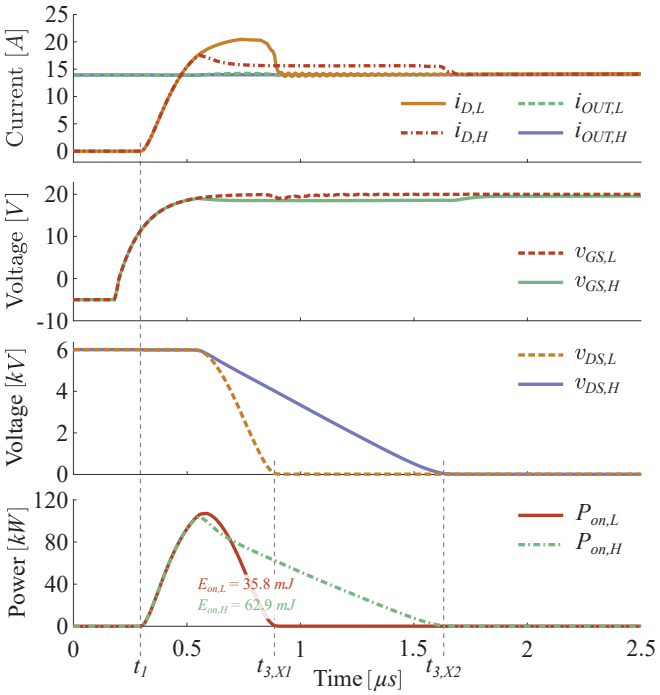

Fig. 6: Simulated turn-on switching waveforms for low-side and high-side DPT's at a load current level of 14 A.

gate-drain capacitance C_{GD} and gate-low capacitance $C_{\sigma GL}$ will be kept as defined in Table I.

The turn-on switching waveforms from the simulated high-side DPT's with varied equivalent high-side Miller capacitances are shown in Fig. 7. The extracted turn-on switching energy losses for both high-side and low-side DPT's are summarized in Table II. From the summarized simulation data in Table II it is observed that the width of the Miller region and the high-side turn-on losses are highly affected for the DPT of the high-side device when varying the high-side gate capacitance, whereas for the DPT of the low-side device the width of the Miller region and the turn-on losses

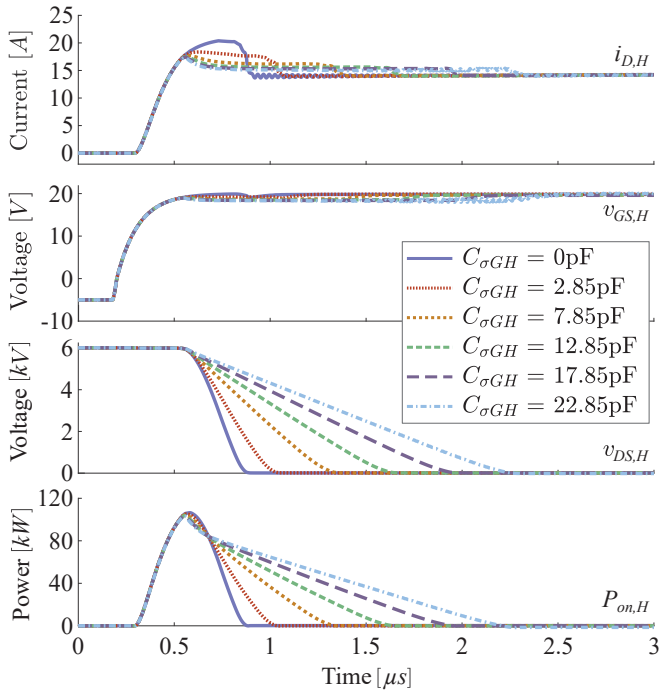

Fig. 7: Simulated turn-on switching waveforms for high-side DPT's at 6 kV / 14 A, with varied gate-high capacitance $C_{\sigma\text{GH}}$.

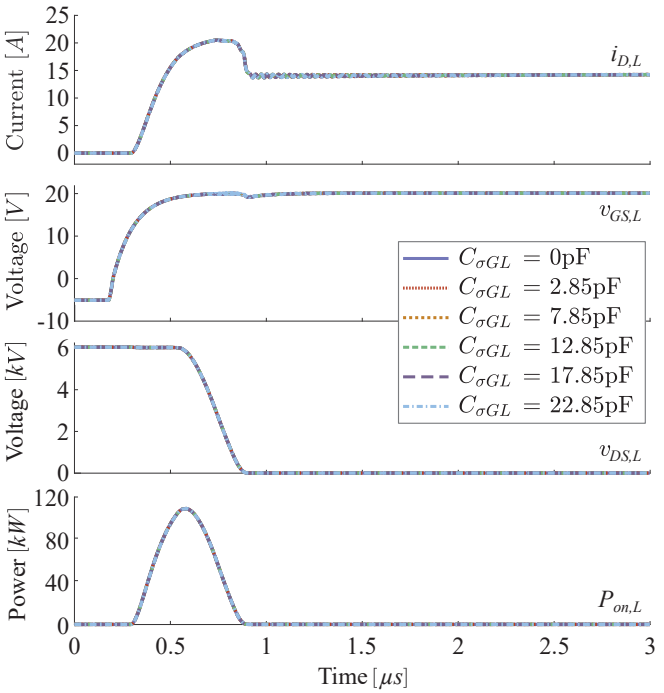

Fig. 8: Simulated turn-on switching waveforms for low-side DPT's at 6 kV / 14 A, with varied gate-low capacitance $C_{\sigma\text{GL}}$.

TABLE II: Summarized simulated turn-on losses for high-side and low-side DPT's with varied gate-high capacitances.

$C_{\sigma GH}$	0	2.85	7.85	12.85	17.85	22.85	[pF]
$E_{on,L}$	34.9	35.1	37.5	35.6	38.2	38.5	[mJ]
$E_{on,H}$	34.9	39.9	51.3	62.9	75.8	88.4	[mJ]
$\Delta t_{mil,L}$	0.333	0.349	0.383	0.357	0.393	0.398	[μs]
$\Delta t_{mil,H}$	0.333	0.490	0.798	1.096	1.416	1.716	[μs]

are nearly not affected by this varying of the high-side gate capacitance. It is shown that an increase of 5 pF in high-side gate capacitance corresponds to an increase in high-side turn-on energy losses of approximately 10 mJ and an increase in duration of the Miller region of approximately 300 ns, for this specific case study and within the defined sweeping range of high-side gate capacitance. This implies a linear relationship between increase in equivalent Miller capacitance and the surplus switching losses incurred. This trend agrees with the analytically derived theory in (5), which states that for the same ΔV_{DS} and under the assumption of a constant gate current, the duration of the Miller region will be linearly proportional to the equivalent Miller capacitance. Assuming that the Miller region losses can be considered as the main contributor to the turn-on switching losses, this linear proportionality between equivalent Miller capacitance and duration of the Miller region, will cause a similar linear proportionality between increase in equivalent Miller capacitance and increase in turn-on switching losses. In addition, it should be highlighted how the 0 pF high-side gate capacitance in Table II depicts a fully balanced half-bridge, where the low-side Miller capacitance is equal to the equivalent high-side Miller capacitance, and thus achieving identical switching dynamics and corresponding switching losses.

C. Gate-Low Capacitance Sensitivity Analysis

To further clarify the difference in sensitivity between gate-high and gate-low parasitic capacitances, the gate-low capacitance $C_{\sigma\text{GL}}$ will be varied in the simulations. The swept range for the gate-low capacitance will be identical to the previous section with steps of ±5 pF from 12.85 pF, yielding 2.85 pF-22.85 pF and a 0 pF simulation as a reference. The gate-drain capacitance C_{GD} and gate-high capacitance $C_{\sigma\text{GH}}$ will be kept as defined in Table I. The turn-on switching waveforms from the simulated low-side DPT's with varied low-side parasitic gate capacitance are shown in Fig. 8. The identical waveforms for the sweep in gate-low capacitance verifies that the gate-low capacitance will not impact the duration of the low-side device Miller region. As was similarly explained in Section II this is due to the parasitic gate-low capacitance being referred to the constant DC- potential, and thus not experiencing the high dv/dt from the switching transition, whereas the parasitic gate-high capacitance is referred to the OUT potential and thus experiences the full dv/dt during switching transition.

The turn-on switching energy dissipation during these low-side DPT simulations are extracted to be between 35.7 and 35.8 mJ, which is similar to the low-side DPT turn-on energy of 35.6 mJ documented in Table II for $C_{\sigma\text{GH}}$ =12.85 pF, as the gate-high capacitance in the simulations in Fig. 8 are kept constant at exactly 12.85 pF. The minor deviations are caused by the computational variations in the numerical integration of the Power waveforms.

IV. Perspectives

The derived model of this paper is generally valid for both Si IGBT and SiC MOSFET based half-bridge configured power modules. However, to the knowledge of the authors the phenomenon of increased equivalent Miller capacitance on the high-side device has not been documented in literature, despite the large impact on the medium voltage power module switching performance demonstrated here. Possible reasons are shared from the authors perspectives:

1) As the active surface area of an Si IGBT die is larger compared to the active area of the SiC MOSFET die the physical size of the gate-drain/collector capacitance is larger for the Si IGBTs. Thus, the relative increase in high-side equivalent Miller capacitance compared to the low-side Miller capacitance for IGBTs is small and thus prevalent research has not been concerned with the discussed phenomenon.

2) The state-of-the-art literature on power device loss characterization are heavily populated by behavioural based Si IGBT loss models with the existing SiC MOSFET loss models being derived from the behavioural based Si IGBT loss models. Thus, as existing loss models are behavioural based black-box models, the physics based phenomenon defined in this paper has not been identified.

3) Double pulse testing is a widely recognised method for determining semiconductor switching energy. Historically DPT has been performed on the low-side device, due to the the exclusion of high-side driver isolation requirements and the convenience of accessibility to the DC- terminal for passive probing. Thus, without characterizing the high-side energy the imbalance observed in this paper has not identified.

4) The increase in operating voltage capabilities of the WBG devices (ΔV_{DS}) have caused in increase in the Miller region switching energy contribution to the overall switching energy dissipation of the SiC power module, which is why the impact of the gate-high capacitance is magnified at higher bus voltages.

V. Conclusion

This paper highlights a difference in equivalent Miller capacitance between high-side and low-side SiC MOSFET in a half-bridge power module, which during the turn-on Miller region charging dynamics causes an increase in the high-side switching energy dissipation. An equivalent circuit representation including MOSFET and half-bridge power module parasitic capacitive couplings is given. The equivalent circuit is used to derive how the gate-high capacitance $C_{\sigma\mathrm{GH}}$ will effectively be coupled in parallel to the gate-drain capacitance C_{GD}, thus increasing the equivalent high-side Miller capacitance compared to the low side Miller capacitance. From analytical derivation of the SiC MOSFET turn-on it is shown how the increase in equivalent high-side Miller capacitance extends the Miller region for the high-side MOSFET, thus incurring additional switching energy dissipation, entailing an imbalance in the half-bridge switching energy distribution between high-side and low-side device. From combined physics based and behavioural based digital twin simulations it is verified how the influence of the equivalent high-side Miller capacitance drastically increases the high-side device switching energy dissipation compared to the low side device. A turn-on energy deviation of $27.1\,\mathrm{mJ}$ corresponding to $76\,\%$ increase of the high-side switching energy dissipation is shown in a simulated DPT configuration for a specific MV SiC-based MOSFET power module. A sensitivity analysis with varying parasitic high-side gate capacitance shows an approximately linear increase in high-side turn-on losses with the increase in equivalent high-side Miller capacitance. These results highlights the importance of considering the power module parasitic gate-high capacitance in the design and loss estimation of MV SiC-based power modules, as this otherwise could negatively impact efficiency, performance estimates and reliability of the designed power module. Due to the significance of the simulated results shown in this paper, the increases equivalent Miller capacitance phenomenon should be experimentally validated for WBG enabled MV half-bridge power modules in future research.

Acknowledgments

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