Aalborg Universitet

AALBORG UNIVERSITY
DENMARK

Thyristor-Pair-and Damping-Submodule-Based Protection Against Valve-Side Single-Phase-to-Ground Faults in MMC-MTDC Systems

Liu, Xiaoxiao; Li, Gen; Zheng, Tao; Yang, Xinhui; Guerrero, Josep M.

Published in:
IEEE Transactions on Power Delivery

DOI (link to publication from Publisher):
10.1109/TPWRD.2021.3125661

Publication date:
2022

Document Version
Accepted author manuscript, peer reviewed version

Link to publication from Aalborg University

Citation for published version (APA):
Liu, X., Li, G., Zheng, T., Yang, X., & Guerrero, J. M. (2022). Thyristor-Pair-and Damping-Submodule-Based Protection Against Valve-Side Single-Phase-to-Ground Faults in MMC-MTDC Systems. *IEEE Transactions on Power Delivery*, *37*(4), 3257-3269. https://doi.org/10.1109/TPWRD.2021.3125661

General rights
Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal -

Take down policy
If you believe that this document breaches copyright please contact us at vbn@aub.aau.dk providing details, and we will remove access to the work immediately and investigate your claim.

Thyristor-Pair- and Damping-Submodule-Based Protection against Valve-Side Single-Phase-to-Ground Faults in MMC-MTDC Systems

Xiaoxiao Liu, *Student Member, IEEE*, Gen Li, *Member, IEEE*, Tao Zheng, *Member, IEEE*, Xinhui Yang, Josep M. Guerrero, *Fellow, IEEE*

***Abstract*—The single-phase-to-ground (SPG) fault at the valve side of the converter transformer is one of the most critical faults threatening the operation of bipolar half-bridge modular-multilevel-converter-based multi-terminal direct-current (HB-MMC MTDC) systems. Following a valve-side SPG fault, the upper-arm submodule (SM) capacitors in the faulty converter may suffer a serious overvoltage, and the grid-side fault currents may experience no zero-crossings. The existing protection methods generally rely on tripping the grid-side alternate-current circuit-breaker (ACCB), which cannot fully isolate the fault. The healthy poles and stations may encounter severe disturbance and be all blocked, which will lead to a power outage of the entire MTDC system. This paper proposes an ACCB-independent scheme based on thyristor-pairs and damping SMs to address these problems. Antiparallel thyristor-pairs are connected in series within the upper and lower arms in each phase. Serial damping SMs are connected within the lower arms to help the lower-arm thyristor pairs cut off the fault currents. Although the proposed additional devices inevitably cause conduction losses, they can effectively protect the faulty converter and healthy circuit in the MTDC system. Simulations in PSCAD/EMTDC have been conducted to verify the effectiveness of the proposed strategy.**

***Index Terms*—Single-phase-to-ground fault, multi-terminal direct-current, modular multilevel converter, thyristor-pair, converter protection.**

I. Introduction

MODULAR multilevel converter (MMC) based high-voltage direct-current (HVDC) technology has been an attractive alternative of line commutated converter (LCC) based HVDC due to its modularity, scalability, superior harmonic performance, and no risk of commutation failure, etc. [1]-[3]. Among variable MMC topologies, the half-bridge submodule (SM) based MMC (HB-MMC) has been primarily deployed in recent multi-terminal HVDC (MTDC) projects owing to their lower power losses and fewer capital costs compared with other MMCs with different topologies [4]. Examples include Zhangbei ±500 kV four-terminal HVDC grid [5]. However, MMC-MTDC systems still face some challenges, including the coordinated control of converters, DC grid protection, and regulation and standardization issues [6].

The fault-tolerant operation capability of HB-MMC MTDC is one of the most significant technical challenges. Research efforts have been made on the DC fault analysis and protection in MMC-MTDC systems [7]-[8]. The clearance of DC faults in an HB-MMC MTDC system can be achieved using alternate-current (AC) or DC circuit breakers (CB) [9]-[10]. However, converter station internal AC faults have drawn less attention compared with DC faults, although they may cause more severe consequences. The single-phase-to-ground (SPG) fault at the converter valve side is one typical station internal AC fault, usually permanent and caused by transformer wall bushing insulation failure.

Although the probability of the SPG fault is low, it may bring severe damages to the equipment and system [11]-[21]. In LCC-HVDC systems, the SPG fault on the inverter side may lead to commutation failure [12]-[13]. In MMC HVDC systems, the converter will be blocked immediately to protect the vulnerable IGBTs once the SPG fault is detected. However, the fault currents can still flow through the arms due to the freewheeling diodes in SMs. For example, the post-fault currents in HB-MMC HVDC systems will flow through the upper-arm SMs to charge the upper-arm SM capacitors, which may cause severe SM overvoltage [17]-[20]. Meanwhile, there will also be fault current through HB-MMC's lower arms. In this case, large DC offsets may be generated in lower-arm and valve-side fault currents due to the continuous unidirectional conduction of the freewheeling diodes in lower-arm SMs, which may cause grid-side non-zero-crossing fault currents. The most challenging difficulty is that the grid-side ACCBs may fail to interrupt such non-zero-crossing currents [17], [18]. Therefore, the valve-side SPG fault should be addressed by proposing proper protection schemes.

Protection methods have been proposed in the existing literature to address the above problems [14]-[20], [22]. In [14],

This work was supported by the Joint Funds of the National Natural Science Foundation of China (Grant No. U216620017), and VILLUM FONDEN under the VILLUM Investigator Grant (no. 25920): Center for Research on Microgrids (CROM); www.crom.et.aau.dk. (*Corresponding author: Tao Zheng, Gen Li*).

X. Liu, T. Zheng, and X. Yang are with the School of Electric and Electronic Engineering, North China Electric Power University, Beijing, 102206, China (Emails: m18811315622@163.com, zhengtao_sf@126.com, 18811658508@163. com).

G. Li is with the School of Engineering, Cardiff University, Cardiff, CF24 3AA, U.K. (Email: LiG9@cardiff.ac.uk).

J. M. Guerrero is with the Villum Center for Research on Microgrids (CROM), AAU Energy, Aalborg University, 9220 Aalborg East, Denmark (Tel: +45 2037 8262; Fax: +45 9815 1411; e-mail: joz@energy.aau.dk)

an auxiliary grounding ACCB with a resistor is installed on the grid-side of the converter transformer to generate zero-crossings in the grid-side currents through creating a grid-side three-phase-to-ground fault. However, the created three-phase-to-ground fault may cause severe disturbance on the AC grid. In [17], one mixed-SM based method is proposed, which uses HB-SMs in the upper arms and FB-SMs in the lower arms. Although this topology can eliminate the issue of grid-side non-zero-crossing currents, the SM capacitors in the upper arms will still suffer severe overvoltage. An *LR* circuit as the DC grounding of the HB-MMC is proposed in [18] to create grid-side zero-crossing current. However, the application of the *LR* circuit in the bipolar HB-MMC HVDC may worsen the overvoltage in the upper-arm SM capacitors and cause great disturbance on the healthy pole. A method of creating a three-phase fault at the valve side using the lower-arm fast bypass switches has been proposed in [15]. Zero-crossings will appear in the grid-side currents due to the created valve-side three-phase symmetrical fault. Then, the grid-side ACCBs will be able to interrupt the grid-side currents. However, in this scheme, the IGBTs face a high risk of overcurrent during the action of the auxiliary arm switches [15]. Another similar scheme uses inversely paralleled thyristor-pairs in the lower-arm SMs to create three-phase symmetrical fault currents, which can be interrupted by the ACCB [16]. Moreover, this scheme can also clamp the overvoltage in upper-arm SMs.

However, the fault isolation in the abovementioned solutions still relies on the tripping of the grid-side ACCB, in which the slow operation of ACCBs may affect the effectiveness of the protection. It is well-known that ACCB may take approximately 100 ms to complete the mechanical opening process [23]-[24]. Even with modern fast ACCB, it may take 2-3 line frequency cycles. During the opening process of ACCB, large fault currents with DC offsets will be generated and flow through the converter lower arms and transformer, which may result in severe damages to the semiconductor devices and the transformer. Besides, the opening of ACCB cannot fully clear the fault, so that the healthy poles and stations may encounter severe disturbance and be all blocked. Therefore, an ACCB-independent scheme that can completely isolate the faulty station from the heathy system should be proposed.

In practical engineering projects, converter-embedded devices, such as SMs with damping resistors installed within HB-MMC arms are used to protect converters from DC faults (e.g. the Zhoushan ±200 kV five-terminal HVDC grid) [25]-[27]. Moreover, several novel MMC topologies that integrate DCCB functions have also been proposed [28]-[30]. In [28], a thyristor-pair branch is installed within HB-SMs to achieve DC fault self-clearing. However, the application of the damping SMs and thyristor-pairs to address station internal SPG faults in HB-MMC MTDC has not attracted wide attention.

The contributions of this paper include:

1) An ACCB-independent scheme based on thyristor-pairs and damping SMs is proposed to address the valve-side SPG faults. Antiparallel thyristor-pairs are connected in series within the upper and lower arms in each phase. Damping SMs are connected in series within the lower arms to accelerate the damping of the lower-arm currents and help the thyristor-pairs turn-off.

2) The proposed scheme can quickly cut off the fault currents and isolate the fault without relying on the grid-side ACCB. Thanks to this fast fault isolation, the upper arm overvoltage can be effectively alleviated.

3) The proposed scheme can greatly mitigate the impact after a valve-side SPG fault on the operation of the healthy stations in the MTDC grid.

The rest of this paper is structured as follows. The characteristics of upper- and lower-arm post-fault currents are analyzed in Section II. The proposed protection method is analyzed in Section III. Then simulation results in PSCAD/EMTDC verify the feasibility of the proposed scheme in Section IV. Finally, Section V concludes the paper. It should also be highlighted that although the proposed thyristor pairs and damping SMs can also be used for DC fault protection, the parameter design of this scheme for DC protection falls out of the scope of this work.

II. Analysis of Valve-Side Single-Phase-to-Ground Faults

In this paper, the analysis is carried out for the positive pole of one station in a bipolar MTDC system. The conclusions can be applied to the negative pole due to the symmetry of the two poles. This section mainly analyzes the characteristics of upper- and lower-arm currents of the faulty converter.

A. Converter Topology

Fig. 1 depicts a typical converter in the positive pole of a bipolar HB-MMC MTDC grid. As shown in Fig. 1(a), each phase of the converter consists of the upper and lower arms. The single-phase arm topology is shown in Fig. 1(b). V_{dc} is the positive-pole DC voltage. u_{x_upper}, u_{x_lower}, i_{x_upper}, and i_{x_lower} (x = a, b, c) are the equivalent SM voltages and currents in upper and lower arms. u_x and i_x are the valve-side voltages and currents. i_{x_circ} is the circulating current. R and L are the arm resistor and inductor.

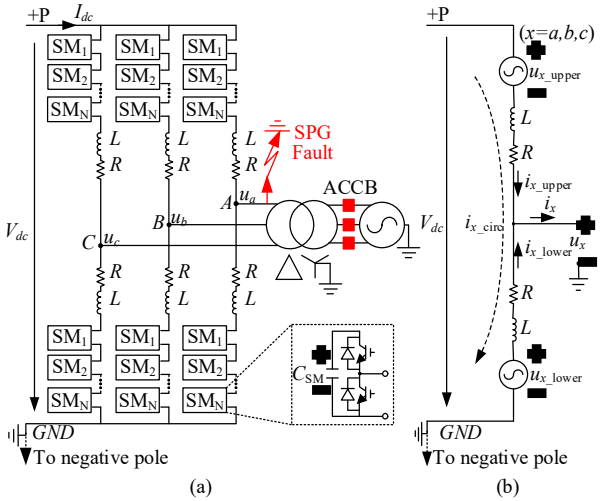


Fig. 1. A typical converter topology in the positive pole of a bipolar HB-MMC MTDC grid. (a) Converter topology. (b) Equivalent circuit of single-phase arm.

The valve-side SPG fault is assumed to occur in Phase *A,* as

shown in Fig. 1(a). Due to the symmetry among the three phases, the faults on the other phases are similar to the fault in Phase *A*. After the occurrence of the fault, fault current loops may be formed through the DC grounding, arms, valve-side windings of the converter transformer, and the fault point. Due to the small loop impedance, the fault current will increase dramatically. To protect the vulnerable IGBTs, the converter overcurrent protection will be activated immediately to block the converter. However, fault currents can still flow through the freewheeling diodes in the SMs. Consequently, the upper-arm SM capacitors may suffer overvoltage, and lower arms may experience large fault currents with DC offsets, which have been analyzed in [15]-[17]. The following analysis mainly focuses on the arm current characteristics after the valve-side SPG fault to discuss the conditions of cutting off these currents. By quickly cutting off the arm currents within the MMC, the SPG fault will be isolated without using the grid-side ACCB.

B. Analysis of Upper-Arm Currents

The fault current paths in the upper arms are depicted in Fig. 2. C_{equ} is the equivalent capacitance of all SM capacitors in each arm. During steady-state operation, the total voltage on all SM capacitors in each arm is V_{dc}. The root-mean-square (RMS) value of valve-side AC line voltage can be expressed as:

$$U_n = \frac{\mu m}{\sqrt{2}} V_{dc} \quad (\mu = 0.866,\ 0 < m \le 1), \tag{1}$$

where μ is the maximum DC voltage utilization rate. It can be seen from (1) that the AC line voltage is lower than V_{dc}.

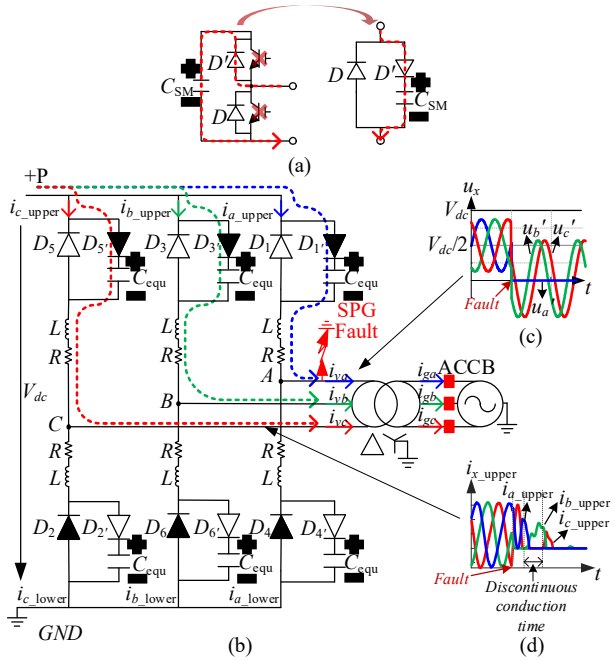


Fig. 2. Equivalent circuits after blocking the converter shown in Fig. 1. (a) Charging current paths in an upper-arm SM. (b) Upper-arm fault current paths. (c) Valve-side voltages. (d) Upper-arm currents.

When the SPG fault occurs, the faulty-phase valve-side voltage u_a will reduce to zero. Because of the delta connection of the valve-side windings in the converter transformer, the post-fault valve-side phase voltages of the healthy phases, u_b' and u_c', will change to the pre-fault line voltages, u_{ba} and u_{ca}, as illustrated in Fig. 2(c). Assuming that the DC voltage and the SM capacitor voltage are unchanged at the moment of the fault occurrence, the voltages across the diodes D_1, D_3, and D_5 will be $-V_{dc}$, $u_{ba}-V_{dc}$, and $u_{ca}-V_{dc}$, which are always negative. And the voltages across the diodes $D_{1'}$, $D_{3'}$, and $D_{5'}$ will be 0, $-u_{ba}$, and $-u_{ca}$. Therefore, diodes D_1, D_3, and D_5 will suffer reverse voltage and will be forced to be turned off. However, $D_{3'}$ and $D_{5'}$ will turn on, and the fault currents will charge the corresponding SM capacitors during every negative half-cycle of the post-fault valve-side voltages. $D_{1'}$ will be turned on if the DC voltage V_{dc} encounters overvoltage during the fault, and therefore, the SM capacitors in the faulty phase will be charged as well. Therefore, the upper arm SM capacitors, especially the ones in the non-faulty arms, will suffer overvoltage, which should be addressed as soon as possible.

The charging current loop, as the dotted lines show in Fig. 2(b), is formed by the DC transmission line, antiparallel diodes ($D_{1'}$, $D_{3'}$, and $D_{5'}$), arm resistors and inductors, and the fault grounding. In the first cycle after the fault, if the arm resistor and the DC voltage change during this short time are ignored, the differential equation of the charging current loops during the SM capacitors charging processes in the healthy-phase upper arms can be expressed by:

$$\begin{cases} V_{dc} = LC_{\text{equ}} \dfrac{d^2 u_{x\_\text{upper}}}{dt^2} + u_{x\_\text{upper}} + u_x' \\ u_x' = \sqrt{2} U_n \sin(\omega t + \theta_x') \end{cases} (x = b, c), \tag{2}$$

where u_x' and θ_x' are post-fault voltage and phase angle of the healthy phases, V_{dc} is the DC voltage when the fault occurs. The initial conditions of the charging process can be expressed as:

$$\begin{cases} u_{x\_\text{upper}}(0+) = u_{x\_\text{upper}}(0-) = V_{dc} \\ i_{x\_\text{upper}}(0+) = i_{x\_\text{upper}}(0-) = 0 \end{cases}, \tag{3}$$

where $i_{x\_\text{upper}} = C_{\text{equ}} \mathrm{d}u_{x\_\text{upper}}/\mathrm{d}t$.

According to (2) and (3), the SM capacitor voltage and upper arm currents can be written as:

$$u_{x\_\text{upper}}(t) = \begin{cases} V_{dc} + \dfrac{\sqrt{2}U_n}{\omega^2 LC_{\text{equ}} - 1} [\sin(\omega t + \theta_x') - \\ \sin\theta_x' \cos\beta t - \dfrac{\omega \cos\theta_x'}{\beta} \sin\beta t] & ,\ u_x' < 0 \\ V_{dc} & ,\ u_x' \ge 0 \end{cases}, \tag{4}$$

$$i_{x\_\text{upper}}(t) = \begin{cases} \dfrac{\sqrt{2}U_n C_{\text{equ}}}{\omega^2 LC_{\text{equ}} - 1} [\omega\cos(\omega t + \theta_x') + \\ \beta \sin\theta_x' \sin\beta t - \omega\cos\theta_x' \cos\beta t] & ,\ u_x' < 0 \\ 0 & ,\ u_x' \ge 0 \end{cases}, \tag{5}$$

where $\beta = 1/\sqrt{LC_{\text{equ}}}$.

Taking phase *B* as an example, the upper arm capacitors will stop being charged once the antiparallel diode $D_{3'}$ is turned off by the reverse voltage force. Their total voltage will reach a maximum value, given by:

$$u_{b\_\text{upper\_max}} = V_{dc} + \max|u_b'| = V_{dc} + \sqrt{3} \times \sqrt{2} U_n. \tag{6}$$

It can be seen from (6) that the overvoltage in upper-arm capacitors can reach to $1.5V_{dc}$ when ignoring the voltage drop on the arm resistor and inductor. Moreover, the operational

mode of the faulty station and the time delay for protection action will affect the overvoltage level. If the valve-side SPG fault occurs in the power-receiving converter with DC voltage control, the power-sending converter station will transmit power to the faulty station continuously, which will aggravate its upper-arm SM capacitor overvoltage. If the power-sending converter takes Δt to block the IGBTs based on either its local protection or a blocking signal received from the faulty converter through communications, the voltage change ΔV_{dc} of the upper-arm SM capacitors in the faulty converter can be obtained using the following equation:

$$P\Delta t = \frac{3}{2}C_{\text{equ}}(V_{dc}+\Delta V_{dc})^2 - \frac{3}{2}C_{\text{equ}}{V_{dc}}^2 . \tag{7}$$

As $\Delta V_{dc} << V_{dc}$, the second-order terms in (7) can be neglected. Therefore, ΔV_{dc} can be expressed as:

$$\Delta V_{dc} = \frac{P\Delta t}{3C_{\text{equ}}V_{dc}} . \tag{8}$$

Based on (7)-(8), the overvoltage of the upper-arm capacitors can reach higher than $1.5V_{dc}$. The overvoltage is also affected by the energy transmitted from the power-sending converter: that the higher the transmitting power (P) and the longer the time (Δt) it takes to stop transmitting such power are, the higher the voltage increase of the SM capacitors will be [20]. In the MTDC system, the healthy converter stations are expected to keep operating when faults occur on other stations. However, this will exacerbate the upper-arm overvoltage of the faulty converter because the power-sending converter may keep sending power to the faulty power-receiving converter. Therefore, it is necessary to clear the fault and isolate the faulty converter from the healthy circuit as soon as possible.

According to (5), the upper-arm currents will become zero during every positive half-cycle of the valve-side voltages, which can be seen from Fig. 2(d). This long discontinuous conduction time can be used to interrupt the upper-arm fault currents. Antiparallel thyristor-pairs connected in series within the upper arms are proposed in Section III of this paper to achieve fault clearance. After the converter is blocked, the firing pulses of the thyristors will be removed. Then the thyristors will turn off automatically during the discontinuous conduction time of i_{x_upper}.

C. Analysis of Lower-Arm Currents

The current path in a lower-arm SM is shown in Fig. 3(a), and the fault current paths in lower arms are shown in Fig. 3(b). When the fault occurs, the voltages across the diodes $D_{4'}$, $D_{6'}$, and $D_{2'}$ will be $-V_{dc}$, $u_{ba}-V_{dc}$, and $u_{ca}-V_{dc}$, which are always negative. The voltages across the diodes D_4, D_6, and D_2 will be 0, $-u_{ba}$, and $-u_{ca}$. Therefore, $D_{4'}$, $D_{6'}$, and $D_{2'}$ will suffer reverse voltage and will be forced to be turned off. However, D_6 and D_2 will conduct during the negative half-cycles of the valve-side voltages. $D_{4'}$ will not be turned off until the current flowing through it decays to zero. The characteristics of lower-arm currents will be analyzed in the following.

The equivalent voltage loop equation in the healthy phases can be expressed as:

$$\begin{cases} u_x' = L\dfrac{di_{x\_\text{lower}}}{dt} + Ri_{x\_\text{lower}} \quad (x=b,c) , \\ u_x' = \sqrt{2}U_n \sin(\omega t+\theta_x') \end{cases} \tag{9}$$

The initial conditions of (9) can be assumed as:

$$i_{x\_\text{lower}}(0+) = i_{x\_\text{lower}}(0-) = I_{x\_\text{lower}} , \tag{10}$$

where I_{x_lower} is the current when the converter is blocked.

The lower-arm currents can be calculated and expressed as (11) by substituting (10) into (9):

$$\begin{cases} i_{x\_\text{lower}} = C_x e^{-\frac{R}{L}t} + A_x \sin(\omega t+\theta_x') - B_x \cos(\omega t+\theta_x') \\ A_x = \dfrac{\sqrt{2}RU_n}{R^2+(\omega L)^2} \\ B_x = \dfrac{\sqrt{2}\omega LU_n}{R^2+(\omega L)^2} \\ C_x = I_{x\_\text{lower}} + B_x\cos\theta_x' - A_x\sin\theta_x' \end{cases} , \tag{11}$$

where A_x can be ignored, and B_x approximately equals to $\sqrt{2}U_n/\omega L$ considering R is small. Therefore, (11) can be simplified as:

$$i_{x\_\text{lower}} = (I_{x\_\text{lower}} + \frac{\sqrt{2}U_n}{\omega L}\cos\theta_x')e^{-\frac{R}{L}t} - \frac{\sqrt{2}U_n}{\omega L}\cos(\omega t+\theta_x') . \tag{12}$$

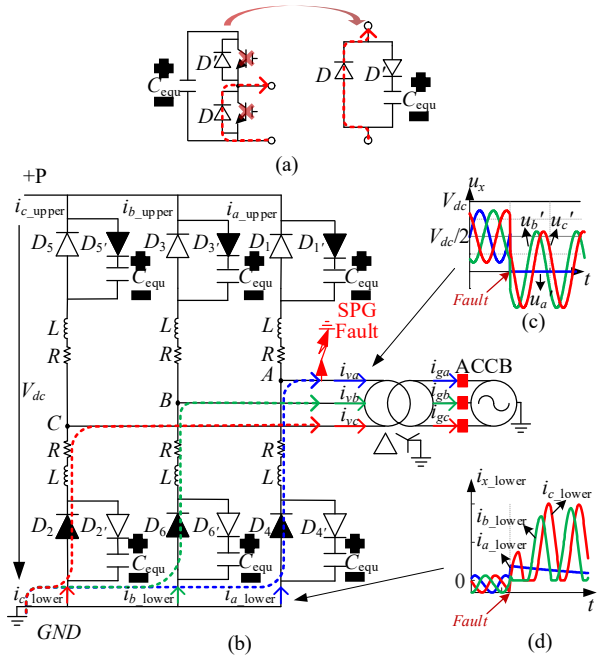


Fig. 3. Equivalent circuits after blocking the converter shown in Fig. 1. (a) Current paths in a lower-arm SM. (b) Lower-arm fault current paths. (c) Valve-side voltages. (d) Lower-arm currents.

Due to the continuous unidirectional characteristic of diodes, the currents in the lower arms will only be the positive item in (12). The maximum DC offsets in the healthy-phase currents will occur when $\theta_x'=0$. Ignoring the decay of the currents, the RMS value of the post-fault lower-arm currents may reach $I_{x\_\text{lower}}+\sqrt{2}U_n/(\omega L)$, which relates to the arm inductance and the values of lower-arm currents and valve-side line voltage at the instant when the converter is blocked. The RMS value can approximately reach 10-20 kA in the Zhangbei project discussed in this paper. The fault currents will continuously

flow through the diodes if the valve-side SPG fault is not cleared. The diodes may have to stand such large currents for more than 2-3 line frequency cycles even after applying the conventional protection methods and fast ACCBs. Therefore, the fault current paths in the lower arms have to be cut quickly as well. The aperiodic component in the lower-arm currents will decay very slowly due to the small resistance in the current loop, resulting in a short discontinuous conduction time of the fault current, as shown in Fig. 3(d). As a result, the thyristor-pairs cannot quickly cut off the lower-arm current paths. Therefore, damping SMs are applied to accelerate the decay of the currents and help the quick turn-off of the thyristor-pairs. The proposed protection scheme will be analyzed in detail in the next section.

D. Impact of Grounding Schemes on the Healthy Stations

DC grid grounding schemes are of vital importance for the operation and control of MMC-MTDC systems. According to the analysis of lower-arm currents, fault currents will flow into the fault point and return to the lower arm through the DC grounding. Therefore, different grounding modes may have impacts on the fault characteristics of healthy stations. For the return path, either ground currents via ground return (GR) or a single point grounded dedicated metallic return (DMR) can be used for bipolar HVDC systems [31]. Fig. 4 shows these two different return paths in a four-terminal MTDC system.

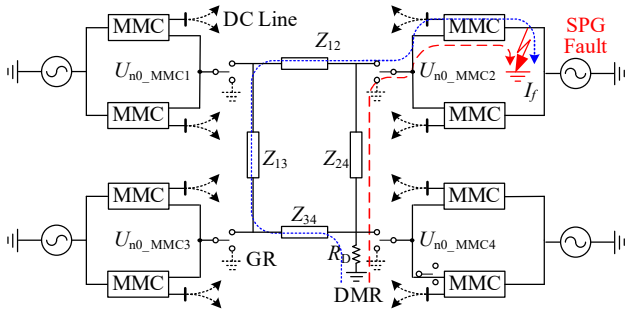


Fig. 4. A four-terminal MTDC system.

It can be seen that the four stations will be independently grounded if GR is utilized. If there is a valve-side SPG fault at the positive pole of MMC2, it will only affect the positive poles of the healthy stations through the charging process of upper-arm SM capacitors in the faulty converter. However, if DMR is utilized, the voltage potential of the DMR circuit will be raised since large fault currents will flow through the common grounding in the DMR circuit, as the dotted line in Fig. 4 shows. If the DMR is utilized, the potential of DC neutral points at each station (U_{n0_MMC1}, U_{n0_MMC2}, U_{n0_MMC3}, and U_{n0_MMC4},) can be expressed as:

$$\begin{cases} U_{n0\_MMC1} = \left(\dfrac{Z_{12}+Z_{13}+Z_{34}}{Z_{\Sigma}} + R_{n0}\right) I_f \\ U_{n0\_MMC2} = \left(\dfrac{Z_{13}+Z_{34}}{Z_{\Sigma}} + R_{n0}\right) I_f \\ U_{n0\_MMC3} = \left(\dfrac{Z_{24}}{Z_{\Sigma}} + R_{n0}\right) I_f \\ U_{n0\_MMC4} = R_{n0} I_f \end{cases}, \quad (13)$$

where I_f is the fault current flowing into the fault grounding. Z_{12}, Z_{13}, Z_{24}, and Z_{34} are the equivalent impedance of each metallic return. Z_{Σ} is the sum of Z_{12}, Z_{13}, Z_{24}, and Z_{34}. R_{n0} is the equivalent resistance of the grounding electrode.

The DC voltages of the healthy stations can be expressed as:

$$\begin{cases} V_{dcP\_MMCm} = V_{dcP} + \Delta V_{dcP} + U_{n0\_MMCm} \\ V_{dcN\_MMCm} = V_{dcN} + U_{n0\_MMCm} \end{cases}, \ (m=1, 2, 3, 4), \quad (14)$$

where V_{dcP_MMCm} and V_{dcN_MMCm} (m=1, 2, 3, and 4) are the rated DC voltage. ΔV_{dcP} is the voltage increase caused by the charging of upper-arm SM capacitors of the faulty station as analyzed in Section II. B. Therefore, the DC voltage of positive poles in healthy stations will experience overvoltage due to the charging process and the voltage increase of the DMR circuit. Meanwhile, the DC voltages of the negative poles will also reflect the potential increase of the DC neutral point.

As a consequence, the valve-side SPG faults have impacts on the healthy stations especially when DMR is utilized. Therefore, fast fault clearance for valve-side SPG faults is requested.

III. Proposed Protection Scheme

Considering the characteristics of the upper- and lower-arm currents, a thyristor-pair- and damping-SM-based SPG fault protection scheme is proposed.

A. Thyristor-Pair- and Damping-SM-Based Protection Scheme

The proposed topology is shown in Fig. 5. The antiparallel thyristor-pairs are installed in the upper and lower arms. The damping SMs are only installed in the lower arms to help the thyristors cut off the fault currents, as shown in Fig. 5(a). During normal operation, the thyristors and IGBTs in the thyristor-pairs and damping SMs are in ON-state. Therefore, the resistors in the damping SMs will be bypassed. These additional devices will not affect the operation and control scheme of the MMC apart from bringing power losses.

The fault clearance process is shown in Fig. 5(b). Once a valve-side SPG fault occurs, the converter overcurrent protection will block the faulty converter. The detection of vale-side SPG faults has been studied in [21]. The criterion of discriminating a valve-side SPG fault can be expressed as:

$$3i_0 = \sum_{x=a}^{c} (i_{x\_upper} + i_{x\_lower}) > \text{threshold}=0.1I_m, (x=a, b, c), \quad (15)$$

where $3i_0$ is the zero-sequence current at the valve-side of the converter transformer and can be calculated using the upper- and lower-arm currents. During normal operation, $3i_0$ equals zero because the three phases are balanced. Once a valve-side SPG fault occurs, the zero-sequence current path will be created, and $3i_0$ will increase instantly. Therefore, $3i_0$ can be used to detect valve-side SPG faults. Moreover, as $3i_0$ is the zero-sequence current at the valve-side of the converter transformer, it ensures the reliable activation of the proposed protection scheme without triggering other AC fault protection set-up. Theoretically, the setting of the threshold should be close to zero. Considering the transforming error of current transformers (CTs) and the precision of devices, some margin should be reserved. Therefore, the threshold is set as $0.1I_m$, in which I_m is the amplitude of valve-side AC phase current in normal operation.

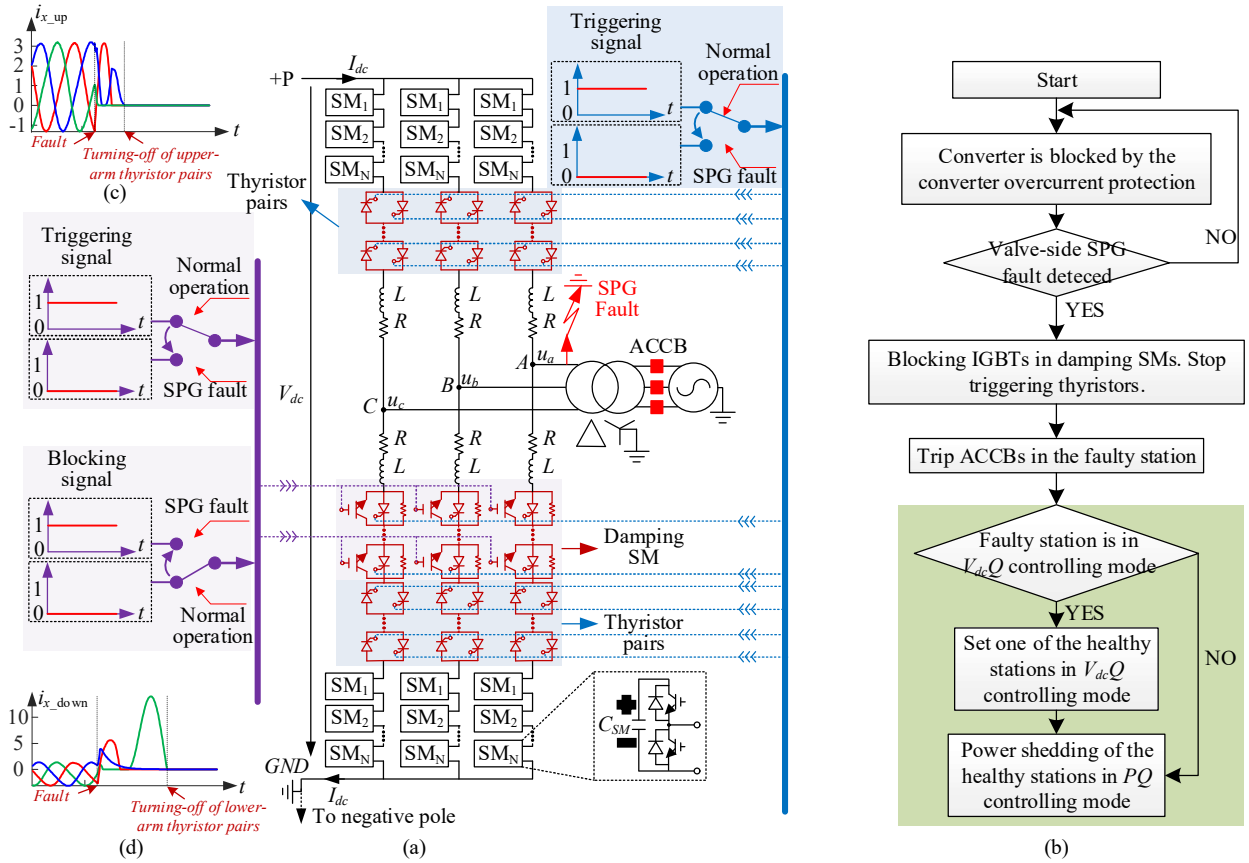


Fig. 5. Proposed protection strategy. (a) Thyristor-pair- and damping-SM-based method. (b) Fault clearance strategy. (c) Upper-arm currents. (d) Lower-arm currents.

Once the valve-side SPG fault is detected, the proposed protection will be triggered. The IGBTs in the damping SMs will be blocked, and the triggering pulses of the thyristors will be removed. The fault current paths in the upper and lower arms will be quickly cut off when the thyristor-pairs are turned off, as the arm currents show in Fig. 5(c) and (d). It should be mentioned that although the proposed protection scheme can protect the converter quickly, as this SPG fault is usually permanent, the grid-side ACCBs also need to be opened to isolate the converter from the AC grid, as shown in Fig. 5(b).

The post-fault control strategy of the healthy stations is also important to ensure the secure operation of the healthy parts in the MTDC system. In the existing research, the healthy converters are suggested to be blocked as soon as possible to limit the overvoltage of the upper-arm SM capacitors in the faulty converter. Otherwise, the non-blocked healthy converter will continue to send power to the faulty converter, which may exacerbate the SM overvoltage [16], [20]. However, in the proposed method, the thyristor-pairs can cut off the charging currents only within one power frequency cycle (20 ms) after the fault. At the same time, the non-blocked healthy converter will not experience severe SM capacitors overvoltage. Therefore, it is unnecessary to block the healthy converters.

To keep the DC bus voltage constant, it is necessary to ensure at least one healthy station is able to keep regulating the DC voltage. For other healthy stations in PQ controlling mode (active and reactive power controlling mode), the references of the active power should be reset and reduced properly to prevent overcurrent caused by overload. The post-fault control strategy is shown in the green shading in Fig. 5(b).

B. Parameter Design

As analyzed in Section II, due to the DC offsets in the lower-arm currents, damping SMs are used to help the thyristor-pairs cut off the fault current. Theoretically, large resistance in the damping SM will accelerate the decay of the fault currents. However, it may also cause overvoltage on the semiconductor devices in the damping SMs. Therefore, a proper design of the resistor in the damping SM is essential.

As analyzed in Section II.C, the most serious condition will occur when $\theta_x'=0$. To simplify the analysis, the lower-arm currents considering the damping SMs can be written as:

$$i_{x\_\text{lower}} = I_{x\_\text{lower}} e^{-\frac{(R+R_D)}{L}t} + \frac{\sqrt{2}U_n}{\omega L}\left[e^{-\frac{(R+R_D)}{L}t} - \cos\omega t\right], \quad (16)$$

where R_D is the equivalent sum resistance of the damping SMs.

It can be seen from (16) that the lower-arm current consists of an aperiodic component with the time constant as $\tau = L/(R+R_D)$ and a periodic component. The decay of the aperiodic component will help the current waveform appear discontinuous conduction. Fig. 6 illustrated the waveforms of (16) when $1/\tau = 0, 1, 2, 5, 10, 20, 50$ (1/s), assuming that I_{x_lower} equals to zero. It can be seen that the discontinuous conduction time of the current is getting longer with the increase of R_D.

According to [32], the turn-off of thyristors generally takes hundreds of microseconds which is approximatively equivalent

to 10° considering a certain margin. Based on Fig. 6, the discontinuous conduction angle will be larger than 10° when $1/\tau > 1$. However, I_{x_lower} is generally larger than zero, and the most severe case is that I_{x_lower} equals the threshold of the converter overcurrent protection. As a result, the aperiodic component will be larger than that described in Fig. 6. Therefore, the selection of R_D should be designed with the actual parameters from the project.

Assuming that the number of the damping SMs is N_D, the largest voltage applied to each damping SM during the fault clearance process can be expressed as:

$$U_D = (I_{x\_lower} + \frac{2\sqrt{2}U_n}{\omega L})R_D \Big/ N_D < U_{IGBT}, \tag{17}$$

where U_{IGBT} is the maximum withstand voltage of IGBT. It can be seen from (17) that the voltage on the damping SMs will increase with the increase of R_D. Therefore, a number of N_D damping SMs should be connected in series to share the voltage force. The selection of N_D should satisfy (17).

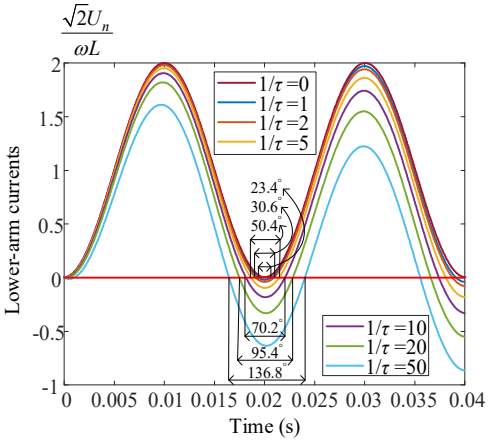


Fig. 6. Waveforms of lower-arm currents under different R_D.

The thyristor-pairs also need to withstand large voltages. The maximum voltage across the lower-arm thyristor-pairs will be the maximum of the post-fault valve-side voltage. And the maximum voltage across the upper-arm thyristor-pairs will be the sum of the post-fault valve-side voltage and the voltage difference (V_{diff}) between the DC line voltage and upper-arm SM total voltage. Therefore, a number of N_T thyristor pairs should be connected in series within the upper and lower arms to share the voltage force. N_T should satisfy:

$$(V_{diff} + \sqrt{2}U_n) \Big/ N_T < U_{Thy}, \tag{18}$$

where U_{Thy} is the maximum withstand voltage of the thyristor.

Although the overvoltage on damping SMs and thyristor pairs can be solved by increasing N_D and N_T, the capital cost and conduction losses will then be increased. Therefore, the selection of N_D and N_T should consider the IGBT and thyristor withstand voltage and the minimization of capital cost and conduction losses. The cost of the proposed method mainly comes from the semiconductor devices in the thyristor-pairs and the damping SMs. Assuming that the costs of the thyristor and IGBT are K_{Thy} and K_{IGBT}. The total cost of the proposed method can be expressed as:

$$K_{Total} = (6N_T + 3N_D)K_{Thy} + 3N_D K_{IGBT} \tag{19}$$

The series thyristor pairs and damping SMs will increase the power losses under normal operation: conduction losses of the IGBTs and thyristors when they are in the ON-state. The extra power losses caused by the additional devices in the converter can be expressed as follows [34]:

$$\begin{aligned} P_x &= \frac{1}{T_0}\int_{t\in\Phi_x} V_x(t)I_x(t)\tau_x(t)dt \\ &= \frac{1}{T_0}\int_{t\in\Phi_x} [a_x + b_x I_x(t) + c_x I_x^2(t)]dt \end{aligned} \tag{20}$$

where x=*TP*, *TD*, and *ID*, which represents the thyristors in thyristor pairs, the thyristors in damping SMs, and the IGBTs in damping SMs. $\tau_x(t)$ is the pulse function, $\tau_x(t)$=1 means the device is on, and $\tau_x(t)$=0 means the device is off. T_0 is the line frequency cycle, Φ_x is the effective on-state time of a device in a line frequency cycle, $V_x(t)$ is the voltage drop of a device when the operating current is $I_x(t)$, a_x, b_x, c_x are the fitted coefficients of the *V-I* curve of a switching device, which relate to the junction temperature. The total power losses caused by the additional devices can be expressed as:

$$P_{\text{loss}} = \sum_{i=1}^{6N_T} P_{TPi} + \sum_{i=1}^{3N_D} P_{TDi} + \sum_{i=1}^{3N_D} P_{IDi} \tag{21}$$

The parameter selection of the proposed method should satisfy (16)-(18), and the overall optimization goal of the parameter design is to minimize the capital cost and conduction losses expressed as (19) and (21). This protection method and the parameter design will be verified based on the Zhangbei four-terminal HB-MMC MTDC project in Section IV.

IV. Simulation Studies and Analysis

In this section, simulations will be carried out in PSCAD/EMTDC to verify the above analysis and protection.

A. System Modeling

The HB-MMC MTDC shown in Fig. 7 has been built in PSCAD. The converter parameters are obtained from the Zhangbei four-terminal ±500 kV HVDC project [5]. As the number of SMs will not affect the equivalent circuit of the MMC once it is blocked, a 41-level MMC is used in this study to ensure acceptable simulation efficiency. However, the SM capacitance is selected to ensure the same equivalent SM capacitance C_{equ} as the Zhangbei project to reflect the same SM capacitor charging behavior in the practical project. Parameters of the overhead line (OHL) model are taken from [35]. The parameters and dimensions of the OHL model are given in the Appendix. The AC systems are modeled as ideal AC sources with short-circuit impedances R_S+jL_S. The X_S/R_S and the AC system short-circuit ratio is assumed to be 10. System parameters are provided in Table I. In the system, MMC2 operates in a DC voltage and reactive power ($V_{dc}Q$) controlling mode, and MMC1, MMC3, and MMC4 operate in an active and reactive power (PQ) controlling mode.

B. Case Studies

1) Simulation analysis during a valve-side SPG fault

The upper-arm SM capacitors may suffer much worse overvoltage if the faulty converter station operates in the $V_{dc}Q$

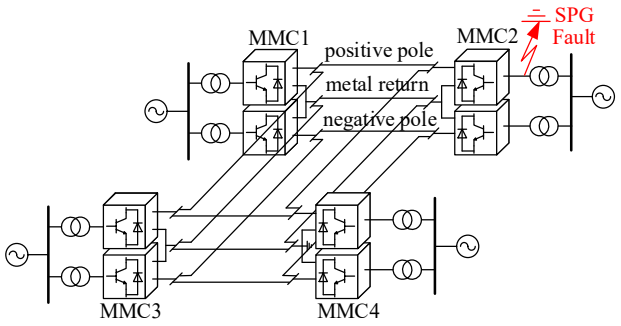


Fig. 7. Bipolar HB-MMC four-terminal MTDC system.

TABLE I
PARAMETERS OF THE BIPOLAR HB-MMC FOUR-TERMINAL MTDC

Parameters	Values
Capacity of each pole (MW)	1500
Rated DC voltage (kV)	±500
Rated AC voltage (kV)	230
AC grid frequency (Hz)	50
Transformer ratio (kV/kV)	230/260
Transformer leakage reactance (p.u.)	0.15
Number of SMs in each arm	40
DC terminal inductor (H)	0.15
SM capacitance (mF)	2.5
Arm inductance L (H)	0.04
Arm resistance R (Ω)	0.1
AC system equivalent resistance R_S (Ω)	0.35092
AC system equivalent reactor L_S (H)	0.01117
Parameters of IGBTs (kV/kA)	4.5 kV/3 kA
Threshold of converter overcurrent protection (kA)	4.5
Parameters of diodes (kV/kA)	4.5 kV/2.62 kA
I^2t of Diodes (10^6A^{2}s)	15.7
Length of the OHL (km)	MMC1-MMC2: 207.9 MMC1-MMC3: 49.9 MMC2-MMC4: 192.7 MMC3-MMC4: 217.6

controlling mode and is absorbing power from the DC circuit. To verify the fault analysis during the worst fault conditions, an SPG fault with a small fault resistance (0.001 Ω) has been applied in phase A of the $V_{dc}Q$ controlling MMC2, as shown in Fig. 7. The fault occurs at t = 2.005 s. The overcurrent protection scheme is employed in the simulation: the faulty converter will be blocked immediately if any arm current becomes over 4.5 kA. The other converters remain unblocked.

Fig. 8 illustrates the upper- and lower-arm SM capacitor voltages, arm currents, post-fault valve-side voltages, and grid-side currents of the faulty $V_{dc}Q$ controlling station (MMC2). As shown in Fig. 8(a), the upper-arm SM capacitors are overcharged during the negative half-cycles of the post-fault voltage. During the period shown in the figure, the capacitor voltage has reached a maximum of 1.80 p.u. Fig. 8(b) illustrates that the capacitor voltages of lower-arm SMs become constant when MMC2 is blocked. However, since the DC voltage controlling station MMC2 is blocked, the DC voltage will continuously increase, as shown in Fig. 8(g). Therefore, the upper-arm SM capacitors will keep being charged until the fault is cleared, which results in the upper-arm charging currents as shown in Fig. 8(c).

Since the charging process is periodic during every negative half-cycle of the valve-side voltages, the charging current will drop to zero when the process reaches a steady state. Therefore, a long discontinuous conduction time can be seen in the upper-arm currents, as shown in Fig. 8(c). Because only positive currents can flow through the lower-arm diodes, as shown in Fig. 8(d), the lower-arm currents contain large DC offsets, and the discontinuous conduction time is very small. Furthermore, the grid-side suffers non-zero-crossing fault currents within 150 ms after the fault, as shown in Fig. 8(f), which brings great challenges for the grid-side ACCB to isolate the fault.

Fig. 9 illustrates the fault current flowing through the antiparallel diodes and the I^2t of the diodes after the fault. The peak value of the current and the I^2t are 12.7 kA and 7.48×10^{6}A^{2}s. The I^2t capacity of the diodes is given in TABLE I and has a value of 15.7×10^{6}A^{2}s [36]. As shown in Fig. 9(b), the I^2t will continuously increase until the fault is cleared, which may exceed the I^2t capacity of the diodes. Therefore, it is

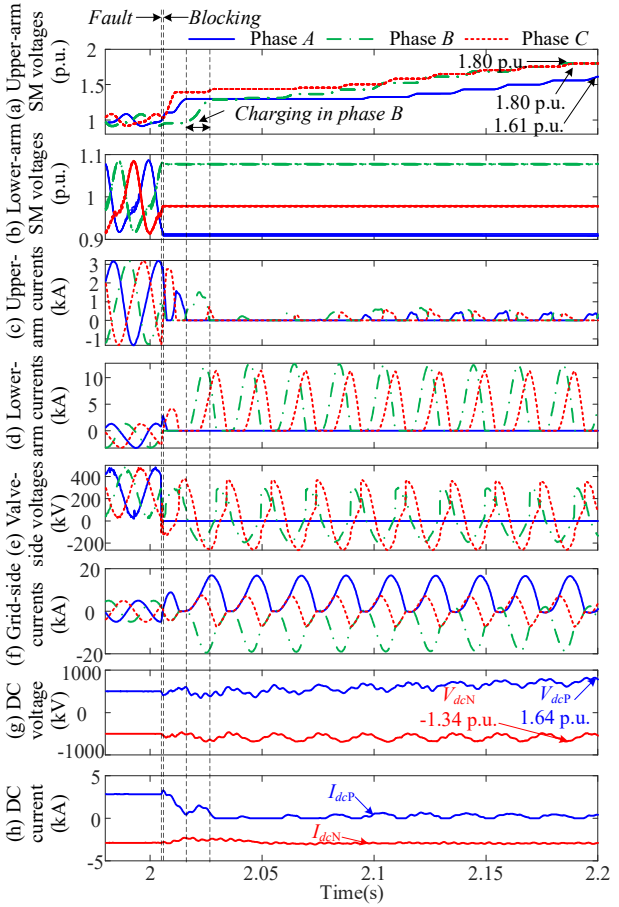


Fig. 8. Fault behavior without using the proposed protection scheme. (a) Upper-arm SM voltages. (b) Lower-arm SM voltages. (c) Upper-arm currents. (d) Lower-arm currents. (e) Valve-side voltages. (f) Grid-side currents. (g) DC current. (h) DC voltage.

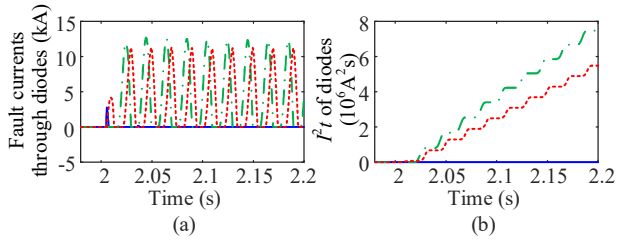


Fig. 9. Fault behavior without using the proposed protection scheme. (a) Fault currents thorough diodes. (b) I^2t of diodes.

necessary to solve the problem of non-zero-crossings and clear the fault as soon as possible.

2) Verification of the proposed protection scheme

To quickly clear the fault without relying on ACCBs and alleviate the SM overvoltage, the proposed protection scheme is used in the system shown in Fig. 7. After blocking the converter, the initial condition of the lower-arm current I_{x_lower} in (16) will be 4.5 kA. Substituting the actual parameters of the Zhangbei Project to (17), according to the analysis in Section III.B, the sum resistance of the damping SMs is set as 10 Ω.

The detection of the valve-side SPG fault is carried out through monitoring $3i_0$. It can be seen in Fig. 10 that $3i_0$ increases significantly once the fault occurs. When $3i_0$ exceeds the threshold after blocking the converter for 0.5 ms, the proposed protection method will be implemented. A 100 ms time delay is used to simulate the operating time of the ACCB [23]-[24] to fully isolate the fault from the AC grid. Moreover, MMC4 is set as the new $V_{dc}Q$ controlling station to stabilize the DC voltage. The transmitted powers of MMC1 and MMC3 are changed from 1500 MW to 750 MW to ensure the secure operation of the healthy converter stations after the fault occurrence. The effect of the protection is shown in Fig. 11.

Based on the analysis in Section II, the currents flowing through the upper arms exhibit a long discontinuous conduction time when the charging process reaches a steady state. The simulation results, as shown in Fig. 8(c), also show this characteristic. Therefore, the upper-arm thyristor-pairs can cut off the charging current path during the current discontinuous conduction period, as shown in Fig. 11(c). Subsequently, the charging process is suspended, and the voltages of upper-arm SM capacitors stabilize at a maximum of 1.39 p.u. as shown in Fig. 11(a). Meanwhile, the DC current reduces to zero, as shown in Fig. 11(h), and the DC voltage stabilizes at the rated DC voltage 500 kV (1.02 p.u.) about 50 ms after the fault, as shown in Fig. 11(g). Besides, Fig. 11(b) illustrates that the capacitor voltages of lower-arm SMs become constant once the converter is blocked, which is similar to Fig. 8(b).

The interruption of the lower-arm currents relies on the damping SMs to accelerate the attenuation of aperiodic components due to the large DC offsets. It can be seen in Fig. 11(d), the aperiodic component in lower-arm currents decays rapidly owing to the damping SMs, and the current waveform quickly shows a large discontinuous conduction angle so that the lower-arm thyristor-pairs can cut off the current at t = 2.03 s. Once the lower-arm currents are cut off, the grid-side currents reduce to zero, as shown in Fig. 11(f). The grid-side voltage becomes zero until the ACCB tripped at t = 2.115 s, as shown in Fig. 11(e). It can be seen from comparing Fig. 11(e) and (f) that the cut-off of the fault current does not rely on the tripping of ACCB.

As analyzed in Section III.B, the number of the thyristor-pairs and the damping SMs depend on the voltage applied to them. Fig. 12 shows the voltages on the upper- and lower-arm thyristor-pairs and the damping SMs. Due to the quick clearance of the fault, the voltage difference (V_{diff}) between the DC line voltage and the total voltage of the upper-arm SMs will be smaller than the valve-side post-fault line voltage and can be

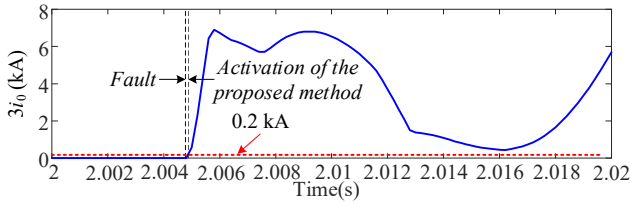


Fig. 10. Characteristics of $3i_0$ during a valve-side SPG fault at MMC_2.

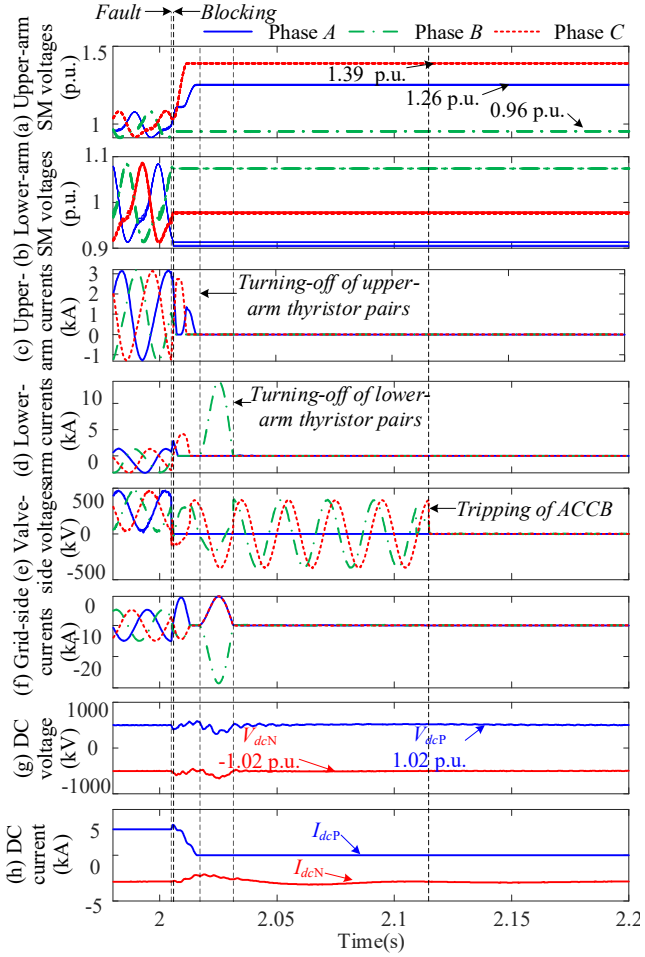


Fig. 11. Fault behavior using the proposed protection scheme. (a) Upper-arm SM voltages. (b) Lower-arm SM voltages. (c) Upper-arm currents. (d) Lower-arm currents. (e) Valve-side voltages. (f) Grid-side currents. (g) DC voltage. (h) DC current.

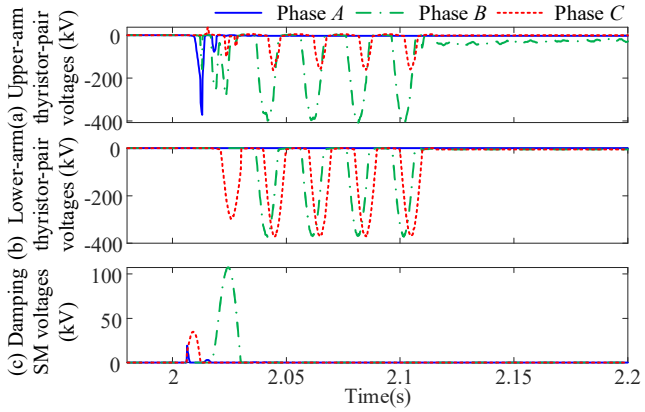


Fig. 12. Voltages of the thyristor-pairs and damping SMs. (a) Upper-arm thyristor-pair voltages. (b) Lower-arm arm thyristor-pair voltages. (c) Damping SM voltages.

ignored. Therefore, the maximum voltage on the upper-arm thyristor-pairs approximately equals the valve-side line voltage. Substituting the parameters of Zhangbei projects to (17)-(18), the maximum voltage on the thyristor-pairs and the damping SMs are 260√2 kV and 123 kV, which are consistent with the simulation results in Fig. 12. The parameters of the widely used thyristor are 8.5 kV/5 kA. The parameters of the IGBTs used in the Zhangbei project are 4.5 kV/3 kA. Therefore, each upper and lower arm should use 45 thyristor-pairs. Each lower arm should use 30 damping SMs, each with a resistor of 0.33 Ω.

3) Responses of the healthy station during the fault

Since the valve-side SPG fault occurs in the station, it is hoped that the protection should only block the faulty station and cut off the connection between the faulty station and the system. Meanwhile, the healthy converter stations should not be affected. Figs. 13 and 14 illustrate the responses of MMC4 during the SPG fault at MMC2 before and after the protection method is employed.

It can be seen in Figs. 13(a) and (b) that the voltages of the lower- and upper-arm SMs will continuously increase after the fault, so does the DC voltage, as shown in Fig. 13(e). The arm currents are similar to the normal operation, as shown in Figs. 13(c) and (d). However, the DC current, as shown in Fig. 13(f), decreases as the DC voltage increases to maintain the active power. In general, the converter will be blocked when the capacitor voltage is higher than 1.2 p.u. Therefore, the receiving stations will both be blocked, and then the sending stations should also be blocked to avoid power surplus. As a result, a blackout may occur to the entire MTDC system.

After applying the protection scheme, the arm SM capacitor voltages are controlled to stabilize at the rated values, as shown in Figs. 14(a) and (b). Since a receiving-end converter station is blocked, the active power reference values of the sending-end converter stations are adjusted to half of the original value, so the arm currents of MMC4 will not increase, as shown in Figs. 14(c) and (d). It can be seen in Figs. 14(e) and (f) that the DC voltage and current stabilize at the rated value about 100 ms after the fault. Therefore, the proposed method effectively avoids the outage of the entire system.

4) Comprehensive comparison with other schemes

As analyzed above, the upper-arm SM capacitor overvoltage, grid-side non-zero-crossing currents, and impacts on the healthy stations are the main problems caused by the valve-side SPG faults. To ensure the occurrence of grid-side current zero-crossings and limit the overvoltage of upper-arm SM capacitors, several protection methods have been proposed to protect the converters against valve-side SPG faults, such as the auxiliary ACCB based protection [14], the *LR* circuit based protection [18], the mixed-SM based protection [17], the bypass-switch based protection [15], and the double-thyristor based protection [16]. Fig. 15 gives the arrangements of the five methods.

To ensure the occurrence of grid-side current zero-crossings, the auxiliary resistor R_{AUX} in Fig. 15(a) has been set as 5 Ω. The L_G and R_G in Fig. 15(b) have been set as 0.4 H and 20 Ω to ensure the grid-side zero-crossing can last longer than 60 ms for the operation of the grid-side ACCB. The mixed-SM based method in Fig. 15(c) applies HB-SMs in the upper arms and FB-SMs in the lower arms. The bypass-switch based method uses the fast bypass switch installed parallel with the lower-arm SMs, as Fig. 15(d) shows. The double-thyristor based method is shown in Fig. 15(e). The abovementioned methods must be combined with the opening of the ACCBs to isolate the fault

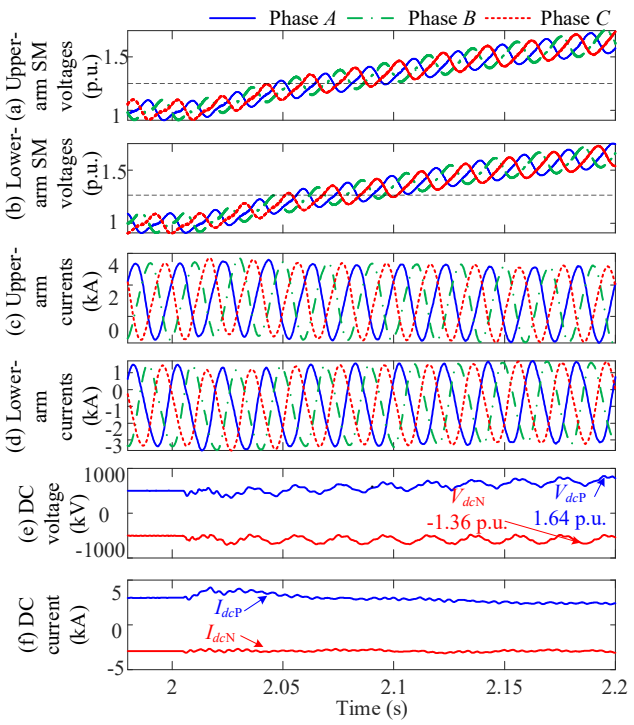


Fig. 13. Fault behavior of MMC4 without using the proposed protection scheme. (a) Upper-arm SM voltages. (b) Lower-arm SM voltages. (c) Upper-arm currents. (d) Lower-arm currents. (e) DC voltage. (f) DC current.

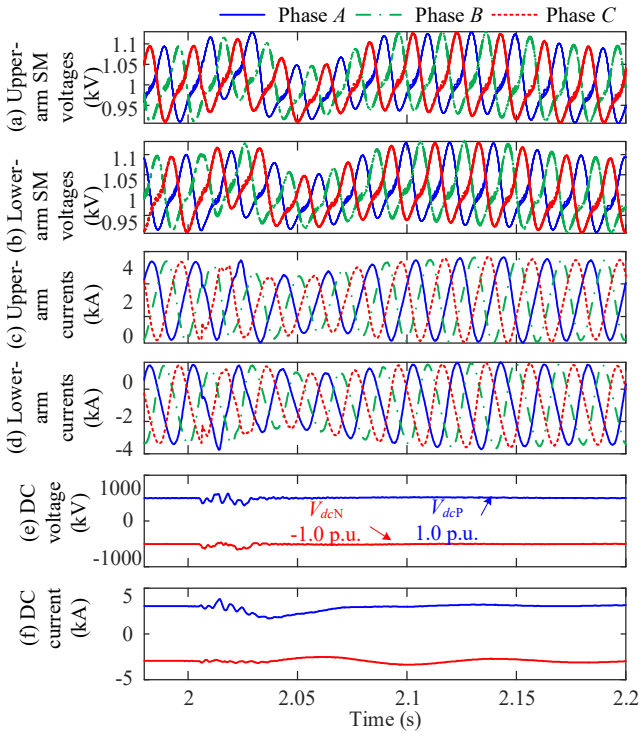


Fig. 14. Fault behavior of MMC4 using the proposed protection scheme. (a) Upper-arm SM voltages. (b) Lower-arm SM voltages. (c) Upper-arm currents. (d) Lower-arm currents. (e) DC voltage. (f) DC current.

from the AC grid, in which fast ACCBs are utilized and the operation time is set as 60 ms. To make a comprehensive comparison between the proposed method with these conventional protection schemes, Fig. 16 illustrates the simulation results of grid-side currents, upper-arm voltage, lower-arm currents, DC voltages, and currents of the positive and negative poles ($V_{dc\mathrm{P}}$, $V_{dc\mathrm{N}}$, $I_{dc\mathrm{P}}$, and $I_{dc\mathrm{N}}$) under different protection methods.

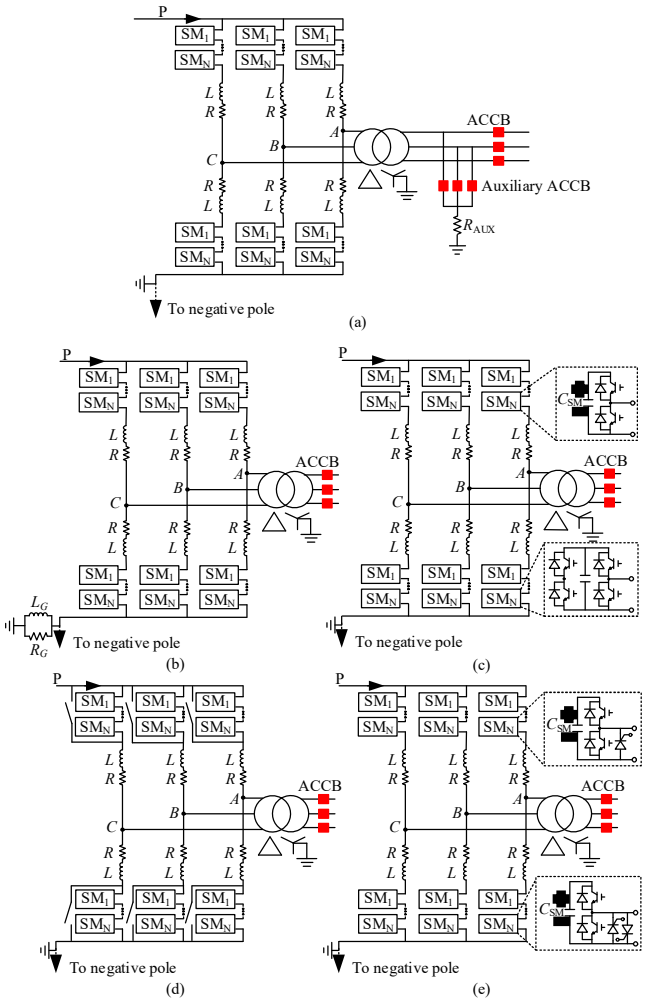


Fig. 15. The arrangements of the five studied protection methods. (a) The pole arrester and auxiliary ACCB based method. (b) The *LR*-circuit based method. (c) The mixed-SM based method. (d) The bypass-switch based method. (e) The double-thyristor based method.

It can be seen from Fig. 16 that all of the methods can create zero-crossings in grid-side currents. Considering the fast ACCBs can open within 2 or 3 times line-frequency cycles, the auxiliary ACCB based method takes longer time (about 120 ms) to clear the fault as the auxiliary ACCB has to be closed before the main ACCB opens to ensure the generation of grid-side current zero-crossings. It can be seen from Fig. 16(a) that, the overvoltage and overcurrent can be mitigated once the ACCB opened. However, the healthy pole in the auxiliary ACCB based method experiences large disturbances as the $V_{dc\mathrm{N}}$ and $I_{dc\mathrm{N}}$ show in Fig. 16(a). Besides, a large disturbance on the AC system will be caused by the created grid-side three-phase fault. It can be seen in Fig. 16(b) that the *LR* circuit based method also causes large disturbance on the healthy pole, which is mainly because that fault currents flow through the *LR* circuit and therefore raise the DC side voltage potential of the converter.

Comparing the proposed method and the five conventional methods, the overvoltage of the proposed method [1.39 p.u. in Fig. 11(a)] is alleviated better than other methods, such as the auxiliary ACCB based method [1.44 p.u. in Fig. 16(a)] and the *LR* circuit based method [1.64 p.u. in Fig. 16(b)]. Although the mixed-SM based method does not lead to overcurrent in the lower arms due to the blocked current path by the FB-SMs, the severe upper-arm overvoltage [1.93 p.u. in Fig. 16(c)] and high capital cost are the main limitations of this method.

As for the bypass-switch based and double-thyristor based methods, the upper-arm overvoltage [1.69 p.u. in Fig. 16(d) and 1.65 p.u. in Fig. 16(e)] is higher than the proposed method [1.39 p.u. in Fig. 11(a)]. The utilization of grid-side fast ACCB in these two methods also contributes to mitigating the overvoltage compared with using slow ACCBs. However, the upper-arm fault current paths cannot be fully cut off after opening the ACCB. The transmitted power from the power-sending station makes the DC voltage and upper-arm SM capacitor voltage continuously increase even after opening the ACCB. Besides, the bypass-switch and double-thyristor based methods lead to a more severe and long-lasting lower-arm overcurrent than the proposed method [as shown in Fig. 11(c)], which increases the risk to thyristors and diodes.

In summary, the proposed method performs better in suppressing upper-arm overvoltage and lower-arm overcurrent and results in the least impact on the healthy pole compared with other conventional methods. Although the capital cost and power losses are increased, they can be minimized by optimizing the parameter design.

V. Conclusion

In order to achieve fast and reliable protection against valve-side SPG faults in bipolar HB-MMC MTDC systems without using the grid-side ACCB and affecting healthy converter stations, this paper proposes an ACCB-independent scheme based on thyristor-pairs and damping SMs. The characteristics of the currents flowing through the upper and lower arms have been theoretically analyzed. The discontinuous conduction time in the first cycle of the arm currents can be used to isolate the converter. Based on the analysis, arm thyristor-pairs are proposed to cut off the arm currents during the discontinuous conduction time. To accelerate the damping of the lower-arm fault currents and help the thyristor-pairs turn off, damping SMs are installed within the lower arms of the converter. The proposed scheme can quickly cut off the arm fault currents without relying on the ACCBs, and therefore, the system can be quickly protected. Although the proposed protection scheme causes conduction losses and increases system complexity, it can effectively protect the faulty converter and healthy circuit in the MTDC system. The minimization of the power losses and system complexity caused by the proposed method will be the future work. The simulation results in PSCAD match well with the theoretical analysis and therefore, verify the effectiveness of the proposed protection.

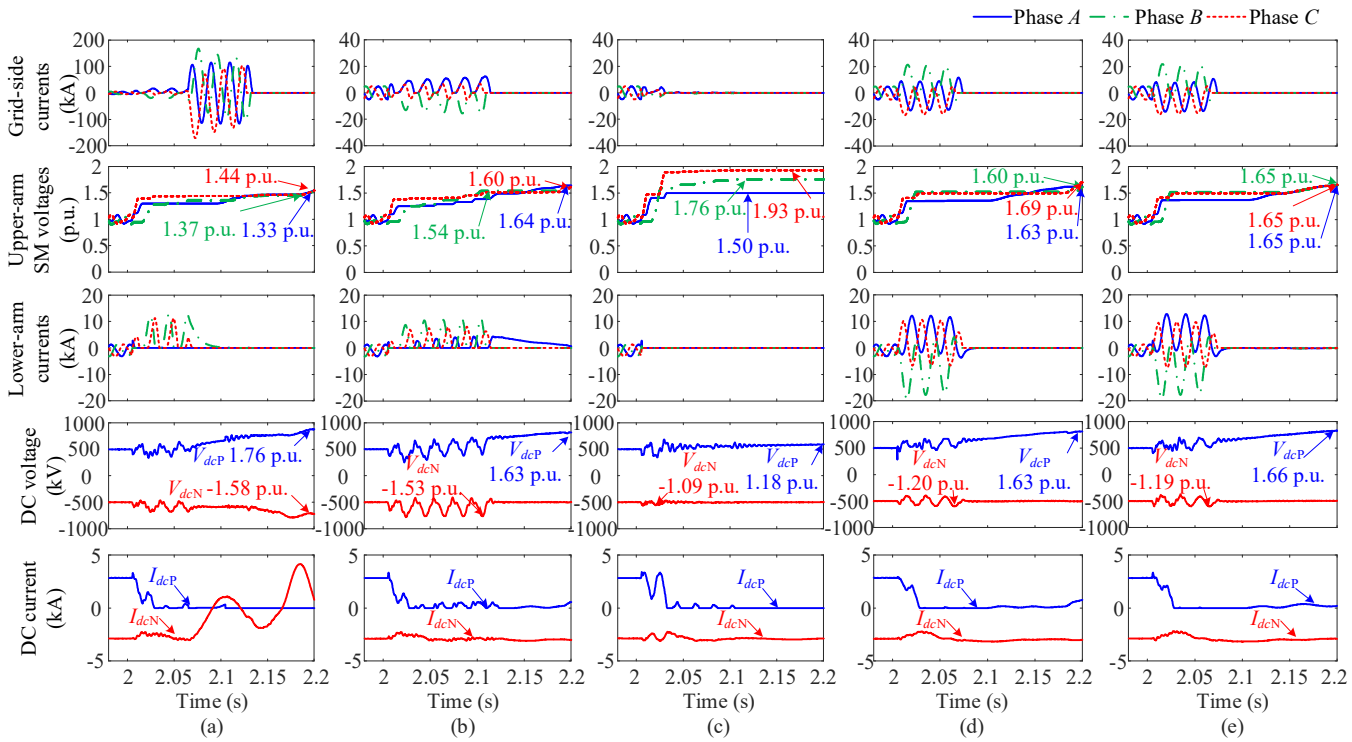


Fig. 16. Results of employing the five studied protection methods. (a) The auxiliary ACCB based method. (b) The *LR*-circuit based method. (c) The mixed-SM based method. (d) The bypass-switch based method. (e) The double-thyristor based method.

APPENDIX

The parameters and dimensions of the OHL used in this paper are shown in Fig. 17.

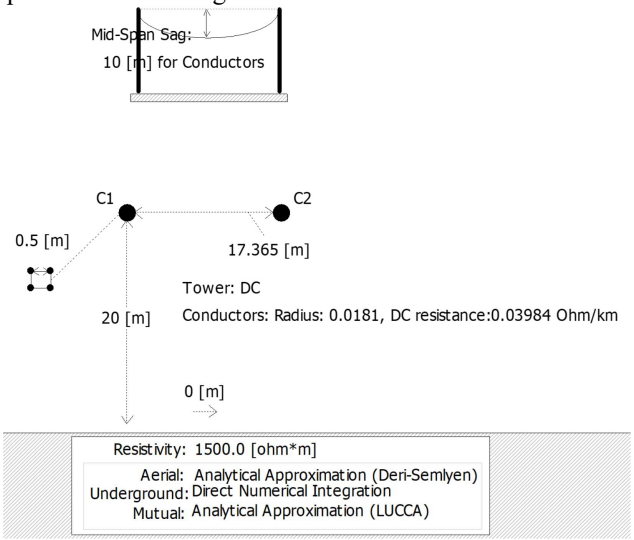


Fig. 17. OHL configuration and dimensions.

REFERENCES

[1] X. Li, Q. Song, W. Liu, H. Rao, S. Xu, and L. Li, "Protection of nonpermanent faults on DC overhead lines in MMC-based HVDC systems," *IEEE Trans. Power Del.*, vol. 28, no. 1, pp. 483-490, Jan. 2013.

[2] G. Li, *et al.*, "Power reversal strategies for hybrid LCC/MMC HVDC systems," *CSEE Journal of Power and Energy Systems*, vol. 6, no. 1, pp. 203-212, March 2020.

[3] R. Hong, "Architecture of Nan'ao multi-terminal VSC-HVDC system and its multi-functional control," *CSEE Journal of Power and Energy Systems,* vol. 1, no.1, pp. 9-18, March 2015.

[4] G. F. Tang, Z. Y. He, H. Pang, X. M. Huang, and X. P. Zhang, "Basic topology and key devices of the five-terminal DC grid," *CSEE Journal of Power and Energy Systems*, vol. 1, no. 2, pp.22-35, June 2015.

[5] Z. Li, Y. Tang, Z. Zhao, et al., "The model and parameters based on the operation mode of a 500 kV multi-terminal flexible dc power grid," *Int. J. Power Eng. Eng. Thermophysics*, vol. 1, no. 1, pp. 16–24, 2017.

[6] D. Van Hertem and M. Ghandhari, "Multi-terminal VSC HVDC for the European supergrid: Obstacles," *Renew. Sustain. Energy Rev.*, vol. 14, no. 9, pp. 3156–3163, 2010.

[7] Q. Huai, K. Liu, A. Hooshyar, H. Ding, K. Chen, and Q. Liang, "Single-ended line fault location method for multi-terminal HVDC system based on optimized variational mode decomposition", *Electr. Power Syst. Res.*, vol. 194, 107054, May 2021.

[8] M. Hajian, L. Zhang, and D. Jovcic, "DC transmission grid with lowspeed protection using mechanical DC circuit breakers," *IEEE Trans. Power Deliv.*, vol. 30, no. 3, pp. 1383–1391, 2015.

[9] L. Tang and B. Ooi, "Locating and Isolating DC Faults in Multi-Terminal DC Systems," *IEEE Trans. Power Del.*, vol. 22, no. 3, pp. 1877-1884, July 2007.

[10] X. Han, W. Sima, M. Yang, L. Li, T. Yuan and Y. Si, "Transient Characteristics Under Ground and Short-Circuit Faults in a ±500 kV MMC-Based HVDC System With Hybrid DC Circuit Breakers," *IEEE Trans. Power Del.*, vol. 33, no. 3, pp. 1378-1387, June 2018.

[11] J. Cheng and Z. Xu, "Analysis of AC faults in converter station and characteristics of its relay protection", *Proc. Chin. Soc. Elect. Electron. Eng.*, vol. 31, no. 22, August 2011, pp. 88-95.

[12] X. Li, Y. Liu L. Yang, Z. Cai and K. Han, "Research on single phase grounding fault at HVDC converter transformer valve side," in *2011 4th International Conference on Electric Utility Deregulation and Restructuring and Power Technologies (DRPT)*, Weihai, Shandong, 2011, pp. 471-476.

[13] T. Zheng, X. Liu, X. Guo, "Analysis of fault-induced inrush current of converter transformer in LCC HVDC system considering DC control and protection," *Int. J. Power Energy Syst.*, vol. 125, 106536. Feb 2021.

[14] G. Andersson and M. Hyttinen, "Skagerrak The Next Generation," in *Proc. HVDC Power Electron. Tech., CIGRE*, 2015, pp. 1–9.

[15] Y. Zhou, Z. He, H. Pang, J. Yang, and Q. Li, "Protection of converter grounding fault on MMC based bipolar HVdc systems," *Proc. Chin. Soc. Elect. Electron. Eng.*, vol. 35, no. 16, pp. 4062–4069, Aug. 2015.

[16] G. Li, W. Liu, T. Joseph, J. Liang and Z. Song, "Double-Thyristor-Based Protection for Valve-Side Single-Phase-to-Ground Faults in HB-MMC-

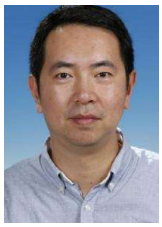
Based Bipolar HVDC Systems," *IEEE Trans. Ind. Electron.*, vol. 67, no. 7, pp. 5810-5815, July 2020.
[17] G. Li, J. Liang, F. Ma, C. E. Ugalde-Loo, H. Liang and H. Li, "Analysis of single-phase-to-ground faults at the valve-side of HB-MMCs in bipolar HVDC systems," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 2659-2665, doi: 10.1109/ECCE.2017.8096501.
[18] G. Li, J. Liang, F. Ma, C. E. Ugalde-Loo and H. Liang, "Analysis of Single-Phase-to-Ground Faults at the Valve-Side of HB-MMCs in HVDC Systems," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2444-2453, March 2019.
[19] W. Liu, G. Li, J. Liang, C. E. Ugalde-Loo, C. Li and X. Guillaud, "Protection of Single-Phase Fault at the Transformer Valve Side of FB-MMC-Based Bipolar HVdc Systems," *IEEE Trans. Ind. Electron.*, vol. 67, no. 10, pp. 8416-8427, Oct. 2020.
[20] G. Li, J. Liang, C. E. Ugalde-Loo, F. Ma, H. Liang and Z. Song, "Protection for Submodule Overvoltage Caused by Converter Valve-Side Single-Phase-to-Ground Faults in FB-MMC Based Bipolar HVDC Systems," *IEEE Trans. Power Del.*, vol. 35, no. 6, pp. 2641-2650, Dec. 2020.
[21] S. Xue, C. Gu, B. Liu and B. Fan, "Analysis and Protection Scheme of Station Internal AC Grounding Faults in a Bipolar MMC-HVDC System," *IEEE Access*, vol. 8, pp. 26536-26548, 2020.
[22] A. Nami, J. Liang, F. Dijkhuizen, and P. Lundberg, "Analysis of modular multilevel converters with DC short circuit fault blocking capability in bipolar HVDC transmission systems," in *17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Geneva, Switzerland, 2015, pp. 1-10.
[23] IEEE Guide for Specifications of High-Voltage Circuit Breakers (over 1000 V), in *IEEE Std C37.12-2018 (Revision of IEEE Std C37.12-2008)*, pp. 1-43, 17 April 2019.
[24] L. X. Tang and B. T. Ooi, "Locating and Isolating DC Faults in Multi-Terminal DC Systems," *IEEE Trans. Power Del.*, vol. 22, no. 3, pp.1877-1884, July 2007.
[25] K. Han, Z. Si, S. Hu, K. Xia, and Lei Z, "Voltage-Balance Characteristics for Submodule of VSC-HVDC Damping Converter Valve During System Charging Process," *Southern Power Syst. Technol.*, vol. 13, no. 6, pp. 8-15+29, Jun. 2019. (in Chinese).
[26] B. Que, J. Li, N. Wang, Y. Dong, Y. Lu, and J. Tian, "Arm Damping Based Quick Recovery Scheme for Flexible HVDC Fault," *Automat Electron Power Sys.*, vol. 40, no. 24, pp. 85-91, Dec. 2016.
[27] H. Ma, W. Yao, J. Wu, D. Hang, M. Yang, S. Sun, et al, "Analysis of DC Pole-to-Pole Short Circuit Fault Behavior in MMC-HVDC Transmission Systems With Bridge Arm Damper," *Power Syst. Technol.*, vol. 41, no. 7, pp. 2099-2106, Jul. 2017.
[28] Q. Song, R. Zeng, Z. Yu, W. Liu, Y. Huang, W. Yang, et al., "A Modular Multilevel Converter Integrated With DC Circuit Breaker," *IEEE Trans. Power Del.*, vol. 33, no. 5, pp. 2502-2512, Oct. 2018.
[29] X. Li, W. Liu, Q. Song, H. Rao and S. Xu, "An enhanced MMC topology with DC fault ride-through capability," *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, Vienna, Austria, 2013, pp. 6182-6188.
[30] P. D. Judge, M. M. C. Merlin, T. C. Green, D. R. Trainer and K. Vershinin, "Thyristor-Bypassed Submodule Power-Groups for Achieving High-Efficiency, DC Fault Tolerant Multilevel VSCs," *IEEE Trans. Power Del.*, vol. 33, no. 1, pp. 349-359, Feb. 2018.
[31] S. Wenig. "Potential of Bipolar Fullt-Bridge MMC-HVdc Transmission for Link and Overlay Grid Applications," Ph.D. dissertation, Elektrotechnik und Informationstechnik, Karlsruhe Institute of Technology, Baden-Würtemberg, Germany, 2019.
[32] M. Singh, K. Khanchandani, "Thyristor: Principles and Charactristics," in *Power Electronics*, 2nd ed. Beijing, China: Tsinghua University Press, 2011,ch. 2, sec. 2.10. pp. 38-55.
[33] Q. Bo, L. Jihong, W. Nannan, et al, "Arm Damping Based Quick Recovery Scheme for Flexible HVDC Fault," *Automation of Electric Power Systems*, vol. 40, no. 2, pp. 85-91, Dec. 2016.
[34] J. Liu, J. Yao, S. Yang and K. Wang, "Loss analysis of two kinds of flexible HVDC converters," in *Proceedings of The 7th International Power Electronics and Motion Control Conference*, Harbin, 2012, pp. 1669-1674.
[35] P. Liu, R. Che, Y. Xu and H. Zhang, "Detailed modeling and simulation of ±500kV HVDC transmission system using PSCAD/EMTDC," in *2015 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, Brisbane, QLD, 2015, pp. 1-3.
[36] *Datasheet: Fast Recovery Diode, 5SDF 28L4520,* ABB, Zurich, Switzerland, 2013.

Xiaoxiao Liu (S'20) received the the B.Eng. degree in Electrical Engineering and Its Automation from North China Electric Power University, Beijing, China, in 2018, the M.Sc. degree in Electrical Engineering from North China Electric Power University, Beijing, China, in 2021. She is now pursuing the Ph.D. degree in Electrical Engineering at KU Leuven, Leuven, Belgium. Her research interests include control and protection of HVDC system.

Gen Li (M'18) received the B.Eng. degree in Electrical Engineering from Northeast Electric Power University, Jilin, China, in 2011, the M.Sc. degree in Power Engineering from Nanyang Technological University, Singapore, in 2013 and the Ph.D. degree in Electrical Engineering from Cardiff University, Cardiff, U.K., in 2018.

From 2013 to 2016, he was a Marie Curie Early Stage Research Fellow funded by the European Commission's MEDOW project. He has been a Visiting Researcher at China Electric Power Research Institute and Global Energy Interconnection Research Institute, Beijing, China, at Elia, Brussels, Belgium and at Toshiba International (Europe), London, U.K. He has been a Research Associate at the School of Engineering, Cardiff University since 2017. His research interests include control and protection of HVDC and MVDC technologies, power electronics, reliability modelling and evaluation of power electronics systems.

Dr. Li is a Chartered Engineer in the U.K. He is an Associate Editor of the CSEE Journal of Power and Energy Systems. He is an Editorial Board Member of CIGRE ELECTRA. He is an IET Professional Registration Advisor. His Ph.D. thesis received the First CIGRE Thesis Award in 2018. He is the Vice-Chair of IEEE PES Young Professionals and the Technical Panel Sectary of CIGRE UK B5 Protection and Automation.



Tao Zheng (M'13) was born in Shandong, China, in 1975. He received the Ph.D. degree in power systems and automation from North China Electric Power University (NCEPU), Beijing, China, in 2005. He is currently a Professor with the School of Electrical and Electronic Engineering, NCEPU. His research interests are focused in the area of power system protection.

Xinhui Yang received the B.Eng. degree in Electrical Engineering from North China Electric Power University, Beijing, China, in 2019. She is now a master student at North China Electric Power University, Beijing, China, in Electrical Engineering.

Josep M. Guerrero (S'01-M'04-SM'08-FM'15) received the B.Sc. degree in telecommunications engineering, the M.Sc. degree in electronics engineering, and the Ph.D. degree in power electronics from the Technical University of Catalonia, Barcelona, in 1997, 2000 and 2003, respectively. Nowadays he is working towards the M.Sc. Degree in Psychobiology and Cognitive Neuroscience at the Autonomous University of Barcelona.

Since 2011, he has been a Full Professor with AAU Energy, Aalborg University, Denmark, where he is responsible for the Microgrid Research Program. From 2019, he became a Villum Investigator by The Villum Fonden, which supports the Center for Research on Microgrids (CROM) at Aalborg University, being Prof. Guerrero the founder and Director of the same center (www.crom.et.aau.dk). His research interests are oriented to different microgrid frameworks in applications like microgrid clusters, IoT-based and digital twin, maritime microgrids for electrical ships, vessels, ferries and seaports, and space microgrids applied to nanosatellites and closed ecological systems.