Fully Symmetrical Hybrid PV Converter with Low Common-mode Noise

Tang, Zhongting; Sangwongwanich, Ariya; Blaabjerg, Frede

Published in:
IEEE Transactions on Industrial Electronics

DOI (link to publication from Publisher):
10.1109/TIE.2023.3285979

Publication date:
2024

Document Version
Accepted author manuscript, peer reviewed version

Fully Symmetrical Hybrid PV Converter with Low Common-mode Noise

Zhongting Tang, *Member, IEEE*, Ariya Sangwongwanich, *Member, IEEE*, and Frede Blaabjerg, *Fellow, IEEE*

***Abstract*—Hybrid converters with multiports (simultaneous DC and AC outputs) are promising solutions to reduce conversion stages from solar energy to various loads, and thereby increasing the utilization of residential PV systems. Considering common-mode noises suppression and high reliability, this paper proposes a fully symmetrical hybrid PV converter concept with two DC ports and one AC port. The proposed converter adopts symmetrical boost impedances at the low-voltage DC port and symmetrical synchronization rectifier switches at the high-voltage DC port. In addition, a symmetrical AC-decoupling inverter, i.e., highly efficient and reliable inverter concept (HERIC), operates as either a boost switch or an inverter to perform DC-DC and DC-AC conversions simultaneously. Combined with a dedicated modulation method with deadtime, the proposed converter has low leakage currents for grid-connected PV applications, low CM noise as a DC-DC converter, and flexible power control capability. Experiments have been carried out on a prototype to verify the effectiveness of the proposed converter.**

***Index Terms*—Common-mode (CM) noise, hybrid power converter, grid-connected, PV system**

I. Introduction

MULTI-port power converters (i.e., multiple DC and/or AC ports) have been extensively developed to meet applications for mixed sources (e.g., solar PV, fuel cells and batteries [1], [2]) and various loads (e.g., AC appliances, electric vehicle (EV) chargers, and data centers) in distributed power systems. For instance, some residential building adopts DC-nanogrid systems to support multiple loads [3]. Such DC-nanogrid systems mostly design the topologies and controls for off-grid applications with low voltage levels [4], [5]. It is difficult for intermittent renewable energy to ensure a stable and reliable power supply for home appliances. Thus, the integration of the energy storage, the grid, and PV energy is highly demanded, which requires advanced techniques of multi-port converters and flexible power management capability [6]. To increase PV-plus-storage utilization and enhance the grid integration of solar energy [7], the intelligent PV system should have several advantages: 1) hybrid multi-port topologies with DC and AC ports for energy storage integration [6], 2) high reliability with few conversion stages, 3) low common-mode (CM) noise (i.e., small electromagnetic interference (EMI) filter) even applying wide-bandgap devices of fast switching speed [8], 4) flexible power control capability for the resilience of power supply to the end-users [1], [6].

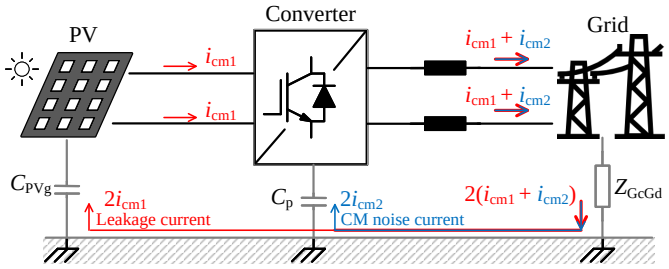

Fig. 1. Common-mode (CM) noise paths of PV converter, where $2i_{cm1}$ is the leakage current/CMC caused by the parasitic capacitor C_{PVg} between the PV panel and the ground, and $2i_{cm2}$ is the CMC caused by the parasitic capacitor C_p between power devices and the ground.

Traditional hybrid multi-port converters are usually composed of several converters in series or parallel, integrating at the DC-bus or AC-bus, e.g., two-stage converters [9], interleaved boost converter-based hybrid converter [10] and cascaded H-bridge converter [11]. For instance, a grid-tied two-stage converter is employed in [9] to connect the DC nanogrid to the utility AC grid, where a synchronous rectifier DC-DC converter and a full-bridge inverter were connected in a cascaded way to provide bidirectional power flow. Literature [12] proposes a systematic method for deriving interleaved-boost-based multiport converters (transformer-based). However, those converter structures in [9]–[12] lead to several limitations regarding power density, current-balance (parallel structure) and voltage-balance (cascaded structure) issues, which resulted in low efficiency and high system costs.

By comparison, the stand-alone multi-port converters have improved performance in power density, control complexity and system costs [6]. The main concept of the stand-alone multiport converter is adopting fewer devices to achieve the same performance as the multi-stage one, increasing conversion efficiency, compactness and reliability [13]–[15]. For example, the stand-alone hybrid converter in [13] adopts a voltage source inverter (VSI) to achieve DC and AC outputs simultaneously (i.e., various power supplies). An interleaved-boost three-port converter was proposed for hybrid renewable energy systems by employing an interleaved DC-DC converter and a transformer [14]. Moreover, the split source inverter was

Manuscript received November 30, 2022; revised February 17 and May 04, 2023; accepted June 07, 2023. This work was supported by the Novo Nordisk Fonden through the Interdisciplinary Synergy Programme (Award Ref. No.: NNF18OC0034952).

Z. Tang, A. Sangwongwanich, and F. Blaabjerg are with AAU Energy, Aalborg University, Aalborg 9220, Denmark (emails: zta@energy.aau.dk, ars@energy.aau.dk, and fbl@et.aau.dk).

used in [15] to achieve high compactness, high efficiency, flexible power control and voltage-boosting. Among them, the boost-derived hybrid converter concept has better performances in terms of efficiency and compactness since its power devices have multi-function [13], though in [13] and [15] the topologies have no leakage current suppression capability.

In respect to the CM noise issues, there are two concerns for hybrid PV converters. One is the CM noise caused by the parasitic capacitor between PV panels and the ground, leading to high leakage current/common-mode current (CMC) (see the red current path in Fig. 1) and it might be threatening the safety of persons and devices [16]. According to DIN VDE 0126 standard in Germany [17], the root-mean-square (RMS) value of the leakage current should be lower than 300 mA, and its transient should be limited. In [14], a transformer is adopted to achieve low leakage currents, compromising power density and efficiency. A transformerless hybrid converter employing a dual-buck inverter as the boost switch is developed to maintain a constant common-mode voltage (CMV) [18]. However, the dual-buck inverter has low utilization of AC inductors, leading to low power density. Another transformerless hybrid converter is introduced by adopting a symmetrical boost inductor and a symmetrical VSI to achieve low leakage currents as well as high power density in [19]. Based on it, an interlinking power converter [20] is proposed to achieve both flexible power control [21] and low leakage current. However, only the CMC between one DC port and the AC port is considered.

Following the blue current path in Fig. 1, the other is the CM conducted noise caused by the parasitic capacitor between power devices and the ground [22], challenging the electromagnetic compatibility (EMC) especially when the switching frequency of the wide-bandgap devices is further increased [8]. To reduce the CM noise and meet the EMC requirements, EMI filters are usually employed, leading to low power density and efficiency. Thus, many research modify the circuit configuration to eliminate the CM noise, mainly containing balancing techniques [23] and passive cancellation methods [24]. For example, the balancing technique in [25] develops a symmetrical circuit configuration to reduce the CM noise. Besides, a compensation filter with a transformer inductor and a capacitor is employed in [24] to attenuate the CM noise, reducing the EMI filter size. Although extra components are needed, those methods can suppress the CM noise, which has been employed in the proposed converter.

To enhance the multiple functions of the multi-port converter, this paper proposes a new fully symmetrical three-port hybrid converter, focusing on low CM noises (i.e., low CM noise for the DC-DC conversion and low leakage current/CMC for the DC-AC conversion) and flexible power control. To achieve those goals, the proposed converter should combine the advantages of the symmetrical structure (i.e., symmetrical boost impedance, symmetrical synchronous rectifier switches) and a symmetrical AC-decoupling inverter as well as a specific modulation method. The fully symmetrical hybrid converter is depicted in Section II, where CM noise models are discussed. In Section III, the analysis of operation modes and CMV performance are described. Then, the proposed modulation scheme and control are introduced in Section IV. Experiments verify the proposed converter in terms of multiple outputs capability, low CM noises and flexible power flow capability in Section V. Finally, conclusions are provided in Section VI.

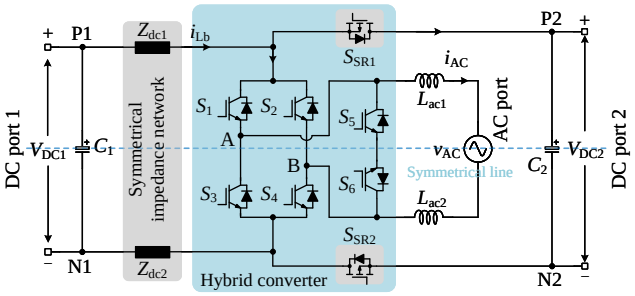

Fig. 2. Topology of the fully symmetrical hybrid converter.

II. Proposed Fully Symmetrical Hybrid PV Converter

A. Topology

Based on the concept of the stand-alone hybrid converter in [13] and balanced configuration [25], a fully symmetrical hybrid converter with two DC ports and one AC port is proposed, as shown in Fig. 2. The proposed converter consists of three symmetrical parts: 1) symmetrical impedances Z_{dc1} and Z_{dc2}, i.e., $Z_{dc1} = Z_{dc2}$; 2) two symmetrical synchronization rectifier switches, S_{SR1} and S_{SR2}; 3) a HERIC inverter (the symmetrical AC-decoupling inverter), which is consisting of six semiconductor devices (insulated-gate bipolar transistors (IGBTs) with anti-parallel diodes) $S_{1\text{-}6}$, and two AC filters L_{ac1} and L_{ac2}, i.e., $L_{ac1} = L_{ac2}$. Besides, C_1 and C_2 are the capacitors of DC port 1 and DC port 2. V_{DC1}, V_{DC2} and v_{AC} are voltages of DC port 1, DC port 2 and the AC port, respectively. i_{Lb} and i_{AC} are the boost impedance current and the AC output current. It should be noted that other symmetrical AC-decoupling inverters can be applied in the proposed hybrid converter to perform the same work as the HERIC with a corresponding modulation method. The HERIC is chosen in the proposed converter due to its relatively high efficiency.

B. CMV model

To address the two CM issues (i.e., leakage current issue and the CM noise impacting EMI performance) mentioned in Section I, the CM model of the proposed fully symmetrical hybrid converter is derived in Fig. 3. The CMVs are analyzed in Fig. 4 under different switching mode operations.

1) **CMV1**: As shown in Fig. 4 (a), the leakage current loop between DC port 1 and the AC port is induced by the parasitic capacitor C_{PVg1} (i.e., connecting PV at DC port 1), where the total CMV1 v_{Tcm1} can be expressed as

$$v_{Tcm1} = v_{cm1} + v_s \tag{1}$$

$$v_{cm1} = \frac{v_{AN1} + v_{BN1}}{2} = \frac{v_{AT} + v_{BT}}{2} + v_{TN1} \tag{2}$$

$$v_s = \frac{v_{dm}(L_1 - L_2)}{2(L_1 + L_2)} \tag{3}$$

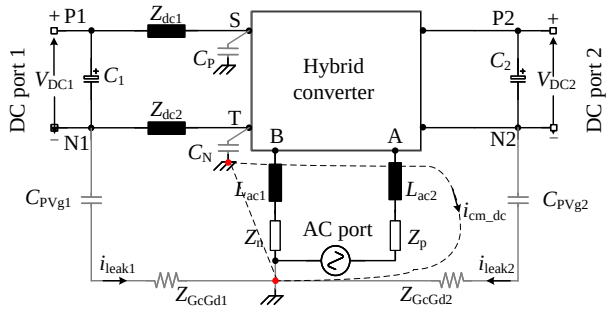

Fig. 3. CM model of the proposed hybrid converter with CM parasitics, where **P1** and **N1** are the positive and negative terminals of DC port 1, **P2** and **N2** are the positive and negative terminals of DC port 2, **S** and **T** are input terminals connected to symmetrical impedances, and **A** and **B** are output terminals connected to AC inductors. C_{PVg1}, i_{leak1} and Z_{GcGd1} are the parasitic capacitor, the leakage current and the corresponding impedance when PV panels are connected to DC port 1, while C_{PVg2}, i_{leak2} and Z_{GcGd2} are those parameters when PV panels are connected to DC port 2. Besides, C_{P} and C_{N} are the parasitic capacitors between the power devices and the ground, and $Z_{\text{p, n}}$ are the parasitic impedances of the AC bus.

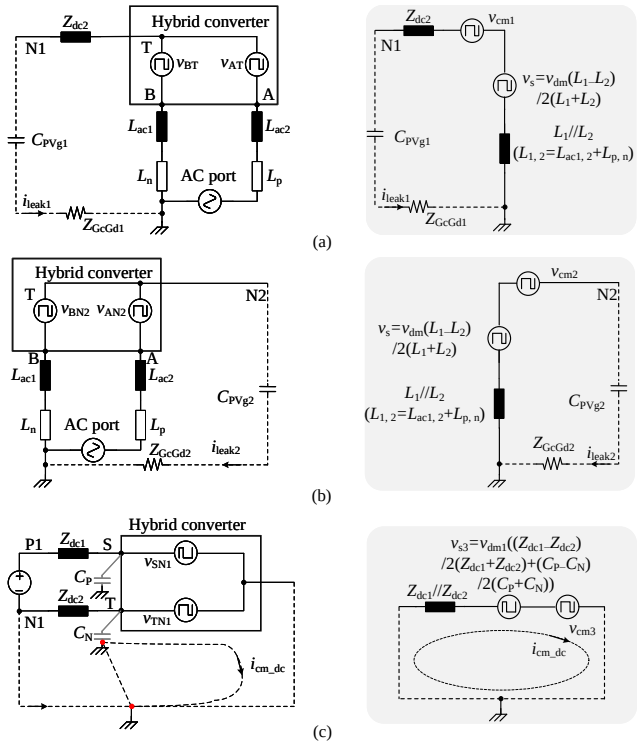

Fig. 4. CMV equivalent circuit analysis: (a) CMV1: between DC port 1 and the AC port, (b) CMV2: between DC port 2 and the AC port, (c) CMV3: between devices and DC ports (acting the DC-DC conversion).

where v_{cm1} is the CMV source generated by the hybrid converter between DC port 1 and the AC port, and v_{s} is the CMV source modeled by the AC output inductors $L_{1,\,2}$ ($L_{1,\,2} = L_{\text{ac1},\,2} + L_{\text{p, n}}$). v_{AN1}, v_{BN1} are the voltages from terminals **A** and **B** to **N1**, and v_{AT}, v_{BT} are the voltages from terminals **A** and **B** to **T** respectively. Besides, v_{dm} is the differential-mode voltage (DMV) at the AC port, which can be calculated as $v_{\text{dm}} = v_{\text{AT}} - v_{\text{BT}} = v_{\text{AB}}$.

2) **CMV2**: The leakage current loop between DC port 2 and the AC port in Fig. 4 (b) derives the total CMV2 as

$$v_{\text{Tcm2}} = v_{\text{cm2}} + v_{\text{s}} \tag{4}$$

$$v_{\text{cm2}} = \frac{v_{\text{AN2}} + v_{\text{BN2}}}{2} \tag{5}$$

where v_{cm2} is the CMV source generated by the hybrid converter between DC port 2 and the AC port, and v_{AN2}, v_{BN2} are the voltages from terminals **A** and **B** to **N2**. Notably, v_{dm} in Fig. 4 is the same when analyzing the CMVs.

3) **CMV3**: When taking the proposed hybrid converter as a DC-DC converter, the total CMV3 can be

$$v_{\text{Tcm3}} = v_{\text{cm3}} + v_{\text{s3}} \tag{6}$$

$$v_{\text{cm3}} = \frac{v_{\text{SN1}} + v_{\text{TN1}}}{2} \tag{7}$$

$$v_{\text{s3}} = \frac{v_{\text{dm1}}}{2}\left(\frac{Z_{\text{dc1}} - Z_{\text{dc2}}}{Z_{\text{dc1}} + Z_{\text{dc2}}} + \frac{C_{\text{p}} - C_{\text{n}}}{C_{\text{p}} + C_{\text{n}}}\right) \tag{8}$$

where v_{cm3} is the CMV source generated by the hybrid converter between devices and DC ports, and v_{SN1}, v_{TN1} are the voltages from terminals **S** and **T** to **N1**, v_{s3} is the CMV source considering the symmetrical impedance $Z_{\text{dc1, 2}}$ and parasitic capacitors $C_{\text{P, N}}$.

Assuming that not only the passive components but also parasitic capacitors and inductors are symmetrical, i.e., $Z_{\text{p}} = Z_{\text{n}}$, and $C_{\text{P}} = C_{\text{N}}$, the CMV sources v_{s} and v_{s3} are thus zero. In that case, those three CMV noises (i.e., CMV1, CMV2, and CMV3) can be eliminated when the proposed hybrid converter can ensure v_{cm1}, v_{cm2}, and v_{cm3} to be constant under all switching modes. According to the CM model, the operation principle and CMV analysis are elaborated in the following.

III. Operation and CMV Analysis

Since the synchronization rectifier switches $S_{\text{SR1, 2}}$ are added to provide bidirectional power flow, the deadtime should be carefully considered in the operation of the proposed hybrid converter to avoid the short-circuit at DC port 2. As shown in Table I, the switching states are detailed, where v_{AB} changes between V_{DC2} and 0 or $-V_{\text{DC2}}$ and 0 at the switching frequency during the positive half-cycle ($v_{\text{ref}} \geq 0$) and the negative half-cycle ($v_{\text{ref}} < 0$), respectively. The switching modes can be classified into two groups. One is the main modes as presented in Fig. 5, including the shoot-through (**ST**) mode, the positive voltage (**Pv**) mode, the negative voltage (**Nv**) mode, and the zero voltage (**Zv**) mode. Another one is the deadtime modes as exhibited in Fig. 6, which contains the positive deadtime modes 1 and 2 (+**Dt1** and +**Dt2**), and the negative deadtime modes 1 and 2 (−**Dt1** and −**Dt2**), and the deadtime (**Dt**) mode from **Zv** mode to **ST** mode, respectively.

According to the CM model and its equivalent circuit analysis of the proposed hybrid converter in Figs. 3 and 4, the CMVs (i.e., v_{cm1}, v_{cm2}, and v_{cm3} in Eq. (2), Eq. (5), and Eq. (7)) can be calculated in Table II, where $V_{\text{Ldc1, 2}}$ are the voltages of the boost inductors, $V_{\text{Cg1-6}}$ and $V_{\text{CSR1-2}}$ are the voltages of the junction capacitors $C_{\text{g1-6}}$ and $C_{\text{SR1-2}}$. To exemplify the leakage current suppression, the operation

TABLE I
SWITCHING STATES IN DIFFERENT OPERATION MODES.

v_{ref}	Mode	S_1	S_2	S_3	S_4	S_5	S_6	$S_{\text{SR1,SR2}}$	v_{AB}
≥ 0	**ST**	+	+	+	+	+	+	−	0
	+Dt1	+	−	−	+	−	+	−	$+V_{\text{DC2}}$
	Pv	+	−	−	+	−	+	+	$+V_{\text{DC2}}$
	+Dt2	−	−	−	−	−	+	+	0
	Zv	−	−	−	−	+	+	+	0
	Dt	−	−	−	−	+	+	−	0
< 0	**ST**	+	+	+	+	+	+	−	0
	−Dt1	−	+	+	−	+	−	−	$-V_{\text{DC2}}$
	Nv	−	+	+	−	+	−	+	$-V_{\text{DC2}}$
	−Dt2	−	−	−	−	+	−	+	0
	Zv	−	−	−	−	+	+	+	0
	Dt	−	−	−	−	+	+	−	0

* v_{AB} and v_{ref} are the inverter output pulse voltage and the reference AC voltage, and '+' and '−' are the ON and OFF states, respectively.

principles and CMV analysis are elaborated for the main modes and the deadtime modes in Figs. 5 and 6 to show the CMV clamping performance.

Main Mode

(1) **ST mode**: **ST** mode is shown in Fig. 5(a), where the HERIC is taken as a boost switch. $S_{1\text{-}6}$ are ON to charge the boost impedance $Z_{\text{dc1, 2}}$. Besides, the symmetrical synchronous rectifier switches $S_{\text{SR1, 2}}$ are OFF to avoid the short-circuit at DC port 2. C_2 supports the voltage of DC port 2 V_{DC2}. The right equivalent circuit in Fig. 5(a) shows that v_{cm1}, v_{cm2}, and v_{cm3} are equal to $V_{\text{DC1}}/2$, $V_{\text{DC2}}/2$, and $V_{\text{DC1}}/2$ according to the CMV analysis, as presented in Table II. Considering the DC-DC and DC-AC conversions during **ST** mode, the HERIC works in the freewheeling mode. Since $S_{1\text{-}6}$ are all ON, the grid current i_{AC} has three flowing paths, which has been verified in [19] that it has low conduction losses compared to the traditional HERIC. Besides, there exist bidirectional current paths to support reactive power injection.

(2) **Pv mode**: The **Pv** mode operation is demonstrated in Fig. 5(b) as well as the corresponding equivalent circuit for the CMV analysis. In **Pv** mode, $S_{1,\,4,\,6}$ are in ON state to generate the positive voltage, i.e., $v_{\text{AB}} = V_{\text{DC2}}$ and $S_{\text{SR1, 2}}$ are ON to provide a bidirectional current path for DC port 2. The symmetrical impedances release the energy to the AC port and DC port 2. As shown in the equivalent circuit in Fig. 5(b), it can be calculated in Table II that $v_{\text{cm1}} = V_{\text{DC1}}/2$, $v_{\text{cm2}} = V_{\text{DC2}}/2$, and $v_{\text{cm3}} = V_{\text{DC1}}/2$. i_{AC} can flow through $S_{1,\,4}$ when $i_{\text{AC}} > 0$, while flows through the anti-parallel diodes of $S_{1,\,4}$ when $i_{\text{AC}} < 0$, having bidirectional current flow paths.

(3) **Nv mode**: The **Nv** mode can generate a negative output voltage, i.e., $v_{\text{AB}} = V_{\text{DC2}}$. As shown in Fig. 5(c), $S_{2,\,3,\,5}$ and $S_{\text{SR1, 2}}$ are ON, where impedances also release the energy to the outputs. The equivalent circuit in Fig. 5(c) shows that $v_{\text{cm1}} = V_{\text{DC1}}/2$, $v_{\text{cm2}} = V_{\text{DC2}}/2$, and $v_{\text{cm3}} = V_{\text{DC1}}/2$ can be achieved at **Nv** mode, as presented in Table II. i_{AC} flows through $S_{2,\,3}$ when $i_{\text{AC}} < 0$, and flows through body diodes of $S_{1,\,4}$ at $i_{\text{AC}} > 0$ to achieve bidirectional current flow.

(4) **Zv mode**: Being different from **ST** mode, the symmetrical impedances are in discharging state in **Zv** mode, where the switching operation is shown in Fig. 5(d) with the ON state of $S_{5,\,6}$. Similarly, the equivalent circuit analysis

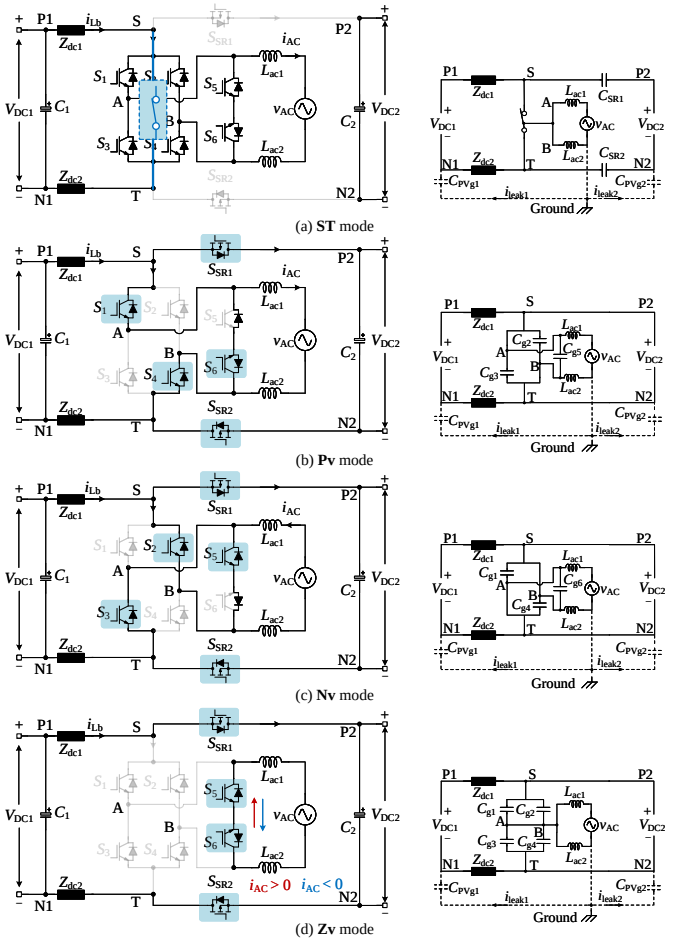

Fig. 5. Main switching modes, (a) **ST** mode: the shoot-through mode, (b) **Pv** mode: the mode of outputting positive modulation voltage at terminals **A** and **B**, (c) **Nv** mode: the mode of generating negative modulation voltage, and (d) **Zv** mode: the freewheeling mode, i.e., outputting zero voltage.

in Fig. 5(d) shows that v_{cm1}, v_{cm2}, and v_{cm3} can also stay constant at $V_{\text{DC1}}/2$, $V_{\text{DC2}}/2$, and $V_{\text{DC1}}/2$ since $V_{\text{Cg3}} - V_{\text{Zdc2}} = V_{\text{Cg4}} - V_{\text{Zdc2}} = V_{\text{DC1}}/2$ and $V_{\text{Cg3}} = V_{\text{Cg4}} = V_{\text{DC2}}/2$ under the symmetrical structure. The bidirectional current paths can be achieved in **Zv** mode, where the DC-AC conversion is in the freewheeling mode as it is the same as **ST** mode.

Deadtime Mode

(1) **+Dt1 mode**: As shown in Fig. 6(a), **+Dt1** mode is a deadtime between **ST** and **Pv** modes, where $S_{1,\,4,\,6}$ are in ON state, and $v_{\text{AB}} = V_{\text{DC1}} + 2V_{\text{Zdc1}} = V_{\text{DC2}}$. According to the right equivalent circuit in Fig. 6(a), the CMVs v_{cm1}, v_{cm2} and v_{cm3} are $V_{\text{DC1}}/2$, $V_{\text{DC2}}/2$, and $V_{\text{DC1}}/2$, respectively, as presented in Table II. When v_{ST} is higher than V_{DC2}, the body diodes of $S_{\text{SR1, 2}}$ are in forward conduction. In that case, $v_{\text{ST}} = V_{\text{DC1}} + 2V_{\text{Zdc1}}$ is clamped to be V_{DC2}, and $V_{\text{CSR1, 2}} = 0$. When V_{DC2} is higher than v_{ST}, the body diodes are OFF, and $V_{\text{CSR1, 2}} = (V_{\text{DC2}} - v_{\text{ST}})/2$. However, v_{cm3} is equal to V_{DC2} under both conditions, which is the same in **−Dt1** mode. Besides, there also exists bidirectional flow paths of i_{AC} like in **Pv** mode.

(2) **−Dt1 mode**: As depicted in Fig. 6(b), **−Dt1** mode is a switching state between **ST** and **Nv** modes, where $v_{\text{AB}} = -V_{\text{DC2}}$ and $S_{2,\,3,\,5}$ are in ON state. As shown in Table II, v_{cm1}, v_{cm2} and v_{cm3} maintain at $V_{\text{DC1}}/2$, $V_{\text{DC2}}/2$, and $V_{\text{DC1}}/2$ based

TABLE II
COMMON-MODE VOLTAGES UNDER DIFFERENT OPERATION MODES OF THE PROPOSED CONVERTER.

v_{ref}	Mode	v_{AN1}	v_{BN1}	v_{AN2}	v_{BN2}	v_{SN1}	v_{TN1}	v_{cm1}	v_{cm2}	v_{cm3}
	ST	V_{Zdc2}	V_{Zdc2}	V_{CSR2}	V_{CSR2}	V_{Zdc2}	V_{Zdc2}	$\frac{V_{\text{DC1}}}{2}$	$\frac{V_{\text{DC2}}}{2}$	$\frac{V_{\text{DC1}}}{2}$
	+Dt1	$V_{\text{DC1}}+V_{\text{Zdc1}}$	$-V_{\text{Zdc2}}$	$V_{\text{DC2}}-V_{\text{CSR1}}$	V_{CSR2}	$V_{\text{DC1}}+V_{\text{Zdc1}}$	$-V_{\text{Zdc2}}$	$\frac{V_{\text{DC1}}}{2}$	$\frac{V_{\text{DC2}}}{2}$	$\frac{V_{\text{DC1}}}{2}$
≥ 0	**Pv**	$V_{\text{DC1}}+V_{\text{Zdc1}}$	$-V_{\text{Zdc2}}$	V_{DC2}	0	$V_{\text{DC1}}+V_{\text{Zdc1}}$	$-V_{\text{Zdc2}}$	$\frac{V_{\text{DC1}}}{2}$	$\frac{V_{\text{DC2}}}{2}$	$\frac{V_{\text{DC1}}}{2}$
	+Dt2	$V_{\text{Cg3}}-V_{\text{Zdc2}}$	$V_{\text{Cg4}}-V_{\text{Zdc2}}$	V_{Cg3}	V_{Cg4}	$V_{\text{DC1}}+V_{\text{Zdc1}}$	$-V_{\text{Zdc2}}$	$\frac{V_{\text{DC1}}}{2}$	$\frac{V_{\text{DC2}}}{2}$	$\frac{V_{\text{DC1}}}{2}$
	Zv	$V_{\text{Cg3}}-V_{\text{Zdc2}}$	$V_{\text{Cg4}}-V_{\text{Zdc2}}$	V_{Cg3}	V_{Cg4}	$V_{\text{DC1}}+V_{\text{Zdc1}}$	$-V_{\text{Zdc2}}$	$\frac{V_{\text{DC1}}}{2}$	$\frac{V_{\text{DC2}}}{2}$	$\frac{V_{\text{DC1}}}{2}$
	Dt	$V_{\text{Cg3}}-V_{\text{Zdc2}}$	$V_{\text{Cg4}}-V_{\text{Zdc2}}$	$V_{\text{Cg3}}+V_{\text{CSR2}}$	$V_{\text{Cg4}}+V_{\text{CSR2}}$	$V_{\text{DC1}}+V_{\text{Zdc1}}$	$-V_{\text{Zdc2}}$	$\frac{V_{\text{DC1}}}{2}$	$\frac{V_{\text{DC2}}}{2}$	$\frac{V_{\text{DC1}}}{2}$
	ST	V_{Zdc2}	V_{Zdc2}	V_{CSR2}	V_{CSR2}	V_{Zdc2}	V_{Zdc2}	$\frac{V_{\text{DC1}}}{2}$	$\frac{V_{\text{DC2}}}{2}$	$\frac{V_{\text{DC1}}}{2}$
	−Dt1	$-V_{\text{Zdc2}}$	$V_{\text{DC1}}+V_{\text{Zdc1}}$	V_{CSR2}	$V_{\text{DC2}}-V_{\text{CSR1}}$	$V_{\text{DC1}}+V_{\text{Zdc1}}$	$-V_{\text{Zdc2}}$	$\frac{V_{\text{DC1}}}{2}$	$\frac{V_{\text{DC2}}}{2}$	$\frac{V_{\text{DC1}}}{2}$
< 0	**Nv**	$-V_{\text{Zdc2}}$	$V_{\text{DC1}}+V_{\text{Zdc1}}$	0	$-V_{\text{DC2}}$	$V_{\text{DC1}}+V_{\text{Zdc1}}$	$-V_{\text{Zdc2}}$	$\frac{V_{\text{DC1}}}{2}$	$\frac{V_{\text{DC2}}}{2}$	$\frac{V_{\text{DC1}}}{2}$
	−Dt2	$V_{\text{Cg3}}-V_{\text{Zdc2}}$	$V_{\text{Cg4}}-V_{\text{Zdc2}}$	V_{Cg3}	V_{Cg4}	$V_{\text{DC1}}+V_{\text{Zdc1}}$	$-V_{\text{Zdc2}}$	$\frac{V_{\text{DC1}}}{2}$	$\frac{V_{\text{DC2}}}{2}$	$\frac{V_{\text{DC1}}}{2}$
	Zv	$V_{\text{Cg3}}-V_{\text{Zdc2}}$	$V_{\text{Cg4}}-V_{\text{Zdc2}}$	V_{Cg3}	V_{Cg4}	$V_{\text{DC1}}+V_{\text{Zdc1}}$	$-V_{\text{Zdc2}}$	$\frac{V_{\text{DC1}}}{2}$	$\frac{V_{\text{DC2}}}{2}$	$\frac{V_{\text{DC1}}}{2}$
	Dt	$V_{\text{Cg3}}-V_{\text{Zdc2}}$	$V_{\text{Cg4}}-V_{\text{Zdc2}}$	$V_{\text{Cg3}}+V_{\text{CSR2}}$	$V_{\text{Cg4}}+V_{\text{CSR2}}$	$V_{\text{DC1}}+V_{\text{Zdc1}}$	$-V_{\text{Zdc2}}$	$\frac{V_{\text{DC1}}}{2}$	$\frac{V_{\text{DC2}}}{2}$	$\frac{V_{\text{DC1}}}{2}$

* $V_{\text{Zdc1}}=V_{\text{Zdc2}}$, $V_{\text{Cg1}}=V_{\text{Cg2}}=V_{\text{Cg3}}=V_{\text{Cg4}}=V_{\text{Cg5}}=V_{\text{Cg6}}$, and $V_{\text{CSR1}}=V_{\text{CSR2}}$ are assumed in all switching states for the proposed symmetrical hybrid converter in the (following) analysis.

on the CMV analysis of the equivalent circuit. Similarly, the bidirectional flow paths of i_{AC} can also be achieved as the same as that in **Nv** mode.

(3) **+Dt2 mode**: The **+Dt2** mode is a transition between **Pv** and **Zv** modes. Fig. 6(c) shows the switching state, where S_6 and $S_{\text{SR1, 2}}$ are ON. When $i_{\text{AC}} > 0$, v_{AB} is 0, while $i_{\text{AC}} < 0$, v_{AB} is V_{DC2}. The compensation method has been proposed in [26] to eliminate the distortion. Since the CMV performance in **+Dt2** mode is the same as that in the **Pv** mode when $i_{\text{AC}} < 0$, Fig. 6(c) presents the equivalent circuit when $i_{\text{AC}} > 0$. Therefore, we can get the results in Table II that $v_{\text{cm1}} = V_{\text{DC1}}/2$, $v_{\text{cm2}} = V_{\text{DC2}}/2$ and $v_{\text{cm3}} = V_{\text{DC1}}/2$.

(4) **−Dt2 mode**: Fig. 6(d) shows **−Dt2** mode, which is a switching state employed between **Nv** and **Zv** modes, where S_5 and $S_{\text{SR1, 2}}$ are in the ON state. Similarly, when $i_{\text{AC}} > 0$, v_{AB} is $-V_{\text{DC2}}$, and the CMV performance is the same as that in **Nv** mode. While $i_{\text{AC}} < 0$, it can achieve $v_{\text{AB}} = 0$, and the equivalent circuit for the CMV analysis in Fig. 6(d) depicts that v_{cm1}, v_{cm2}, and v_{cm3} can also maintain at $V_{\text{DC1}}/2$, $V_{\text{DC2}}/2$, and $V_{\text{DC1}}/2$, respectively. Notably, the bidirectional current paths can also be achieved, yet the deadtime effect on the power quality should be compensated [26].

(5) **Dt mode**: As presented in Fig. 6(e), **Dt** mode is a transition between **Zv** and **ST** modes. To avoid the short-circuit phenomenon, $S_{\text{SR1, 2}}$ are OFF, and $S_{5,\,6}$ are in the ON state, where v_{AB} is equal to 0. The CMV analysis according to the right equivalent circuit for the CMV analysis can also obtain that $v_{\text{cm1}} = V_{\text{DC1}}/2$, $v_{\text{cm2}} = V_{\text{DC2}}/2$ and $v_{\text{cm3}} = V_{\text{DC1}}/2$, as shown in Table II. Besides, the ON state of $S_{5,\,6}$ guarantees the reactive power injection of the DC-AC conversion.

Table II illustrates that v_{cm1}, v_{cm2} and v_{cm3} can maintain at the constant values under the proposed fully symmetrical structure. Therefore, it can achieve low CM noises, i.e., low leakage currents between both DC ports and the ac port and low CM noise between devices and DC ports. Furthermore, the proposed converter can enhance bidirectional current paths among those three ports, leading to a more flexible integration of different energy source systems.

IV. STEADY-STATE ANALYSIS DISCUSSION

A. Modulation Scheme

A dedicated modulation method for the proposed hybrid converter is shown in Fig. 7. Fig. 7(a) shows the modulation scheme in one grid period, where **+Dts** and **−Dts** are the deadtime periods in the positive half-cycle and negative half-cycle, respectively. Fig. 7(b) details the operation in one switching period, which agrees well with the state in Section III. As presented in Fig. 7(a), the gate signals of $S_{1\text{-}6}$ and $S_{\text{SR1, 2}}$ can be obtained by comparing the DC-DC gain D_{g} and DC-AC modulation signal m_{inv} with triangle carriers u_{tri}. D_{g} will be different when the proposed converter adopts different symmetrical impedance. As shown in Fig. 8, the typical symmetrical impedance has the symmetrical boost inductor and the Z-source impedance. Taking the Z-source impedance for example, D_{g} can be expressed as

$$D_{\text{g}} = \frac{V_{\text{DC2}}}{V_{\text{DC1}}} = \frac{1}{1-2d} \tag{9}$$

where d is the **ST** interval. Since DC-DC and DC-AC conversions must be finished in one switching cycle, the maximum of the DC-AC modulation signal should meet $|m_{\text{inv}}| \leq 1-d$. Thus, the peak of the AC output voltage V_{acpeak} should be

$$V_{\text{acpeak}} = m_{\text{invm}} V_{\text{DC2}} = (1+\frac{d}{1-2d}) V_{\text{DC1}} \tag{10}$$

where m_{invm} is the amplitude of the DC-AC modulation signal (i.e., the maximum DC-AC modulation signal). When the DC-DC and DC-AC conversions satisfy the condition in Eq. (10), the regulations of d and m_{inv} are decoupled. It should be noted that the proposed hybrid converter can act as a synchronous rectifier DC-DC converter ($D_{\text{g}} > 1$) if $m_{\text{inv}} = 0$, while it can operate as a HERIC inverter when $d = 0$. In that case, the proposed hybrid converter can achieve multi-functions.

B. Control Diagram

Fig. 8 shows the control block of the proposed hybrid converter, where the control can be separated into two parts,

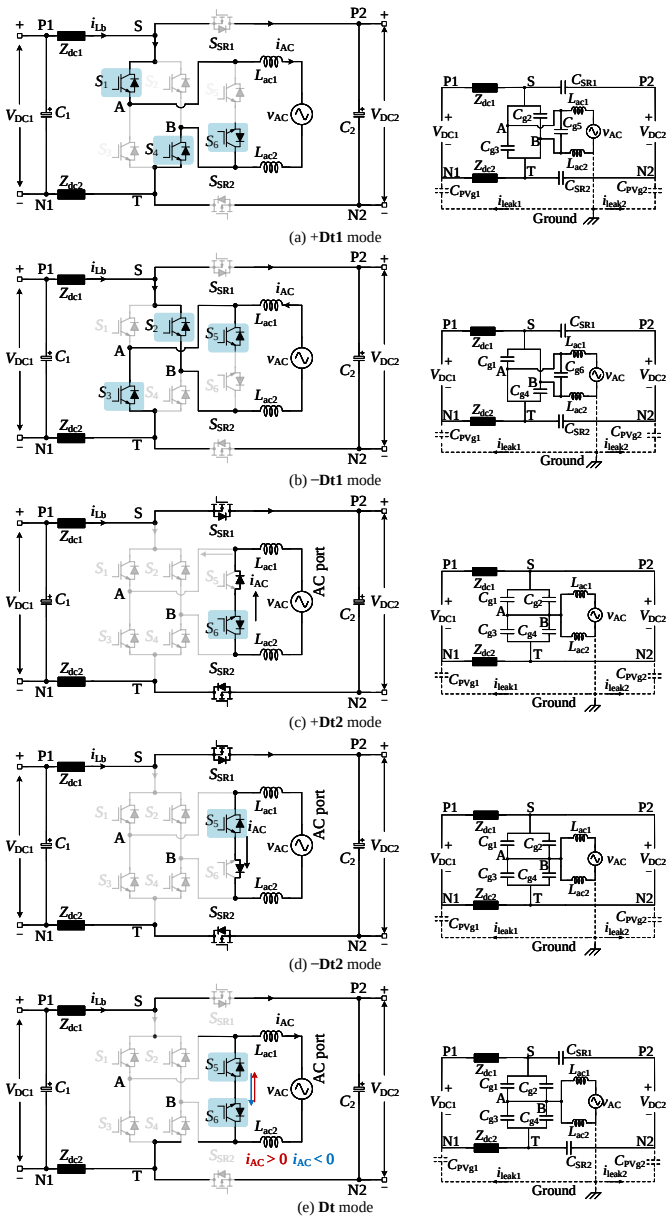

Fig. 6. Deadtime modes, (a) **+Dt1** mode: the deadtime between **ST** and **Pv** modes, (b) −**Dt1** mode: the deadtime between **ST** and **Nv** modes, (c) **+Dt2** mode: the deadtime between **Pv** and **Zv** modes, (d) −**Dt2** mode: the deadtime between **Nv** and **Zv** modes, and (e) **Dt** mode: the deadtime between **Zv** and **ST** modes.

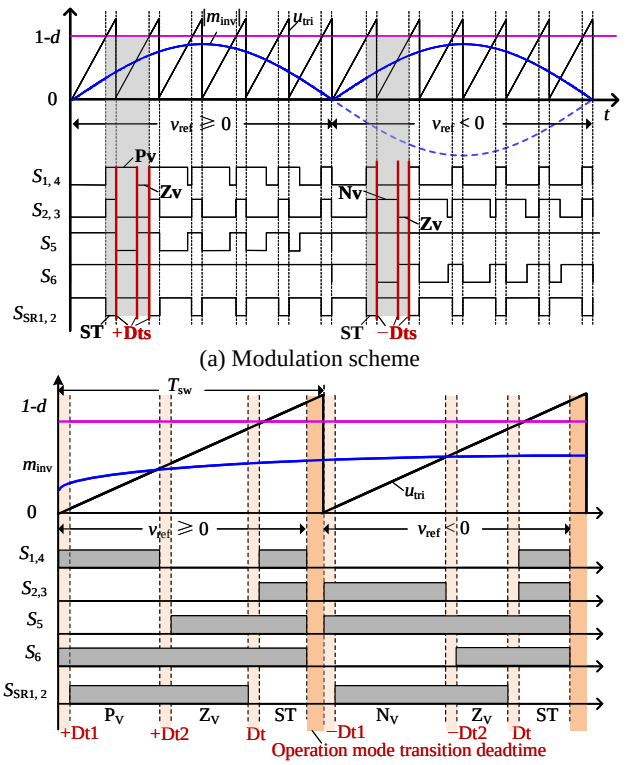

Fig. 7. Dedicated modulation scheme of the proposed hybrid converter, (a) modulation scheme and (b) detail switching principle with deadtime, where the operation mode transition deadtime means the deadtime inserted when the switching state changes from the area of $v_{\text{ref}} \geq 0$ to that of $v_{\text{ref}} < 0$.

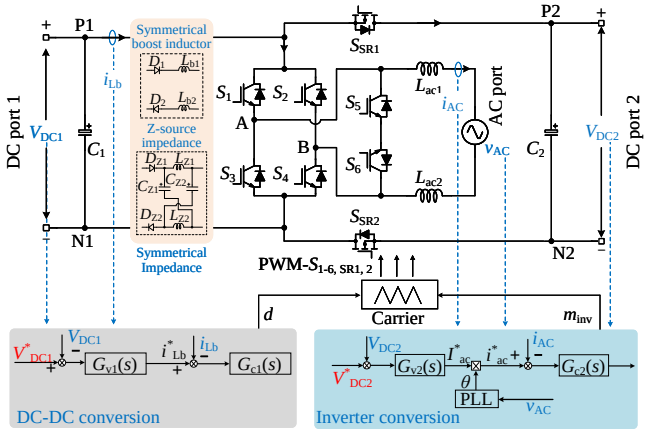

Fig. 8. General control block diagram for the proposed converter.

i.e., the DC-AC conversion control and the DC-DC conversion control. As to the DC-DC conversion, the DC port 1 voltage V_{DC1}^* is controlled, which can regulate the maximum power point tracking (MPPT) control of the PV panels. The double-loop control with two Proportional-Integral (PI) controllers (i.e., the outer voltage controller $G_{\text{v1}}(s)$ and the internal current controller $G_{\text{c1}}(s)$) are employed to generate the DC-DC duty cycle d. Regarding the DC-AC conversion, the DC port 2 voltage V_{DC2}^* has been taken as the control variable, which also adopts a double-loop controller. The AC current reference I_{ac}^* is generated through the outer voltage controller $G_{\text{v2}}(s)$ (i.e., a PI controller) and a phase-locked-loop (PLL) (i.e., synchronized with the AC voltage). Then, the internal current controller $G_{\text{c2}}(s)$ (i.e., a Proportional-Resonant (PR) controller) regulates the error of the i_{ac}^* and the feedback i_{ac} to achieve the DC-AC modulation signal m_{inv}. The control for the DC-DC and DC-AC conversions is simple, flexible and mutually independent.

C. Comparison discussion

A comparison with prior-art hybrid converters is shown in Table III, which includes characteristics of CM noise suppression, boost capability, power density, and reactive power injection. Compared with [9]–[11], the proposed converter has fewer conversion stages. Converters in [11], [13], [15] cannot suppress CM noises. The interleaved-boost one in [12]

TABLE III
COMPARISON WITH PRIOR-ART MULTIPORT CONVERTERS

Type	Ref.	CM noise suppression	boost capability	power density	reactive power injection
Parallel	[9]	++	+++	++	+++
	[10]	++	+++	++	+++
Cascaded	[11]	Non	+	+	++
Transformer	[12]	+++	+++	+	+++
Standalone	[13]	Non	++	+++	+
	[15]	Non	+++	+++	++
	[18]	+	+	+	+
	[19]	+	+	+++	+
	proposed	+++	++	+++	+++

* The more '+' means the better performance, representing the comparative level. 'Non' represents there is no such functionality.

TABLE IV
SYSTEM PARAMETERS OF THE TEST SYSTEM

Parameters	Symbol	Values
DC port 1 voltage	V_{DC1}	192 V (OCV)
DC port 2 voltage	V_{DC2}	200 V
AC grid voltage (RMS)	v_{AC}	110 V
Grid frequency	f_g	50 Hz
Boost impedance	$L_{Z1,2}$, $C_{Z1,2}$	0.2 mH, 300 μF
DC port capacitors	C_1, C_2	1000 μF
L-type AC inductors	L_{ac1}, L_{ac2}	1 mH
Switching frequency	f_s	20 kHz

adopts a transformer, reducing the power density. In all, it can be seen from Table III that the proposed fully symmetrical hybrid converter is the best when considering those four characteristics.

V. EXPERIMENTAL VALIDATION

To verify the low common-mode noise performance of the proposed converter, experimental tests are carried out on a 110 V/RMS prototype, where the hardware is shown in Fig. 9. The key parameters are shown in Table IV. To validate the different conversion gains described in Section IV. A (i.e., D_g and m_{inv}), DC port 1 voltage can be adjusted flexibly. DC port 1, DC port 2 and the AC port are connected to a PV simulator, a battery simulator and a grid simulator, respectively.

Fig. 10 shows the steady-state performance of the proposed hybrid converter, where V_{DC1} and V_{DC2} are voltages of DC port 1 and DC port 2, and v_{AC} and i_{AC} are the AC voltage and current. Fig. 10(a) shows a performance to validate simultaneous AC and DC outputs. Figs. 10(b) and (c) present steady-state results with reactive power injection, where the power factor of Fig. 10(b) is -0.7 and that of Fig. 10(c) is 0.7. In addition, the total harmonic distortions (THDs) of i_{AC} have been presented, i.e., 3.52%, 3.92%, and 3.68% in Fig. 10(a), (b), and (c), respectively. That means the proposed converter can achieve the basic requirement of the grid-connected standard in terms of flexible power control and power quality.

Fig. 11 shows the dynamic performance of the proposed hybrid converter in the experiment. There is a step change of

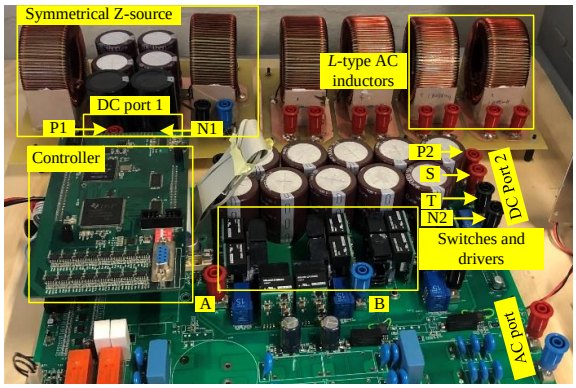

Fig. 9. Experimental prototype of the proposed hybrid converter.

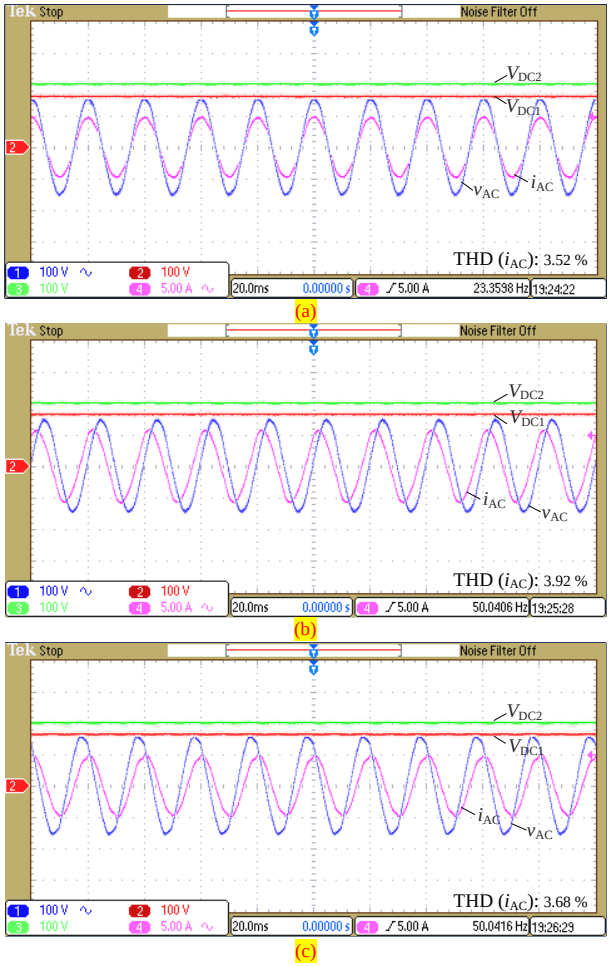

Fig. 10. Steady-state performance of the proposed fully symmetrical hybrid converter, (a) unity power factor, (b) power factor of -0.7 (i_{AC} leads v_{AC}), and (c) power factor of 0.7 (i_{AC} lags v_{AC}) (time: 20 ms/div).

V_{DC1} from 170 V to 152 V in both Figs. 11(a) and (b). The waveforms in Fig. 11(a) aim to show different boost gains, where D_g is 1.18 when V_{acpeak} (156 V) $< V_{DC1}$ (170 V), and D_g is 1.32 when V_{acpeak} (156 V) $> V_{DC1}$ (152 V). It can be seen that the proposed hybrid converter can achieve an improved boost gain compared to the limitation in literature [13] (i.e., V_{acpeak} must be lower than $> V_{DC1}$). Fig. 11(b) shows different power outputs of the PV simulator to mimic the changeable output power of the PV panel, where the grid current increases since the PV voltage V_{DC1} decreases to 152 V. That means the

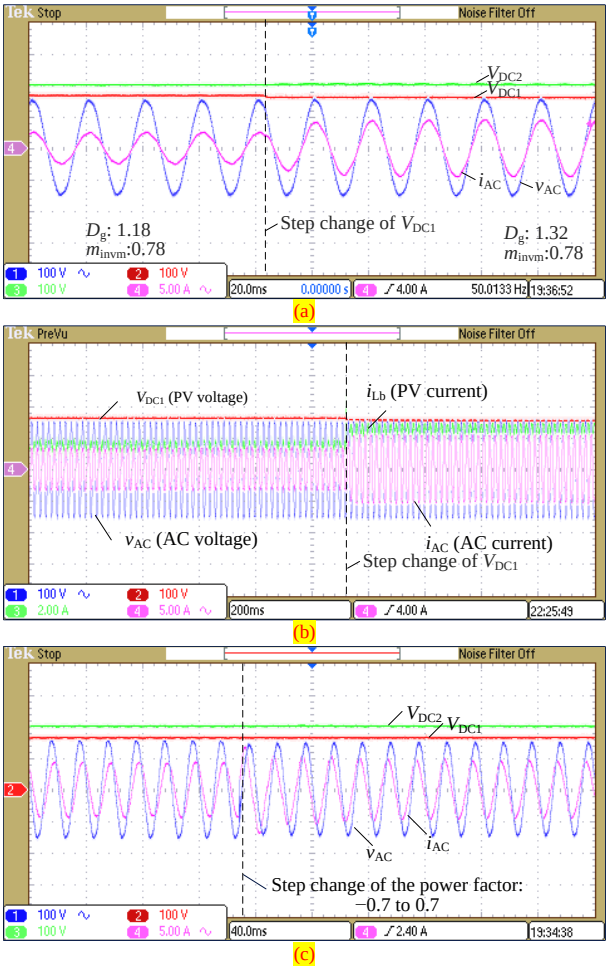

Fig. 11. Dynamic performance of the proposed fully symmetrical hybrid converter, (a) step change of V_{DC1} to show different boost gains (time: 20 ms/div), (b) step change of V_{DC1} to mimic the changeable output power of the PV panel (time: 20 ms/div), and (c) step change of the power factor from 0.7 to -0.7 (time: 40 ms/div).

control method for the proposed converter in Fig. 8 reserves the MPPT function. Besides, Fig. 11(c) shows a step change of the power factor from 0.7 to -0.7 to further verify the reactive power injection.

Comparative results of the CM performance (i.e., CMVs and CMCs) between the non-symmetrical hybrid converter and the proposed fully symmetrical one are shown in Figs. 12 and 13. When measuring CMCs, the parasitic capacitor C_p and the impedance to ground Z_{GcGd} are set as $60\ nF$ and $3.3\ \Omega$ according to the PV power [18]. The non-symmetrical converter is composed of one boost impedance, a HERIC and an SR switch, which is derived based on the concept in [13]. Thus, terminals N1, T and N2 in Fig. 2 are connected directly, which means v_{cm1} and v_{cm2}, i_{ileak1} and i_{leak2} are the same, which has been shown in Figs. 12(a) and (b) as well as v_{AN1}, v_{BN1}, v_{AC}, and i_{AC}. Besides, Figs.12(c) and (d) show the CM performance between power devices and DC ports, including waveforms of v_{SN1}, v_{TN1}, v_{cm3}, and i_{cm_dc}. The results in Figs. 12(a) and (c) show that both v_{cm1}/v_{cm2} and v_{cm3} change between $V_{DC2}/2$ and 0 at a switching frequency (i.e., detailed in the zoomed-in figure using 40 us/div). Figs. 12(b) and (d) show the measured CMCs when setting C_p and Z_{GcGd}

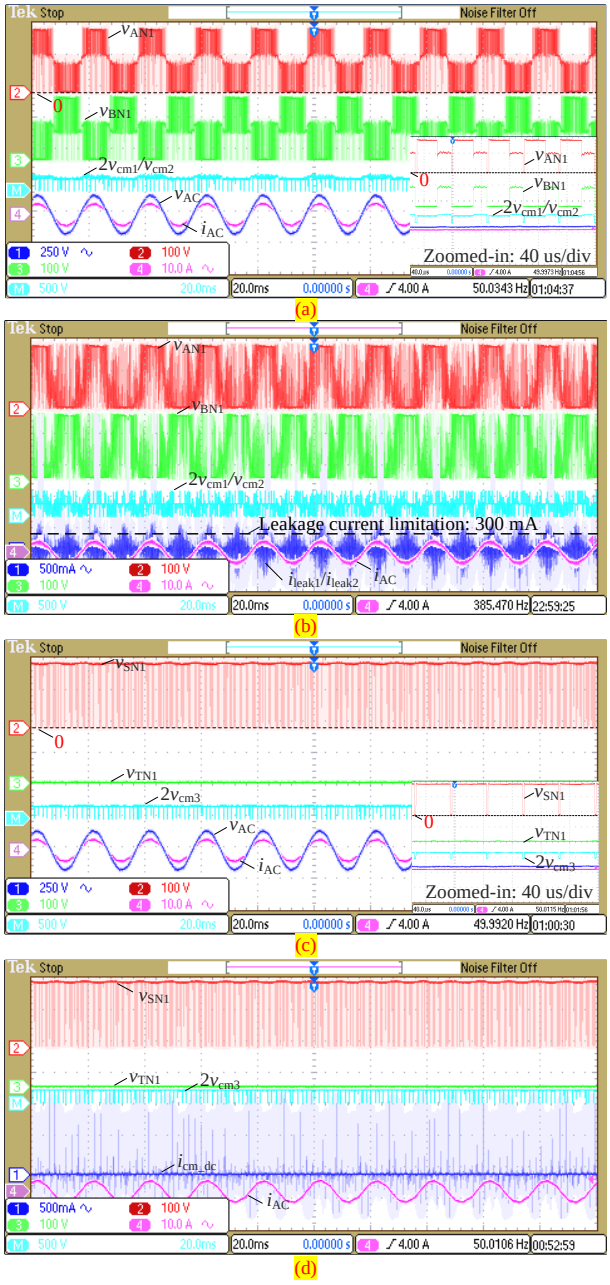

Fig. 12. CM performance of a non-symmetrical hybrid converter, (a) CMV between the DC ports and the AC port v_{cm1}/v_{cm2}, (b) CMC between the DC ports and the AC port i_{leak1}/i_{leak2} and, (c) CMV between the power devices and the DC ports v_{cm3}, and (d) CMC between the power devices and the DC ports i_{cm_dc} (time: 20 ms/div).

as Fig. 4(a) and (c), where both i_{leak1}/i_{leak2} (i.e., be higher than 300 mA) and i_{cm_dc} are serious. It should be noted that v_{cm1}/v_{cm2} is more serious when adding C_p and Z_{GcGd}, as shown in Fig. 12(b). Fig. 12 verifies that the non-symmetrical hybrid converter has no CM noise suppression capability.

Figs. 13(a), (c), and (e) show CMVs v_{cm1}, v_{cm2}, and v_{cm3}, Besides, Figs. 13(b), (d), and (f) show CMCs i_{leak1}, i_{leak2}, and i_{cm_dc}. $2v_{cm1}$ and $2v_{cm2}$ in Figs. 13(a) and (c) are the constant value of V_{DC1} and V_{DC2}, respectively, which can be further depicted in the zoomed-in figure using 40 us/div. Although there are oscillations at the waveforms of v_{AN1}, v_{BN1}, v_{AN2}, and v_{BN2}, v_{cm1} and v_{cm2} are not affected since the oscillations

Fig. 13. CM performance of the proposed hybrid converter, (a) v_{cm1}, (b) i_{leak1}, (c) v_{cm2}, (d) i_{leak2}, (e) v_{cm3}, and (f) i_{cm_dc} (time: 20 ms/div).

on the four terminal voltages are almost symmetrical and equal (neglecting differences due to inductance imbalance). Besides, i_{leak1} and i_{leak2} are very low (far below 300 mA), which are also much lower than that shown in Fig. 12(b). The constant v_{cm1}, v_{cm2} and low i_{leak1}, i_{leak2} indicate that there are low leakage currents between DC ports 1, 2 and the AC port, which means that the proposed converter can employ the PV panel in both the DC port 1 and 2 with no leakage current issue. Similarly, $2v_{cm3}$ in Fig. 13(e) is also a constant of V_{DC2}, in which the zoom-in figure (40 us/div) in the right corner also shows the detail. Further i_{cm_dc} in Fig. 13(f) is much lower than that in Fig. 12(d), and almost being zero. That means the proposed converter can achieve a low CM noise when considering it as a DC-DC converter. Although the setting of C_p and Z_{GcGd} as in Fig. 4 breaks the symmetry of the proposed converter, good performance of CM noise suppression can be achieved.

Fig. 14 shows the power loss (i.e., total losses of semiconductor devices) and the efficiency (i.e., measured from the experiment considering the losses of inductors), where P_{AC} is the output power of the AC port, and P_{DC} is the output power of DC port 2. 'P_{AC} varies, $P_{DC} = 0$' means that the proposed hybrid converter only acts as an inverter, 'P_{DC} varies, $P_{AC} = 0$' is the converter acts as a DC-DC converter, and '$P_{DC} : P_{AC} = 1 : 1$' means the proposed converter simultaneously outputs equal DC and AC power. It can be seen that the efficiency of the hybrid conversion is higher than

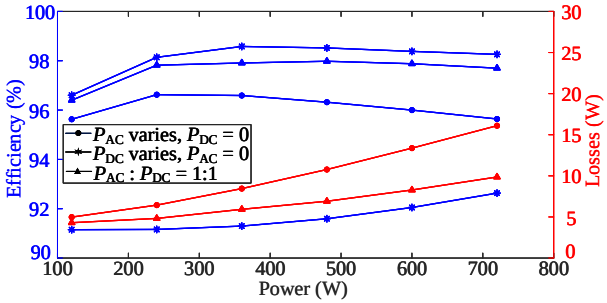

Fig. 14. Efficiency of the proposed converter and losses of semiconductor devices for different operation modes.

the average of the DC-DC and DC-AC conversion efficiency. In comparison, the above experimental results verify that the proposed converter has AC and DC outputs simultaneously, voltage boost function, and flexible power control. In addition, the proposed converter can achieve better performance in CM noise suppression than the non-symmetrical one (i.e., agreeing well with the CMV analysis in Section III). Thus, the power density can be increased due to the reduction of the EMI filter and the standalone symmetrical structure.

VI. Conclusion

This paper proposes a fully symmetrical hybrid PV converter, which can be flexibly applied as a DC-DC converter, an inverter, and a hybrid converter generating AC and DC outputs

simultaneously. Moreover, the fully symmetrical structure of the proposed converter can guarantee low CM noise for both the DC-DC and DC-AC conversions. The corresponding modulation scheme and active symmetrical switches are adopted to achieve flexible grid integration. Finally, the steady-state and comparative results are in good agreement with the analysis of the CMV noise, voltage boost and reactive power injection, validating the good performance of the proposed converter.

REFERENCES

[1] M. Shahidehpour, Z. Li, W. Gong, S. Bahramirad, and M. Lopata, "A hybrid ac-dc nanogrid: The keating hall installation at the illinois institute of technology." *IEEE Electrification Mag.*, vol. 5, no. 2, pp. 36–46, 2017.

[2] S. Dutta and K. Chatterjee, "An ac-dc hybrid nanogrid system for pv and battery storage based futuristic buildings," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 2, no. 3, pp. 314–323, 2021.

[3] K. R. Naik, B. Rajpathak, A. Mitra, and M. Kolhe, "A review of nanogrid technologies for forming reliable residential grid," in *Proc. of IEEE STPEC*, pp. 1–6, Sep. 2020.

[4] H. Wu, J. Zhang, and Y. Xing, "A family of multiport buck-boost converters based on dc-link-inductors (DLIs)," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 735–746, 2015.

[5] R. Adda, O. Ray, S. K. Mishra, and A. Joshi, "Synchronous-reference-frame-based control of switched boost inverter for standalone dc nanogrid applications," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1219–1233, 2013.

[6] A. K. Bhattacharjee, N. Kutkut, and I. Batarseh, "Review of multiport converters for solar and energy storage integration," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1431–1445, 2019.

[7] Z. Tang, Y. Yang, and F. Blaabjerg, "Power electronics: The enabling technology for renewable energy integration," *CSEE J. Power Energy Syst.*, vol. 8, no. 1, pp. 39–52, 2022.

[8] B. Zhang and S. Wang, "A survey of emi research in power electronics systems with wide-bandgap semiconductor devices," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 8, no. 1, pp. 626–643, 2020.

[9] D. Dong, I. Cvetkovic, D. Boroyevich, W. Zhang, R. Wang, and P. Mattavelli, "Grid-interface bidirectional converter for residential dc distribution systems-part one: High-density two-stage topology," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1655–1666, 2013.

[10] W. Jiang and B. Fahimi, "Multi-port power electric interface for renewable energy sources," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 347–352, 2009.

[11] Y. Pan, A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "A phase-shifting mppt to mitigate interharmonics from cascaded h-bridge pv inverters," *IEEE Trans. Ind. Appl.*, vol. 57, no. 3, pp. 3052–3063, 2021.

[12] H. Wu, P. Xu, H. Hu, Z. Zhou, and Y. Xing, "Multiport converters based on integration of full-bridge and bidirectional dc-dc topologies for renewable generation systems," *IEEE Trans. Ind. Electron.*, vol. 61, no. 2, pp. 856–869, 2014.

[13] O. Ray and S. Mishra, "Boost-derived hybrid converter with simultaneous dc and ac outputs," *IEEE Trans. Ind. Appl.*, vol. 50, no. 2, pp. 1082–1093, 2014.

[14] M. C. Mira, Z. Zhang, A. Knott, and M. A. E. Andersen, "Analysis, design, modeling, and control of an interleaved-boost full-bridge three-port converter for hybrid renewable energy systems," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1138–1155, 2017.

[15] S. S. Lee, A. S. T. Tan, D. Ishak, and R. Mohd-Mokhtar, "Single-phase simplified split-source inverter (S3I) for boost dc-ac power conversion," *IEEE Trans. Ind. Electron.*, vol. 66, no. 10, pp. 7643–7652, 2019.

[16] H. Xiao and S. Xie, "Leakage current analytical model and application in single-phase transformerless photovoltaic grid-connected inverter," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 4, pp. 902–913, 2010.

[17] DIN VDE 0126, *Automatic disconnection device between a generator and the public low-voltage grid*, German Standard Std., 2010.

[18] S. Dey, V. K. Bussa, and R. K. Singh, "Transformerless hybrid converter with ac and dc outputs and reduced leakage current," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 7, no. 2, pp. 1329–1341, 2019.

[20] Z. Tang, Y. Yang, and F. Blaabjerg, "An interlinking converter for renewable energy integration into hybrid grids," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2499–2504, 2021.

[19] Z. Tang, Y. Yang, J. Wan, and F. Blaabjerg, "Hybrid transformerless PV converters with low leakage currents: Analysis and configuration," *IET Renew. Power Gener.*, vol. 15, no. 2, pp. 368–381, Jan. 2021.

[21] IEEE Standard Committee, *IEEE standard for interconnection and interoperability of distributed energy resources with associated electric power systems interfaces*, IEEE Std 1547-2018 Std., Apr. 2018.

[22] L. Xie, X. Ruan, H. Zhu, and Y.-K. Lo, "Common-mode voltage cancellation for reducing the common-mode noise in dc-dc converters," *IEEE Trans. Ind. Electron.*, vol. 68, no. 5, pp. 3887–3897, 2021.

[23] L. Xie and X. Yuan, "Non-isolated dc-dc converters with low common-mode noise by using split-winding configuration," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 452–461, 2022.

[24] D. Cochrane, D. Chen, and D. Boroyevic, "Passive cancellation of common-mode noise in power electronic circuits," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 756–763, 2003.

[25] M. Shoyama, G. Li, and T. Ninomiya, "Balanced switching converter to reduce common-mode conducted noise," *IEEE Trans. Ind. Electron.*, vol. 50, no. 6, pp. 1095–1099, 2003.

[26] Z. Tang, Y. Yang, M. Su, T. Jiang, F. Blaabjerg, H. Dan, and X. Liang, "Modulation for the avc-heric inverter to compensate for deadtime and minimum pulsewidth limitation distortions," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2571–2584, 2020.

Zhongting Tang (S'18-M'20) received her B.S. degree in Automation Control in 2012 and Ph.D. degree in Control Science and Engineering in 2020 from Central South University, Changsha, China. During 2018 2020, she studied as a guest Ph.D. student at AAU Energy in Aalborg University, Aalborg, Denmark. Now, she is working as a postdoc here. Her research focus is on the topology and modulation technology of the grid-integrated photovoltaics converter and its application and reliability, and closed-loop impedance modeling for generic converters considering the EMI performance.

Ariya Sangwongwanich (S'15-M'19) received the M.Sc. and Ph.D. degree in energy engineering from Aalborg University, Denmark, in 2015 and 2018, respectively. Currently, he is working as an Assistant Professor at the Department of Energy Technology, Aalborg University, where he is a Vice-Leader of Photovoltaic Systems research program. His research interests include control of grid connected converter, photovoltaic systems and multilevel converters. He was a Visiting Researcher with RWTH Aachen, Aachen, Germany from September to December 2017. Dr. Sangwongwanich was the recipient of the Danish Academy of Natural Sciences0 Ph.D. Prize and the Spar Nord Foundation Research Award for his Ph.D. thesis in 2019.

Frede Blaabjerg (S'86-M'88-SM'97-F'03) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he got the PhD degree in Electrical Engineering at Aalborg University in 1995. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. From 2017 he became a Villum Investigator. He is honoris causa at University Politehnica Timisoara (UPT), Romania and Tallinn Technical University (TTU) in Estonia. His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives. He has received the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, the Villum Kann Rasmussen Research Award 2014, the Global Energy Prize in 2019 and the 2020 IEEE Edison Medal. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. In 2019-2020 he serves a President of IEEE Power Electronics Society. He is Vice-President of the Danish Academy of Technical Sciences too. He is nominated in 2014-2019 by Thomson Reuters to be between the most 250 cited researchers in Engineering in the world.