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Design and Implementation of a Single source 17-level Inverter for a Single-phase Transformerless grid-connected photovoltaic systems

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***Abstract*—Transformerless multilevel inverters based on switched capacitors are gaining importance due to the voltage boosting ability from a single input DC source and inherent capacitor voltage balancing capability. Most of the grid-connected transformerless inverters are 5-level and are commonly grounded so that their leakage current is zero. However, some major challenges like higher total standing voltage (TSV), more losses due to capacitor voltage ripples, higher charging current, and peak VA rating of the switches are comparatively higher. The motivation of the proposed work is to reduce the voltage ripple across the capacitors, minimum TSV, higher efficiency close to 98% at 1 kW, and lower cost. By using a modified sinusoidal pulse width modulation (PWM) technique for the proposed single-phase 17-level inverter, a transformerless grid-interfacing can be realized as the leakage current is (≈22mA) well within the acceptable value (<300mA) and is independent of the switching frequency. In order to validate the performance of the proposed structure, its performances are compared with the recently developed transformerless inverters. The experimental prototype of a 1 kW single-phase 17-level inverter is designed and tested for grid-connected and standalone mode, and the corresponding results are verified.**

***Index Terms*—Transformerless inverters, common-mode voltage, leakage current, reduced cost, total standing voltage, Photovoltaic system.**

I. Introduction

Multi-level inverters (MLIs) have become a core foundation of a DC to AC power conversion system in transformerless grid-connected photovoltaic (PV) applications. As the bulky line frequency transformer is removed from the PV system, it is possible to achieve a compact, lightweight grid-connected system at a much lower cost. In addition, the absence of core and ohmic losses improves the efficiency of the system. However, the flow of leakage current from the grid side to the PV panel through ground parasitic capacitances and ground resistance may violate the safety issues. According to power electronic researchers, the flow of leakage current more than a certain magnitude for a longer period can also damage the PV panels. As per the German standard DIN VDE-0126-1-1 [1], the leakage current flowing in the system must be less than 300 mA. The magnitude of leakage current is determined by the combined impedance imposed by the grid, filter circuit at the grid side, ground resistance, and parasitic capacitance (C_{pg}) across the PV panel. It is also observed the value of C_{pg} is dependent on climatic variations, the gap between cells and aluminum frame, etc.

In order to overcome the problems of leakage current in some H-bridge-based conventional transformerless inverters [2]-[5], their common-mode voltages (CMV) at the switching frequency are minimized. The H5 inverter [2] requires one extra switch attached with an H-bridge at the DC side that decoupled the input PV source from the AC grid during the freewheeling period to make the CMV minimum. Similarly, the H6 inverter [3] that connecting two extra switches with the DC voltage terminals for DC decoupling. Two more inverters based on H-bridge are H-bridge zero voltage rectifier (HB-ZVR) [4] and the Highly efficient reliable inverter concept (HERIC) [5]. These inverters used two additional switches at the grid side to decouple the input DC source to the grid side in the freewheeling mode to minimize the CMV. However, all the conventional transformerless topologies [2]-[5] reported have common problems like lack of input voltage boosting capability. Thus, an additional DC-DC boost converter is required to enhance the input DC voltage to the grid voltage level. Secondly, all the switches must withstand the entire DC-link voltage, and hence the total standing voltage (TSV) of the inverters rises. Moreover, these 2-level inverters required a heavy filter circuit to operate at a very high switching frequency and have higher switching losses.

The problems of different losses in the conventional transformerless topologies are overcome by some modified H6 topologies [6]-[7]. In addition, the soft-switching technique is adopted for high-frequency switches to minimize the switching loss. A 3-level neutral point clamped (3L-NPC) inverter [8] is used that eliminates the leakage current by connecting the midpoint of two DC link capacitors to the neutral end of the grid. However, only half of the DC link voltage is utilized at the output, and the inverter switches have a higher dv/dt stress. Another transformerless 3-level split-inductor NPC inverter is proposed in [9], where the shoot-through problem due to switching transition is minimized by a large filter inductor. Thus, a lower current total harmonic distortion and higher efficiency are observed at light loads. However, the inverter operates at higher switching (25kHz) and has large filter components make the system less efficient at rated load.

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To overcome the problems of the 3-level topologies, recently, some 5-level common ground topologies [10]-[15] with voltage boosting capability have been developed. The topology [10] uses six switches, two diodes, and three capacitors to generate five voltage levels. By using a peak current controller, the flow of both the active and reactive power is controlled. The major limitation of this topology is that one of the capacitors is charged at twice the input voltage, which increases the inverter total standing voltage (TSV) and some of the switches carry a large inrush current resulting in higher conduction loss. The 5-level PV inverter [11] has a constant total common-mode voltage and hence a smaller leakage current. However, the inverter uses additional two switches for DC decoupling. Moreover, the topology has no voltage boosting capability. The common grounded 5-level topologies [12] and [15] operate in almost the same principle in which a virtual capacitor is charged twice the magnitude of PV voltage in the positive half-cycle and discharged during the negative half-cycle. The topology proposed in [13] is an extension of the HERIC inverter structure that can boost the input voltage twice. In order to achieve a constant total common-mode voltage (TCMV) for a leakage current of 17mA, three different modulation schemes have been proposed. The topology presented in [14] is a commonly grounded generalized switched-capacitor inverter structure based on a 5-level inverter. The basic 5-level inverter uses a single DC source and two capacitors with uniform charging and discharging of capacitors over a complete cycle. However, at higher voltage levels, the numbers of charging instants are lesser than the number of discharging ones. Thus, the current drawn by the capacitors from the DC source becomes large, increasing the components' current rating. In order to limit the inrush current drawn from the source, an inductor of a small value is connected with the source.

The majority of the 5-level common-grounded topologies [12], [14], and [15] reported so far have the common problem of charging the capacitors either equal to the DC-link voltage or twice the magnitude of DC-link voltage. Moreover, the capacitors of these 5-level boost inverters usually draw a heavy inrush current during charging, increasing the inverter components' peak VA ratings. Thus, the cost and power losses of the inverter become high, making these inverter-based systems inefficient at a higher output power.

Recently, some of the high gains switched-capacitor multilevel inverters (SC-MLIs) [16], [24]-[28], [30]-[33] have been developed using minimum switching counts and shrinkage in filter size. The topology [16] does not contain an extra H-bridge for polarity reversal, and it is suitable for transformerless grid-connected PV applications. However, four input sources used in the topology increases its net cost. Moreover, a higher voltage ripple loss and conduction loss decrease its efficiency at a higher power level. The topology [24] uses a single DC source to achieve a voltage gain of 8. However, it needed seven capacitors, eighteen switches, and seven diodes to obtain seventeen levels. In addition, the polarity reversal H-bridge withstands the sum of voltages, which increases the inverter TSV as well as its cost. Also, conduction loss and voltage ripple loss are also higher. Similarly, a high gain 17-level SC-MLI is reported in [25] that is designed using a single-DC source. However, the inverter used twenty-nine switches, six diodes, and eight capacitors. Another 17-level topology [26] requires two DC sources, eighteen switches, two diodes, and six capacitors. As these topologies [25],[26] required a much higher number of components, these SC-MLIs have higher TSV, kVA rating, and cost, along with reliability issues. Moreover, due to the higher number of conducting switches and higher number of capacitors, the conduction loss, switching loss, and voltage ripple loss become significant, lowering the inverter efficiency. The topology [27] needed an extra front-end DC-DC converter at the input for charging the switched capacitors, which reduces the inrush current of the capacitors. A single source 17-level topology [28] requires ten switches, six diodes, six capacitors, has a voltage gain of 8. However, these topologies [27],[28] have higher capacitor voltage ripple loss, and higher conduction losses reduce the efficiency of the inverter at higher output power. The topology [30] requires thirteen switches, two capacitors, and two DC sources in the ratio of 1:4 to generate nineteen levels at the output. As the inverter [30] has no polarity reversal H-bridge, the inverter TSV is comparatively lower. The topology [31] needs twelve switches, six diodes, and four DC sources to produce thirteen voltage levels. It is observed that the conduction loss and the net cost of the inverter are comparatively higher. The topology [32] requires ten switches, four asymmetrical DC sources to produce seventeen levels at the output. This inverter has lower switching and conduction losses, and hence the efficiency is higher than most of the inverters reported. However, these multi-source MLIs [30]-[32] have a power mismatch problem due to the asymmetry of DC sources for a PV system under non-uniform irradiation. The single DC source 17-level topology [33] is proposed that operates under a selective harmonic elimination PWM (SHE-PWM) technique to minimize the impact of dominant harmonics. However, the inverter has twenty-six switches, seven capacitors, and two diodes, increasing costs and complexities and lowering efficiency.

Thus, from the above studies, it is observed that most of the existing transformerless grid-connected PV inverters are designed for low voltage levels (3-level/5-level). These inverters have a higher inrush current and TSV, and hence the components have a much higher VA rating. Moreover, the switches operate at a high switching frequency and have large filter components. Whereas the high-level or high gain SC-MLIs have higher voltage ripple loss due to more discharging time of the capacitors than the charging time, and hence lower efficiency. Moreover, many SC-MLIs cannot limit the leakage current within the permissible limit, making it unsuitable for transformerless grid-connected PV applications. Thus, the motivation of the proposed work is to design a multilevel inverter with a smaller leakage current, lower VA rating, smaller components, and hence lower the TSV and higher efficiency. The important features of the proposed SC-MLI are listed as:

- The proposed 17-level inverter has a better output voltage quality and harmonic even at a switching frequency ≤3kHz.
- The leakage current of the proposed 17-level SC-MLI can be restricted to a lower value by maintaining constant

TCMV using a modified sine-PWM technique so that the magnitude of leakage current is independent of the inverter switching frequency.

- The devices' peak voltage rating is less than or equal to half of the input voltage source and much lesser than the output voltage, and hence the inverter has lower TSV and cost.
- Higher charging time than discharging one and a small input rector limit the inrush current to a much lower value. Moreover, the smaller capacitor voltage ripples improve the inverter efficiency.

Thus, the proposed MLI can be suitable for industrial applications, including a transformerless grid-connected system. The proposed work is organized into nine sections. In section-II, the proposed basic 17-level inverter and its operation are explained. Section III describes the generalized model of the proposed structure. Control of the proposed inverter under grid-connected mode and its stabilities are explained in section IV. The performance analysis and comparison of the proposed structure with other MLIs have explained in section V. Section VI describes the power loss and efficiency of the proposed MLI. The design parameters of the proposed grid-tied system are elaborated in Section VII. The experimental verification is made in section VIII, and finally, the conclusions in Section IX.

II. PROPOSED BASIC 17- LEVEL INVERTER CELL AND ITS MODES OF OPERATION

A single-source basic 17-level switched-capacitor MLI (SC-MLI) with a PV source is shown in Fig. 1. The proposed inverter structure has a level generating (LG) part, voltage multiplier (VM) circuit, and a polarity reversal half-bridge, as depicted in Fig. 1. The LG part is composed of a cross-connected (CC) circuit and a switched-capacitor cell (i.e.cell-1). The cross-connected (CC) circuit is made up of two switches (S_2, S'_2), switch-diode pairs S_1-D_1 and S'_1-D'_1, and a voltage source V_{DC}. The main purpose of the CC-circuit is to charge the capacitors C_1 and C'_1 of the cell-1 at a voltage of $0.5V_{DC}$ each from the input voltage V_{DC}, by turning ON the switch-diode pairs to obtain different voltage levels in association with the other part of the inverter.

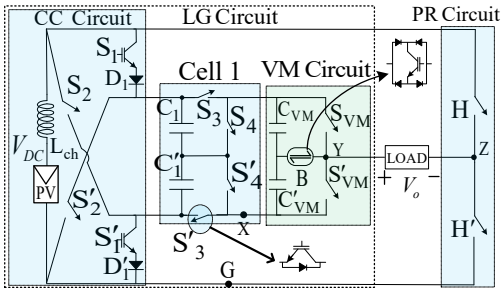


Fig. 1. Proposed 17-level SC-MLI structure containing cross-connected circuit, LG cell, and VM circuit.

By combining, the input voltage V_{DC} in the cross-connected circuit and the voltage of the capacitor's at cell-1, four positive voltage levels of magnitude 0, $0.5V_{DC}$, V_{DC}, $1.5V_{DC}$, and two negative voltage levels $-0.5V_{DC}$ and $-V_{DC}$ are obtained across the terminal X and G of Fig. 1.

Table I
The switching states (S_x) and status of the capacitors (NC=no change, C=charging, D=discharging) for the 17-level SC-MLI with input V_{DC}

S_x	Status of the 17-level SC-MLI switches (1=ON, 0=OFF)													Status of capacitors				V_o
	CC Circuit				LG Cell							PR Circuit						
	S_1	S'_1	S_2	S'_2	S_3	S'_3	S_4	S'_4	S_{VM}	S'_{VM}	B	H	H'	C_1	C'_1	C_{VM}	C'_{VM}	
1	0	0	1	0	0	0	0	1	1	0	0	0	1	NC	D	D	D	$2V_{DC}$
2	0	0	1	0	0	0	0	1	0	0	1	0	1	NC	D	NC	D	$1.75V_{DC}$
3	0	0	1	0	0	0	0	1	0	1	0	0	1	NC	D	NC	NC	$1.5V_{DC}$
4	0	0	1	0	0	1	0	0	0	0	1	0	1	NC	NC	NC	D	$1.25V_{DC}$
5	1	1	0	0	1	0	0	0	1	0	0	0	1	C	C	NC	NC	V_{DC}
6	1	1	0	0	0	0	0	1	0	0	1	0	1	C	C	NC	D	$0.75V_{DC}$
7	1	1	0	0	0	1	1	0	1	0	0	0	1	C	C	C	C	$0.5V_{DC}$
8	1	1	0	0	0	1	1	0	0	0	1	0	1	C	C	C	C	$0.25V_{DC}$
9	1	1	0	0	0	1	1	0	0	1	0	0	1	C	C	C	C	0
10	1	1	0	0	1	0	1	0	0	0	1	1	0	C	C	C	C	$-0.25V_{DC}$
11	1	1	0	0	1	0	0	1	0	1	0	1	0	C	C	C	C	$-0.5V_{DC}$
12	1	1	0	0	0	0	1	0	0	0	1	1	0	C	C	D	NC	$-0.75V_{DC}$
13	1	1	0	0	0	1	0	0	0	1	0	1	0	C	C	NC	NC	$-V_{DC}$
14	0	0	0	1	1	0	0	0	0	0	1	1	0	NC	NC	D	NC	$-1.25V_{DC}$
15	0	0	0	1	0	0	1	0	1	0	0	1	0	D	NC	NC	NC	$-1.5V_{DC}$
16	0	0	0	1	0	0	1	0	0	0	1	1	0	D	NC	D	NC	$-1.75V_{DC}$
17	0	0	0	1	0	0	1	0	0	1	0	1	0	D	NC	D	D	$-2V_{DC}$

In addition, the voltage multiplier (VM) circuit is composed of two unidirectional switches (S_{VM}, S'_{VM}), one bi-directional switch B, and a pair of capacitors (C_{VM}, C'_{VM}). The capacitors (C_{VM}, C'_{VM}) are charged by either of the capacitors C_1 or C'_1 of the cell-1 to a voltage of magnitude $0.25V_{DC}$. As a result, the VM circuit can generate three positive voltage steps like 0, $0.25V_{DC,}$ and $0.5V_{DC}$ across the terminals X and Y. Combining cell-1 and the VM circuit, the basic inverter can generate eight positive voltage levels $0.25V_{DC}$, $0.5V_{DC}$, $0.75V_{DC}$, V_{DC}, $1.25V_{DC}$, $1.5V_{DC}$, $1.75V_{DC,}$ and $2V_{DC,}$ including zero and four negative voltage levels $-0.25V_{DC}$, $-0.5V_{DC}$, $-0.75V_{DC}$ and $-V_{DC}$ across the terminals Y and G. Thus, the VM circuit multiplied the voltage levels produced by the LG cell, which is further converted to the respective negative voltage levels using the polarity reversal switches (H, H′) to obtain 17 voltage levels across the output. In order to limit the inrush current through the inverter components, an inductor of very small inductance (L_{ch}) is incorporated in series with the voltage source V_{DC}, as depicted in Fig. 1, similar to the concept given in [16]. The value of L_{ch} depends on the magnitude of V_{DC} and the allowable inrush current through the components. The detailed operations of the proposed 17-level inverter, the ON/OFF status of the switches, and the charging/discharging operation of capacitors under different states (S_x) are depicted in Table I. From Table I, it can be demonstrated that under state-1, only four switches (S_2, S'_4, $S_{VM,}$ and H′) are triggered to obtain an output voltage $2V_{DC}$. Further, the current flows through the components for the charging/discharging of the capacitors under positive states, including zero (1 to 10), as depicted in Table I are schematically represented in Fig. 2. Under state-1, the output voltage (V_o) of level zero can be obtained by turning ON the switches (S'_1-D'_1), $S'_{3,}$ $S'_{VM,}$ and H′, as shown in Fig. 2(*a*). In addition, during the zero voltage levels, the capacitor pairs (C_1, C'_1) are also charged to a voltage of $0.5V_{DC}$ by the switch-diode pair S_1-D_1 from the input source V_{DC}. Similarly, the capacitor pairs (C_{VM}, C'_{VM}) are also charged to $0.25V_{DC}$ under this state-1 by turning ON the additional switch S_4. Thus, during state-1, charging of all the capacitors can be done in addition to getting zero voltage. The direction of current through the different components is also shown in Fig. 2.

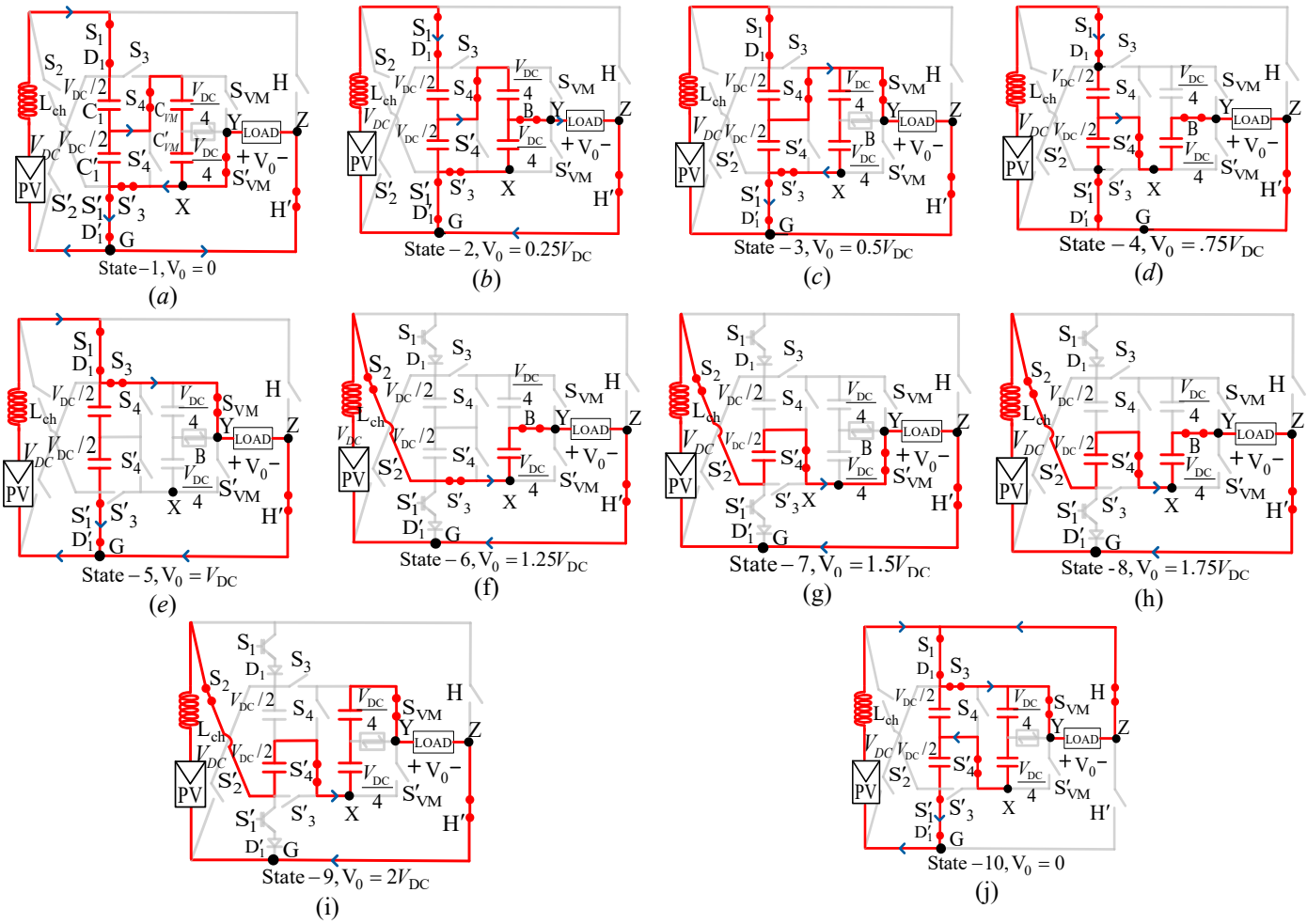


Fig. 2. Operating states for the positive voltage level generation of the proposed 17-level inverter.

In state-2, the V_o is $0.25V_{DC}$ by turning ON the switches (S′$_1$-D′$_1$), S′$_3$, B, and H, such that the voltage across the capacitor C′$_{VM}$ reflects at the inverter output terminal, as shown in Fig. 2(*b*). Similarly, the rest of the operating states, including negative voltage level generation, are self-explanatory from Fig. 2.

III. MODEL EXTENSION

The Generalized structure of the proposed inverter topology having '*m*' numbers of cells in cascaded is shown in Fig. 3. The m^{th} cell in the level generating (LG) circuit is designed with four unidirectional switches S_{2m+1}, S_{2m+2}, S'_{2m+1}, and S'_{2m+2} connected with two capacitors C_m and C'_m having voltages V_{cm} and V'_{cm}. In the proposed inverter, the voltage source V_{DC} is used to charge the capacitors C_1 and C'_1 of cell-1 with a voltage $0.5V_{DC}$ (i.e., $V_{c1}= V'_{c2}= 0.5V_{DC}$) by turning-ON the switch-diode pairs. The voltages V_{c1} and V'_{c2} are further used to charge the successive capacitors (i.e. C_2 and C'_2 of cell-2) with a voltage magnitude of $(0.5)^2V_{DC}$ by turning-ON either the switches S_4 and S'_3 or S_3 and S'_4. In this manner, the voltage of the capacitors of m^{th} cell (C_m or C'_m) is maintained equal (i.e. $V_{cm}= V'_{cm}= 0.5^mV_{DC}$) by turning ON the switches S_{2m} and S'_{2m-1} or S_{2m-1} and S'_{2m} of the $(m-1)^{th}$ cell.

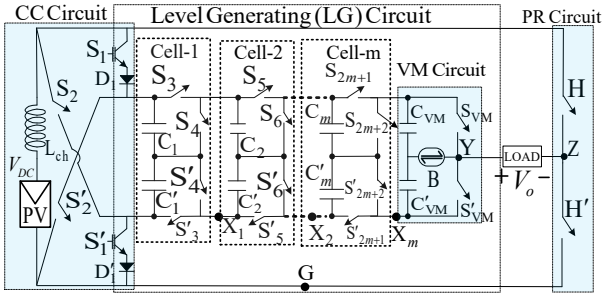


Fig. 3. Generalized structure of the proposed inverter topology having *m* numbers of cells.

Further, the capacitors of the VM circuit (C_{VM} or C'_{VM}) are charged to the step voltage of the inverter (V_{DC}) using either of the capacitor voltages V_{Cm} or $V_{C'm}$ of the m^{th} cell (i.e.$V_{VM}= V'_{VM} = 0.5^{m+1}V_{DC}= V_{DC}$) by turning ON either of the switches S_{2m+2} and S'_{2m+1} or S_{2m+1} and S'_{2m+2} of the m^{th} cell. Thus the capacitor voltages are balanced with the help of switching states, modified PWM technique, and closed-loop current control technique, as discussed in the next section (Section-IV). For the balanced capacitor voltages present in the inverter having *m* number of cells with a voltage ratio of 1:0.5:….0.5^m, the LG part of the proposed generalized inverter generates the voltage levels like 0, $\pm0.5^{m+1}V_{DC}$, $\pm0.5^mV_{DC}$, ….., $\pm0.25V_{DC}$, $\pm0.5V_{DC}$, $\pm V_{DC}$ in associate with the polarity reversal half-bridge. The

numbers of switches (N_{sw}), gate driver circuits (N_{Driver}), and capacitors (N_C) required by the generalized structure of the inverter having m number switched-capacitor (SC) cells are calculated as:

$$N_{sw} = 4m+9 \quad (1)$$

$$N_{Driver} = 4m+8 \quad (2)$$

$$N_C = 2m+2 \quad (3)$$

The number of output voltage levels (N_L) and the peak outputvoltage of the inverter, $V_{0,\,max}$ are calculated for a given V_{DC} as:

$$N_L = 2^{m+3} + 1 \quad (4)$$

$$V_{o,\,max} = 2^m V_{DC} \quad (5)$$

The generalized expression of the total standing voltage (TSV) of the proposed inverter is calculated as:

$$TSV = (2^{m+3} - 2^{2m} - 0.75)V_{DC} \quad (6)$$

For m=1, the number of voltage levels (N_L) of the proposed MLI becomes 17, and the corresponding output voltage ($V_{o,max}$) and the value of TSV are calculated as $2V_{DC}$ and $11.25V_{DC}$, respectively, for a given input voltage V_{DC} as observed from (4)-(6). For a given output voltage ($V_{o,max}$), the value of only input voltage V_{DC} can be calculated. For the proposed SC-MLI, the magnitude of voltages across the capacitors of the j^{th} cell is calculated as:

$$V_{Cj} = (0.5)^j V_{DC} j = 1, 2, 3, \ldots m \quad (7)$$

The value of the voltages across the capacitors can be maintained by charging/discharging the capacitors equally using a PWM switching technique, as discussed in the next section.

IV. CONTROL OF TRANSFORMERLESS GRID-CONNECTED PV SYSTEM

A control technique using a d-q current controller for the proposed multilevel inverter-based grid-tied PV system is developed here in order to make the grid-current maximum sinusoidal pattern and synchronized with the grid voltage. Several current control techniques are developed for single-phase grid-connected inverters [23] like model predictive control (MPC), proportional-resonant (PR) current control, energy balance controller and proportional-integral (PI) control using d-q current control [16], etc. The conventional PI-based current controllers are very simple to implement for the grid-connected system. However, the PI controller is much more effective for controlling DC components, which eliminates the DC errors, is more accurate, and has higher bandwidth. Fig. 4 represents a single-phase 17-level inverter connected to the transformerless grid-connected PV system. Here, the grid Voltage V_g is used as V_m sinωt and the current I_g is I_m sinωt, which are first transformed into stationary α-β coordinate axis components (V_α, V_β) and (I_α, I_β), respectively, using 90^0 phase shifter block. These α-β components are further converted to the corresponding DC quantities like (V_d, V_q) and (I_d, I_q) using a d-q transformation. The parameter ωt is used for coordinate transformation between the α-β and d-q components, obtained using a delay-based phase-locked-loop (PLL) technique by setting reference at V^*_q =0 such that V_d is aligned with the d-axis. Once V_d is aligned with the d-axis, the current references I_{dref} and I_{qref} are calculated. The value of I_{qref} is set to zero to transfer active power to the grid, and the current phasor I_d will be in line with the voltage space vector V_d of the rotating d-q-axis frame. The value of I_{dref} is the current at the maximum power point obtained from the maximum power point tracker (MPPT). For proper functioning of MPPT, the perturb and observe (P & O) control algorithm is used.

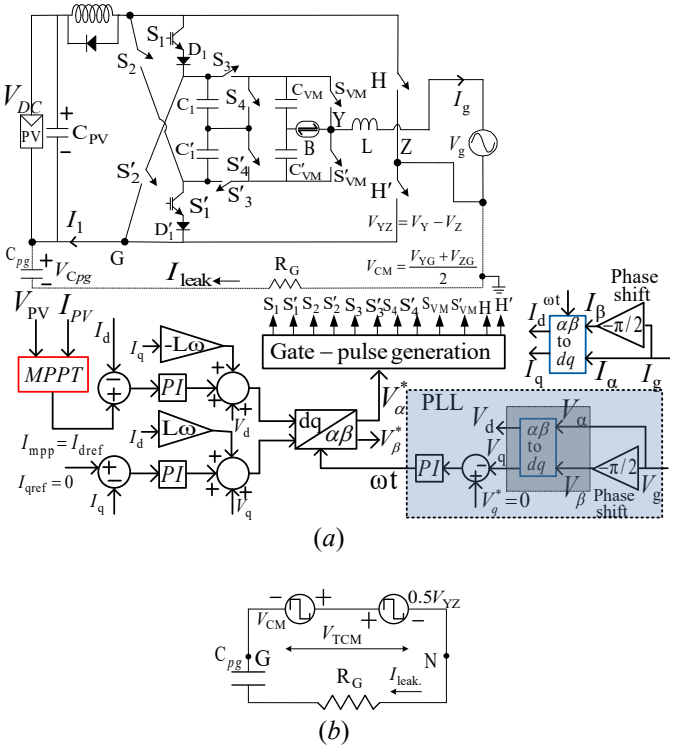


Fig. 4. Current control of single-phase transformerless grid-connected PV model (*a*) Proposed 17-level inverter structure, (*b*) equivalent circuit model of the 17-level inverter depicting net common-mode voltage (V_{TCM}), stray capacitance C_{pg} and ground resistance R_G for the flow of leakage current.

A. ANALYSIS OF TOTAL COMMON-MODE VOLTAGE (TCMV) AND LEAKAGE CURRENT

The transformer plays a major role in arresting the leakage current (I_{leak}) flowing from the grid side to the PV panel produced by the varying common-mode voltage across the inverter terminals [17]-[18]. The flow of I_{leak} is very harmful to a transformerless PV system as it can damage the insulation of the PV panels, reduce efficiency, and raises electromagnetic interference concerns. In a transformerless PV system, the flow of leakage current is limited by the stray capacitance C_{pg} and the ground resistance R_G of PV panel and the ground. Therefore, the transformerless MLIs faced significant challenges in restricting the flowing of leakage current (I_{leak}) below a certain acceptable value (i.e. 300mA according to the German standard DIN VDE 0126-1-1) that reduces the life-span the PV panels. It is also observed that the main cause of leakage current flowing through the PV panel and ground is due to the varying common-mode voltage (V_{CM}) developed across inverter output terminals and the differential voltage (V_{YZ}) [17]-[18].

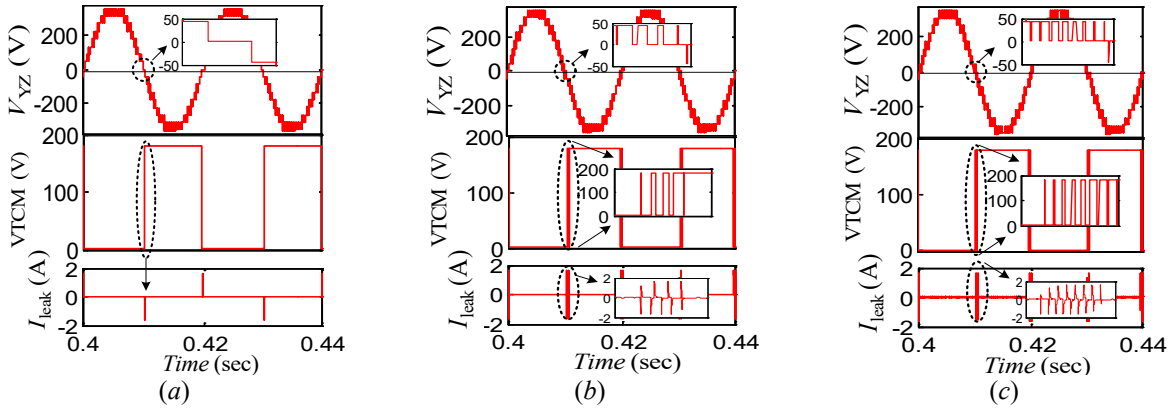


Fig. 6. Simulation results of output voltage, total common mode voltage and leakage current using (*a*) modified SPWM technique at f_{sw}=3kHz, (*b*) conventional SPWM technique at f_{sw}=3kHz and (*c*) conventionalSPWM technique at f_{sw}=10kHz.

The equations for the V_{CM} and V_{YZ} are calculated as:

$$V_{CM} = \frac{V_{YG} + V_{ZG}}{2} \tag{8}$$

$$V_{YZ} = V_{YG} - V_{ZG} \tag{9}$$

Where V_{YG} and V_{ZG} are the node voltages measured across the basic 17-level inverter structure. Using equations (8) and (9), the total common-mode voltage (V_{TCM}) developed across the stray capacitance (C_{pg}), and the ground resistance (R_G) is due to the combination of V_{CM} and -0.5V_{YZ} as mentioned in [18]. Therefore, the value of V_{TCM} across the terminals Z and G is calculated as:

$$V_{TCM} = V_{ZG} = V_{CM} - \frac{1}{2}V_{YZ} \tag{10}$$

The flow of I_{leak} through the stray capacitance (C_{pg}) and the ground resistance (R_G) due to the presence of V_{TCM} is schematically explained in Fig. 4(*b*). Using KVL, the value of I_{leak} through C_{pg} and R_G is measured as:

$$I_{leak} = V_{TCM} \Big/ \left(R_G + \frac{1}{sC_{pg}} \right) \tag{11}$$

From equations (10) and (11) it can be concluded that for a constant value of V_{TCM}, the value of I_{leak} becomes zero. This can only happen due to the presence of C_{pg}, which is charged at a constant value of V_{TCM}. For a sudden transition of V_{TCM}, the current I_{leak} starts flowing through the circuit. Using equations (8)-(10) and the equivalent circuit model of the proposed 17-level inverter in Fig. 4(*b*), the value of total common-mode voltage (V_{TCM}) across the inverter output terminal for some of the output voltage levels are calculated as depicted in Table II. Table II shows that during step change in output voltage from -0.25V_{DC} to 0 and vice versa, there is a transition in V_{TCM} between 0 and V_{DC}. However, for the remaining output voltage steps, the value of V_{TCM} maintains constant magnitude either at 0 or V_{DC}, respectively. Due to the presence of parasitic capacitances, C_{pg} in the PV system as depicted in Fig. 4, any transition in voltage during interval 0, π, 2π, …, nπ would cause instantaneous flow of I_{leak} during that instant of time. The current I_{leak} decays to zero as soon as the stray capacitance has charged to voltage V_{TCM}.

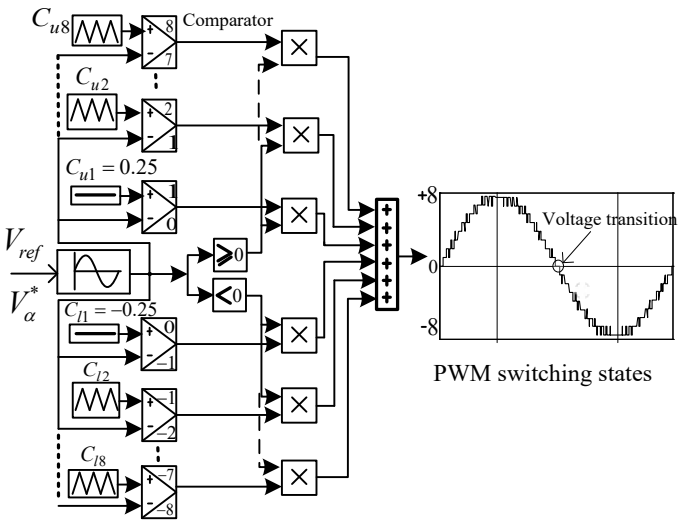


Fig. 5. Modified SPWM generation control block.

A modified sinusoidal pulse width modulation (SPWM) technique similar to the concept given in [19] is used to control the gate pulse of the switches for the proposed 17-level inverter, as depicted in Fig. 5. In order to generate the switching pulses of the proposed 17-level inverter, eight carrier signals towards

Table II
Analysis of total common mode voltage (TCMV) for some of the voltage levels of the proposed 17-level inverter using modified SPWM technique.

$V_{O/P}$	$2V_{DC}$	$1.75V_{DC}$	$1.25V_{DC}$	$0.75V_{DC}$	$0.5V_{DC}$	$0.25V_{DC}$	0	$-0.25V_{DC}$	$-0.5V_{DC}$	$-0.75V_{DC}$	$-1.25V_{DC}$	$-1.75V_{DC}$	$-2V_{DC}$
V_{YZ}	$2V_{DC}$	$1.75V_{DC}$	$1.25V_{DC}$	$0.75V_{DC}$	$0.5V_{DC}$	$0.25V_{DC}$	0	$-0.25V_{DC}$	$-0.5V_{DC}$	$-0.75V_{DC}$	$-1.25V_{DC}$	$-1.75V_{DC}$	$-2V_{DC}$
V_{YG}	$2V_{DC}$	$1.75V_{DC}$	$1.25V_{DC}$	$0.75V_{DC}$	$0.5V_{DC}$	$0.25V_{DC}$	0	$0.75V_{DC}$	$0.5V_{DC}$	$0.25V_{DC}$	$-0.25V_{DC}$	$-0.75V_{DC}$	$-V_{DC}$
V_{ZG}	0	0	0	0	0	0	0	V_{DC}	V_{DC}	V_{DC}	V_{DC}	V_{DC}	V_{DC}
V_{CM}	V_{DC}	$0.875V_{DC}$	$0.625V_{DC}$	$0.375V_{DC}$	$0.375V_{DC}$	$0.125V_{DC}$	0	$0.75V_1$	$0.75V_1$	$0.625V_1$	$0.375V_1$	$0.25V_1$	0
V_{TCM}	0	0	0	0	0	0	0	V_{DC}	V_{DC}	V_{DC}	V_{DC}	V_{DC}	V_{DC}

the upper side (C_{u1} to C_{u8}) of the zero lines and eight lower carrier signals (C_{l1} to C_{l8}) are compared with a reference sine signal. The gate pulses of the switches that produce $+0.25V_{DC}$ and $-0.25V_{DC}$ voltage levels operating at fundamental switching can be obtained by comparing the carriers C_{u1} and C_{l1} of respective constant magnitudes equal to +0.25 and -0.25 with the reference sine signal. The switches that generate other voltage levels are operated at a much higher switching frequency, which can be obtained by comparing the high-frequency (f_{sw}=3 kHz) triangular carriers with the reference sine wave.

The advantage of the proposed PWM technique is that the waveform of V_{TCM} of the proposed 17-level inverter is independent of f_{sw} during the transition of voltage between 0 and V_{DC}. Thus, the RMS value of I_{leak} remains constant irrespective of f_{sw}

A detailed schematic comparison is made in Fig. 6(*a*)-(b), where the inverter is operated under modified and normal SPWM at f_{sw} of 3 kHz. It is observed in the waveform of V_{TCM} (given Fig. 6(*a*)) that a single transition in V_{TCM} during the change of the voltage from 0 to V_{DC} causes a lower magnitude of I_{leak} compared to the values when the inverter operates under the normal SPWM technique as shown in Fig. 6(*b*). The magnitude of I_{leak} using the conventional SPWM is about 34.22 mA at 3 kHz switching frequency. Another interesting feature observed in Fig. 6(*c*) is that the corresponding value of I_{leak} rises to 84.53 mA at f_{sw} =10 kHz due to more number of transitions of V_{TCM} when output voltage changes from $-0.25V_{DC}$ to 0 or vice versa. Therefore, increase in f_{sw} using the normal SPWM technique, the value of I_{leak} increases proportionately due to $C_{pg}\times(dV_{TCM}/dt)$. In order to overcome this major problem, an advantage of the modified SPWM technique is adopted in the proposed inverter such that the value of I_{leak} is independent of f_{sw}. Moreover, no major change is observed in output current and voltage %THD. The simulation is carried out considering parameters C_{pg} =100 nF, R_G =25 Ω, V_{DC} =180 V and V_{grid}=240 V. The RMS value of I_{leak} is obtained as 20 mA, which is much lower than the limit specified by the German standard DIN VDE 0126-1-1. It can be concluded that the proposed 17-level inverter is well applicable for single-phase transformerless grid-connected PV systems.

B. Stability Analysis of the Current Control Loop of the Grid-Connected System

Fig. 7 represents the closed-loop representation of the d-axis current control for the proposed 17-level inverter. The transfer function block associated with the current control loop is $G_d(s)$ represented for the total delay in the current control loop, including pulse width modulation delay, analog to digital conversion delay, and computational delay. C(s) represents the proportional (K_p) and integral (K_i) controller block, G(s) is the plant transfer function that includes grid resistance (R_g) and grid inductance (L_g), including the L filter. Here, K_{PWM} is the inverter gain, and T_d is the sampling time of the system considering sampling frequency to be equal to the switching frequency [20]. Also, the bandwidth is assumed as 0.1 times the sampling frequency. The open-loop gain (OLG) of the current control loop for the proposed 17-level inverter-based system is represented as:

$$OLG = \left(K_P + \frac{K_i}{s}\right)\frac{K_{PWM}}{(sL_g + R_g)}\frac{1}{(1+1.5T_d s)} \quad (12)$$

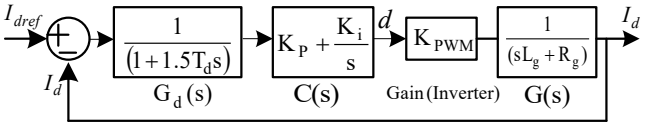


Fig. 7. d-axis closed-loop current control for the proposed 17-level inverter.

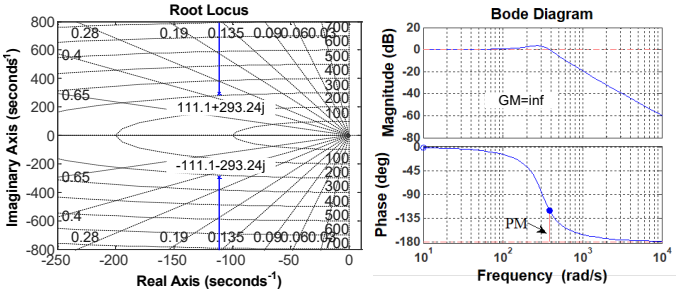


Fig. 8. Stability analysis of the d-axis current loop using (*a*) Root locus curve, (b) Bode plot.

The OLG in eq. (12) is arranged in a manner such that zero of the PI controller ($\lambda=K_i/K_p$) would cancel out the slow-moving pole of the plant (including L filter) ($\lambda=R_g/L_g$). Thus Eq.(12) is rearranged as:

$$OLG = \frac{K_{PWM}K_P}{sL_g(1+1.5T_d s)} \quad (13)$$

The closed-loop transfer function is derived from eq. (13) and Fig. 7 as:

$$\frac{I_d}{I_{dref}} = \frac{K_P K_{PWM}/1.5T_d L_g}{s^2 + s/1.5T_d + K_P K_{PWM}/1.5T_d L_g} \quad (14)$$

The eq. (14) represents the second-order transfer function having natural frequency ω_n and damping coefficient ζ, whose value is depicted in eq. (15) and eq. (16) as:

$$\omega_n = \sqrt{\frac{K_P K_{PWM}}{1.5T_d L_g}} \quad (15)$$

$$\xi = \left(\frac{1}{2\omega_n}\right)\left(\frac{1}{1.5T_d}\right) \quad (16)$$

Considering, K_{PWM}=2, L_g=0.004H, R_g=1Ω, f_{sw}=3 kHz and bandwidth=315 Hz. The values of K_p and K_i are obtained as 0.88 and 220. The closed-loop transfer function of eq. (14) is represented as:

$$\frac{I_d}{I_{dref}} = \frac{98333.33}{s^2 + 222.22s + 98333.33} \quad (17)$$

Fig. 8 describes the stability analysis of the closed-loop transfer function using equation (17). Analysis of the closed-loop transfer function is made considering the grid-connected PV

system model as depicted in Fig. 7. The stability of the closed-loop transfer function is first determined by the location of closed-loop poles present in the Root-locus plane, as shown in Fig. 8(*a*). The two complex conjugate poles obtained like λ_1=(-111.1+293.24j) and λ_2=(-111.1-293.24j) lie in the left half of the s-plane indicated that the system is stable. The system stability is further verified by drawing Bode Plot in Matlab Simulation. It is observed from the Bode plot, as given in Fig. 8(b), that both the phase margin (PM) and gain margin (GM) of the system are positive and equal to 60.14^0 and infinity, respectively. Thus, the proposed grid-controlled system is stable.

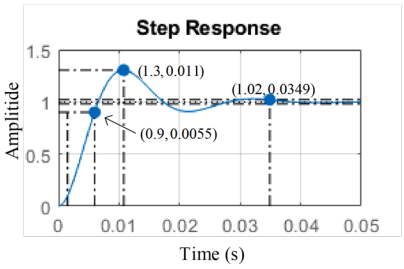


Fig. 9. Step response of the closed-loop transfer function.

Further, to find the system's speed, the step response of the transfer function is determined in the Matlab/Simulink environment, and various parameters like rise-time, peak-overshoot, and settling time are measured as shown in Fig. 9. It is observed that system stability is reached after a short transient time of 0.0349 sec.

V. PERFORMANCE COMPARISON

The key performance-related parameters like components count and their VA rating, per unit TSV, cost, efficiency, leakage current, etc., of the proposed MLI and some other similar kinds of existing MLIs, are determined and compared in this section. The performance comparison of the proposed 17-level SC-MLI with some other established inverters for transformerless grid-connected applications [10], [12]-[18], [34] is presented in Table III. Further, the performance of the proposed 17-level inverter is also compared with some other high-level SC-MLIs [16], [24]-[28], [30]-[33]. From Table III, it is observed that for a specimen 1kW output at V_o=400V, the sum of peak VA rating of switches to inverter peak output power (i.e. $\sum\left(V_{\text{sw.peak}} \times I_{\text{sw.peak}}\right)/\left(\text{P}_{\text{out}}\right)$) of the proposed 17-level inverter is 18.1, which is much better than most of the transformerless topologies [10], [12]-[16]. This is mainly due to the large inrush current drawn from the source while charging and the higher voltage stress of these 5-level MLIs. However, the topologies with unity voltage gain [18], [31]-[32], and [34] presented in Table IV have a lesser peak VA rating of the switches than the proposed one. This is due to the lesser number of capacitors [18] or no capacitors in the MLIs [31-[32]. In terms of inverter TSV to its output voltage (i.e., TSV_{PU}), the proposed 17-level SC-MLI is better than most of the transformerless topologies [10], [12]-[15], [18], and [34] presented in Table III. For grid-tied application with a 1.5 mH, the total harmonic distortion of load current (THD_I) is much better than the transformerless topologies [10], [12]-[15], [18], and [34], due to a higher number of voltage levels. Similarly, the value of cost function to N_L (i.e. $(N_{\text{sw}}+N_{\text{driver}}+N_\text{C}+N_\text{D}+\beta\times\text{TSV}_{\text{PU}})*N_{\text{DC}}/N_\text{L})$), of the proposed 17-level inverter is superior to other MLIs [16], [24]-[28], [30]-[33].

For economic viability, the number of major components and their approximate cost for all the MLIs listed in Table III and Table IV and the proposed 17-level are estimated for the same output voltage (V_o=400V) condition under unity power factor load. For cost estimation, the rating of all IGBTs and diodes (DSEI60-06A) are considered as 900V, 60A, and 600V, 60A, respectively. The unit cost of IGBT (CT60AM-18F) and fast recovery diode (DSEI60-06A) from MITSUBISHI are considered as $2.30 and $1.13, respectively, and gate driver ICs (IR2110) from Infineon Technologies is considered $2.68. The unit cost of 4700µF capacitors of voltage rating as 50V, 100V, and 200V from Vishay are considered as $4.95, $10.74 and $37.72, respectively. Similarly, the unit cost of different voltage source models N6752A (50V, 10A), N5768A (80V, 19A), N5769A (100V, 15A), N5770A (150V, 10A), N8741A (300V, 11A) and N8943A (500 V, 30 A) from Keysight are considered as $1980.26, $2140, $3599, $3575, $5646, and $8287, respectively. It is observed in Table IV that all the single source SC-MLIs [24], [25], [27], [28], and [33] with voltage gain 8 have a lower cost than the multiple source topologies [16], [26], [30]-[32], including the proposed 17-level inverter. This is due to the higher cost of voltage source of a higher rating than the high-gain SC-MLIs. However, these high gain SC-MLIs, as given in Table IV needed a line frequency transformer in the grid side, which results in an increase in both size and cost of the system compared to the proposed transformerless based 17-level SC-MLI. It is also observed that the single source grid-connected transformerless inverters [10], [12]-[15], [18] given in Table III can generate five voltage levels (boosting factor two). Although these inverters require fewer components than the proposed 17-level inverter, they are more costly. This is due to the higher VA rating of the capacitors compared to the proposed one. In addition, all the topologies except [16] (a common grounded topology) have leakage current greater than 300 mA than the proposed topology with a leakage current of 22 mA (RMS) only. Hence, the topology can be used for a transformerless grid-connected PV application. Similarly, in terms of efficiency at specified power, the single source transformerless PV inverters [10], [12]-[15], [18], and [34] given in Table III are much more efficient than single-source SC-MLIs [24], [25], [27], [28], and [33] in Table IV. This is due to the much higher number of capacitors. However, the proposed 17-level SC-MLI also has four capacitors, yet its efficiency is better than the other SC-MLIs given in Table III and Table IV. The detailed efficiency calculation is depicted in the following section.

VI. POWER LOSS ANALYSIS OF THE PROPOSED 17-LEVEL INVERTER

The total power losses in the proposed SC-MLI are divided into three parts as (*a*) switching loss, (*b*) conduction loss, and (*c*) voltage ripple loss. Each of these losses is described mathematically.

Table III

Qualitative analysis of the proposed inverter with other single source transformerless grid-connected PV inverters at V_{out}=400V, P_{Out}=1kW and f_{sw}=3 kHz with L filter (L_{filter}=1.5mH).

MLI Topology	N_L	N_{sw}	N_D	N_C	Gain	$\sum(V_{sw.peak} \times I_{sw.peak})/(P_{out})$	$TSV_{P.U}$ (=TSV/V_o)	η(%) @1kW	Cost($)	%THD_i
[10]	5	6	2	3	2	173.5	6.5	96.8	5802	2.84
[12]	5	7	0	3	2	901	6	96.3	5791	2.58
[13]	5	7	2	2	2	44.5	6	97.4	5759	1.86
[14]	5	8	0	3	2	364.5	5.5	97.8	5799	3.07
[15]	5	6	1	3	2	86.5	6	97.2	5791	2.37
[18]	5	6	2	2	1	6	6	97.65	8395	2.19
[34] (HERIC)	3	6	0	1	1	6	6	98.2	8382	2.62
Proposed	17	13	6	4	2	18.1	5.6	98.2	5748	0.61

Table IV

Comparison of the proposed 17-level inverter with recently developed other higher-level inverters for R-load at output voltage 400V (peak).

MLI Topology	N_L	N_{sw}	N_{DC}	N_C	Gain	$\sum(V_{sw.peak} \times I_{sw.peak})/(P_{out})$	C.F/N_L (β=0.5)	η(%) @ f_{sw} = 3 kHz	Total cost ($) @$V_{out}$ = 400V (peak)	Leakage current limiting capability	Transformerless interfacing capability
[16]	9	6	4	4	1	26@505.4W	13.33	91@505.4W	18559	Yes	Yes
[24]	17	18	1	7	8	25.9@550.4W	4.11	90.14 @550.4W	2112	No	No
[25]	17	29	1	7	8	40.2@523.4W	6.5	89.2 @523.4W	2166	No	No
[26]	17	18	2	6	4	35.4@516.9W	5.6	93.92 @516.9W	4082	No	No
[27]	17	26	1	7	8	36.9@506.2W	4.23	91.94 @506.2W	2145	No	No
[28]	17	10	1	6	8	27.08@517.3W	2.58	92.24 @517.3W	2143	No	No
[30]	19	13	2	2	4	56.84@502.6W	3.61	95.98 @502.6W	7709	No	No
[31]	13	12	4	0	1	4.91@511.2W	10	97.74 @511.2W	5775	No	No
[32]	17	10	4	0	1	4.4@500W	5	98.6 @500W	12800	No	No
[33]	17	26	1	7	8	100.3@500W	3.95	89.0 @500W	2146	No	No
Proposed	17	13	1	4	2	20.9@512W	2.45	96.9 @512W	5748	Yes	Yes

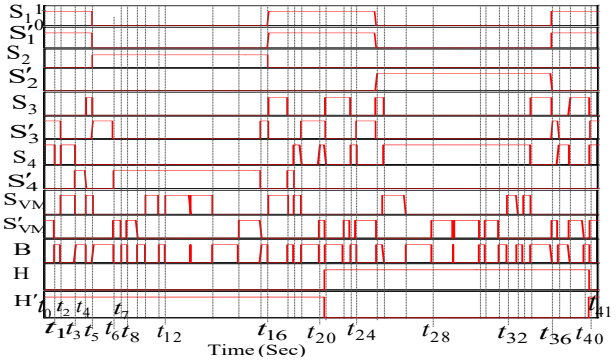


Fig. 10. Pulse pattern of the proposed 17-level SC-MLI under SPWM at a specimen 1 kHz frequency over one cycle.

(a) Switching loss: By assuming a linear overlap of the current and voltage during each switching transition, the switching loss (P_{sw}) of individual switches can be calculated. The total switching loss ($P_{SW,T}$) of the proposed basic 17-level inverter is the sum of the losses in all the unidirectional switches ($P_{swt.Uj}$), switched-diode ($P_{swt.SW\text{-}Dk}$), and the bi-directional switches ($P_{swt.B}$), can be expressed as:

$$P_{SW,T} = P_{SW,B} + \sum_{k=1}^{2}\left(P_{SW,SW-D_k}\right) + \sum_{j=1}^{10}\left(P_{SW,Uj}\right) \quad (18)$$

The loss is further derived in terms of the blocking voltages of unidirectional, switched-diode and bidirectional switches (i.e., $V_{Bl,Uj}$, $V_{Bl,SW\text{-}Dk}$ and $V_{Bl,B}$) as:

$$P_{SW,T} = \frac{I(t_{ON}+t_{OFF})}{6}\left[V_{Bl,B}f_B + \sum_{k=1}^{2}\left(V_{Bl,SW-D_k}f_{SW-D_k}\right) + \sum_{j=1}^{10}\left(V_{Bl,Uj}f_{Uj}\right)\right] \quad (19)$$

Where t_{ON}, t_{OFF}, turn-ON, and turn-OFF time of switches. Here, $f_{U,}$ $f_{SW\text{-}D,}$ and f_B are the operating frequencies of the unidirectional switches, switched-diode devices, and bidirectional switches, respectively. Fig. 10 shows the switching pulse pattern under sinusoidal PWM technique at a specimen 1kHz carrier frequency. The value of f_{Uj}, $f_{SW\text{-}D,}$ and f_B can be obtained by counting the number of switching transitions of the respective types of switches, as observed from Fig. 10. From Fig. 10, corresponding to the pulse pattern, it is observed that the operating frequency of switched-diode pairs (S_1-D_1 and S'_1-D'_1) at 1kHz switching frequency is equal to three times the fundamental frequency (i.e., $f_{SW\text{-}D}$=3f). In the same manner, the operating frequency of bidirectional switch, B, is nearly f_B=20f. The operating frequency of other unidirectional switches can

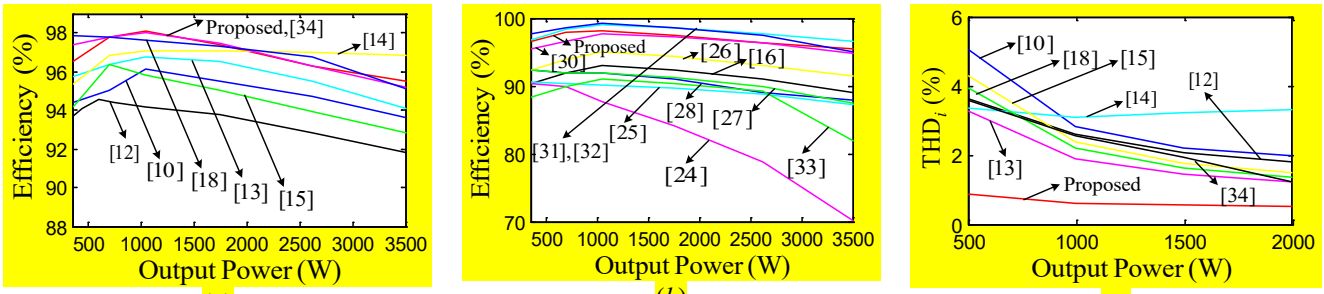


Fig. 11. Comparison of (*a*) & (b) efficiency versus output power of state-of-art transformerless 5-level and some higher level SC-MLIs and the proposed-17 level SC-MLIs, (*c*) value of THDi in the proposed and other Transformerless 5-level PV Inverters at different output power.

also be calculated from the switching pulse pattern (Fig. 10). However, the actual operating frequency of the devices at 3kHz switching frequency will be approximately equal to three times the calculated frequency. On the other hand, the blocking voltage of the switches can be calculated from the circuit analysis under different states, as described in Fig. 2. The value of the blocking voltages for the switches are equal to: $V_{bl,S1\text{-}D1}=V_{bl,S'1\text{-}D'1}=V_{DC}$, $V_{bl,S2}=V_{bl,S'2}=2V_{DC}$, $V_{bl,S3}=V_{bl,S'3}=0.5V_{DC}$, $V_{bl,S4}=V_{bl,S'4}=0.5V_{DC}$, $V_{bl,SVM}=V_{bl,S'VM}=0.5V_{DC}$, and $V_{bl,H}=V_{bl,H'}=V_{DC}$, respectively.

(b) Conduction loss:

The conduction losses of all the unidirectional and bidirectional conducting switches for an RMS load current (I) are calculated separately. The total conduction loss ($P_{Con,U}$) of a unidirectional switch ($P_{Cond,\ SW}$) is due to the conduction of either switches or the power diodes ($P_{Cond,\ D}$). The instantaneous value of conduction loss [21] for the unidirectional switch ($P_{Cond,U}(t)$) is calculated as:

$$\left.\begin{aligned} P_{Cond,U}(t)&=P_{Cond,SW}(t)=V_{sw}\times I\sin(\omega t)+R_{sw}\times I^{\beta+1}\sin^{\beta+1}(wt)\\ P_{Cond,U}(t)&=P_{Cond,D}(t)=V_d\times I\sin(\omega t)+R_d\times I^2\sin^2(wt)\end{aligned}\right\} \quad (20)$$

The proposed 17-level SC-MLI also consists of a pair of switched-diode devices, and hence the conduction loss of each device ($P_{Cond,\ SW\text{-}D}$) is derived as:

$$P_{Cond,SW-D}(t)=(V_{sw}+V_d)I\sin(\omega t)+r_dI^2\sin^2(wt)+R_{sw}I^{\beta+1}\sin^{\beta+1}(wt) \quad (21)$$

Similarly, during the conduction of the bidirectional switch, two diodes are conducted along with one switch. If the conduction loss of each switch is $P_{Cond,\ SW}$ and power diode is $P_{Cond,\ D}$[21], the instantaneous value of conduction loss for the bidirectional switch ($P_{Cond,\ B}(t)$) is calculated as:

$$P_{Cond,B}(t)=(V_{sw}+2V_d)I\sin(\omega t)+2r_dI^2\sin^2(wt)+R_{sw}I^{\beta+1}\sin^{\beta+1}(wt) \quad (22)$$

Here, V_{sw} and V_d are the on-state voltage drop of switches (here IGBT), and the diodes, $R_{sw,}$ and r_d are their equivalent resistances, and β is the current gain of the IGBT. Therefore, the conduction loss (P_{Cond}) of the proposed SC-MLI that has *x(t)* unidirectional switches (or diode), *y(t)* bidirectional switches, and *z*(t) switched-diode conducting at a time can be expressed as:

$$P_{Cond}(t)=\left[x(t)P_{Cond,U}(t)+y(t)P_{Cond,B}(t)+z(t)P_{Cond,SW-D}(t)\right] \quad (23)$$

The value of *x(t)*, y(t), and *z(t)* at any time is not fixed, as observed in the pulse pattern waveform given in Fig. 10. It is observed from Fig. 10 that during t_0 to t_1, three unidirectional switches and two switched-diode devices are conducting, and hence during this period, the conduction loss becomes equal to ($3P_{Cond,U}(t)+2P_{Cond,SW\text{-}D}(t)$), as reflected in (24). Similarly, the value of conduction loss can be calculated for all the durations in one fundamental cycle. Thus, the average conduction loss (P_{COND}) of the proposed 17-level SC-MLI over the cycle is calculated as:

$$P_{COND}=\frac{1}{T}\left[\begin{aligned}&\int_{t_0}^{t_1}\left(3P_{Cond,U}(t)+2P_{Cond,SW\text{-}D}(t)\right)dt+\int_{t_1}^{t_2}\left(P_{Cond,U}(t)+P_{Cond,B}(t)+2P_{Cond,SW\text{-}D}(t)\right)dt+\\&\int_{t_2}^{t_3}\left(2P_{Cond,U}(t)+2P_{Cond,SW\text{-}D}(t)\right)dt+\int_{t_3}^{t_4}\left(P_{Cond,U}(t)+P_{Cond,B}(t)+2P_{Cond,SW-D}(t)\right)dt+\\&\int_{t_4}^{t_5}\left(2P_{Cond,U}(t)+2P_{Cond,SW-D}(t)\right)dt+\int_{t_5}^{t_6}\left(2P_{Cond,U}(t)+P_{Cond,B}(t)\right)dt+\int_{t_6}^{t_7}\left(4P_{Cond,U}(t)\right)dt+\\&\int_{t_7}^{t_8}\left(3P_{Cond,U}(t)+P_{Cond,B}(t)\right)dt+\ldots\ldots\ldots\ldots\ldots\ldots+\int_{t_{40}}^{t_{41}}\left(4P_{Cond,U}(t)+2P_{Cond,SW-D}(t)\right)dt\end{aligned}\right] \quad (24)$$

In order to verify the conduction loss, the equivalent circuit diagram of the proposed 17-level inverter under different operating conditions is presented in Fig. 12. The equivalent series resistance (ESR) of all the capacitors is considered as r_c. The on-state voltage drops of an IGBT switch and its resistance are V_{sw} and R_{sw}, respectively. Similarly, for the fast recovery diode, the corresponding values are V_d and $r_{d,}$ respectively. The magnitude of voltages across the capacitors (C_1 and C'_1) are assumed as $v_{c1,}$ and for capacitors (C_{VM} and C'_{VM}) are v_{cvm} with respective charging currents are i_{c1} and i_{cvm}. For a load current (i_L) through the load resistance R_L, the equivalent circuit diagrams under some selected switching states are presented in Fig. 12. For an inverter switching frequency of 3 kHz under the SPWM technique [21], with an input voltage of 200V, the different power losses (conduction loss, switching loss, and voltage ripple loss) can also be calculated based on the equivalent model given in Fig. 12.

(c) Voltage ripple loss: While solving the voltage ripple loss across the capacitors, the most important analysis is to find out the voltage ripple (ΔV_{Ci}) using the charging current ($i_{Ch,i}$) flowing through the i^{th} capacitor [28]. It is obtained as:

$$\Delta V_{Ci} = \frac{1}{C_i}\int_{t_j}^{t_{j+1}} i_{Ch,i}\,dt \tag{25}$$

Where time t_j to t_{j+1} is the time during which the i^{th} capacitor is discharging in a particular voltage state. Considering F_{ref} as the power frequency, the power loss occurred due to the voltage ripple across the capacitors in a particular voltage state is given as:

$$P_{ripple,loss} = \frac{F_{ref}}{2}\sum_{i=1}^{n} C_i(\Delta V_{Ci})^2 \tag{26}$$

Knowing the value of output power (P_o), Total switching loss ($P_{SW,\,T}$), average conduction loss ($P_{Cond,loss}$), and total voltage ripple loss ($P_{ripple,loss}$) over one cycle, one can easily determine the power efficiency of the proposed SC-MLI as:

$$\text{Power efficiency} = \frac{P_o}{P_o + P_{SW,T} + P_{COND} + P_{ripple,loss}} \tag{27}$$

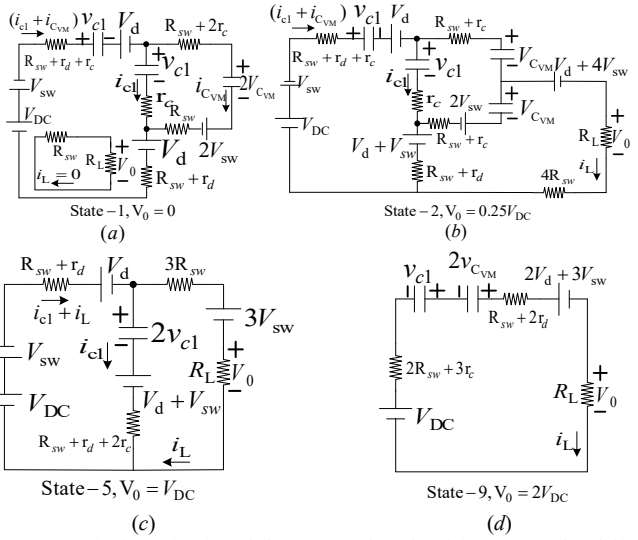


Fig. 12. Equivalent circuits of the proposed 17-level inverter under different operating states.

Thus, using the parameters given in Table V, and based on (20)-(26), different losses [21], [28], of the proposed 17-level SC-MLI are calculated for R-load at 3 kHz switching frequency. The values of switching loss, conduction loss, and voltage ripple loss at an output power of 512W are calculated as 0.036 W, 11.62 W, and 4.6 W, respectively. The corresponding efficiency of the proposed inverter is calculated as 96.9 %.

Moreover, the calculated efficiency of the proposed 17-level and other state-of-art transformerless 5-level PV inverters (given in Table III) and some higher-level SC-MLIs (given in Table IV) are presented graphically in Fig. 11 (a)-(b), for a wide range of output power (350 W to 3500 W). It is observed that the proposed inverter has better efficiency than most of the other MLIs reported here. This is due to a comparatively lower amount of conduction and voltage ripple losses of the proposed SC-MLI. Fig. 11 (c) depicts the value of current THD_i of the proposed-17 level and the existing transformerless 5-level PV inverters at different output power. It is observed that, as the proposed MLI has higher number voltage levels, the output current has much lesser harmonics.

For PV inverters, it is observed that the maximum efficiency is obtained during the peak demand of the loading. Generally, the maximum efficiency is not always helpful to the users because the PV inverters operate normally at 20-30% of the inverter rated power. Thus, for satisfactory performance measurement, weighted efficiency like CEC efficiency, as recommended by the California Energy Commission (CEC) [29], can be used. The CEC efficiency is calculated as a mean value of inverter efficiency at six different power outputs ranging from 10% to 100% of the rated power and the corresponding weighted factors (α_i), as indicated in Table V. The CEC efficiency can be expressed as:

$$\eta_{CEC} = \sum_{i=1}^{6} \alpha_i \times \eta_i \quad \text{i=load incidents} \tag{28}$$

Thus, the CEC efficiency for the proposed 17-level inverter based on six different %loading $(\alpha_i)_{i=1\text{ to }6}$ using equation (28) is calculated as 96.74%.

Table V
Efficiency of the proposed 17-level inverter for R-load at different output power.

$V_{c1}=V'_{c1}$=50V, $V_{cvm}=V'_{cvm}$= 25V, V_d=0.6V, V_{sw} =1.25 V, R_{sw} =11.9mΩ, r_c=0.03Ω & r_d=70.7 mΩ, P_{rated}=3500W, $f$sw=3kHz, V_{DC}=100V, β=3					
Output P_o (W)		Corresponding	α	α ×Ƞ	η_{CEC}
% of P_o	P_o (in watt)	efficiency Ƞ (%)		(%)	(%)
10%	350	96.50	0.04	3.86	96.74
20%	700	97.80	0.05	4.89	
30%	1050	98.10	0.12	11.77	
50%	1750	97.40	0.21	20.45	
75%	2625	96.30	0.53	51.00	
100%	3500	95.50	0.05	4.77	

VII. DESIGN PARAMETERS OF THE PROPOSED MLI

For a given maximum load current ($I_{o,max}$) of fundamental frequency (f) and a power factor, pf=cosφ, the amount of charge discharged by the capacitors C_1 (or C'_1) for a % ripple 'x' during a period t_5 to t_{11} (or t_{21} to t_{27}) as highlighted in Fig. 13 is calculated as:

$$Q_{C1,C'1} = \frac{I_{o,\max}}{2\pi f \times \%x}\left[\cos(\omega t_8 - \varphi) - \cos(\omega t_{11} - \varphi)\right] \tag{29}$$

Thus, the value of the capacitors C_1 and C'_1 is calculated for an average capacitor voltage V_{c1} by (30) as:

$$C_1, C'_1 = \frac{I_{o,\max}}{2\pi f \times V_{C1} \times \%x}\left[\cos(\omega t_8 - \varphi) - \cos(\omega t_{11} - \varphi)\right] \tag{30}$$

Similarly, the amount of charge ($Q_{CVM,\,C'VM}$) is discharged by the capacitors C_{VM}(or C'_{VM}) and the respective capacitor magnitude for a power factor angle φ, and % ripple (x) during the LDP period between t_7 to t_{10} (or t_{23} to t_{26}) is:

$$Q_{C_{VM},C'_{VM}} = \frac{I_{O\max}}{2\pi f \times \%x}\left[\cos(\omega t_8 - \varphi) - \cos(\omega t_{10} - \varphi)\right] \quad (31)$$

The corresponding value of the capacitors (C_{VM} and C'_{VM}) is calculated for an average capacitor voltage V_{CVM} by (32) as:

$$C_{VM}, C'_{VM} = \frac{I_{O\max}}{2\pi f \times V_{C_{VM}} \times \%x}\left[\cos(\omega t_8 - \varphi) - \cos(\omega t_{10} - \varphi)\right] \quad (32)$$

Equations (29)-(32) depicted that the value of a capacitor is inversely proportional to the percentage capacitor voltage ripple (%x). However, the capacitor discharges the highest amount of charge at unity power factor load for a given load current and voltage ripple.

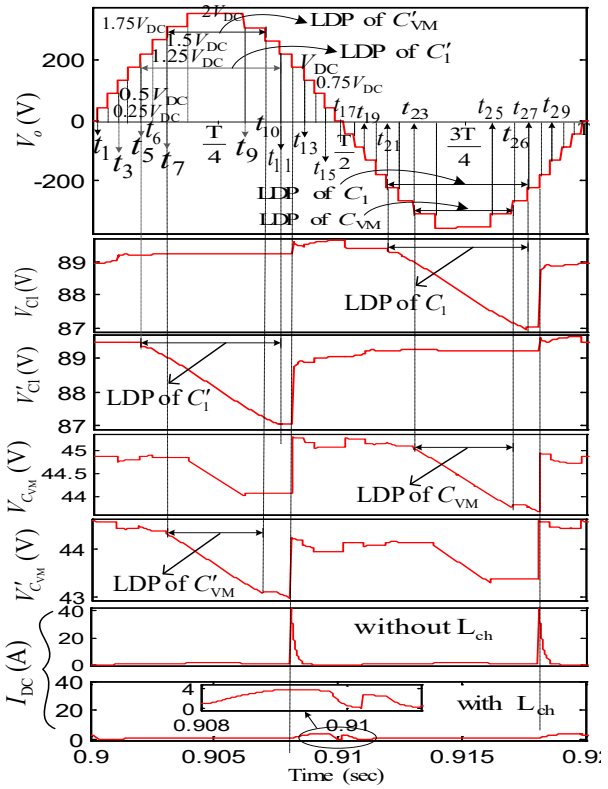


Fig. 13. Waveforms of output voltage, capacitor voltages & input DC currents without and with an L_{ch} under resistive load.

The value of capacitors (C_{VM} or C'_{VM} and C_1 or C'_1) versus the load resistance and power factor angle for different % ripple voltage is presented in Fig. 14. It is observed from Fig. 14 that the value of capacitances (C_{VM} or C'_{VM} and C_1 or C'_1) (in µF) for 5% ripple is much lesser than the respective capacitors with 2% ripple. Hence, the value of capacitances is chosen based on the 5% of ripple. It is observed from Figs. 14 (*a*)-(*b*) that the value of capacitances decreases with the increase of the load resistance. However, the capacitance value is less dependent on the power factor angle of the load, as observed from Figs. 14 (*c*)-(*d*). In order to limit the inrush current from the input or through the capacitors of the proposed switched-capacitor MLI (SC-MLI), an appropriate value of inductor (L_{ch}) is required to connect in series with the input voltage source [16].

Though, a large inductor causes additional problems like commutation and voltage spikes across the switches used for charging the capacitors. However, a small value of L_{ch} should be selected, which can limit the input current spike under the acceptable limit (33) [16] as:

$$L_{ch} = \frac{1}{(4\pi f)^2 \times C_m} \quad (33)$$

Where f represents the fundamental frequency of inverter voltage and C_m depicts the capacitance used for the proposed 17-level inverter. Thus, for the proposed 17-level inverter operating at a fundamental frequency of 50 Hz with a capacitor of capacitance 4700 µF, the value of L_{ch} is obtained as 0.53 mH, which is sufficient to limit the inrush current and does not create any adverse effects on the switching commutations. The waveforms of input DC current (I_{DC}) without and with an inductor are also presented in Fig. 13. It is observed from the input current waveforms from Fig. 13, that its peak value with the inductor (L_{ch}=0.53mH) becomes <4A, which reduces the inverter's VA rating also. For the grid-tied inverter of voltage levels (N_L), the minimum value of inductor ($L_{Filter,min}$) required for an L-type filter [22] is calculated as:

$$L_{Filter,min} = \frac{V_{DC} \times m_i \times (1 - m_i)}{8 \times f_{sw} \times \Delta I_L} \quad (34)$$

For a ripple current through the L filter (ΔI_L) of magnitude 20% of maximum grid current (I_L=6A), and switching frequency (f_{sw}=3kHz), the value of $L_{Filter,min}$=1 mH for N_L=17, with V_{DC}=180V at a modulation index (m_i)=0.8. However, the value of L_{Filter} for the proposed system is selected as 1.5mH.

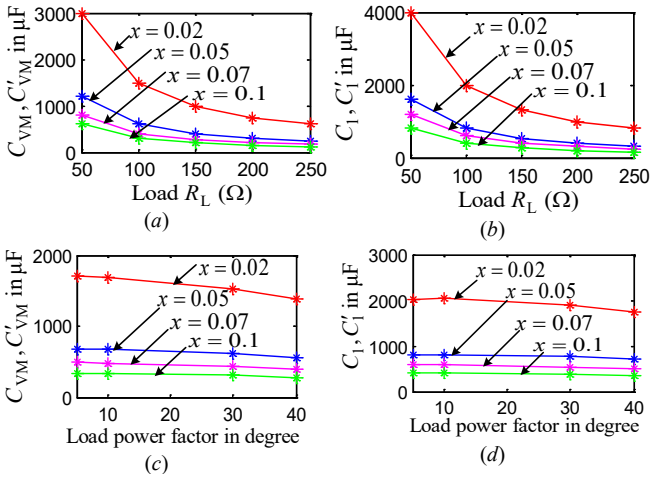


Fig. 14. Selection of the value of capacitors (*a*) C_{VM}, C'_{VM} for different values of %*x* and R_L, (*b*) C_1, C'_1 for different values of %*x* and R_L. (*c*) C_{VM}, C'_{VM} for different values of %*x* and power factor φ. (*d*) C_1, C'_1 for different values of %*x* and power factor φ.

VIII. EXPERIMENTAL VERIFICATION

The experimental setup of the proposed 17-level SC-MLI for grid-tied PV system (also for R-L load) is depicted in Fig. 15. The inverter is designed for a specimen of 1 kW (output). For standalone operation, the input voltage (V_{DC}) is considered as 200V for an R-L load (75 Ω, and 35 mH). However, for an experimental grid-connected system, the input voltage is set at 180V, which is obtained from a programmable DC power source with a solar array simulator model (LAB/SMS

8600). The major components of the experimental setup are indicated in Fig. 14, and their specification for simulation and the experimental setup are depicted in Table VI.

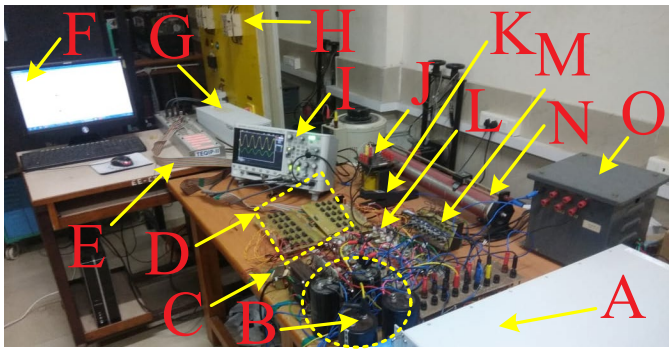


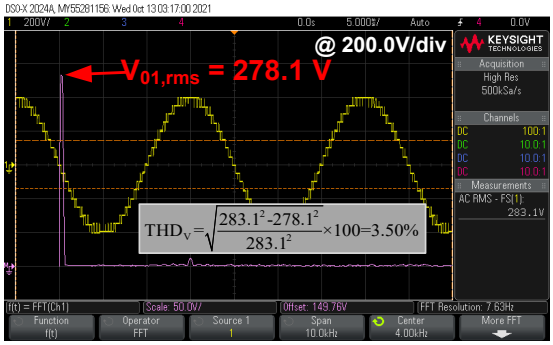
Fig. 15. Experimental setup of the proposed 17-level inverter consists of A: Programmable DC source (600V/15A), B: Electrolytic capacitors (400V, 3300µF and 400V, 4700µF), C & M: Isolated supply for driver ICs (240V/20V, 500mA) and delay circuit (240V/5V), D: Delay circuit board, E: Flat ribbon cable from DS1103 connector, F: PC, G: DS1103 controller, H: Single-phase grid panel (240V, 50Hz), I: DSO-X 2024A, J: Inductor for L filter (1.5mH), K: Current probe (1146B, 100 kHz/100A), L: IGBT based 17-level SCMLI with driver ICs, N: Rheostat, O: Inrush current limiting inductor (0.53mH).

Table VI
Experimental/simulation specifications

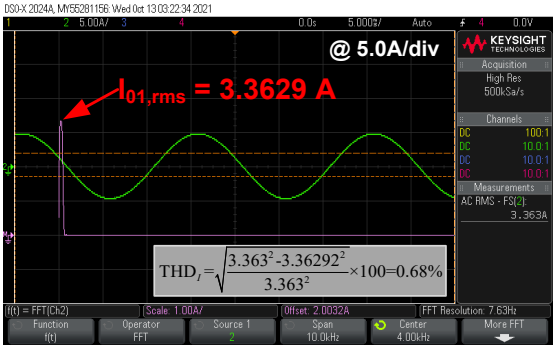
Parameters	Specifications
Programmable DC source as solar array simulator (LAB/SMS 8600)	600V, 15A, 8kW for experimental studies
L_{ch}, L_{Filter}	0.53mH, 1.5mH
IGBT (CT60AM18F)	900V, 60A
Diode (DSEI60-06A)	600V, 60A
Switching frequency (f_{sw})	3kHz
Single-phase grid voltage	240V, 50Hz
Input voltage, V_{DC}	180V for experiments, 200V for simulation
(C_1, C'_1) and (C_{VM}, C'_{VM}) at 400V	3300µF and 4700µF
Parasitic capacitance (C_{pg}) and R_G	100nF and 25Ω
K_P and K_i	0.88 and 220
R-L load values of R and L	75 Ω and 35 mH

The entire closed-loop control algorithm for grid-tied PV system is implemented using DS1103 based digital controller. The modified sinusoidal pulse width modulation (SPWM) technique is implemented at switching frequency f_{sw}=3kHz to obtain the PWM pulses. A delay-time of 2µsec is introduced using an external delay circuit, which is further passed through the gate driver circuit. A high sampling time of 20 µsec is selected for both simulation and experimental development to detect the unwanted events and respond to maintain high reliability and system efficiency. The gate driver circuit is used for isolation of the power circuit from the control circuit as well as to provide DC voltage value of (±20V) for turning ON the IGBT switches.

The experimental results output voltage, current, and their THD (i.e. THD_V and THD_i) for R-L load (R=75 Ω, and L=35 mH) of the proposed 17-level inverter are depicted in Fig. 16. It is observed in Fig. 16 that for a given input voltage of 200 V, the RMS value of the output voltage and fundamental voltage are 283.1 V and 278.1 V, respectively. In comparison, the RMS value of the output and its fundamental current is 3.363A and 3.36292A, respectively. Based on these voltages and currents, the THD_V and THD_i are calculated as 3.5% and 0.68%, respectively.



(*a*)



(*b*)

Fig. 16. Experimental waveforms of the proposed 17-level inverter at modulation index (m_i=1.0) for (a) output voltage and its THD, (*b*) load current for R-L load with V_{DC}=200V.

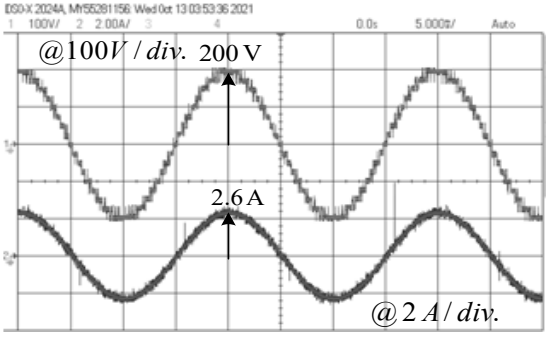
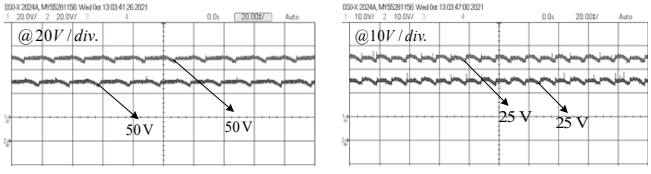


Fig. 17. Experimental output voltage and current waveform of the proposed 17-level inverter for an input voltage of 100 V.



(*a*) (*b*)

Fig. 18. Experimental voltage waveform of (*a*) C_1 and C'_1, (*b*) C_{VM} and C'_{VM} for the input voltage of 100 V.

For V_{DC}=100V, the inverter's experimental output voltage and current waveform under R-L load (R=75 Ω, and L=35 mH) are presented in Fig. 17. It is observed that the peak value of output voltage current are 200V and 2.5A, respectively. The experimental waveforms of the voltages across the capacitors (C_1, C'_1) and (C_{VM}, C'_{VM}) are shown in Fig. 18. It is observed that voltages across the capacitors (C_1, C'_1) and (C_{VM}, C'_{VM}) are 50 V and 25 V, respectively.

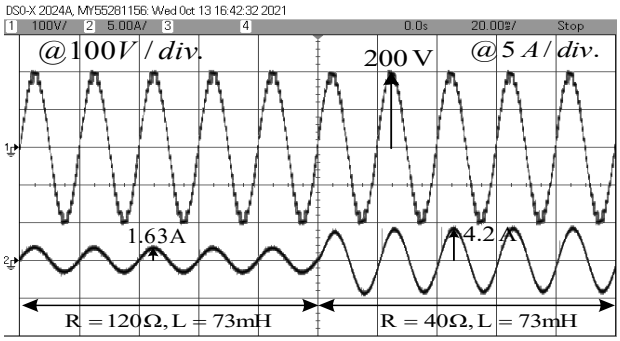


Fig. 19. Experimental waveform of output voltage and current of the proposed 17-level inverter under dynamic loading condition.

Fig. 19 represents the experimental waveforms of inverter output voltage and current under a dynamic loading corresponding to the step-change in load resistance from R=120 Ω, to R=40 Ω. As a result, the change in the value of peak current changes from 1.63A to 4.2A. The experimental waveforms of the capacitor voltages under the same dynamic loading condition are also presented in Fig. 20. It is observed from Fig. 20 that the average voltage across the capacitors remains the same, but the rate of charging/discharging of the capacitors varies with change in load current.

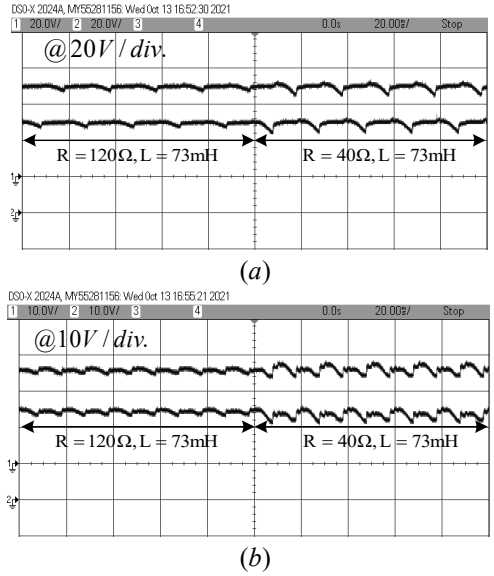


Fig. 20. Experimental voltage waveform of (*a*) C1 and C′1, (*b*) CVM and C′VM for the fixed input voltage of 100 V and dynamic loading condition.

Fig. 21 depicts the measured efficiency of the proposed 17-level inverter with the variation of output power in the range of 350W to 2500W. It is observed that around 1.15KW, the proposed inverter has reached its maximum efficiency of 96.62 %.

Similarly, for a grid-connected system, the experimental results of the current from the PV Emulator (LAB/SMS 8600) and inverter input current at irradiation 800W/m^2 are depicted

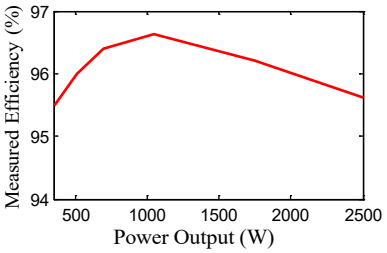


Fig. 21. Measured efficiency of the proposed 17-level inverter.

in Fig. 22. From Fig. 22, it is observed that, due to the presence of L_{ch}, the peak input current (I_{in}) of the inverter is reduced to an approximate value of 24A.

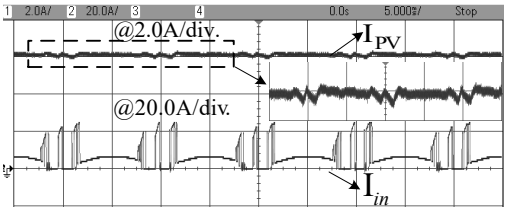


Fig. 22. The experimental waveform of the input current of PV and inverter.

The experimental results of grid voltage (V_{Grid}), inverter output voltage (V_{out}), and grid current (I_{Grid}) at unity power factor for irradiation of 800W/m^2 to 600W/m^2 are depicted in Fig. 23(*a*)-(*b*). Using a simple L filter of inductance, L_{filter}=1.5 mH, the current I_{Grid} becomes sinusoidal. It is also observed that with a decrease in solar irradiation, mainly the value of I_{Grid} decreases with a minor change of PV voltage (V_{pv}) or inverter output voltage.

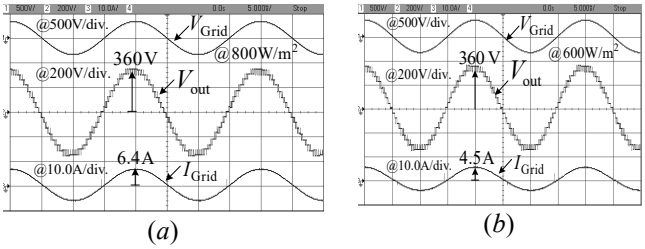
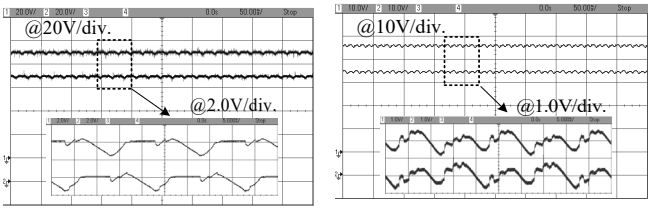


Fig. 23. Experimental waveform of grid voltage, inverter voltage & grid current at irradiation (*a*) 800W/m^2, and (*b*) 600W/m^2.

The steady-state voltage waveform of the capacitor C_1, C'_1, C_{VM} and C'_{VM} are shown in Fig. 24. It is observed that voltage across the capacitors, which maintained a fixed average voltage magnitude under steady-state. The voltage across the capacitors C_1 and C'_1 are measured as almost 88.5V, whereas the voltage across capacitors C_{VM} and C'_{VM} are measured as 44.38V. Thus the ratio of their voltage is always maintained 2:1 as per the requirements.

The performance of the proposed system is also tested under dynamic conditions like a change of solar irradiation from 800 W/m^2 to 600 W/m^2 as presented in Fig. 25. From Fig. 25, it is observed that with a decrease in the above irradiation, the PV voltage is slightly changed from 180V to 176.2V, but the grid

current is reduced from 6A (peak) to 4.5A (peak). Thus, the inverter output voltage magnitude is maintained nearly constant value around 353V (peak) during steady-state. $_{leak}$) flowing from the grid-side to the PV side during the step-change in V_{TCM} from 0 to 180V are measured as 22 mA (RMS), as depicted in Fig. 26, which is well within the acceptable limit.



(*a*) (*b*)

Fig. 24. Experimental voltage waveform of (*a*) C_1 and C'_1, (*b*) C_{VM} and C'_{VM}.

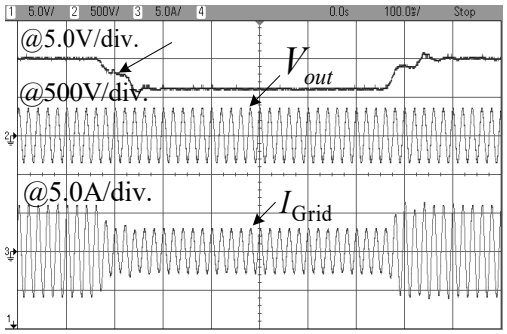


Fig. 25. Dynamic performance of PV voltage, inverter voltage, and grid current with change in irradiation from 800W/m^2 to 600W/m^2.

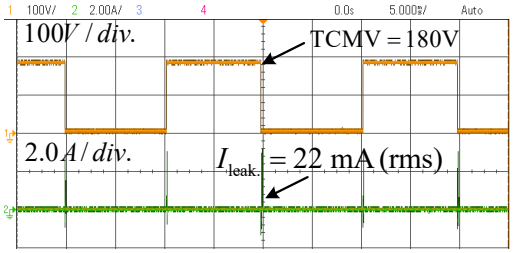


Fig. 26. Experimental results of TCMV and leakage current (I_{leak}).

IX. CONCLUSIONS

A basic single-phase 17-level boost inverter-based PV system is designed for a transformerless grid-connected system. The proposed inverter is able to limit the leakage current to 22mA, which is much lesser than the acceptable limit of 300mA as per the German standard. The modified SPWM technique further makes the leakage current independent of the inverter switching frequency. The ripple voltage across the capacitors is much smaller, which reduces the overall losses and improves the inverter efficiency even at increased output power. Comparative studies proved that the performance of the proposed MLI is better than most of the other similar kinds of MLIs. A d-q based closed-loop current control is implemented for the grid-tied system using DS1103 based digital controller to control the active power transfer from the PV to the grid. Experimental results are presented to verify the simulation results. Moreover, the closed-loop system remains stable after the transient is over.

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