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Computation-Efficient Variable Angle Phase-Shifting PWM Method for Cascaded H-Bridge Converters

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***Abstract*—When the cells of a cascaded H-bridge (CHB) converter are unbalanced, variable angle phase-shifting (VAPS) pulse-width modulation (PWM) methods can be employed to improve the total harmonic distortion (THD) performance. However, as conventional methods are based on optimization algorithms which require a large number of evolutionary computations, the optimal carrier phase-shifting (PS) angles cannot be timely updated with a common standard digital signal processor (DSP) or microcontrollers. During the period when the optimization is not finished, the THD of the total output voltage may significantly increase, bringing about higher power losses. Thus, a computation-efficient VAPS PWM method is proposed in this paper. With multiple calculation units (CUs) implemented in field programmable gate arrays (FPGAs), multiple calculations can be executed in parallel, significantly improving the optimization speed of the VAPS PWM method. Experimental results on a 4-cell CHB converter have demonstrated the effectiveness of the proposed method.**

Keywords—Cascaded H-bridge converter (CHB), harmonic mitigation, phase-shifting (PS) modulation, parallel computing.

I. INTRODUCTION

Phase-shifting pulse-width modulation (PSPWM) methods have been widely employed for cascaded H-bridge (CHB) converters [1]-[4]. By properly shifting the carrier phase-shifting (PS) angles, the equivalent switching frequency of the CHB converter can be increased to $2nf_s$, where f_s is the switching frequency of one bridge arm, and n is the number of cascaded cells. As a result, harmonics at lower frequencies can be canceled [1]. However, when individual cells are unbalanced, i.e., nonidentical DC voltages, modulation indices, and power factors (PFs), the conventional PSPWM will lose its harmonic cancellation property [3], [4]. Consequently, the THD of the total output voltage can be significantly increased. Such unbalanced operation conditions are common in many applications, e.g., modular multilevel photovoltaic (PV) converter systems [5], hybrid energy storage systems [6], and series PV-battery systems [7], [8]. To address this issue, variable angle phase-shifting (VAPS) pulse-width modulation (PWM) methods can be employed, where the carrier PS angles of all cells are regulated [3], [4], [9]-[14]. In [4], [9]-[12], the carrier PS angles are real-time calculated according to the outputs of individual converters using inverse trigonometric functions. By doing so, harmonic components with their frequencies being near $2f_s$ (f_s is the switching frequency of one bridge arm) can be eliminated. However, this method cannot be applied to systems when the PFs of individual cells are different (e.g., series-PV-battery systems), where the optimal carrier PS angles are mathematically unfeasible. More recently, a closed-loop harmonic suppression scheme has been developed in [13], where the carrier PS angles are adjusted online with proportional-integral regulators. Nevertheless, only the harmonic at a specific frequency can be suppressed with this method, while it is unable to achieve a minimum THD of the total output voltage.

Considering the above, mathematical searching algorithms can be employed to calculate proper carrier PS angles, such as the exchange marketing algorithm (EMA) [14], and the particle swarm optimization (PSO) algorithm [15]. However, these methods are of slow dynamics, because a large number of iterative computations are involved in the optimization, which is time-consuming (e.g., hundreds of milliseconds) if it is executed with a standard DSP. When the optimal angles are not calculated, the high-frequency harmonics may increase significantly, leading to higher power losses and a degraded power quality. In fact, only the steady-state performance has been demonstrated in previous research, while the dynamics of the VAPS PWM method based on optimization algorithms has not been evaluated.

Therefore, to improve the dynamic response of the VAPS PWM methods, a computation-efficient method is proposed in this paper. By building modular calculation units (CUs) in field programmable gate arrays (FPGAs), multiple computations are executed in parallel, thus significantly improving the optimization speed of the VAPS PWM method. The rest of this paper is organized as follows. In Section II, the PSO algorithm which is used for the VAPS PWM method is introduced. Then, the implementation of the proposed computation-efficient method is discussed in Section III. In Section IV, the effectiveness of the proposed is validated on a 4-cell CHB converter using a control system with one DSP and two FPGAs. In Section IV, the performance of the proposed method for CHB converters with more cascaded cells is quantitively evaluated in terms of the execution time and the hardware requirements. Finally, concluding remarks are given in Section V.

II. CONVENTIONAL VAPS PWM METHODS

The block diagram of the VAPS PWM method is shown in Fig. 1, where a 4-cell CHB converter is exemplified. Two opposite carriers are assigned to each H-bridge cell to double the switching frequency of its output voltage [16], while all carriers

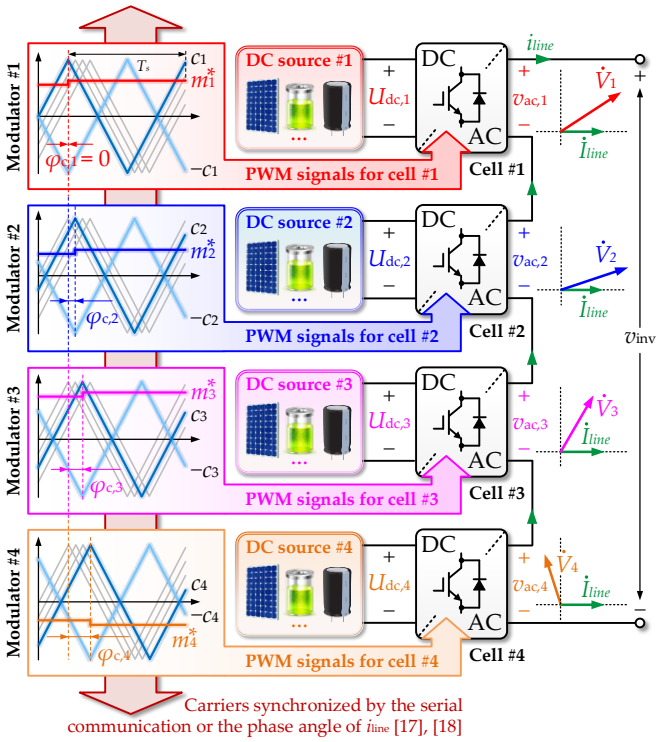

Fig. 1. Diagram of the VAPS PWM method for a 4-cell CHB converter, where $U_{dc,k}$, $v_{ac,k}$, m_k^*, c_k and $\varphi_{c,k}$ refer to the DC voltage, output AC voltage, modulation index, carrier, and carrier PS angles for the k^{th} converter (k = 1, 2, 3, …), respectively, v_{inv} is the total output voltage of the CHB converter, and $\dot{V}_k$ and $\dot{I}_{line}$ are the phasors of $v_{ac,k}$ and i_{line}, respectively.

are synchronized and phase-shifted with respect to the carrier of the first cell [17], [18]. When PV panels or batteries are connected to the DC rails of individual cells, the DC and AC voltages of these converter cells can be unbalanced. For instance, the DC and AC voltages of a PV converter cell is dependent on the PV voltage and the available PV power, which can be affected by solar irradiance and ambient temperature. The unbalanced voltages among different cells can lead to a varying THD of the total output voltage v_{inv}, if all the carrier PS angles are fixed. Thus, the objective of the VAPS PWM method in [14] is to find a set of carrier PS angles for individual cells that minimize the total harmonic contents in the output voltage, which is expressed as [16]

$$U_{h,sum}=\sqrt{\sum_{f=f_0+1}^{\infty}\left[\left(\sum_{k=1}^{n}U_{hkf}\cos\varphi_{hkf}\right)^2+\left(\sum_{k=1}^{n}U_{hkf}\sin\varphi_{hkf}\right)^2\right]} \quad (1)$$

with

$$\varphi_{hkf}=\varphi_{hk(h_1f_c+h_2f_0)}=2h_1\pi\varphi_{c,k}+(2h_2-1)\varphi_{0,k} \quad (2)$$

$$U_{hkf}=U_{hk(h_1f_c+h_2f_0)}=\frac{\sqrt{2}U_{dc,k}}{\pi h_1}J_{2h_2-1}(h_1\pi M_k)\cos(h_1+h_2-1). \quad (3)$$

where $U_{h,sum}$ is the sum of the voltage harmonics. U_{hkf} and φ_{hkf} are the amplitude and phase-angle of the voltage harmonic at the frequency being f for the k^{th} cell, where $f = h_1f_c + h_2f_0$. f_0 and f_c are the fundamental and carrier frequencies, respectively, and h_1 and h_2 are two integers ($h_1 > 0$). M_k, $U_{dc,k}$, $\varphi_{0,k}$ and $\varphi_{c,k}$ are the amplitude of the modulation index, DC voltage, phase angle of the fundamental voltage and carrier PS angle for the k^{th} cell, respectively. $J_i(x)$ is the Bessel function [16]

$$J_i(x)=\sum_{j=0}^{\infty}\frac{(-1)^j}{j!(j+i)!}\left(\frac{x}{2}\right)^{2j+i}. \quad (4)$$

It is known that for a given set of $\vec{U}_{dc}$, $\vec{M}$ and $\vec{\varphi}_0$ ($\vec{U}_{dc}$ = [$U_{dc,1}$, $U_{dc,2}$, … $U_{dc,n}$], $\vec{M}$ = [M_1, M_2, … M_n], and $\vec{\varphi}_0$ = [$\varphi_{0,1}$, $\varphi_{0,2}$, … $\varphi_{0,n}$], it is difficult to find an analytical solution of $\vec{\varphi}_c$ ($\vec{\varphi}_c$ = [$\varphi_{c,1}$, $\varphi_{c,2}$, … $\varphi_{c,n}$]) that minimizes $U_{h,sum}$ in (1). To solve this large-scale nonlinear optimization problem, the PSO algorithm is employed, as illustrated in Fig. 2 and explained as follows.

1) Initialize the positions and velocities randomly in the feasible region for all particles using

$$\vec{\varphi}_{c,\beta}^{\,0}=\left[\varphi_{c,\beta,1}^{0}\quad\varphi_{c,\beta,2}^{0}\quad\cdots\quad\varphi_{c,\beta,n}^{0}\right]^T=\left[0\quad rand(0,\pi)\quad\cdots\quad rand(0,\pi)\right]^T \quad (5)$$

and

$$\vec{v}_{\beta}^{\,0}=\left[v_{\beta,1}^{0}\quad v_{\beta,2}^{0}\quad\cdots\quad v_{\beta,n}^{0}\right]^T=\left[0\quad rand(-v_{max},v_{max})\quad\cdots\quad rand(-v_{max},v_{max})\right]^T \quad (6)$$

where $\varphi_{c,\beta,k}^{0}$ and $v_{\beta,k}^{0}$ are the initial carrier PS angle and velocity for the β^{th} particle and the k^{th} converter cell, respectively, and $\vec{\varphi}_{c,\beta}^{\,0}$ and $\vec{v}_{\beta}^{\,0}$ are the corresponding initial arrays. $rand([a,b])$ refers to a random number within the range of $[a,b]$, and v_{max} is the predefined maximum velocity.

2) Calculate $U_{h,sum}^2$ for all particles using (1)-(3). Then, store the historical best position (with the minimum $U_{h,sum}^2$) for each particle (denoted as $\vec{\varphi}_{c,\beta}^{\,best}$ for the β^{th} particle), and the historical global best position among all particles ($\vec{\varphi}_{c,g}^{\,best}$).

3) Update the positions and velocities of all particles using

$$\vec{\varphi}_{c,\beta}^{\,\alpha+1}=\vec{\varphi}_{c,\beta}^{\,\alpha}+\vec{v}_{\beta}^{\,\alpha+1} \quad (7)$$

and

$$\vec{v}_{\beta}^{\,\alpha+1}=\omega_{PSO}\vec{v}_{\beta}^{\,\alpha}+c_p r_{1,\beta}\left(\vec{\varphi}_{c,\beta}^{\,best}-\vec{\varphi}_{c,\beta}^{\,\alpha}\right)+c_g r_{2,\beta}\left(\vec{\varphi}_{c,g}^{\,best}-\vec{\varphi}_{c,\beta}^{\,\alpha}\right) \quad (8)$$

where $\vec{\varphi}_{c,\beta}^{\,\alpha}$ = [$\varphi_{c,\beta,1}^{\alpha}$, $\varphi_{c,\beta,2}^{\alpha}$, … $\varphi_{c,\beta,n}^{\alpha}$] and $\vec{v}_{\beta}^{\,\alpha}$ = [$v_{\beta,1}^{\alpha}$, $v_{\beta,2}^{\alpha}$, … $v_{\beta,n}^{\alpha}$] are the arrays of the carrier PS angles and velocities for the β^{th} particle in the α^{th} iteration, respectively, ω_{PSO} is the coefficient for updating the velocity of each particle, c_p and c_g are the local and global learning factors in the PSO algorithm, respectively, and $r_{1,\beta}$ and $r_{2,\beta}$ are two random numbers within the range of [0,1] for the β^{th} particle. Then, repeat steps 2) and 3), until the iteration reaches the maximum cycle index α_{max}.

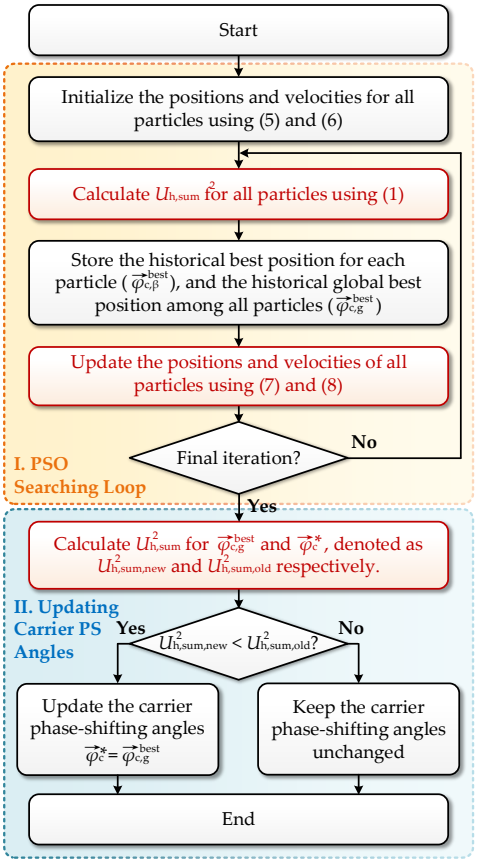

Fig. 2. Flow chart of the PSO-based algorithm to calculate the carrier PS angles.

4) When the optimized $\vec{\varphi}_{c,g}^{best} = [\varphi_{c,g,1}^{best}, \varphi_{c,g,2}^{best}, \ldots \varphi_{c,g,n}^{best}]$ is obtained after a certain number of iterations, $U_{h,sum}^2$ will be calculated with the carrier PS angles being $\vec{\varphi}_{c,g}^{best}$ and $\vec{\varphi}_c^*$. Here, $\vec{\varphi}_c^*$ is the array of the carrier PS angle reference at the current state, and $\vec{\varphi}_c^* = [\varphi_{c,1}^*, \varphi_{c,2}^*, \ldots \varphi_{c,n}^*]$. Then, if $U_{h,sum,new}^2$ is smaller than $U_{h,sum,old}^2$, $\vec{\varphi}_c^*$ will be replaced by $\vec{\varphi}_{c,g}^{best}$. Otherwise, it will be kept unchanged. Finally, $\vec{\varphi}_c^*$ will be used as the array of the carrier PS angle references for the modulator.

It can be noticed that many calculations are involved in the algorithm, where $U_{h,sum}^2$ should be calculated for all particles in each round of iteration. Considering that (1) is complex, it is time-consuming for a DSP to solve the optimization problem. When the output voltage of each converter changes, conventional VAPS PWM methods cannot timely update the optimized carrier PS angles. During the period when the optimization is not finished, the THD performance of the converter can be degraded due to the presence of high-frequency harmonics below $2nf_s$. Especially for operating conditions when the DC or AC voltages of individual converters frequently change, the THD performance can be much worse with the DSP-based optimization due to slow dynamics. For instance, due to the maximum power point tracking (MPPT) control, the operating points of each converter in a CHB PV system will change every 1 to 10 ms, which can be faster than the response

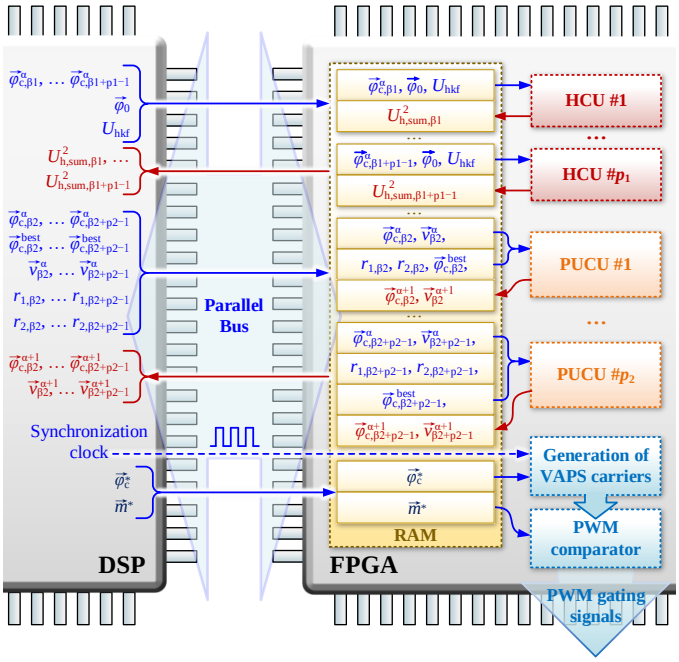

Fig. 3. Hardware schematic for the proposed FPGA-enabled VAPS PWM method, where $\vec{m}^* = [m_1^*, m_1^*, \ldots m_1^*]$ is the array of the modulation indices for all converter cells.

speed of the VAPS PWM method. In this case, the VAPS PWM method may fail to find the optimal carrier PS angles all the time. Considering the above, it calls for the development of faster VAPS PWM methods.

III. FPGA-Enabled Computation-Efficient Method

To overcome the computing limitation, multicore computing can be considered. The basic idea is to build several calculation units (CUs) with additional hardware, where multiple calculations can be executed in parallel, thus improving the optimization speed. The schematic of the proposed method for a 4-cell CHB is shown in Fig. 3, where multiple CUs are implemented in the FPGA, including several harmonic calculation units (HCUs) and particle updating calculation units (PUCUs). The HCUs are responsible for calculating $U_{h,sum}^2$ with the given set of U_{hkf}, $\vec{\varphi}_0$ and $\vec{\varphi}_c$ from the DSP, while the PUCUs are responsible for calculating the updated position $\vec{\varphi}_{c,\beta}^{\alpha+1}$ and velocity $\vec{v}_\beta^{\alpha+1}$ for each particle with the given $\vec{v}_\beta^{\alpha}$, $\vec{\varphi}_{c,\beta}^{\alpha}$, $\vec{\varphi}_{c,\beta}^{best}$, $\vec{\varphi}_{c,g}^{best}$, $r_{1,\beta}$, and $r_{2,\beta}$ from the DSP using (7) and (8), respectively (the subscript "β" denotes that the variable is for the β^{th} particle). Those variables are exchanged between the DSP and the FPGA through the parallel communication bus that has high bandwidth. The DSP is to execute the rest of the algorithm, e.g., initialization, logic execution, and random number generation.

The structures of the PUCU and the HCU are shown in Figs. 4 and 5, respectively, where multiple calculations are also in parallel. To simplify the calculation while better utilizing the limited hardware resources in FPGAs, the hardware structures of these CUs are optimized from the following aspects:

1) For the convenience of mod operations, per unit values have been employed for all phase angle variables (including all $\vec{\varphi}_0$, $\vec{\varphi}_c$, and φ_{hkf}).

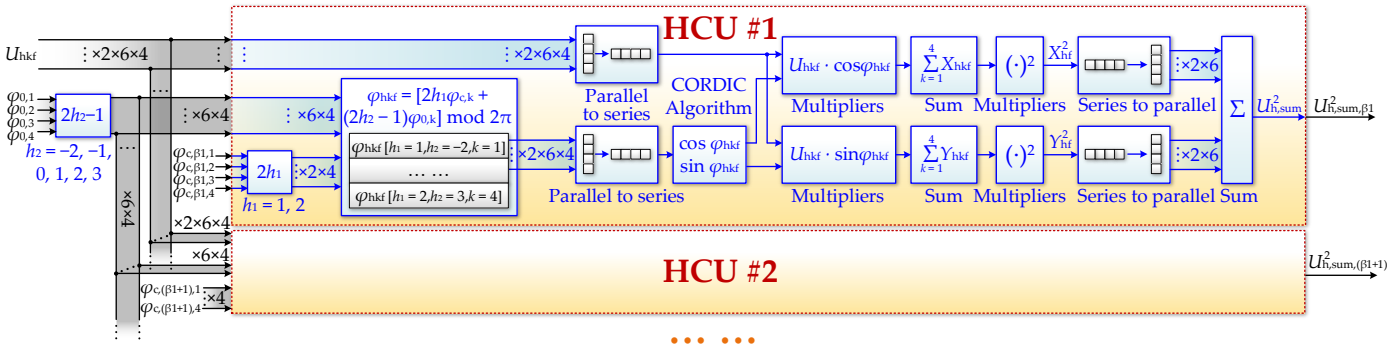

Fig. 4. Hardware structure of HCUs for a 4-cell CHB converter, where X_{hkf} and Y_{hkf} are the amplitudes of the real and imaginary part of U_{hkf}, respectively, and X_{hf} and Y_{hf} are the amplitudes of the real and imaginary part of one harmonic in the total output voltage, respectively.

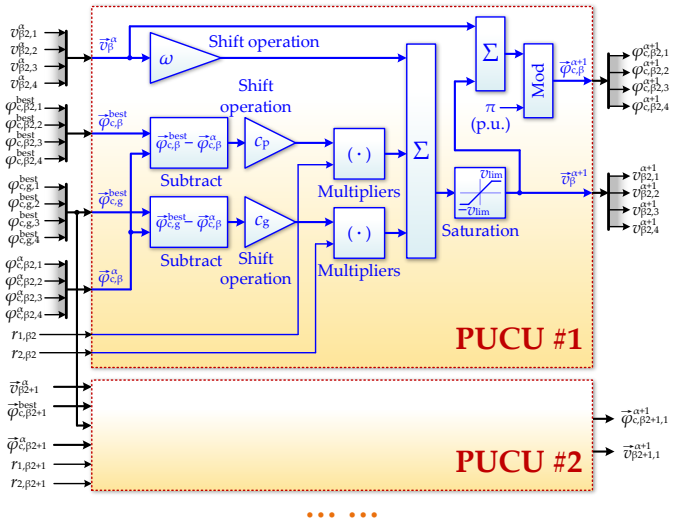

Fig. 5. Hardware structure of PUCUs for a 4-cell CHB converter.

2) To simplify trigonometric operations, the coordinate rotation digital computer (CORDIC) algorithm is employed.

3) To better utilize the limited hardware resources, several complex computations are executed in series, including several trigonometric and multiplication operations, which require a large amount of hardware resources. Although the series computing will slow down the calculation speed, more HCUs can be implemented in FPGAs due to the reduced circuit size, enabling the parallel computing of multiple particles.

With the above FPGA-enabled calculation, the speed of the optimization algorithm can be improved:

1) When calculating $U^2_{h,sum}$, $\vec{\varphi}^{\alpha+1}_{c,\beta}$ and $\vec{v}^{\alpha+1}_{\beta}$ for each particle, multiple additions and multiplications (can be replaced by shifts and additions) can be executed in parallel.

2) Multiple particles can be processed in parallel with multiple CUs.

3) The calculation speed can be further improved with higher clock frequency for the FPGA, e.g., using hardware phase locked loop (PLL) in the FPGA.

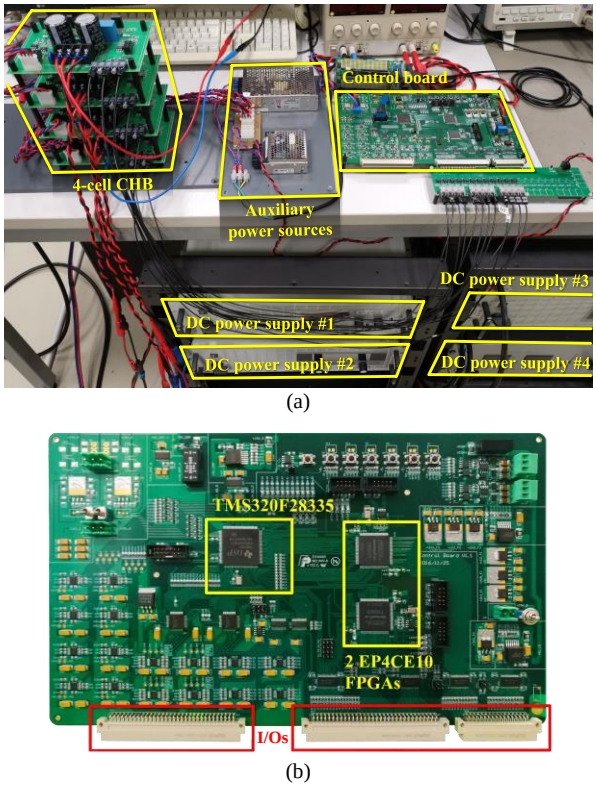

Fig. 6. Photo of the experimental platform: (a) the 4-cell CHB inverter, and (b) the DSP+FPGA control system used in Fig. 6(a).

IV. Experimental Verification

To validate the effectiveness of the proposed method, experiments have been performed on a 4-cell CHB prototype (f_s = 1.25 kHz), where $\vec{U}_{dc}$ = [120 V, 100 V, 110 V, 80 V], and the modulation indices change from $\vec{M}$ = [0.9, 0.3, 0.9, 0.9] and $\vec{\varphi}_0$ = [0, 3.1293, 0, 0] to $\vec{M}$ = [0.9, 0.8, 0.9, 0.3] and $\vec{\varphi}_0$ = [0.5277, 0, 0, 3.1293]. The photo of the experimental prototype is shown in Fig. 6, where the control system includes one TMS320F28335 DSP and two EP4CE10 FPGAs. The parameters of the system, as well as the resolution of all variables are given in Tables I and II, respectively. One-hundred particles with ten times of iteration have been employed in the

TABLE I
PARAMETERS IN THE EXPERIMENTS

Parameter	Value
System clock frequency of the DSP	150 MHz
Main Clock frequency of the FPGA	150 MHz
Bus-width of the parallel communication	12-bit
Bus-frequency of the parallel communication	28 MB/s
Control and sampling frequency	1.25 kHz
Switching frequency of one bridge arm	1.25 kHz

TABLE II
OPERATIONAL PRECISION FOR VARIABLES IN HCUS AND PUCUS

Variables	Sign bit	Integer bits	Decimal bits
U_{hkf}	1	12	12
φ_{hkf} (p.u.)	0	1	8
$\cos(\varphi_{hkf})$ and $\sin(\varphi_{hkf})$	1	1	8
$U_{hkf} \cdot \cos(\varphi_{hkf})$ and $U_{hkf} \cdot \sin(\varphi_{hkf})$	1	10	18
ΣX_{hkf} and ΣY_{hkf}	1	10	10
X_{hf}^2 and Y_{hf}^2	0	20	20
$U_{h,sum}^2$	0	20	4
$\varphi_{c,\beta,k}^{\alpha}$, $\varphi_{c,\beta,k}^{best}$, and $\varphi_{c,g,k}^{best}$ (p.u.)	0	1	8
$v_{\beta,k}^{\alpha}$ (p.u.)	1	0	8
r_1 and r_2	0	0	9

*subscript "k" is the converter index.

optimization. Lookup tables (LUTs) have been used for the Bessel function and trigonometric functions to simplify the calculation.

Figs. 7 and 8 demonstrate the experimental results with the DSP-based method. Initially, the CHB converter is operating with optimal carrier PS angles ($\vec{\varphi}_c^* = [0, 1.1290, 2.0249, 1.6690]$). After the change of the modulation indices, the THD performance of v_{inv} is degraded for 580 ms, until the optimal angles $\vec{\varphi}_c^* = [0, 0.0736, 2.1598, 1.0677]$ are obtained. The THD performance is even worse during the transition, i.e., in the first 11 fundamental cycles, where it is increased to 58.03%, being much higher than the initial 31.50%, as shown in Figs. 8(a) and (b). The THD is optimized to 41.28% after the 1st optimization, which is still not as good as the optimal 37.74% THD in steady state, which is obtained after the 3rd optimization.

Experimental results of the proposed computation-efficient VAPS PWM method are shown in Figs. 9 and 10, where four HCUs and one PUCU have been implemented in two FPGAs. The THD of v_{inv} in Zones 1 and 2 is almost identical with that in Zones 3 and 6 in Fig. 7, respectively, as demonstrated in Fig. 10. However, the required time to calculate the optimal angles is reduced from 580 ms to 28 ms, indicating a significant improvement in the optimization speed. Especially for the period where the voltage THD is significantly degraded (Zone 3 in Fig. 9(b)), it only lasts for less than one fundamental cycle. Thus, with the proposed method, the dynamics of the VAPS PWM method can be significantly improved.

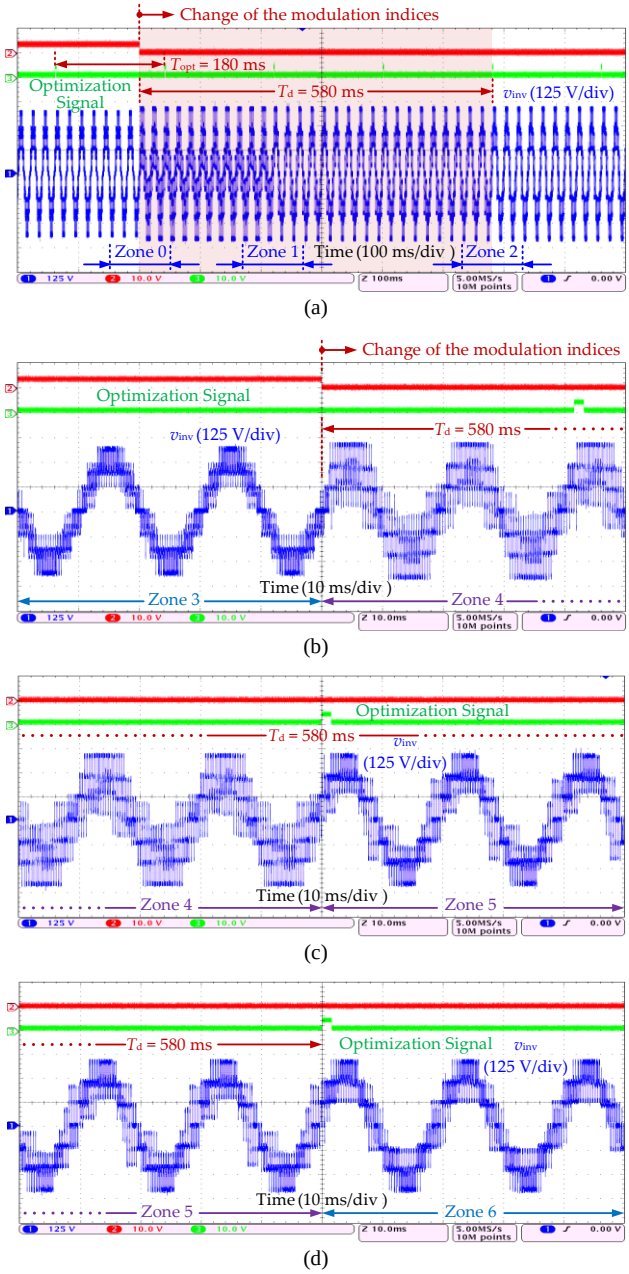

Fig. 7. Experimental results of Case 2 with the DSP-based VAPS PWM: (a) output multilevel voltage, and (b), (c), and (d) zoomed-in plots of Zones 0, 1, and 2 in Fig. 7(a).

V. PERFORMANCE EVALUATION OF THE PROPOSED METHOD

In terms of the execution time for the optimization, three cases of the proposed computation-efficient method are compared with the conventional DSP-based approach, as shown in Figs. 11 and 12. According to Fig. 11(a), for one round of iteration with 100 particles, the calculation speed can be accelerated nine times faster than the DSP-based method using 1 HCU in the FPGA. The most time-consuming part in the optimization is the calculation of $U_{h,sum}^2$, which takes 93% of the total time for the DSP-based method, while it only accounts for

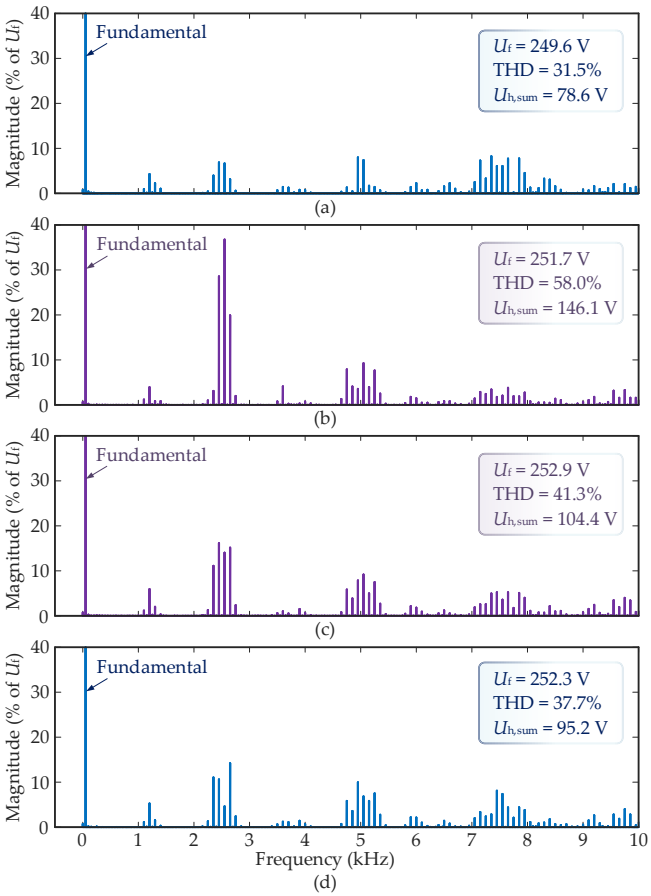

Fig. 8. Experimental results of Case 2 with the DSP-based VAPS PWM: (a) output multilevel voltage, and (b), (c), and (d) zoomed-in plots of Zones 0, 1, and 2 in Fig. 7(a).

43% of the total time with 1 HCU, being only 0.86 ms. The calculation of $\vec{\varphi}_{c,\beta}^{\alpha+1}$ and $\vec{v}_{\beta}^{\alpha+1}$ can be accelerated by adding 1 PUCU in the FPGA, with which the time for calculating all $\vec{\varphi}_{c,\beta}^{\alpha+1}$ and $\vec{v}_{\beta}^{\alpha+1}$ values is reduced from 0.68 ms to 0.27 ms (17% of the total time, including the time for manipulating the parallel bus), as shown in Fig. 12(c). When 4 HCUs and 1 PUCU are equipped, the calculation speed can be accelerated 19.3 times faster than the DSP-based method. However, compared to the case with 1 HCU and 1 PUCU, the improvements of the 4-HCU approach is not very significant, being only 1.7 times faster. This is because the manipulation of the parallel bus as well as other codes in the DSP (e.g., logic execution) have become the most time-consuming parts in the entire algorithm, being 33% and 37% of the total time, respectively, while the calculations which are accelerated by FPGAs only account for 29% of the total time. This indicates that the improvements will become minor when more CUs are equipped, because the communication between the DSP and the FPGA will be the bottleneck in the optimization speed. Considering the above, in order to further accelerate the optimization speed, efforts can be made from the following two aspects:

1) A parallel bus between the DSP and FPGAs with wider bus-width can be employed to reduce the time spent on the communication, e.g., a maximum 32-bit data bus.

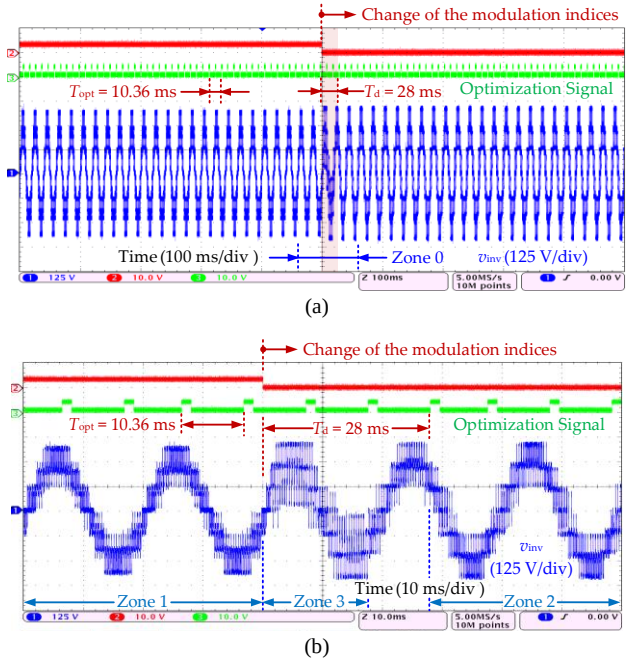

Fig. 9. Experimental results of Case 2 using the proposed computation-efficient VAPS PWM method: (a) output multilevel voltage, and (b) zoomed-in plot of Zone 0 in Fig. 9(a).

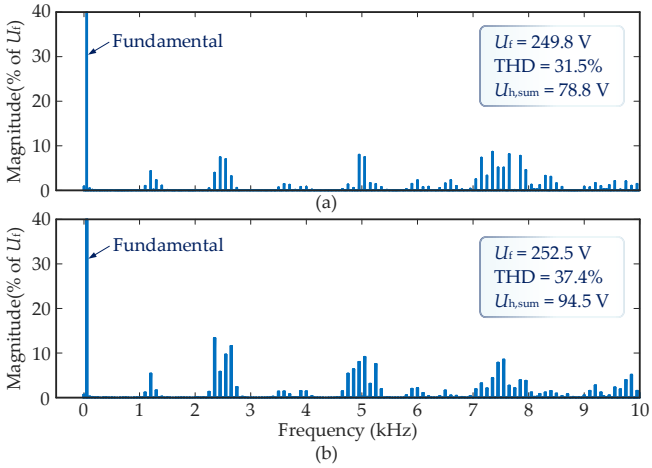

Fig. 10. Frequency spectra of the multilevel voltage in (a) Zone 1, and (b) Zone 2 of Fig. 9(b).

2) Apart from the implementation of a few CUs, the rest of the optimization can be incorporated in the FPGA. By doing so, the time spent on the communication between the FPGA and the DSP (33% of the total time in Fig. 12(d)), as well as the logic execution of the optimization algorithm (37% of the total time in Fig. 12(e) (Other codes)) can be further reduced.

The improvements in terms of the dynamic response will be more significant for CHB converters with a higher number of cascaded cells. As it can be seen from Fig. 13, with the increase of the cascaded cell number, more time is required to obtain the optimal carrier PS angles due to an increased amount of computation. When 10 cells are cascaded, the required time for

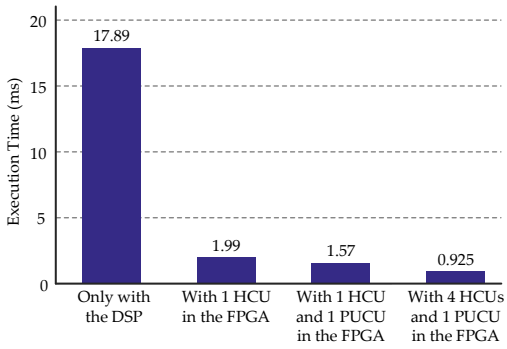

Fig. 11. Time consumption of the VAPS PWM method with different number of CUs for one iteration with 100 particles.

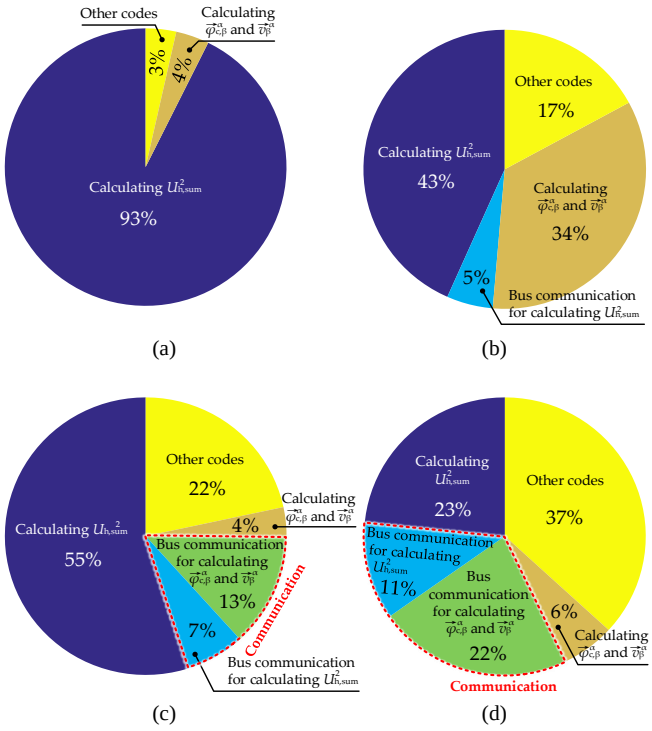

Fig. 12. Time proportions of different parts of the optimization algorithm with 100 particles using (a) only the DSP, (b) 1 HCU, (c) 1 HCU and 1 PUCU, and (d) with 4 HCUs and 1 PUCU.

the DSP-based method is 538 ms, being approximately 27 fundamental cycles. In this case, the optimization speed can be improved 24 times faster with the proposed method using 4 HCUs and 1 PUCU, being only 22.3 ms (around one fundamental cycle).

On the other hand, the acceleration process is also limited by hardware resources. As shown in Fig. 14, with the increase of the cascaded cell number, more hardware resources are required for the proposed approach. For instance, approximately 42800 LEs and 148 hardware 9-bit multipliers are required for the 10-cell VAPS PWM method with 4 HCUs and 1 PUCU. To achieve this, the two EP4CE10 FPGAs in Fig. 6 should be upgraded by two EP4CE22 FPGAs, which have more hardware resources. In practice, tradeoffs should be made when selecting the appropriate FPGA in the control system considering 1) the

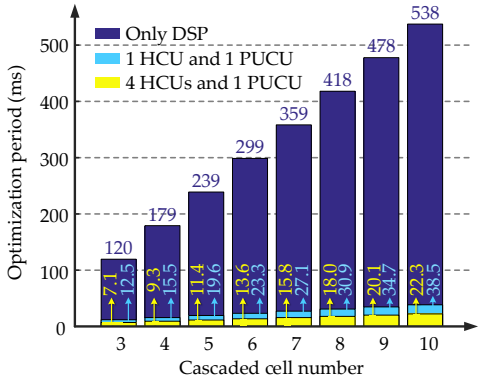

Fig. 13. Optimization speed of the conventional and the proposed computation-efficient VAPS PWM methods for *N*-cell CHB converters.

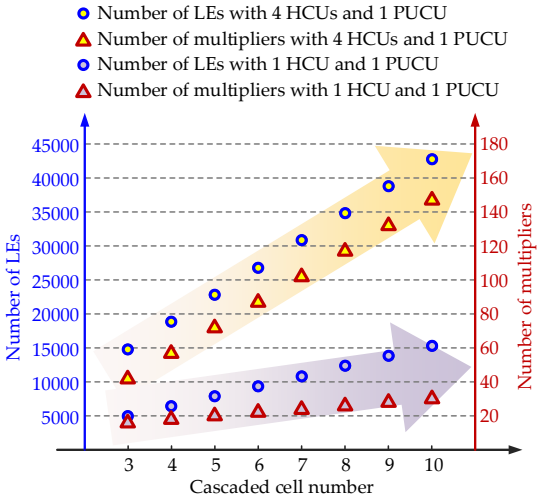

Fig. 14. Required hardware resources for *N*-cell CHB converters with the computation-efficient VAPS PWM method.

overall hardware cost, 2) the desired response speed of the VAPS PWM method (determined by the number of CUs), and 3) design margins to ensure that the FPGA can provide the sufficient hardware resources for the implementation of the proposed method.

VI. Conclusions

In this paper, a computation-efficient VAPS PWM method was proposed, which uses the parallel computing in FPGAs to reduce the time for calculating the optimal carrier PS angles, thus improving the dynamics of the VAPS PWM method. The computation speed is improved from three aspects: 1) by building multiple CUs in the FPGA, multiple particles in the PSO algorithm are calculated in parallel; 2) for each CU, multiple calculations are executed simultaneously; and 3) by simply improving the clock frequency of the FPGA, the calculation can be further accelerated. With most calculations in the optimization algorithm achieved by FPGAs, the consumed calculation time for calculating the optimal carrier PS angles is reduced to less than 10% of the time required by the conventional DSP-based approach. The performance of the proposed method is also evaluated by quantitatively analyzing

1) the time consumed by each part of the optimization algorithm and 2) the hardware requirements. The proposed computation-efficient VAPS PWM method can be easily applied to CHB converters with more cascaded cell number. Experiments on a 4-cell CHB converter have verified the effectiveness of the proposed method.

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