A Robust Testing Method for DC and AC Capacitors With Minimum Required Power Supply

Bo, Yao; Wang, Qian; Wang, Haoran; Hasegawa, Kazunori; Wang, Huai

Published in:
I E E E Transactions on Power Electronics

DOI (link to publication from Publisher):
10.1109/TPEL.2021.3130085

Publication date:
2022

Document Version
Accepted author manuscript, peer reviewed version

Letters

A Robust Testing Method for DC and AC Capacitors with Minimum Required Power Supply

Bo Yao, *Student Member, IEEE,* Qian Wang, *Member, IEEE,* Haoran Wang, *Member, IEEE,* Kazunori Hasegawa, *Member, IEEE,* and Huai Wang, *Senior Member, IEEE*

***Abstract*—This letter proposes a testing method to emulate realistic stress conditions of DC and AC capacitors, with minimum required power supply and robust operation at the presence of capacitor degradation. It is especially suitable for parameter characterization and accelerated degradation testing of high-voltage and high-ripple current power electronic capacitors. The circuit architecture of the proposed testing method and the constraints of the testing samples under given designs are discussed. Proof-of-concept experiments on both DC and AC capacitors verify the feasibility.**

***Index Terms*—DC capacitor, AC capacitor, power electronics, degradation testing**

I. Introduction

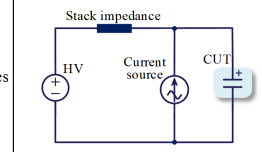
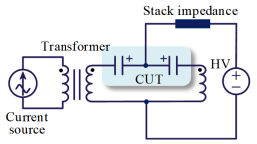
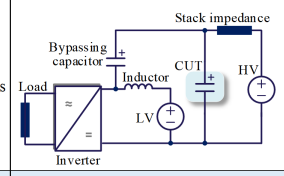
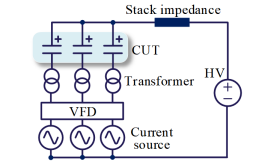
THERE are two emerging demands for capacitor testing in power electronics applications. The first is parameter characterizations under realistic operating points beyond what are provided in supplier data-sheets [1]. The testing results could help build better capacitor parametric models to optimize design margins in power converters. The second is application-oriented accelerated degradation testing under realistic voltage and current stresses [2].

Existing methods emulating realistic high power capacitor electrical stress have at least one of the two issues:

1) The power supply and power processing circuit requirements make them not viable solutions for capacitors in tens of kW to multi-MW power electronics applications. For example, the Type I [3] [4] [5] and Type II [6] [7] solutions are shown in Table I. The stacked methods need to attain DC offset for testing with AC ripple voltage and current. The current sources in the circuits need to process the full voltage and current, implying a considerable power loss as well. In Type II, the commercial ripple current testers emulate up to 500 V DC voltage, 30 V ripple voltage and 30 A ripple current for DC capacitor [7].

2) It is lack of robustness to capacitance mismatch between testing samples due to degradation or tolerance. Type III [8] and Type IV [9] solutions shown in Table I reduces the power supply requirement and power loss of the testing system. Nevertheless, low-frequency ripple current component would flow into the HV source at the presence of capacitance mismatch among Capacitors Under Testing (CUT). The mismatch could be caused by initial capacitance tolerance, different degradation rate, and open-circuit fault. It would raise the capacity requirement of the HV source in practical implementation.

TABLE I
COMPARISONS OF THE TYPICAL TEST METHODS.

	Type I [3] [4] [5]	Type II [6] [7]
Structures		
Source	Required power supply: + + + +	Required power supply: + + +
	Type III [8]	**Type IV [9]**
Structures		
Source	Required power supply: + +	Required power supply: + +
Issue	Unbalance current flow into high voltage source when the capacitance mismatchs of CUTs	

This letter focuses on proposing a method for application-oriented capacitor characterizations (i.e., measuring capacitor parameters) and degradation testing by emulating more realistic voltage and current stresses and over comes the above two issues. The contributions of the presented study are: 1) compared to existing methods, the method can provide the testing conditions of high-power electrical stress with the minimum requirements on power supply; 2) the method can control the testing conditions in a robust way at the presence of capacitance mismatch during the testing; and 3) the testing capability in terms of DC voltage, ripple current and ripple voltage ranges of the CUTs are analytically derived.

II. Proposed Capacitor Test Method

A. Circuit architecture and control structure

The circuit architecture of the proposed testing method is shown in Fig. 1. The LV power supply U_L and the power stack

B. Yao, Q. Wang, H. Wang, and H. Wang are with the Department of Energy Technology, Aalborg University, 9220 Aalborg, Denmark (e-mail:ybo@energy.aau.dk, qiw@energy.aau.dk, hao@energy.aau.dk, and hwa@energy.aau.dk).

K. Hasegawa is with Dept. of of Electrical and Electronic Engineering, Kyushu Institute of Technology, Japan (e-mail: hasegawa@ele.kyutech.ac.jp).

(Corresponding author: Qian Wang.)

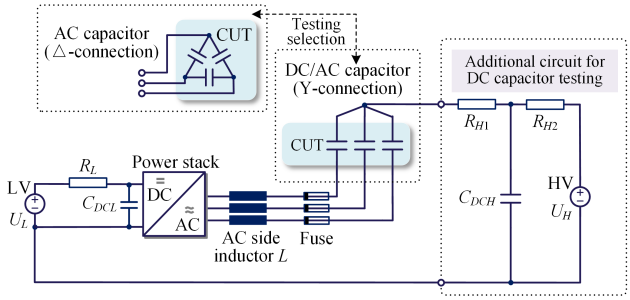


Fig. 1. Circuit architecture of the proposed capacitor testing method (for AC capacitor testing, HV source U_H, filter capacitor C_{DCH}, resistors R_{H1}, and R_{H2} can be excluded).

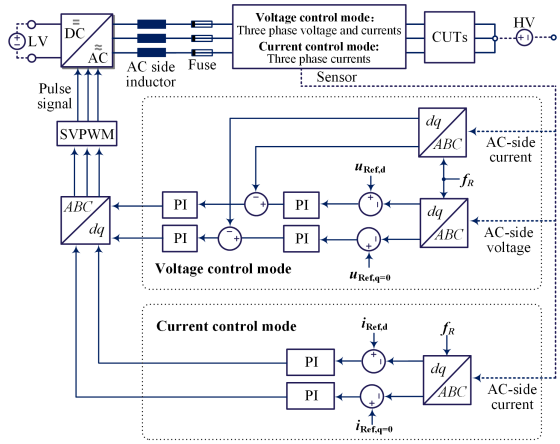


Fig. 2. Control structure of the proposed capacitor testing method.

are used to generate AC ripple voltage or current. The HV power supply U_H is used to generate DC bias voltage, which is only needed for DC capacitor testing. The AC side inductors L are used for both filtering the harmonics and boosting the AC side output voltage. The CUTs can be configured into Y- or Δ-connection for AC capacitors, and Y-connection for DC capacitors, with single or multiple such connections in parallel. Therefore, the maximum CUTs ripple voltage is limited by U_L, L, and the modulation of the power stack inverter. The maximum CUTs DC voltage is limited by U_H. The maximum CUTs ripple current is limited by the current rating of the power stack and the power rating of the LV power supply. The LV power supply compensates the power losses of the testing system, mainly from the power stack, AC inductors, and CUTs. In addition, the filter capacitors C_{DCL} and C_{DCH} are configured on both sides of the LV and HV power supplies. The startup resistor R_L is added to prevent overcurrent of the LV power supply during startup. The current limiting resistors R_{H1} and R_{H2} are added to limit the current of the HV power supply.

The control of the proposed testing method is shown in Fig. 2. Through the closed-loop controller, the control strategy is to modulate the robust three-phase current with low-frequency sinusoidal waveforms with 120° phase shift. No matter the degradation status of the CUTs during the life-cycle test, the low-frequency current are recycling internally and balanced all the time based on the feedback PI control loop, which can not be achieved by existing solutions in [8] and [9]. In the control, by maintaining the given ripple voltage $u_{Ref,d}$ or ripple current $i_{Ref,d}$, and ripple frequency f_R, so that the voltage or current stresses in AC side can keep balanced without flowing into the HV source side, even if the capacitance mismatches. Since the phase currents of the power stack can be controlled independently, the ripple current is also adaptively changed at the presence of ESR changes to maintain the voltage stresses. The fuses shown in Fig. 1 are for short-circuit protection. Depending on the testing requirement, constant ripple voltage and constant ripple current can be achieved by the voltage-mode control and current-mode control, respectively.

B. Testing capability and constraints

This part quantitatively analyzes the testing capability of the proposed testing method, including the ripple voltage and ripple current testing capability of the CUTs, and the constraints of the power stack and the LV source on the testing capability.

1) Ripple voltage and ripple current capability: The testing capability of the proposed test method can be represented by the ripple voltage and ripple current of CUTs.

In the AC side, the reactive power of the CUT Q_C and the AC inductor Q_L can be given by the RMS value of ripple current I_{ripple} and the ripple frequency f_R:

$$Q_C = \frac{I_{ripple}^2}{2\pi f_R \times C_{test}} \tag{1}$$

$$Q_L = I_{ripple}^2 \times 2\pi f_R \times L \tag{2}$$

where C_{test} is the capacitance of the CUTs and L is the inductance of the AC inductor.

The RMS value of ripple current I_{ripple} and the RMS value of ripple voltage U_{ripple} of the CUTs are given by:

$$I_{ripple} = \frac{|Q_c - Q_L|}{U_m} = \frac{U_m}{|\ \frac{1}{2\pi f_R \times C_{test}} - 2\pi f_R \times L\ |} \tag{3}$$

$$U_{ripple} = \frac{I_{ripple}}{2\pi f_R \times C_{test}} = \frac{U_m}{|\ 1 - 4\pi^2 f_R^2 \times LC_{test}\ |} \tag{4}$$

where U_m represent the RMS value of the output voltage in the power stack.

The range of I_{ripple} and U_{ripple} of CUTs is proportional to the value of U_m. Meanwhile, when the value of C_{test} and L are closer to the cut-off frequency f_c, the range of U_{ripple} and I_{ripple} are larger:

$$f_c = \frac{1}{2\pi \times \sqrt{LC_{test}}} \tag{5}$$

2) Constraint of power stack: The ripple voltage and ripple current of the CUTs are limited by the rated RMS value of output voltage in the power stack U_{o-rate}. In (2), the U_m should be less than the U_{o-rate}:

$$U_m = m \times U_L \leq U_{o-rate} \quad (m \leq 0.707) \tag{6}$$

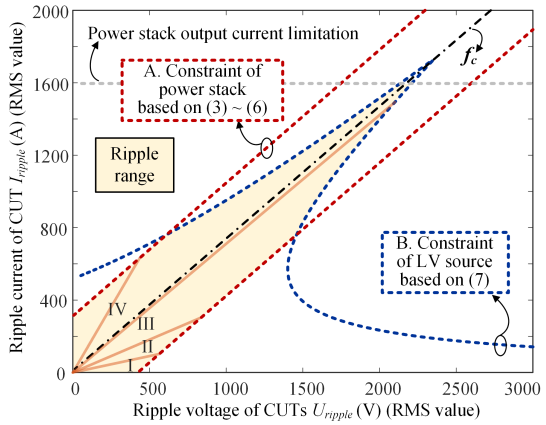


Fig. 3. Ripple voltage and ripple current testing capability. (LV source output voltage and current:600V, 20A; Power stack output voltage (RMS), current (RMS), and efficiency: 530V, 1600A, 97%; Ripple frequency: 50Hz; Inductance: 2.5mH; CUTs value in Case I to Case IV: 1mF, 2mF, 4mF, 8mF.)

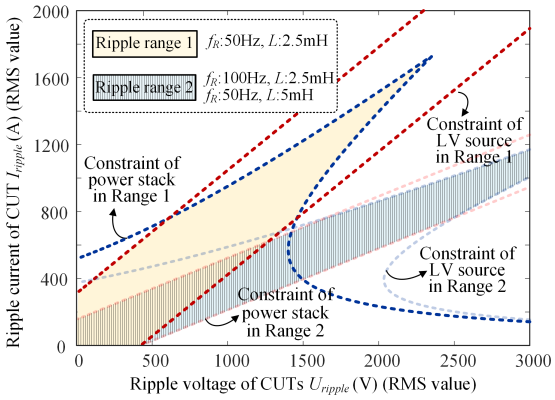


Fig. 4. Impact of different ripple frequency and inductance on ripple voltage and ripple current testing capability. (specific conditions are same as that in Fig. 3)

where m and U_L represent the utilization rate of DC-link voltage in SVPWM modulation [10] and the LV output voltage, respectively.

3) Constraint of LV source: The testing capability of the ripple current is also affected by its the output power of the LV power supply P_{out}, which is limited by the output voltage U_L and the rated current I_{rate} of the LV source. It can be expressed as:

$$P_{out} \approx I_{ripple}^2 R_{total} + (1-\eta) I_{ripple} U_m \leq U_L \times I_{rate} \quad (7)$$

where the η is the efficiency of the power stack and inductors at the specific operating condition of interest, and the R_{total} represents the Equivalent Series Resistance (ESR) of the CUTs.

III. Testing Capability Analysis and Benchmark

This section presents the testing capability canalysis and benchmark of proposed testing methods, with specifications for high power capacitor [11].

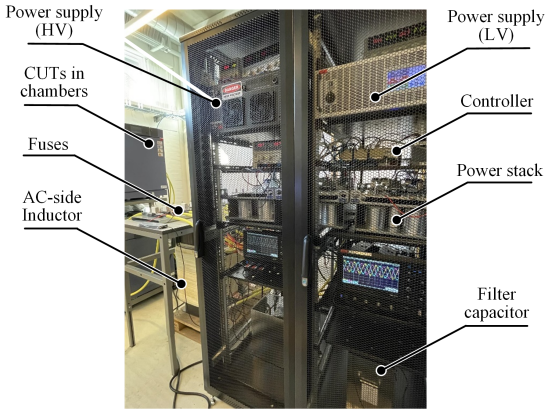


Fig. 5. The implemented AC and DC capacitor testing setup based on the proposed method.

TABLE II
EXPERIMENTAL PLATFORM PARAMETERS.

CUTs setup	AC capacitor (Δ-conection)			DC capacitor (Y-conection)		
AC-side inductor L	2.5mH					
Ripple frequency f_R	50Hz					
Efficiency η	96.5%					
LV source voltage U_L	600V					
HV source voltage U_H	0V			2800V		
Capacitance of CUTs	(75μF*3)*9			220μF*2+40μF		
Ripple amplitude voltage	1200V			500V		
	Calculation	Testing	Error	Calculation	Testing	Error
Ripple amplitude current	441A	440A	0.2%	75.4A	75.2A	0.3%
LV source output current	7.6A	7.8A	2.6%	1.31A	1.35A	2.9%

A. Testing capability analysis

According to the constraints in Section III, the testing capability of a studied case specification is shown in Fig. 3. The ripple voltage and ripple current testing range of different CUTs can be obtained in (3) and (4). (6) and (7) respectively express the constraints of the power stack and LV source. The proposed method can boost the output voltage of the power stack from 530 V to 2200 V in maximum through the series circuit of the CUTs and inductors. Meanwhile, higher efficiency, larger the rated output voltage of the power stack and larger current of the LV source are beneficial to extend the tesing ranges.

The influence of different parameters on the ripple voltage and ripple current testing range is further analyzed and shown in Fig. 4. The power stack constraint in (6) and the LV source constraint in (7) on the test capability is affect by the ripple frequency and inductance value. Different ripple testing capabilities can be obtained by selecting different test frequencies and different inductances in this method.

A and B represent voltage and current respectively.

B. Benchmark with existing test methods

1) Required power supply: Compared with the existing test mothods, the proposed mothod has the minimum required power supply. In the case of emulating the same ripple current and ripple voltage, the required power supply for single set of the CUTs in the proposed test method only accounts for 1% in Type I and Type II, 15% in the Type III and 50% in the Type IV, as shown in Fig. 6 (a). Compared to Type I and Type II, the power supply of the proposed method only

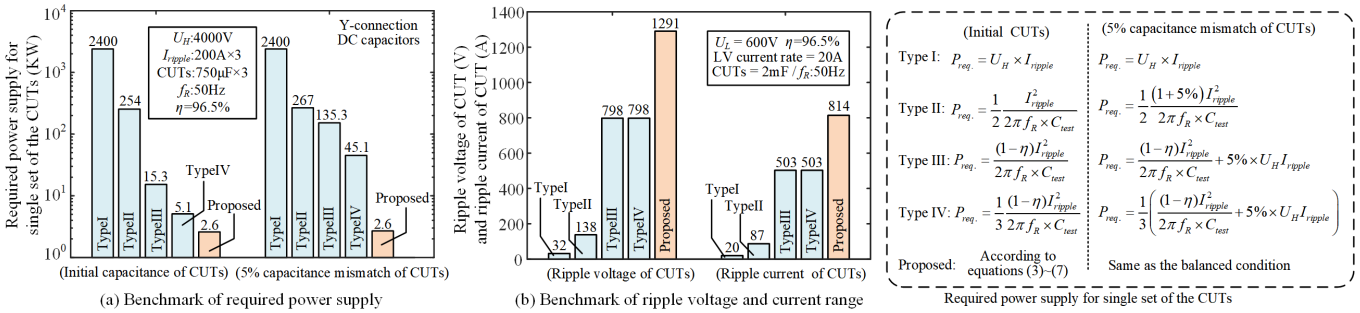


Fig. 6. Benchmark of existing test methods in [3]-[9] and the proposed test method. ($P_{req.}$ represents the required power supply for single set of the CUTs; η represents the efficiency of converters, transformers, and inductors; U_H and U_L respectively represent the output voltage of high-voltage power supply and low-voltage power supply; C_{test}, f_R, and I_{ripple} represent the capacitance, ripple frequency and ripple current of CUTs, respectively.)

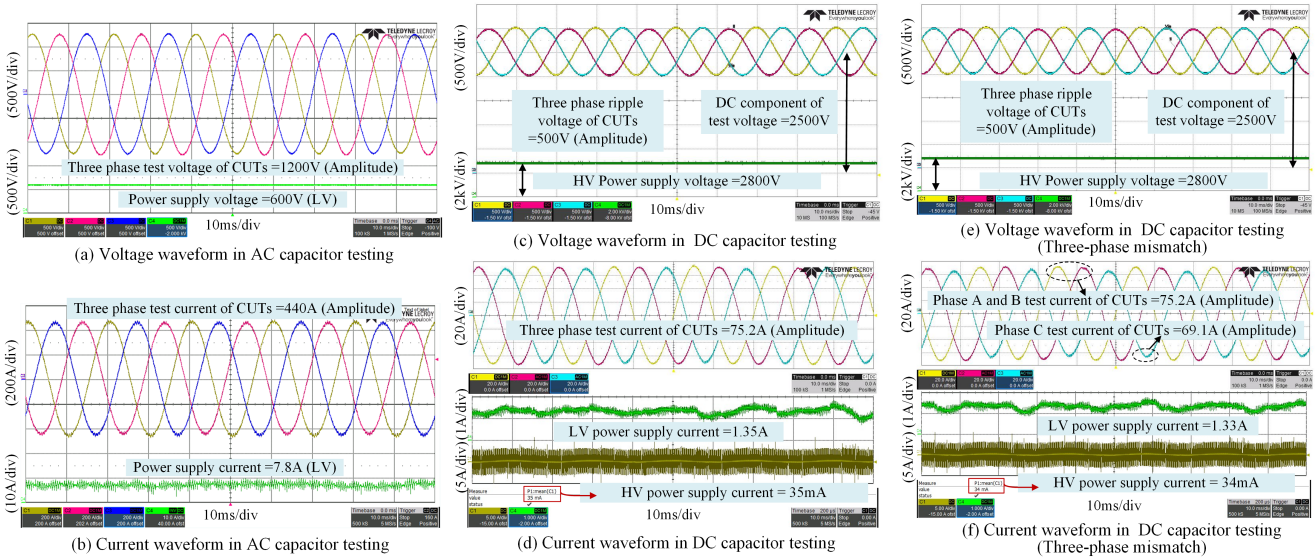


Fig. 7. Experimental testing waveforms.

need to deal with the power loss of component in the system. Therefore, the required power supply is much smaller than the Type I and Type II methods. Compare Type III and Type IV, in the proposed test method, due to the reactive power provided by the AC inductor, the output voltage of the converter is lower than the tested ripple voltage. Therefore, the required power supply is still less than the Type III and Type IV methods. Meanwhile, when the degradation rate of the DC capacitor is mismatched, the test system in Type III and Type IV cannot handle the three-phase unbalanced component, so that the unbalanced current flows into the HV source. In the proposed method, the ripple current is recycling in the AC-side internally all the time through the closed-loop controller, which need the minimum required power supply.

2) Ripple voltage and current testing range: Compared with the existing test mothods, the proposed mothod has a wider range of the ripple voltage and current. In the case of choosing the same specification CUTs and power sources, the ripple voltage and current capability of the proposed mothod are ten times higher than Type I and Type II, and 60% higher than Type III and Type IV, as shown in Fig. 6 (b). Type III, Type IV and the proposed mothod have improved the test capability of ripple voltage and current beacause the reactive power circulate between the power stack and the AC side circuit in their structures. In the proposed mothod, the inductor and the CUTs form the series circuit, which can obtain a higher ripple voltage than the output voltage of the power stack, thus having a greater test capability of ripple current and ripple voltage than Type III and Type IV.

IV. Experimental Verification

The experimental platform is shown in Fig. 5, and its main parameters are shown in Table II. Fig. 7 (a) and (b) show the waveform of AC capacitor testing. The ripple voltage and current of the CUTs are stable under three-phase balanced condition. At this time, the total reactive power of the CUTs reaches 528 kVA, while the low-voltage power supply only needs to provide 4.68 kW of power. As shown in Fig. 7 (c) (d), when the three-phase capacitors are balanced, the ripple voltage and current of the DC test capacitor are also stable. In Fig. 7 (e) and (f), the branch capacitor of one phase is disconnected to simulate the aging and failure of the CUTs in the DC capacitor testing. The capacitance value of one phase CUTs is reduced from 480 μF to 440 μF. When the

capacitance of the CUTs mismatchs, the ripple voltage and ripple current of the CUTs and the output current of the power supplies are still stable. Meanwhile, the HV source only needs to provide the mA current and is not affected by the capacitance mismatch. Therefore, the test bench can generate stable ripple current and ripple voltage for the CUTs, and maintain the same required power supply, even if the CUTs degrades and has open-ciruit during the testing. Further comparing the theoretical calculation with the test results in Table II, the error of ripple current and LV source output current between the calculated value and the test results is less than 3%, indicating that the theoretical analysis of the proposed method is reasonable.

V. Conclusion

This letter proposes a robust and scalable testing method for DC and AC capacitors with minimum required power supply, which can to emulate the realistic voltage and current stresses in the high voltage and high current application.

Compared to the solutions in [8] and [9], it extends the ripple voltage and ripple current ranges by 60% and reduce the power loss of the testing system by 50%, based on a case study of Fig. 6. Proof-of-concept experiments have verify the concept of the proposed method for DC capacitors and AC capacitors. The LV source only needs to supply the power losses of the overall testing system and the current of the HV supply is in the range of mA. A testing under capacitance mismatch among the three-phase capacitor DUTs proves the robustness of the testing method. This test method can provide a suitable choice for the parameter evaluation, degradation and lifetime testing of high power capacitors.

References

[1] S. Liu, Z. Shen, and H. Wang, "Safe operating area of dc-link film capacitors," *IEEE Transactions on Power Electronics*, vol. 36, no. 10, pp. 11 014–11 018, 2021.

[2] H. Wang and F. Blaabjerg, "Reliability of capacitors for dc-link applications in power electronic converters—an overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sep./Oct. 2014.

[3] K. Abdennadher, P. Venet, G. Rojat, J.-M. Rétif, and C. Rosset, "A real-time predictive-maintenance system of aluminum electrolytic capacitors used in uninterrupted power supplies," *IEEE Trans. Ind. Appl.*, vol. 46, no. 4, pp. 1644–1652, Jul./Aug. 2010.

[4] D. Menzi, D. Bortis, G. Zulauf, M. Heller, and J. W. Kolar, "Novel igse-c loss modeling of x7r ceramic capacitors," *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13 367–13 383, 2020.

[5] S. Coday and R. C. Pilawa-Podgurski, "High accuracy calorimetric measurements and modeling of ceramic capacitor losses under large ripple operation," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 188–194.

[6] M. Makdessi, A. Sari, P. Venet, P. Bevilacqua, and C. Joubert, "Accelerated ageing of metallized film capacitors under high ripple currents combined with a dc voltage," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2435–2444, May. 2015.

[7] "Ripple current tester model 11800/11801/11810." Chroma ATE Inc, http://www.chromaate.com/product/11800_11801_11810_Ripple_Current_Tester.htm, 2012.

[8] K. Hasegawa, I. Omura, and S.-i. Nishizawa, "Design and analysis of a new evaluation circuit for capacitors used in a high-power three-phase inverter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2679–2687, May. 2016.

[9] X. Wang, M. Karami, and R. M. Tallam, "Test fixtures to apply variable dc bias and ac ripple current for reliability testing of electrolytic capacitors," *IEEE Trans. Ind. Appl.*, vol. 55, no. 4, pp. 4073–4079, Jul./Aug. 2019.

[10] H. Djeghloud, H. Benalla, and A. Bentounsi, "Application of svpwm to three-level voltage and current inverters," in *44th Int. Univ. Power Eng. Conf.*, Sep. 2009, pp. 1–5.

[11] B. Yao, X. Ge, D. Xie, S. Li, Y. Zhang, H. Wang, and H. Wang, "Electrothermal stress analysis and lifetime evaluation of dc-link capacitor banks in the railway traction drive system," *IEEE J. of Emerg. Se. Topics in Power Electron.*, vol. 9, no. 4, pp. 4269–4284, 2021.