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Model-Based Design for Reactors of the Modular Multilevel Converter

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***Abstract*—For complex power electronic converters, typical design approaches divide the system into multiple independent subsystems without sufficiently considering the interactions among them. In this paper, a model-based approach for sizing the reactors of the modular multilevel converter (MMC) is proposed. The proposed method quantitatively considers the interactions between the reactor sizing and other design parameters, such as power ratings, protection schemes, and component-level short-circuit capabilities. Meanwhile, three deterministic factors are provided in this paper for sizing reactors to ensure enough robustness during extreme situations instead of the heuristic factor in the existing work. The quantified interactions presented in this paper also reveal that a proper over-rating of the active components is able to reduce reactance, increase efficiency, and improve power density. The proposed method not only serves as a quantitative design tool for the MMC, but also emphasizes the significance of the modeling of the interactions in the model-based design. Finally, the effectiveness of the proposed method is validated by simulations and experiments. This paper is also accompanied by software codes for reproducibility.**

***Index Terms*—Limiting reactor, model-based design, modular multilevel converter (MMC), sizing criteria, short circuit**

I. Introduction

Modular multilevel converters (MMC) are complex systems, composed of many components, and exposed to critical loads [1]. Thereby, a detailed design of its components is of preeminent importance to achieve satisfactory performance with a constraint design margin while ensuring sufficient robustness during extreme situations (e.g., fault transients). Although many efforts have been devoted to achieving a better design of the MMC [2]–[4], most of the existing methods divide the system into multiple independent sub-systems and consider few interactions among them. As shown in Fig. 1, the design based on the independent analysis often ignores these inherent interactions, thereby leading to introducing some empirical factors and intensive trial-and-errors. As such, a better model-based design considering these interactions is preferable to address this challenge.

One specific research gap of the model-based design of the MMC is the reactor sizing considering pole-to-pole (P2P) short-circuit faults. The reactor is significant to limit the fault current and protect the power semiconductor devices and other critical components from catastrophic damages [5]. However, the existing design methods of the reactor sizing ignore its inherent interactions with other parameters, such as power ratings, the selection of active components, protection schemes, etc., which leads to using the following heuristic criterion to size reactor [6], [7], namely,

$$L_0 = \frac{U_{\rm dc}}{2\lambda_{\rm emp}}, \tag{1}$$

where $U_{\rm dc}$ is the DC bus voltage, L_0 is the arm inductance, and $\lambda_{\rm emp}$ is an empirical factor of the pre-set maximum current rise rate which is based on the heuristic experience. For instance, the existing studies provide different values of $\lambda_{\rm emp}$, e.g., a wide range of 2-10 kA/ms [6], 100 kA/ms [7], and 1.3 kA/ms [8]. These empirical factors may be applicable for the specific projects, but applying them to different projects are problematic. Moreover, the design criterion of (1) is over-simplified, which ignores that the MMC system typically has multiple reactors and different fault transient stages [9], [10]. Thus, a revisit of the limiting reactor sizing is necessary.

To successfully model the interactions between the reactor sizing and other design parameters, three specific challenges are intertwined from the system-level short-circuit behaviors and component-level robustness. Specifically, the P2P fault transient of the MMC is firstly highly nonlinear and has multiple stages. The previous studies provide dedicated circuit analysis before and after the IGBT blocking [9], [10], but the analysis of sizing the limiting reactors and their interactions with the power semiconductor devices and other design parameters are yet to discuss sufficiently. Moreover, the fault transient of the MMC involves multiple power

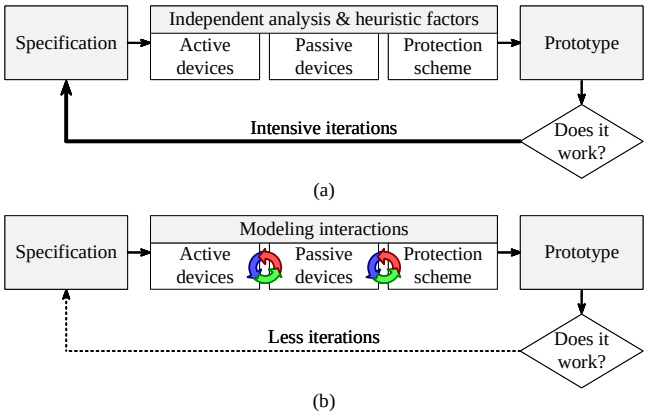

Fig. 1. Model-based designs: (a) design based on independent analysis and heuristic experience and (b) design with considering the interactions among different sub-systems.

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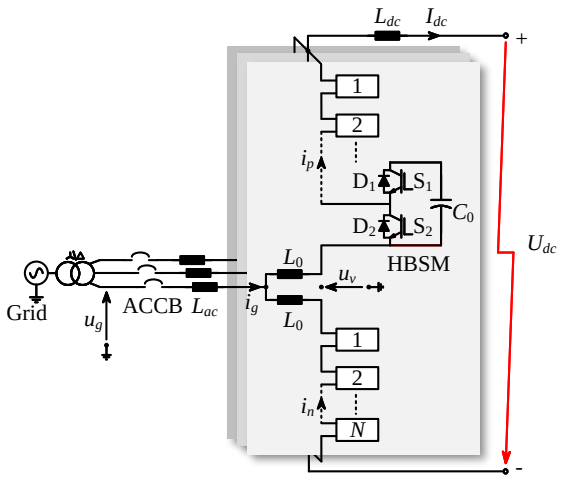


Functions	L_0	L_{ac}	L_{dc}
Limit the short-circuit current of DC loop	✓		✓
Limit the short-circuit current of AC loop	✓	✓	
Limit circulating current	✓		
Contribute interface to grid	✓	✓	
Filter harmonics	✓	✓	

Fig. 2. A half-bridge submodule (HBSM)-based MMC subjected to a pole-to-pole DC fault.

semiconductor devices, such as IGBTs and diodes. These components not only have different time sequences during the fault transient but also have distinct short-circuit capabilities. Page *et al.* [11] propose a simulation-based method to size the limiting reactors considering diodes only. However, an analytical method considering different components is still missing. Finally, multiple reactors are involved in the grid-connected MMC system shown in Fig. 2, which all have different roles. The existing studies often study these functions independently, a comprehensive investigation is missing. Therefore, to address the aforementioned three challenges, the sizing of the limiting reactors should comprehensively bridge the knowledge between the system-level short-circuit behaviors and the capabilities of different components.

This paper bridges the analytical relationship between the system-level reactor sizing and the device-level robustness of power semiconductor devices considering a P2P short-circuit. The established analytical model quantifies the interactions between reactor sizing and other design parameters, such as power ratings, protection schemes, and component-level short-circuit capabilities. Meanwhile, three deterministic factors are provided in this paper to take place the heuristic factor in the existing work. The proposed method not only provides guidelines to better size the hardware parameters and adjusts the protection settings of the MMC, but also emphasizes the modeling of the interactions in the model-based design. This paper is also accompanied by software codes [12].

II. Configuration of an HBSM-based MMC and Time Sequence of Pole-to-Pole DC Fault

Fig. 2 shows a typical configuration of an MMC with ACCB protection. The MMC consists of six arms. Each arm is

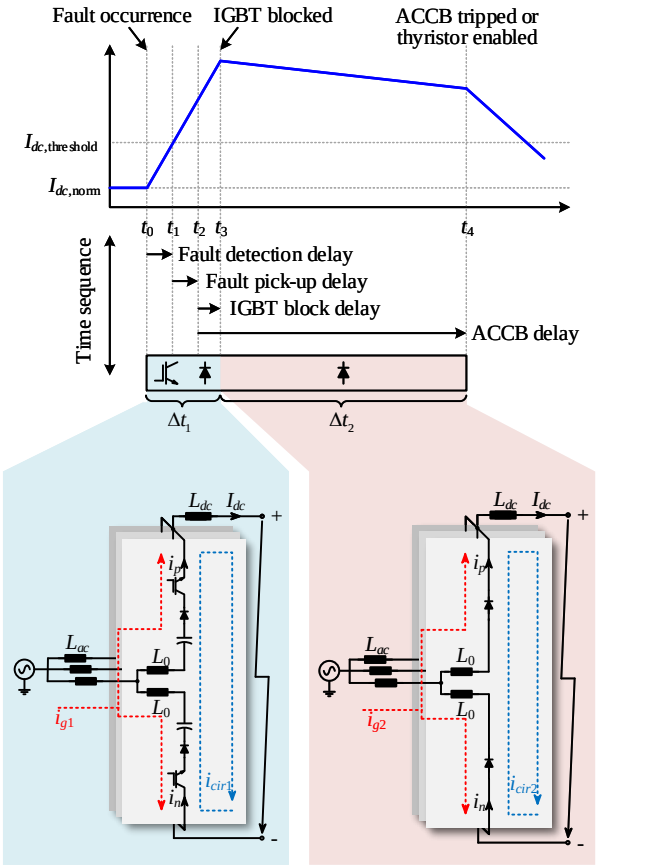


Fig. 3. Time sequence of the P2P short circuit, the conducting power semiconductor devices, and the corresponding equivalent circuits.

comprised of N identical series-connected HBSMs with two different power semiconductor devices (i.e., two IGBTs and two diodes) in each SM and an arm reactor L_0.

In addition to the arm reactors, the MMC has two other reactors, i.e., the AC reactor $L_{\rm ac}$, and the DC reactor $L_{\rm dc}$ with their functions summarized in Fig. 2. All of these reactors contribute to limiting the short-circuit fault current. The difference is that L_0 and $L_{\rm dc}$ suppress the DC-loop short-circuit current, while L_0 and $L_{\rm ac}$ suppress the fault current of the AC loop. To focus on the short-circuit limiting of the reactors, two equivalent inductances in DC and AC loops are given by

$$L_{\rm eqdc} = \frac{2}{3}L_0 + L_{\rm dc},\ L_{\rm eqac} = \frac{1}{2}L_0 + L_{\rm ac}. \tag{2}$$

Moreover, a P2P short-circuit fault interacts with multiple power semiconductors and limiting reactors. To investigate their electrical stresses during different fault transients, this paper is in accordance with the industry report [13] to classify the short-circuit transient into the following stages (see Fig. 3)

1) Fault detection delay $[t_0, t_1)$*:* A P2P short-circuit fault occurs at t_0 and is detected till reaching a threshold at t_1.

2) Fault pick-up delay $[t_1, t_2)$*:* Fault pick-up time is necessary in practice to avoid measurement errors. When the measured fault signal exceeds the threshold for a period, the blocking signal is triggered at t_2 and the controller sends

protection commands to IGBTs and ACCBs. This paper selects the fault pick-up delay of 50 μs according to [13].

3) IGBT blocking delay $[t_2, t_3)$*:* When the blocking signal of the MMC is triggered, with a 20 μs delay, the IGBTs are blocked. This time delay considers the multiple control stage of the MMC and the delay of the devices themselves [13].

4) Diode conduction only $[t_3, t_4)$*:* The IGBTs are fully blocked at t_3 while the ACCB has not been fully triggered. During this period, diodes conduct the fault current only, which stresses the diode seriously.

5) ACCBs are tripped $[t_4, \infty)$*:* The ACCBs are tripped at t_4, so that the fault is cleared.

Thus, a comprehensive reactor design of the MMC has to consider the interactions of the multiple reactors, different types of power semiconductors, and the aforementioned time sequence of the short circuit transient.

III. Analysis of Short-Circuit Fault Stress on the MMC Components

This section serves to analytically bridge the system-level short-circuit behaviors and the component-level electrical stresses. By contrast to the previous studies focusing on the short circuit transient on DC grids [14]–[16], this section aims to obtain the electrical stresses of the major power semiconductor devices. Two fault periods are defined as shown in Fig. 3. Fault period Δt_1 is related to both IGBTs and diodes, and fault period Δt_2 is related to the diodes only. Both of these periods reflect the protection settings of the system.

A. Period Δt_1: Fault Occurrence to IGBT Blocking $[t_0, t_3)$

At the moment of fault occurrence (t_0), the IGBTs have not been blocked yet. As shown in Fig. 3, the fault current consists of a circulating current i_{cir1} (dominated by SM capacitors discharging) through the DC loop and AC fed-in current i_{g1}, which are introduced as follows.

1) DC loop: the SM capacitor discharge current can be described as a second-order form in Appendix (A1). Considering the worst case with negligible resistance and short Δt_1, the current is simplified as

$$i_{\text{cir1}}(t) = \frac{1}{3}[\frac{U_{\text{dc}}(t-t_0)}{L_{\text{eqdc}}} + I_{\text{dc}}(t_0)], \tag{3}$$

where $I_{\text{dc}}(t_0)$ is the initial DC current.

2) AC loop: the AC loop stays the same at the moment of the fault occurrence, where the AC voltage $u_{\text{g}}(t)$ and current $i_{\text{g1}}(t)$ are described by

$$u_{\text{g}}(t) = \hat{U}_{\text{g}}\sin(\omega t + \alpha), \tag{4}$$

$$i_{\text{g1}}(t) = \hat{I}_{\text{g1}}\sin(\omega t + \alpha - \varphi_c), \tag{5}$$

where $\hat{U}_{\text{g}}$ and $\hat{I}_{\text{g1}}$ represent the magnitudes of the grid voltage and current, respectively. ω is the synchronous angular frequency, α is the phase angle at the fault occurrence t_0, and φ_c is the initial grid phase angle.

3) Electrical stresses of the components: the AC current of (5) is equally split into the upper and the lower arms in this stage. Considering that the variation of $i_{g1}(t)$ is negligible with a short Δt_1, the arm current in the worst scenario is expressed as

$$i_{\text{p1}}(t)_{\text{sim,max}} = \frac{1}{3}[\frac{U_{\text{dc}}\cdot(t-t_0)}{L_{\text{eqdc}}} + I_{\text{dc}}(t_0)] + \frac{1}{2}\hat{I}_{\text{g1}}. \tag{6}$$

B. Period Δt_2: IGBT Blocking to ACCB Tripping $[t_3, t_4)$

1) DC loop: IGBTs are blocked at t_3. The equivalent circuit is changed as shown in Fig. 3. With a τ_{dc} defined in Appendix, the circulating current i_{cir2} is dominated by a freewheeling current through the DC loop and is expressed as

$$i_{\text{cir2}}(t) = i_{\text{cir1}}(t_3)e^{-\frac{t-t_3}{\tau_{\text{dc}}}}. \tag{7}$$

2) AC loop: the AC voltages are all applied to the AC and arm reactors. Consequently, the AC current is described as the transient circuit, which is

$$\begin{aligned} i_{\text{g2}}(t) =& \hat{I}_{\text{g2}}\sin[\omega(t-t_3)+\alpha-\varphi]+ \\ & [\hat{I}_{\text{g1}}\sin(\alpha-\varphi_c) - \hat{I}_{\text{g2}}\sin(\alpha-\varphi)]e^{-\frac{t-t_3}{\tau_{\text{dc}}}}, \end{aligned} \tag{8}$$

in which $\varphi = \arctan(\omega L_{\text{eqac}}/R_{\text{eqac}})$. R_{eqac} is the AC-loop equivalent resistance. $\hat{I}_{\text{g2}}$ and τ_{ac} are given by

$$\hat{I}_{\text{g2}} = \frac{\hat{U_{\text{g}}}}{\sqrt{R_{\text{eqac}}^2 + (\omega L_{\text{eqac}})^2}}, \tau_{\text{ac}} = \frac{L_{\text{eqac}}}{R_{\text{eqac}}}. \tag{9}$$

3) Electrical stresses of the components: the arm current within the period Δt_2 is composed of (7) and half of (8). Considering the worst case, it can be obtained that $\omega L_{\text{eqac}} \gg R_{\text{eqac}}$. The negligible R_{eqdc} and R_{eqac} cause large τ_{dc} and τ_{ac}. The maximum arm current is simplified as

$$\begin{aligned} i_{\text{p2}}(t)_{\text{sim\_max}} =& \frac{1}{3}[\frac{U_{\text{dc}}(t_3-t_0)}{L_{\text{eqdc}}} + I_{\text{dc}}(t_0)] \\ & - \frac{1}{2}\frac{\hat{U}_{\text{g}}}{\omega L_{\text{eqac}}}\cos[\omega(t-t_3)] + \frac{1}{2}(\hat{I}_{\text{g1}} + \frac{\hat{U}_{\text{g}}}{\omega L_{\text{eqac}}}). \end{aligned} \tag{10}$$

In summary, the maximum electrical stress on the components is combined with (6) and (10), which is expressed by

$$i(t)_{\max} = \begin{cases} i_{\text{p1}}(t)_{\text{sim,max}}, & t \in [t_0, t_3) \text{ or } \Delta t_1 \\ i_{\text{p2}}(t)_{\text{sim,max}}, & t \in [t_3, t_4) \text{ or } \Delta t_2. \end{cases} \tag{11}$$

C. Simulation Verification of the Analytical Models

The aforementioned analytical models are established based upon a certain simplification, e.g., the active power is constant, the resistance is negligible, etc. For the sake of verifications, a 60-MVA MMC-HVDC system with its parameters listed in Table I is used for simulations. As shown in Fig. 4(a), when a P2P DC fault occurs at $\alpha = 0$ and $\varphi_c = 0$, the simulation results and analytical calculations are closely matched. Meanwhile, Fig. 4(b) has similar results with changed α and φ_c. These results verify the effectiveness of the established models.

As the fault current is varied with fault occurrence (modeled by α) and power factor (φ_c), a design with sufficient

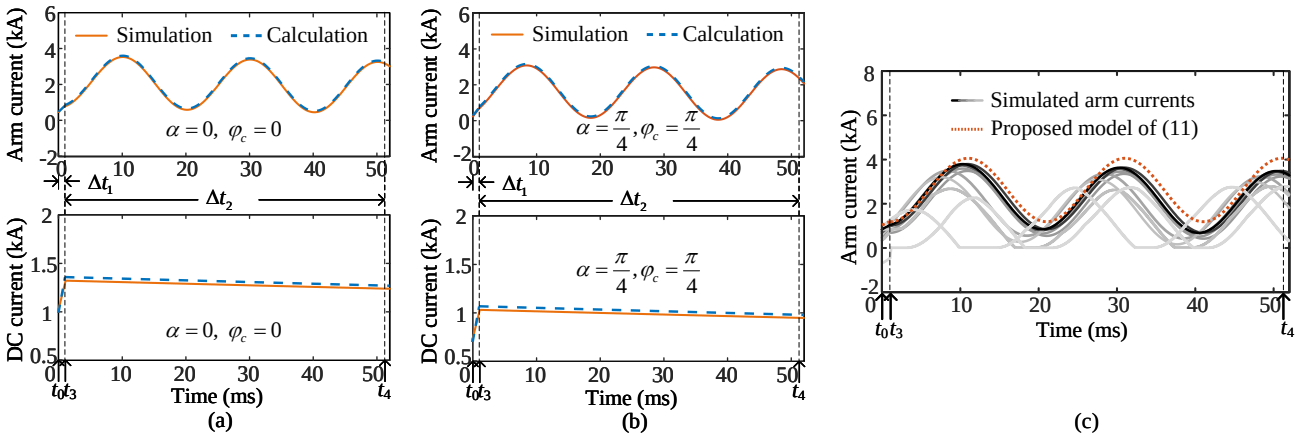


Fig. 4. Comparison of the established analytical models and simulations: (a) $\alpha = 0$ and $\varphi_c = 0$, (b) $\alpha = \frac{\pi}{4}$ and $\varphi_c = \frac{\pi}{4}$, and (c) the proposed model described by (11) can represent the envelope of the arm currents under different fault occurrence α and power factors φ_c.

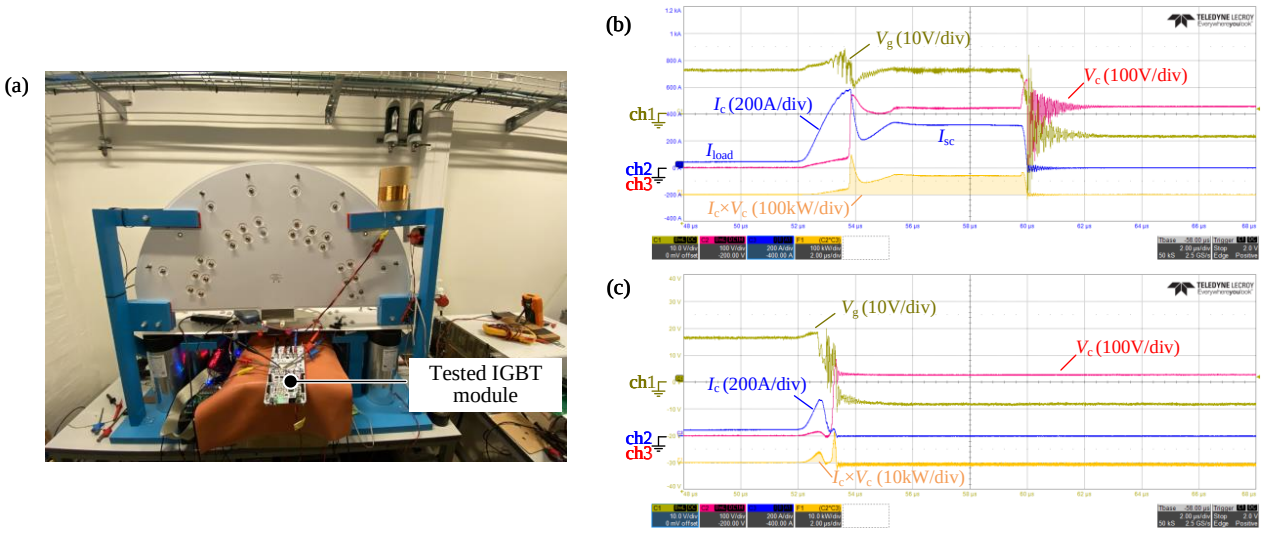


Fig. 5. Type II short-circuit measurements: (a) the photo of the tested platform, (b) waveform of Type II short circuit with de-saturation protection only, and (c) turn off IGBT before reaching the saturation current (I_{SC}) (V_C - collector-emitter voltage, I_C - collector current, V_g - gate voltage).

TABLE I
MMC PARAMETERS FOR BOTH SIMULATIONS AND HARDWARE-IN-LOOP EXPERIMENTS

Symbol	Parameter	Value and Unit
S_N	Power rating	60 MVA
$\hat{U}_g$	Grid voltage amplitude	28.3 kV
$\hat{I}_{g1}$	Grid current amplitude	1.41 kA
f	Grid frequency	50 Hz
U_{dc}	DC bus voltage	60 kV
N	Number of SMs per arm	20
C_0	SM capacitance	2.65 mF
L_0	Arm reactor	50 mH
R_0	Arm resistance	0.02 Ω
L_{dc}	DC reactor	100 mH
L_{ac}	AC reactor	6.4 mH
R_{ac}	AC filter resistance	0.1 Ω
Δt_1	Fault period 1*	1.07 ms
Δt_2	Fault period 2	50 ms

*Includes the fault detection time of 1 ms [17], fault pick-up time of 50 μs [13], and IGBT block delays of 20 μs [13]

robustness must consider the worst-case scenario. By varying both α and φ_c, the arm currents under different conditions are shown in Fig. 4(c). The proposed model described by (11) can represent the envelope of different cases. Thus, the established maximum arm current can be used to size the hardware parameters in the next section.

IV. SHORT-CIRCUIT CAPABILITIES OF POWER SEMICONDUCTORS

To ensure enough robustness for the power devices of the MMC, this section further bridges the above established electrical stresses to the short-circuit capabilities of the power semiconductor devices.

A. IGBT

A data sheet of the IGBT typically provides the data for the Type-I short-circuit fault only, which has zero current at the moment of fault happening. However, the short circuit in the MMC often occurs when the IGBT is already conducting a large current, which is a more severe Type-II short circuit [18]. Moreover, the short-circuit current of the MMC is generated by N HBSMs in series, which is even more severe than the Tyepe-II short circuit in two-level converters.

In the existing literature, the sizing of the limiting reactors usually does not take the short-circuit capability of the IGBT

into consideration, because their holding a view that the de-saturation of the IGBT can protect the device by itself. However, based on the short circuit testing platform [Fig. 5(a)], the waveform of Type II short circuit applying the de-saturation protection has high stresses on the tested device [see Fig. 5(b)]. Specifically, when the de-saturation current is reached, the collector-emitter voltage $V_{\rm C}$ shows a positive slope ($\mathrm{d}v/\mathrm{d}t$) up to and even beyond the DC-link voltage. This positive $\mathrm{d}v/\mathrm{d}t$ causes a displacement current through the inevitable parasitic Miller capacitance of the IGBT, overcharging the gate and consequently leading a higher V_g and short-circuit current amplitude. The high overvoltage and overcurrent generate massive peak power, which is around 150 kW at the maximum. Thus, this paper holds a view that an effective sensing and protection to turn the IGBTs off before reaching the saturation current ($I_{\rm SC}$) is necessary. The case applying this strategy is shown in Fig. 5(c). The peak dissipation is only 10 kW and the period is within 2 μs only, which from the perspective of the safe operating area protects the IGBT against the stresses.

Accordingly, a criterion for IGBTs of the MMC is selected as

$$I_{\rm SC} \geq i_{\rm p1}(t_3), \tag{12}$$

where $I_{\rm SC}$ refers to the IGBT's datasheet. Substituting (11) into (12), the sizing of the DC-loop equivalent inductance has the following criterion

$$L_{\rm eqdc} \geq \frac{U_{\rm dc}}{\lambda_{\rm dc1}}, \tag{13}$$

where

$$\lambda_{\rm dc1} = \frac{3(I_{\rm SC} - I_0)}{\Delta t_1}\ [\mathrm{A/s}], \tag{14}$$

$$I_0 = \frac{1}{3} I_{\rm dc}(t_0) + \frac{1}{2}\hat{I}_{\rm g1}. \tag{15}$$

In (13)-(15), the proposed equivalent current rise rate $\lambda_{\rm dc1}$ comprehensively consider three aspects, i.e., power rating related I_0, protection setting Δt_1, and the short-circuit capability of the IGBT $I_{\rm SC}$. This addresses the existing study of (1) relies on empirical $\lambda_{\rm emp}$ without analytical expressions.

B. Diodes

By contrast to the IGBTs, diodes are not self-controlled. The short-circuit capability of the diodes is limited by the thermal stress introduced by the surge current. However, many parameters affect the peak junction temperature of the diode during short circuits [19], such as initial diode junction temperature, short circuit duration, forward voltage, thermal impedance, etc. Thus, the standard method [20] introduces the surge current integral I^2t to quantify the short-circuit capability of the diode, which is expressed as

$$I^2 t = \int_0^{t_p} i^2(t) dt, \tag{16}$$

where $i(t)$ is the conducting current for the duration t_p. In other words, if the short-circuit current stresses are kept within the given limits, the diode will stay within the guaranteed characteristics. Therefore, the MMC needs to fulfill the following condition:

$$I^2 t_{\rm (diode)} \geq \int_{t_0}^{t_3} i_{\rm p1}^2(t) dt + \int_{t_3}^{t_4} i_{\rm p2}^2(t) dt, \tag{17}$$

where $I^2t_{\rm (diode)}$ refers to the diode's datasheet provided by the manufacturer. Substituting the established diode stresses of (11) into (17), the following two criteria are deduced as

$$L_{\rm eqdc} > \frac{U_{\rm dc}}{\lambda_{\rm dc2}}, \text{and } L_{\rm eqac} \geq \frac{\hat{U}_{\rm g}}{\lambda_{\rm ac}}, \tag{18}$$

where

$$\lambda_{\rm dc2} = (\sqrt{a_1 I^2 t_{\rm (diode)} - a_2 I_0^2} - a_3 I_0)/\Delta t_1, \tag{19}$$

$$\lambda_{\rm ac} = \omega[\sqrt{b_1\eta^2 + b_2\eta I_0 + b_3 I_0^2 + b_4 \omega I^2 t_{\rm (diode)}} - b_5(I_0 + \frac{1}{3}\eta)], \tag{20}$$

where the parameters a_1, a_2, a_3, b_1, b_2, b_3, b_4, b_5 and η are related to Δt_1 and Δt_2 as given in the Appendix. The proposed two additional equivalent current rise rates $\lambda_{\rm dc2}$ and $\lambda_{\rm ac}$ consider the ratings of the MMC, the protection settings Δt_1 and Δt_2, and short-circuit capability of the diodes $I^2t_{\rm (diode)}$ as well.

C. Summary of the Sizing Criteria of Limiting Reactors

The proposed three sizing criteria of the limiting reactors are summarized in Fig. 6. The proposed method comprehensively considers three aspects, i.e., ratings of the MMC ($U_{\rm dc}$, $\hat{U}_{\rm g}$, and I_0), the protection speeds (Δt_1 and Δt_2), and short-circuit capabilities of the power semiconductors ($I_{\rm SC}$ for IGBTs, and I^2t for diodes). Among them, the limiting reactors are proportional to the ratings of the MMC, while are inversely proportional to the protection speeds and the short-circuit capabilities of the power semiconductors. The three constraints constitute the feasible range of the limiting reactors, which is able to serve the design optimizations. For instance, the boundary of the feasible range indicates the minimum requirements. When $L_{\rm eqdc}$ is in low area, $L_{\rm eqac}$ will be dramatically increased and almost flat in large $L_{\rm eqdc}$ value. That reveals a trade-off between the $L_{\rm eqdc}$ and $L_{\rm eqac}$.

Meanwhile, the impacts of different parameters are shown in Fig. 7. With the increase of the ratings of the MMC (i.e., $U_{\rm dc}$, $\hat{U}_{\rm g}$) or the protection time (i.e., Δt_1 and Δt_2), the feasible range of the limiting reactor is squeezed to the right corner. Conversely, the feasible range is enlarged by a large short-circuit capability of the diode. By contrast, the conventional method only relies on the $U_{\rm dc}$ and an empirical current rise rate $\lambda_{\rm emp}$. Its output is a fixed arm inductance L_0 only. Intensive trial-and-errors of the parameter $\lambda_{\rm emp}$ are inevitable in the conventional method. To let readers utilize the proposed methods easily, an open-access software is also included as shown in Fig. 8.

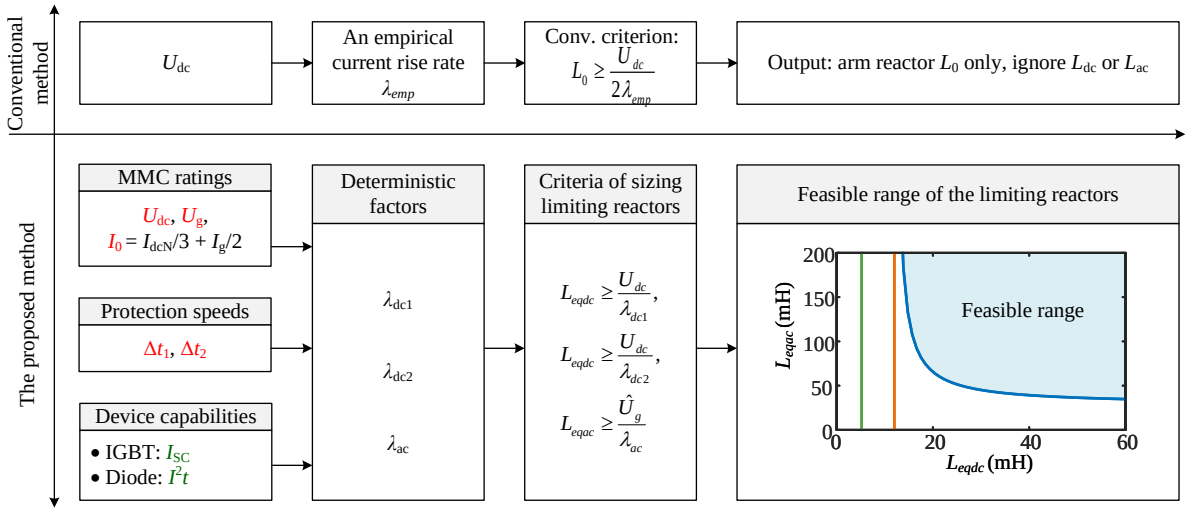


Fig. 6. Comparison of the proposed sizing criteria and the conventional method for the limiting reactors. The proposed method comprehensively considers three aspects, i.e., the ratings of the MMC, the protection speeds, and the device short-circuit capabilities. The obtained feasible range is able to serve the design optimizations.

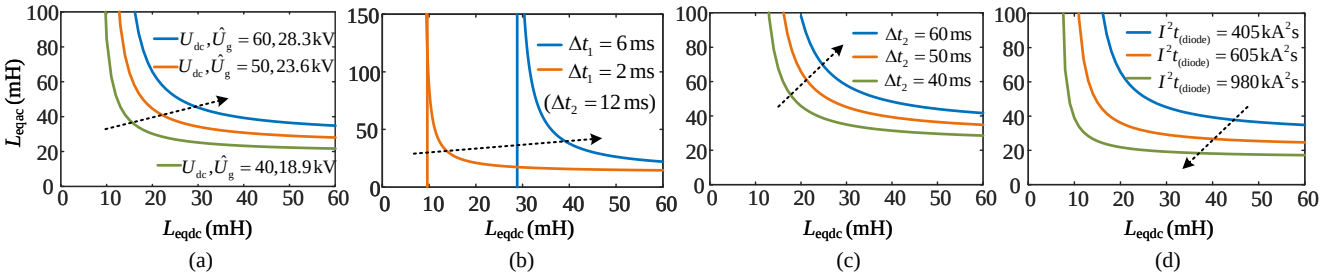


Fig. 7. The impact of the parameters on the feasible range of the limiting reactors: (a) increase the ratings of the MMC, (b) increase the protection time Δt_1, (c) increase the protection time Δt_2, and (d) increase the short circuit capability of the diode.

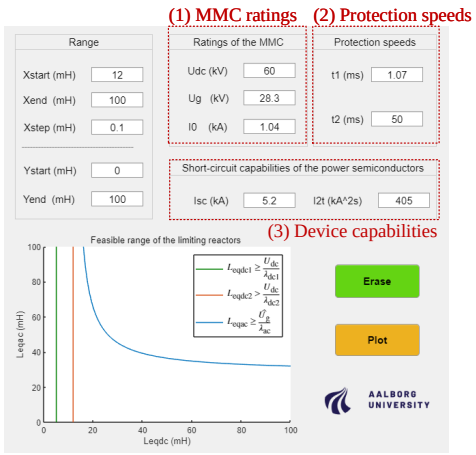


Fig. 8. A software is provided to apply the proposed method.

V. Verification and Comparison

To verify the effectiveness of the proposed method, a hardware-in-the-loop (HIL) experimental platform has been built as shown in Fig. 9. The MMC is emulated using Typhoon HIL-402 and the controller selects dSPACE MicroLabBox. The experimental parameters are listed in Table I. To verify the effects of different power semiconductors, two IGBT modules with different current ratings and short-circuit capabilities are listed in Table II.

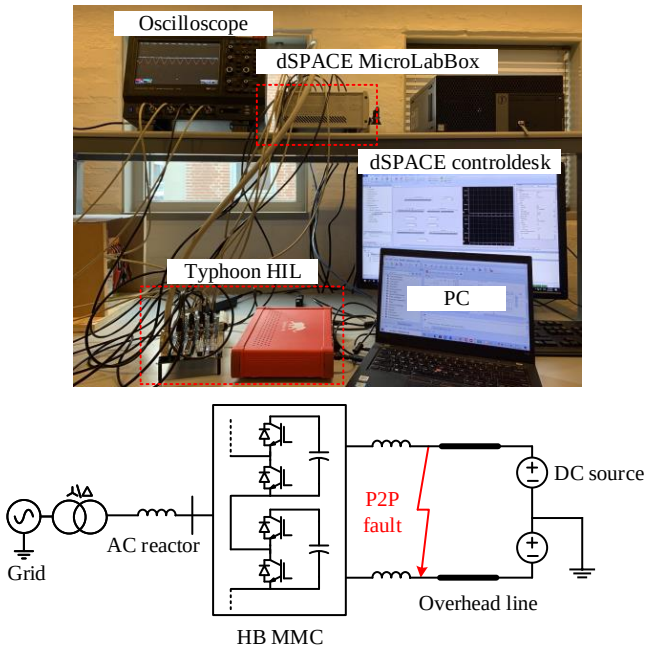


Fig. 9. The photo and the configuration of the experimental platform.

A. Verification of the Fault Current Estimation

To validate the established fault current estimation method, the comparison of a P2P short-circuit fault and the estimations

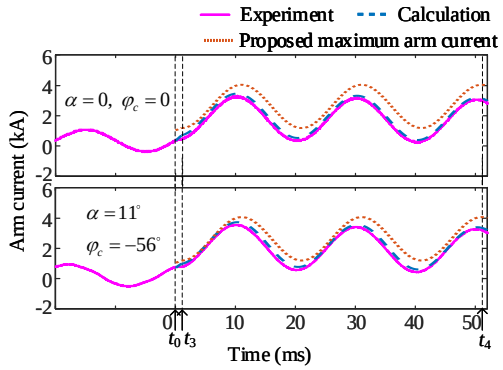
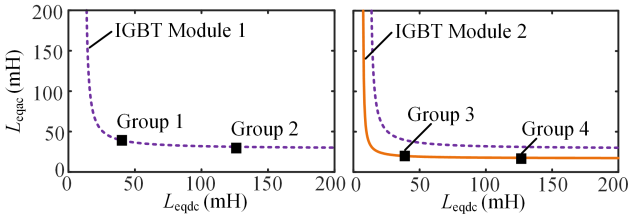


Fig. 10. Comparison of the experimental and theoretical results of the proposed maximum arm current under different α and φ_c.



Parameters (mH)	Group 1	Group 2	Group 3	Group 4
Equivalent DC inductance L_{eqdc}	40.2	126.1	38.8	127.0
Equivalent AC inductance L_{eqac}	39.2	31.2	19.9	17.6
Arm reactor L_0	50	50	30	30
DC reactor L_{dc}	7	93	19	107
AC reactor L_{ac}	14.2	6.2	5	3

Fig. 11. The feasible range of the limiting reactors based on IGBT Module 1 and Module 2, respectively, and the corresponding inductance.

TABLE II
THE DATA OF TWO STUDIED IGBT MODULES, AND THEIR CORRESPONDINGLY ESTIMATED POWER LOSSES, THERMAL RESISTANCE OF THE HEAT SINK AND THE CORRESPONDING VOLUME.

		IGBT Module1		IGBT Module2	
		IGBT	Diode	IGBT	Diode
Data sheet provided values [21], [22]	Voltage [kV]	4.5		4.5	
	Current [kA]	1.2		1.5	
	I_{SC} [kA]	5.2	-	7.8	-
	$I^2t_{(diode)}$ [kA^{2}s]	-	405	-	871
	R_{thjc} [K/kW]	9.5	19	9.8	16
	R_{thch} [K/kW]	9	18	8	11
		IGBT Module 1		IGBT Module 2	
Estimated power losses	S_1 [W]	382		357	
	D_1 [W]	451	Total:	420	Total:
	S_2 [W]	1542	2477	1401	2287
	D_2 [W]	102		109	
Thermal resistance of heat sink	R_{thhs} [K/kW]	5.4		10.7	
Estimated volume	Heat sink volume [cm^3]	14788		7567	

Note: R_{thjc}: junction-to-case thermal resistance, R_{thch}: case-to-heatsink thermal resistance, R_{thhs}: heatsink-to-ambient thermal resistance.

are shown in Fig. 10. The experiments are conducted with two different sets of α and φ_c. The experimental results coincide well with their corresponding theoretical calculations. Meanwhile, the proposed maximum arm current is constant in the two cases, which models the worst-case scenario to design the limiting reactors. It should be mentioned that the HIL experiment cannot provide dedicated device-level transients. To compensate for this limitation, two short-circuit transients of the device are provided in Figs. 5(b) and (c) where Type-II is more relevant to the MMC.

B. Verification of the Proposed Criteria with IGBT Module 1

With the selection of IGBT Module 1, the proposed method provides a feasible range of the limiting reactors as shown in Fig. 11. To validate the proposed criteria, two sets of parameters on the boundary are selected, which are denoted as Group 1 and Group 2, respectively. It should be noted that the proposed method considering the P2P fault only determines the relation of L_{eqdc} and L_{eqac}. To select the specific values of the three reactors is discussed in Section VI.

Fig. 12(a) shows the experimental DC currents with parameters of Groups 1 and 2. The case of Group 1 has a large DC current rise rate due to a smaller L_{eqdc}. Moreover, Fig. 12(b) shows the comparison of the withstanding stresses and the short-circuit capabilities of the IGBTs and diodes, respectively. First, the arm current at t_3 is much smaller than the I_{SC} of the IGBT, which implies the main limitation of this case is not the short-circuit capability of the IGBT. On the contrary, $I^2t_{(diode)}$ of two cases are rising from t_0 to t_4, but the maximum $I^2t_{(diode)}$ is within the datasheet provided value. Thus, the selected limiting reactors based on the proposed criteria are able to guarantee the operation of the power semiconductors within their safe operating areas.

For the MMC system with identical ratings and power semiconductors, Group 2 has L_{eqdc} = 126.1 mH which is approximately three times Group 1. However, both the arm currents and current integral are similar under the two different parameters apart from the different DC current rise rates. Therefore, the parameters of Group 1 near the knee area of the feasible range in Fig. 11 is more cost-effective.

C. Verification of the IGBT Module 2 with Larger Capabilities

To further investigate the impact of the short-circuit capability of the power semiconductor devices, IGBT Module 2 with an increased short-circuit capability is selected. The feasible range based on IGBT Module 2 is obtained as shown in Fig. 11 as well. Compared to IGBT Module 1, the feasible range of IGBT Module 2 is enlarged to the lower left corner, which means a smaller inductance can be selected by increasing the short-circuit capability of the power module. Two parameters on the boundary are also selected and denoted as Group 3 and Group 4, respectively.

Similarly, Fig. 11(c) shows the corresponding DC currents, and Fig. 11(d) shows the comparison between the experimental results of the arm currents and the short-circuit capability of power semiconductor devices. Both IGBTs and diodes are within their safe operating areas, which validates the effectiveness of the proposed method. Moreover, Group 3 which has the parameters near the knee area of the feasible range has only 1/4 of L_{eqdc} compared to the case of Group 4. It reveals that the proposed feasible range is able to explore better parameters with consideration of the P2P fault. Furthermore, L_{eqdc} and

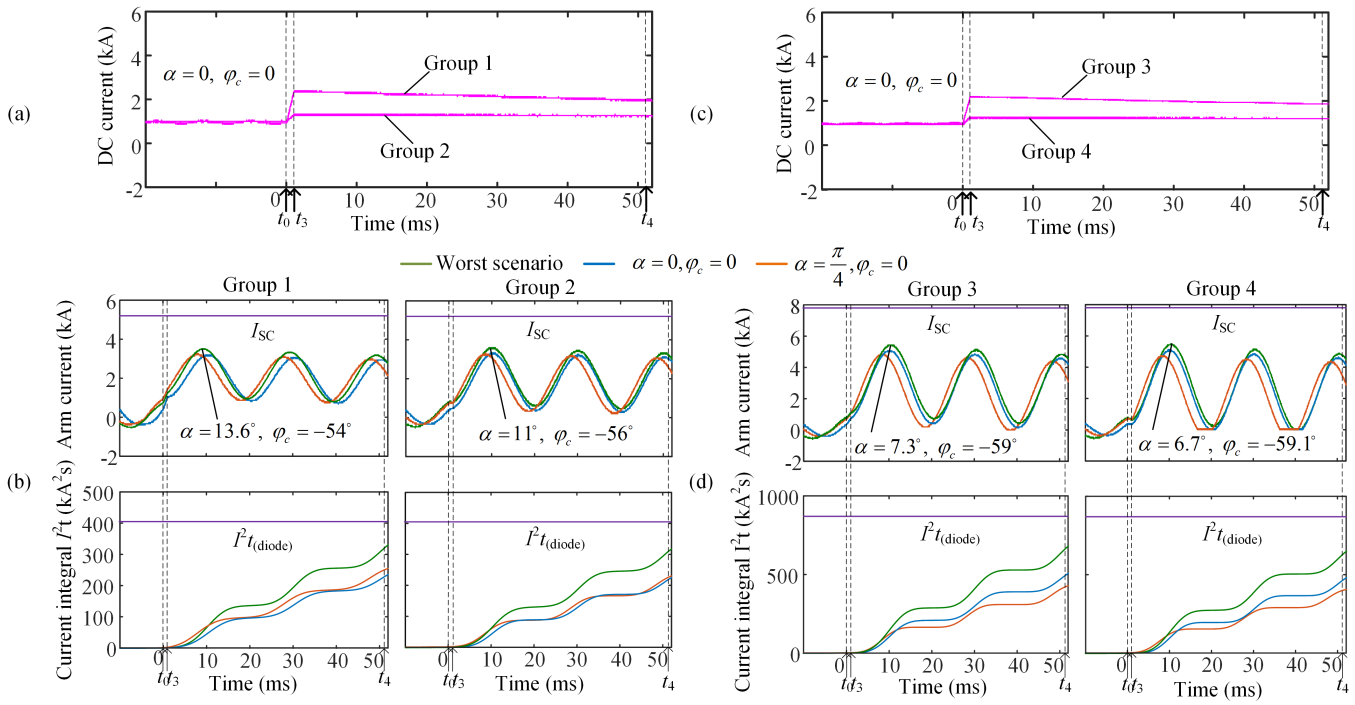


Fig. 12. Experimental results when using parameters of Groups 1-4: (a) DC currents (Groups 1 and 2). (b) comparison between arm currents and I_{SC}, and comparison between current integral and $I^2t_{(\mathrm{diode})}$ (Groups 1 and 2). (c) DC currents (Groups 3 and 4). (b) comparison between arm currents and I_{SC}, and comparison between current integral and $I^2t_{(\mathrm{diode})}$ (Groups 3 and 4).

L_{eqac} of Group 3 have reduced by 4% and 50%, respectively, compared to the ones of Group 1. This demonstrates that the demand for the passive device can also be alleviated by upgrading the active devices.

D. Impacts of Reactor Sizing on Power Losses and Cooling Systems

Sections V-B and V-C have revealed that the reactor sizing is intertwined with the parameters of the power devices. The further impacts on power losses and cooling systems are estimated and listed in Table II. The estimation methods are in accordance with the previous studies of [23] and [24]. First, IGBT Module 2 has slightly reduced power losses. However, due to the reduced thermal resistances of IGBT Module 2, the required thermal resistance of the heat sink changes by a factor of two. The estimated volume of the heat sink of IGBT Module 2 is about half of the one for IGBT Module 1. This reveals that a proper over-rating of the power module not only reduces the reactance, but also increases efficiency and reduce volume. The quantified interactions presented in this paper help to guide to achieve a better trade-off among them.

E. Comparison of the Proposed Criteria with the Previous Methods

The existing studies use an empirical constant to size the limiting reactor as per (1). In the literature, different values of the λ_{emp}, such as a wide range of 2-10 kA/ms in [6], 100 kA/ms [7], or 1.3 kA/ms [8], have been reported. Applying $\lambda_{\mathrm{emp}} = 1.3$ kA/ms to the case studies of this paper, the calculated $L_0 = 23$ mH and the corresponding short-circuit waveforms are shown in Fig. 13. Both the selected IGBT modules do not meet the short-circuit requirements considering I_{SC} or $I^2t_{(\mathrm{diode})}$. Moreover, it reveals that the provided λ_{emp} in the literature is problematic to be applied to different cases.

F. Comparison of the Proposed Criteria to the Installed Projects

To further demonstrate the proposed criteria under various parameters, six installed HBSM-based MMC projects along with their feasible ranges are compared in Fig. 14. The equivalent inductance of these projects is all within the feasible range provided by the proposed method, which verifies the effectiveness of the proposed method.

VI. Discussion

In this paper, the reactors are designed to suppress the DC short-circuit faults and the feasible range of the two equivalent inductances is presented. However, it should be mentioned the reactors of the MMC have different functions, such as suppressing the resonance of the circulating currents, providing an interface to the AC grid, filtering the harmonics, etc. The conversion from the obtained feasible range of L_{eqdc} and L_{eqac} into the values of L_0, L_{ac} and L_{dc} needs to consider these requirements as well. This paper summarizes these requirements as listed in Table III. Apart from the resonance requirement related to the arm inductance L_0 directly, others correlate to the equivalent inductance L_{eqdc} and L_{eqac}.

To further clarify the trade-offs, a demonstration based on the study case of this paper is shown in Fig. 15. First, with

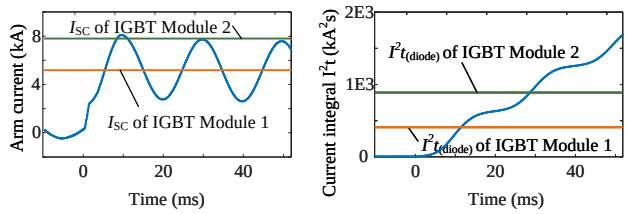


Fig. 13. Applying the parameter of the existing work $\lambda_{emp} = 1.3$ kA/ms [8] to the case study of this paper. Both IGBT modules do not meet the short-cicuit requirements in terms of I_{SC} or $I^2t_{(diode)}$.

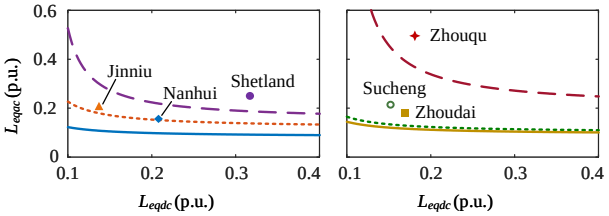


Fig. 14. Comparison of the proposed feasible range (lines) and the parameters of the installed projects (dots). Projects: Nanhui [25], Shetland [26], Jinniu and Sucheng [27], Zhouqu and Zhoudai [28].

TABLE III
THE CRITERIA OF REACTOR SIZING CONSIDERING FOUR DIFFERENT ASPECTS.

Functions of the reactors	Criteria	Involved parameters	Ref.
Limiting short circuit transient	The proposed λ_{dc1}, λ_{dc2}, λ_{ac} in (13) and (18).	L_{eqdc}, L_{eqac}	–
Avoid current resonance	$L_{res,n} = \frac{N}{\omega^2 C_0}\frac{2(h^2-1)+m_a^2h^2}{8h^2(h^2-1)} \Rightarrow L_0 > \frac{N}{\omega^2 C_0}\frac{3+2m_a^2}{48}$	L_0	[29], [30]
Interface to AC grid	$m_a = \frac{2}{U_{dc}}\sqrt{\left(\hat{U}_g - \frac{2S\sin\varphi_c}{3\hat{U}_g}\omega L_{eqac}\right)^2 + \left(\frac{2S\cos\varphi_c}{3\hat{U}_g}\omega L_{eqac}\right)^2} \le 1$	L_{eqac}	[31]
Filter harmonics	$\mathrm{THD}_{pcc} = \frac{L_s}{L_s+L_{eqac}}\mathrm{THD}_c = \frac{L_s}{L_s+L_{eqac}}\frac{1}{f(1)}\sqrt{\sum_{h=2k+1}^{\infty}\left[\frac{f(h)}{h}\right]^2}$	L_{eqac}	[32]–[36]

Notes: m_a is the modulation index, THD_{PCC} and THD_c are total harmonic distortion at the point of common coupling and the converter side, respectively, L_s is the equivalent inductance of the AC grid, $f(h) = \sum_{i=1}^{s}\cos(h\theta_i)$ with the positive integer $k = 1, 2, 3, \ldots$, s is the number of switching angles in the first quarter of cycle, and θ_i is the i-th switching angle.

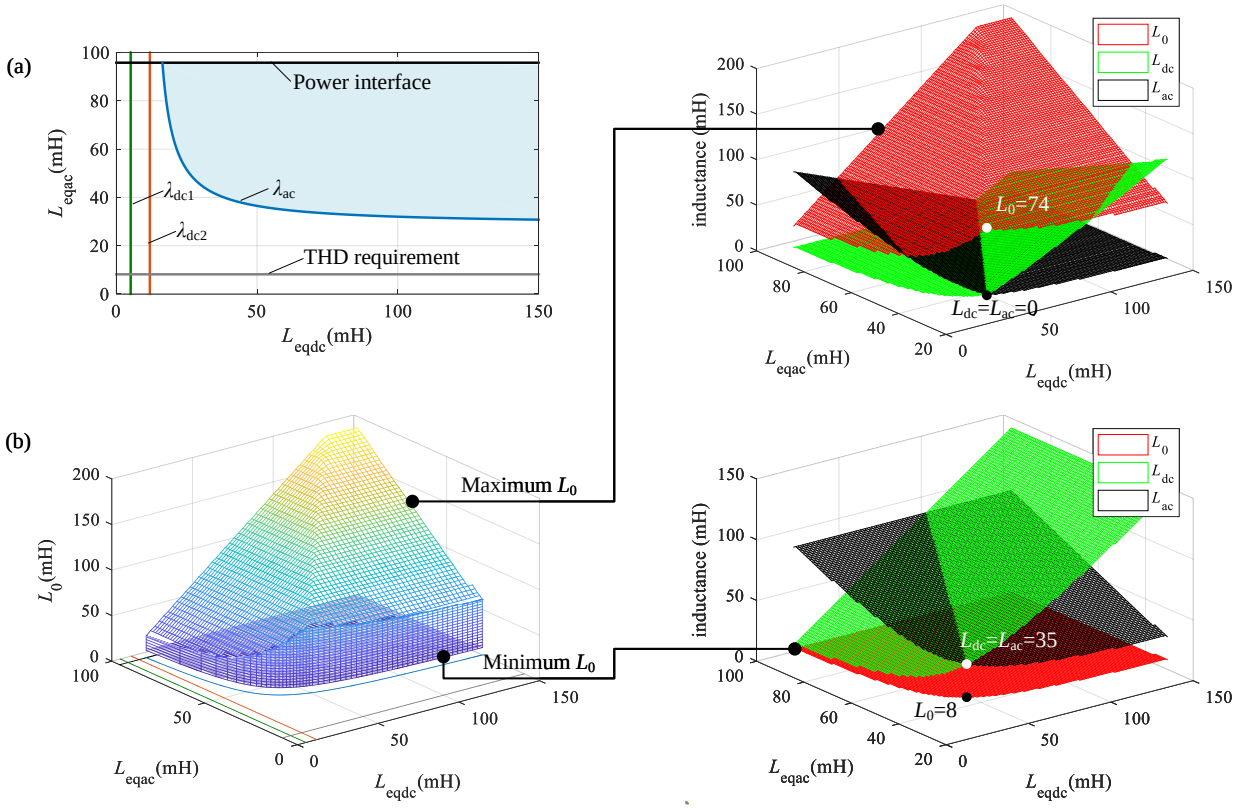


Fig. 15. The results with considering all constraints in Table III comprehensively: (a) the feasible range of L_{eqdc} and L_{eqac} with two more constraints, and (b) the feasible ranges of arm, dc and ac reactors (L_0, L_{dc}, and L_{ac}) and their interactions. (Parameters are based on $L_s = 6.37$ mH, $\mathrm{THD}_{PCC} \le 1.5\%$, $\varphi_c \le \frac{\pi}{4}$, and Table I)

consideration of the interface to the AC grid and the THD requirements, the feasible region of the AC and DC loop inductance is narrowed slightly as shown in Fig. 15(a). The power interface limits the maximum L_{eqac}, but the dominant factor is still related to the short circuit. Next, the feasible region of the arm inductance L_0 is obtained as shown in Fig. 15(b), which consists of a flat minimum surface and a cone shape of the maximum. The minimum L_0 surface is limited by that the arm inductance L_0 needs to be greater than 8 mH to avoid the circulating current resonance. The maximum L_0 surface consists of the upper constraints of $L_0 \leq 1.5L_{\text{eqdc}}$ and $L_0 \leq 2L_{\text{eqac}}$ according to (2). Considering the designs based on the two extreme surfaces, the corresponding L_{dc} and L_{ac} are obtained in the right-hand side of Fig. 15(b). For either case, the surfaces of L_{dc} and L_{ac} have inverse trends at two ends and have an intersection in the middle. For instance, considering the situation with the maximum L_0, the intersection has $L_{\text{dc}} = L_{\text{ac}} = 0$ mH and $L_0 = 74$ mH. It represents a design using the arm reactors to fulfill all requirements. On the contrary, for the case on the minimum L_0 plane, the additional L_{dc} and L_{ac} are mandatory. The intersection has $L_{\text{dc}} = L_{\text{ac}} = 35$ mH and $L_0 = 8$ mH.

Moreover, it is worth mentioning that this paper is focused on the most typical HBSM MMC and other topologies with full-bridge submodules (SM), clamping double SMs, and/or a hybrid combination of different SMs [37] are not covered. For those topologies, as during the fault, the SM capacitors are in the path of fault current, the limiting reactor sizing need to consider the SM capacitor charging and other factors.

VII. Conclusion

This paper proposes a model-based design approach for the MMC. It contributes to sizing multiple reactors of the MMC to keep the short-circuit current within the robust limits of power devices and the interactions of different constraints. The following conclusions can be summarized.

1) By bridging the system-level short-circuit behaviors and component-level robustness of the MMC, this paper proposes three deterministic factors λ_{dc1}, λ_{dc2}, and λ_{ac} to take place the empirical λ_{emp} in the existing studies.
2) Based on the proposed method, this paper quantitatively points out that the sizing of the limiting reactors depends on three intertwined aspects: a) ratings of the MMC, b) fault protection speeds, and c) short-circuit capabilities of power semiconductors.
3) A feasible region of designing the AC-loop and DC-loop inductances is provided. The parameters near the knee area of the feasible range provide better cost-effective solutions, and the demand for the passive devices can be alleviated by upgrading the active devices. These properties reveal that the proposed method with better modeling of the interactions is able to serve to explore design optimization.
4) All constraints of the reactor sizing of the MMC are comprehensively considered, including both fault (i.e., short circuit) and normal states. Based on the parameters of the case study, the dominant factor is related to the fault state. It indicates that the optimization of power electronics converters often depends on fault states instead of often talked normal operations.

The proposed method has been verified by simulations and experiments as well as comparison with the parameters of several installed projects.

Appendix

The capacitor discharging in the period Δt_1 is

$$i_{\text{cir1}}(t) = \frac{1}{3}\frac{e^{-(t-t_0)/2\tau_{\text{dc}}}}{\sqrt{1-\xi^2}}\{\frac{U_{\text{dc}}}{\omega_{\text{dc}}L_{\text{eqdc}}}\sin[\omega_{\text{dc}}\sqrt{1-\xi^2}(t-t_0)] - I_{\text{dc}}(t_0)\sin[\omega_{\text{dc}}\sqrt{1-\xi^2}(t-t_0)-\theta_{\text{dc}}]\}, \quad \text{(A1)}$$

where R_{eqdc} is the DC-loop equivalent resistance. The expressions of τ_{dc}, ω_{dc}, ξ and θ_{dc} are given as

$$\tau_{\text{dc}} = \frac{L_{\text{eqdc}}}{R_{\text{eqdc}}}, \omega_{\text{dc}} = \sqrt{\frac{1}{L_{eqdc}C_{\text{eq}}}},$$
$$\xi = \frac{R_{\text{eqdc}}}{2}\sqrt{\frac{C_{\text{eq}}}{L_{\text{eqdc}}}}, \theta_{\text{dc}} = \arctan\frac{\sqrt{1-\xi^2}}{\xi}. \quad \text{(A2)}$$

The detailed parameters in the sizing criteria of DC-loop and AC-loop equivalent inductance for diodes are given as

$$a_1 = \frac{27}{3\Delta t_2 + \Delta t_1}, a_2 = \frac{27\Delta t_1(4\Delta t_2 + \Delta t_1)}{4(3\Delta t_2 + \Delta t_1)^2},$$
$$a_3 = \frac{9(2\Delta t_2 + \Delta t_1)}{2(3\Delta t_2 + \Delta t_1)}. \quad \text{(A3)}$$

$$b_1 = \frac{64}{9}m^2 - \frac{16\omega(3\Delta t_2 + \Delta t_1)}{27}n,$$
$$b_2 = \frac{128}{3}m^2 - \frac{16\omega(2\Delta t_2 + \Delta t_1)}{3}n,$$
$$b_3 = 64m^2 - 16\omega(\Delta t_2 + \Delta t_1)n, b_4 = 16n, b_5 = 8m. \quad \text{(A4)}$$

$$\eta = \frac{U_{\text{dc}}\Delta t_1}{L_{\text{eqdc}}}, \quad \text{(A5)}$$

$$m = \frac{\omega\Delta t_2 - \sin(\omega\Delta t_2)}{6\omega\Delta t_2 + \sin(2\omega\Delta t_2) - 8\sin(\omega\Delta t_2)},$$
$$n = \frac{m}{\omega\Delta t_2 - \sin(\omega\Delta t_2)}. \quad \text{(A6)}$$

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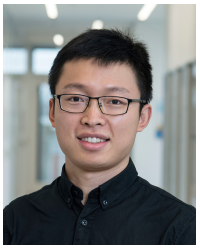

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