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A Novel Fault-Tolerant Operation Approach for the Modular Multilevel Converter-Based STATCOM with the Enhanced Operation Capability

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***Abstract*—The operation capability of the modular multilevel converter (MMC)-based static synchronous compensator (STATCOM) is limited under submodule (SM) failures. When running in the STATCOM mode, the floating dc-link voltage of the MMC is adjustable. Therefore, this paper proposes a novel fault-tolerant operation approach to enhance operation capability of the MMC under severe SM failures. Firstly, the dc-link voltage is dynamically regulated under SM failures, where the capacitor voltages of all SMs are slightly increased. The modulation ranges of the faulty and healthy phases can be enlarged, and the even voltage stress distribution can be realized. Then, a low-magnitude fundamental frequency zero-sequence voltage is injected to balance the line-to-line voltages. Finally, the virtual energy idea is proposed, where the capacitor voltages of faulty SMs are considered to be clamped at the reference value. As a result, the arm energy reference will be the same in all six arms, and the arm energy balancing control is simplified. Detailed comparisons show the proposed approach has an enhanced operation capability with lower capacitor voltage increment. Simulation and experimental results verify that even under severe SM failures, the proposed approach can still guarantee the fault-tolerant operation within the specified security region.**

***Index Terms*—Fault-tolerant operation, modular multilevel converter, operation capability, static synchronous compensator, submodule failure.**

I. Introduction

REACTIVE power compensation can be applied to correct the power factor, thus improving power quality and reducing the power loss [1], [2]. With the fast response and low harmonic distortion, static synchronous compensators (STATCOMs) are widely adopted in medium- and high-voltage applications, such as power transmission [3], renewable energy power plants [4], and battery energy storage systems (BESSs) [5]. In recent years, the modular multilevel converter (MMC) has been recognized as an attractive topology for STATCOMs, because of its advantages of modularity, scalability, reliability, and excellent harmonic performance [6], [7]. However, the large number of SMs in the MMC also increases the possibility of potential switch failures. The misoperation of faulty SMs will cause overmodulation, affect the tracking accuracy of controllers, and even lead to secondary damage or system failure [8]. Therefore, it is necessary to study the fault-tolerant operation approach for the MMC-based STATCOM.

The fault-tolerant control aims to guarantee the uninterrupted and stable operation of power converters with moderate performance [9]. When an SM failure is detected, the SM is usually bypassed directly. There are two kinds of bypass operations. The first operation is to bypass the faulty SMs [7], and the second one is to bypass the faulty SMs and the same number of SMs in other arms [10]. The second scheme has asymmetric output characteristics, but the first scheme is more widely applied due to its full use of healthy SMs. When the faulty SM is bypassed, the fault-tolerant control approach can be applied. Generally, fault-tolerant control methods of the MMC can be categorized into the voltage reference adjustment (VRA) -based methods, special modulation technique and hardware (SMH)-based methods, and redundant-SM-based methods.

For the VRA-based methods, the fundamental frequency zero-sequence voltage (FF-ZSV) injection is usually applied [11]. Through injection of the FF-ZSV, three-phase voltage references are adjusted according to their modulation margins. The third harmonic voltage (THV) can also be injected to lower the amplitude of three-phase modulation waves under SM failures [12]. In addition, an improved fault-tolerant control method based on the FF-ZSV injection and dc neutral shift is proposed in [13], and an extended operation region is obtained under multi-phase SM failures. An irregular zero-sequence voltage is injected in [14], and higher attainable line-to-line voltages can be obtained in multilevel converters, compared with the FF-ZSV-based methods. However, when it is applied in the MMC, it will encounter circulating current distortion due to the unbalanced power between the upper and lower arms.

For the SMH-based methods, reference [15] analyzes a selective harmonic elimination (SHE)-based fault-tolerant control method for a single SM failure, where the magnitude of the fundamental frequency component is guaranteed. The SHE-based method is further analyzed in [16] to deal with multi-fault conditions. In addition, a space-vector-based fault-tolerant control method is proposed in [17]. The special-modulation-based methods are usually suitable for applications with a small

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number of SMs, and the complexity of these algorithms increases significantly with the number of SMs. In [18], a fault-tolerant control method based on redistributed pulsewidth modulation is designed for the MMC-based BESS. It is designed to deal with a single SM failure, and the redundant SMs are necessary for this method. The overmodulation operation can also be used for fault-tolerant operation. Although the MMC is usually designed to operate within the linear region, the modulation reference can increase beyond its limit [7]. The overmodulation-based method in [19] shows that the MMC-based STATCOM presents a notable inherent tolerance in the overmodulation region. In addition, an improved SM topology with higher fault-tolerant operation capability is proposed in [20]. However, the modified SM topology requires a high additional cost and brings inconvenience for the manufacturer.

The redundant-SM-based methods include the cold-reserve and hot-reserve-based methods. For the cold-reserve-based method, the redundant SMs are usually bypassed during normal operation conditions [21]. It has a reduced conduction loss and provides high availability of reserved SMs. However, the disadvantages in harmonic performance and capacitor voltage charging process in redundant SMs limit its application. For the hot-reserve-based method, the redundant SMs participate in the normal operation to obtain a better harmonic performance [22]. However, it also has a higher switching loss. To solve this issue, a fault-tolerant control method with rotating carriers is proposed in [23], where the SMs take turns to work. Therefore, even if the faulty SMs are bypassed, the system can operate normally with symmetric characteristics. However, this process needs carrier exchanges, and both the SM utilization rate and harmonic performance are limited. To improve the harmonic performance during post-fault operation, the hot-reserve SMs take part in operation constantly, and the carrier frequencies are reconfigured in the faulty phase [24]. A redundant-SM-based method combining phase-shifted carrier (PSC) PWM and the sorting algorithm is proposed in [25], where the carrier reconfigurations and SM voltage balancing control are avoided during fault-tolerant operation. Based on this, an improved method is proposed by adjusting the capacitor voltages according to the grid voltage instead of the dc-link voltage, and a lower capacitor voltage increment can be obtained in each SM [26]. This method improves the fault-tolerant operation capability, especially in applications with a large number of SMs.

To enhance the operation capability of the MMC-based STATCOM under SM failures, this paper proposes a novel fault-tolerant operation approach. Firstly, the capacitor voltages of all SMs are increased to enlarge the modulation range in the faulty and healthy phases. Then, the FF-ZSV is injected to generate balanced line-to-line voltages. Finally, the virtual energy idea is proposed to calculate the circulating current references for the arm energy balancing control. Compared with the conventional methods, the proposed approach can enhance the operation capability under severe SM failures.

The rest of the paper is outlined as follows. Section II presents the topology of the MMC-based STATCOM and the conventional hot-reserve-based fault-tolerant control method. The proposed fault-tolerant operation approach is introduced and compared with the conventional methods in Section III. Simulation and experimental results are presented in Section IV and Section V, respectively, which verify the effectiveness and advantages of the proposed scheme. The main conclusion is summarized in Section VI.

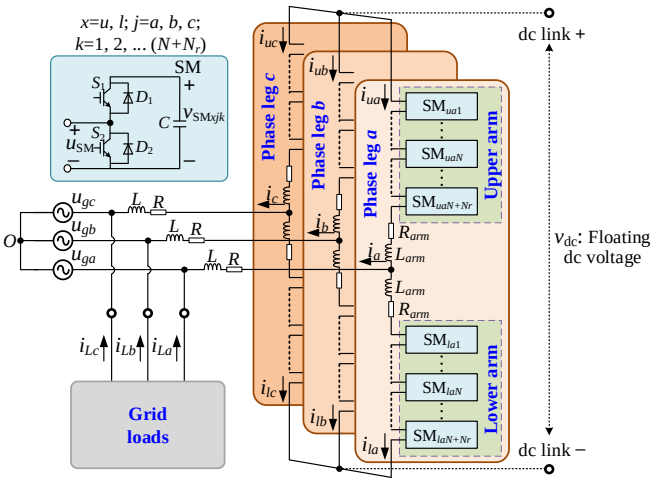

Fig. 1. MMC-based STATCOM topology.

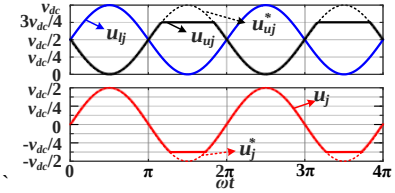

Fig. 2. Operation condition under SM failures in the upper arm (N=3, N_r =1).

II. Topology of the MMC-Based STATCOM and the Conventional Hot-Reserve-Based Method

In this section, the topology of the MMC-based STATCOM is illustrated, firstly. Then, the conventional hot-reserve-based fault-tolerant control method is briefly introduced.

A. Topology of the MMC-Based STATCOM

As shown in Fig. 1, the MMC-based STATCOM contains three phases, each including the upper and lower arms. In each arm, there are (N+N_r) series-connected half-bridge (HB) SMs and an arm inductor L_{arm}, where N and N_r are the numbers of normal and redundant SMs, respectively. The upper and lower arms are connected to the ac grid through filter inductors L. The equivalent resistances of L_{arm} and L are defined as R_{arm} and R, respectively. Each SM will output the capacitor voltage v_{SMxjk} if inserted and zero volts if bypassed. x indicates the arm position (x=u, l); j indicates the phase order (j = a, b, c); k indicates the SM order number (k = 1, 2, … , (N+N_r)). By the combination of SM output states, multilevel waveforms can be generated. Based on the circuit configuration, the output current and the circulating current of the MMC are defined as

$$i_j = i_{uj} - i_{lj},\ i_{cirj} = (i_{uj} + i_{lj})/2 \tag{1}$$

where i_{uj} and i_{lj} are the arm currents of the upper and lower arms, respectively.

According to the analysis in [26], the arm output voltage references in the upper and lower arms (u^*_{uj} and u^*_{lj}) can be calculated based on the equivalent output voltage reference u^*_j and the circulating current control reference u^*_{cirj}

$$u^*_{uj} = v_{dc}/2 - u^*_j + u^*_{cirj},\ u^*_{lj} = v_{dc}/2 + u^*_j + u^*_{cirj} \tag{2}$$

With the calculated u^*_{uj} and u^*_{lj}, the number of inserted SMs in

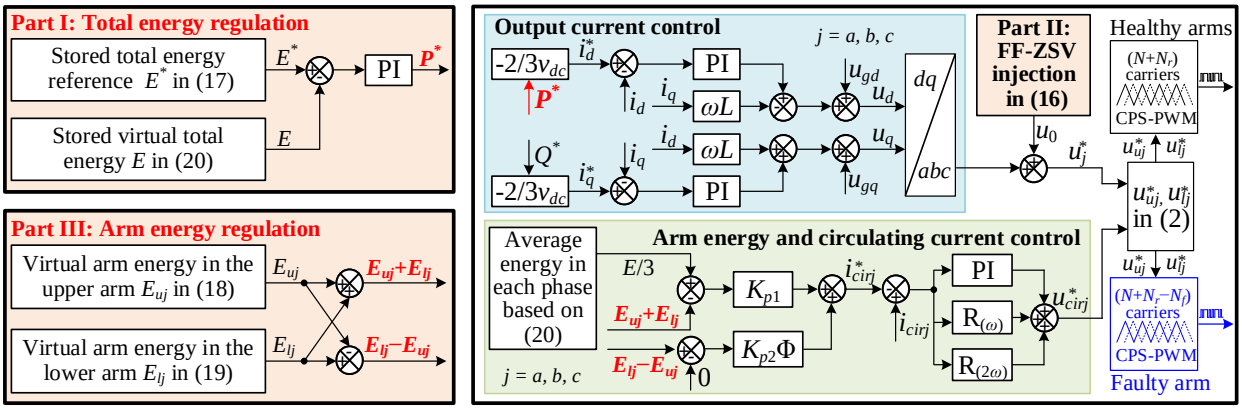

Fig. 3. Overall control diagram of the MMC-based STATCOM.

each arm can be calculated.

B. Conventional Hot-Reserve-Based Fault-Tolerant Control

To realize the fault-tolerant operation, the redundant SMs are usually configured. For the conventional hot-reserve-based methods in [22], the redundant SMs participate in the normal operation. Therefore, the capacitor voltage in each SM is usually lower than the rated value. As a result, there will be enough space for the SM capacitor voltage increment when the SM failure occurs. More detailed configurations are as follows.

The SM capacitor voltage under normal operation conditions should be

$$v_{SM}^* = v_{dc}/(N+N_r) \tag{3}$$

The rated capacitor voltages can be expressed as

$$v_{SM\_rated}^* = v_{dc}/N. \tag{4}$$

Suppose there are three SMs and one redundant SM in each arm, the operation condition under SM failure in the upper arm is shown in Fig. 2, where u_{uj} and u_{lj} are the arm output voltages in the upper and lower arms, respectively; u_j is the equivalent output voltage. When SM failures occur, the faulty SMs are bypassed, and the range of arm output voltage is reduced. To restore the normal range of arm output voltage, the capacitor voltages in the faulty arm should be increased to the value in (5), and the arm output voltage can recover to its normal range.

$$v_{SM\_HR}^* = v_{dc}/(N+N_r-N_f) \tag{5}$$

where N_f is the number of faulty SMs.

However, when the faulty SMs outnumber the redundant SMs, the healthy SMs cannot further increase their voltages, and the voltages are clamped to the rated value. In this condition, the converter enters the overmodulation region.

Hereby, the redundant index and fault index are defined as

$$n_r = N_r/N, \quad n_f = N_f/N_r \tag{6}$$

where n_r is the redundant index and n_f is the fault index.

To avoid overmodulation, the MMC-based STATCOM should operate within the following region

$$n_f \in [0,1]. \tag{7}$$

Therefore, the maximum allowable fault index of the conventional hot-reserve-based fault-tolerant control method is 1.

III. Proposed Fault-Tolerant Operation Approach

Firstly, the proposed fault-tolerant operation approach is presented in this section. Then, its characteristics are compared with the conventional methods.

A. Proposed Fault-Tolerant Operation Approach

The overall control diagram of the MMC-based STATCOM is illustrated in Fig. 3. It mainly includes output current control and arm energy and circulating current control. Namely, the output current control is used to control the active and reactive current of the converter. The arm energy and circulating current control is used to balance the internal capacitor voltages and suppress the harmonics in circulating currents. In addition, in the modulation part, the carriers in the faulty arms need to be adjusted for better harmonic performance, as discussed in [24].

The main idea of the proposed approach can be divided into three parts, as shown in Fig. 3. **Part I** is the total energy regulation, which is used to control the sum of all capacitor voltages together with dc-link voltage. **Part II** is the FF-ZSV injection, which is used to generate balanced line-to-line voltages. **Part III** is the arm energy regulation, which is used to balance the capacitor voltages between each arm.

To better demonstrate the characteristics of the proposed approach, a phasor diagram analysis with one SM failure in phase *a* is illustrated in Fig. 4. Figs. 4(a), (b), and (c) show the phasor diagram of normal operation conditions, SM failure conditions, and fault-tolerant operation conditions, respectively. In the figures, $\boldsymbol{V_a}$, $\boldsymbol{V_b}$, and $\boldsymbol{V_c}$ are the three-phase output voltage vectors during normal operation conditions; $\boldsymbol{V'_a}$ is the output voltage vector in phase *a* after SM failure; $\boldsymbol{V''_a}$, $\boldsymbol{V''_b}$, and $\boldsymbol{V''_c}$ are the three-phase output voltage vectors of the fault-tolerant operation. When SM failures occur in phase *a*, the modulation range reduces accordingly. To realize fault-tolerant operation, the capacitor voltages in all SMs are increased together with the dc-link voltage, and the modulation ranges are enlarged, as indicated by the red dash circle in Fig. 4. Then, the FF-ZSV is injected with a lower magnitude, and the balanced line-to-line voltages can be generated. It is noted that after the injection of FF-ZSV, the magnitude of the modified output voltage phasors should be smaller than the maximum value in the figure.

1) Principle of Part I and Part II

Part I and **Part II** involve the average capacitor voltage adjustment and FF-ZSV injection. The value of capacitor voltage increment and the magnitude of injected FF-ZSV are analyzed as follows. The following analysis takes SM failures in the upper arm as an example. When SM failures occur, the maximum output phase voltage depends on the healthy SMs in the healthy arm. Suppose there are N_f SM failures in the upper arm, the maximum arm output voltage and the maximum

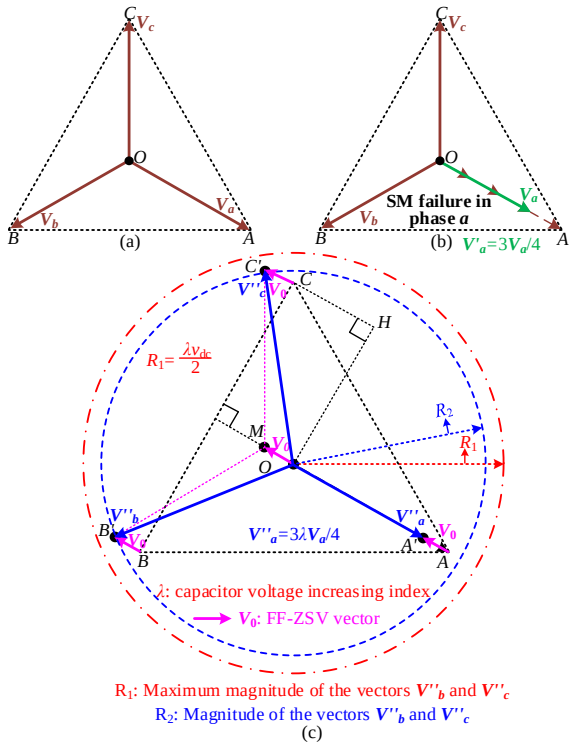

Fig. 4. Phasor diagrams of the proposed fault-tolerant operation approach (N=3, N_r=1). (a) Normal operation condition, (b) one SM failure condition in phase *a*, and (c) the fault-tolerant operation condition.

output voltage in the faulty phase should be

$$\begin{cases} u_{uf\_\max} = (N+N_r-N_f)v_{dc}/(N+N_r) \\ u_{f\_\max} = (N+N_r-N_f)v_{dc}/(2N+2N_r) \end{cases} \tag{8}$$

where u_{uf_max} is the maximum arm output voltage and u_{f_max} is the maximum output phase voltage under SM failures.

As shown in Fig. 4, to enlarge the modulation ranges, the capacitor voltages in all SMs will increase to the same value as

$$v^*_{SM\_PR} = \lambda v_{dc}/(N+N_r) \tag{9}$$

where λ is the increasing index of capacitor voltages and $v^*_{SM\_PR}$ is the capacitor voltage reference of the proposed approach.

Correspondingly, the dc-link voltage will also increase to

$$v^*_{dc\_PR} = \lambda v_{dc}. \tag{10}$$

where v^*_{dc} is the dc-link voltage of the MMC-based STATCOM.

Substituting (9) into (8), the maximum arm output voltage and maximum output voltage in the faulty phase will be

$$\begin{cases} u_{uFT\_\max} = \lambda(N+N_r-N_f)v_{dc}/(N+N_r) \\ u_{FT\_\max} = \lambda(N+N_r-N_f)v_{dc}/(2N+2N_r) \end{cases} \tag{11}$$

where u_{uFT_max} and u_{FT_max} are the maximum arm output voltage and the maximum output phase voltage under fault-tolerant operations, respectively.

With the increased capacitor voltages in all the healthy SMs, the modulation ranges are enlarged in both the faulty and the healthy phases. To generate balanced line-to-line voltages, the FF-ZSV injection with a lower magnitude is required. The injected FF-ZSV should meet the constraint that the magnitude of the equivalent output voltage in phase *a* should be the same as the original value (MA'=AA'). Therefore, the magnitude of the required FF-ZSV injection V_0 can be expressed as

$$V_0 = v_{dc}/2 - \lambda(N+N_r-N_f)v_{dc}/2(N+N_r). \tag{12}$$

As shown in Fig. 4, the maximum amplitude of the normal output voltage is $v_{dc}/2$. Then, the magnitude of CH is equal to $v_{dc}/4$, and the magnitude of HO is equal to $\sqrt{3}v_{dc}/2$. With the above FF-ZSV injection, the amplitude of the final output voltage references in other healthy phases can be expressed as

$$\begin{aligned} V_b = V_c = OB' = OC' &= \sqrt{(HC')^2+(OH)^2} \\ &= \sqrt{\left(0.75v_{dc} - \frac{\lambda(N+N_r-N_f)v_{dc}}{2(N+N_r)}\right)^2 + \left(\frac{\sqrt{3}}{4}v_{dc}\right)^2}. \end{aligned} \tag{13}$$

To avoid the overmodulation, the modulation waves should be within the modulation range. Hence, the amplitude of the modulation wave in the healthy phases should meet the constraint

$$V_b = V_c \le \lambda v_{dc}/2. \tag{14}$$

Substituting (13) into (14), the minimum increasing index λ under different SM failure conditions can be calculated as (15).

$$\begin{cases} \lambda \ge \dfrac{-3F(N_r,N_f)+\sqrt{9F^2(N_r,N_f)+12\left(1-F^2(N_r,N_f)\right)}}{2\left(1-F^2(N_r,N_f)\right)} \\ F(N_r,N_f) = (N+N_r-N_f)/(N+N_r) \end{cases} \tag{15}$$

With the calculated λ, the magnitude of injected FF-ZSV can be derived by substituting (15) into (12), and the final reference in **Part II** can be expressed as

$$u_0 = V_0\cos(\omega t) \tag{16}$$

where ω is the grid frequency.

To effectively control the capacitor voltages of all SMs and the dc-link voltage in **Part I**, the stored total energy needs to be regulated in the MMC-based STATCOM. Based on the capacitor voltage references in (9), the reference value of the stored total energy in all capacitors can be expressed as

$$E^* = \begin{cases} 6(N+N_r)C(v^*_{SM})^2/2; & \text{No SM failure} \\ 6(N+N_r)C(v^*_{SM\_PR})^2/2; & \text{SM failure} \end{cases}. \tag{17}$$

In **Part I**, proportional-integral (PI) controllers are applied to calculate the circulating current references, thus regulating the stored total energy [19]. Then, PI controllers are used to control the output current [19]. Finally, the FF-ZSV is injected in **Part II** to generate balanced line-to-line voltages. Thereby, the total energy and output currents can be controlled.

2) Virtual energy idea

It is noted that under fault-tolerant operation conditions, the stored energy in the faulty SM needs to be excluded from the system, and the arm energy balancing between the faulty and healthy arms could be quite complicated due to the different arm energy references.

To avoid complicated references configurations, the virtual energy idea is proposed in this paper. Based on this idea, a uniformed arm energy reference can be adopted in each arm, and the arm energy balancing process can be greatly simplified.

For the virtual energy idea, the energy in the faulty SM is considered to be the same as the reference value, and its influence on the arm energy can be eliminated. Meanwhile, the virtual arm energy in each arm can be defined as

$$E_{uj} = N_f C(v^*_{SM\_PR})^2/2 + \sum_{k=1,k\ne\Omega_{uj}}^{N+Nr} Cv^2_{SMujk}/2 \tag{18}$$

$$E_{lj} = N_f C(v^*_{SM\_PR})^2/2 + \sum_{k=1,k\ne\Omega_{lj}}^{N+Nr} Cv^2_{SMljk}/2 \tag{19}$$

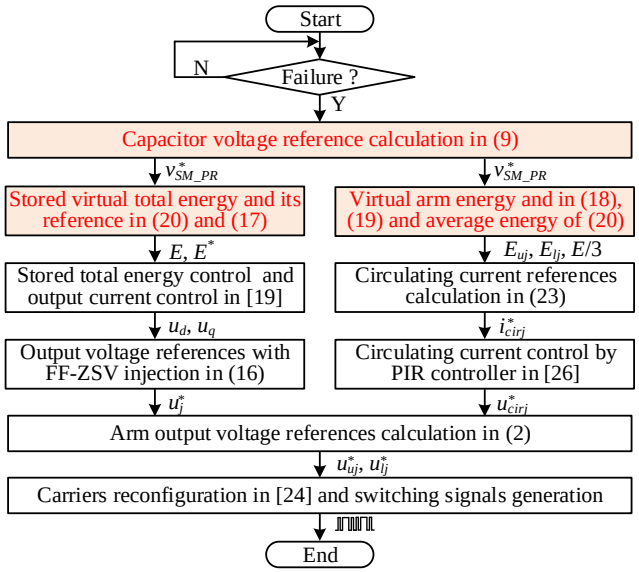

Fig. 5. Flowchart of the proposed approach under fault-tolerant operation.

where v_{SMujk} and v_{SMljk} are the capacitor voltages in the upper and lower arms, respectively; Ω_{uj} and Ω_{lj} are the order number sets of the faulty SMs in the upper and lower arms, respectively. E_{uj} and E_{lj} (j=a, b, c.) are the virtual arm energy in the upper and lower arms, respectively.

Based on (18) and (19), the stored virtual total energy E can be defined as

$$E = \sum_{j=a,b,c} (E_{uj} + E_{lj}). \tag{20}$$

The stored virtual total energy E will be used for the total energy regulation in **Part I** and the average energy calculation in each phase in **Part III**. The virtual arm energy E_{uj} and E_{lj} will be used for the arm energy regulation in **Part III**.

3) Principle of Part III

During the fault-tolerant operation, the arm energy will be unequally distributed, which is analyzed as follows. Suppose the output currents of the MMC-based STATCOM are

$$\begin{cases} i_a = I_p \cos(\omega t + \varphi_i) \\ i_b = I_p \cos(\omega t - 2\pi/3 + \varphi_i) \\ i_c = I_p \cos(\omega t + 2\pi/3 + \varphi_i) \end{cases} \tag{21}$$

where I_p and φ_i are the amplitude and phase angle of the output currents, respectively (φ_i=π/2 or $-\pi$/2).

The active power flow among three phases brought by the FF-ZSV injection can be expressed as

$$\begin{cases} P_a = V_0 I_p \cos(\varphi_i) \\ P_b = V_0 I_p \cos(\varphi_i - 2\pi/3). \\ P_c = V_0 I_p \cos(\varphi_i + 2\pi/3) \end{cases} \tag{22}$$

It can be seen that during fault-tolerant operation conditions, the FF-ZSV injection leads to unbalanced power flow among three phases. In addition, the asymmetric SM configuration causes unbalanced power flow between the upper and lower arms. Therefore, the arm energy balancing control is necessary.

According to [1], the dc circulating currents can be injected to balance the active power between three phases, and the fundamental frequency circulating currents can be injected to balance the arm energy between the upper and lower arms. The defined stored virtual total energy (E) and virtual energy of the upper and lower arms (E_{uj} and E_{lj}) are used to balance the arm energy, and the final circulating current references in **Part III** can be expressed as

$$\begin{bmatrix} i^*_{cira} \\ i^*_{cirb} \\ i^*_{circ} \end{bmatrix} = K_{p1}\left(\frac{E}{3} - \begin{bmatrix} E_{la}+E_{ua} \\ E_{lb}+E_{ub} \\ E_{lc}+E_{uc} \end{bmatrix}\right) + K_{p2}\frac{\Phi}{\sqrt{3}}\begin{bmatrix} E_{la}-E_{ua} \\ E_{lb}-E_{ub} \\ E_{lc}-E_{uc} \end{bmatrix} \tag{23}$$

where i^*_{cirj} is the circulating current reference; K_{p1} and K_{p2} are the control parameters; Φ is the middle transfer matrix, which can be expressed as

$$\Phi = \begin{bmatrix} \sqrt{3}\cos\omega t & \cos(\omega t + \pi/2) & \cos(\omega t - \pi/2) \\ \cos(\omega t - 7\pi/6) & \sqrt{3}\cos(\omega t - 2\pi/3) & \cos(\omega t - \pi/6) \\ \cos(\omega t + 7\pi/6) & \cos(\omega t + \pi/6) & \sqrt{3}\cos(\omega t + 2\pi/3) \end{bmatrix}. \tag{24}$$

By the above circulating current reference adjustments, the arm energy balancing control can be realized.

To accurately track their reference values and suppress the second-order components, proportional-integral-resonant (PIR) controllers are usually used to control the circulating currents, as discussed in [26]. In addition, it is necessary to save about 5% modulation margin for the circulating current control [26].

4) Flowchart of the proposed approach

The flowchart of the proposed approach under fault-tolerant operation is shown in Fig. 5. When the SM failures are detected, firstly, the capacitor voltage reference in all SMs is calculated, and the stored total energy of all capacitors in the MMC-based STATCOM is regulated. Then, the FF-ZSV is injected to generate balanced line-to-line voltages, and the output currents are controlled. Next, to balance the capacitor voltages between each arm, the circulating current references are calculated based on the defined virtual arm energy, and PIR controllers are used to control the circulating current. With the above steps, references for the output current control and circulating current control can be calculated, and the arm modulation references can be further derived based on (2). In addition, the number and the phase shift angles of the carriers need to be reconfigured, as discussed in [24], and the switching signals can be generated.

B. Comparison with the Conventional methods

To better illustrate the advantages of the proposed approach, its operation region is compared with the conventional hot-reserve-based fault-tolerant control method. According to (5) and (6), when the fault index is smaller than 1, the capacitor voltages of the conventional hot-reserve-based method will be

$$v^*_{SM\_HR} = v_{dc}/[N(1+n_r-n_r n_f)]. \tag{25}$$

For the proposed operation approach, the capacitor voltage can be derived based on (9) and (15).

$$\begin{cases} v^*_{SM\_PR} = \dfrac{-3f(n_r,n_f) + \sqrt{9f^2(n_r,n_f) + 12\left(1-f^2(n_r,n_f)\right)}}{2N\left(1-f^2(n_r,n_f)\right)(1+n_r)} v_{dc} \\ f(n_r,n_f) = (1+n_r-n_r n_f)/(1+n_r) \end{cases} \tag{26}$$

For the conventional hot-reserve-based fault-tolerant control method, the maximum allowable fault index is 1. For the proposed fault-tolerant operation approach, the maximum capacitor voltage should meet the constraint

$$v^*_{SM\_PR} \le v_{dc}/N. \tag{27}$$

TABLE I COMPARISON WITH OTHER EXISTING FAULT-TOLERANT OPERATION APPROACHES

Approaches	Capacitor voltage increment	Modulation wave changes	Crucial factors for tolerant ability	dc-link voltage	Fault-tolerant capability	Applications
Pulse redistribution [18]	No	No	①: No. of inserted SMs	Fixed	Low	MMC-based BESS
FF-ZSV [11]	No	Yes	②: The modulation margin ($m = 2U_g/v_{dc}$)	Fixed	Low	MMC
SHE [15],[16]	No	No		Fixed		Cascaded H-bridge
FF-ZSV+dc shift [13]	No	Yes		Fixed	Low	MMC
THV injection [12]	No	Yes	Fixed tolerant ability: Modulation margin increases by about 15.47 %	Fixed	Medium Fixed	MMC
Overmodulation [19]	No	No		Adjustable		MMC-based STATCOM
SVM [17]	No	No		Fixed		MMC
Cold-reserve [21]	No	No	③: No. of redundant SMs	Fixed	Medium	MMC
Hot reserve [22]	Yes, in the faulty arm	No	③: No. of redundant SMs	Fixed		MMC
Hot-reserve [25]	Yes, in the faulty arm	Yes	Both ② and ③	Fixed	Medium	MMC
Proposed	**Yes, in all SMs**	**Yes**	**Both ② and ③**	**Increment**	**High**	**MMC-based STATCOM**

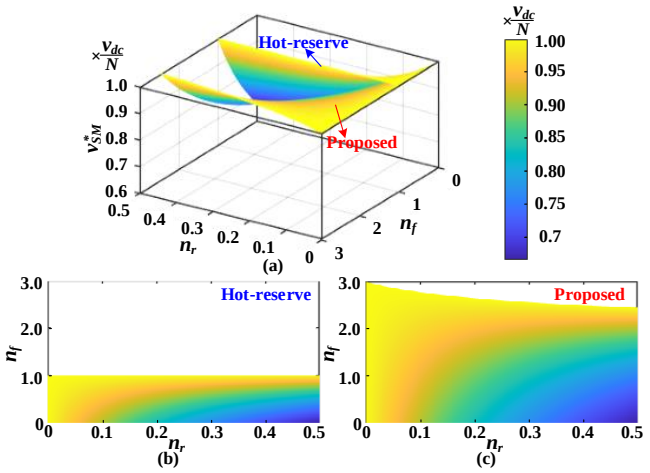

Fig. 6. Operation capability comparison with the conventional hot-reserve-based method. (a) Capacitor voltages, (b) operation region of the hot-reserve-based method in [22], and (c) operation region of the proposed approach.

Therefore, the allowable fault index of the proposed approach meets the constraint

$$\frac{-3f(n_r,n_f)+\sqrt{9f^2(n_r,n_f)+12\left(1-f^2(n_r,n_f)\right)}}{2\left(1-f^2(n_r,n_f)\right)(1+n_r)} \le 1 \qquad (28)$$

Based on the above derivations, the necessary capacitor voltages for the two fault-tolerant operation approaches are compared in Fig. 6. As shown in Fig. 6(a), with the same redundant index n_r and fault index n_f, the proposed approach requires a lower capacitor voltage increment. The higher n_f is, the more noticeable this phenomenon is. In addition, according to Figs. 6(b) and (c), the operation region of the proposed approach can be extended. The lower the redundant index is, the more noticeable this phenomenon is. The above analysis indicates that the proposed approach has a significantly enhanced operation capability under multiple SM failures than the conventional hot-reserve-based fault-tolerant control method.

More comparisons with the existing methods are listed in Table I. When SM failures occur, the conventional methods usually increase the SM voltages in the faulty arm or inject a relative-high-magnitude FF-ZSV. Hence, their fault-tolerant operation capability depends on either the modulation margin (decided by the amplitude of grid voltages) or the redundant SM configurations. In contrast, the operation capability of the proposed approach is influenced by both the above factors. Some other methods in [12], [17], and [19] make full use of the linear-modulation region, and the modulation margin can be increased by about 15.47%. In addition, most of the existing methods are designed for the MMCwith a fixed dc-link voltage. However, the proposed approach acquires an adjustable dc-link voltage due to the floating dc-link voltage. The dc-link of the MMC is also floating in [19], but its dc-link voltage remains at a fixed value. In contrast, the proposed approach can obtain a higher fault-tolerant operation capability by flexible dc-link voltage adjustment and small-magnitude FF-ZSV injection.

IV. SIMULATION RESULTS

The MMC-based STATCOM simulation model is built, and the parameters are listed in Table II. Fault-tolerant operation results of the conventional hot-reserve-based method and the proposed approach are shown in Figs. 7 and 8, respectively.

A. Operation of the Conventional Hot-Reserve-Based Method

As shown in Fig. 7, from 0.15 s to 0.25 s, the amplitude of the output currents in the MMC-based STATCOM is 100 A, and the capacitor voltages are stable at about 1 kV during normal operation conditions. The maximum number of inserted SM in the upper arm in phase *a* is 10. At 0.25 s, the first SM failure occurs, the amplitude of the output currents remains at about 100 A. With the conventional control method, the capacitor voltages increase to about 1.11 kV in the upper arm, and the maximum number of inserted SMs in the upper arm reduces to 9. At 0.35 s, the second SM failure occurs, the output currents remain almost the same. The capacitor voltages in the faulty arm increase to about 1.25 kV while the remaining SMs remains at about 1 kV. In addition, the maximum number of inserted SMs decreases to 8. Then, at 0.45 s, the third SM failure occurs. The capacitor voltages cannot increase and

TABLE II SYSTEM PARAMETERS

Items		Symbols	Simulation	Experiment
Rated dc-link voltage		v_{dc}	10 kV	200 V
ac line-to-line voltage		U_{gl}	5.5 kV	98 V
Arm inductor	**Inductance**	L_{arm}	3 mH	5 mH
	Resistance	R_{arm}	0.0942 Ω	0.3 Ω
ac inductor	**Inductance**	L	2 mH	2.5 mH
	Resistance	R	0.0628 Ω	0.15 Ω
Carrier frequency		$f_{carrier}$	2 kHz	5 kHz
SM number per arm		N	8	3
Number of redundant SM		N_r	2	1
SM capacitance		C	2 mF	3.84 mF

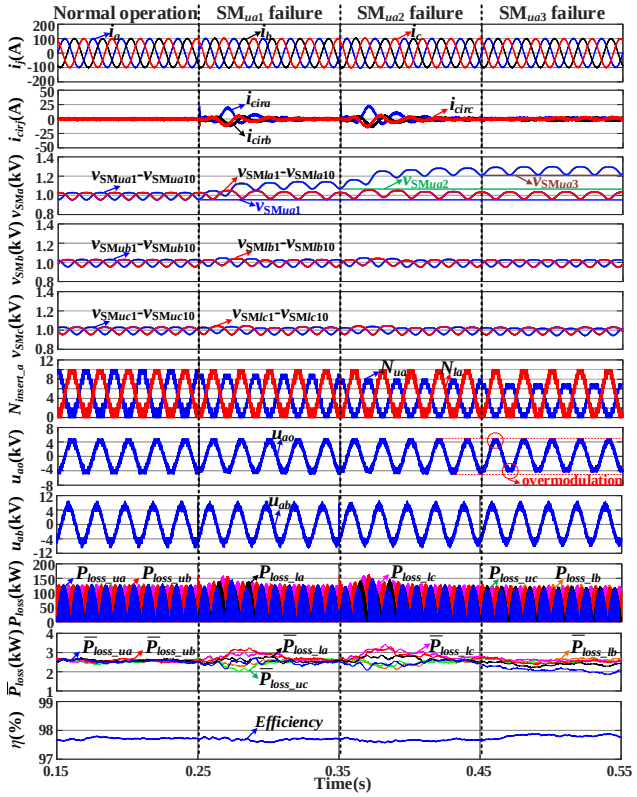

Fig. 7. Simulation results of the conventional hot-reserve-based fault-tolerant control method under SM failures in the upper arm in phase *a*.

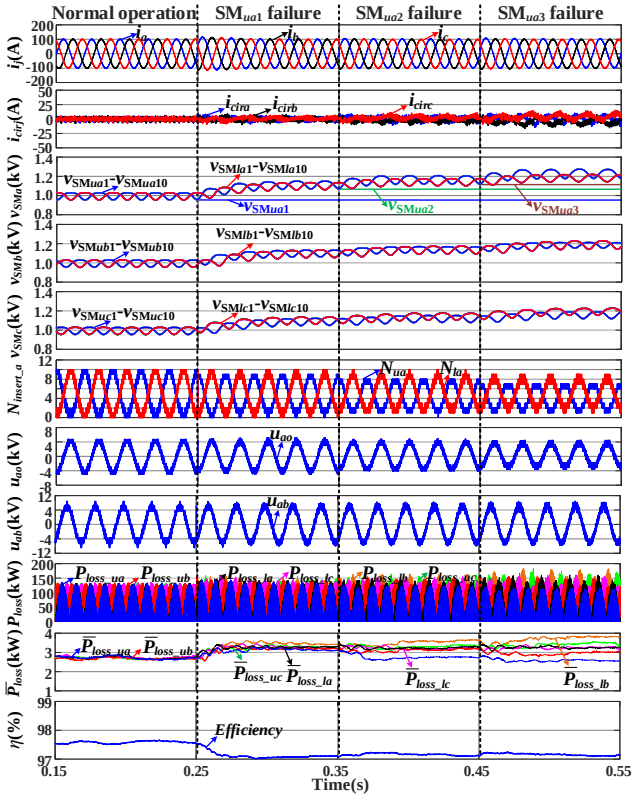

Fig. 8. Simulation results of the proposed fault-tolerant operation approach under SM failures in the upper arm in phase *a*.

remain at about 1.25 kV, and the MMC enters the overmodulation region. At this time, the arm output voltage is asymmetric, and the MMC-based STATCOM will operate with distorted waveforms due to the overmodulation operation [19].

Considering the IGBT and diode loss, the total power loss analysis can be expressed as

$$P_{\text{loss\_total}} = \sum P_{\text{loss\_IGBT}} + \sum P_{\text{loss\_diode}} \tag{29}$$

where $P_{\text{loss\_total}}$ is the total power loss of each SM; $P_{\text{loss\_IGBT}}$ is the power loss of the IGBT; $P_{\text{loss\_diode}}$ is the power loss of the diode. $P_{\text{loss\_IGBT}}$ and $P_{\text{loss\_diode}}$ can be further expanded as

$$\begin{cases} P_{\text{loss\_IGBT}} = P_{\text{cond\_T}} + P_{\text{switch\_T}} \\ P_{\text{loss\_diode}} = P_{\text{cond\_D}} + P_{\text{switch\_D}} \end{cases}. \tag{30}$$

where $P_{\text{cond\_T}}$ and $P_{\text{switch\_T}}$ are the conduction and switching loss of the IGBT, respectively; $P_{\text{cond\_D}}$ and $P_{\text{switch\_D}}$ are the conduction and switching loss of the diode, respectively.

According to [27], the conduction losses of the IGBT and diode can be expressed as

$$\begin{cases} P_{\text{cond\_T}} = f_0 \int_0^{1/f_0} S_{\text{T}} u_{\text{cond\_T}}(i_{\text{T}}, T_{j\_\text{T}}) i_{\text{T}} dt \\ P_{\text{cond\_D}} = f_0 \int_0^{1/f_0} S_{\text{D}} u_{\text{cond\_D}}(i_{\text{D}}, T_{j\_\text{D}}) i_{\text{D}} dt \end{cases}. \tag{31}$$

where f_0 is the fundamental frequency; S_{T} and S_{D} are the conduction function of the IGBT and diode, respectively; i_{T} and i_{D} are the current flowing through the IGBT and diode, respectively; $u_{\text{cond\_T}}$ and $u_{\text{cond\_D}}$ are the on-state voltage drops across the IGBT and diode, respectively, which are related to the current and junction temperatures. The relation between on-state voltage drops ($u_{\text{cond\_T}}$, $u_{\text{cond\_D}}$) and the junction temperature (T_{j_T}, T_{j_D}) can be found in the datasheet.

According to [28], the switching loss of the IGBT and diode can be expressed as

$$\begin{cases} P_{\text{switch\_T}} = f_0 \sum_{i=1}^{k} [E_{on\_\text{T}}(i_{\text{T}}, T_{j\_\text{T}}) + E_{off\_\text{T}}(i_{\text{T}}, T_{j\_\text{T}})] \\ P_{\text{switch\_D}} = f_0 \sum_{i=1}^{k} [E_{rec\_\text{D}}(i_{\text{D}}, T_{j\_\text{D}})] \end{cases}. \tag{32}$$

where E_{on_T} and E_{on_T} are the switching-on and -off the energy of the IGBT, respectively; E_{rec_D} is the switching energy of the diode. According to [27], they can be further expressed as

$$\begin{cases} E_{sw\_\text{T}}(i_{\text{T}}, T_{j\_\text{T}}) = E_{on\_\text{T}}(i_{\text{T}}, T_{j\_\text{T}}) + E_{off\_\text{T}}(i_{\text{T}}, T_{j\_\text{T}}) \\ \qquad\qquad = E_{sw\_\text{T}}(i_{\text{T}})[1 + K_{\text{T}}(T_{j\_\text{T}} - T_{ref\_\text{T}})] \\ E_{rec\_\text{D}}(i_{\text{D}}, T_{j\_\text{D}}) = E_{sw\_\text{D}}(i_{\text{D}})[1 + K_{\text{D}}(T_{j\_\text{D}} - T_{ref\_\text{D}})] \end{cases}, \tag{33}$$

where more detailed parameters can be found in the datasheet.

The thermal and power loss are conducted with the IGBT module 5SNE0800M170100. Operation parameters of the IGBT and diode can be found in the datasheet. As shown in Fig. 7, the average power loss in each arm is almost equal to about

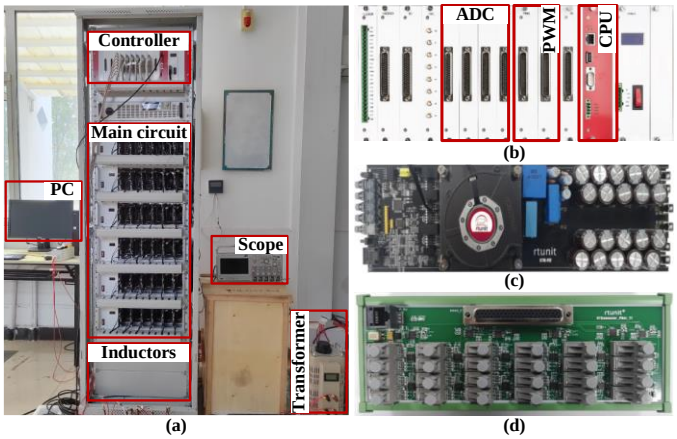

Fig. 9. Laboratory prototype of the MMC-based STATCOM. (a) MMC setup, (b) central controller, (c) SM board, and (d) fiber signal transition board.

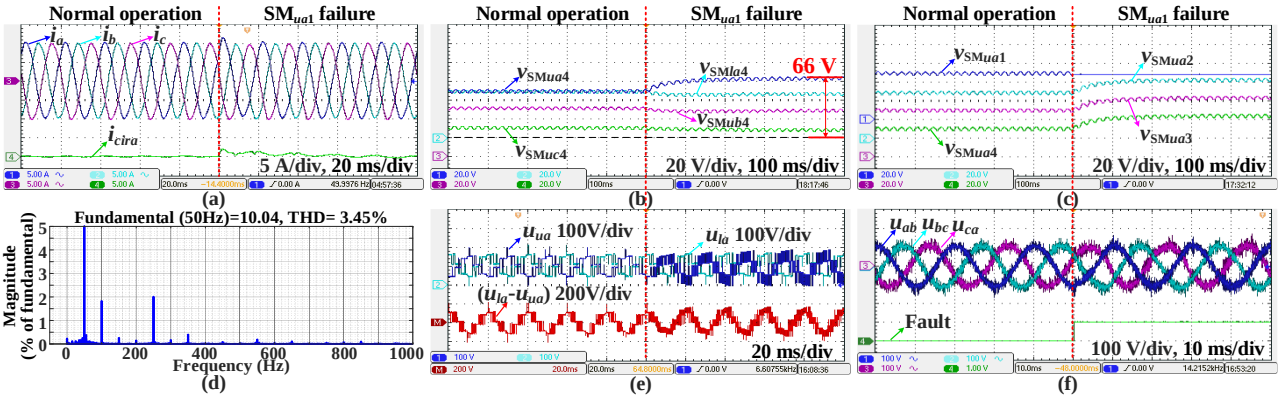

Fig. 10. Experimental results of the conventional hot-reserve-based method under single SM failure in phase *a*. (a) Output currents and circulating current, (b) three-phase capacitor voltages, (c) capacitor voltages in the faulty arm, (d) post-fault steady-state THD values, (e) arm output voltages, and (f) line-to-line voltages.

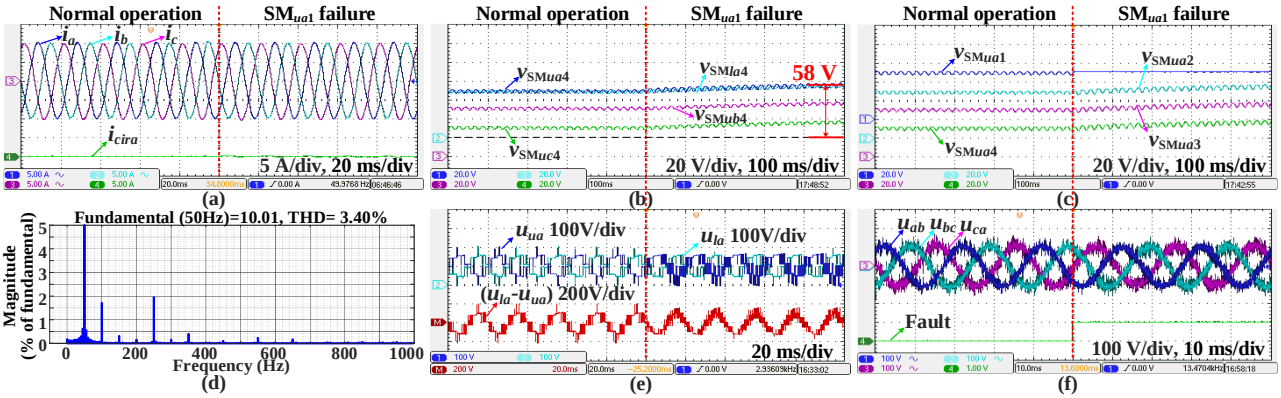

Fig. 11. Experimental results of the proposed fault-tolerant operation approach under single SM failure in phase *a*. (a) Output currents and circulating current, (b) three-phase capacitor voltages, (c) capacitor voltages in the faulty arm, (d) post-fault steady-state THD values, (e) arm output voltages, and (f) line-to-line voltages.

2.57 kW, and the efficiency is about 97.71%.

B. Operation of the Proposed Approach

As shown in Fig. 8, from 0.15 s to 0.25 s, the MMC-based STATCOM is in normal operation conditions, where the amplitude of the output currents is 100 A, and the capacitor voltages are stable at about 1 kV. At 0.25 s, the first SM failure occurs. The amplitude of the output currents remains at about 100 A. With the proposed fault-tolerant operation approach, the capacitor voltages increase to about 1.09 kV, which corresponds with the results calculated by (9) and (15). The maximum number of inserted SMs in the upper arm reduces to 9, but the line-to-line voltages remain the same as steady-state operation. The second SM failure occurs at 0.35 s, and number of faulty SMs is is equal to the number of redundant SMs. At this time, the amplitude of the output currents is still about 100 A. The capacitor voltages in three phases increase to about 1.13 kV, and the maximum number of inserted SMs decreases to 8 in the faulty arm. In addition, the output phase voltage decreases while the line-to-line voltages remain almost the same. The third SM failure occurs at 0.45 s, where the faulty SMs outnumber the redundant SMs. For the proposed approach, the faulty SMs are bypassed, and the capacitor voltages in the remaining SMs increase to about 1.18 kV. It is noted that in this condition, the injected FF-ZSV influences the active power flow in three phases. Therefore, dc circulating currents are injected to balance the arm energy. When SM failure occurs, the maximum number of inserted SMs decreases to 7. The output voltage in phase *a* decreases, but the line-to-line voltages remain the same as normal operation conditions. Therefore, the effectiveness of the proposed approach is verified under severe SM failures ($N_f > N_r$), and the proposed fault-tolerant operation approach has an enhanced operation capability under multiple SM failures.

The thermal and power loss analysis of the proposed approach is conducted, and the results are shown in Fig. 8. When the SM faults occur, the power loss in each arm becomes different. It can be seen that the more SM faults, the higher power loss differences. In addition, when the fault-tolerant operations begin, the average power loss in each arm is about 3.18 kW, and the average efficiency is about 97.16%.

V. Experimental Results

The MMC-based STATCOM laboratory prototype in Fig. 9 is used to verify the effectiveness of the proposed approach. Fig. 9(a) shows the overall profile of the MMC setup. Fig. 9(b) shows the central controller. Fig. 9(c) shows the SM board, and Fig. 9(d) shows the fiber signal transition board. The control algorithm is implemented in the DSP digital process controller, and the FPGA is applied to generate the driving signals of power switches. These driving signals are sent to the local SM board through optical fibers, while the SM voltage and current values are sent to the central controller through optical fibers. More detailed circuit parameters are listed in Table II.

A. SM_{ua1} Failure

Experimental results of the conventional hot-reserve-based

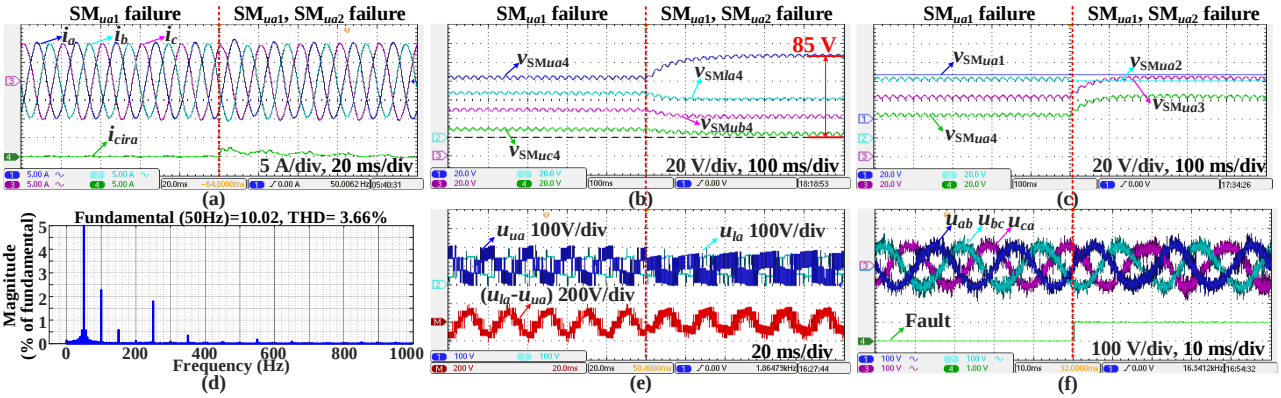

Fig. 12. Experimental results of the conventional hot-reserve-based method under two SM failures in phase *a*. (a) Output currents and circulating current, (b) three-phase capacitor voltages, (c) capacitor voltages in the faulty arm, (d) post-fault steady-state THD values, (e) arm output voltages, and (f) line-to-line voltages.

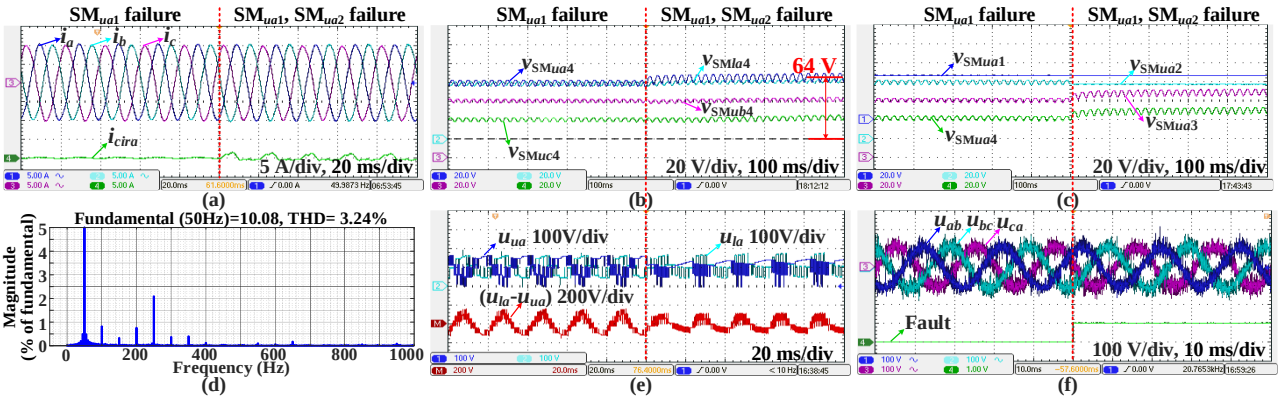

Fig. 13. Experimental results of the proposed fault-tolerant operation approach under two SM failures in phase *a*. (a) Output currents and circulating current, (b) three-phase capacitor voltages, (c) capacitor voltages in the faulty arm, (d) post-fault steady-state THD values, (e) arm output voltages, and (f) line-to-line voltages.

method and the proposed approach under single SM failure are shown in Figs. 10 and 11, respectively. As shown in Figs. 10(a) and 11(a), when the first SM failure occurs in the upper arm in phase *a*, the output current waveforms are almost the same by these two methods. However, the circulating current ripple of the conventional method is higher than the proposed approach due to higher capacitor voltages increment. The three-phase capacitor voltages are shown in Figs. 10(b) and 11(b). The voltages only increase in the upper arm, and the values are about 66 V by the conventional method. In comparison, the capacitor voltages increase in three phases by the proposed method, and the values are about 58 V. Detailed capacitor voltages in the faulty arm are shown in Figs. 10(c) and 11(c). The post-fault steady-state THD values are shown in Figs. 10(d) and 11(d), which are about 3.45% and 3.40%, respectively. The arm output and phase voltages are shown in Figs. 10(e) and 11(e), where the maximum number of inserted SMs decreases from 4 to 3 in the faulty arm. In addition, the amplitude of phase voltage by the conventional method is higher compared with the proposed approach. As shown in Figs. 10(f) and 11(f), the line-to-line voltages remain almost the same under both approaches when the SM failure occurs.

The above results verify the effectiveness of the proposed approach under $N_f < N_r$. In addition, the proposed approach requires a lower capacitor voltage increment in the faulty arm and has a balanced distribution of voltage stress in all SMs.

B. SM_{ua1} *and* SM_{ua2} *Failures*

Experimental results of the conventional hot-reserve-based method and the proposed approach under two SM failures are shown in Figs. 12 and 13. It is noted when the second SM failure occurs in the MMC prototype, it meets $N_f > N_r$, and the MMC enters a severe overmodulation region by the conventional method. In this condition, the MMC-based STATCOM cannot be accurately controlled.

When the second SM failure occurs in the upper arm in phase *a*, the output currents remain the same with a little fluctuation, as shown in Figs. 12(a) and 13(a), due to the adjustment of the capacitor voltages. In addition, the circulating current injections increase slightly to balance the arm energy when the second SM failure occurs. As shown in Fig. 12(b), the capacitor voltages in the faulty arm increase from about 66 V to about 85 V by the conventional method, which are not well regulated and exceeds the limit. In practical application, it could cause damage to the device. In comparison, the three-phase capacitor voltages increase from about 58 V to about 64 V by the proposed approach, as shown in Fig. 13(b), which is equal to the reference value. In addition, the three-phase voltage balancing process of the conventional method is slower due to the internal arm energy balancing. Figs. 12(c) and 13(c) show the capacitor voltages in the upper arm in phase *a*, where the faulty SMs are both bypassed, and their capacitor voltages almost keep constant. The post-fault steady-state THD values are shown in Figs. 12(d) and 13(d), which are about 3.66% and 3.24%, respectively. The output voltage waveforms in the arm and lower arms are shown in Figs. 12(e) and 13(e), where the output levels

decrease from 3 to 2 when the second SM failure occurs. The line-to-line voltages are shown in Figs. 12(f) and 13(f), which remain almost the same after the second SM failure.

The above results validate the effectiveness and advantages of the proposed fault-tolerant operation approach under $N_f > N_r$.

VI. Conclusion

In this paper, a novel fault-tolerant operation approach has been proposed for the MMC-based STATCOM. By capacitor voltage increment in all SMs and FF-ZSV injection, the operation capability can be enhanced under multiple SM failures. Based on the simulation and experimental results, the following conclusion can be summarized:

1) Under minor failure conditions when the redundant SMs outnumber the faulty SMs, the proposed approach requires a lower capacitor voltage increment than the conventional hot-reserve-based fault-tolerant control method.

2) Under severe failure conditions, when the faulty SMs outnumber the redundant SMs, the proposed approach can still realize stable operation within the specified security region.

3) By the virtual energy idea, the arm energy is well balanced, and an even voltage stress distribution is achieved in the healthy SMs, even during fault-tolerant operations.

Nevertheless, this paper only discussed the single-phase SM failure conditions. For multi-phase failure conditions, interpretable machine learning solutions such as [29] could be adopted to effectively improve the system operation capability. This will be discussed in future research work.

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