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Advanced 2*N*+1 Submodule Unified PWM with Reduced DC-Link Current Ripple for Modular Multilevel Converters

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***Abstract*-The 2*N*+1 submodule unified PWM (SUPWM) is attractive for modular multilevel converters (MMCs). In order to generate 2*N*+1 voltage levels, the SUPWM results in voltage pulses imposed on the arm inductors, which produces large high-frequency current ripple in the dc link of the MMC and deteriorates the dc-link performance. In this paper, the dc-link high-frequency current ripple under 2*N*+1 SUPWM is analyzed and a reduced dc-link current ripple control method is proposed for advanced 2*N*+1 SUPWM. By regulating the phase angles of the three-phase carriers in each carrier period, the resulted voltage pulses on the arm inductors of three phases can be counteracted, and therefore the dc-link high-frequency current ripple is suppressed. With the proposed method, the MMC has much reduced dc-link current ripple, which effectively improves the performance of the MMC under 2*N*+1 SUPWM. Simulations and experiments are conducted to verify the validity and effectiveness of the proposed control.**

***Index Terms*- Control strategy, dc-link current ripple, modular multilevel converters (MMCs), 2*N*+1 SUPWM.**

I. Introduction

Modular multilevel converters (MMCs) have aroused extensive research interests from both academia and industry since it was first presented in 2000s [1] and have received increasing attentions over the past decade [2]-[4]. It consists of many stacked submodules (SMs) with energy storage capacitors in the arms so that the dc-link capacitor is removed [5]. Compared with other existing multilevel converters, the MMC brings many merits, such as modularity, scalability, flexibility, common dc bus and high efficiency, which makes it a promising topology for high-power applications [6]-[8].

The dc-link current ripple is one of the issues for the MMC, which has been addressed by a number of research works so far [9]-[19]. It will distort the delivered dc-link current, deteriorate the dc-link power quality, result in extra losses and potential instability issues, and affect the power equipment connected to the dc link. Therefore, it is of significance to suppress the dc-link current ripple.

To date, a few literatures have focused on solving the fluctuations of the dc-link current for MMCs under faults, such as the unbalanced grid conditions [9], [10] and the submodule faults [11], [12]. However, the dc-link current ripple is also produced in the MMC under its normal operation, which has been addressed by some studies [13]-[21]. Depending on the different causes, these studies can be grouped into two categories. One category is that the dc-link current ripple is caused by the circulating current control. Reference [13] investigates the mechanism of the dc-link current ripple caused by circulating current suppression (CCS). Reference [14] presents a modified MMC topology by employing a CCS inverter and replacing the arm inductors with three-winding transformers. The current harmonics in the arms caused by CCS is absorbed by the submodule capacitors and does not flow into the dc link of the MMC with this topology, which achieves lower dc-link current ripple and better dc-link power quality. Reference [15] develops an arm inductor selection rule for the MMC considering the effect of CCS under the submodule unified PWM (SUPWM), which can reduce the high-frequency harmonics of the arm current and the dc-link current ripple. Reference [16] presents a hybrid modulation-based control, where the ac-side voltage is modulated by the nearest level modulation (NLM) and the CCS voltage is modulated by the PWM. The dc-link current ripple is reduced compared with the conventional NLM. Reference [17] presents a dc-link high-frequency current ripple eliminating control method by employing the two-group carriers-based phase-disposition PWM (PD-PWM), where the ac-side voltage and the CCS voltage are modulated separately by different group of carriers. Reference [18] presents a control method based on the improved two-group multicarrier PD-PWM to suppress the dc-link current ripple caused by the CCS. Reference [19] presents a model predictive control method considering the dc-link current, where the dc-link current ripple caused by high-frequency circulating current injection is reduced. The other category is that the dc-link current ripple is caused by the carriers' configuration in modulation. In [20], a carrier phase shifted PWM (CPS-PWM) method with modified phase shifting angles is presented, which would lead to high-frequency current ripple in the dc link of the MMC. To solve the problem, [21] presents a control method based on the regulation of the phase-shifted angles of the carrier waves, which can eliminate the dc-link current ripple.

The technique that applying carriers with same phase angles for both the upper arm and lower arm of one phase-leg is widely used in the MMC, where the maximum ac output voltage levels can increase from *N*+1 to 2*N*+1. The ac side voltage harmonics analysis with this technique under various modulation schemes has been conducted in [22], [23]. But

little attention has been paid on the dc-link current performance of the MMC. The SUPWM is attractive for its lower computational burden and relatively small control complexity [15], [24]-[28]. Reference [27] presents the 2*N*+1 SUPWM, which has better ac voltage quality in comparison with the *N*+1 SUPWM. The ac voltage spectrums of 2*N*+1 SUPWM are also given in [28]. However, the number of total inserted SMs in each phase of the MMC under 2*N*+1 modulation does not always equal *N*, but varies among *N*-1, *N*, and *N*+1. Consequently, the 2*N*+1 SUPWM causes voltage pulses imposed on the arm inductors and produces high-frequency current harmonics in the arm current, which further results in a large current ripple in the dc link of the MMC. Unfortunately, it has not been discussed and solved yet.

In this paper, the dc-link high-frequency current ripple caused by 2*N*+1 SUPWM is analyzed in detail. A reduced dc-link current ripple control method is proposed to suppress the dc-link high-frequency current ripple of the three-phase MMC under 2*N*+1 SUPWM. Through shifting the phase angles of the carriers in phases A, B and C, respectively, in each carrier period, the high-frequency current ripple in the dc link of the MMC can be eliminated, which effectively improves the performance of the MMC. The primary contributions of this paper are: 1) it reveals the dc-link current ripple under conventional 2*N*+1 SUPWM theoretically, 2) it proposes an advanced 2*N*+1 SUPWM method to reduce the dc-link current ripple without affecting the phase voltage quality in comparison with [27].

The rest of this paper is organized as follows. Section II introduces the operation principle of the MMC. Section III analyzes the 2*N*+1 SUPWM and the resulted dc-link high-frequency current ripple. Section IV proposes a reduced dc-link current ripple control method. Sections V and VI present the simulation and experimental results, respectively, to demonstrate the effectiveness and validity of the proposed control. Finally, Section VII draws the conclusions.

II. Description Of MMCs

Fig. 1 shows a three-phase MMC, which consists of six arms. The upper arm and lower arm of one phase make up a phase-leg. Each arm has *N* identical SMs and an arm inductor L_s. Each SM consists of a storage capacitor C_{SM} and two switches T_1, T_2. The SM mainly has two states in normal operation. If T_1 is switched on and T_2 is switched off, the SM is "Inserted" and the SM output voltage equals the capacitor voltage u_c. If T_1 is switched off and T_2 is switched on, the SM is "Bypassed" and the SM output voltage equals zero.

With the capacitor voltage balancing control [26], the capacitor voltage in the MMC can be kept balanced as

$$U_C=U_{dc}/N \tag{1}$$

where U_{dc} is the dc-link voltage of the MMC.

According to [29], the ac electromotive force (EMF) in phase *j* (*j*=*a*, *b*, *c*) of the MMC is

$$u_{ej}=\frac{u_{lj}-u_{uj}}{2} \tag{2}$$

with

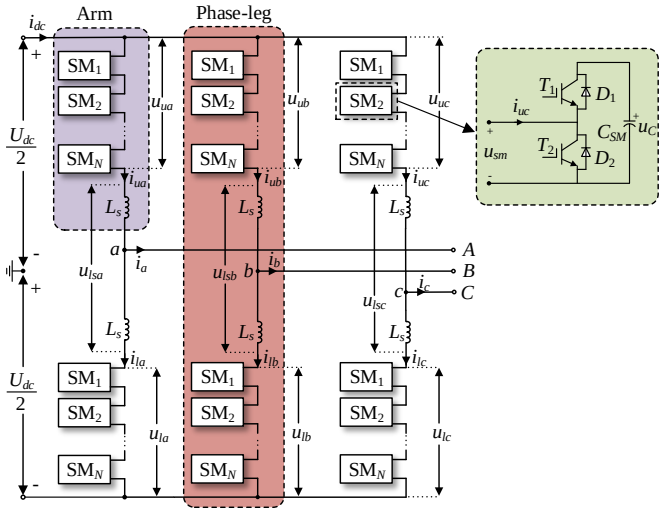


Fig. 1. Three-phase MMC.

$$\begin{cases} u_{uj}=\sum_{i=1}^{N}u_{smuj\_i} \\ u_{lj}=\sum_{i=1}^{N}u_{smlj\_i} \end{cases} \tag{3}$$

where u_{uj} and u_{lj} are the total output voltages of the series-connected SMs in the upper arm and lower arm of phase *j*, respectively. u_{smuj_i} and u_{smlj_i} are, respectively, the *i*-th SM output voltage in the upper arm and lower arm of phase *j*.

In Fig. 1, the total voltage u_{lsj} on the upper and lower arm inductors of phase *j* is

$$u_{lsj}=U_{dc}-(u_{uj}+u_{lj}) \tag{4}$$

III. Analysis of DC-Link Current Ripple for MMCs under 2*N*+1 SUPWM

A. MMCs under 2N+1 SUPWM

In the MMC, the reference voltages u_{uj_ref} and u_{lj_ref} for the upper and lower arm of phase *j* are expressed as

$$\begin{cases} u_{uj\_ref}=U_{dc}(1-y_j)/2 \\ u_{lj\_ref}=U_{dc}(1+y_j)/2 \end{cases} \tag{5}$$

with

$$\begin{cases} y_a=m\cos(\omega_0 t) \\ y_b=m\cos(\omega_0 t-2\pi/3) \\ y_c=m\cos(\omega_0 t+2\pi/3) \end{cases} \tag{6}$$

where y_j is the reference for phase *j*. *m* is the modulation index and ω_0 is angular frequency.

In the SUPWM, in order to generate the upper arm reference voltage u_{uj_ref} and lower arm reference voltage u_{lj_ref}, there are always K_{uj} and K_{lj} SMs fully inserted in the upper arm and lower arm, respectively, as

$$\begin{cases} K_{uj}=\mathrm{floor}\left(\frac{u_{uj\_ref}}{U_C}\right)=\mathrm{floor}\left(\frac{N}{2}(1-y_j)\right) \\ K_{lj}=\mathrm{floor}\left(\frac{u_{lj\_ref}}{U_C}\right)=\mathrm{floor}\left(\frac{N}{2}(1+y_j)\right) \end{cases} \tag{7}$$

where the function floor(x) is to take the integer part of x. On the other hand, in order to compensate the error introduced by floor(x) in the SUPWM, one SM working in the form of pulse with the duty of D_{uj} and D_{lj}, which is called as "switching SM", is introduced for the upper and lower arm respectively, where $0<D_{uj}, D_{lj}<1$. In the SUPWM, the D_{uj} and D_{lj} are

$$\begin{cases} D_{uj} = \dfrac{N}{2}\left(1-y_j\right)-K_{uj} \\ D_{lj} = \dfrac{N}{2}\left(1+y_j\right)-K_{lj} \end{cases} \tag{8}$$

with

$$\begin{cases} D_{uj}+D_{lj}=1 \\ K_{uj}+K_{lj}=N-1 \end{cases} \tag{9}$$

Fig. 2 shows the control scheme for phase j of the MMC under $2N$+1 SUPWM [27]. In every carrier period, the $2N$+1 SUPWM for the upper arm (lower arm) includes two parts. One part is K_{uj} (K_{lj}), which is obtained based on (7). In the other part, D_{uj} (D_{lj}) is obtained based on (8), which is compared with an isosceles triangle carrier W_{uj} (W_{lj}). The W_{uj} (W_{lj}) is between 0 and 1. If D_{uj} (D_{lj})>W_{uj} (W_{lj}), the output of this part is 1. If D_{uj} (D_{lj})<W_{uj} (W_{lj}), the output of this part is 0. The sum of above two parts is n_{uj} (n_{lj}), which is the number of SMs to be inserted for the upper arm (lower arm). Afterwards, according to n_{uj} (n_{lj}), all SM capacitor voltages u_{Cuj1}~u_{CujN} (u_{Clj1}~u_{CljN}) in the arm and the direction of the arm current i_{uj} (i_{lj}), the driving signals for all SMs in the arm can be properly generated based on the capacitor voltage balancing control to ensure capacitor voltage balance.

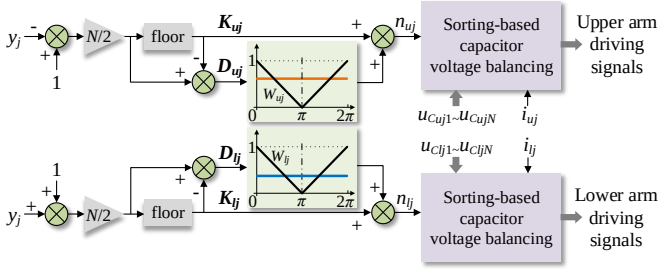


Fig. 2. MMC control scheme with $2N$+1 SUPWM.

B. Inductor Voltage u_{lsj} under 2N+1 SUPWM

According to (1)~(3) and Fig. 2, the EMF in phase j of the MMC can be expressed as

$$u_{ej} = \frac{n_{lj}-n_{uj}}{2}U_C \tag{10}$$

According to (1), (3), (4) and Fig. 2, the total voltage on the upper arm and lower arm inductors of phase j can be written as

$$u_{lsj} = U_{dc} - \left(n_{uj}+n_{lj}\right)U_C \tag{11}$$

Fig. 3 shows the $2N$+1 SUPWM for phase j of the MMC in one carrier period, where the carrier waves W_{uj} for the upper arm and W_{lj} for the lower arm are of same phase angle. The carrier frequency is f_s and $\omega_s=2\pi f_s$. The whole carrier period can be divided into five intervals I~V. The $2N$+1 SUPWM would have two cases for the MMC depending on the duty D_{uj} and D_{lj}, as shown in Figs. 3(a) and (b), respectively.

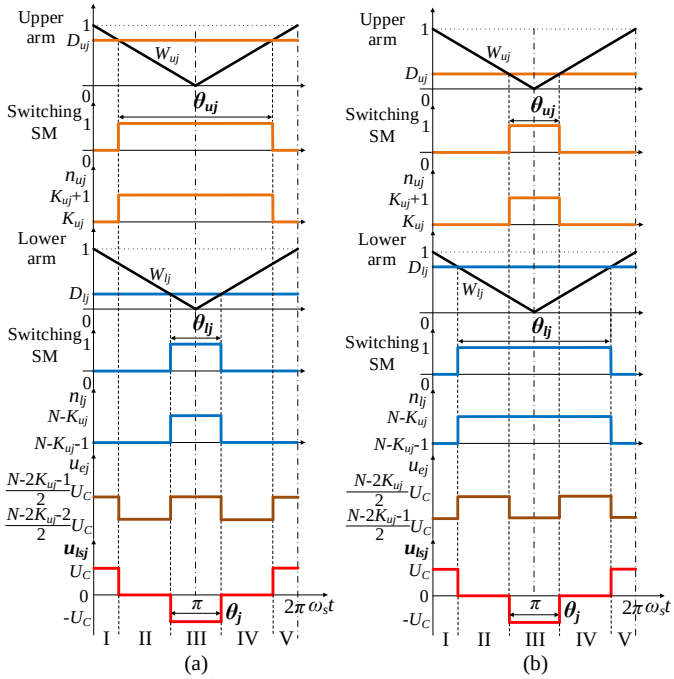


Fig. 3. $2N$+1 SUPWM for MMCs. (a) D_{uj}>0.5>D_{lj}, (b) D_{uj}<0.5<D_{lj}.

1) Case-1: D_{uj}>0.5>D_{lj}, as shown in Fig. 3(a). For the upper arm, the switching SM equals 0 in I, V and equals 1 in II, III and IV. Thus, the number of the inserted SMs in the upper arm is between K_{uj} and K_{uj}+1. For the lower arm, the switching SM equals 0 in I, II, IV, V and equals 1 in III. Thus, the number of the inserted SMs in the lower arm is between N-K_{uj}-1 and N-K_{uj}. According to (10), the u_{ej} is between U_C(N-2K_{uj}-2)/2 and U_C(N-2K_{uj}-1)/2. According to (11), the total voltage u_{lsj} on the upper and lower arm inductors of phase j can be obtained as follows.

- Intervals I & V: the number of inserted SMs in phase j is N-1, and accordingly the arm inductors withstand a positive voltage as $u_{lsj}=U_C$.
- Intervals II & IV: the number of inserted SMs in phase j is N, and accordingly u_{lsj} is zero.
- Interval III: the number of inserted SMs in phase j is N+1, and accordingly the arm inductors withstand a negative voltage as $u_{lsj}=-U_C$.

2) Case-2: D_{uj}<0.5<D_{lj}, as shown in Fig. 3(b). For the upper arm, the switching SM equals 0 in I, II, IV, V and equals 1 in III. Thus, the number of the inserted SMs in the upper arm is between K_{uj} and K_{uj}+1. For the lower arm, the switching SM equals 0 in I and V and equals 1 in II, III, IV. Thus, the number of the inserted SMs in the lower arm is between N-K_{uj}-1 and N-K_{uj}. According to (10), the u_{ej} is between U_C(N-2K_{uj}-1)/2 and U_C(N-2K_{uj})/2. In Case-2, the u_{lsj} has the same three states as in Case-1, as shown in Fig. 3.

Based on the above analysis, it can be observed that the pulse widths θ_{uj} and θ_{lj} of the switching SM in the upper arm and lower arm of phase j, as shown in Fig. 3, can be calculated as

$$\begin{cases} \theta_{uj} = D_{uj}\cdot 2\pi \\ \theta_{lj} = D_{lj}\cdot 2\pi = (1-D_{uj})\cdot 2\pi \end{cases} \tag{12}$$

The inductor voltage u_{lsj} has a positive pulse and a negative pulse in one carrier period. The middle point of the negative pulse is always at $\omega_s t=\pi$ and the middle point of the positive pulse is always at $\omega_s t=0$ (2π). The durations of the positive pulse and negative pulses in u_{lsj} in one carrier period are the same, which can be easily obtained as

$$\theta_j = \min(\theta_{uj}, \theta_{lj}) \tag{13}$$

C. DC-Link High-Frequency Current Ripple under 2N+1 SUPWM

Using the Fourier Series Expansion, the arm inductor voltage u_{lsj} in phase j, as shown in Fig. 3, can be expressed as

$$u_{lsj} = \frac{2}{\pi}\frac{U_{dc}}{N}\sum_{k=1}^{\infty}\frac{1}{k}\left[1-\cos(k\pi)\right]\sin\frac{k\theta_j}{2}\cos(k\omega_s t) \tag{14}$$

where k is index of the summation terms in Fourier Series Expansion. Obviously, the u_{lsj} would bring high-frequency current harmonics in phase j, which will flow into the dc link of MMCs and cause current ripple related to the carrier frequency. According to (14) and Fig. 1, the resulted high-frequency component i_{dc_h} in the dc-link current of MMCs can be obtained as

$$\begin{aligned} i_{dc\_h} &= \frac{1}{2L_s}\int(u_{lsa}+u_{lsb}+u_{lsc})dt \\ &= \frac{U_{dc}}{\pi N\omega_s L_s}\sum_{k=1}^{\infty}\left[\frac{1-\cos(k\pi)}{k^2}\cdot(\sin\frac{k\theta_a}{2}+\sin\frac{k\theta_b}{2}\right. \\ &\quad \left.+\sin\frac{k\theta_c}{2})\cdot\sin(k\omega_s t)\right] \end{aligned} \tag{15}$$

According to (15), it can be observed that the i_{dc_h} does not contain the even order component, but contains odd order components. Usually, there is $\sin(k\theta_a/2)+\sin(k\theta_b/2)+\sin(k\theta_c/2)\neq 0$. Consequently, a high-frequency current ripple would exist in the dc link of the MMC, which would deteriorate dc-link performance of the MMC. Fig. 4 illustrates the diagram of the total voltages on the upper and lower arm inductors in phase A, B and C and the resulted dc-link current ripple Δi_{dc} (peak-to-peak value of the dc-link current i_{dc}) in one carrier period.

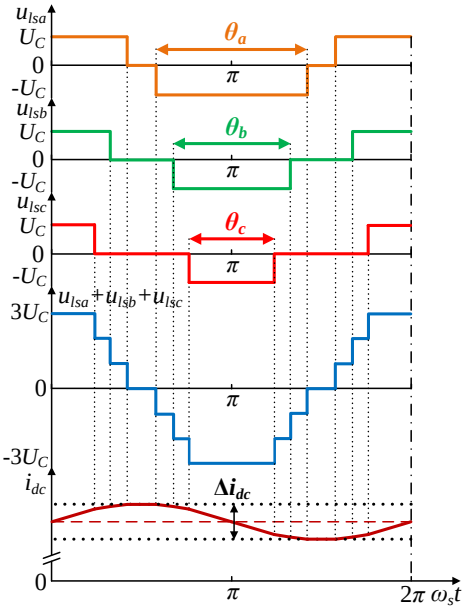


Fig. 4. Arm inductor voltages of phase A, B, C and dc-link current.

Fig. 5 shows the calculated amplitudes of the first-, third-, fifth- and seventh- order components of i_{dc_h} in the MMC under various carrier frequencies, which is based on the simulation system parameters in Table II. The dc-link high-frequency current mainly contains the fundamental component at the carrier frequency and the other components are much smaller than the component at the carrier frequency. Fig. 6 shows the calculated maximum value of Δi_{dc} in the MMC under various carrier frequencies. Along with the reduction of the carrier frequency, the dc-link high-frequency current ripple is gradually increased.

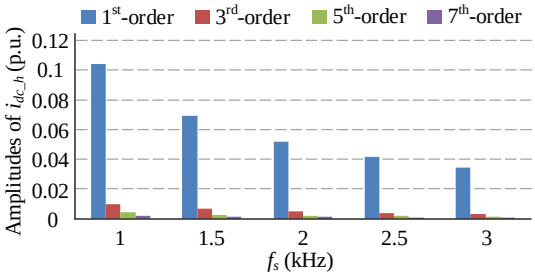


Fig. 5. Amplitudes of the first-, third-, fifth-, and seventh- order components of i_{dc_h} under various carrier frequencies.

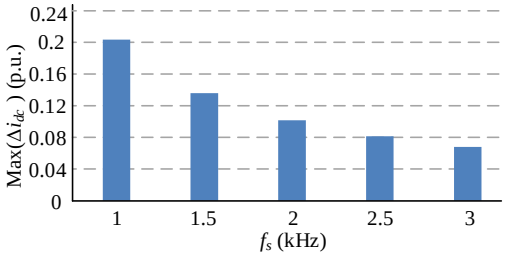


Fig. 6. Maximum Δi_{dc} under various carrier frequencies.

IV. Proposed Reduced DC-Link Current Ripple Control Method

A. Analysis of Relationships among Inductor Voltage Pulse Widths θ_a, θ_b and θ_c

For the MMC under 2N+1 SUPWM, according to (6)~(8), the relationship among D_{ua}, D_{ub} and D_{uc} (D_{la}, D_{lb} and D_{lc}) can be obtained as

$$\begin{cases} \sum_{j=a,b,c} D_{uj} = \dfrac{3N}{2} - \sum_{j=a,b,c} K_{uj} \\ \sum_{j=a,b,c} D_{lj} = 3 - \sum_{j=a,b,c} D_{uj} \end{cases} \tag{16}$$

In the MMC, the SM number N is normally even [30]-[32]. According to (12) and (13), the MMC would have eight operation modes under 2N+1 SUPWM, as shown in Table I, as follows.

- Mode-1: $D_{ua}\geq 0.5$, $D_{ub}\geq 0.5$, and $D_{uc}\geq 0.5$. According to (16), there is $D_{ua}+D_{ub}+D_{uc}=2$. According to (13), there are $\theta_a=(1-D_{ua})\cdot 2\pi$, $\theta_b=(1-D_{ub})\cdot 2\pi$, $\theta_c=(1-D_{uc})\cdot 2\pi$. Obviously, it can be observed that $\theta_a+\theta_b+\theta_c=2\pi$.

- Mode-2: D_{ua}<0.5, D_{ub}<0.5, and D_{uc}<0.5. According to (16), there is $D_{ua}+D_{ub}+D_{uc}=1$. According to (13), there are $\theta_a=D_{ua}\cdot 2\pi$, $\theta_b=D_{ub}\cdot 2\pi$, $\theta_c=D_{uc}\cdot 2\pi$. Obviously, it can be observed that $\theta_a+\theta_b+\theta_c=2\pi$.
- Mode-3: $D_{ua}\geq$0.5, D_{ub}<0.5, and D_{uc}<0.5. According to (16), there is $D_{ua}+D_{ub}+D_{uc}=1$. According to (13), there are $\theta_a=(1-D_{ua})\cdot 2\pi$, $\theta_b=D_{ub}\cdot 2\pi$, $\theta_c=D_{uc}\cdot 2\pi$. Obviously, it can be observed that $-\theta_a+\theta_b+\theta_c=0$.
- Mode-4: $D_{ua}\geq$0.5, D_{ub}<0.5, and $D_{uc}\geq$0.5. According to (16), there is $D_{ua}+D_{ub}+D_{uc}=2$. According to (13), there are $\theta_a=(1-D_{ua})\cdot 2\pi$, $\theta_b=D_{ub}\cdot 2\pi$, $\theta_c=(1-D_{uc})\cdot 2\pi$. Obviously, it can be observed that $\theta_a-\theta_b+\theta_c=0$.
- Mode-5: $D_{ua}\geq$0.5, $D_{ub}\geq$0.5, and D_{uc}<0.5. According to (16), there is $D_{ua}+D_{ub}+D_{uc}=2$. According to (13), there are $\theta_a=(1-D_{ua})\cdot 2\pi$, $\theta_b=(1-D_{ub})\cdot 2\pi$, $\theta_c=D_{uc}\cdot 2\pi$. Obviously, it can be observed that $\theta_a+\theta_b-\theta_c=0$.
- Mode-6: D_{ua}<0.5, $D_{ub}\geq$0.5, and $D_{uc}\geq$0.5. According to (16), there is $D_{ua}+D_{ub}+D_{uc}=2$. According to (13), there are $\theta_a=D_{ua}\cdot 2\pi$, $\theta_b=(1-D_{ub})\cdot 2\pi$, $\theta_c=(1-D_{uc})\cdot 2\pi$. Obviously, it can be observed that $-\theta_a+\theta_b+\theta_c=0$.
- Mode-7: D_{ua}<0.5, $D_{ub}\geq$0.5, and D_{uc}<0.5. According to (16), there is $D_{ua}+D_{ub}+D_{uc}=1$. According to (13), there are $\theta_a=D_{ua}\cdot 2\pi$, $\theta_b=(1-D_{ub})\cdot 2\pi$, $\theta_c=D_{uc}\cdot 2\pi$. Obviously, it can be observed that $\theta_a-\theta_b+\theta_c=0$.
- Mode-8: D_{ua}<0.5, D_{ub}<0.5, and $D_{uc}\geq$0.5. According to (16), there is $D_{ua}+D_{ub}+D_{uc}=1$. According to (13), there are $\theta_a=D_{ua}\cdot 2\pi$, $\theta_b=D_{ub}\cdot 2\pi$, $\theta_c=(1-D_{uc})\cdot 2\pi$. Obviously, it can be observed that $\theta_a+\theta_b-\theta_c=0$.

From Table I, it can be seen that the widths θ_a, θ_b and θ_c of the three-phase inductor pulse voltage u_{lsa}, u_{lsb} and u_{lsc} mainly have two types of relationships, as follows.

- Type-I: the sum of θ_a, θ_b, and θ_c are equal to 2π.
- Type-II: one inductor voltage pulse's width is the sum of the other two inductor voltage pulses' widths.

TABLE I
RELATIONSHIPS AMONG θ_a, θ_b AND θ_c

Type	Mode	D_{ua}	D_{ub}	D_{uc}	Sum of D_{ua}, D_{ub}, D_{uc}	Relationships among θ_a, θ_b, θ_c
I	1	≥0.5	≥0.5	≥0.5	2	$\theta_a+\theta_b+\theta_c=2\pi$
	2	<0.5	<0.5	<0.5	1	$\theta_a+\theta_b+\theta_c=2\pi$
II	3	≥0.5	<0.5	<0.5	1	$-\theta_a+\theta_b+\theta_c=0$
	4	≥0.5	<0.5	≥0.5	2	$\theta_a-\theta_b+\theta_c=0$
	5	≥0.5	≥0.5	<0.5	2	$\theta_a+\theta_b-\theta_c=0$
	6	<0.5	≥0.5	≥0.5	2	$-\theta_a+\theta_b+\theta_c=0$
	7	<0.5	≥0.5	<0.5	1	$\theta_a-\theta_b+\theta_c=0$
	8	<0.5	<0.5	≥0.5	1	$\theta_a+\theta_b-\theta_c=0$

B. Proposed Carriers-Phase-Shifting Approach

In order to suppress the dc-link high-frequency current i_{dc_h}, the upper arm carrier W_{uj} and the lower arm carrier W_{lj} for phase j in Fig. 3 are both phase-shifted by an angle denoted as θ_{sj} ($-\pi\leq\theta_{sj}\leq\pi$). If $\theta_{sj}>0$, the W_{uj} and W_{lj} in Fig. 3 are phase-shifted to the left by $|\theta_{sj}|$. If $\theta_{sj}<0$, the W_{uj} and W_{lj} in Fig. 3 are phase-shifted to the right by $|\theta_{sj}|$. If $\theta_{sj}=0$, the W_{uj} and W_{lj} in Fig. 3 are not phase-shifted.

Considering the phase-shifted angle θ_{sa}, θ_{sb} and θ_{sc} in phase A, B and C of the MMC, the dc-link high-frequency current can be derived in a similar way like (14) and (15), as

$$\begin{aligned} i_{dc\_h} &= \frac{1}{2L_s}\int (u_{lsa}+u_{lsb}+u_{lsc})dt \\ &= \frac{U_{dc}}{\pi N\omega_s L_s}\cdot\sum_{k=1}^{\infty}\left\{\frac{1-\cos(k\pi)}{k^2}\cdot[\cos(k\theta_{sa})\sin\frac{k\theta_a}{2}\right. \\ &\left.+\cos(k\theta_{sb})\sin\frac{k\theta_b}{2}+\cos(k\theta_{sc})\sin\frac{k\theta_c}{2}]\cdot\sin(k\omega_s t)\right\} \end{aligned} \tag{17}$$

Based on (17) and Table I, a carrier phase-shifting approach is proposed to obtain suitable phase-shifted angles θ_{sa}, θ_{sb} and θ_{sc}, so as to eliminate the dc-link high-frequency current as $i_{dc\_h}=0$, as follows.

1) If $\theta_a>\theta_b>\theta_c$, then

$$\theta_{sa}=0 \tag{18a}$$

$$\theta_{sb}=\begin{cases}-(\theta_{ua}+\theta_{ub})/2, & \theta_{ua}+\theta_{ub}\leq 2\pi\\ 2\pi-(\theta_{ua}+\theta_{ub})/2, & \theta_{ua}+\theta_{ub}>2\pi\end{cases} \tag{18b}$$

$$\theta_{sc}=\begin{cases}(\theta_{ua}+\theta_{uc})/2, & \theta_{ua}+\theta_{uc}\leq 2\pi\\ (\theta_{ua}+\theta_{uc})/2-2\pi, & \theta_{ua}+\theta_{uc}>2\pi\end{cases} \tag{18c}$$

2) If $\theta_a>\theta_c>\theta_b$, then

$$\theta_{sa}=0 \tag{19a}$$

$$\theta_{sb}=\begin{cases}(\theta_{ua}+\theta_{ub})/2, & \theta_{ua}+\theta_{ub}\leq 2\pi\\ (\theta_{ua}+\theta_{ub})/2-2\pi, & \theta_{ua}+\theta_{ub}>2\pi\end{cases} \tag{19b}$$

$$\theta_{sc}=\begin{cases}-(\theta_{ua}+\theta_{uc})/2, & \theta_{ua}+\theta_{uc}\leq 2\pi\\ 2\pi-(\theta_{ua}+\theta_{uc})/2, & \theta_{ua}+\theta_{uc}>2\pi\end{cases} \tag{19c}$$

3) If $\theta_b>\theta_a>\theta_c$, then

$$\theta_{sa}=\begin{cases}-(\theta_{ub}+\theta_{ua})/2, & \theta_{ub}+\theta_{ua}\leq 2\pi\\ 2\pi-(\theta_{ub}+\theta_{ua})/2, & \theta_{ub}+\theta_{ua}>2\pi\end{cases} \tag{20a}$$

$$\theta_{sb}=0 \tag{20b}$$

$$\theta_{sc}=\begin{cases}(\theta_{ub}+\theta_{uc})/2, & \theta_{ub}+\theta_{uc}\leq 2\pi\\ (\theta_{ub}+\theta_{uc})/2-2\pi, & \theta_{ub}+\theta_{uc}>2\pi\end{cases} \tag{20c}$$

4) If $\theta_b>\theta_c>\theta_a$, then

$$\theta_{sa}=\begin{cases}(\theta_{ub}+\theta_{ua})/2, & \theta_{ub}+\theta_{ua}\leq 2\pi\\ (\theta_{ub}+\theta_{ua})/2-2\pi, & \theta_{ub}+\theta_{ua}>2\pi\end{cases} \tag{21a}$$

$$\theta_{sb}=0 \tag{21b}$$

$$\theta_{sc}=\begin{cases}-(\theta_{ub}+\theta_{uc})/2, & \theta_{ub}+\theta_{uc}\leq 2\pi\\ 2\pi-(\theta_{ub}+\theta_{uc})/2, & \theta_{ub}+\theta_{uc}>2\pi\end{cases} \tag{21c}$$

5) If $\theta_c>\theta_a>\theta_b$, then

$$\theta_{sa}=\begin{cases}-(\theta_{uc}+\theta_{ua})/2, & \theta_{uc}+\theta_{ua}\leq 2\pi\\ 2\pi-(\theta_{uc}+\theta_{ua})/2, & \theta_{uc}+\theta_{ua}>2\pi\end{cases} \tag{22a}$$

$$\theta_{sb}=\begin{cases}(\theta_{uc}+\theta_{ub})/2, & \theta_{uc}+\theta_{ub}\leq 2\pi\\ (\theta_{uc}+\theta_{ub})/2-2\pi, & \theta_{uc}+\theta_{ub}>2\pi\end{cases} \tag{22b}$$

$$\theta_{sc}=0 \tag{22c}$$

6) If $\theta_c>\theta_b>\theta_a$, then

$$\theta_{sa}=\begin{cases}(\theta_{uc}+\theta_{ua})/2, & \theta_{uc}+\theta_{ua}\le 2\pi\\ (\theta_{uc}+\theta_{ua})/2-2\pi, & \theta_{uc}+\theta_{ua}>2\pi\end{cases} \tag{23a}$$

$$\theta_{sb}=\begin{cases}-(\theta_{uc}+\theta_{ub})/2, & \theta_{uc}+\theta_{ub}\le 2\pi\\ 2\pi-(\theta_{uc}+\theta_{ub})/2, & \theta_{uc}+\theta_{ub}>2\pi\end{cases} \tag{23b}$$

$$\theta_{sc}=0 \tag{23c}$$

Fig. 7 shows the carriers-phase-shifting approach in one carrier period for the two types in Table I, as follows.

1) Type I: Fig. 7(a) illustrates the phase-shifting of the carriers in phase A, B and C for the Type I in Table I. Here, the Mode 2 in Table I is considered with D_{ua}<0.5, D_{ub}<0.5, D_{uc}<0.5. The three-phase arm inductor pulses' widths meet $\theta_a>\theta_b>\theta_c$. According to the proposed approach, θ_{sa}=0 and the carriers for phase A is not phase-shifted; the carriers for phase B here is phase-shifted to the left by θ_{sb}=-(θ_{ua}+θ_{ub})/2; the carriers for phase C here is phase-shifted to the right by θ_{sc}=(θ_{ua}+θ_{uc})/2. The inductor voltage pulses in phase A, B, and C are counteracted in the whole carrier period so that u_{sla}+u_{slb}+u_{slc}=0. As a result, the dc-link high-frequency current i_{dc_h} can be effectively eliminated. The analysis for the other Modes in Type I is similar to that for the Mode 2, which is not repeated here.

2) Type II: Fig. 7(b) illustrates the phase-shifting of the carriers in phase A, B and C for the Type II in Table I. The Mode 3 in Table I is considered here with D_{ua}>0.5, D_{ub}<0.5, D_{uc}<0.5. The three-phase arm inductor pulses' widths meet $\theta_a>\theta_b>\theta_c$. According to the proposed approach, θ_{sa}=0 and the carriers for phase A is not phase-shifted; the carriers for phase B here is phase-shifted to the left by θ_{sb}=-(θ_{ua}+θ_{ub})/2; the carriers for phase C here is phase-shifted to the right by θ_{sc}=(θ_{ua}+θ_{uc})/2. The inductor voltage pulses in phase A, B, and C are counteracted in the whole carrier period so that u_{sla}+u_{slb}+u_{slc}=0. As a result, the dc-link high-frequency current i_{dc_h} can be eliminated effectively. The analysis for the other modes in Type II is similar to that for the Mode 3, which is not repeated here.

C. Proposed Reduced DC-Link Current Ripple Control

In order to improve the performance of the MMC under 2*N*+1 SUPWM, this paper proposes a reduced dc-link current ripple control method, as shown in Fig. 8. Through shifting the phase angles of the carriers in phases A, B and C, based on (18)~(23), the dc-link high-frequency current ripple can be suppressed.

Fig. 8(a) shows the calculation of the shifted angles θ_{sa}, θ_{sb} and θ_{sc}. In each carrier period, the widths θ_{ua}, θ_{ub}, θ_{uc} for the upper arm and the widths θ_{la}, θ_{lb}, θ_{lc} for the lower arm switching SMs of phase A, B and C are first calculated based on (6)~(8) and (12). Afterwards, the arm inductor voltage pulses' widths θ_a, θ_b and θ_c are obtained based on (13). Depending on the θ_a, θ_b, θ_c and θ_{ua}, θ_{ub}, θ_{uc}, the shifted angles θ_{sa}, θ_{sb} and θ_{sc} can be determined by (18)~(23). Depending on the θ_a, θ_b, θ_c and θ_{ua}, θ_{ub}, θ_{uc}, the shifted angles θ_{sa}, θ_{sb} and θ_{sc} can be determined by (18)~(23).

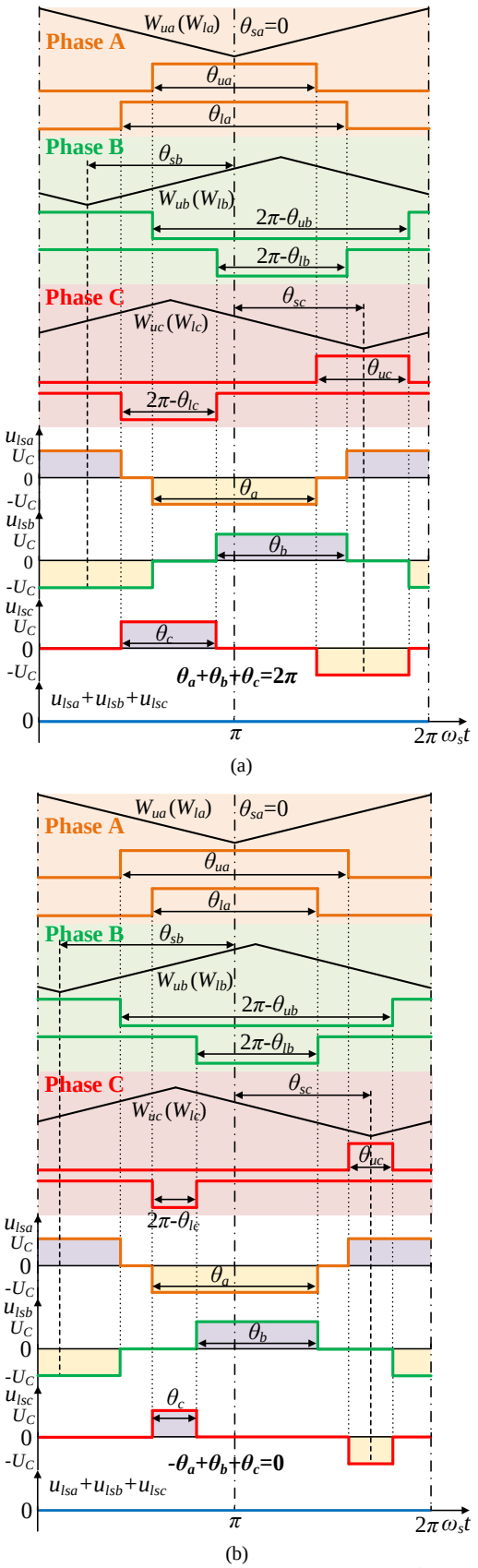


Fig. 7. Voltages u_{als}, u_{bls}, and u_{cls} under carriers' phase-shifting. (a) Type I, (b) Type II.

Fig. 8(b) shows the overall control block of the proposed control method in phase *j*. In each carrier period, based on Fig. 8(a), the carriers of the upper arm and lower arm in phase *j* are both phase-shifted by θ_{sj} to the right position. The modulation and the capacitor voltage balancing control are the same as that in Fig. 2.

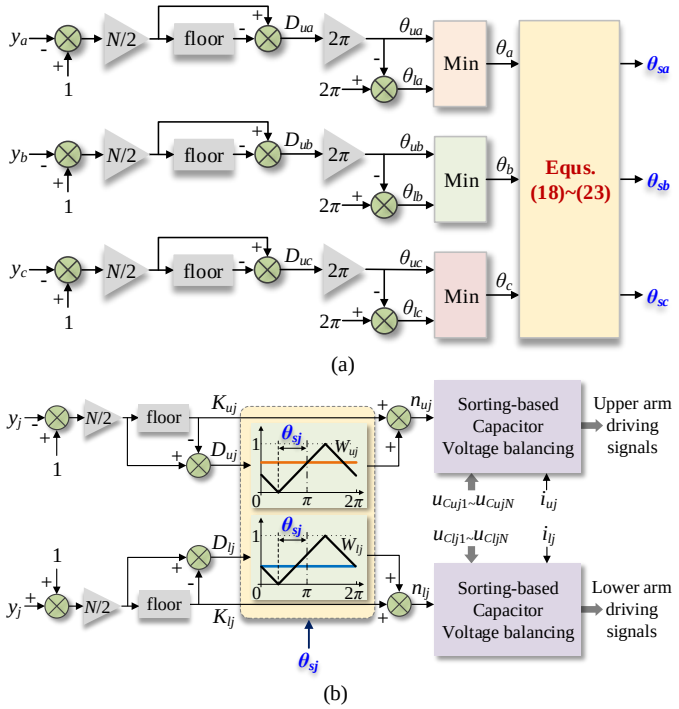


Fig. 8. Proposed control method. (a) Calculation of shifted angles θ_{sa}, θ_{sb} and θ_{sc}. (b) Overall control block of the proposed method in phase *j*.

V. Simulation

To verify the proposed control, a three-phase MMC connected to ac grid is simulated with PSCAD/EMTDC, as shown in Fig. 9. The parameters of the simulated system are shown in Table II.

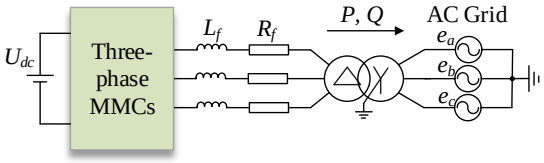


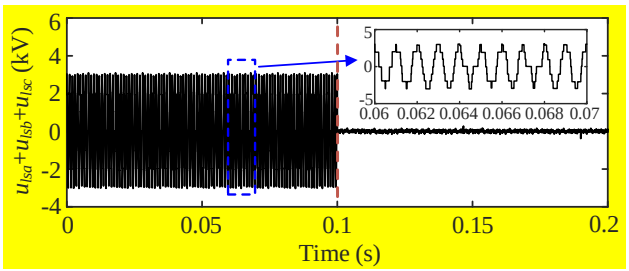
Fig. 9. Simulated system.

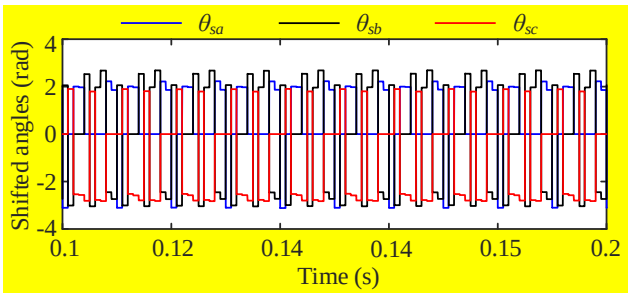
TABLE II
Simulation System Parameters

Parameter	Value
Rated active power *P* (MW)	3
DC-link voltage U_{dc} (kV)	6
Grid line-to-line voltage (kV)	33
Grid frequency (Hz)	50
Transformer voltage rating	3 kV/33 kV
Number of SMs per arm *N*	6
SM capacitance C_{sm} (mF)	6
Arm inductance L_s (mH)	5
Inductance L_f (mH)	1

In the simulation, the MMC works under 2*N*+1 SUPWM without proposed control before 0.1 s. At *t*=0.1 s, the proposed control is enabled. The carrier frequency is 1 kHz. The power factor angle φ=0.

Fig. 10 shows the dc-link performance of the MMC. Fig. 10(a) shows the sum of u_{sla}, u_{slb} and u_{slc}. Before *t*=0.1 s, it varies between -3kV and 3 kV. When the proposed control is enabled, the inductor voltage pulses of u_{sla}, u_{slb}, and u_{slc} are phase-shifted to be counteracted and the $u_{sla}+u_{slb}+u_{slc}$ equals zero. Fig. 10 (b) shows the shifted angles of the carriers in phase A, B and C with proposed control. Fig. 10 (c) shows the dc-link current of MMCs. Before *t*=0.1 s, i_{dc} has large current ripple, where the maximum Δi_{dc} reaches to 20.8% of the rated dc-link current. When the proposed control is enabled at *t*=0.1 s, the dc-link current ripple is eliminated dramatically.





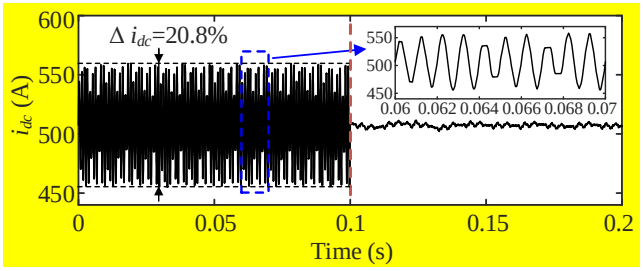
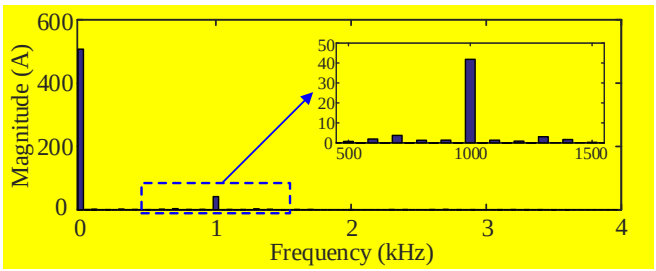
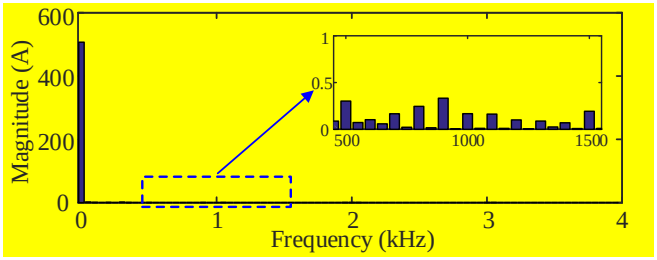


Fig. 10. The dc-link performance of the MMC. (a) sum of u_{sla}, u_{slb} and u_{slc}. (b) shifted angles of the carriers, (c) dc-link current.



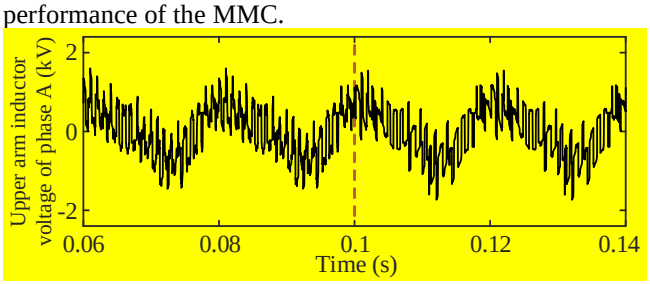


(b)

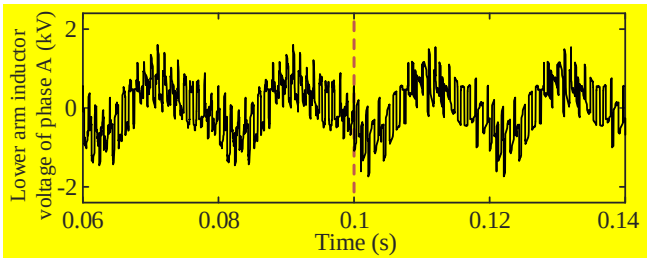
Fig. 11. FFT analysis of the dc-link current. (a) with 2*N*+1 SUPWM, (b) with proposed control.

Fig. 11 shows the FFT results of the dc-link current of the MMC. Fig. 11(a) shows the spectrum of i_{dc} without the proposed control. It can be seen that i_{dc} has a large component at the carrier frequency of 1 kHz. Fig. 11 (b) shows the spectrum of i_{dc} when the proposed control is used. It shows that the high-frequency component of i_{dc} is very small, which verifies the effectiveness of the proposed control.

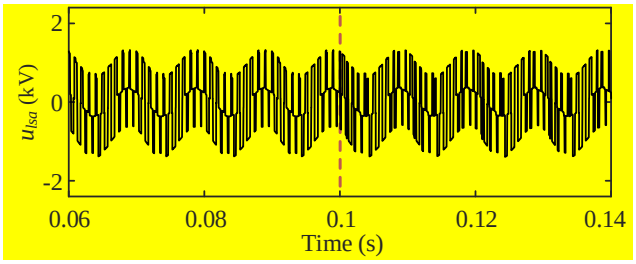
Figs. 12(a)~(c) show upper arm inductor voltage, lower arm inductor voltage and sum of upper and lower arm inductor voltages u_{lsa} of phase A, which have little change before t=0.1 s and after t=0.1 s. The proposed control does not increase the arm inductor voltage stress. Figs. 12(d)~(f) show arm currents, EMFs and grid currents, respectively. According to Fig. 12, the waveforms of arm currents, EMFs and grid currents have very small difference before t=0.1 s and after t=0.1 s, where the EMFs always have 13 voltage levels. The THD of the EMFs remains nearly unchanged after t=0.1 s. Therefore, the proposed control has little effect on the arm and ac-side performance of the MMC.



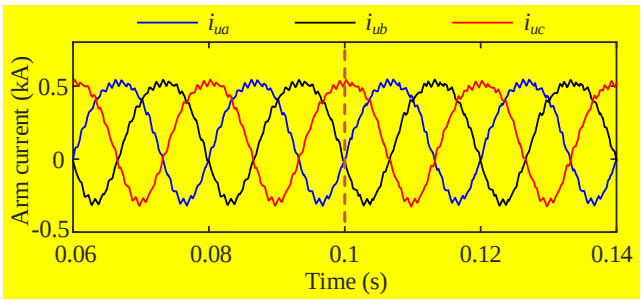
(a)



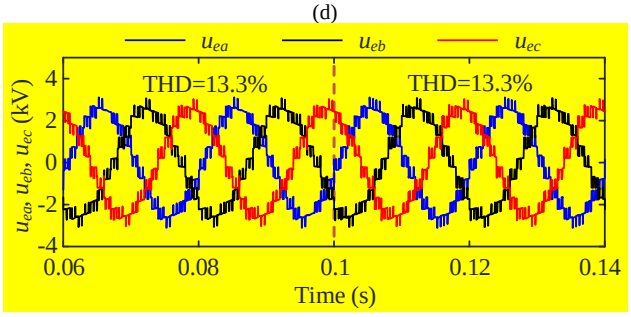
(b)



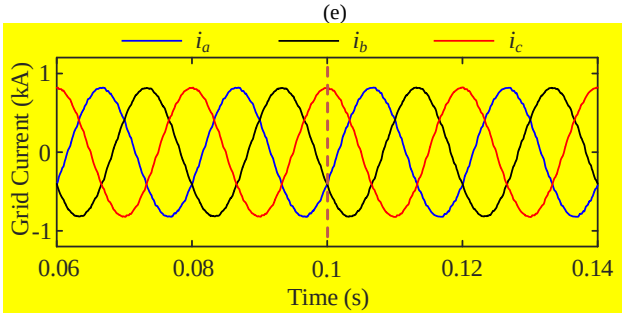
(c)



(d)



(e)



(f)

Fig. 12. MMC performance. (a) upper arm inductor voltage of phase A, (b) lower arm inductor voltage of phase A, (c) the sum of upper arm and lower arm inductor voltage of phase A, (d) arm currents i_{ua}, i_{ub} and i_{uc}, (e) EMFs u_{ea}, u_{eb} and u_{ec}, (f) grid currents i_a, i_b and i_c.

Fig. 13 shows the simulated results of the dc-link current ripple without the proposed control and with the proposed control under various carrier frequencies. The dc-link current ripple is reduced along with the increase of the carrier frequency. Besides, the dc-link current ripple is effectively suppressed with the proposed control in comparison with that without the proposed control.

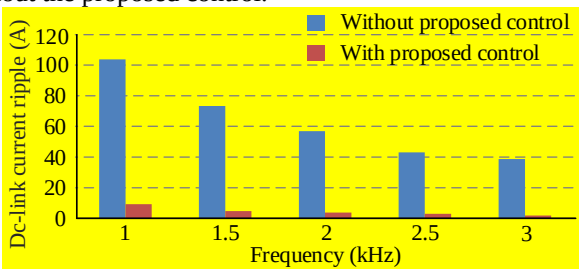
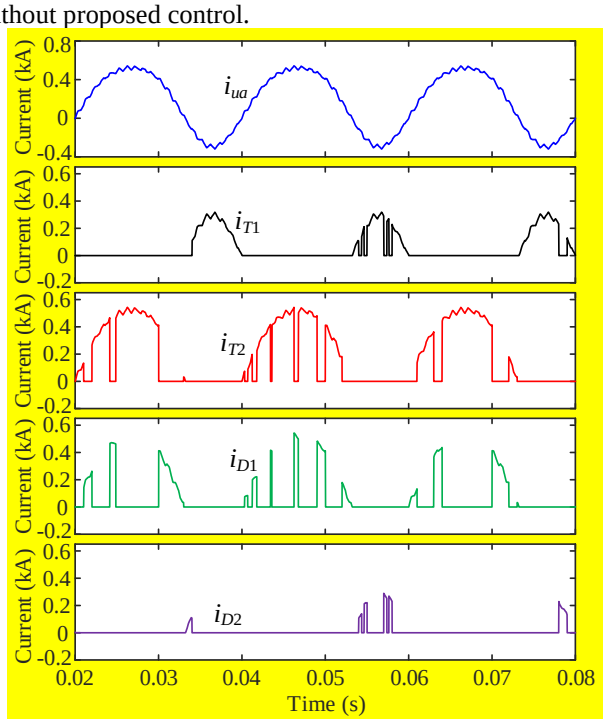


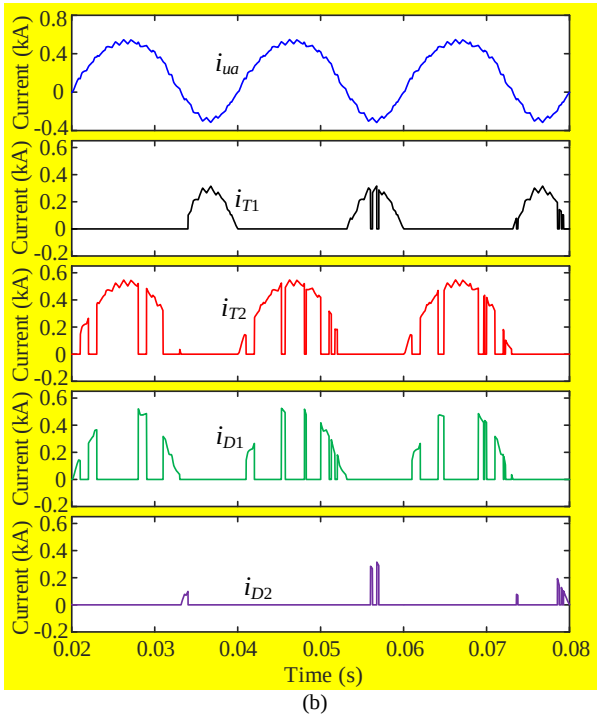
Fig. 13. Simulated dc-link current ripple under various carrier frequencies.

Fig. 14 shows the current waveforms of the semiconductor devices in the SM and the power losses, where the power factor angle is φ=0. The i_{T1}, i_{T2}, i_{D1} and i_{D2} respectively represent current flowing through T_1, T_2, D_1 and D_2 in the SM. Fig. 14(a) shows i_{ua}, i_{T1}, i_{T2}, i_{D1} and i_{D2} without proposed

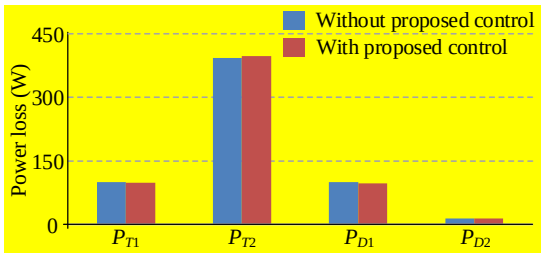
control. Fig. 14(b) shows i_{ua}, i_{T1}, i_{T2}, i_{D1} and i_{D2} with proposed control. Considering that Infineon IGBT FZ600R17KE4 is employed in the MMC, based on Figs. 14(a), (b) and the semiconductor datasheet from manufacturer, the power losses of T_1, T_2, D_1 and D_2 are calculated [33]. The junction temperature is considered as 125 ℃. Fig. 14(c) shows the power losses of T_1, T_2, D_1 and D_2 without proposed control and with proposed control, which are denoted as P_{T1}, P_{T2}, P_{D1} and P_{D2}, respectively. It can be observed that the P_{T1}, P_{T2}, P_{D1} and P_{D2} with proposed control are almost the same to those without proposed control.



(a)



(b)



(c)

Fig. 14. The waveforms of current flowing through SM semiconductor devices and the power losses. (φ=0). (a) current waveforms without proposed control, (b) current waveforms with proposed control, (c) power losses.

Fig. 15 shows the total power loss of one SM (the sum of P_{T1}, P_{T2}, P_{D1} and P_{D2}) with proposed control and without proposed control, where various power factor angles are considered including φ=0, φ=π/2, φ=π and φ=3π/2. It shows that the power losses with proposed control and without proposed control have very small difference.

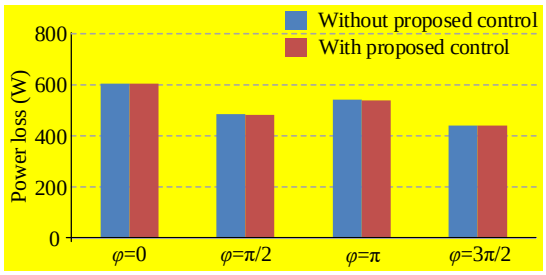


Fig. 15. Power loss of SM.

VI. Experimental Studies

In order to validate the proposed control, a downscaled three-phase MMC prototype is built in the laboratory, as shown in Fig. 16. A dc power supply paralleled with the resistor is used to support the dc-link voltage of the MMC. The MMC's ac side is connected to the grid via an autotransformer and an isolation transformer. The control algorithm is implemented by digital signal processor (DSP) and the driving signals are transferred to the driving panel of each SM by optical fibers. The parameters of the experimental setup are listed in Table III.

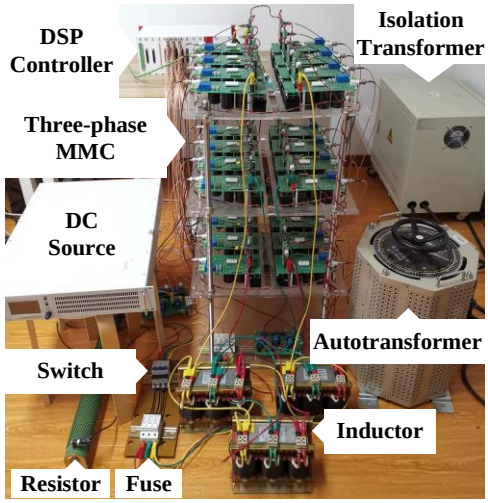


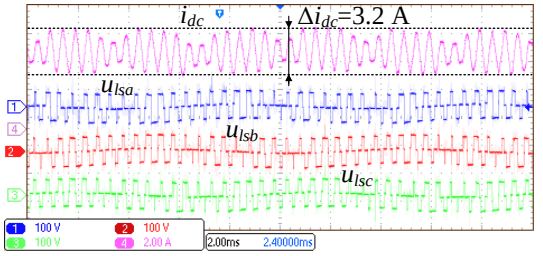
Fig. 16. Photo of the experimental setup.

TABLE III
EXPERIMENTAL SYSTEM PARAMETERS

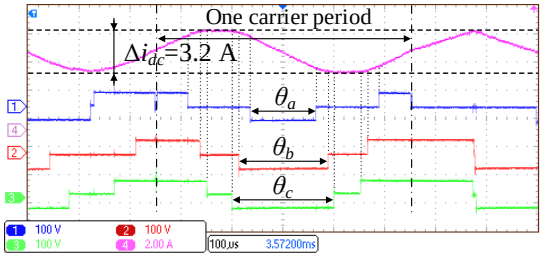
Parameter	Value
Active power P (kW)	1
DC-link voltage U_{dc} (V)	200
Grid line-to-line voltage (V)	100
Grid frequency (Hz)	50
Number of SMs per arm N	4
SM capacitance C_{sm} (mF)	2.35
Arm inductance L_s (mH)	5
Inductance L_f (mH)	1.8

A. Without Proposed Control

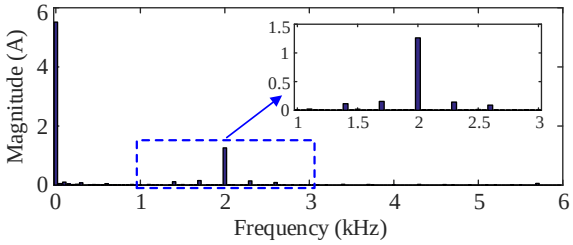
Figs. 17 and 18 show the performance of the MMC without the proposed control. The carrier frequency in Fig. 17 is 2 kHz. Fig. 17(a) shows the arm total inductor voltages u_{lsa}, u_{lsb}, u_{lsc} and the MMC's dc-link current i_{dc}. The u_{lsa}, u_{lsb}, u_{lsc} always have positive and negative pulses appearing alternately with varying widths. The maximum dc-link current ripple Δi_{dc} is 3.2 A. Fig. 17(b) shows the u_{lsa}, u_{lsb}, u_{lsc} and i_{dc} in one carrier period. Fig. 17(c) shows the FFT results of i_{dc}. The high frequency component mainly appears at the carrier frequency of 2 kHz, which is consistent with the theoretical analysis. Fig. 17(d) shows the upper arm current i_{ua} and lower arm current i_{la} in phase A. Fig. 17(e) shows the waveform of the u_{ua}, u_{la} and $2u_{ea}$. With $2N$+1 SUPWM, though the upper arm and lower arm output five voltage levels, the $2u_{ea}$ has 9 voltage levels. The THD of $2u_{ea}$ is 18.8%. Fig. 17(f) shows the waveforms of the grid currents i_a, i_b, i_c in phase A, B and C.



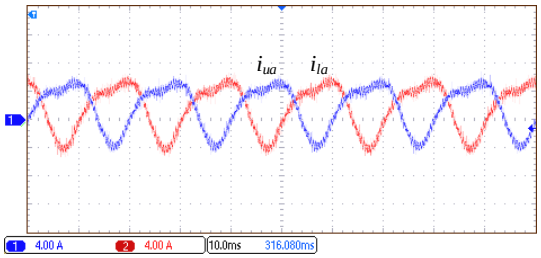
(a)



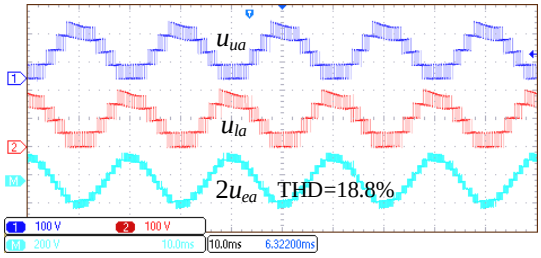
(b)



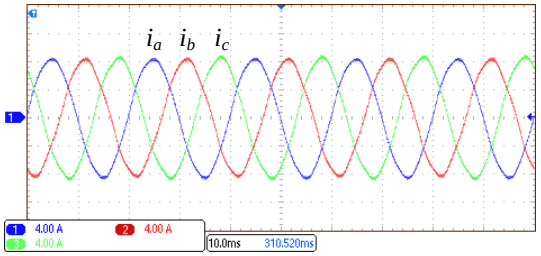
(c)



(d)



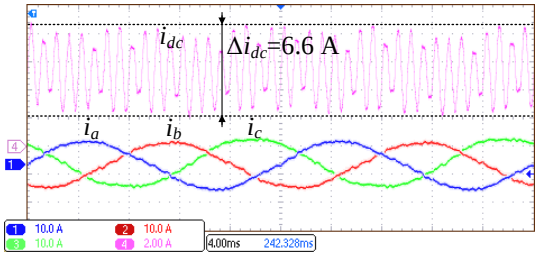
(e)



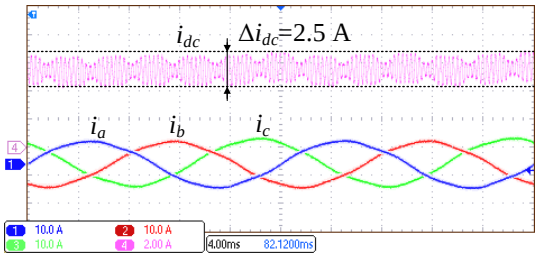
(f)

Fig. 17. Experimental waveforms without proposed control. The carrier frequency is 2 kHz. (a) u_{lsa}, u_{lsb}, u_{lsc} (100 V/div) and i_{dc} (2 A/div). Time base is 2 ms. (b) u_{lsa}, u_{lsb}, u_{lsc} (100 V/div) and i_{dc} (2 A/div). Time base is 100 μs. (c) FFT analysis of i_{dc}. (d) i_{ua} and i_{la} (4 A/div). Time base is 10 ms. (e) u_{ua}, u_{la}, (100 V/div) and $2u_{ea}$ (200 V/div). Time base is 10 ms. (f) i_a, i_b, and i_c (4 A/div). Time base is 10 ms.

Figs. 18(a) and (b) shows i_{dc} and grid current i_a, i_b, i_c of the MMC under different carrier frequencies including 1 kHz and 3 kHz. It can be observed that the dc-link current ripples are 6.6 A and 2.5 A under the carrier frequency of 1 kHz and 3 kHz, respectively.



(a)



(b)

Fig. 18. Experimental waveforms without proposed control including i_a, i_b, i_c (10 A/div) and i_{dc} (2 A/div). Time base is 4 ms. (a) carrier frequency is 1 kHz. (b) carrier frequency is 3 kHz.

Fig. 19 shows i_{ua}, i_{la} and i_{dc} when the circulating current suppression control [34] and the arm energy control [35] are enabled. The second-order circulating current is well suppressed. The peak-to-peak value of i_{dc} is 4 A.

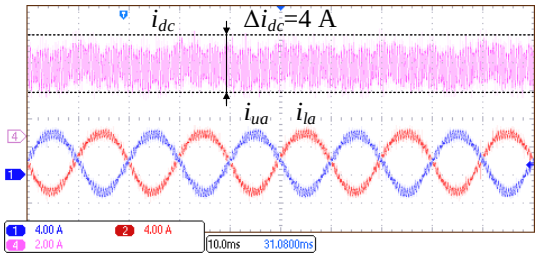
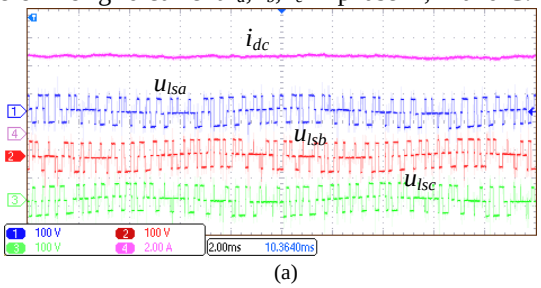


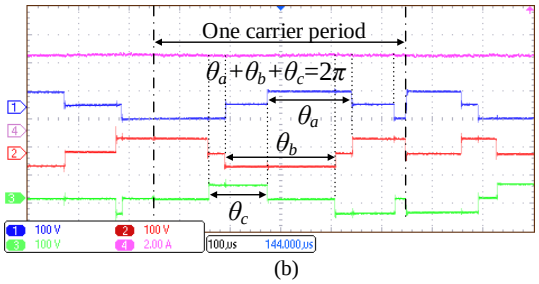
Fig. 19. Experimental waveforms without proposed control including i_{ua}, i_{la} (4 A/div) and i_{dc} (2 A/div). Time base is 10 ms. The circulating current suppression is enabled. Carrier frequency is 2 kHz.

B. With Proposed Control

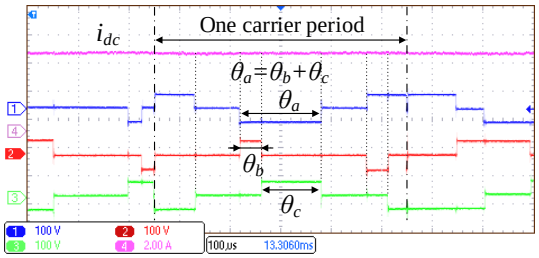
Figs. 20 and 21 show MMC performance with proposed control. The carrier frequency in Fig. 20 is 2 kHz. Fig. 20(a) shows the total inductor voltages u_{lsa}, u_{lsb}, u_{lsc} in phase A, B, C and dc-link current i_{dc}. It can be observed that the high-frequency ripple in dc-link current i_{dc} is effectively eliminated with proposed control in comparison with Fig. 17(a). Fig. 20(b) shows the u_{lsa}, u_{lsb}, u_{lsc} and i_{dc} in one carrier period, where $\theta_a+\theta_b+\theta_c=2\pi$ (Type I). Fig. 20(c) shows u_{lsa}, u_{lsb}, u_{lsc} and i_{dc} in one carrier period, where $-\theta_a+\theta_b+\theta_c=0$ (Type II). It can be observed that the pulses of u_{lsa}, u_{lsb} and u_{lsc} in Figs. 20(b) and (c) are both counteracted in the whole carrier period by phase shifting. Consequently, i_{dc} remains nearly constant. Fig. 20(d) shows FFT results of i_{dc}. Compared with Fig. 17(c), the high frequency component at 2 kHz is eliminated, which verifies the effectiveness of proposed control. Fig. 20(e) shows the upper arm current i_{ua} and lower arm current i_{la} in phase A. Fig. 20(f) shows the waveform of u_{ua}, u_{la} and $2u_{ea}$, where the $2u_{ea}$ has 9 voltage levels. The THD of $2u_{ea}$ is 18.9%, which is very close to that without proposed control. Fig. 20(g) shows the waveform of grid current i_a, i_b, i_c in phase A, B and C.



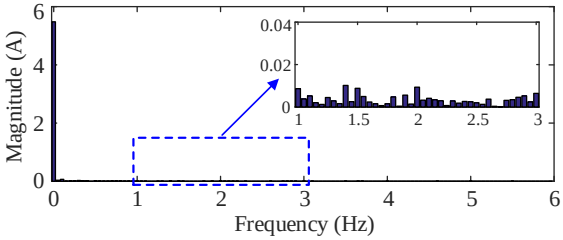
(a)



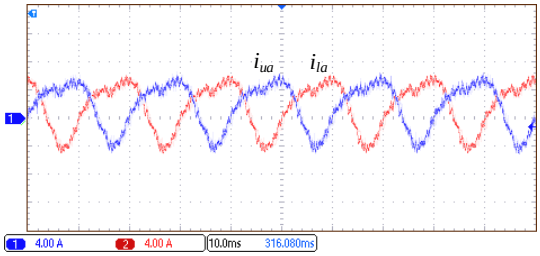
(b)



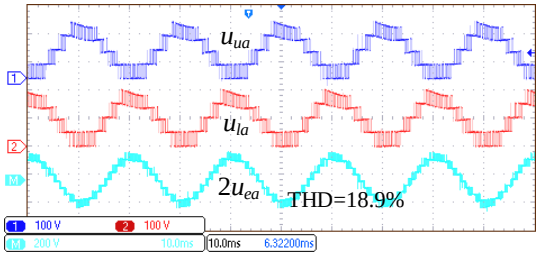
(c)



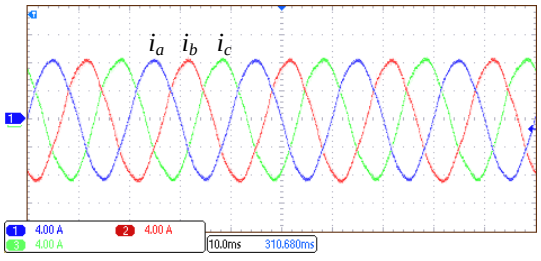
(d)



(e)



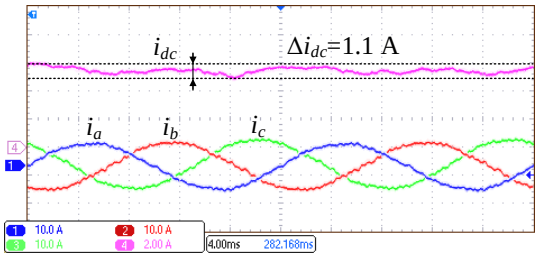
(f)



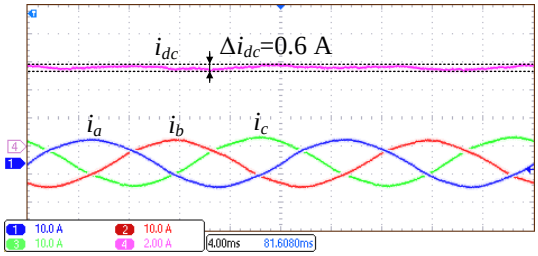
(g)

Fig. 20. Experimental waveforms of dc-link current with proposed control (the carrier frequency is 2 kHz). (a) u_{lsa}, u_{lsb}, u_{lsc} (100 V/div) and i_{dc} (2 A/div). Time base is 2 ms. (b) u_{lsa}, u_{lsb}, u_{lsc} (100 V/div) and i_{dc} (2 A/div) (Type I). Time base is 100 μs. (c) u_{lsa}, u_{lsb}, u_{lsc} (100 V/div) and i_{dc} (2 A/div) (Type II). Time base is 100 μs. (d) FFT analysis of i_{dc}. (e) i_{ua} and i_{la} (4 A/div). Time base is 10 ms. (f) u_{ua}, u_{la}, (100 V/div) and $2u_{ea}$ (200 V/div). Time base is 10 ms. (g) i_a, i_b, and i_c (4 A/div). Time base is 10 ms.

Figs. 21(a) and (b) show that the dc-link current ripples are 1.1 A and 0.6 A under the carrier frequency of 1 kHz and 3 kHz, respectively. Compared with Fig. 18, the grid currents i_a, i_b, i_c remain nearly unchanged, while the dc-link current ripple with the proposed control is much lower.



(a)



(b)

Fig. 21. Experimental waveforms with proposed control including i_a, i_b, i_c (10 A/div) and i_{dc} (2 A/div). Time base is 4 ms. (a) carrier frequency is 1 kHz. (b) carrier frequency is 3 kHz.

Fig. 22 shows i_{ua}, i_{la} and i_{dc} of the MMC when the circulating current suppression control and the energy control are enabled. It can be seen that the second-order circulating current is well suppressed. The peak-to-peak value of i_{dc} is 1.2 A. Compared with Fig. 19, the dc-link current ripple with the proposed control is reduced to 30% of that without the proposed control.

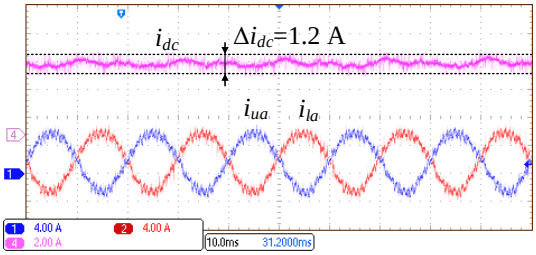


Fig. 22. Experimental waveforms with the proposed control including i_{ua}, i_{la} (4 A/div) and i_{dc} (2 A/div). Time base is 10 ms. The circulating current suppression control and the arm energy control are enabled. The carrier frequency is 2 kHz.

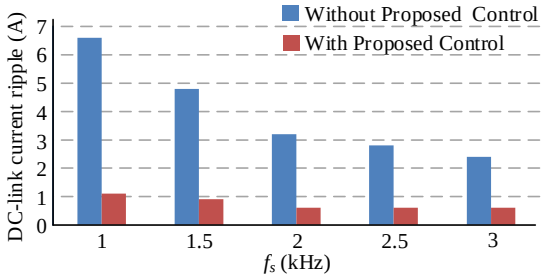
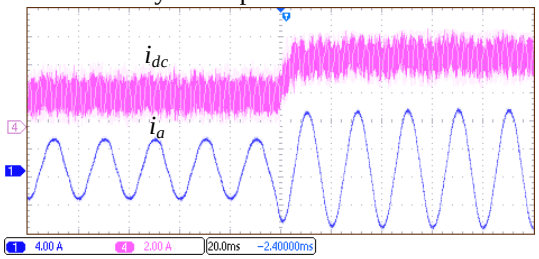


Fig. 23. Experimental dc-link current ripple under various carrier frequencies.

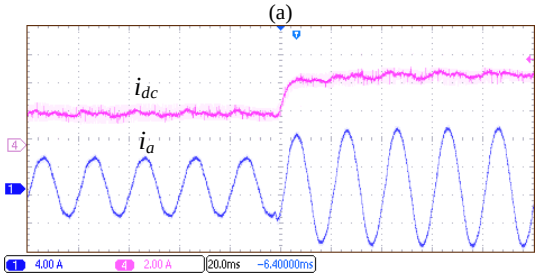
Fig. 23 shows the experimental results of the dc-link current ripple without proposed control and with proposed control, where the different carrier frequencies including 1 kHz, 1.5 kHz, 2 kHz, 2.5 kHz and 3 kHz are considered. It can be observed that the dc-link current ripple of the MMC with the proposed control is much lower than that without proposed control, which verifies the effectiveness of proposed control.

C. Dynamic Performance of MMCs

Figs. 24 and 25 show the dynamic performance of MMC. Figs. 24(a) and (b) show experimental waveforms of i_{dc} and i_a without the proposed control and with the proposed control respectively, where the active power is stepped from 500 W to 1000 W. Figs. 25(a) and (b) show i_{dc} and i_a without the proposed control and with the proposed control respectively, where the reactive power is stepped from 0 to 500 var. The dc-link current ripple of MMCs is greatly reduced with the proposed control. From Figs. 24 and 25, the proposed control does not affect the dynamic performance of the MMC.

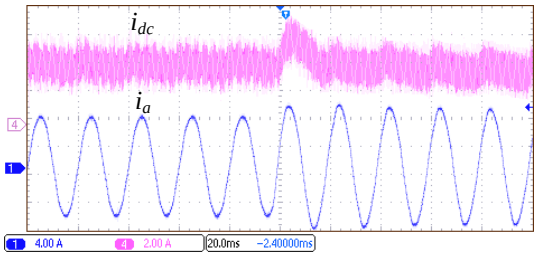


(a)

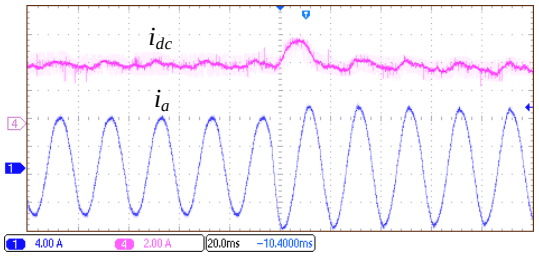


(b)

Fig. 24. Experimental waveforms when the active power is stepped from 500 W to 1000 W, including i_a (4 A/div) and i_{dc} (2 A/div). Time base is 20 ms. (a) without proposed control. (b) with proposed control. Carrier frequency is 2 kHz.



(a)



(b)

Fig. 25. Experimental waveforms when the reactive power is stepped from 0 to 500 VAR, including i_a (4 A/div) and i_{dc} (2 A/div). Time base is 20 ms. (a) without proposed control. (b) with proposed control. The carrier frequency is 2 kHz.

VII. Conclusions

This paper reveals that the conventional 2*N*+1 SUPWM will produce a high-frequency current ripple in the dc link of the MMC, which deteriorates the dc-link current performance. In order to solve the problem, this paper analyzes this issue in detail and proposes a reduced dc-link current ripple control method. Through regulating the phase angles of the carriers in three phases, the total voltages on the arm inductors of three phases can be counteracted in whole carrier period, so that the dc-link high-frequency current ripple is suppressed. The proposed control method improves the dc-link current performance of the MMC. The effectiveness of the proposed method has been verified by simulations and experimental results.

References

[1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Bologna Power Tech Conf.*, Jun, 2003, vol. 3, pp. 272-277.

[2] Y. Luo, Z. Li, L. Xu, X. Xiong, Y. Li and Cong Zhao, "An adaptive voltage-balancing method for high-power modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 2901-2912, Apr. 2018.

[3] D. Wu, and L. Peng, "Analysis and suppressing method for the output voltage harmonics of modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4755-4765, Jul. 2016.

[4] J. Wang, Y. Tang, P. Lin, X. Liu and J. Pou, "Deadbeat predictive current control for modular multilevel converters with enhanced steady-state performance and stability," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 6878-6894, Jul. 2020.

[5] A. Pérez-Basante, S. Ceballos, G. Konstantinou, J. Pou, J. Andrue, and I. M. de Alegria, "(2N+1) selective harmonic elimination-PWM for modular multilevel converters: a generalized formulation and a circulating current control method," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 802-818, Jan. 2018.

[6] C. Liu, F. Deng, Q. Heng, X. Cai, R. Zhu, and M. Liserre, "Crossing thyristor branches based hybrid modular multilevel converters for dc line faults," *IEEE Trans. Ind. Electron.*, early access. DOI: 10.1109/TIE.2020.3026277.

[7] B. Li, L. Han, S. Mao, S. Zhou, Z. Qu, and D. Xu, "Decoupled modulation scheme for modular multilevel converters in medium-voltage applications," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11430-11441, Nov. 2020.

[8] F. Deng, Y. Lv, C. Liu, Q. Heng, Q. Yu and J. Zhao, "Overview on Submodule Topologies, Modeling, Modulation, Control Schemes, Fault Diagnosis and Tolerant Control Strategies of Modular Multilevel Converters," *Chinese Journal of Electrical Engineering*, vol. 6, no. 1, pp. 1-21, March 2020.

[9] A. Dekka, B. Wu, and N. R. Zargari, "Minimization of dc-bus current ripple in modular multilevel converter under unbalanced conditions," *IEEE Trans. Power Electron. Lett.*, vol. 32, no. 6, pp. 4125-4131, Jun. 2017.

[10] J. Wang, J. Liang, C. Wang and X. Dong, "Circulating current suppression for MMC-HVDC under unbalanced grid conditions," *IEEE Trans. Ind. Appl.*, vol. 53, no. 4, pp. 3250–3259, Jul./Aug. 2017.

[11] J. Wang, and Y. Tang, "A fault tolerant operation method for medium voltage modular multilevel converters with phase-shifted carrier modulation," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9459–9470, Oct. 2019.

[12] F. Deng, Y. Tian, R. Zhu, and Z. Chen, "Fault-tolerant approach for modular multilevel converters under submodule faults," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7253-7263, Nov. 2016.

[13] Y. Li, E. A. Jones, and F. Wang, "Switching-frequency ripple on dc link voltage in a modular multilevel converter with circulating current suppressing control," *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, Fort Worth, TX, USA, 2014, pp. 191-195.

[14] K. Li, Y. Liao, H. Lin, R. Lin and J. Zhang, "Circulating current suppression with improved dc-link power quality for modular multilevel converter," *IET Gener. Transm. & Distrib.*, vol. 12, no. 10, pp. 2220–2230, Apr. 2018.

[15] Y. Li, E. A. Jones and F. Wang, "Circulating current suppressing control's impact on arm inductance selection for modular multilevel converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 182–188, Mar. 2017

[16] B. He, K. Ma, X. Xin, and W. Wang, "Hybrid modulation method for nearest-level-control-based MMC to suppress dc power fluctuation when enabling circulating current suppression," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 6232-6237.

[17] F. Deng, Q. Yu, Q. Wang, R. Zhu, X. Cai and Z. Chen, "Suppression of dc-link current ripple for modular multilevel converters under phase-disposition PWM," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 3310–3324, Mar. 2020.

[18] Q. Yu, F. Deng, C. Liu, J. Zhao, F. Blaabjerg and S. Abulanwar, "DC-link high-frequency current ripple elimination strategy for MMCs using phase-shifted double-group multicarrier based phase-disposition PWM," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 8872-8886, Aug. 2021.

[19] X. Gao, W. Tian, Y. Pang, and R. Kennel, "Model predictive control for modular multilevel converters operating at wide frequency range with a novel cost function," *IEEE Trans. Ind. Electron.*, early access. DOI: 10.1109/TIE.2021.3090705.

[20] F. Deng and Z. Chen, "A control method for voltage balancing in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 66–76, Jan. 2014.

[21] F. Deng and Z. Chen, "Elimination of dc-link current ripple for modular multilevel converters with capacitor voltage balancing pulse-shifted carrier PWM," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 284–296, Jan. 2015.

[22] B. Li, R. Yang, D. Xu, G. Wang, W. Wang, and D. Xu, "Analysis of the phase-shifted carrier modulation for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 297-310, Jan. 2015.

[23] B. P. McGrath, C. A. Teixeira, and D. G. Holmes, "Optimized phase disposition (PD) modulation of a modular multilevel converter," *IEEE Trans. Ind. Appl.*, vol. 53, no. 5, pp. 4624-4633, Sept.-Oct. 2017.

[24] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses, and semiconductor requirements of modular multilevel converters, " *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2633-2642, Aug. 2010.

[25] J. Liu, P. Wang, Z. Li, and Y. Li, "A comparative research of two modulation strategies widely applied in modular multilevel converter, " in *Proc. International Conference on Electrical Machines and Systems (ICEMS)*, 2013, pp. 1683-1687.

[26] J. Wang, X. Han, H. Ma, and Z. Bai, "Analysis and injection control of circulating current for modular multilevel converters, " *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2280-2290, Mar. 2019.

[27] Z. Li, P. Wang, H. Zhu, Z. Chu, and Y. Li, "An improved pulse width modulation method for chopper-cell-based modular multilevel converters, " *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3472-3481, Aug. 2012.

[28] S. Lu, K. Li, X. Deng, S. Li, and Z. Zhao, "An improved submodule unified pulse modulation scheme for a hybrid modular multilevel converter, " *CES Trans. Electr. Mach. Syst.*, vol. 1, no. 3, pp. 322-333, Sep. 2017.

[29] L. Lin, Y. Lin, Z. He, Y. Chen, J. Hu, and W. Li, "Improved nearest-level modulation for a modular multilevel converter with a lower submodule number," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5369-5377, Aug. 2016.

[30] X. Chen, J. Liu, S. Song and S. Ouyang, "Circulating harmonic currents suppression of level-increased NLM based modular multilevel converter with deadbeat control," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11418–11429, Nov. 2020.

[31] X. Shi, Z. Wang, B. Liu, et al., "Characteristic investigation and control of modular multilevel converter-based HVDC system under single-line-to-ground fault conditions," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 18-36, Jan. 2015.

[32] Y. Okazaki, W. Kawamura, M. Hagiwara, H. Akagi, et al., "Experimental comparisons between modular multilevel DSCC inverters and TSBC converters for medium-voltage motor drives," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1805-1817, Mar. 2017.

[33] Y. Zhang, H. Wang, Z. Wang, F. Blaabjerg, and M. Saeedifard, "Mission profile-based system-level reliability prediction method for modular multilevel converters," *IEEE Trans. Power Electron*., vol. 35, no. 7, pp. 6916-6930, Jul. 2020.

[34] Z. Li, P. Wang, Z. Chu, H. Zhu, Y. Luo, and Y. Li, "An inner current suppressing method for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4873-4879, Nov. 2013.

[35] S. Wang, G. P. Adam, A. M. Massoud, D. Holliday, and B. W. Williams, "Analysis and assessment of modular multilevel converter internal control schemes," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 697–719, Mar. 2020.