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Hardware Design of High Current Prismatic Smart Battery Packs

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Abstract

Smart battery (SB) architecture is defined as the inclusion of a half bridge converter at cell level in a Li-ion battery pack along with a wireless battery management system (BMS). This architecture provides additional degrees of freedom at cell level where a cell can be either inserted or bypassed in a pack. This leads to the pulsed operation that can improve the cycle life and advantages in pack monitoring and diagnostics. In this paper, the hardware design for a 50Ah prismatic SB cell and a pack design with 8 cells in series is detailed. Considering 2C as the highest current, the hardware design takes into account the power losses, PCB design aspects and an optimum configuration for the pack design. A detailed description of the design along with 3D models is provided. The proposed SB cell design can be extended to any other cell of different capacity, which is expected to be highly effective and efficient for a wide range of applications.

1 Introduction

Electrification of the transportation is enabled by the rapid growth in the energy density of the Li-ion cells. This has led to an increasing number of electric cars available to consumers. It is not just passenger cars that are benefitting from this trend, but high duty vehicles such as buses and trucks are also being developed with all-electric energy systems [1]. It is important that the Li-ion cells used for the electric mobility have higher lifetime, safety, improved fault-tolerance and condition monitoring.

Smart battery (SB) architecture has been proposed [2] for improving the lifetime of the Li-ion cells along with a wireless battery management system (BMS) for reducing the wiring complexity and easier maintenance. In addition, artificial intelligence has been integrated into the SB structure to monitor and control the state of cells, provide predictive maintenance, and further improve the battery's reliability [3]. The SB architecture involves adding a half bridge (HB) topology across each cell in a Li-ion battery pack. The system architecture is shown in Fig. 1 [4].

Figure 1: Smart battery architecture showing the half bridge across a cell and the wireless BMS.

As it can be seen from Fig. 1, by turning on either the top or the bottom switch, the cell can be either inserted or bypassed in the pack. Each cell has a controller that sends the gate drive signals and sensors (voltage, current and temperature) that are used for monitoring the cell status and send the data to the BMS master using wireless communication.

In this paper, the SB cell for a 50Ah prismatic cell with NMC chemistry is designed. Considering 2C rate for the continuous operation, the MOSFETs and the current path for the SB cell is designed for 100A current. This leads to a careful selection of the MOSFETs for the HB circuit along with a detailed PCB design. The power loss in the SB for the highest current is determined. Alternate solutions for reducing the power loss are also discussed.

The proposed design aims at adding the SB PCB with the similar geometric profile as the prismatic cell in order to facilitate the pack design. This paper also presents the pack design considering 8 cells in series, that can be extended for any higher number of series cells. By considering a higher number of cells in series, the pack design can be further optimized for better performance.
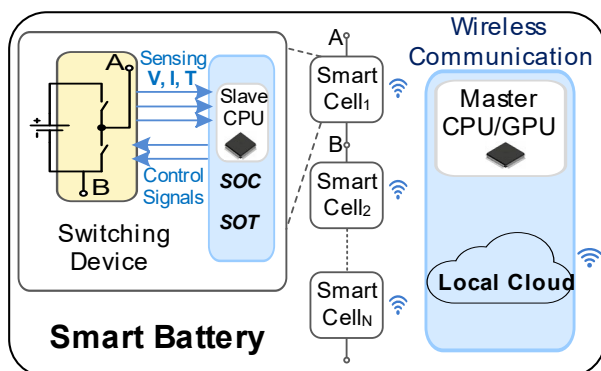
2. Device Selection and High Current PCB Design

The MOSFETs used for the HB will have conduction losses in both insert or bypass mode of the SB. Thus, for the high current design, it becomes necessary to parallel the MOSFETs to reduce the conduction losses and to reduce the temperature rise. The SB does not require fast switching. As indicated in [2], pulsed charging at very low frequency is sufficient to improve the battery state-of-health (SoH). Thus, the HB MOSFETs will be switching at most at a few hundred hertz for diagnostic cases to estimate the cell impedance [5] and at these frequencies the switching losses are negligibly small.

The design philosophy for selecting the MOSFETs is summarized below:

- Sub-milli-ohm on resistance.
- Low thermal resistance to the ambient.
- Paralleling of the MOSFETs to ensure a temperature rise of $< 20^oC$ during the maximum rated current of the smart cell.

Considering the above points, the MOSFET IAUA250N04S6N005 from Infineon [6] is selected with three of them in parallel for the top and bottom switches of the HB.

2.1 Power loss and temperature rise calculation

For a junction temperature of 100°C, the typical on-resistance for the chosen MOSFET is 0.56mohms. With three in parallel, we have,

$$r_{dson} = \frac{0.56}{3} = 0.187 m\Omega \qquad (1)$$

Thus, at 100A continuous current, we will have a conduction loss of,

$$P_{cond,tot} = 100^2 \times r_{dson} = 1.87W \qquad (2)$$

As the switching is typically in tens of hertz or less, the switching losses can be ignored. This is because the rise time and fall time of the device are 13ns and 26ns, their ratio with switching frequency (say max. 100Hz) is negligibly small. Note that with lower temperature, the conduction loss will be lower.

The conduction loss in (2) is for the three MOSFETs in total. Thus, the loss per MOSFET is given by,

$$P_{cond} = 0.623W \qquad (3)$$

As per the datasheet [1], without any heatsink, the junction to ambient thermal resistance is,

$$R_{thja} = 22.7K/W \qquad (4)$$

Temperature-rise from ambient for this case (for each MOSFET) is given by,

$$\Delta T = P_{cond}R_{thja} = 14.1^oC \qquad (5)$$

Thus, the selection meets the design criterion of maintaining the temperature rise under 20°C.

2.2. Current sense resistor

The SB has current sense capability at the cell level, unlike the conventional battery packs. For the design discussed in this paper, current sense resistors are used to measure the cell current. It must be noted that the resistors will also introduce additional power losses, hence, their selection is similar to the selection of the MOSFETs with the aim of lowering the losses and the temperature rise.

To achieve the above design considerations, two current sense resistors with $0.2m\Omega$ resistance are used in parallel. With this, they will have a power loss of 0.5W each and a total loss of 1W.

The sense resistors are rated for a power of 5W each. However, the temperature rise of these resistors reaches significantly higher levels at the rated power and they will need forced cooling for reducing the temperature. Fig. 2 shows the temperature rise versus fraction of the rated power $P_{r120} = 5W$. As the power dissipation is only 0.5W, the temperature rise is about 10°C, hence meeting the design criteria similar to the MOSFETs.
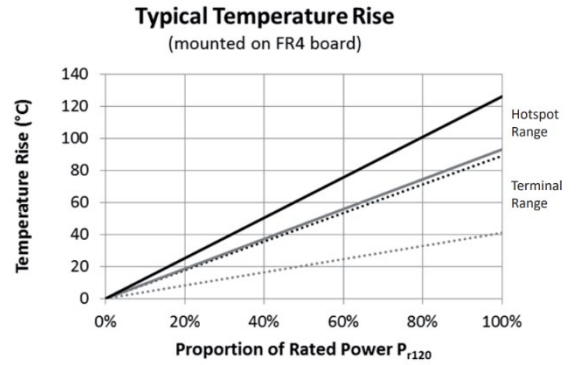

Figure 2: Temperature rise versus power [7].

2.3. PCB track design

The PCBs will carry the maximum 100A current through the top or bottom MOSFETs corresponding to the insert or bypass mode.

Based on the available maximum copper thickness (10 oz), the minimum trace width is computed using the following set of equations.

The copper area A_{cu} for a maximum rms current of I along with a temperature rise of ΔT is given by,

$$A_{cu} = \left(\frac{I}{k\Delta T^b}\right)^{\frac{1}{c}} \qquad (7)$$

Here k, b and c are constants given by 0.048, 0.44 and 0.725 respectively. Note that the temperature rise is in degrees Celsius, and the current is in amperes. The copper area computed by (7) is in square mils.

Using (7), the required copper width is determined using,

$$cu_{width} = \frac{A_{cu}}{t_{oz} \times 1.378} \qquad (8)$$

The copper thickness is specified by $\boldsymbol{t_{oz}}$=10 oz. Using this, the equation (8) provides the required copper width in mils. The

equations (7) and (8) are obtained from the IPC-2221A generic standard on printed board design [8].

Fig. 3 shows the variation of the PCB track current capability with the copper cross sectional area. This is plotted using (7) considering a maximum temperature rise $\Delta T = 20^oC$. As it can be seen, for 100A current, the cross-sectional area necessary is about $A_{cu} = 3.87 mm^2$. Now using (8) after converting the cross-sectional area into square mils, the necessary copper width can be computed for the available copper thickness of 10 oz.

So, considering 100A current along with a maximum temperature rise of 20^oC, equations (7) and (8) result in a minimum copper width of 11.1mm or 0.44 inches. This copper width can be distributed as 5.55mm copper width in 2 layers. The PCB design needs to strictly meet this copper width and thickness in order to conduct the desired maximum current of 100A.
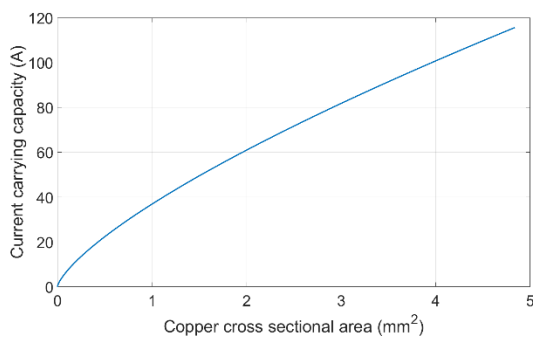

Figure 3: PCB track current carrying capacity versus copper cross-sectional area.

Note that the parameter k in (7) has a lower value for the internal PCB layers. Thus, it is preferred to have the high current copper tracks on the top and bottom layers, where cooling is better that provides the higher current carrying capacity.

3 Smart Cell and Smart Battery Pack Design

In this work, a 50Ah prismatic cell from CALB is used for designing the smart cell. Fig. 4 shows the view of the cell. The electronics will be mounted on the top side with the same rectangular profile as the top view of the prismatic cell.
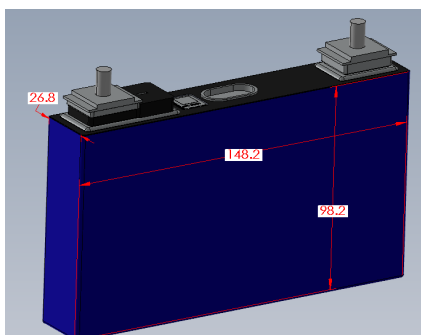

Figure 4: Prismatic cell (50Ah) used for the smart cell with the dimensions marked in mm.

As it can be observed from Fig. 4, the width of the PCB will be at most 26.8mm. The copper width from (8) is determined to be 0.445 in or 11.3mm, which is close to half of the cell width. Thus, the copper traces carrying the high current will occupy either half of the width on one layer or a quarter of the width on both top and bottom sides of the PCB. Since the available width is very small, the smart cell is designed with 2 PCBs that connect to each other using a board-to-board connector. The high current PCB will have only the MOSFETs, current sense resistors and temperature sensors. This PCB is called as the bypass PCB.

The wireless BMS controller and sensors are designed in another PCB that is mounted on top of the bypass PCB.

3.1 Control and bypass PCB design
Fig. 5 shows the 3D image of the bypass PCB. It consists of the wireless controller, sensors (voltage and current), voltage regulators to produce the voltage to supply the electronics, and communication connectors such as JTAG and serial.
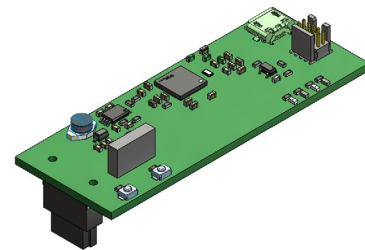

Figure 5: Control PCB for the wireless BMS.

The board-to-board connector can be observed at the bottom side of the PCB, which will be used to connect with the bypass PCB carrying 100A current. The wireless controller used, CC2652R, is from Texas Instruments from the Simple Link family of devices[9].

Fig. 6 (a) shows the bypass PCB with the key components placed in the bottom side. Fig. 6(b) shows the 3D view where the board-to-board connector can be observed to be on the top side of the PCB, which mates with the control PCB shown in Fig. 5.
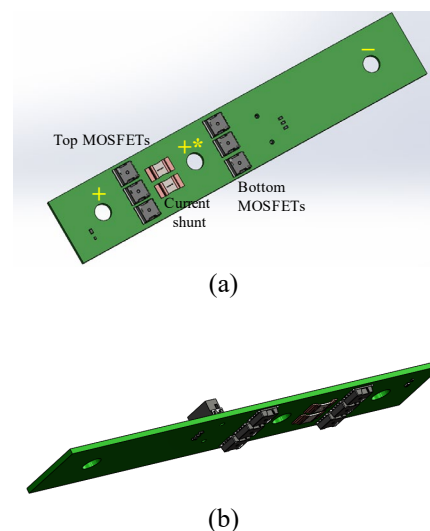

(a)

(b)

Figure 6: (a) Bottom view of the bypass PCB, (b) 3D view showing the components on both top and bottom side.

3.3 Smart Cell Assembly

With the PCBs designed as per requirement, the smart cell is assembled using the cell in Fig. 3 and the control and bypass PCBs in Figs. (5) and (6) respectively. The assembled smart cell is shown in Fig. 7. As it can be observed, the control PCB is mounted on top of the bypass PCB and the usable terminals are the negative (marked as $-$) and the HB midpoint terminal (marked as $+*$).
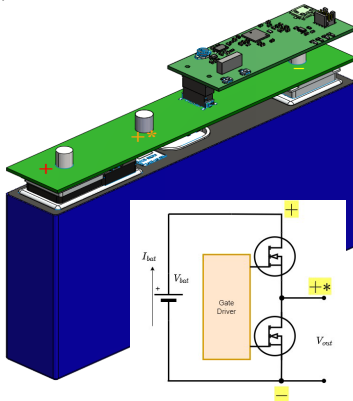

Figure 7: Smart Cell assembly along with the HB schematic shown.

4 Smart Battery Pack

The smart cell developed in Fig. 7 is used to make an illustrative battery pack with 8 cells in series. Typical arrangement of prismatic cells is to place them with alternate polarities adjacent to each other so that the series connections can be made with small copper bus bars. Similar philosophy is used in developing the smart battery pack.
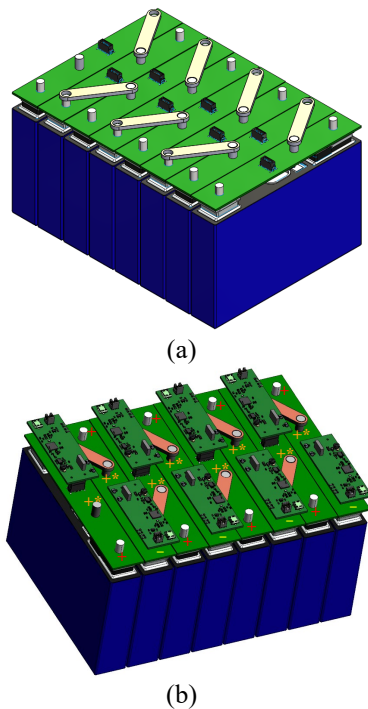

(a)

(b)

Figure 8: (a) Series connection of the 8 smart cells and (b) mounting of the control PCBs to complete the assembly of the smart battery pack.

The steps used for the assembly are as follows:

- Place the prismatic cells with alternating polarity in a tight package.
- Mount and secure the bypass PCB on each of the cells.
- Mount the copper bus bars to make the series connection.
- Mount the control PCBs on top of the bypass PCB.

Fig. 8(a) shows the series connection of the cells using copper bus bars and the complete mounting in Fig. 8(b).

5 Conclusion

In this paper, the design of a high-current smart battery pack for the prismatic geometry is described. The design considers the power loss and temperature rise as the main criteria to determine the type and paralleling of the power MOSFETs used in the half-bridge circuit across each cell. Additionally, the same philosophy is used to select the current sense resistors. A high current of 100A flows through the PCB tracks and IPC-2221A standard is used to select the copper width and thickness necessary to support this current flow.

The bypass and control PCBs are developed separately and connected via board-to-board connector and mounted on the cell to form a single smart cell. The resulting smart cell is made up 8 cells in series. However, it is worth noting that the proposed approach is generic and can be extended to any group of series/parallel connected cells, making it a valuable contribution to the field of battery management.

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