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Closed-loop Control of MOSFET Gate Voltage for Charge Balance in a Smart Li-ion Battery Cell

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***Abstract*-- A smart battery (SB) cell integrates a half-bridge topology with Li-ion cells using very low on-resistance MOSFETs. The half-bridge provides additional degrees of freedom such as bypassing or inserting the cell in a pack depending on the cell state-of-charge (SoC) and state-of-health (SoH). In this paper, a new operation mode is proposed where the gate voltage of the bottom MOSFET is controlled in closed-loop to provide additional current path, which can be made independent of the charge/discharge current magnitude. This controllable additional current through the bottom MOSFET provides a new approach to balance the SoCs of the batteries without the requirement of a full-scale dc-dc converter. The current magnitude can be controlled based on the amount of SoC unbalance and the time required to balance. The parameters of the analog controller to get the desired transient response are determined. Since this operation mode introduces additional power loss, a thermal analysis is performed to optimize the balancing current and the temperature rise. The results are verified using the real device models in a spice simulation environment.**

***Index Terms*—Charge balancing, Li-ion cells, passive and active balancing methods, smart cells, power loss analysis**

I. Introduction

Lithium-ion batteries are the key enablers for the actively growing electric vehicle industry. Considerable amount of research is channeled towards improving the lifetime and for the optimal operation of the Li-ion battery packs for EV applications. One such method is integrating a half-bridge to Li-ion cells, which provides a number of advantages and possibilities to optimize the performance of the cells in a pack [1].

Fig. 1 shows the integration of the half bridge to a cell, termed smart battery (SB) cell, using two complementarily switched MOSFETs with sub-milliohm on-resistance.

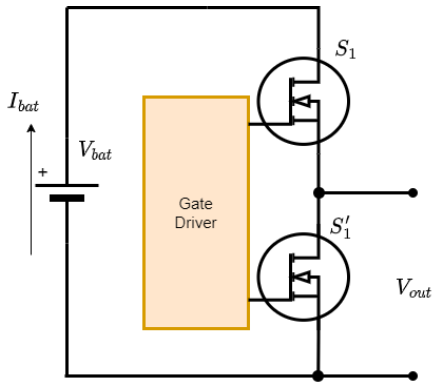


Figure 1: Integration of a half bridge circuit to a Li-ion cell.

In the SB cell, the top MOSFET (S_1) can be turned ON to insert the cell in a pack. Similarly, by turning the bottom MOSFET (S_1') ON, the output voltage of the SB will be zero and the cell is bypassed from the pack. This allows for seamless pulsed operation for the cell, which is shown to have a positive impact on the battery life and SoH [2]. The half bridge is integrated for every cell in a pack. Hence, by controlling the mode (insert or bypass), the cells can be individually inserted or bypassed in the pack.

Typically, the Li-ion cells will have a balancing circuit as part of the BMS to balance the SoC/voltages that may be unbalanced due to manufacturing tolerances, unequal aging, different thermal stresses etc. The balancing circuits are either passive or active [3,4]. The passive balancing methods use balancing resistors and active switches. Any higher charge is dumped into the resistors. This is a lossy approach and requires a large resistor active switch network. The advantage of this method is the lower cost and complexity.

On the other hand, for active balancing methods, power converters such as flyback, DAB, Ćuk [5] – [7] are used to actively transfer charge from one cell to the other in order to balance them. These methods are usually complex and increase the system cost just for the purpose of balancing. The system reliability may also be negatively impacted if the performance of the additional power converters and their control is not optimal.

In this paper, a novel control is proposed to a SB cell making use of the existing half bridge for cell balancing. The balancing of SB cell by using the bypass mode is reported in earlier literature [8]. Consider the scenario of charging. If a cell has higher SoC than a threshold, it can be bypassed till all the other cells in the pack reach the same SoC. After this point, the cell can be inserted again. With this approach, the balancing is practically lossless. However, this also has some disadvantages: it is not possible to finely control the balancing time since the cell under consideration is fully bypassed. Additionally, this approach will vary the dc bus voltage. For example, while discharging, if multiple cells have lower SoC, if they are bypassed, the net dc bus voltage reduces by the amount of cells bypassed.

In contrast, in the proposed approach, the top MOSFET of the SB is ON, thereby inserting the cell in the pack. The bottom MOSFET is not turned-off. Instead, it is controlled with a gate voltage higher than the threshold but lower than the typical ON voltage (15V). This gate voltage is controlled to circulate a known current within the cell and the half bridge. The additional current from the cell can be used for charge balancing, say, when the cell has higher

SoC during discharge. Similarly, when the cell has higher SoC during charging, the current into the cell can be finely controlled instead of completely bypassing it.

The drawback of this method is the power loss in the MOSFET that carries the controlled current. This paper presents a thermal analysis and a closed-loop adjustment of the current to limit the temperature rise. The proposed method can be used in conjunction with the method in [8] to achieve robust and fast balancing without losing the dc bus voltage during the process.

The proposed method is implemented in closed loop and a new modification is proposed to the gate drive circuit to ensure a simple low-cost implementation. The design of the controller is described. The overall control can be implemented using purely analog circuits.

The performance of the proposed method is verified using meticulous simulations performed using LTSpice. Actual device models are used and the performance of the analog controller has been validated.

II. Balancing of Cells in a Smart Battery Architecture

In this Section, the balancing method for SB cells is described as a combination of the gate voltage control and bypass.

Fig. 2 shows only two cells within a pack for illustration purpose. There can be three types of operation for the SB cell for balancing. The scenarios shown in Fig. 2 are for discharge. In Fig. 2(a), both the cells are within their nominal SoC and terminal voltage. Thus, Thus, the top devices S_1 and S_2 are ON to ensure the series connection of the cells The total dc bus voltage for this case is:

$$V_{dc,balanced} = V_{bat1} + V_{bat2} \quad (1)$$

The current path is marked in red.

Now consider the case when the first cell has higher SoC, more than a prescribed threshold value. In this case,

$$V_{bat1} > V_{bat2}$$

For the second cell, the operation is still with the top switch S_2 ON and S_2' OFF. Thus, the current is flowing only through S_2. For the first cell, the proposed operation mode is introduced. The bottom MOSFET S_1' is controlled with a voltage V_{GS} to ensure that it carries a known amount of current ΔI. This is shown with the blue line in Fig. 2(center).

In this case, the net dc bus voltage is still given by,

$$V_{dc,proposed} = V_{bat1} + V_{bat2} \quad (2)$$

because the top devices of both the cells are conducting.

Now, consider the case when the SoC of the first cell is very low during the discharge operation. This is shown in Fig. 2(right). This situation can be addressed using two approaches. One is to bypass the low SoC cell, as shown in Fig. 2(right). This will reduce the net dc bus voltage at the output. In this case, the net dc bus voltage is given by,

$$V_{dc,bypassed} = V_{bat2} \quad (3)$$

Alternate approach in this case is to use the proposed gate voltage control for the bottom cell with higher SoC so that it discharges faster.

Now, considering a generic case of N series cells in a pack, the following are the two scenarios of balancing.

If u cells are unbalanced, for the full bypass approach as in [8], the net dc bus voltage is $(N-u)V_{cell}$ assuming the balanced cells have equal voltages.

With the proposed approach, where we keep the u cells inserted but enable the bottom switch to control the cell current, the net dc bus voltage is $(N-u)V_{cell} + uV_{cell}^{'}$ considering the unbalanced cells have a voltage of $V_{cell}^{'}$.

A. Determination of the required gate voltage

The MOSFETs used for SB cells need to have a very low on-resistance $r_{ds,on}$ to reduce the conduction losses during the operation. Table I shows some commercially available MOSFETs [9]with sub-milliohm on resistance.

Table 1: Commercial low $r_{ds,on}$ MOSFETs for SB architecture.

MOSFET Part number	$R_{ds,on}$(mΩ)	Rated current (A)	Power loss at 50A (W)
IPT004N03L	0.4	300	1
IST006N04NM6	0.6	475	1.5
IPLU300N04S4-R8	0.77	300	1.92
AUIRF8739L2TR	0.35	545	0.875

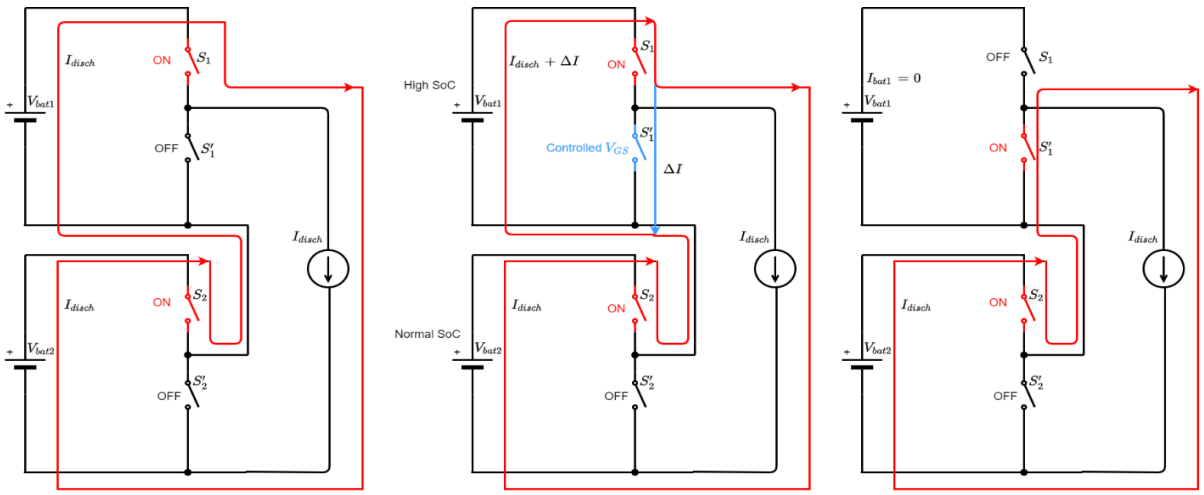


Figure 2: Discharge operation with two series connected SBs. (Left) Both cells are balanced, (center) top cell has higher SoC (right) top cell has very low SoC.

Depending on the battery capacity, more MOSFETs need to be connected in parallel to limit the power losses.
Typically, these MOSFETs need to be controlled with a gate voltage of at least 10V in order to ensure minimum on resistance and minimum power loss. Also, note that the two MOSFETs in a SB are typically switched complimentarily. So, one of the device is applied with a gate to source voltage (V_{GS}) of 15V (for fully on condition) and the other device is applied with a V_{GS} of 0V to ensure complete turn-off.
With the proposed approach, the top device is fully turned-on with a V_{GS} of 15V, while the bottom device V_{GS} is controlled between the threshold voltage and the maximum voltage to ensure a fine control of its current. The extreme case of the bottom device with the full gate voltage of V_{GS} will result in a complete short circuit of the cell, which is not an allowed operation mode.
In proposed operation mode of MOSFETs, the V_{DS} is at least 2.7V if we consider an NMC cell. Considering that the threshold voltage can be between 2-4V, the proposed operation keeps the MOSFET in saturation. During the saturation mode, the drain current is proportional to square of the V_{GS}. The drain current expression is given by,

$$I_{drain} = k((V_{GS} - V_T)^2) \quad (4)$$

In (4), the drain to source voltage is represented as V_{DS}. The parameter k is device dependent and is affected by channel length, width and gate capacitance.
Fig. 3 shows the variation of the drain current with V_{GS} for a V_{DS} that varies between 2.7V to 4.2V considering the terminal voltage of NMC cells.

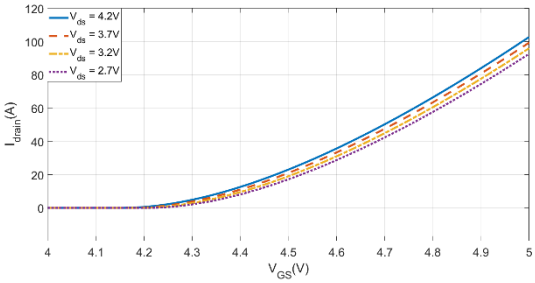


Figure 3: Variation of drain current with gate to source voltage for a low $r_{ds,on}$ MOSFET.

As it can be seen from Fig. 3, the variation is indeed quadratic as described by (4).
Above the threshold voltage, fine control over the gate voltage is necessary to ensure correct control of the current amplitude. Note that the above curve will change based on the operating temperature. Hence, it is important to have a closed-loop control method to ensure safe operation.

B. Impact of temperature on the MOSFET current during paralleled operation.

When the SB cell has multiple MOSFETs in parallel (for high-capacity cells), it is natural that the MOSFETs can have differences in their threshold voltages. This can create a problem in current sharing between them during balancing operations.

The Spice model for the device provided by Infineon provides an option to simulate the behavior of the MOSFETs for different threshold voltage conditions. This is utilized to study the behavior when same V_GS is applied to two MOSFETs in parallel where one has the typical threshold voltage while the other has the lowest possible threshold voltage.

The resultant currents are shown in Fig. 4.

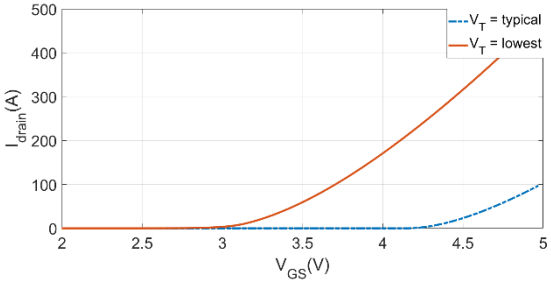


Figure 4: Drain current versus V_{GS} for mismatched parallel MOSFETs.

It is known that higher temperature reduces the threshold voltage. Thus, if common V_{GS} is used, the proposed approach may result in unbalance in the currents shared by the MOSFETs, which is undesirable. Hence, it is proposed to use individual correction voltages for each MOSFET to ensure equal current sharing. This is discussed in the Section III.

III. Implementation of the Proposed Balancing Method

A. Overview

The SB architecture utilizes a master controlling slaves, which are Li ion cells with the half bridge topology[11].

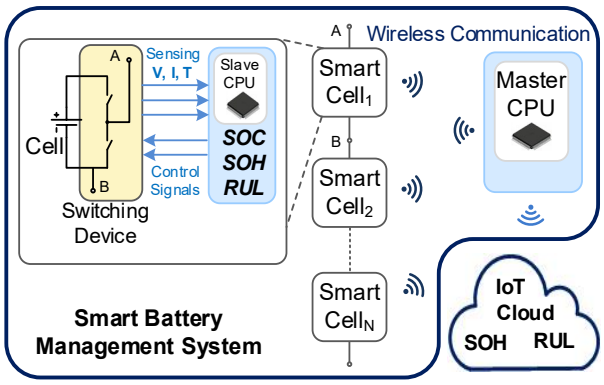


Figure 5: SB architecture showing master-slave wireless BMS.

As it can be observed from Fig. 5, the master sends either insert or bypass commands, based on the state from each cell. However, with the proposed method, the master will send the additional command for individual gate voltage control of the MOSFETs.

Each half bridge circuit is equipped with gate drivers to switch the top and bottom MOSFETs. Commercial gate

drivers (GDs) operate only in two states. During ON state, the GD applies the supply voltage (typically 15V) between gate and source to make the MOSFET on. Similarly, the GD will apply zero volts to turn-off the MOSFET. As the proposed method requires the bottom MOSFET to be fully on, fully off and in saturation mode, the gate drive circuitry needs to be modified.

Fig. 6 shows the proposed gate drive control for the bottom MOSFET.

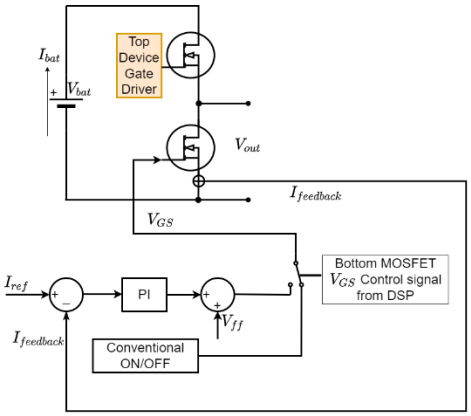


Figure 6: Proposed gate drive for the bottom MOSFET.

The operation of the proposed GD is explained below:

- During normal operation, when the SB cell is inserted, the top device is ON, the bottom GD produces zero voltage from the conventional ON/OFF control block.
- During bypass mode, the top device is OFF, while the bottom GD produces a high gate drive voltage (15V) to ensure that the bottom MOSFET carries the charge/ discharge current with minimal on-resistance.
- During balance mode, the closed-loop control shown in Fig. 6 gets activated. It will produce the desired analog voltage to ensure the desired current flow in the bottom MOSFET.

B. Practical Implementation

The practical implementation of the proposed method requires analog circuits such as opamps for realizing type 2 or type 3 controllers, summers to add an offset voltage to adjust for variations in temperature and threshold voltages, ORing diodes.

Fig. 7 shows the schematic of the proposed implementation.

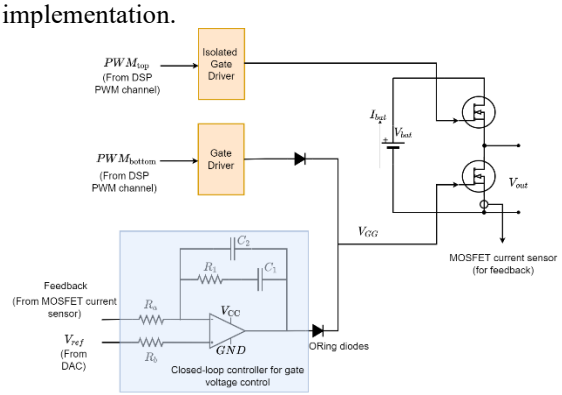


Figure 7: Proposed gate drive circuit for the SB cell.

The SB cell is controlled using a digital signal processor (DSP) which communicates with a master controller for performance optimization. This DSP produces the conventional PWM signals for the SB MOSFETs in complimentary fashion. Depending on the requirement of the balancing, a small analog circuit is included for the gate drive of the bottom device.

The analog circuit takes the reference current as an equivalent reference voltage V_{ref} from the digital-to-analog controller (DAC) output of the DSP. The master sends the balancing command to the slave, which in turn computes the amount of current needed for the balancing. The V_{ref} is computed proportional to the current required. During this mode of operation, the PWM from DSP is made low. Thus, V_{GG} in Fig. 7 is from the analog circuitry and the ORing diode at the output of low-side PWM will be reverse biased. During the bypass mode, even if there is a voltage from the opamp, the PWM signal will be high, hence the ORing diode will take over and completely turn-on the bottom MOSFET.

Let the maximum deviation in the SoC of the cells in the pack after which balancing is initiated be $SoC_{th}(\%)$. The balancing current can be computed based on the time necessary for balancing.

If the initial SoC is SoC_i and the target SoC is SoC_t, let the balancing current be Δi. Then, it can be written as,

$$SoC_t = SoC_i + \frac{1}{Q}\int_0^{T_b} \Delta i \, dt \qquad (5)$$

In (5), T_b is the time for balancing and Q is the capacity of the cell. Note that, it is necessary to have:

$$SoC_{th} > SoC_t - SoC_i \qquad (6)$$

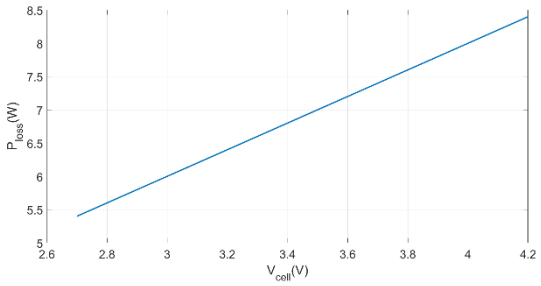
Now, the current for balancing is computed from (5) as,

$$\Delta i = \frac{(SoC_t - SoC_i)Q}{T_b} \qquad (7)$$

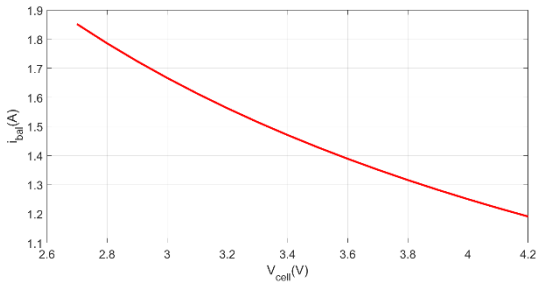
For example, in a 50Ah cell with 5% unbalance to trigger the proposed approach, a current of 1A will be necessary to ensure the balancing to complete in 2.5 hours, under ideal conditions. Note that conventional BMSs can take many hours to realize balancing since they operate with very low currents in the order of tens of milliamps. It is possible to have low current balancing in the proposed approach also since the current can be controlled in closed loop based on the reference from the DSP.

C. Power Loss Analysis

The current for balancing can also be set based on the power loss on the MOSFET. Consider the case, when constant balancing current of 2A is used. As described earlier, for a 50Ah cell, 2A balancing current can result in balancing in 1.25 hours for a predefined threshold of 5%. Fig. 8(a) shows the power loss versus cell voltage for this case. Similarly, if the power loss is fixed, the current will reduce with the cell voltage. The variation of the balancing current with the cell voltage for a predefined power loss of 5W is shown in Fig. 8(b). It is also possible to adaptively control the current based on the device temperature since the SB as shown in Fig. 5 is equipped with cell level temperature sensor.



(a)



(b)

Figure 8: (a) Power loss in the bottom MOSFET versus cell voltage, (b) Balancing current versus cell voltage for 5W power loss.

For the device IPLU300N04S4-R8 from Infineon, the junction to case thermal resistance $R_{th,jc} = 0.35\,K/W$. Thus, for a temperature rise of within 10K during balancing, the heatsink thermal resistance is calculated as below for a power loss of 5W.

Considering a case to sink thermal resistance $R_{th,cs} = 0.4\,K/W$ with a thermal paste, the heatsink thermal resistance to ambient $R_{th,sa}$ is,

$$R_{th,sa} = \frac{\Delta T}{R_{th,jc} + R_{th,cs}} = \frac{10}{0.35 + 0.4} = 13.33\,\frac{K}{W} \quad (8)$$

As the battery packs are typically in thermally controlled environment, it is possible to achieve the above thermal resistance or lower and hence the temperature rise can be minimized. Also, as mentioned earlier, the proposed approach can lower the current and reduce the temperature rise further. In that case, the balancing time will increase to the same order as the conventional passive BMS methods.

D. Controller Parameter Selection

The proposed gate driver uses a type-2 compensator for controlling the MOSFET current in closed loop. The compensator is shown in Fig. 7. The values of the resistors and capacitors is based on the dc gain and pole placement. As the proposed method does not require a very fast transient response, the first RC pole is placed at 50Hz. The second pole will be at 100 times higher frequency. The dc gain is tuned based on the response time required at these bandwidths. Fig. 9 shows the type 2 compensator implementation in LTSpice along with its parameter expressions. The bode plot of the proposed control for the specified pole placement is obtained from the ac analysis of LTSpice and it is shown in Fig. 10.

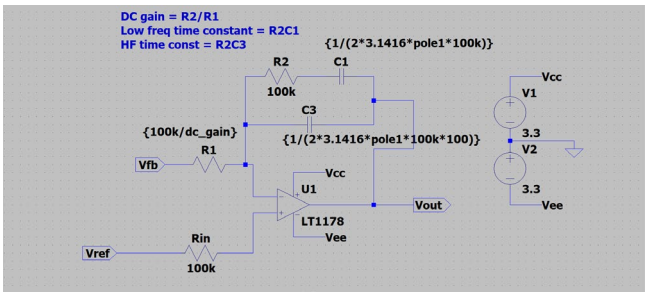


Figure 9: Type 2 compensator for closed-loop current control.

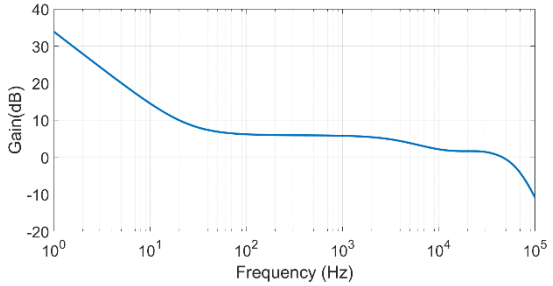


Figure 10: Bode gain plot for the designed type 2 compensator.

IV. Results

The control of the gate voltage is simulated using actual Spice models of the MOSFET and analog circuits provided by the manufacturers. The simulation is performed for a single SB with the cell voltage set at 4.2V. The discharge current is 20A. To illustrate the fine control of the circulating current, the reference is changed between 2A and 5A and the analog simulation shows perfect tracking of the reference. This is shown in Fig. 11.

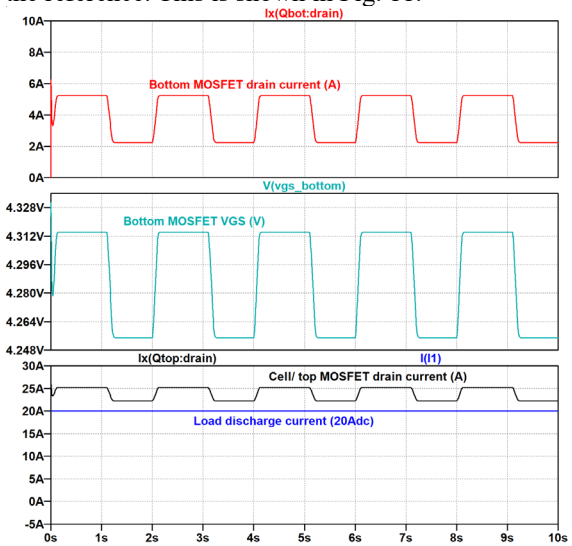


Figure 11: Performance of the proposed controller for step change in current reference.

The impact of the closed-loop control dc gain is highlighted next. In Fig. 12(a), the dc gain is set at 1. In Fig. 12(b), the dc gain is set at 5. As it can be observed, the higher dc gain results in faster transient response.

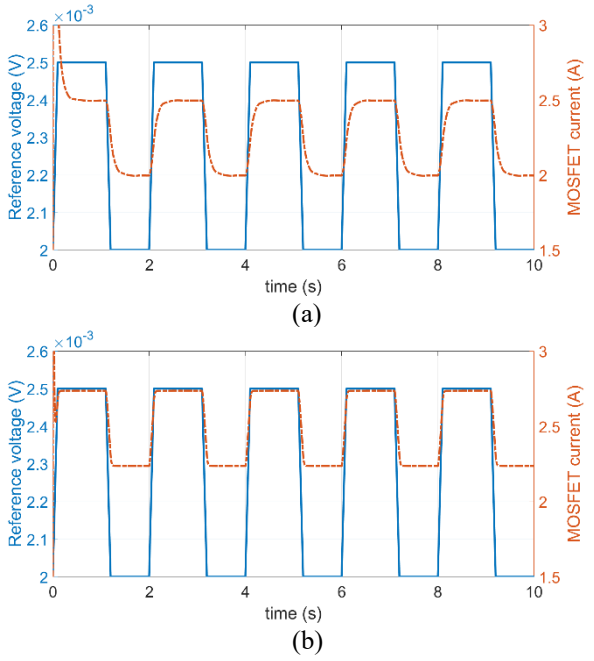


Figure 12: Transient response of the proposed controller (a) with dc gain = 1, (b) with a dc gain = 5.

The balancing method is illustrated using a simulation performed in Simulink using four 50Ah SB cells. The system considered is shown in Fig. 13. The Li ion cells used are of the NMC chemistry. The proposed gate driver has also been implemented in Simscape environment to demonstrate the balancing operation since Simscape provides easier modeling options for Li-ion cells compared to circuit simulation environment such as LTSpice.

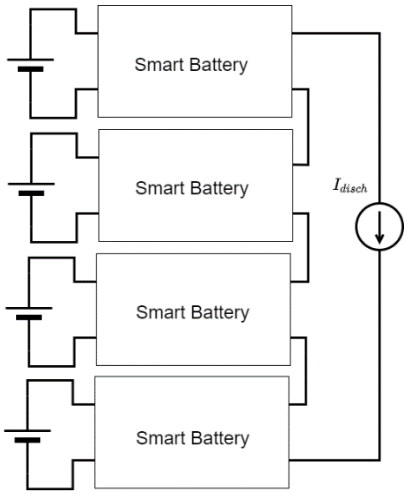


Figure 13: Setup condition for balancing.

The SoCs of the first three cells in Fig. 13 are respectively, 95%, 92% and 89% while the fourth cell has 50% SoC. It can be seen in Fig. 14 that the balancing occurs as expected. Note that balancing current can be controlled by the user to limit the power loss and to ensure that the SoCs never diverge to a large extent during any operating mode.

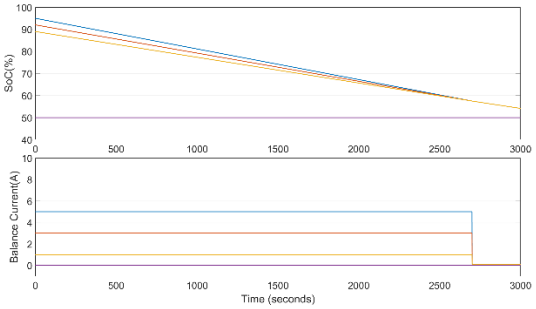


Figure 14: Illustration of charge balance with the proposed method.

V. Conclusions

In this paper, smart battery (SB) architecture is considered for Li-ion cells where each cell is embedded with a half bridge topology for providing additional operational modes for the cell. The SB architecture can facilitate pulsed operation which can improve the cycle life. A new balancing method is proposed for this architecture, where closed-loop current control of the bottom MOSFET is developed. This can provide additional current path to either increase the discharge current of the cell or to divert the excess charging current. This method can smoothly provide SoC balancing without additional active or passive balancing elements. The control and thermal design of this system is described. The proposed method has been validated with real device models and balancing has also been verified.

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