A Fully Integrated Darlington-Cascode Distributed Amplifier with m-Derived Matching Sections

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A Fully Integrated Darlington-Cascode Distributed Amplifier with m-derived Matching Sections

Yong Mu Yang, Xian Qi Lin, Senior Member, IEEE, Jin Sheng Dong, Peng Hao and Peng Mei

***Abstract*—This letter proposes a 0.01-40 GHz fully integrated Darlington-Cascode distributed amplifier (DA) in a commercial 0.15 μm GaAs pHEMT process. Analysis indicates that the Darlington-Cascode gain cell (DCGC) can simultaneously enhance gain, bandwidth, and output power. The first and last stage of the DA can be equivalent to two m-derived matching sections, optimizing the return loss of the input port. An on-chip DC-fed network is employed for DC biasing of the DA. The chip area of the DA is about 1.8 mm×1.5 mm. measurement results demonstrate that the distributed amplifier (DA) achieves a gain of 11 dB with ±1.5 dB flatness, 14%-24% power-added efficiency (PAE), and 17.2–19.5 dBm saturated output power.**

Index Terms—Distributed amplifiers, GaAs pHEMT, Darlington, Cascode, Gain, Wideband.

I. INTRODUCTION

DISTRIBUTED amplifiers (DAs), which have multioctave bandwidth [1][2][3], are attractive circuit blocks for applications such as optical links, high-resolution imaging, radar and measurement instrumentation. Advanced integrated circuit processes, such as InP [4][5][6], SOI [7], etc., boasting high cutoff frequencies (f_T), can significantly augment the bandwidth of DAs. However, with a fixed f_T, the gain, bandwidth, and power consumption of DAs become a set of trade-offs. Introducing a gate series capacitor can broaden the bandwidth of DAs, albeit at the expense of gain [8]. While cascaded topology enables high gain [9], it does so at the cost of increased power consumption. Non-uniform configuration [10][11][12] improves power-added efficiency (PAE), but the tapered output impedance restricts the effective use of the number of stages. The stack gain cells [13] can increase the output power of the DA but at the cost of a high voltage power supply. The DC bias of DAs is also a challenge, due to the wideband operation characteristics, external bias tees are usually required, which leads to larger circuit module size. Distributed choke inductor in [14] is used to feed the DA, however, this method significantly increases the chip area. Active bias termination topology in [15] is used to provide bias tee free DA, however, it will decrease the linearity of DA and increase the power consumption.

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Yong Mu Yang, Xian Qi Lin and Jin Sheng Dong and Peng Hao are with the Yangtze Delta Region Institute (Huzhou), University of Electronic Science and Technology of China, Huzhou 313001, P. R. China (e-mail: yym@csj.uestc.edu.cn; xqlin@uestc.edu.cn; dongjs@csj.uestc.edu.cn; penghao@csj.uestc.edu.cn).

Peng Mei is with the Department of Electronic Systems, Aalborg University, 9220 Aalborg, Denmark. (mei@es.aau.dk)

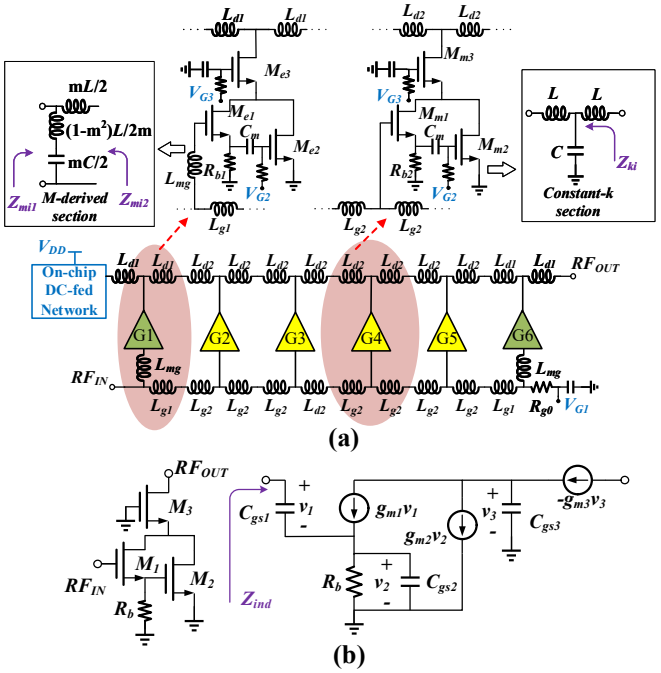

Fig. 1. (a) Schematic of the proposed DA (b) simplified topology and small-signal equivalent circuit of the DCGC.

This letter presents a fully integrated Darlington-Cascode distributed amplifier (DA) operating from 0.01 to 40 GHz, implemented in a commercial 0.15 μm GaAs pHEMT process. The incorporation of the Darlington-cascode gain cell serves to concurrently improve the gain and bandwidth of the DA. By accommodating larger device sizes and higher operating currents without compromising bandwidth, the gain cell also enhances the output power of the DA. The first and last gain cells of the DA can be equivalent to two m-derived matching sections, maintaining the input and output return loss better than 15 dB across the entire frequency range. Additionally, an on-chip DC-fed network is proposed to supply the drain DC bias and ensure a constant impedance termination for the output artificial transmission line (ATL), thereby eliminating the need for an external bias tee.

II. ANALYSIS AND CIRCUIT DESIGN

A. Darlington-Cascode Gain Cells

A typical distributed amplifier (DA) comprises n gain cells and input/output artificial transmission lines (ATLs). The bandwidth of a DA is primarily dictated by the cutoff frequency ω_C of the ATLs, which is defined as:

$$\omega_C = 2/CR_0 \ , \qquad (1)$$

where C denotes the input or output equivalent shunt

capacitance of the gain cell, and R_0 is the nominal characteristic impedance of the ATL, usually set to 50Ω for impedance matching. Since the input equivalent capacitance of the gain cell is larger than the output equivalent capacitance [14], the bandwidth of a DA is primarily constrained by the cutoff frequency of the input ATL. Therefore, from (1), bandwidth expansion can be achievable by reducing the shunt capacitance. A common strategy involves diminishing the overall device size of the gain cell, thereby reducing the equivalent capacitance. For an ideal DA, its gain G_{dis} can be expressed as:

$$G_{dis} = G_m^2 N^2 R_{0g} R_{0d}/4 \tag{2}$$

where, G_m is the equivalent transconductance of the gain cell, N is the number of gain cells, and R_{0g} and R_{0d} are the nominal characteristic impedances of the input and output ATLs, respectively. As G_m is proportional to the device size, adopting smaller devices diminishes the gain of the DA.

Fig.1(a) illustrates the schematic of the proposed DA as with the Darlington-Cascode gain cells (DCGCs). The DA comprises six gain cells, including four middle gain cells denoted as G2 to G5 and the first and last gain cells denoted as G1 and G6. As shown in Fig. 1(a) the DCGC consists of three transistors along with a capacitor C_m for DC decoupling and a resistor R_b for bias and stability. Fig.1(b) shows the simplified topology and small-signal equivalent circuit of the DCGC. From the small-signal equivalent circuit the input impedance of DCGC can be expressed as:

$$Z_{ind} = 1/j\omega C_{gs1} + 1/j\omega C_1 + 1/j\omega C_2 + R_1 + R_2 \ . \tag{3}$$

The parameters C_1, C_2, R_1, R_2 in (3) are given by:

$$C_1 = C_{gs1}(\omega^2 C_{gs2}^2 + g_b^2)/g_{m1} g_b \tag{4}$$

$$C_2 = g_b^2/\omega^2 C_{gs2} + C_{gs2} \tag{5}$$

$$R_1 = g_b/(\omega^2 C_{gs2}^2 + g_b^2) \tag{6}$$

$$R_2 = -g_{m1} C_{gs2}/C_{gs1}(\omega^2 C_{gs2}^2 + g_b^2) \tag{7}$$

where g_{m1} and g_{m2} are the transconductance of M_1 and M_2, C_{gs1} and C_{gs2} are the gate-source capacitance of M_1 and M_2, and g_b is the conductance of R_b. As indicated in equation (3), the input impedance of the DCGC can be conceptualized as a series of three capacitors, namely, C_{gs1}, C_1, C_2, and two resistors, namely, R_1, R_2. The total input capacitance of the gain cell is less than that of M_1. When R_b is sufficiently large that $g_b \approx 0$, and assuming similar sizes for M_1 and M_2, then the total input capacitance is expressed as:

$$C_{in} = C_{gs1} C_{gs2}/(C_{gs1} + C_{gs2}) \approx C_{gs1}/2 \tag{8}$$

Thus, a distributed amplifier employing DCGCs can achieve a wider bandwidth due to the reduction in input capacitance. The equivalent transconductance G_m of the DCGC can also be obtained from the small-signal equivalent circuit of Fig.1(b), which expressed as:

$$G_m = g_{m1}(g_{m2} + g_b)/(g_{m1} + g_b) \tag{9}$$

Similarly, when g_b is much smaller than g_{m1} and g_{m2}, it can be given as $G_m \approx g_{m2}$. The transconductance of the gain cell is therefore mainly determined by g_{m2}. Thus, adjusting the sizes of M_1, M_2, and M_3 in the DCGC allows for individual tuning of the gain, bandwidth, and output power. For instance, M_1 should have a smaller periphery to decrease input capacitance for bandwidth extension, while M_2 should possess a larger periphery to enhance G_m and boost the gain. The common-gate transistor, M_3, is utilized to further enhance the gain, offer suitable output capacitance, and increase the isolation between the input and output ATLs.

From (7), it's important to note that R_2 is a negative resistor. If g_b is very small that the total input resistance $R_1 + R_2 \approx -g_{m1}/\omega^2 C_{gs2} C_{gs1}$. Due to the presence of negative resistance, this could lead to instability in the DA. However, if g_b is too large, it can lead to a decrease in gain. Therefore, the value of g_b needs to be chosen properly to balance stability and gain considerations [16].

B. M-derived Matching Sections

Traditionally, the ATL can be regarded as a cascade of n constant-k filter sections [17]. As shown in Fig. 1(a), for the input ATL, the gain cells G2 to G5 can be equivalent to four constant-k filter sections. The constant-*k* filter section is a symmetric two-port network, which exhibits equal input and output image impedances, defined as:

$$Z_{ki} = R_0 \sqrt{1 - (\omega^2/\omega_C^2\ )} \tag{10}$$

From (10), the frequency dependence of the image impedance of the constant-k filter section can result in impedance mismatch at higher frequencies, given the DA's fixed terminal impedance at 50 Ohm. Gain cells G1 and G6, with respect to the input ATL, can be equivalent to bisected m-derived matching sections. As shown in Fig. 1(a), the input and output image impedances Z_{mi1} and Z_{mi2} of the bisected m-derived matching section are defined as:

$$Z_{mi1} = R_0[1 - (1 - m^2)(\omega/\omega_C\ )^2]/\sqrt{1 - (\omega/\omega_C\ )^2} \tag{4}$$

$$Z_{mi2} = Z_{ki} = R_0 \sqrt{1 - (\omega^2/\omega_C^2\ )} \tag{5}$$

where $0 < m \leq 1$. The output image impedance Z_{mi2} remains the same as (1). The input image impedance Z_{mi1} allows us to use m to minimize its frequency dependence. An m value of 0.6 generally gives the best results [18]. Adjusting the device size of G1 and the inductance values of L_{mg} and L_{g1} allows achieving an m value of 0.6, thereby reducing the frequency dependence of the input ATL's image impedance.

C. Circuit Implementation

The proposed DAs were designed using a commercial 0.15um GaAs pHEMT process with 100μm substrate thickness. The f_T of 90 GHz, and the high transconductance of 460 mS/mm, make it suitable for broadband DA design. The transistors M_{e1}, M_{e2} and M_{e3} of the first and last gain cells have periphery of 2×25um, 2×75um, and 2×45um, respectively. The transistors M_{m1}, M_{m2} and M_{m3} of the middle gain cells have periphery of 2×50um, 2×100um, 2×70um, respectively. The inductor L_{mg} is implemented using a microstrip line with a length of 25μm and a width of 7μm. Similarly, the series inductors L_{g1}, L_{g2}, L_{d1}, and L_{d2} are realized using microstrip lines with lengths of 200μm, 248μm, 240μm, 364μm, and widths of 7μm, 7μm, 12μm,12μm, respectively.

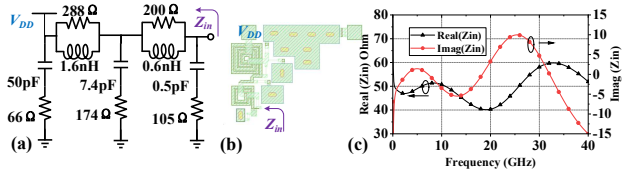

Fig. 2. (a) Schematic and (b) layout of the on-chip DC-fed network. (c) Simulated input impedance of the on-chip DC-fed network.

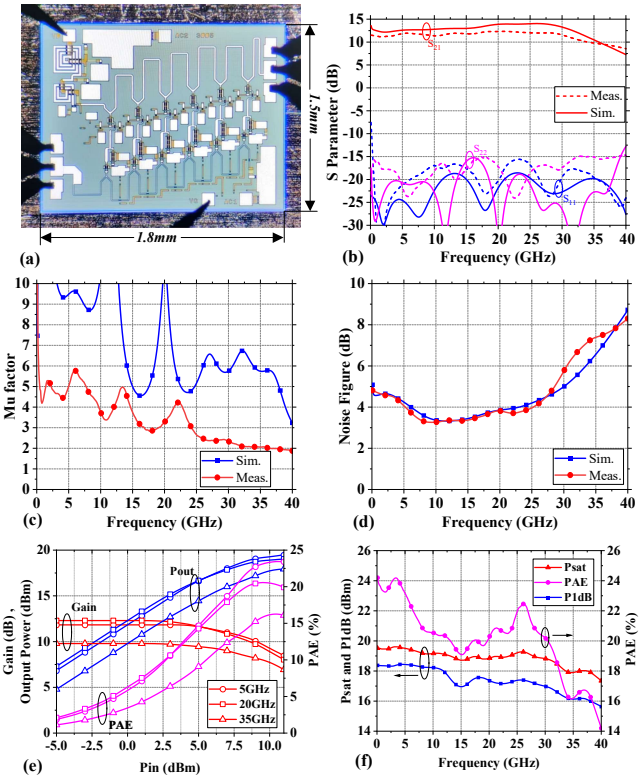

Fig. 3. (a) Micrograph of the DA chip. (b) Measured S-parameters. (c) Measured stability factor (μ-factor). (d) Measured noise figure. (e) Measured Pout, Gain, PAE versus input power. (f) Measured Psat, P1dB, PAE versus frequency.

The resistance value of R_b is chosen to be 32Ω, considering stability and overall gain. To ensure impedance matching of the ATLs, the right end of the input ATL is connected to a 50Ω resistor, grounded through a capacitor. The left end of the output ATL is connected to an on-chip DC-fed network, whose schematic and layout are shown in Fig. 2(a) and Fig. 2(b). The DC current can directly flow into the amplifier through the series inductor, which, due to its low resistance, minimally increases DC power consumption. For AC signals the DC-fed network acts as a constant impedance termination, with its impedance's real part, as shown in Fig. 2(c), ranging from 40-60Ω across the frequency range of 10MHz to 40GHz.

III. Measurement Results

The micrograph of the chip is shown in Fig. 3(a), and the chip occupies an area of 1.8 mm×1.5 mm. The DA is on-wafer measured with the supply voltage V_{DD} of 4V with a quiescent current of 60mA. All transistors in the DA utilize an on-chip resistive voltage-divider network for gate biasing.

TABLE I
PERFORMANCE COMPARISON WITH THE STATE-OF-THE-ART

Ref.	Tech.	BW (GHz)	Peak P1dB (dBm)	P_{dc} (mW)	Size (mm²)	Gain (dB)*	Fmax (GHz)	FOM
[10] MWTL	0.15um GaAs	0.8-18	19.2	330	4	10	220	6.23
[11] TCAS	0.1um GaAs	2-45	9.5	110	1.88	15.2	180	11.1
[15] TMTT	GaAs HEMT–HBT	DC-43.5	8	225	2	8.2	70	4.47
[6] TMTT	InP HBT	3-230	17.6	726	1.28	13	550	14.6
[3] MWCL	0.1um GaAs	0.01-22	20	3040	3.75	23	240	4.
[13] IMS	45nm SOI	1-17	18	427	1.14	15.8	300	4.85
[5] IMS	InP HBT	DC-90	19	400	1.12	10	380	14.8
THIS WORK	**0.15um GaAs**	**DC-40**	**18.3**	**240**	**2.7**	**11**	**220**	**18.09**

* The gain listed in the table represents the average gain in band.

The gate-source voltages for transistors M_{e1} and M_{m1} are set to -0.85V, M_{e2} and M_{m2} to -1V, and M_{e3} and M_{m3} to -0.8V. The measured S-parameters are presented in Fig. 3(b). The average small signal gain (S_{21}) is 11 dB from 0.01 to 40 GHz with the gain flatness of ±1.5dB. The input return loss is better than 15 dB, which benefits from the *m*-derived matching section. The measured stability factor (μ-factor) is greater than 2 up to 40 GHz [Fig. 3(c)]. The measured noise figure (NF) is < 8.2 dB at 0.01–40 GHz with a minimum of 3.1 dB at 13 GHz [Fig. 3(d)]. The continuous-wave (CW) large-signal performance versus frequency is shown in Fig. 3(e) and Fig. 3(f). The DA achieves an average Psat and P1dB of 18.5 and 17 dBm, respectively. The DA demonstrates a peak Psat and P1dB of 19.5 and 18.3 dBm, respectively, around 4 GHz. The maximum and minimum PAE are 24% at 4GHz and 14% at 40GHz. The performance summary and comparison of the proposed DA with other DAs are carried out in Table I. A figure-of-merit (FOM) in [13] is proposed as:

$$FOM = \frac{Gain[abs] \cdot BW_{3dB}[GHz] \cdot P1dB[mW]}{P_{dc}[mW] \cdot f_{max}[GHz]}(\%) \,. \quad (13)$$

Among the literature presented in Table I, the proposed DA can achieve best FOM.

IV. Conclusion

This letter presents a 0.01-40 GHz Darlington-Cascode distributed amplifier fabricates using a 0.15 μm GaAs process. Measurement shows it achieves 11 dB gain and 14%-24% PAE with 17.2–19.5 dBm saturated output power. The results show that the Darlington-Cascode gain cell has great potential for high gain bandwidth product distributed power amplifier designs.

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