Aalborg Universitet



Fault Recovery Analysis of Grid-Forming Inverters With Priority-Based Current Limiters

Fan, Bo; Wang, Xiongfei

Published in: IEEE Transactions on Power Systems

DOI (link to publication from Publisher): 10.1109/TPWRS.2022.3221209

Creative Commons License CC BY 4.0

Publication date: 2022

Document Version Publisher's PDF, also known as Version of record

Link to publication from Aalborg University

Citation for published version (APA): Fan, B., & Wang, X. (2022). Fault Recovery Analysis of Grid-Forming Inverters With Priority-Based Current Limiters. *IEEE Transactions on Power Systems*, *38*(6), 5102-5112. https://doi.org/10.1109/TPWRS.2022.3221209

General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
 You may not further distribute the material or use it for any profit-making activity or commercial gain
 You may freely distribute the URL identifying the publication in the public portal -

Take down policy

If you believe that this document breaches copyright please contact us at vbn@aub.aau.dk providing details, and we will remove access to the work immediately and investigate your claim.

Fault Recovery Analysis of Grid-Forming Inverters With Priority-Based Current Limiters

Bo Fan[®], *Member, IEEE*, and Xiongfei Wang[®], *Senior Member, IEEE*

Abstract—Grid-forming (GFM) inverters are required to operate robustly against grid faults. However, due to the limited overcurrent capability of inverters, current-limiting controls are usually applied to protect these semiconductor devices, which may prevent GFM inverters from a successful fault recovery. To understand this phenomenon, this study analyzes the fault recovery process of a GFM inverter with a priority-based current limiter. According to whether the GFM inverter can ensure transient stability and exit the current-limiting mode after fault clearance, three post-fault scenarios are identified, including *normal operation, current limitation, and oscillations*. Further, the impacts of the short-circuit ratio and control parameters on the post-fault behavior of GFM inverters are demonstrated. To illustrate the implications of these theoretical results, typical numerical examples are presented. Finally, the theoretical findings are validated through experimental tests.

Index Terms—Grid-forming (GFM) inverter, priority-based current limiter, fault recovery, post-fault phenomenon.

I. INTRODUCTION

POWER electronic inverters have been widely applied in power grids due to their efficient conversion and flexible control of electricity [1], [2]. Generally, inverters can be classified into two categories according to their control methods, i.e., grid-following (GFL) inverters and grid-forming (GFM) inverters [3], [4]. By directly regulating the voltage and frequency, GFM inverters are recognized as a promising solution for future inverter-dominated power grids [5].

In reality, temporary power grid faults are inevitable, such as short-circuit faults, grid phase angle jumps, etc. Reliable operation of the power grid requires GFM inverters to operate robustly against these grid faults. When faults are cleared, the GFM inverters should be able to automatically resume normal operation with guaranteed transient stability [6]. In the past years, the post-fault behavior of the GFM inverters has been investigated based on the phase plane analysis [7], [8] or the

Xiongfei Wang is with the Division of Electric Power and Energy Systems, KTH Royal Institute of Technology, 11428 Stockholm, Sweden, and also with the Department of Energy (AAU Energy), Aalborg University, 9220 Aalborg, Denmark (e-mail: xwa@energy.aau.dk).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPWRS.2022.3221209.

Digital Object Identifier 10.1109/TPWRS.2022.3221209

Lyapunov direct method [9]. However, these studies assume that the output currents of GFM inverters are always within the maximum allowable ranges.

Like synchronous generators (SGs), GFM inverters act as voltage sources behind impedance [10]. As a consequence, their output currents are highly dependent on the electrical network conditions [5]. Under grid faults, the SGs can provide short-circuit currents up to seven times the rated ones to the grid [11]. However, the semiconductor-based inverters can only handle tens of percent of over-current [6]. Therefore, current-limiting control strategies are critical to protect the GFM inverters.

To restrict the inverter output currents, one way is to switch the GFM inverters to the GFL ones in case of grid faults [12]. However, this solution requires a backup phase-locked loop (PLL), which may induce instability issues in weak grids [13], [14]. Alternatively, without switching the synchronization methods, two typical current-limiting control methods are proposed in the literature, i.e., virtual impedance methods [15] and current limiters [16], [17]. The former modifies the voltage control reference by adding virtual impedance when the inverter output current exceeds a given threshold [18]. The latter directly restricts the current reference signals by using circular or priority-based limiters [19], [20]. Comparative studies between these two types of current-limiting methods are performed in [21], which reveals that the current limiters can achieve a better current-limiting performance, while the virtual impedance methods can tolerate a longer fault period.

With these current-limiting controls, the post-fault behavior of the GFM inverters needs to be re-evaluated. In [22], a theoretical approach is proposed to explain the post-fault behavior of GFM inverters with virtual impedance. Further, Fan et al. [23] demonstrated the fault recovery process of GFM inverters with circular current limiters based on an equivalent circuit model. In [24], [25], transient instability induced by d-axis prioritybased current limiters when faults are cleared is revealed. In [26], an optimized priority-based current limiter is presented with improved transient stability.

When current-limiting strategies are applied, the "windup" or "latch-up" phenomena may exist in voltage control loops [5], [27], which prevent the GFM inverter from a successful fault recovery. More specifically, when faults are cleared, the GFM inverter can still remain in the current-limiting mode even if transient stability is ensured. In [15], it is shown that the virtual impedance methods are inherently free of these phenomena since the voltage control loops are always utilized to track their references in either normal operating mode or current-limiting

© 2022 The Authors. This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

Manuscript received 26 January 2022; revised 13 July 2022; accepted 6 November 2022. Date of publication 10 November 2022; date of current version 20 October 2023. This work was supported by the European Union's Horizon 2020 Research and Innovation Programme under the Marie Skłodowska-Curie Grant 101031512 (FRESLING). Paper no. TPWRS-00143-2022. (*Corresponding author: Xiongfei Wang.*)

Bo Fan is with the Department of Energy (AAU Energy), Aalborg University, 9220 Aalborg, Denmark (e-mail: bof@et.aau.dk).

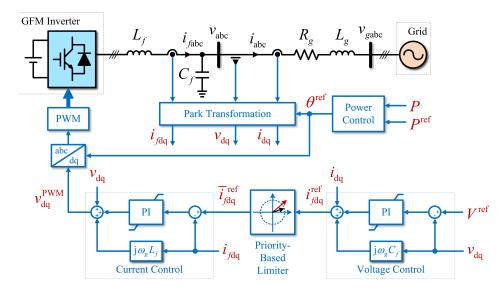


Fig. 1. Overall system diagram of a grid-connected GFM inverter with the priority-based current limiter.

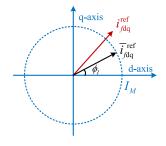


Fig. 2. Illustration of the priority-based current limiter.

mode [21], [22]. Moreover, the results in [23] reveal that the GFM inverter with circular current limiters can also avoid these phenomena since the inverter behaves similarly to those with virtual resistors. Different from the virtual impedance methods and the circular current limiters, the GFM inverters with priority-based current limiters will behave as power-synchronized current sources after fault clearance [28]. In previous studies [21], [25], [26], it is assumed that the GFM inverter can restore normal operation at the intersection point in the $P - \delta$ curves of the normal operating and current-limiting modes. However, no conditions are given under which this assumption is valid. The post-fault behavior of a GFM inverter with the priority-based current limiter is still an open issue and requires further investigation.

To approach this remaining issue, firstly, the GFM inverter models in both normal operating mode and current-limiting mode are derived. With these models, theoretical analysis results on the post-fault phenomena are obtained. Further, numerical examples are presented to illustrate the implications of the theoretical results. Finally, experimental tests are conducted to validate the theoretical findings. The main contributions of this study are as follows:

1) It is the first time that the fault recovery process of a GFM inverter with the priority-based current limiter is analyzed

theoretically. To facilitate the analysis, simplified closed-loop GFM inverter dynamic models are obtained in both normal operating mode and current-limiting mode.

2) This study presents a systematic approach to analyze the post-fault behavior of GFM inverters. The logic of switching between the normal operating mode and the current-limiting mode of GFM inverters is revealed, based on which three post-fault scenarios are identified, including *normal operation, current limitation, and oscillations*.

3) The impact of the current-limiting control parameters and short-circuit ratio (SCR) on the fault recovery process of the GFM inverter is revealed. Theoretical results indicate that the inverter with the priority-based limiter may fail to restore the normal operating mode in weak grids and even jeopardize transient stability under certain control parameters.

The remainder of this paper is organized as follows. Section II illustrates the system topology of a grid-connected GFM inverter and the control structure. The effect of the priority-based current limiter on the fault recovery process is analyzed theoretically in Section III. Numerical examples are given in Section IV and the corresponding experimental results are presented in Section V. Finally, Section VI concludes this paper.

Notation: For a complex variable x, $\operatorname{Re}\{x\}$ and $\operatorname{Im}\{x\}$ denote its real and imaginary parts, respectively. x_{abc} and x_{dq} denote xin the *abc*-frame and the *dq*-frame, respectively. x^* and ||x||are the conjugate and modulus of x, respectively. j is the unit imaginary number. The set \mathbb{S} denotes the unit circle [29]. For two sets $\Omega_A \subseteq \mathbb{S}$ and $\Omega_B \subseteq \mathbb{S}$, define $\Omega_A \setminus \Omega_B$ as the set difference, i.e., $\Omega_A \setminus \Omega_B = \{x | x \in \Omega_A \text{ and } x \notin \Omega_B\}$.

II. GRID-CONNECTED GFM INVERTER

A. System Description

Fig. 1 shows the topology of a GFM inverter connected to a power grid through an *LC*-filter. A power control loop is applied to synchronize the inverter with the grid. Voltage and current

proportional-integral (PI) control loops are used to regulate the capacitor voltage. The priority-based current limiter is applied in this study to protect the GFM inverter against over-current [16], [25], [26].

 C_f and L_f denote the filter's capacitance and inductance, respectively. R_g and L_g denote the resistance and inductance of the cable. i_{fabc} and i_{abc} represent the inverter-side current and the grid-side current, respectively. v_{abc} and v_{gabc} represent the capacitor voltage and the grid voltage, respectively.

B. Control Structure

For the ease of the demonstration of the fault recovery process, the P - f droop control is utilized as the power control loop, expressed as

$$\dot{\theta}^{\text{ref}} = \omega_g + K_P \left(P^{\text{ref}} - P \right) \tag{1}$$

where θ^{ref} is the phase angle reference used for the Park transformation in Fig. 1, ω_g is the grid angular frequency, P^{ref} is the active power reference, $P = \text{Re}\{v_{\text{dq}}i_{\text{dq}}^*\}$ is the active power output of the inverter, and $K_P > 0$ is the constant power control gain.

As shown in Fig. 2, the priority-based current limiter is expressed as

$$\bar{i}_{fdq}^{\text{ref}} = \begin{cases} I_M e^{j\phi_I}, & \|i_{fdq}^{\text{ref}}\| > I_M\\ i_{fdq}^{\text{ref}}, & \|i_{fdq}^{\text{ref}}\| \le I_M \end{cases}$$
(2)

where i_{fdq}^{ref} is the original inverter-side current reference generated by the voltage PI control, $\bar{i}_{fdq}^{\text{ref}}$ is the saturated current reference, I_M is the maximum allowable inverter-side current magnitude, and ϕ_I is a user-defined constant angle, representing the angle between the inverter-side current vector and the d-axis oriented to θ^{ref} . Two selections for ϕ_I are commonly used in the literature. When $\phi_I = 0$, the current limiter becomes a d-axis priority-based one [16], [25]. Rokrok et al. [26] presented an optimized selection method with $-\pi/2 < \phi_I < 0$.

Notice that once the current limiter is triggered, the voltage controller will behave as a fault detector, determining whether the GFM inverter remains operating at the current-limiting mode $(\|i_{fdq}^{ref}\| > I_M)$ or switch back to the normal operating mode $(\|i_{fdq}^{ref}\| > I_M)$.

During normal operation, the output of the voltage integrator is close to zero in the steady-state since it is merely used to remove the impact of modeling errors [30]. Therefore, once the current limiter is triggered, the voltage integrator is kept at zero to avoid its windup [23].

Usually, the inner control loops are designed to be much faster than the outer power one [2], [3], [5]. Hence, the following commonly used assumptions are introduced.

Assumption ([25], [26]): The dynamics of the capacitor and inductors is negligible. The dynamics of the current control

loop is negligible, i.e., $i_{fdq} = \bar{i}_{fdq}^{ref}$. During normal operation, the voltage control loop is idealized as a unity gain, i.e., $v_{dq} = V^{ref}$ with V^{ref} being the capacitor voltage reference.

Remark 1: In this study, the current limitation is achieved by a current control loop with the current reference satisfying $\|\bar{i}_{fdq}^{ref}\| \leq I_M$. If I_M is chosen close to the threshold of the conventional protection scheme that freezes the PWM signals, temporary over-currents may trigger the conventional protection scheme during current transients. In practice, I_M is usually selected to be smaller than the threshold of conventional protection schemes to avoid this issue.

III. EFFECT OF PRIORITY-BASED CURRENT LIMITER ON FAULT RECOVERY

In this section, the effect of the priority-based current limiter on the fault recovery process is analyzed. Firstly, the closedloop system model is established. Further, the logic of switching between the normal operating mode and the current-limiting mode of the GFM inverter is derived, based on which the fault recovery process is analyzed.

A. System Modeling

With the Park transformation shown in Fig. 1, the grid voltage can be rewritten as $v_{gdq} = V_g e^{-j\delta}$ where $\delta \triangleq \theta^{ref} - \theta_g$ with V_g and θ_g being its amplitude and angular frequency, respectively. Based on Kirchhoff's Circuit Law and Assumption, the expressions of the physical variables i_{fdq} , i_{dq} , and v_{dq} with respect to δ can be derived and found in Appendix.

When the current limiter is not triggered, one has $v_{dq} = V^{ref}$. According to Appendix A and $P = \text{Re}\{v_{dq}i_{dq}^*\}$, the active power output can be calculated as

$$P(\delta) = \frac{R_g \left(V^{\text{ref}}\right)^2 - R_g V^{\text{ref}} V_g \cos \delta + X_g V^{\text{ref}} V_g \sin \delta}{R_g^2 + X_g^2}.$$
 (3)

When the current limiter is triggered, according to Appendix B, the active power output is calculated as in (4) shown at the bottom of this page.

By revoking (1), the closed-loop system dynamics can be represented as

$$\dot{\delta} = K_P \left(P^{\text{ref}} - P(\delta) \right)$$

$$P(\delta) = \begin{cases} (3), & \text{Normal operating mode} \\ (4), & \text{Current-limiting mode} \end{cases}$$
(5)

As shown in (5), the closed-loop system has two operating modes. In previous studies [21], [25], [26], theoretical results of when the closed-loop system enters the current-limiting mode are explained. However, there is still a lack of theoretical analysis of the post-fault behavior of the inverter, i.e., the phenomena after clearing faults.

$$P(\delta) = \frac{R_g I_M^2 + \frac{R_g}{X_c} V_g I_M \sin(\delta + \phi_I) + \left(\frac{X_g}{X_c} + 1\right) V_g I_M \cos(\delta + \phi_I)}{\left(\frac{X_g}{X_c} + 1\right)^2 + \left(\frac{R_g}{X_c}\right)^2}$$
(4)

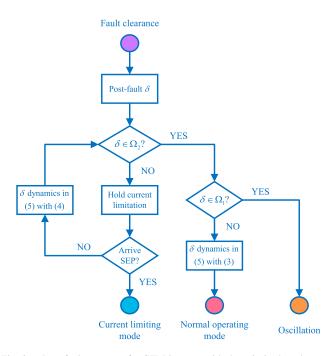


Fig. 3. Post-fault process of a GFM inverter with the priority-based current limiter.

B. Operating-Mode Switching Logic

To analyze the post-fault phenomena, the operating-mode switching logic is firstly derived.

1) From Normal Operating Mode to Current-Limiting Mode: According to (2), the inverter restricts its inverter-side current if $\|i_{fdq}^{ref}\|$ during normal operation is greater than I_M . Based on the assumption $i_{fdq} = \bar{i}_{fdq}^{ref}$ and the premise $\bar{i}_{fdq}^{ref} = i_{fdq}^{ref}$, the GFM inverter enters the current-limiting mode if

$$\delta \in \Omega_1 \triangleq \left\{ \delta' \in \mathbb{S} | \| i_{fdq} \left(\delta' \right) \| > I_M \right\}$$
(6)

with $i_{fdq}(\delta')$ given in (9).

2) From Current-Limiting Mode to Normal Operating Mode: Based on (2), the inverter exits the current-limiting mode if $\|i_{fdq}^{ref}\|$ is smaller or equal to I_M . With the considered voltage control loop in Fig. 1 and the anti-windup method in Section II-B, the GFM inverter switches back to the normal operating mode if

$$\delta \in \Omega_2 \triangleq \left\{ \delta' \in \mathbb{S} \big| \|i_{fdq}^{\text{ref}}(\delta')\| \le I_M \right\}$$
(7)

where $i_{fdq}^{ref}(\delta') = i_{dq}(\delta') + \frac{v_{dq}(\delta')}{jX_c} + K_P^V(V^{ref} - v_{dq}(\delta'))$ with $K_P^V > 0$ being the voltage proportional control gain and $v_{dq}(\delta')$, $i_{dq}(\delta')$ given in (10), (11), respectively.

Equations (6) and (7) reveal the switching mechanism between the two modes of the GFM inverter with the closed-loop system dynamics in (5). The two sets Ω_1 and Ω_2 determine the restricted operating areas for δ in the normal operating mode and the current-limiting mode, respectively.

Remark 2: Note that the operating-mode switching logic is developed based on (2). For other state-dependent switching logic, the post-fault behavior of the GFM inverter with the

TABLE I System and Control Parameters

Quantity	ValueValueValue(Set 1)(Set 2)(Set 3)
Cable inductance L_g Cable ESR R_g	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $
Grid phase voltage V_g Grid angular frequency ω_g LC -filter L_f and C_f Active power reference P^{ref} Voltage reference V^{ref} Power control gain K_P Maximum current I_M Voltage control P & I gain Current control P & I gain Switching frequency Sampling frequency	$\begin{array}{c} 77\sqrt{2} \ \mathrm{V} \ (1 \ \mathrm{p.u.}) \\ 100\pi \ \mathrm{rad/s} \ (1 \ \mathrm{p.u.}) \\ 1.5 \ \mathrm{mH}, \ 15 \ \mu\mathrm{F} \\ 2.56 \ \mathrm{kW} \ (0.8 \ \mathrm{p.u.}) \\ 1 \ \mathrm{p.u.} \\ 0.01 \ \mathrm{p.u.} \\ 1.2 \ \mathrm{p.u.} \\ 0.5 \ \mathrm{p.u.}, \ 20 \ \mathrm{p.u.} \\ 2.0 \ \mathrm{p.u.}, \ 10 \ \mathrm{p.u.} \\ 10 \ \mathrm{kHz} \\ 10 \ \mathrm{kHz} \end{array}$

priority-based limiter can be readily analyzed by re-calculating the two sets Ω_1 and Ω_2 .

C. Fault Recovery Analysis

If the current limiter is never triggered, the fault recovery analysis can be found in [7]. Therefore, this study focuses on the analysis of the fault recovery process when the priority-based current limiter is triggered during the fault.

Three post-fault phenomena are found and illustrated as follows:

1) Current-Limiting Mode ($\delta \notin \Omega_2$): As illustrated in Section III-B2, once the current limiter is triggered, the GFM inverter will remain in the current-limiting mode since $\forall \delta \notin \Omega_2$, $\|i_{fdg}^{ref}\| > I_M$.

2) Normal Operating Mode ($\delta \in \Omega_2 \setminus \Omega_1$): Since $\delta \in \Omega_2$, the GFM inverter can exit the current-limiting mode. Thereafter, the voltage controller tries to regulate the capacitor voltage v_{dq} to its reference V^{ref} . According to Section III-B1, the current limiter cannot be triggered again since $\forall \delta \notin \Omega_1, \|i_{fdq}\| \leq I_M$. The GFM inverter can remain in the normal operating mode.

3) Oscillations ($\delta \in \Omega_1 \cap \Omega_2$): Since $\delta \in \Omega_2$, the GFM inverter tends to restore the normal operating mode. In the meantime, however, $\delta \in \Omega_1$ induces an inverter-side current that is larger than I_M , triggering the current limiter again. Consequently, the current limiter introduces oscillations to the GFM inverter due to the switching between the normal operating mode and the current-limiting mode.

The whole post-fault process can be a combination of these three phenomena, which is depicted in Fig. 3. The abbreviation "SEP" stands for the stable equilibrium point. Numerical examples are presented in Section IV for ease of understanding. Experimental tests verify the numerical examples are given in Section V.

D. Impact of SCR and ϕ_I on Fault Recovery Process

Based on these theoretical results, the impacts of the SCR and ϕ_I on the fault recovery process are explained. The parameters in Table I are utilized. An X/R ratio of 12.5 is selected in the calculation. The corresponding results are given in Fig. 4, where three main areas are identified.

TABLE II NUMERICAL EXAMPLE SETUP

Area $ \delta$ smaller than the UEP $ \delta$ larger than the UEP $ \delta$ in the oscillation zone $ \delta$ outside the oscillation zone						
Example 1 Example 3	Example 2 Example 4	n/a n/a	n/a n/a Example 6			
	Example 1	Example 1 Example 2 Example 3 Example 4	Example 1Example 2n/aExample 3Example 4n/a			

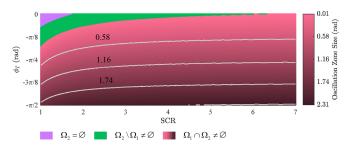


Fig. 4. Impact of SCR and ϕ_I on the fault recovery process.

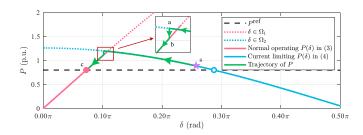


Fig. 5. Example 1–Trajectory of P with the parameters in Set 1 and the postfault δ being smaller than the UEP in the current-limiting mode. SEP: solid dot (•). UEP: hollow dot (•). Post-fault δ : star (*).

Purple area: This area denotes the one of $\Omega_2 = \emptyset$. More specifically, once a GFM inverter with the SCR and ϕ_I in this area enters the current-limiting mode, it cannot restore the normal operating mode after fault clearance.

Green area: This area denotes the one of $\Omega_2 \setminus \Omega_1 \neq \emptyset$, in which a GFM inverter may be able to exit the current-limiting mode after fault clearance. However, a successful fault recovery is not guaranteed since the GFM inverter can stabilize at an abnormal SEP before δ enters $\Omega_2 \setminus \Omega_1$.

Pink area: This area represents the one of $\Omega_1 \cap \Omega_2 \neq \emptyset$. Hence, the GFM inverter can suffer from oscillations after fault clearance if $\delta \in \Omega_1 \cap \Omega_2$.

For the impact of SCR, from Fig. 4, one can notice that for a grid with 1.7 < SCR < 6, a GFM inverter with the d-axis priority-based limiter ($\phi_I = 0$) may be able to recover from the post-fault status. When SCR drops below 1.7, the d-axis priority-based limiter can prevent the GFM inverter from a successful fault recovery since $\Omega_2 = \emptyset$. When SCR increases above 6, oscillation zones are observed based on the analysis in Section III-C.

For the impact of ϕ_I , when SCR > 1, 7, one can notice that as ϕ_I decreases from 0 to $-\pi/2$, the size of the oscillation zone increases. When SCR < 1.7, the decrease in ϕ_I can help the GFM inverter to restore the normal operating mode. However, the further decrease in ϕ_I will again increase the size of the oscillation zone.

IV. NUMERICAL EXAMPLES

Six typical numerical examples are applied in this section to illustrate the post-fault phenomena when the GFM inverter lies in different areas given in Fig. 4. The setup for these examples is given in Table II. The abbreviation "UEP" stands for the unstable equilibrium point. The system and control parameters used in these examples are listed in Table I. The fault recovery process is demonstrated through $P - \delta$ curves in the following examples.

A. Example 1

In this example, the parameters in Set 1 are utilized, where the priority-based current limiter is selected as the d-axis one $(\phi_I = 0)$. The SCR of the system is 3.54. According to Fig. 4, one can notice that the GFM inverter may be able to recover from the post-fault status. Assume that the post-fault δ is smaller than the UEP in the current-limiting mode.

The abscissa of the purple star denotes the post-fault angle δ . The solid and hollow dots with different colors denote the SEP and UEP in corresponding operating modes, respectively. The theoretically calculated trajectory of P is illustrated in Fig. 5, denoted by the green line with the arrows being the moving direction. The pink and blue lines represent the $P(\delta)$ in normal operating and current-limiting modes, respectively. The dashed lines denote the restricted areas where the GFM inverter needs to switch its operating mode. These legends will be utilized in the following examples.

The whole fault recovery process is demonstrated through the following three steps:

Step 1: As denoted by point "s" in Fig. 5, since the post-fault δ satisfies $\delta \notin \Omega_2$, the GFM inverter remains in the currentlimiting mode according to Section III-C1. Moreover, notice that P is larger than its reference. Based on (5), δ keeps decreasing along with the blue line.

Step 2: As shown in the zoomed picture in Fig. 5, δ keeps decreasing until it reaches point "a" and enters the restricted area Ω_2 , denoted by the dashed blue line. Therefore, the GFM inverter needs to exit the current-limiting mode. At the same time, $\delta \notin \Omega_1$ holds, i.e., the corresponding pink line is solid. Therefore, the GFM inverter restores the normal operating mode. The power output *P* jumps from the blue line to the pink one, denoted by the vertical green line between point "a" and "b".

Step 3: When the GFM inverter restores the normal operating mode, P is still larger than its reference. Hence, with the help of (5), δ keeps decreasing along with the pink line until it returns its normal SEP, denoted by point "c".

In this example, the GFM inverter can successfully recover from the current-limiting mode.

Remark 3: In previous studies [21], [25], [26], it is usually assumed that the GFM inverter can automatically restore the

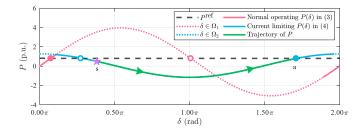


Fig. 6. Example 2–Trajectory of P with the parameters in Set 1 and the postfault δ being larger than the UEP in the current-limiting mode. SEP: solid dot (•). UEP: hollow dot (\circ). Post-fault δ : star (\star).

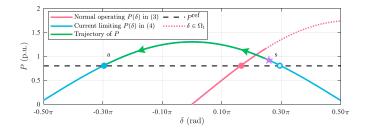


Fig. 7. Example 3–Trajectory of P with the parameters in Set 2 and the postfault δ being smaller than the UEP in the current-limiting mode. SEP: solid dot (•). UEP: hollow dot (\circ). Post-fault δ : star (\star).

normal operating mode if the post-fault δ is smaller than the UEP. However, according to Section III-C2, such an assumption is only valid in situations similar to Example 1, i.e., δ can enter the non-empty set $\Omega_2 \setminus \Omega_1$.

B. Example 2

This example again uses the parameters in Set 1. Different from Example 1, this example analyzes the system response when the post-fault δ is larger than the UEP in the currentlimiting mode. The theoretically calculated trajectory of P is illustrated in Fig. 6.

According to Section III-C1, the GFM inverter has to remain in the current-limiting mode since $\delta \notin \Omega_2$, as denoted by point "s". Besides, the power output P is smaller than its reference and thus δ keeps increasing along with the blue line based on (5). Finally, the GFM inverter stabilizes at the SEP in the currentlimiting mode, represented by point "a".

This example indicates that the GFM inverter cannot recover from the current-limiting mode even the set $\Omega_2 \setminus \Omega_1$ is non-empty since the GFM inverter will not enter the restricted area Ω_2 before it reaches an SEP.

C. Example 3

Example 3 utilizes the parameters in Set 2. The d-axis prioritybased current limiter is applied again, while the cable impedance is increased. The SCR drops to 1.61. According to Fig. 4, the GFM inverter cannot restore the normal operating mode since Ω_2 is empty. Assume that the post-fault δ is smaller than the UEP in the current-limiting mode. The theoretically calculated trajectory of P is illustrated in Fig. 7.

Notice that in this example, the power output P is larger than its reference and thus δ keeps decreasing along with the blue

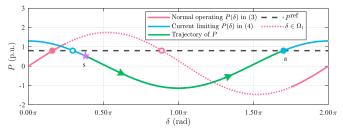


Fig. 8. Example 4–Trajectory of P with the parameters in Set 2 and the postfault δ being larger than the UEP in the current-limiting mode. SEP: solid dot (•). UEP: hollow dot (\circ). Post-fault δ : star (\star).

line based on (5), which is illustrated by the green line between point "s" and "a". Thereafter, the GFM inverter stabilizes at an SEP in the current-limiting mode.

Again, the GFM inverter cannot recover from the currentlimiting mode in this example since the set Ω_2 is empty.

D. Example 4

Example 4 also applies the parameters in Set 2, but assumes that the post-fault δ is larger than the UEP in the current-limiting mode. The theoretically calculated trajectory of P is illustrated in Fig. 8.

Since Ω_2 is empty with the parameters in Set 2, the GFM inverter remains in the current-limiting mode according to Section III-C1. In this example, the power output *P* is smaller than its reference and thus δ keeps increasing along with the blue line, which is represented by the green line between point "s" and "a". Finally, the GFM inverter stabilizes at a new SEP in the current-limiting mode.

In this example, again, the GFM inverter cannot recover from the current-limiting mode due to the empty set Ω_2 .

Remark 4: Unlike the previous Examples 1 and 2, Examples 3 and 4 indicate that the modification of the power control loop that generates δ [25], or equivalently θ^{ref} in Fig. 1, is helpless for a successful fault recovery since $\Omega_2 = \emptyset$. Once the current limiter is triggered, the inverter will become a power-synchronized current control grid-connected inverter [28] with a fixed inverter-side current magnitude I_M .

E. Example 5

In this example, the parameters in Set 3 are used. An optimized ϕ_I suggested in [26] is applied, which is about -1.4 rad. As shown in Figs. 4 and 9, an oscillation zone whose size is about 1.5 rad is observed.

According to Section III-C3, the GFM inverter will suffer from oscillations if the post-fault δ satisfies ($\delta \in \Omega_1$) \wedge ($\delta \in \Omega_2$) as depicted in Fig. 9. The GFM inverter may not recover from the current-limiting mode. If δ can finally leave the oscillation zone, the GFM inverter maybe stable. But in the worst case, δ can stay in the oscillation zone. Thereafter, the stability of the GFM inverter can be jeopardized.

Remark 5: According to the developed model in (5) and the analysis in Section III-B, the oscillation zones are identified, which indicates that the GFM inverter can suffer from

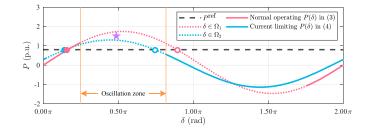


Fig. 9. Example 5–The post-fault δ falls in the oscillation zone with the parameters in Set 3. SEP: solid dot (•). UEP: hollow dot (\circ). Post-fault δ : star (\star).

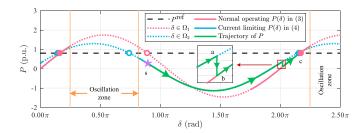


Fig. 10. Example 6–Trajectory of P with the parameters in Set 3 and the post-fault δ being not in the oscillation zone. SEP: solid dot (•). UEP: hollow dot (•). Post-fault δ : star (\star).

oscillations induced by the priority-based current limiters. However, the post-fault behavior of the GFM inverter after entering the oscillation zones cannot be demonstrated through the model in (5) since the dynamics of the current control loop and circuit can no longer be ignored.

F. Example 6

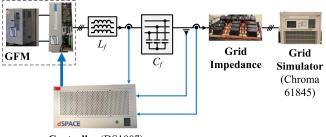
This example again uses the parameters in Set 3. Assume that the post-fault δ is not in the oscillation zone. The theoretically calculated trajectory of *P* is illustrated in Fig. 10.

The whole fault recovery process is demonstrated through the following three steps:

Step 1: The post-fault δ in Fig. 10 satisfies $\delta \notin \Omega_2$, denoted by point "s". Hence, the GFM inverter remains in the currentlimiting mode according to Section III-C1. Since *P* is smaller than its reference, δ keeps increasing along with the blue line based on (5), as represented by the green line between point "s" and "a".

Step 2: As shown in the zoomed picture in Fig. 10, similar to Example 1, δ keeps increasing until it enters the restricted area Ω_2 , denoted by the dashed blue line. Simultaneously, $\delta \notin \Omega_1$ holds, i.e., the corresponding pink line is solid. Hence, according to Section III-C2, the GFM inverter restores the normal operating mode. The power output P jumps from the blue line to the pink one, denoted by the vertical green line between point "a" and "b".

Step 3: When the GFM inverter restores the normal operating mode, P is still smaller than its reference. Hence, with Section III-C2 and (5), δ keeps increasing along with the pink line until it stabilizes at a normal SEP, represented by point "c".



Controller (DS1007)

Fig. 11. Illustration of the experimental setup.

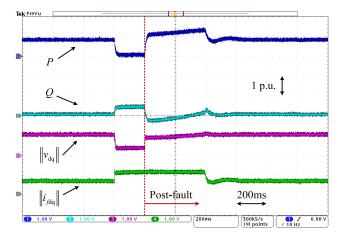


Fig. 12. Case 1–Experimental results of Example 1 with parameters in Set 1 under grid voltage drops to 0 p.u. for 200 ms.

In this example, the GFM inverter can successfully recover from the current-limiting mode. Although oscillation zones exist, the GFM inverter will not enter these zones before it reaches an SEP.

V. EXPERIMENTAL STUDIES

A. Experimental Setup

In this section, experimental results are performed to verify the numerical examples analyzed based on the theoretical results in Section III-C. The experimental setup is shown in Fig. 11, whose topology is the same as the one in Fig. 1. The power grid is emulated by the Grid Simulator Chroma 61845. The controllers are implemented in the DS1007 PPC processor board with an NXP QorIQ P5020 dual-core real-time processor (64-bit, 2 GHz) and a 32-bit I/O bus. The currents and voltages are measured through the DS2004 high-speed A/D board with a 16-bit resolution and 800 ns conversion time. The switching pulses are generated via the DS5101 digital waveform output board with a 25 ns resolution. The control and system parameters are listed in Table I. To obtain the post-fault status, a grid voltage drop to 0 p.u. with different fault periods is utilized.

B. Case 1: Experimental Results of Example 1

In this case, the parameters in Set 1 are used. The grid voltage drops to 0 p.u. for 200 ms to obtain a post-fault δ smaller than

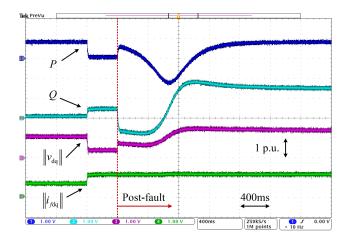


Fig. 13. Case 2–Experimental results of Example 2 with parameters in Set 1 under grid voltage drops to 0 p.u. for 400 ms.

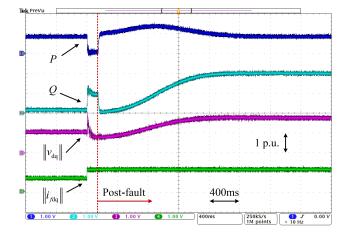


Fig. 14. Case 3–Experimental results of Example 3 with parameters in Set 2 under grid voltage drops to 0 p.u. for 150 ms.

the UEP in the current-limiting mode. The results are illustrated in Fig. 12.

Notice that although the fault is cleared, the post-fault system cannot restore its normal operating point for about 400 ms with the saturated inverter-side current. As illustrated in Section III-C1 and Example 1, such a phenomenon is due to the fact that $\delta \notin \Omega_2$, i.e., $||i_{fdq}^{ref}|| > I_M$ holds. Afterward, from Fig. 12, the GFM inverter restores and remains in the normal operating mode since δ enters the set ($\delta \notin \Omega_1$) \land ($\delta \in \Omega_2$), i.e., $||i_{fdq}^{ref}|| \leq I_M$ and the regulation of the capacitor voltage will not trigger the current limiter. Therefore, the GFM inverter successfully recovers from the current-limiting mode.

C. Case 2: Experimental Results of Example 2

In this case, the parameters in Set 1 are again applied, while the grid voltage drops to 0 p.u. for 400 ms to obtain a post-fault δ larger than the UEP in the current-limiting mode. The results are shown in Fig. 13.

From Fig. 13, it is obvious that the GFM inverter maintains in the current-limiting mode after fault clearance. As

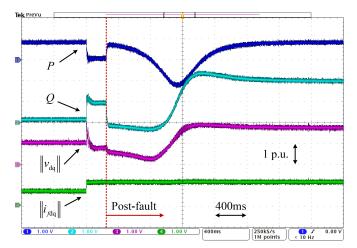


Fig. 15. Case 4–Experimental results of Example 4 with parameters in Set 2 under grid voltage drops to 0 p.u. for 250 ms.

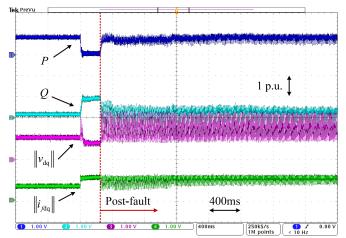


Fig. 16. Case 5–Experimental results of Example 5 with parameters in Set 3 under grid voltage drops to 0 p.u. for 250 ms.

demonstrated in Example 2, this phenomenon is induced since $\delta \notin \Omega_2$ holds, or equivalently, $\|i_{fdq}^{ref}\| > I_M$ holds. Hence, based on (2), the current limiter is always triggered, which prevents the GFM inverter successfully recovering from the fault.

D. Case 3: Experimental Results of Example 3

The parameters in Set 2 are applied in this case. A grid voltage drop to 0 p.u. for 150 ms is used to obtain a post-fault δ smaller than the UEP in the current-limiting mode. The results are shown in Fig. 14.

As shown in Fig. 14, the GFM inverter again maintains in the current-limiting mode after clearing the fault. With the parameters in Set 2 and the theoretical analysis in Example 3, one has that the set Ω_2 is empty. More specifically, once the current limiter is triggered, $||i_{fdq}^{ref}|| > I_M$ always holds. Hence, the GFM inverter cannot restore the normal operating mode even for a post-fault δ smaller than the UEP in the current-limiting mode as illustrated in Fig. 14.

TABLE III SUMMARY OF EXPERIMENTAL RESULTS

Case number	Priority-based current limiter type (ϕ_I)	Fault time	Cable impedance	Recoverable	Stable	Oscillation
1	d-axis (0 rad)	200 ms	$L_q = 5$ mH, $R_q = 0.2 \Omega$	1	1	×
2	d-axis (0 rad)	400 ms	$L_q = 5$ mH, $R_q = 0.2 \Omega$	×	1	×
3	d-axis (0 rad)	150 ms	$L_{q} = 11 \text{ mH}, \ R_{q} = 0.3 \ \Omega$	×	1	×
4	d-axis (0 rad)	250 ms	$L_{q} = 11 \text{ mH}, R_{q} = 0.3 \Omega$	×	1	×
5	Optimized (-1.4 rad)	250 ms	$L_{q} = 11 \text{ mH}, R_{q} = 0.3 \Omega$	×	X	1
6	Optimized (-1.4 rad)	700 ms	$L_{q} = 11 \text{ mH}, R_{q} = 0.3 \Omega$	1	1	1
7	Optimized (-1.4 rad)	1000 ms	$L_g = 11 \text{ mH}, R_g = 0.3 \Omega$	1	1	×

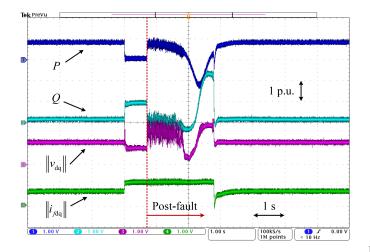


Fig. 17. Case 6–Experimental results of Example 5 with parameters in Set 3 under grid voltage drops to 0 p.u. for 700 ms.

E. Case 4: Experimental Results of Example 4

In this case, the parameters in Set 2 are applied. A grid voltage drop to 0 p.u. for 250 ms is used to obtain a post-fault δ larger than the UEP in the current-limiting mode. The corresponding results are shown in Fig. 15.

Notice that in Fig. 15, the GFM inverter still cannot restore the normal operating mode due to the empty Ω_2 as illustrated in Example 4.

F. Cases 5 and 6: Experimental Results of Example 5

In this test, the parameters in Set 3 are utilized, where oscillation zones exist according to Example 5. Grid voltage drops to 0 p.u. for 250 ms and 700 ms are used to obtain the post-fault δ falling in the oscillation zones. The corresponding results are shown in Figs. 16–17.

As illustrated in Example 5, once the post-fault δ falls in the oscillation zone, i.e., $(\delta \in \Omega_1) \wedge (\delta \in \Omega_2)$, the GFM inverter will suffer from oscillations induced by the current limiter. From Fig. 16, one can notice that the post-fault system is unstable due to these oscillations.

When the fault period increased, as shown in Fig. 17, the GFM inverter still suffers from oscillations for about 800 ms, but can finally leave the oscillation zone. Afterward, the system responses are almost identical to the theoretical analysis in Example 6, which will be discussed in detail in the next case.

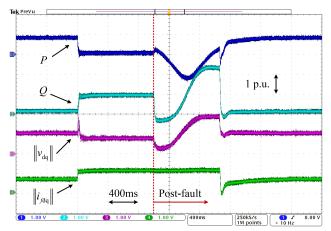


Fig. 18. Case 7–Experimental results of Example 6 with parameters in Set 3 under grid voltage drops to 0 p.u. for 1000 ms.

G. Case 7: Experimental Results of Example 6

In this case, the parameters in Set 3 are utilized, while the grid voltage drops to 0 p.u. for 1 s to make the post-fault δ be not in the oscillation zones. The corresponding results are shown in Fig. 18.

As shown in Fig. 18, the GFM inverter remains in the currentlimiting mode for about 800 ms. According to Section III-C1 and Example 6, this is because that $\delta \notin \Omega_2$. Thereafter, $\delta \in \Omega_2$ is met. Hence, the GFM inverter restores the normal operating mode, i.e., the inverter-side current is no longer saturated as observed in Fig. 18. Finally, although the oscillation zone exists, the GFM inverter stabilizes at an SEP in normal operating mode before it enters the oscillation zone.

Table III summarizes the experimental results. It can be observed that the GFM inverter can successfully recover from the current-limiting mode without oscillations only in the first and the last case. In Case 6, although the GFM inverter can also recover from the fault, it suffers from oscillations. In Cases 2-4, the GFM inverter is stable finally. However, it cannot exit the current-limiting mode. In the worst case (Case 5), the stability of the GFM inverter is jeopardized.

VI. CONCLUSION

This study has analyzed the fault recovery process of GFM inverters with priority-based current limiters. It has revealed the mechanism of switching between the normal operating mode and the current-limiting mode of the GFM inverters, based on which the *normal operation, current limitation, and oscillations* post-fault phenomena have been identified. Further theoretical analysis has indicated that the inverter with the priority-based limiter can fail to resume normal operation in weak grids and even suffer from transient instability issues. Finally, these results have been illustrated by numerical examples and verified by experimental results.

APPENDIX EXPRESSIONS OF PHYSICAL VARIABLES

A. Normal Operating Mode

When the current limiter is not triggered, one has $v_{dq} = V^{ref}$. Hence,

$$i_{\rm dq}(\delta) = \frac{V^{\rm ref} - V_g e^{-j\delta}}{R_g + jX_g} \tag{8}$$

and

$$i_{fdq}(\delta) = \frac{V^{ref}}{jX_c} + \frac{V^{ref} - V_g e^{-j\delta}}{R_g + jX_g}$$
(9)

where $X_g = \omega_g L_g$ and $X_c = -1/\omega_g C_f$.

B. Current-Limiting Mode

When the current limiter in (2) is triggered, the inverter-side current is determined by the angle ϕ_I , i.e., $i_{fdq} = I_M e^{j\phi_I}$. Therefore,

$$v_{\rm dq}(\delta) = \frac{(jR_g X_c - X_g X_c) I_M e^{j\phi_I} + jX_c V_g e^{-j\delta}}{R_g + j (X_g + X_c)}$$
(10)

and

$$i_{\rm dq}(\delta) = \frac{jX_c I_M e^{j\phi_I} - V_g e^{-j\delta}}{R_g + j \left(X_g + X_c\right)}.$$
 (11)

REFERENCES

- R. H. Lasseter, Z. Chen, and D. Pattabiraman, "Grid-forming inverters: A critical asset for the power grid," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 2, pp. 925–935, Jun. 2020.
- [2] B. Fan and X. Wang, "A Lyapunov-based nonlinear power control algorithm for grid-connected VSCs," *IEEE Trans. Ind. Electron.*, vol. 69, no. 3, pp. 2916–2926, Mar. 2022, doi: 10.1109/TIE.2021.3065614.
- [3] X. Wang, M. G. Taul, H. Wu, Y. Liao, F. Blaabjerg, and L. Harnefors, "Grid-synchronization stability of converter-based resources–An overview," *IEEE Open J. Ind. Appl.*, vol. 1, pp. 115–134, 2020.
- [4] L. Harnefors, J. Kukkola, M. Routimo, M. Hinkkanen, and X. Wang, "A universal controller for grid-connected voltage-source converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 5, pp. 5761–5770, Oct. 2021.
- [5] R. Rosso, X. Wang, M. Liserre, X. Lu, and S. Engelken, "Grid-forming converters: Control approaches, grid-synchronization, and future trends-a review," *IEEE Open J. Ind. Appl.*, vol. 2, pp. 93–109, 2021.
- [6] N. Hatziargyriou et al., "Stability definitions and characterization of dynamic behavior in systems with high penetration of power electronic interfaced technologies," IEEE Power Energy Soc., Piscataway, NJ, USA, Tech. Rep. PES-TR77, May 2020.
- [7] H. Wu and X. Wang, "Design-oriented transient stability analysis of gridconnected converters with power synchronization control," *IEEE Trans. Ind. Electron.*, vol. 66, no. 8, pp. 6473–6482, Aug. 2019.
- [8] D. Pan, X. Wang, F. Liu, and R. Shi, "Transient stability of voltage-source converters with grid-forming control: A design-oriented study," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 2, pp. 1019–1033, Jun. 2020.

- [9] Z. Shuai, C. Shen, X. Liu, Z. Li, and Z. J. Shen, "Transient angle stability of virtual synchronous generators using Lyapunov's direct method," *IEEE Trans. Smart Grid*, vol. 10, no. 4, pp. 4648–4661, Jul. 2019.
- [10] Y. Lin et al., "Research roadmap on grid-forming inverters," Nat. Renew. Energy Lab., Golden, CO, USA, Tech. Rep. NREL/TP-5D00-73476, Nov. 2020.
- [11] G. Denis, T. Prevost, M.-S. Debry, F. Xavier, X. Guillaud, and A. Menze, "The Migrate project: The challenges of operating a transmission grid with only inverter-based generation. a grid-forming control improvement with transient current-limiting control," *IET Renew. Power Gener.*, vol. 12, no. 5, pp. 523–529, 2018.
- [12] L. Zhang, L. Harnefors, and H.-P. Nee, "Power-synchronization control of grid-connected voltage-source converters," *IEEE Trans. Power Syst.*, vol. 25, no. 2, pp. 809–820, May 2010.
- [13] Q. Hu, L. Fu, F. Ma, and F. Ji, "Large signal synchronizing instability of PLL-based VSC connected to weak AC grid," *IEEE Trans. Power Syst.*, vol. 34, no. 4, pp. 3220–3229, Jul. 2019.
- [14] M. G. Taul, X. Wang, P. Davari, and F. Blaabjerg, "Current limiting control with enhanced dynamics of grid-forming converters during fault conditions," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 2, pp. 1062–1073, Jun. 2020.
- [15] A. D. Paquette and D. M. Divan, "Virtual impedance current limiting for inverters in microgrids with synchronous generators," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1630–1638, Mar./Apr. 2015.
- [16] P. Giroux and G. Sybille, Static Synchronous Compensator (STATCOM) Used for Midpoint Voltage Regulation on a 500 kV Transmission Line, Natick, MA, USA: The Math Works, 2006.
- [17] M. N. Marwali and A. Keyhani, "Control of distributed generation systems-part I: Voltages and currents control," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1541–1550, Nov. 2004.
- [18] T. Liu, X. Wang, F. Liu, K. Xin, and Y. Liu, "A current limiting method for single-loop voltage-magnitude controlled grid-forming converters during symmetrical faults," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4751–4763, Apr. 2022, doi: 10.1109/TPEL.2021.3122744.
- [19] B. Fan and X. Wang, "Impact of circular current limiters on transient stability of grid-forming converters," in *Proc. IEEE Int. Power Electron. Conf. (IPEC-Himeji Asia)*, 2022, pp. 429–434.
- [20] M. Awal and I. Husain, "Transient stability assessment for current constrained and unconstrained fault ride-through in virtual oscillator controlled converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 6, pp. 6935–6946, Dec. 2021, doi: 10.1109/JESTPE.2021.3080236.
- [21] T. Qoria, F. Gruson, F. Colas, X. Kestelyn, and X. Guillaud, "Current limiting algorithms and transient stability analysis of grid-forming VSCs," *Elect. Power Syst. Res.*, vol. 189, 2020, Art. no. 106726.
- [22] T. Qoria, F. Gruson, F. Colas, G. Denis, T. Prevost, and X. Guillaud, "Critical clearing time determination and enhancement of grid-forming converters embedding virtual impedance as current limitation algorithm," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 2, pp. 1050–1061, Jun. 2020.
- [23] B. Fan and X. Wang, "Equivalent circuit model of grid-forming converters with circular current limiter for transient stability analysis," *IEEE Trans. Power Syst.*, vol. 37, no. 4, pp. 3141–3144, Jul. 2022.
- [24] H. Xin, L. Huang, L. Zhang, Z. Wang, and J. Hu, "Synchronous instability mechanism of pf droop-controlled voltage source converter caused by current saturation," *IEEE Trans. Power Syst.*, vol. 31, no. 6, pp. 5206–5207, Nov. 2016.
- [25] L. Huang, H. Xin, Z. Wang, L. Zhang, K. Wu, and J. Hu, "Transient stability analysis and control design of droop-controlled voltage source converters considering current limitation," *IEEE Trans. Smart Grid*, vol. 10, no. 1, pp. 578–591, Jan. 2019.
- [26] E. Rokrok, T. Qoria, A. Bruyere, B. Francois, and X. Guillaud, "Transient stability assessment and enhancement of grid-forming converters embedding current reference saturation as current limiting strategy," *IEEE Trans. Power Syst.*, vol. 37, no. 2, pp. 1519–1531, Mar. 2022, doi: 10.1109/TP-WRS.2021.3107959.
- [27] N. Bottrell and T. C. Green, "Comparison of current-limiting strategies during fault ride-through of inverters to prevent latch-up and wind-up," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3786–3797, Jul. 2014.
- [28] X. Wang and X. Wang, "Power-synchronized current control for gridconnected converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2021, pp. 329–334.
- [29] J. W. Simpson-Porco, F. Dörfler, and F. Bullo, "Synchronization and power sharing for droop-controlled inverters in islanded microgrids," *Automatica*, vol. 49, no. 9, pp. 2603–2611, 2013.

[30] L. Harnefors, M. Bongiorno, and S. Lundberg, "Input-admittance calculation and shaping for controlled voltage-source converters," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3323–3334, Dec. 2007.



Bo Fan (Member, IEEE) received the B.S. degree in automation and the Ph.D. degree in control science and engineering from Zhejiang University, Hangzhou, China, in 2014 and 2019, respectively. Since 2020, he has been with the Department of Energy (AAU Energy), Aalborg University, Aalborg, Denmark, where he is currently a Postdoctoral Researcher. His research interests include power system stability, power electronics, smart grid, distributed control, and nonlinear systems. Dr. Fan was the recipient of the Best Reviewer Award of IEEE TRANSAC-

TIONS ON SMART GRID in 2019, Outstanding Reviewer Awards of IEEE TRANS-ACTIONS ON POWER SYSTEMS in 2019 and 2021, and Marie Skłodowska-Curie Individual Fellowship in 2021.



Xiongfei Wang (Senior Member, IEEE) received the B.S. degree in electrical engineering from Yanshan University, Qinhuangdao, China, in 2006, the M.S. degree in electrical engineering from the Harbin Institute of Technology, Harbin, China, in 2008, and the Ph.D. degree in energy technology from Aalborg University, Aalborg, Denmark, in 2013. Since 2009, he has been with the Department of Energy, Aalborg University (AAU Energy), where he became an Assistant Professor in 2014 and 2016, a Full Professor and Leader of Electronic Power Grid (eGrid) Research

Group in 2018. Since 2022, he has been a Full Professor with the KTH Royal Institute of Technology, Stockholm, Sweden. His research interests include modeling and control of power electronic converters and systems, stability and power quality of power-electronics-dominated power systems, and high-power converters. Dr. Wang is currently the Co-Editor-in-Chief of the IEEE TRANSAC-TIONS ON POWER ELECTRONICS and an Associate Editor for the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He was the recipient of 10 IEEE Prize Paper Awards, 2016 AAU Talent for Future Research Leaders, 2018 Richard M. Bass Outstanding Young Power Electronics Engineer Award, 2019 IEEE PELS Sustainable Energy Systems Technical Achievement Award, 2020 JESTPE Star Associate Editor Award, 2022 Isao Takahashi Power Electronics Award, and Highly Cited Researcher in the Web of Science from 2019.