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X-in-the-Loop Validation of Deep Learning-Based Virtual Sensing for Lifetime Estimation of Automotive Power Electronics Converters

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***Abstract*—Health degradation issues in automotive power electronics converter systems (PECs) are present due to repetitive thermomechanical stress endured while the vehicle is in real-field operation. This stress results from heat generation, a byproduct of semiconductor operation within PECs, leading to degradation in semiconductor operating life. The best practice in academia and industry is to rely on detailed Physics-of-Failure (PoF) based models for lifetime estimation. However, the PoF-based model of PECs requires substantial computational time and robust devices to estimate lifetime accurately. According to literature surveys, the computational time of the PoF-based models could be reduced further by using a low-fidelity and/or reduced-order model (ROM) that may result in unacceptable accuracy. To fulfill this research gap, this paper proposes a real-time executable, deep learning-based virtual sensing method that enables vehicle manufacturers to estimate the lifetime of the PECs onboard. This computationally efficient virtual sensing method has been integrated into an onboard vehicle validator edge (VVE). At the same time, multiple DL configurations are being explored, and optimization is performed on compositions, hyper-parameters, training, and testing datasets to obtain the best DL model. Finally, to demonstrate the feasibility and accuracy of the proposed method before its implementation within the complex VVE, an X-in-the-Loop (XiL) test is performed with vehicle frontloading.**

***Index Terms*—Virtual sensing, electric vehicles, power electronics converter, SiC power module, electro-thermal model, system-level lifetime, vehicle edge, and X-in-the-loop.**

I. INTRODUCTION

The need for clean and sustainable energy independence is one of the most crucial challenges facing the European Union (EU) today. The EU aims to make Europe the world's first climate-neutral continent by 2050. To achieve this ambitious aim, the EU declared manufacturing 100% zero-emission cars in 2035 [1]. This goal pushes for more sustainable growth and demand for electric vehicles (EVs) and anticipates a Compound Annual Growth Rate (CAGR) of >16% in the European vehicle market, which is expected to lead to an estimated revenue of $1.3 Trillion by 2032, compared to $303.6 billion in 2022, according to Global Market Insights 2023 report. Two aspects from the power electronics perspective are essential for EV industries to cope with this faster growth sustainability: (a) firstly, electrical energy efficiency enhancement of PECs which can significantly improve the overall battery electric vehicle (BEV) range utilizing new Wide-Band Gap (WBG) semiconductor materials [2], [3]. A recent press release of Infineon [4] highlights that PECs utilizing the WBG semiconductor materials exhibit a significant 5% reduction in battery capacity consumption. The report mentions that while a Si-based PEC requires a battery capacity of 91.3 kWh, adopting SiC lowers the energy requirement to 87.2 kWh due to the reduced losses associated with SiC PECs. To that, WBG-based PECs make it possible to achieve energy efficiency; however, PECs with WBG technology are not widely available at automotive quality yet [5]–[7]; (b) secondly, as the electronics inside BEVs become more complex and need to operate within harsh coolant temperatures ranges of -45^{0}C to 150^{0}C, the likelihood of failure in these devices is expected to rise. Therefore, the complexity of achieving a zero-failure rate in PECs is heightened by the intricate nature of these circuits, involving a multitude of electronic chips, active switches, and passive components, which may lead to potential safety hazards and significant costs associated with recalls.

Therefore, the PECs that are mounted in BEVs are expected to satisfy specific automotive lifetime tests set by *AEC Q100, Q101, Q200, IEC60749-34,* and/or *LV324,* as any failure or malfunction in these converters can have significant consequences, ranging from decreased vehicle efficiency and performance to potential safety hazards [7], [8]. Considering their essential role in enabling the proper functioning of critical vehicle systems, automotive PECs are deemed mission-critical components that directly affect the overall reliability and safety of the vehicle.

The automotive PEC designs generally assess their reliability by employing the Physics-of-Failure (PoF) credible model to conform to stringent safety requirements [7], [9]–[11]. According to articles [12]–[18], among thermo-mechanical stresses such as temperature, threshold voltage, vibration, and humidity, instantaneous temperature gradients i.e., junction temperature (Tj), and junction temperature swings (ΔTj), are the two thermal metrics crucial for estimating the most prevalent failure mode in WBG-based PECs. While Tj plays a significant role in package-related wear-out, ΔTj accelerates degradation, leading to various damages such as bond wire lift-off, solder joint damage, bond wire heel-crack, and wire rupture. By leveraging repetitive thermomechanical stress data alongside lifetime parameters, automotive power electronics reliability engineers can estimate either the overall lifetime of the PECs or predict the timing of potential failures [7], [15], [18]–[22].

A comprehensive list of multi-scale and multi-physics tools has been identified in the literature [7]–[21], [23], [24], [29] for the PoF-based reliability assessment. These tools encompass a wide array of models, spanning from accurate 1D electro-thermal simulations using circuit simulator tools such as

TABLE 1. PHYSICS-OF FAILURE-BASED LIFETIME ASSESSMENT METHODS FOR AUTOMOTIVE PECS.

Ref	Device under Test	Advantages and limitations	Maximum Error in Tj	Maximum Error in Lifetime	Execution Time	
					Simulation Time (s)	Time in model (s)
[22]	Discrete Si switch	✓ Machine learning-based lifetime model; computationally efficient to predict the damage progression in solder contacts; and optimized hyperparameters ✗ Large training dataset required to predict accurately	Damage prediction: less than 10 % using 350 h training data and less than 5 % using 1400 h training data length ~50% of the available dataset			
[29]	3-Phase Inverter	✓ Digital twin for thermal model comprises finite element analysis (FEA) simulation, two neural network models, and experimental validation on rated load condition. ✗ Junction temperature under diverse operating conditions, and in real-world scenarios are not tested, and the merits of this method in lifetime estimation are not investigated.	Under typical working conditions with a rated current load of over 150 A, demonstrates that the estimating accuracy of the digital twin approach exceeds 95%. The combined operating time of two NNs is reported to be 405.9 μs.			
[31], [32]	HV DC/DC converter	✓ Switched-based accurate model; used in switch fault/short circuit diagnosis ✗ High execution time is required; and mission profile simulation is not possible	0.20% MPE on 0.10 s	NA	0.1	90720
[31]	HV DC/DC converter	✓ Universal loss-based accurate model; PWM behaviour is captured; and used in PoF-based lifetime assessment ✗ Not applicable for RT deployment	0.55% MPE on 0.10 s	This is a benchmark model	1800	45000
[31]	HV DC/DC converter	✓ Average power loss model; RT monitor of maximum temperature ✗ Significant deviation in Tj swing; and less accurate lifetime assessment	0.61% MPE on 0.10 s	58% at reliability percentile 90%	1800	1725
[33]	3-Phase traction inverter	✓ Steady-state model; captured detailed operating mode of motor; and suitable for PoF-based lifetime assessment ✗ Not applicable for RT deployment	Less than 3%	3.83%	1800	12600
[34]	3-Phase traction inverter	✓ Switching period-based power loss model; effective for high dynamic system; and suitable for PoF-based lifetime assessment ✗ Not applicable for RT deployment	This is a benchmark model		598	Not available
[34]	3-Phase traction inverter	✓ Output period average power loss model; effective for less dynamic system; and faster than RT executable ✗ Significant deviation in Tj swing; Less accurate in lifetime assessment	Acceleration period: 20% Constant period: 0.5%	35.8 time for IGBT	598	Not available
[35]	3-Phase traction inverter	✓ Optimized ANN-based thermal equivalent model; exported as FMU block set for mission profile test; and good accuracy w.r.t Amesim thermal model ✗ Absence of RT deployment and HW test	IGBT and diode within $\pm$ 2% error	Within $\pm$ 2% error	1200	1200
[36]	Industrial inverter	✓ Machine learning based thermal model; effective for condition monitoring ✗ Not optimized for hyperparameters and large execution time 6000 parameters for CNN; Accuracy for Tj swing is not shown	MPE in case temperature: 0.94 on 500 min profile	NA	Training time: 403.84 sec	
Proposed model	HV DC/DC converter	✓ Optimized Deep learning-based thermal equivalent model; RT capable and highly accurate virtual sensor; less dependent on topology and applicable for any automotive PE converters, no additional sensor of edge is required; and suitable for PoF-based lifetime assessment ✗ Online training and parameter updates are not tested	RMSE → MOSFETs: 2.57, 3.52 Diodes: 1.97, 2.5 on entier 6700 s profile	The relative error is respectively 0.35% and 1.52% at the reliability percentile 99% and 90%	6700	6700

SABER, PSpice, PLECS, MATLAB Simulink/Simscape®, and LTSpice, to comprehensive 3D finite elements method-based (FEM) simulation tools like ANSYS, COMSOL, MagNet Infolytica, and JMAG.

While these 3D finite element models offer high accuracy, they often demand significant computational resources, requiring days or even weeks to compute simulations [18], [25]–[28]. To tackle this issue several methodologies have been adopted. For instance, in [29], the 3D high-fidelity thermal models are utilized to develop thermal digital twins reduced-order models to reduce the simulation time while sacrificing the accuracy of the model output. Siemens has introduced the Simcenter FLOEFD platform for this purpose, allowing the generation of reduced-order models up to 40X times faster than traditional 3D FEM models [30].

Table 1 presents thermal modeling and simulation techniques for PECs in automotive and industrial applications available in the literature. It highlights the challenges of accurate estimation and computational time, referencing prior research and various models. The table also provides quantitative data on simulation

time and accuracy of T_j estimation [7], [15], [33]–[36], [18]–[22], [30]–[32]. The various types of models namely equation-based model, switching model, 3D FEM, reduced order model, and machine learning-based models offer unique advantages and limitations. To achieve online condition monitoring and predictive health management, the reduced order model needs to be capable of real-time execution on commercially available microprocessors while maintaining good accuracy. Therefore, the objective of this paper is to address current research gaps and contribute to the development of a real-time executable and accurate model. This paper aims to achieve this goal through five folds results:

(a) First, experimental characterization of the semiconductor power module (i.e., double pulse test) is conducted to estimate power loss parameters during operation accurately. Often, datasheets offer specifications that are narrower than the range required for an automotive application, e.g., temperature. In this paper, an accurate device-level electro-thermal model is developed based on these experimental parameters, which encompasses switching and conduction losses. Then, a datasheet-driven Foster equivalent thermal model is utilized to create training data for deep learning-based (DL) models, effectively overcoming inaccuracies associated with the corresponding training data.

(b) Secondly, training datasets are required for multiple cycles to capture responses for different driving conditions to enhance the accuracy of the DL-based models. Therefore, as part of the idea, an acceptable simulation speed for the universal loss model of the device is ensured. This is obtained through a combination of parameters from experimental measurements and vendor datasheets, combining analytical equations and lookup tables (LUTs), effectively eliminating the need for differential or recursive equations. This universal loss model facilitates seamless integration of the semiconductor power module into the PEC model. Optimized simulation times enable the analysis of a driving cycle within a ballpark of hours, effectively supporting accurate estimation of Tj and ΔTj response for different driving cycles;

(c) Thirdly, an edge-deployable and optimal Deep Learning (DL) model is proposed that can predict the thermal response (i.e., Tj and ΔTj) of power switches in real-time with global control signals of PEC as input to the DL model. The challenge is to capture the dynamic behavior of non-linear systems with useful training data, which can replace computationally intensive mathematical models. This is an upcoming research area in power electronics for black box modelling, system identification, and virtual sensor design. In this respect, multiple DL configurations are explored, and holistic optimization is performed on compositions, hyper-parameters, training, and testing datasets to obtain the best RT executable DL model.

(d) Fourthly, the optimized DL model has been deployed on a dSPACE MicroLabBox to replicate the VVE, and it is referred to as the sensor-hardware-in-the-loop (sHiL) system. This step is taken to validate the feasibility and real-time operation (RTO) of the proposed DL model before investing in the effort/expense of physically implementing the proposed method. This is accomplished by using a heterogeneous strategy called X-in-the-Loop (XiL), which combines Software-in-the-Loop (SiL), sHiL, and Hardware-in-the-Loop (HiL) with a frontloading testbed facility.

(e) Finally, the accuracy of the proposed method in lifetime assessment is demonstrated using a state-of-the-art mission-profile-oriented reliability framework.

II. The Proposed Concept

In the following section, the main concept and methodology are outlined in a stepwise manner. The overall method is categorized into six different layers: (a) application definition, (b) characterization, (c) device modelling, (d) data-driven modelling, (e) X-in-the-Loop (XiL) testing, and (f) system-level lifetime estimation, as depicted in Figure 1.

As part of (a) the application layer, the specific device under test (DUT) and applied mission profile have been defined. An electric vehicle is composed of several power electronics converters with different ratings for different classes of EVs, namely on-board charger, traction inverter, High Voltage (HV) DC/DC converter, and Low Voltage (LV) DC/DC converter. In this paper, only pure battery electric light commercial vehicle (BEV) is considered. An EU H2020 project, HiFi-Elements, identified five different powertrain topologies of BEVs [37]. The difference between powertrain topologies arises with the presence of an HV DC/DC Converter between the Battery and Inverter. There are two possibilities: connect the battery system directly to the inverter or place an HV DC/DC booster between the battery and inverter. To boost the range of a BEV with the same battery size, three solutions are available, i.e., (a) increase the size of the e-motor or incorporating an additional motor – as seen in the case of Tesla's dual motor setup, which involves optimizing the front-wheel motor for power and the rear-wheel motor for extended range [38]; (b) employing a multi-speed gearbox in the BEV, that involves adjusting the speed and torque distribution to align with the efficient region of the e-motor. Notably, ZF Friedrichshafen AG has recently introduced a multi-speed drivetrain for BEVs [39] and (c) utilizing a bidirectional HV DC/DC boost converter between the battery and the inverter that controls the DC-link voltage at various motor load conditions to operate the inverter and motor efficiently, and thereby increasing the range. Therefore, a recent trend is to substitute a 400 V powertrain system with an 800 V and/or post 800 V powertrain utilizing an HV DC/DC converter to supply a stable voltage and to reduce the constraints in the electric motor (EM) design and to reduce the charging time considerably, e.g., Kia EV6, Porsche Tycan, Lucid Air and Hyundai Ioniq 5 [40]–[42]. The advantages of including HV DC/DC in BEVs are inevitable. Nonetheless, a noticeable absence of long-duration reliability test data for the HV DC/DC converter exists.

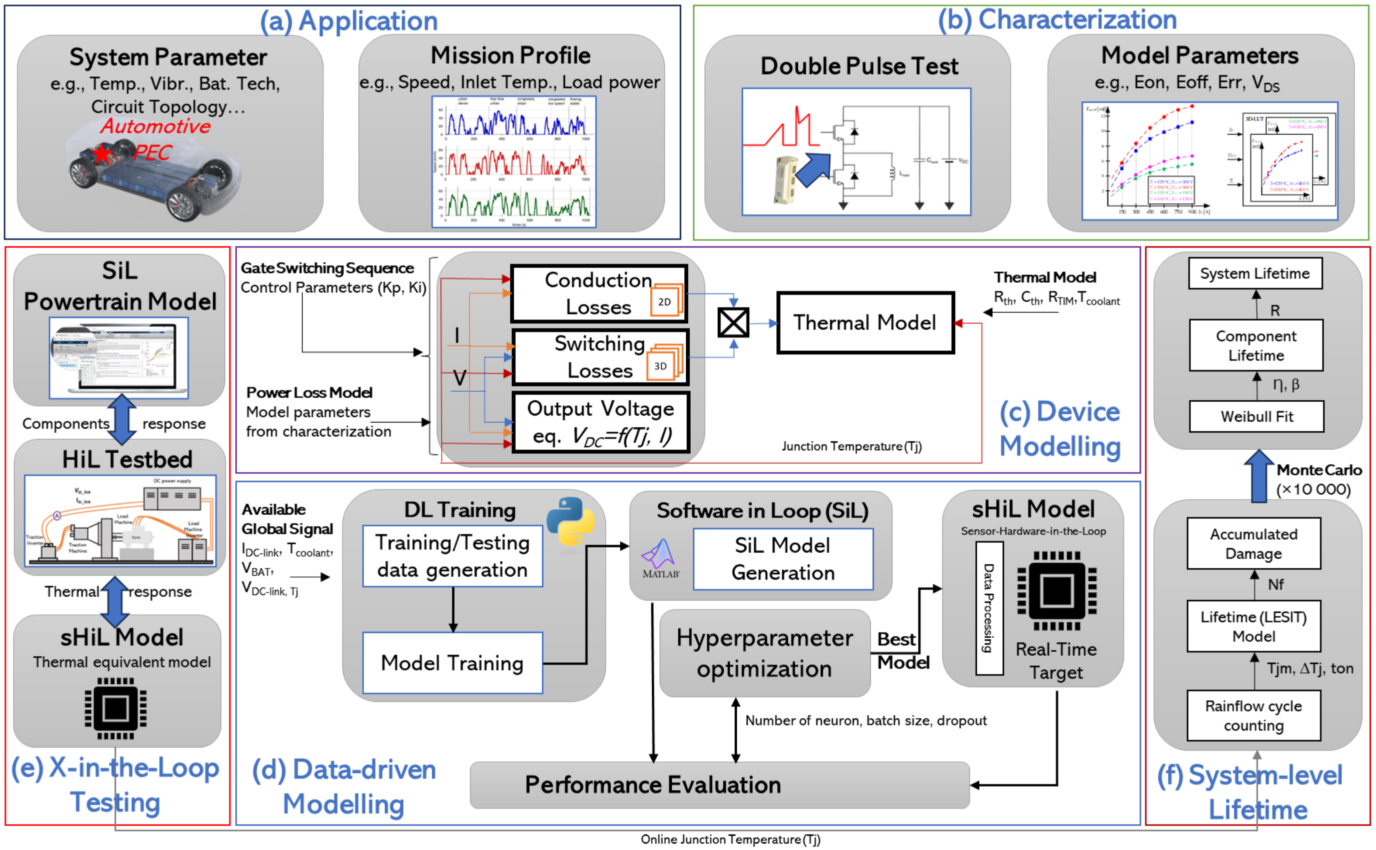


Figure 1. Stepwise concept overview of the proposed data-driven virtual sensing for lifetime estimation of an automotive power electronics converter system: (a) application layer is responsible for providing data regarding vehicle functional loads and mission profile; (b) characterization is responsible for providing accurate parameters for (c) detailed device-level modelling;(d) data-driven modeling executes deep-learning (DL) based temperature estimation and deploys the DL model on an RT processor; (e) XiL illustrates the feasibility of the proposed method in the automotive sector using a frontloading testbed, and (f) System-level lifetime assessment aims to evaluate the lifetime of the PEC.

Furthermore, the harsh operating conditions that automotive PECs may face, such as high ambient temperatures, electrical transients, noise, vibration and mechanical stress, and high road elevations, make it imperative to establish a comprehensive and credible lifetime benchmark when introducing a new component to the existing powertrain, as suggested in references [43]–[45]. As a result, in this paper, the HV DC/DC converter is considered as the device under test (DUT), as shown in Figure 2; however, the proposed methodology can be applicable to all automotive PECs and extendable for stationary PEC applications.

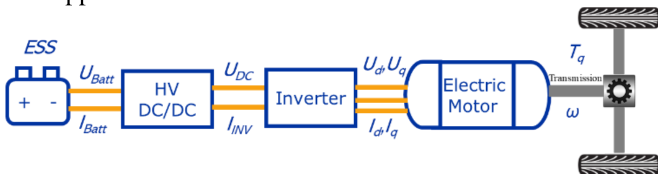


Figure 2. Considered BEV powertrain topology with a bidirectional HV DC/DC converter (device under test)

According to the handbook for robustness validation [46], "*Mission Profile is a representation of all relevant conditions an electrical/electronic module will be exposed to in all of its intended applications throughout its entire life cycle.*"
The main purpose of specifying a mission profile is not just to provide a test description but instead to establish functional boundaries, define boundary parameters, simulation, and modeling approaches, which involves determining how to accurately model both environmental and operational load-based stress factors to assess the total lifetime of a DUT. This paper has applied five dynamic mission profile datasets from an OEM's chassis measurement test bench. These profiles were used to conduct consumption testing of the vehicle, taking into account the new powertrain component, as shown in Table 2.

TABLE 2. KEY PARAMETERS OF THE CONSIDERED BEV MISSION PROFILE.

Speed Profile	Characteristics
Worldwide Harmonized Light Vehicle Test Procedure (WLTC)	Distance= 23.1 km, duration= 1800 s, max speed= 36.47 m/s, average speed= 12.9 m/s
New European Driving Cycle (NEDC)	Distance= 11.03 km, duration= 1180 s, max speed= 33.33 m/s, average speed= 9.33 m/s
Extra-Urban Driving Cycle (EUDC)	Distance= 20.6 km, duration= 4845 s, max speed= 14.58 m/s, average speed= 4.24 m/s
Urban Driving Cycle (UDC)	Distance= 20.3 km, duration= 1500 s, max speed= 23.47 m/s, average speed= 13.55 m/s

Subsequently, the mission profile is translated into device-level loading factors using a map-based analytical forward-type model of the BEV's powertrain. This powertrain model encompasses various components, including the vehicle, gears, Electric Motor (EM) and inverter, bidirectional HV DC/DC converter, and the Energy Storage System (ESS) in the traction

system. The analysis of the vehicle powertrain consumption is conducted based on the targeted mission profile (as in Table 2) under which the vehicle operates. A parameterized EV simulation tool [47] is utilized, where the targeted mission profile is fed as an input into the driver model that generates desired torque and brake commands. The torque command is then directed to the motor model, while the brake command initially enters the vehicle dynamics model. Based on the requested torque demand, the HV DC/DC load current is applied, and supplied by the ESS. Hence, load current request (i_{Load}), battery voltage provided (V_{BAT}), and DC-link voltage reference (V_{DC}) are considered as device-level loading. Typically, a cooling system based on a radiator fan is employed to circulate the inlet coolant and effectively dissipate the heat generated from the powertrain components, i.e., HV DC/DC converter, inverter, and EM. This system works to ensure that the junction temperature of the powertrain converter and EM remain significantly below its maximum temperature, as the mission profile affects the powertrain's coolant temperature primarily due to its impact on heat generation, cooling system efficiency, airflow, and coolant circulation. While higher speeds lead to better cooling due to increased airflow, lower speeds potentially result in higher coolant temperatures due to reduced airflow and lower cooling system efficiency. To that, the inlet coolant temperature (T_{cool}) of the cooling system is also considered as device-level loading.

Based on the device-level loading factors, (b) characterization parameters for the SiC power module have been identified, e.g., DC-link voltage, operating current levels, and temperature. The standard Double Pulse Test (DPT) accurately determines the loss parameters. While the resulting parameters will be used to estimate power losses consecutively Tj and ΔTj, any uncertainties related to the accuracy of the universal loss model during actual operating conditions are considered negligible. Afterward, based on obtained DPT parameters, (c) a universal-loss-based device level modelling can be prepared. The universal loss model separates the conduction and the switching characteristics of the SiC-based semiconductor. It models the switching behavior focusing on power loss estimation within a single simulation step [48]. To accurately calculate power losses and junction temperature, modeling the MOSFET's static and dynamic behavior is vital. An accurate physical model replicates real-world behavior, addressing electricity, heat, and mechanical aspects in loss and temperature calculation. Since the device-level model needs to capture turn-on and turn-off switching events on a μsec scale, the entire simulation takes several hours to simulate a half-hour profile, as mentioned in the above section. Therefore, the highly accurate and considerably fast universal loss-based device model is not suitable for virtual sensing as the response of this type of model is not real-time (RT). Hence, this paper suggests designing a (d) deep-learning-based (DL) virtual sensor to estimate T_j for diode and SiC MOSFET from device-level loading factors mentioned in the application layer. For the RT, the virtual sensor is embedded into a processor that enables power-in-the-loop tests. To validate the applicability of the overall method, a (e) streamlined X-in-the-loop (XiL) test has been executed through a co-simulation between the HiL and PiL test as part of a complete vehicle simulation conducted under real-life conditions. The impact of the virtual sensor on the (f) system-level lifetime estimation concerning the universal loss-based device model is depicted, where a state-of-the-art Scheuermann's lifetime model [51] for system-level lifetime estimation is applied.

III. CHARACTERIZATION AND DEVICE MODELLING

The universal losses model has been developed in this work for modelling the electrical behavior of the semiconductors. In this level of modeling, switching losses are simulated within a singular computational step, which accelerates the simulation speed. This category of models achieves an acceptable accuracy and helps to model the electrical and thermal behavior of the semiconductors without affecting simulation speed. Figure 3 illustrates the characterization testbench and fundamental process of estimating power loss during switching transitions.

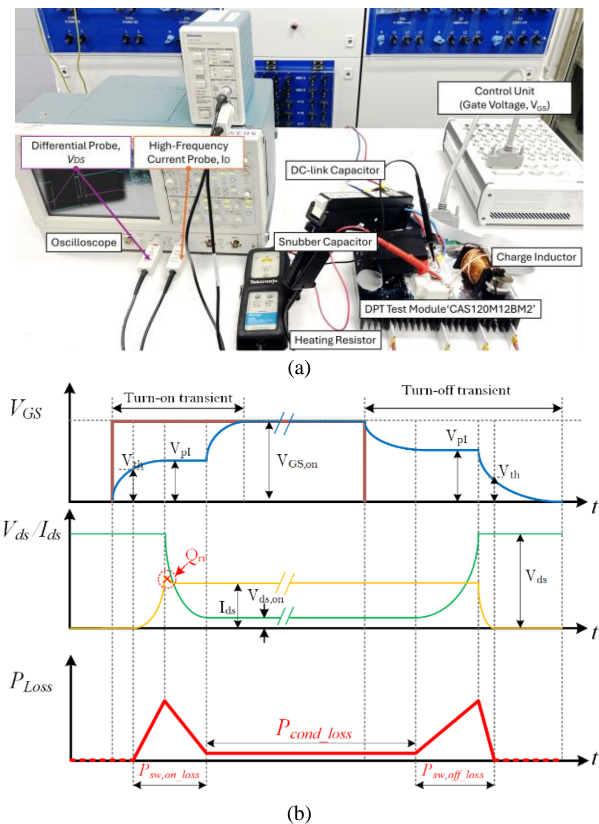


Figure 3. (a) Double pulse test setup, and (b) typical switching waveforms of a SiC MOSFET and gate driver voltage.

Figure 3 depicts the turn-on and turn-off phases, along with the plateau voltage (V_{pl}) and gate-source voltage (V_{th}), which are presented in the gate-source voltage (V_{GS}) waveform. These factors determine how the switch voltage (V_{ds}) and current (I_{ds}) appear during transitions. These dynamic behaviors are closely tied to the underlying principles of semiconductor physics. Subsequently, as the voltage and current coexist during switching transitions, it becomes possible to compute the losses during the switching (i.e., P_{sw,on_loss} and P_{sw,off_loss}). Furthermore, multiplying Ids with the switch on-state voltage ($V_{ds,on}$) makes it feasible to calculate conduction losses (P_{cond_loss}) too.

A. *Standard Double Pulse Test*

Standard Double Pulse Test (DPT) has been utilized to estimate switching loss parameters. The DPT test has been carried out using absolute gate-source voltage and gate resistance values at different voltage levels, current levels, and junction temperature levels to estimate these losses accurately. The results of the DPT are organized into a 3D Look-up table (LuT) comprising three inputs: voltage, current, and the previous junction temperature value. A similar approach is taken to determine the reverse recovery energy of the DUT's body diode. Figure 4 shows the waveforms representing the gate pulse (V_{gs}), drain-source current (I_{ds}), and drain-source voltage (V_{ds}) which are applied to the semiconductor as part of the double-pulse test procedure.

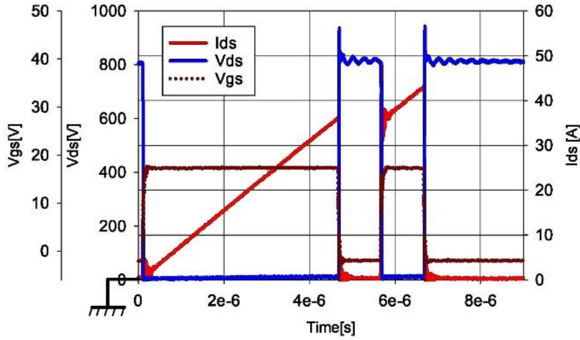


Figure 4. Measured double pulse test waveform at 800 V, 40 A, and 25^{0}C ambient.

This characterization method is employed to analyze the switching characteristics and thermal performance of power semiconductor devices. Several tests have been executed: (a) switching characteristics at different load currents, (b) switching characteristics at different junction temperatures. For switching characteristics at different load currents, the DPT is conducted utilizing two source voltages (V_{DD}), 400 V and 800 V, under three discrete current levels (20 A, 40 A, and 60 A). The experiments have been carried out at ambient temperature condition of 25^{0}C. The variance between the values reported in this study and those outlined in the datasheet is attributed to parasitic capacitance, leading to overshooting during switching transitions. The results are illustrated in Figure 5, where E_{on} and E_{off} correspond to the turn-on energy and turn-off energy, respectively.

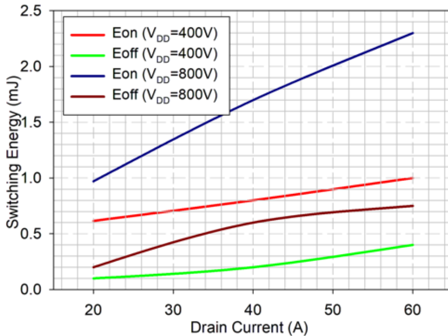


Figure 5. Measured device switching energy loss through DPT: Eon, Eoff dependence on load current and source voltage.

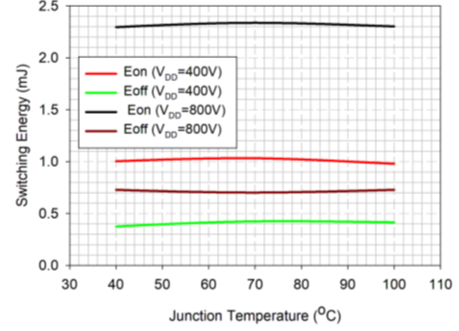


Figure 6. Measured device switching energy loss through DPT: Eon, Eoff dependence on junction temperature at *40 A*.

For switching characteristics at different junction temperatures, the DUT is deliberately heated from 40°C to 100°C in a step of 10°C. This is achieved by applying external heat through heating resistors to the heatsink. Two source voltages (V_{DD}) are utilized, namely 400 V and 800 V, while maintaining a load current of 40 A. Subsequently, switching energy loss (i.e., E_{on} and E_{off}) parameters are precisely derived from the waveforms for the range of temperatures. Figure 6 illustrates the switching losses observed at different junction temperatures and source voltages.

B. *Universal loss Modeling*

The subsequent step entails the universal losses modelling upon obtaining the model parameters. The calculation of the switching losses estimation is given below:

$$P_{sw_loss} = f_{sw} \times \left(E_{on}(T_j) + E_{off}(T_j)\right) \times \frac{2\sqrt{2}}{\pi} \times \frac{I_{RMS}}{I_{Ref}} \times \frac{V_{DD}}{V_{Ref}} \qquad (1)$$

Equation (1) establishes the relationship for the switching losses (P_{sw_loss}), which depends on several parameters. These parameters include the switching frequency (f_{sw}), the turn-on energy (E_{on}), and the turn-off energy (E_{off}) associated with the junction temperature (T_j). These energies are scaled concerning the test load current (I_{Ref}) and the bus voltage (V_{Ref}). Additionally, the DC bus voltage (V_{DD}) and RMS value of switch current (I_{RMS}) play a role in influencing the switching loss magnitude. Notably, V_{DD} corresponds to $V_{BAT,}$ and I_{RMS} corresponds to i_{LOAD} at the system level. As mentioned above, the values for the parameters E_{on}, E_{off}, I_{Ref}, and V_{Ref} have been obtained through the DPT.

Furthermore, the conduction losses of the SiC MOSFET can be calculated as:

$$P_{cond_loss} = R_{ds,on}(T_j) \times I_{RMS}^2 \qquad (2)$$

Equation (2) highlights the three primary factors influencing conduction losses calculation, P_{cond_loss}: (a) the RMS values of the switch current I_{RMS}, (b) the on-resistance of the MOSFETs $R_{ds,\text{on}}$, and (c) the junction temperature Tj. Initially, the RMS value of the switch current for each cycle is determined. Subsequently, the conduction losses are computed by utilizing the product of on-resistance of the MOSFETs and the square of the RMS current, yielding $R_{ds,on} \times I_{RMS}^2$. In addition, the datasheet-driven Foster thermal model is utilized to compute the instantaneous junction temperature, as mentioned in sub-section C. Consequently, the on-state resistance $R_{ds,on}(T_j)$ is adjusted to align with the computed junction temperature. It's

important to note that the gate voltage remains constant at 18V throughout the analysis.

Both conduction and switching losses are estimated concurrently using equations (1)-(2), considering time-based DPT parameters as waveforms directly retrieved from the oscilloscope, and the instantaneous current conducting through the MOSFET or its body diode. These power losses are coupled to the thermal models of the semiconductors and the resulting junction temperatures are fed back again to complete the electro-thermal coupling, being able to achieve a high degree of accuracy with a reduced computational cost.

C. Thermal model

To estimate the junction temperature that is synchronized with the real-time power losses, it is important to incorporate the thermal model for each semiconductor module. The Foster model, which is utilized in this paper, comprises three distinct layers: Layer 1: the junction-to-case thermal impedance ($Z_{th(JC)}$), Layer 2: the case-to-heatsink thermal impedance ($Z_{th(CH)}$), and Layer 3: the heatsink-to-coolant thermal impedance ($Z_{th(HCool)}$). Integration of these components is imperative to attain an accurate understanding of the semiconductor's thermal behavior. The thermal model is represented by (3)-(6) below:

$$T_{jn} = T_{coolant} + \Delta T_{JC} + \Delta T_{CH} + \Delta T_{HCool} \quad (3)$$

$$\Delta T_{HC} = Z_{th(HCool)} \sum P_n \quad (4)$$

$$\Delta T_{SH} = P_n Z_{th(CH)n} \quad (5)$$

$$\Delta T_{JC} = P_n Z_{th(JC)n} \quad (6)$$

Where T_{jn} is the junction temperature of nth MOSFET, $T_{coolant}$ is temperature of coolant unit, ΔT_{JS} is junction to case temperature, ΔT_{CH} is case to heatsink temperature, ΔT_{HCool} is heatsink to coolant temperature. Pn is the power losses of nth MOSFET or diodes.

D. DC-link Voltage Modeling

By conducting DPT testing over a temperature range, as shown in Figure 6, a temperature-dependent DC-link voltage model is obtained that accurately captures temperature effects. This modeling approach is crucial for achieving precise output predictions, particularly in environments with extreme temperatures and for critical output voltage converters. The equation below defines the voltage equation, which varies corresponding to junction temperature and current:

$$V_{MP} = V_{DC} - v_D(T_j, I) \text{ or } V_{MP} = 0 - v_D(T_j, I)$$

The classical definition of the Mid-Point Voltage (V_{MP}), is typically assigned as either 0 V or V_{DC} based on the switching pattern. However, in this paper, V_{MP} is redefined in equation (7) to replicate dependencies on both current and junction temperature. It's worth noting that this critical dependency is often overlooked in many existing electrical simulation tools.

IV. Data-Driven Modelling For Virtual Sensing

This section outlines the method and design technique of data-driven virtual sensing to estimate the junction temperature (T_j) in the SiC-based HV DC/DC converter. Virtual sensing is built upon the available sensor data, and eliminating the need for additional sensors. For this purpose, virtual sensing techniques consider device-level loading factors as input signals, as sensors for these signals are already installed. This initiates a black-box-oriented modeling problem, where a correlation is created between an available set of input data and the desired output data of a dynamical system. The problem of black-box modeling and system identification has been a long-researched topic for PECs. PECs are inherently time-invariant dynamic non-linear systems. Generalized State Space Averaging (GSSA) [49] and Discrete Time Modelling [50] are two popular methods that use mathematical equations to create models. Polytopic is also a popular large-signal modelling paradigm, which uses multiple state-space models at different operating points connected via weighting functions [51]. The equation-based models become very complex and heavy in computational requirements when designing for complex PECs.

Deep learning (DL) based black-box modelling suits the application's need. DL models are easily deployable in low-cost embedded hardware from leading chip manufacturers like Texas Instruments, STMicroelectronics, and single-board computers (SBCs). Much recent work has been done on black box modelling of PECs using DL. The authors in [52] show the development of the Long-Short Term Memory (LSTM) network-based model from the switching model of a buck converter. Furthermore, it compares the result from a developed model with a Feed Forward Artificial Neural Network (FF-ANN). In [53], a Non-Linear Autoregressive Network with Exogenous Input (NARX) is used to model DC/DC buck converters. A comparison between LSTM and NARX has been performed on a 48V-12V bidirectional DC/DC converter used in mild hybrid electric vehicles [54]. The following subsection details the development and comparison of different DL-based models, i.e., FF-ANN, LSTM, and multiple configurations of the NARX network to obtain the most optimal virtual sensor design.

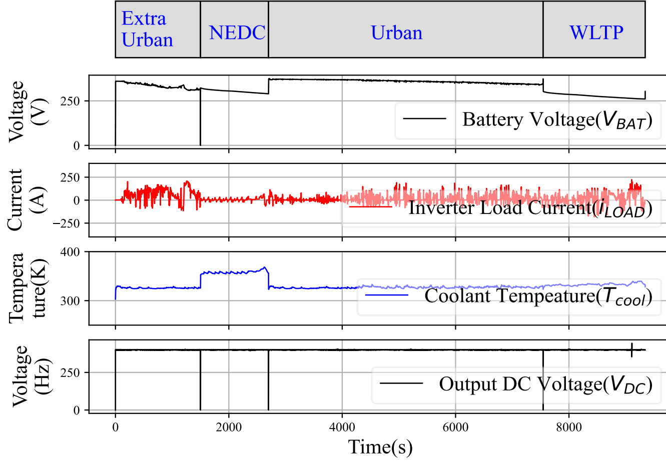
A. Dataset preparation for Deep-Learning (DL) models

The device-level modelling is updated and calibrated using characterization parameters (e.g., Eon, Eoff) retrieved from DPT waveforms. Then, the long-term simulation data are obtained using device-level modelling, where the accurate electro-thermal model of the DC/DC converter is used to estimate losses, Tj and ΔTj concerning the mission profile. Afterward, the datasets from the device model are fed as input for DL model development. As mentioned above, the device-level model is simulated for four dynamic standard driving cycles to generate enough data to capture the dynamics of the simulation model.

TABLE 3. TRAINING-TESTING DATASET FROM SIMULATION OUTPUT BASED ON SIMULATED DRIVING CYCLES

Training Dataset	Testing Dataset	Configuration
EUDC, NEDC	UDC, WLTP	Config-1
EUDC, UDC	WLTP, NEDC	Config-2
EUDC, WLTP	UDC, NEDC	Config-3
NEDC, UDC	WLTP, EUDC	Config-4
NEDC, WLTP	UDC, EUDC	Config-5
UDC, WLTP	NEDC, EUDC	Config-6
Number of different models: 5		*Σ30 Variants*

Figure 7 shows the developed simulation data plots. The data and its nomenclature are also shown.



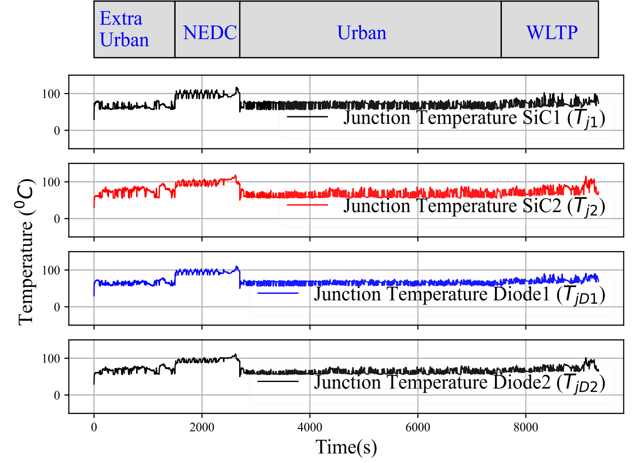


Figure 7. Device-level model simulation output used for the development of deep learning model. Model inputs are: V_{BAT}, i_{Load}, $T_{coolant}$, and V_{DC} (Left) and Model Outputs are: $T_{j1}, T_{j2}, T_{jD1}, T_{jD2}$ (Right) for Extra Urban, NEDC, Urban, and WLTP cycles (Only one leg of the inverter is used in the illustration).

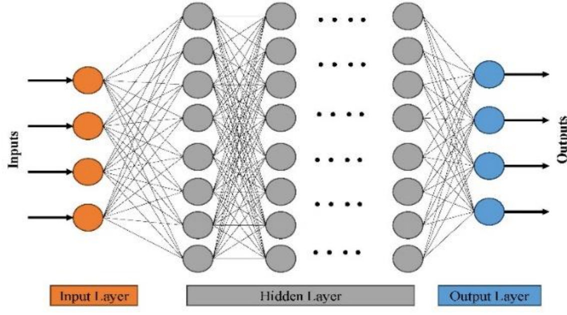


Figure 8: Structure of a FF-ANN model.

The left plot shows the input and the right plot shows the output T_j from the simulation model. A crucial optimization choice in DL model design involves dataset selection for training and testing purposes. In this context, two cycles are allocated for training, and the other two cycles are used for testing. Six training-testing configurations are employed using five different models; thus, 30 variants are used to identify the optimal model. The driving cycle variants are listed in Table 3.

B. *Modelling context*

Multiple DL models are explored to find the most suitable model for T_j estimation. Along with complex DL models, a simpler linear regression model is also evaluated to compare the performance of the different DL models.

a. *Feed-Forward Artificial Neural Network (FF-ANN)*

The FF-ANN is the most conventional and straightforward neural network. The basic application of FF-ANN is to find a non-linear correlation between inputs and outputs by passing the input through a series of calculation layers. Figure 8 shows the three distinct layer structs of FF-ANN, viz., input Layer, output layer, and hidden layers. The output of each layer can be expressed in the following equation.

$$y = \gamma(w^T x + b) \tag{7}$$

Where γ is the activation function, which introduces a non-linearity to the FF-ANN output, w is the weight matrix, x is the input vector, and y is the output vector. A piecewise linear function called the Rectified linear activation function (ReLU) is used for training and comparison purposes.

$$\gamma(x) = max\ (0, x) \tag{8}$$

The FF-ANN training aims to reduce the error between predicted output (y_p) and true output (y) by changing the w and b matrix. The root Mean Square Error (RMSE) method is used to evaluate the loss function for optimization, which is defined as equation 9.

$$RMSE = \sqrt{\frac{1}{m}\sum_{1}^{m}\left(y_i - y_{pi}\right)^2} \tag{9}$$

The unavailability of the memory block in the FF-ANN limits its capability to learn time-dependent patterns and capture short/long dependencies, restricting it's applicability to the modelling of dynamic systems [55].

b. *LSTM based RNN*

Recurrent Neural Network (RNN) can solve the limitation posed by FF-ANN by storing and passing the state of a neuron to the next step in the computation while processing sequential data. The structure of an LSTM unit is shown in Figure 9, which learns both the short-term and long-term dependencies of sequential data. The x_t is the input vector, c_t is the cell state storing long-term dependencies, and h_t is the hidden state storing short-term dependencies at time step t. It should be noted that the cell state does not pass through any of the fully connected layers and is updated through each time step. There are four gates (fully connected layers) viz. forget gate (f_t), input gate $(i_t\ and\ \hat{c}_t)$, and output gate (o_t). The working of LSTM can be divided into three main parts. The forget gate discards a few features and keeps the rest of the features from the cell state, using the sigmoid function, whose output is from 0-1, implying the importance of features in the cell state [56]. The $\hat{c}_t$ adds or subtracts to the cell state, using the tanh function, whose output varies from -1 to 1. An additional gate (i_t) similar to (f_t) is used so that $\hat{c}_t$ only adds relevant features to

cell state (c_{t-1}). The h_t gets updated from h_{t-1} by passing it through o_t and a tanh function on the c_t [56].
The equations for the LSTM unit are given below

$$f_t = \sigma\left(W_f \cdot [h_{t-1}, x_t] + b_f\right) \quad (10)$$

$$i_t = \sigma(W_i . [h_{t-1}, x_t] + b_i) \quad (11)$$

$$\hat{c}_t = tanh(W_c . [h_{t-1}, x_t] + b_c) \quad (12)$$

$$c_t = f_t . c_{t-1} + i_t . \hat{c}_t \quad (13)$$

$$o_t = \sigma(W_o . [h_{t-1}, x_t] + b_o) \quad (14)$$

$$h_t = o_t . tanh\ (c_t) \quad (15)$$

Where W_f, W_i, W_c, W_o are weight matrices and b_f, b_i, b_c, b_o are bias vectors for the fully connected layers [57].

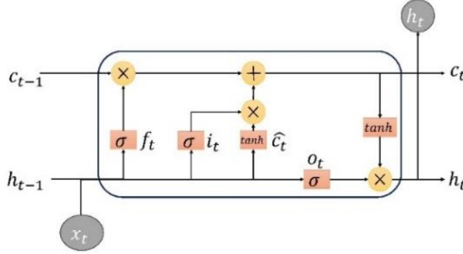


Figure 9: Structure of an LSTM unit, each gate $f_t, i_t, \hat{c}_t, o_t$ is fully connected layers with activation function σ = sigmoid function, tanh = hyperbolic tangent function, ⊕: element-wise addition, ⊗: element-wise multiplication.

c. NARX with FF-ANN and LSTM-ANN

The NARX is a recurrent neural network that uses a specific number of past input ($[x_n, x_{n-1}, x_{n-2}, x_{n-3} \dots x_{n-k}]$) and a specific number of past outputs ($[y_{n-1}, \ y_{n-2}, y_{n-3} \cdots y_{n-m}]$) for the prediction of the current output (y_n) [58]. The output of the NARX can be written by:

$$y_n = f(y_{n-1}, y_{n-2}, \dots y_{n-m}, x_n, x_{n-1}, x_{n-2}, \dots, x_{n-k}) \quad (16)$$

$$y_n = f(\hat{y}_{n-1}, \hat{y}_{n-2}, \dots \hat{y}_{n-m}, x_n, x_{n-1}, x_{n-2}, \dots, x_{n-k}) \quad (17)$$

Here y is the actual network input and $\hat{y}$ is the input from a training data set of output. Based on the equation two different NARX architectures can be created which are shown in Figure 10 and Figure 11.

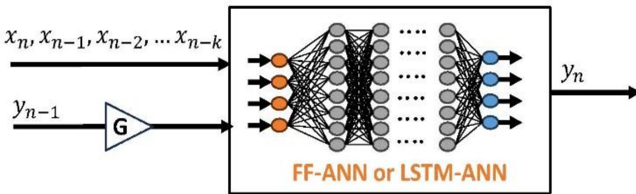


Figure 10: Series-Parallel architecture, only 1 delayed output is used in the paper with G=0.3

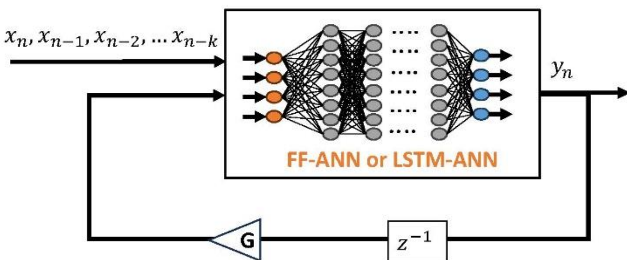


Figure 11: Parallel architecture, only 1 delayed output is used in the paper with G=0.3

The series-parallel architecture is used for training the NARX model while the parallel architecture is used for deployment of the NARX model. A particular issue that was found during deployment of NARX is that an initial condition is required on the x and y during the start of the model, as initial past values of x, y, are not available during a real-time deployment. This led to the parameter G optimization, which was found that a higher value of G (> 0.5) makes the NARX model unstable during the deployment leading to an output very different from training outputs. An optimal value of *G=0.3* is chosen. The value of 0.3 is chosen based on trial and error for stable deployment output. The training is done to find the function f in equation (7) and (8). Two types of ANN are used to estimate the function f, viz FF-ANN and LSTM-based RNN. The former one is referred to as only NARX and the latter one is referred to as NARX-LSTM in the later sections of articles.

Four different models, namely FF-ANN, LSTM-RNN, NARX, and NARX-LSTM, are trained using the simulation dataset. To provide a comprehensive overview of the research findings, a linear regression is also tested using the same input and output variables, and the results have been compared with the listed four deep learning models. These results are elaborated upon in the following subsections.

C. Model training and DL model generation

The models are trained in Python using sci-kit-learn [59] for linear regression and TensorFlow [60] for DL models. The methodology of the parameter estimation for model evaluation, dataset preparation, training the deep learning (DL) models, and performance evaluation is shown in Figure 12. The datasets for training and testing the DL models are generated within a Python environment by simulating the universal loss-based device-level model for the specified mission profiles given in Table 2. The DL model is initialized, trained, and then transferred to MATLAB for evaluation. This is an important step, as NARX models could be evaluated in a parallel architecture with zero initial conditions, resembling real-life deployment.

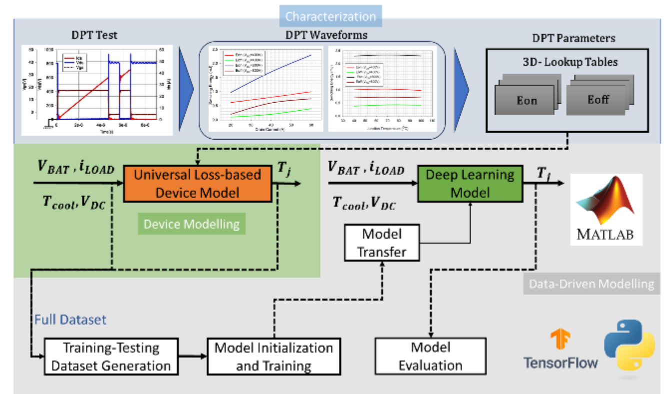


Figure 12: DL model generation methodology: the accurate universal loss model (i.e., Device Modelling) is used to generate a full training dataset, incorporating DPT characterization data (Eon, Eoff). The obtained full training dataset is used for deep learning model training and validation using Python and MATLAB.

To have a homogeneity between the DL models, DL models are configured as follows:

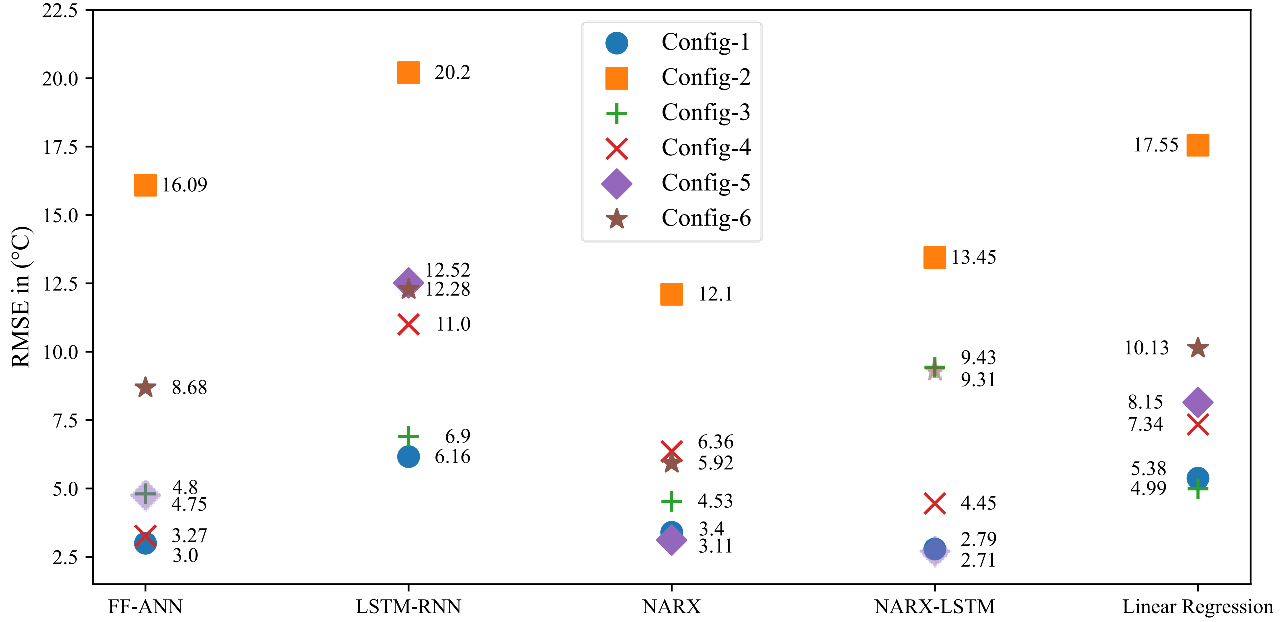


Figure 13: RMSE comparison on the test data of all the trained models with respect to all training-testing datasets (Refer to Table 3.), the most accurate model is NARX-LSTM with RMSE on the test data 2.67 trained on 'WLTP' and 'NEDC' cycle. The second best model is NARX-LSTM (RMSE 2.79) trained on 'EUDC' and 'NEDC'.

i. FF-ANNs: Input Layer – Hidden Layer (4 fully connected layers with 256 neurons) – Output Layer
ii. LSTM-RNNs: Input Layer, - Hidden Layer (2 LSTM Layers with 256 units, 2 fully connected layers with 256 neurons) – output layer
iii. NARXs: FF-ANN with inputs $(x_n, x_{n-1,} x_{n-2}, .. x_{n-10})$ and one sample delay from output with a gain of 0.3.
iv. NARX-LSTMs: LSTM-RNN with inputs $(x_n, x_{n-1,} x_{n-2}, .. x_{n-10})$ and one sample delay from output with a gain of 0.3.

Comparative results of the 35 variants in terms of accuracy are depicted in Figure 13 and it shows the RMSE on the test data concerning the trained model. As observed from Table 4, Config-5 (Training data: NEDC and WLTP cycle) and Config-1 (Training Data: EUDC and NEDC cycle), which employ the NARX-LSTM model, outperform the rest of the 33 variants.

TABLE 4. BEST MODELS FROM MODEL SELECTION TRAINING.

Model ID	Test data: RMSE	Full data: RMSE	Training Data
NARX-LSTM, Model-I	2.71	2.3	Config-5
NARX-LSTM, Model-II	2.78	2.39	Config-1

D. DL model optimization

The model presented in Table 4 needs further optimization for final testing and deployment in HiL scenarios. The key objective of this optimization is to avoid overfitting the DL models during the training phase. Overfitting happens when the model learns excessively from the training data, leading to poor performance on the validation and/or testing data [61]. Overfitting becomes evident during training when the training loss decreases with each iteration (epoch), while the validation loss does not exhibit a corresponding decrease with each epoch. To solve the issue with overfitting and to find an accurate DL model a grid search is performed by doing the following variation in the model configuration.

i. *Number of neurons on each layer:* The variation matrix is [16, 32, 64, 128, 256].
ii. *Drop-out layer configuration:* The dropout parameter is the percentage of neurons randomly dropped out from LSTM layers to control overfitting. The variation matrix is [0.1, 0.2, 0.3].
iii. *Batch size:* Batch size is a training parameter, which indicates the number of samples the training algorithm takes at a time and propagates through the network to train the model. The variation matrix is [8, 16].

TABLE 5. BEST PERFORMED DL MODEL STRUCTURE.

Model ID	Neurons-Batch size - dropout	RMSE			Execution Time (ms)
		Training Data	Testing Data	Full Data	
Model-I	256-16-0 Original Model	0.98	2.71	2.3	193
	16-16-0.2	3.32	2.7	2.91	1.9
	16-16-0.1	2.66	2.74	2.71	1.9
	32-8-0.3	4.72	2.9	3.58	4.8
Model-II	256-16-0 Original Model	0.86	2.78	2.39	192
	256-16-0.2	1.31	2.59	2.29	323
	128-16-0.2	1.53	2.61	2.35	63
	32-16-0.1	2.75	2.64	2.67	4.8

A total of 30 unique combinations are prepared corresponding to Model-I and Model-II using the variables mentioned above. In total, 60 models are prepared to obtain the optimal deployment model. Table 5, depicts the performance of the original model from Table 4 and the 3 best-performing structures out of the 30 models. It can be observed from Table 5 that for Model-1, the original model with 256 neurons, a batch size of 16, and no dropout layer configuration, outperforms the

other 30 configurations. In the best configuration for Model-I, RMSE values of 0.98, 2.71, and 2.3 are obtained for the training data, testing data, and the full dataset, respectively. For Model-II, which has a configuration of 256 neurons, a batch size of 16, and a 0.2 dropout layer, the best RMSE values of 1.31, 2.59, and 2.29 are achieved for the training data, testing data, and the full dataset, respectively. Execution time is a key parameter for the selection of the final model, for deployment and testing. The execution time is also shown in Table 5. The execution time given in the table is the time required for the model for single inference on a dSPACE MicroLabBox, using a 32-bit NXP processor. The sampling rate of junction temperature sensing is 100 ms, so the best model with real-time capability is Model-II with 128 neurons, with a 20% dropout rate and trained with a 16 batch size. The training results on EUDC and NEDC are shown in Figure 15. The junction temperature comparison between the training data and predicted data for 2 MOSFETs and 2 diodes is given in Figure 15. The RMSE between the true value and predicted value is 1.26°C, 1.66°C, 1.45°C, 1.97°C for $T_{jD1}, T_{j1}, T_{jD2}, T_{j2}$ respectively.

V. X-in-the-Loop Testing

To validate the feasibility of the proposed method, three distinct test environments have been streamlined following the standard V-scheme and ISO 26262 X-in-the-Loop (XiL) methodology [62]. These include (a) Software-in-the-Loop (SiL), (b) Sensor-Hardware-in-the-Loop (sHiL), and (d) Hardware-in-the-Loop (HiL), as shown in Figure 14. The XiL tests were performed for standard Urban and WLTP driving cycles which represent one complete lap of the OEM's dynamic track with highly varying slopes and altitudes. As part of the SiL, a map-based forward-facing powertrain dynamic model, 1D powertrain thermal model, vehicle control unit (VCU) model, and driver model are being utilized in MATLAB 2019b environment.

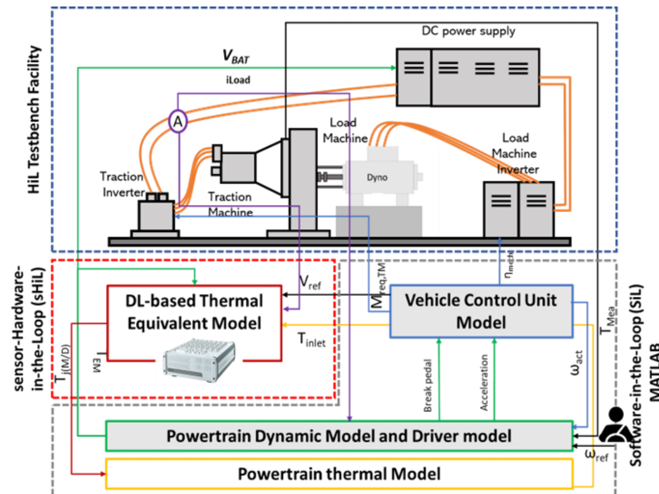


Figure 14. A detailed schematic overview of the XiL test execution: (a) SiL: the software model of the powertrain and the thermal simulator MATLAB model are considered (shown as a gray dashed box), (b) sHiL: the dSPACE MicroLabBox is utilized as the virtual sensor for the DUT (shown as a red dashed box), and the HiL test bench facility is shown as a blue dashed box.

On one hand, the SiL is responsible for generating several signals for sHiL and HiL, i.e., DC-link voltage (V_{DC}), battery pack voltage (V_{BAT}), inlet coolant temperature (T_{cool}), torque request ($M_{req, TM}$) and base speed (η_{mech}). On the other hand, SiL also receives several output signals from the sHiL and HiL, notably the Junction temperature of DUT's MOSFET and diode ($T_{J(M/D)}$), actual torque (T_{Mea}) and load current (i_{Load}).

The sHiL is embedded into the dSPACE MicroLabBox, which computes the DL-based thermal response of the DUT for targeted mission profiles, and automotive OEMs prefer to use dSPACE MicroLabBox as a VVE prototype. sHiL is configured based on the I/O of the DL model. Input signals are: DC-link voltage (V_{DC}), battery pack voltage (V_{BAT}), inlet coolant temperature (T_{cool}), and load current (i_{Load}), whereas the output is Junction temperature of DUT's MOSFET and diode ($T_{J(M/D)}$).

The HiL frontloading testbench comprises a back-to-back motor-inverter setup and both inverters are powered via a DC power supply. The communication between SiL, sHiL, and HiL has been established using EtherCAT.

The main challenge in this paper is to deploy the DL-based equivalent thermal model onto the hardware. The dSPACE MicroLabBox is being utilized for hardware deployment, thanks to its high computational power combined with very low I/O latencies, which provide excellent real-time performance [62]. Checking for real-time compatibility is one of the fundamental processes. The main characteristic is to determine whether the model is capable of actually running in real-time on the simulator.

The workflow of the RT test is carried out as follows: First, the DL-based equivalent thermal model is created and checked so that no errors are seen in the offline simulation (MATLAB). Afterward, the sHiL is programmed in dSPACE through the MATLAB/Simulink interface, which is capable of deploying the deep learning model into the RT platform. Finally, the input data to dSPACE is passed and the output of the model is received through Ethernet communication.

For analyzing the correct real-time execution of the different models, three task information are considered: (a) Task Call Counter, (b) Task Turnaround Time, and (c) Overrun Count. The real-time (RT) model in dSPACE is executed at fixed discrete points with Ts = 100 ms. The maximum task Turnaround Time Measurement indicates a maximum task turnaround time of 63 ms for a periodic task of 100 ms. The Overrun Count Measurement shows that the overrun count value is null, signifying that the timing performance is acceptable. The computational effort shows that the performance of the DL model is satisfactory, with no task turnarounds or overruns occurring during the execution of the RT block. Both compilation and performance stages are carried out successfully. In conclusion, it can be stated that the DL-based thermal model is capable of running on an RT platform without any issues.

VI. Results and Discussions

The accuracy of the universal loss-based device-level modelling is confirmed through validation using a 30 kW interleaved DC/DC converter prototype test bench equipped with all SiC power modules.

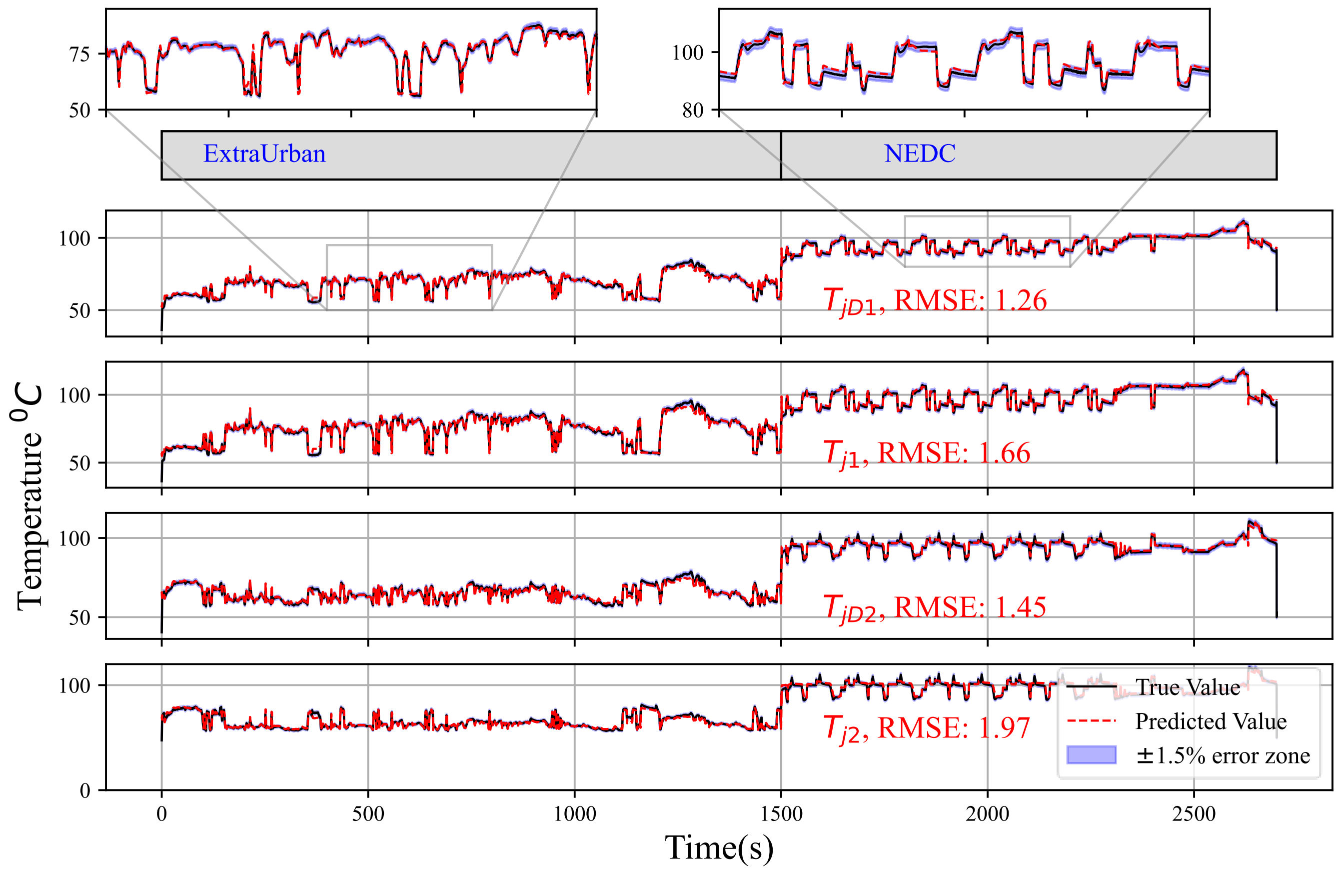


Figure 15: Predicted Junction temperature via Model-II (128-16-0.2) on training data, where the temperatures are depicted for a SiC half-bridge power module's Diodes and MOSFETs, and all predicted values remained within ±1.5% error zone.

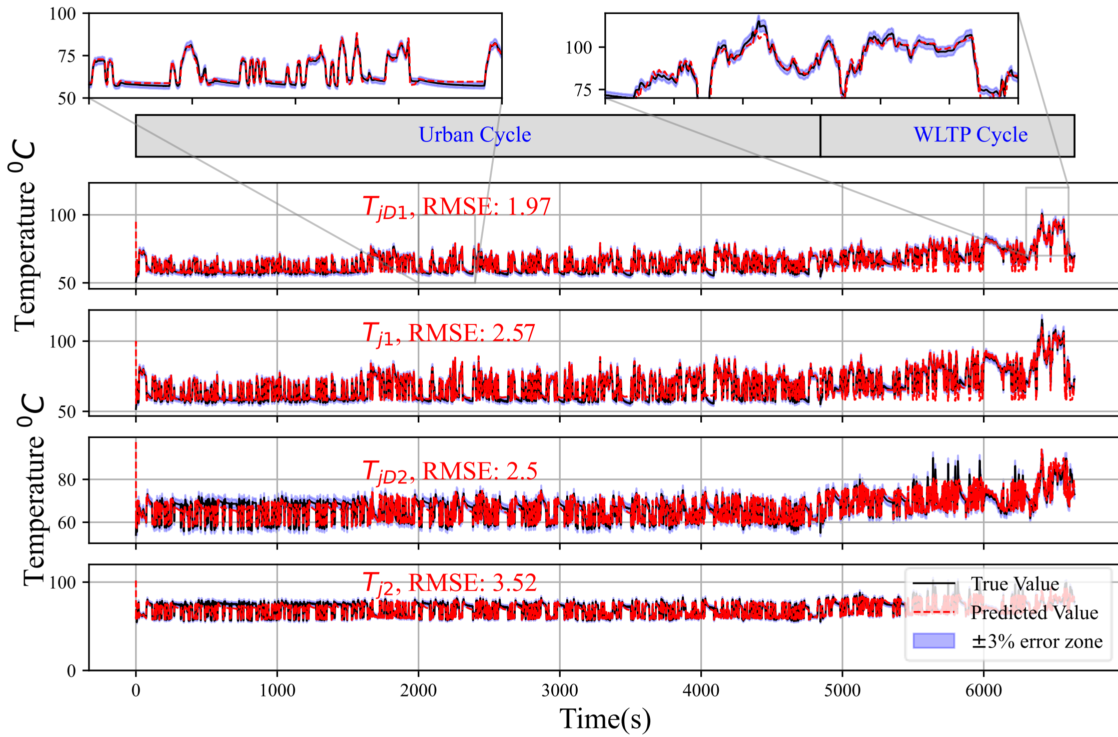


Figure 16: Result of HiL testing of Model-II (128-16-0.2) on unknown testing data (i.e., Urban and WLTP), where the predicted Junction temperature values of the Diodes and MOSFETs remained within ±1.5% error. The RMSE in MOSFET1, MOSFET2, Diode 1, and Diode 2 is respectively 2.57, 3.52, 1.97, and 2.5.

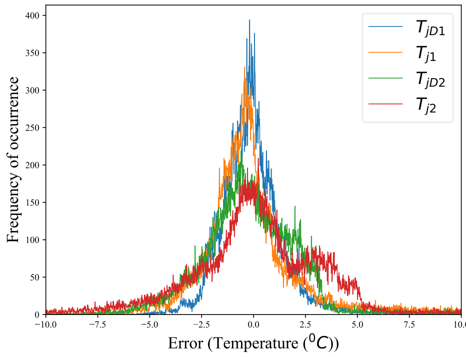


Figure 17: Error distribution plot for each temperature prediction during HiL testing.

DPT parameters are inputted into the universal loss model to estimate converter efficiency and junction temperature responses, imposing the validation of the device-level modelling. The accuracy of the device-level modelling is pivotal as the data it generates is utilized for training DL models. The specification of the converter testbench is depicted in Table 6.

The validation of the device-level model for the DC/DC converter has been carried out across load variations ranging from 10% to 100%, covering both buck and boost modes of operation. Figure 18 depicts the experimental test bench for the 30 kW DC/DC converter prototype.

TABLE 6. SPECIFICATION OF THE 30 KW ALL SIC HV DC/DC CONVERTER PROTOTYPE.

Converter Parameters	Values
Interleaved phases	3
Semiconductor power module	SiC: CAS120M12BM2
Phase Inductance	~175 µH
Inductor Core material	AMCC50 Metglas
DC-link Capacitance	~160 µF
Switching frequency *[fsw]*	55 kHz
Battery emulator as input	*Digatron: 1000V, 2×80 kW*
Dynamic resistive load	*3.3 kW to 30 kW*

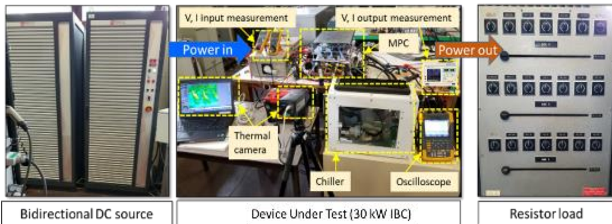


Figure 18. The experimental setup consists of a 30 kW bidirectional DC/DC converter prototype with all SiC components. Power is supplied by the Digatron EVT module (1000V, 2×80kW), and liquid-cooling thermal management is facilitated by a chiller. Thermal distribution is monitored using a FLIR thermal camera, while efficiency measurements are conducted with a YOKOGAWA WT1804E power analyzer, and load changes using a dynamic load matrix.

A. *Experimental Verification of the Device-Level Model*

Figure 19 presents a comparison of efficiencies between the measurement and device modeling at different load powers. The measurements have been conducted using a highly precise power analyzer, i.e., Yokogawa WT1804E (with a power accuracy of 0.02%). A high goodness of fit is achieved between the device model and measurements, confirming the accuracy of the model. The highest mean percentage error (MPE) is only 0.40%, and a deviation of 20 W occurs at maximum load.

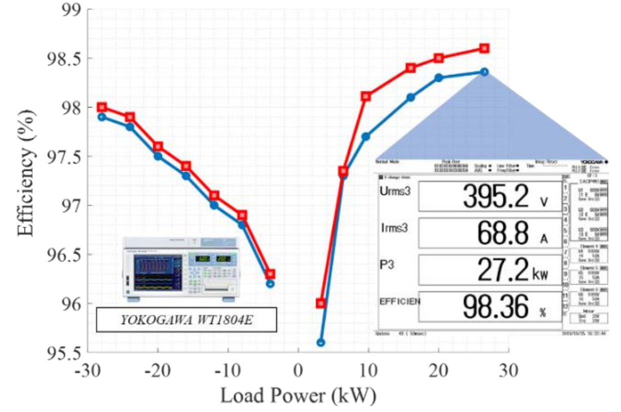


Figure 19. Comparative efficiency between RT measurement (blue curve) and device model estimation (red curves). The efficiency characteristics of the HV DC/DC converter are measured as follows: in Buck mode (negative current region), with V_{in} = 395 V, V_o = 200 V, and f_{sw} = 60 kHz. The test is conducted at different load power levels ranging from 3.6 kW to 26 kW, and in Boost mode (positive current region), with V_{in} = 220 V, V_o = 395 V, and f_{sw} = 60 kHz, the test is carried out at various load power levels ranging from 3.6 kW to 27.2 kW. The obtained efficiency at max load is shown during boost mode operation.

B. *Verification of the proposed methodology in HiL testbench*

The result of the HiL testing of the best-designed model is shown in Figure 16. The training data are almost half the size and unknown testing data. The model is seen to be able to capture the dynamic behavioral pattern and successfully make the prediction on unseen Urban and WLTP data during HiL testing. Figure 16 shows the real-time predicted junction temperature data and its comparison to device-level model true value, for two SiC MOSFETs and two Diodes. The RMSE between the true value and the predicted value is 1.97°C, 2.57°C, 2.5°C, 3.52°C for $T_{jD1}, T_{j1}, T_{jD2}, T_{j2}$ respectively.

Figure 17 also shows the error distribution for four different temperatures. The model performance is better with Urban than with WLTP data. The RMSE on Urban is 2.2°C, while with WLTP data is 3.72°C. The decrease in the performance of the model WLTP data occurs during highly dynamic and step change areas, as seen in Figure 16.

C. *Performance of the proposed methodology in Lifetime estimation*

To evaluate the performance of the proposed methodology LESIT parameters-based state-of-the-art Scheuermann's lifetime model is being utilized. For the lifetime estimation of the SiC power module, the state-of-the-art mission-profile-oriented lifetime assessment tool is used. In addition, not only package-related wear-outs are considered but also the intrinsic effect of dielectric breakdown of the SiC power module is considered, and detailed equations and parameters are referred to [18].

Based on the Junction temperature profile from XiL testbench using a DL-based thermal model and universal loss-based model, as depicted in Figure 15, the corresponding number of cycles and accumulated lifetime of the individual components for the subjected mission profiles are calculated using a rainflow cycle counting algorithm.

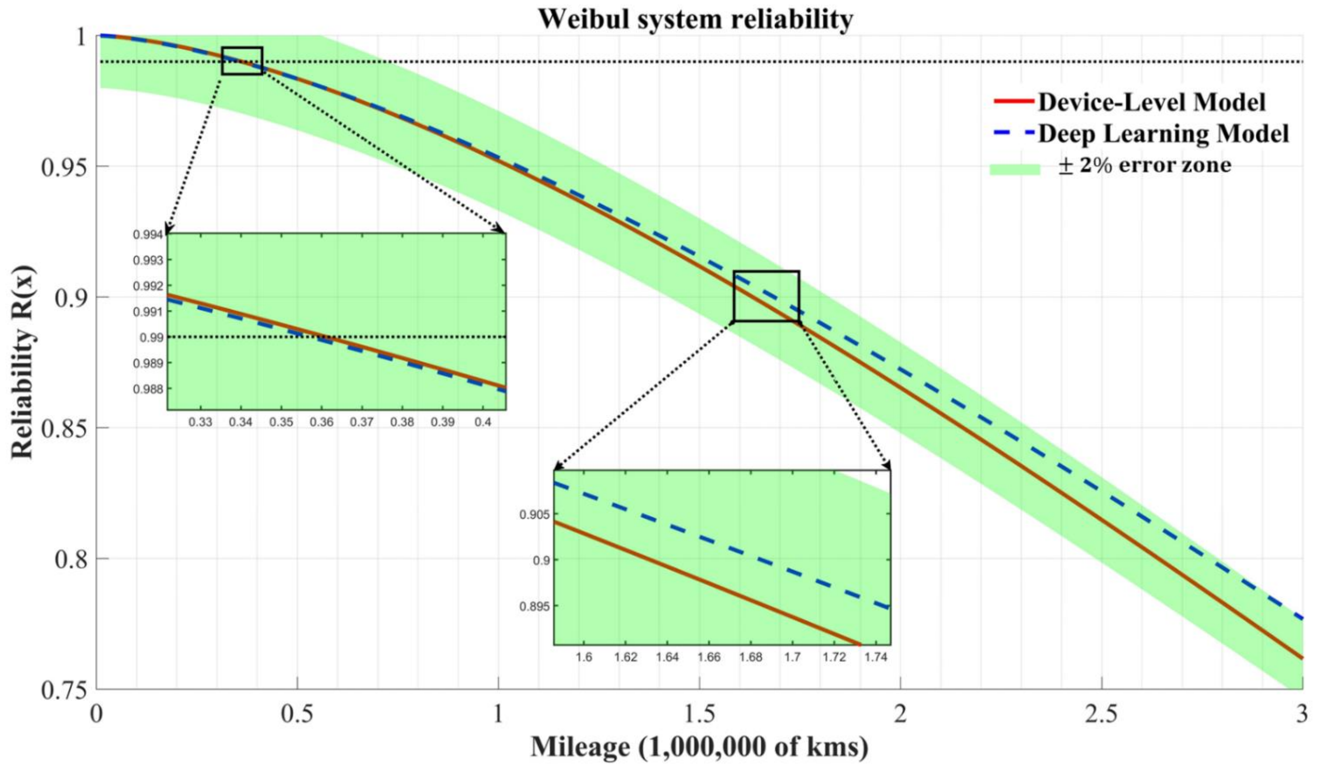


Figure 20. Weibull system reliability calculation using both device-level model (red color) and DL-based model (dotted blue color) for the DUT (i.e., HV DC/DC) while considering Urban and WLTP mission profiles, where only series combination of MOSFETs and Diodes is taken into consideration $R(sys) = RD_1{}^3.RM_1{}^3.RD_2{}^3.RM_2{}^3$. A zoomed-in view of the reliability percentiles at 99% and 90% is provided, and a 2% error zone is marked to observe the response up to the 75% reliability percentile. And both lifetime models have been developed using state-of-the-art Scheuermann's lifetime model and LESIT parameters [18].

For a more realistic estimation, uncertainties in the lifetime parameters of the SiC power module have been introduced using Monte Carlo simulations. Afterward, the system-level lifetime and reliability percentile of the PE converter are estimated concerning mileage using the Weibull function. In automotive applications, a high probability of failure, i.e., a 90% reliability percentile, is not realistic, and the more interesting point is expected high-reliability rates in the parts per million (ppm) range—specifically, the 99% reliability level. Therefore, in this paper, the accuracy of reliability percentiles at 99% and 90% between the DL-based model and the device-level model is investigated. In both cases, the relative percentage error is 0.35% and 1.52%, and the error does not exceed 2% until the reliability percentile reaches 75%, as shown in Figure 20. Based on the obtained results, it can be concluded that using the RT DL model allows for the estimation of system-level reliability with a high degree of accuracy, especially when compared to a physics-based loss model.

VII. CONCLUSION

This paper introduces and validates an optimal deep-learning-based thermal equivalent modelling approach for an automotive power electronics converter, designed to estimate the junction temperature and junction temperature swings of MOSFETs and diodes. The main findings and limitations of this study are presented here:

a. The characterization test of a SiC module is depicted, which retrieve key power loss parameters and enables a highly accurate and fast mission profile-oriented long-term electro-thermal simulation model having an MPE of 0.40% and a maximum deviation of 20W.

b. A highly accurate virtual sensor is proposed which achieves a maximum RMSE of 2.57 for MOSFETs Tj and 1.97 for diodes Tj when applied to two entirely unknown profiles (Urban and WLTP), using only existing sensor data. This virtual sensor is both scalable and adaptable for use with any automotive power electronics converter.

c. A computationally efficient virtual sensor model is deployed in an RT hardware, i.e., dSPACE MicroLabBox and it is replicable as a VVE. It provides automotive OEMs with RT thermal monitoring of drive systems and reduces costs through eliminating physical sensors in the drives.

d. High accuracy is maintained up to crucial reliability points, specifically up to the 90% reliability percentile, where the relative error is found to be 1.52% compared to the highly computational demanding Physics-based degradation model. Hence, this highly accurate RT virtual sensor is capable of maintaining a high level of safety and reliability for mission-critical PE systems, especially in harsh operation conditions and during end-of-life management.

e. Following exhaustive XiL validation, it is evident that all functionalities of the virtual sensor align with its design description and they are valid. The heterogeneous co-simulation stages, including SiL (Software-in-the-Loop), sHiL (sensor-hardware-in-the-loop), and HiL

(Hardware-in-the-Loop), are successfully executed. This streamlined strategy can further benefit automotive OEMs through a reduction in real testing efforts.

This study also has some limitations and future aims, which are:

- The parameters of the switch, e.g., R_{dson}, may drift during operation. Consequently, the device-level model parameters may change over time. However, this paper does not discuss the requirement to update both the device-level model and the DL model as these parameters change;
- The data collected from sensors may experience malfunctions, leading to values that do not align with the training data. This study does not include testing or analysis of sensor malfunctions. Also, continuous learning is not investigated with new data that are acquired during operation by the sensors.

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