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An Analysis of the PLLs With Secondary Control Path

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***Abstract*—The phase-locked loops (PLLs) are widely used in different areas of applications particularly for synchronization and control purposes in grid connected applications. A major challenge associated with the PLLs is how to improve their dynamic performance without jeopardizing their stability and filtering capability. Recently, some approaches based on adding a secondary control path (SCP) to the PLL structure have been proposed to deal with this challenge. The objective of this paper is to briefly analyze these approaches. The study starts with an overview of the PLLs with SCP. The paper proceeds with the small-signal modeling of some of these PLLs, which significantly simplifies the analysis. Using these models, the effects of adding the SCP on the PLL structure are studied. The obtained results show that the SCP may not be a practical approach to improve the PLL dynamic performance mainly because it aggravates the stability problem.**

***Index Terms*—Dynamic performance, phase locked loop (PLL), synchronization.**

I. Introduction

GENERALLY speaking, a PLL is a closed-loop feedback control system which synchronizes its output signal in frequency as well as in phase with an input signal [1]. The phase detector (PD), the loop filter (LF), and the voltage controlled oscillator (VCO) are the main building blocks of a typical PLL [2].

A major challenge associated with the PLLs is how to improve their dynamic performance without jeopardizing their stability and filtering capability. To overcome this challenge, several approaches have been proposed in literature, which are reviewed in the following.

To provide a fast dynamic response and, at the same time, to achieve a high disturbance rejection capability, Freijedo *et al.* [3] suggest to add one or more lead compensators in cascade with the LF in the forward path of the PLL. The suggested lead compensators are second order and have pairs of purely imaginary poles and zeros. So, they provide the selective cancellation like a notch filter without lagging the loop below -180° (stability limit). Thus, the PLL can achieve a high bandwidth (a fast dynamic response) without jeopardizing the stability and the filtering capability.

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To improve the PLL dynamic performance during the startup and phase jumps without degrading its filtering capability, an effective method based on adaptive adjustment of the gain of the frequency estimation loop is suggested by Karimi Ghartemani *et al.* [4]. This approach has a general form and can be applied to a wide variety of three-phase and single-phase PLLs.

To provide a fast phase angle re-tracking during the transients, Thacker *et al.* [5] suggest to add a frequency feedback (FFB) term to the PD. During the transients, the FFB term dynamically adjusts the LF gains, while keeping the LF zero fixed, thus improves the PLL dynamic response. This approach, similar to the Karimi's approach [4], is applicable to a wide range of single-phase and three-phase PLLs.

To improve the stability and dynamic performance of the pre-filtered synchronous reference frame PLLs (SRF-PLL) while maintaining good filtering capability using a derivative filtered proportional-integral-derivative (PID) controller as the LF is suggested in [6]. Compared with the commonly adopted proportional-integral (PI) type LF, the PID-type LF provides an additional degree of freedom, and enables the designer to compensate the phase delay introduced by the pre-filtering stage of the PLL.

In recent years, some approaches based on adding a secondary control path (SCP) to the PLL structure have been proposed in literature [7]-[10]. Supposedly, the SCP improves the PLL dynamic performance without affecting its stability condition. However, no formal analysis has yet been performed to support this claim.

This paper deals with the analysis of the PLLs with SCP. The study starts with a brief overview of these PLLs. The small-signal modelling of these PLLs are then presented which simplifies the analysis. Using these models, the effects of adding the SCP on the PLL structure are briefly studied. The obtained results show that adding the SCP to the PLL structure may not be a practical approach to improve its dynamic performance mainly because it aggravates the stability problem.

II. Overview

Fig. 1 shows the basic scheme of the proposed PLL by Riccardo *et al* [7], which includes a classical quadrature PLL (*q*PLL) and a SCP. The SCP operates in a *dq* reference frame, rotating synchronously with the grid voltage nominal angular frequency ω_n, and provides an estimation of the grid voltage angle. The authors in [7] claim that the suggested SCP improves the PLL dynamic response without affecting its stability condition. To justify this, the small-signal model

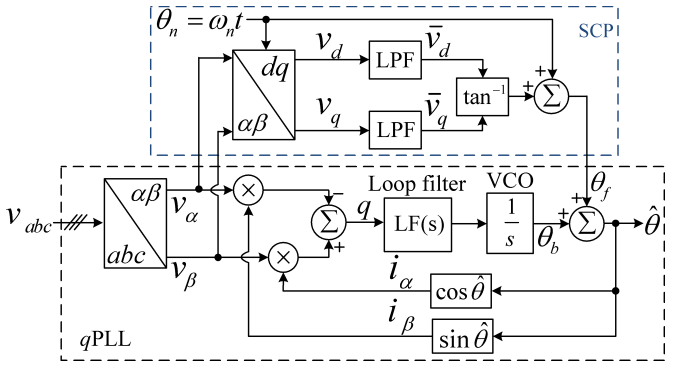

Fig. 1. Basic scheme of the feedforward qPLL (FFqPLL) [7].

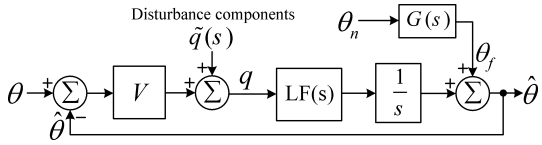

Fig. 2. Small signal model of the FFqPLL [7].

of the FFqPLL is obtained as shown in Fig 2. In this model, the action of SCP is modeled by an unknown transfer function, named $G(s)$. Then, it is discussed that the poles of $G(s)$ are external to the feedback loop. Consequently, the presence of the SCP has no effect on the qPLL stability.

Fig. 3 shows the proposed PLL by Rani *et al.* [8], which includes a conventional SRF-PLL and a SCP. In this PLL, referred to as the feedforward frequency PLL (FPLL), the VCO's center frequency is dynamically adjusted by the SCP. The authors in [8] claim that the suggested SCP improves the PLL dynamic performance without jeopardizing its stability condition.

In [9] and [10], a PLL referred to as the all-digital PLL (ADPLL) is proposed. The ADPLL can be understood as a traditional digital PLL (DPLL) which a SCP has been included in its structure. The SCP is a period detector which makes the center frequency changeable. Its main purpose, as mentioned in [9] and [10], is to improve the DPLL tracking speed. In the small-signal model of the ADPLL, the dynamics of the SCP has been neglected (see Fig. 5 in [9] and [10]).

III. Small-Signal Modeling

In this section, the small-signal modeling of the FPLL and the FFqPLL are presented. These models consider the dynamics of the SCPs. Regarding the ADPLL, this modeling cannot be done, as no detailed information about the implementation of SCP is given in [9] and [10].

A. FPLL

For the sake of simplicity, let the three-phase input voltages of the FPLL be of the form

$$\begin{aligned} v_a(t) &= V\cos\overbrace{(\omega t+\phi)}^{\theta} \\ v_b(t) &= V\cos(\omega t+\phi-2\pi/3) \\ v_c(t) &= V\cos(\omega t+\phi+2\pi/3) \end{aligned} \tag{1}$$

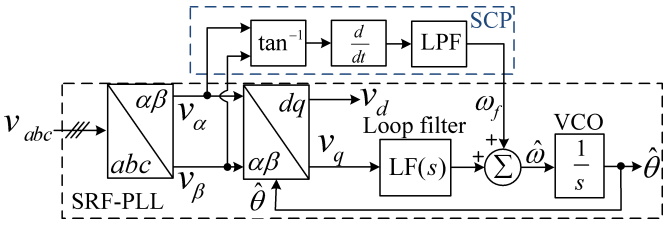

Fig. 3. Basic scheme of the feedforward frequency PLL (FPLL) [8].

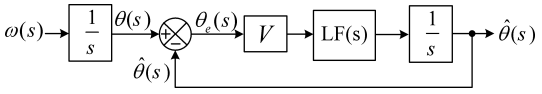

Fig. 4. The small-signal model of the conventional SRF-PLL.

where V, ω, and ϕ are the input voltages amplitude, angular frequency, and initial phase-angle, respectively.

Applying the Clarke transformation to the three-phase input voltages (1) yields the $\alpha\beta$ coordinate voltages as

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = \begin{bmatrix} V\cos(\theta) \\ V\sin(\theta) \end{bmatrix}. \tag{2}$$

According to Fig. 3, the SCP output signal can be expressed in the Laplace domain as

$$\omega_f(s) = \mathrm{LPF}(s)\times L\left(\frac{d\left\{\tan^{-1}\left(v_\beta(t)/v_\alpha(t)\right)\right\}}{dt}\right). \tag{3}$$

where L denotes the Laplace operator.

Substituting the $\alpha\beta$ coordinate voltages (2) into (3), yields

$$\begin{aligned} \omega_f(s) &= \mathrm{LPF}(s)\times L\left(\frac{d\left\{\tan^{-1}\left(\tan(\theta)\right)\right\}}{dt}\right) \\ &= \mathrm{LPF}(s)\times \underbrace{L\left(\frac{d\{\theta\}}{dt}\right)}_{\omega} = \mathrm{LPF}(s)\times\omega(s). \end{aligned} \tag{4}$$

Using (4), and the small-signal model of the conventional SRF-PLL as shown in Fig. 4, the small-signal model of the FPLL can be obtained as shown in Fig. 5. An alternative mathematically-equivalent representation of this model is shown in Fig. 6.

B. FFqPLL

The small-signal modeling of the FFqPLL is performed under the same simplifying assumption as in the case of FPLL, i.e., considering the input voltages as an undistorted and balanced three-phase system.

As shown in Fig. 1, the dq coordinate voltages in the SCP are obtained by applying the Park transformation with a rotating angle of $\theta_n = \omega_n t$ to the $\alpha\beta$ coordinate voltages, i.e.,

$$\begin{aligned} \begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} &= \begin{bmatrix} \cos(\theta_n) & \sin(\theta_n) \\ -\sin(\theta_n) & \cos(\theta_n) \end{bmatrix}\begin{bmatrix} V\cos(\theta) \\ V\sin(\theta) \end{bmatrix} \\ &= \begin{bmatrix} V\cos\left(\theta-\theta_n\right) \\ V\sin\left(\theta-\theta_n\right) \end{bmatrix} \end{aligned} \tag{5}$$

These dq coordinate voltages are then passed through two

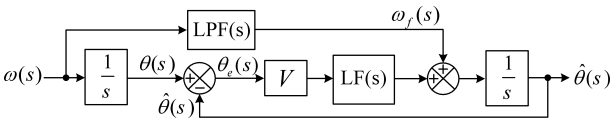

Fig. 5. The small-signal model of the FPLL.

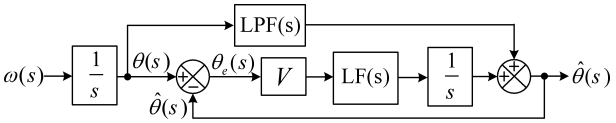

Fig. 6. Alternative mathematically-equivalent representation of the small-signal model of Fig. 5.

low-pass filters (LPFs). The SCP output signal θ_f is finally obtained by applying the inverse tangent operation to the outputs of the LPFs, and adding θ_n to the result. It is very difficult to analytically obtain a compact expression for θ_f. However, based on extensive simulation studies, we have found that it can be approximated by

$$\theta_f(s) \approx LPF(s)\left[\theta(s) - \theta_n(s)\right] + \theta_n(s) \tag{6}$$

when the grid voltage frequency is close to its nominal value; the more closer the grid frequency to its nominal value, the more accurate the approximation.

Using (6), and considering that the *q*PLL and the conventional SRF-PLL are actually the same systems, the small-signal model of the FF*q*PLL can be obtained as shown in Fig. 7, which is very similar to the FPLL's small-signal model (Fig. 6).

To evaluate the accuracy of the obtained small-signal models, a performance comparison between the PLLs under study and their small-signal models is carried out. In this study, a PI controller as the LF (i.e., $\mathrm{LF}(s) = k_p + k_i/s$ where k_p and k_i are the proportional and integral gains, respectively), and a first order LPF as the filter of the SCP (i.e., $\mathrm{LPF}(s) = \omega_p/(s+\omega_p)$, where ω_p is the cutoff frequency) is considered. The values of the control parameters are summarized in Table I. The obtained results are shown in Fig. 8. It can be observed that, for both PLLs, the small-signal model can accurately predict the actual PLL behavior.

IV. Effects of SCP

This section deals with the study of the effects caused by SCP. It was shown that the FPLL and the FF*q*PLL have almost same small-signal models. Therefore, throughout this study, the FPLL's small-signal model is considered.

TABLE I
PLLs Parameters values.

Parameter	Value
Proportional gain, k_p	70
Integral gain, k_i	6500
Cutoff frequency, ω_p	30 rad/s
Amplitude, V	1 pu
Sampling frequency, f_s	10 kHz
Nominal frequency, ω_n	$2\pi 50$ rad/s

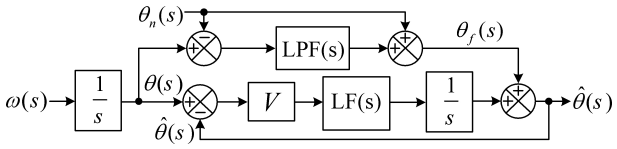

Fig. 7. The small-signal model of the FF*q*PLL.

A. Stability

The aim of this section is to answer this question: Does the SCP affect the PLL stability?

It is clear from Fig. 5 that without the SCP, the FPLL is the conventional SRF-PLL. Therefore, according to Fig. 4, the open-loop transfer function can be obtained as

$$G_{ol}^{\mathrm{SRF}} = V\,LF(s)\frac{1}{s}. \tag{7}$$

In most applications, a PI controller is selected as the LF, i.e., $LF(s) = k_p + k_i/s$. With this selection, (7) can be rewritten as

$$G_{ol}^{\mathrm{SRF}} = V\,\frac{k_p s + k_i}{s^2}. \tag{8}$$

which describes a type-*2* control system. Notice that a type-*N* control system is characterized by presence of *N* poles at the origin in its open-loop transfer function [11].

Now, the open-loop transfer function with considering the SCP is obtained. From Fig. 5, and by considering the LPF block in the SCP as a first-order LPF, i.e., $LPF(s) = \omega_p/(s+\omega_p)$, the open-loop transfer function of the FPLL can be obtained as

$$G_{ol}^{\mathrm{FPLL}} = \frac{\hat{\theta}}{\theta_e} = \frac{(Vk_p + \omega_p)\,s^2 + V\,(k_i + k_p\omega_p)\,s + Vk_i\omega_p}{s^3} \tag{9}$$

By comparing (9) with (8), it can be concluded that the SCP increases the type of the tracking loop by one. It is known that increasing the type of tracking loop aggravates the stability problem [12], [13]. Therefore, contrary to what was reported in [7] and [8], the SCP affects the PLL stability.

B. Static Performance

In this section, the effect of the SCP on the steady-state performance of the PLL is investigated.

It was shown in previous section that the SCP increases the type of tracking loop by one. It is well-known that increasing the type of tracking loop enables the control system to track faster reference signals with a lower steady-state error [13]. Therefore, it can be concluded that, in terms of the steady-state performance, the SCP improves the PLL performance. For example, Fig. 9 provides a comparison between the SRF-PLL (FPLL without SCP) and the FPLL when the grid voltage frequency changes linearly with time. The control parameters are given in Table I. As shown, the FPLL yields a zero steady-state phase error during frequency ramping interval, while the SRF-PLL has a steady-state phase error of about 0.9°. This result was expected as the FPLL is a type-3 control system.

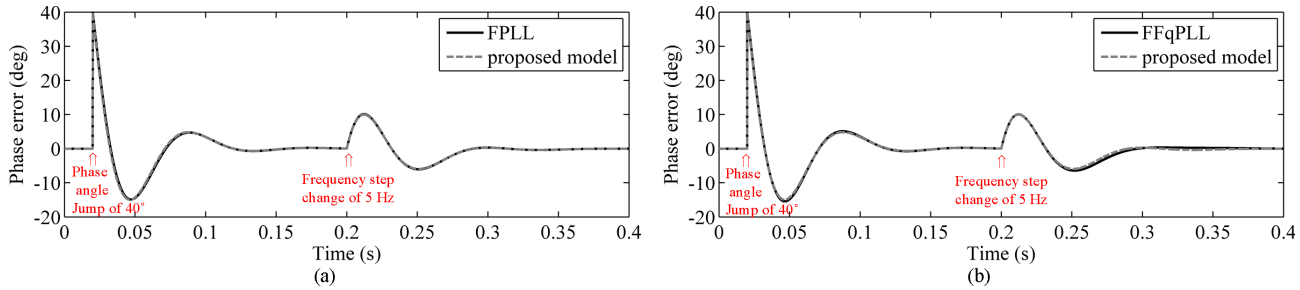

Fig. 8. Performance comparison between (a) the FPLL and its small-signal model, (b) the FFqPLL and its small-signal model under a phase-angle jump of $+40°$ and a frequency step change of $+5$ Hz.

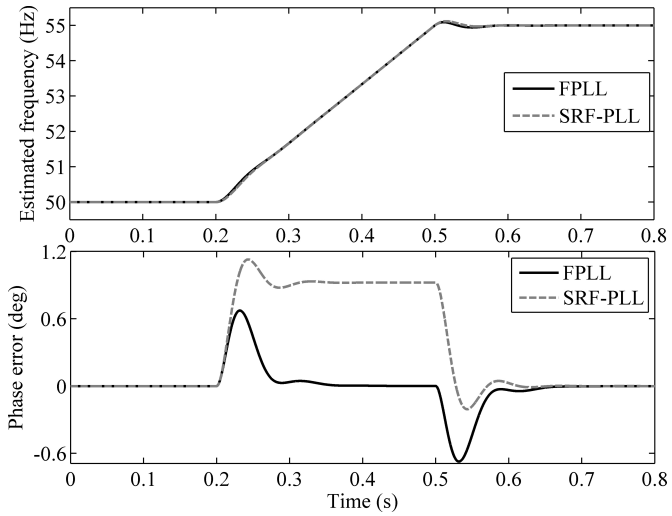

Fig. 9. Performance comparison between the FPLL and SRF-PLL (FPLL without SCP) when the grid frequency changes linearly with time.

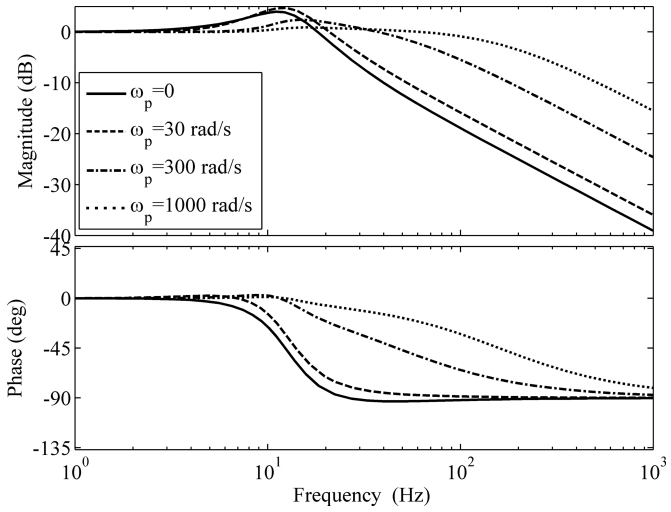

Fig. 10. Bode plots of the closed-loop transfer function (10) for $V = 1$ pu, $k_p = 70$, $k_i = 6500$ and four different values of ω_p : $\omega_p = 0$ (solid line), 30 rad/s (dashed line), 300 rad/s (dash-dotted line), and 1000 rad/s (dotted line)

C. Dynamic Performance

In this section, the effect of SCP on the PLL dynamic performance is studied.

From Fig. 5, the closed loop transfer function of the FPLL can be obtained as

$$G_{cl}^{\text{FPLL}}(s) = \frac{\hat{\theta}}{\theta} = \frac{(Vk_p + \omega_p)\, s^2 + V\,(k_i + k_p\omega_p)\, s + Vk_i\omega_p}{s^3 + (Vk_p + \omega_p)\, s^2 + V\,(k_i + k_p\omega_p)\, s + Vk_i\omega_p} \quad (10)$$

Fig. 10 shows the Bode plots of the closed-loop transfer function (10) for $V = 1$ pu, $k_p = 70$, $k_i = 6500$, and four different values of ω_p: $\omega_p = 0$, 30, 300, and 1000 rad/s. Notice that $\omega_p = 0$ corresponds to disconnecting the SCP from FPLL. From Fig. 10, it can be observed that the presence of the SCP increases the PLL closed-loop bandwidth, and in this way improves the PLL dynamic performance. The higher the cutoff frequency ω_p, the higher the closed-loop bandwidth, and the faster the dynamic response.

It should be emphasized here that all conclusions drawn in section IV are for the case of using the PI-type LF in the PLL control loop, and they may not be valid as a general rule.

V. SCP-less Equivalent of PLL with SCP

It is shown in this section that adding the SCP to the PLL is mathematically equivalent to changing its LF.

From Fig. 5, the open-loop transfer function of the FPLL can be obtained in general form as

$$G_{ol}^{\text{FPLL}}(s) = V \times \underbrace{\frac{\text{LF}(s) + s\text{LPF}(s)/V}{1 - \text{LPF}(s)}}_{\text{LF}^*(s)} \times \frac{1}{s}. \quad (11)$$

By comparing (11) with the open-loop transfer function of the SRF-PLL, i.e., (7), it can be concluded that the FPLL is mathematically equivalent with a conventional SRF-PLL with $\text{LF}^*(s)$ as the LF transfer function. For example, (12) expresses $\text{LF}^*(s)$ for a simple case of $\text{LF}(s) = k_p + k_i/s$ and $\text{LPF}(s) = \omega_p/(s + \omega_p)$. Notice that the coefficient(s) of $\text{LF}^*(s)$ depend on the input voltage amplitude. Therefore, the equivalency is valid for a fixed voltage amplitude.

$$\text{LF}^*(s) = \overbrace{(k_p + \omega_p/V)}^{C_0} + \frac{\overbrace{(k_i + k_p\omega_p)}^{C_1}}{s} + \frac{\overbrace{k_i\omega_p}^{C_2}}{s^2}. \quad (12)$$

VI. Conclusion

The aim of this paper was to analyze the PLLs with a SCP. The paper was started with an overview of these PLLs. The small-signal modeling of these PLLs was then presented. Using these models, an analysis was performed. It was shown that: 1) the SCP increases the type of PLL control loop by one, which aggravates the stability problem; 2) the SCP enables the PLL to track faster reference signals with a lower tracking error; 3) the SCP increases the PLL bandwidth, and thus improves its dynamic performance. It was also shown that adding the SCP to the PLL is mathematically equivalent to changing its LF. Considering that the SCP increases the PLL implementation complexity, and aggravates the stability problem, it can be concluded it may not be a practical approach to improve the PLL dynamic performance. However, it may be useful when tracking the fast reference signals, such as frequency ramps, is necessary for the PLL.

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