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Published in:
I E E E Transactions on Electron Devices

DOI (link to publication from Publisher):
10.1109/TED.2013.2275177

Publication date:
2013

Document Version
Accepted author manuscript, peer reviewed version

Modeling and Design Guidelines for P$^+$ Guard Rings in Lightly Doped CMOS Substrates

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***Abstract*—This paper presents a compact model for P$^+$ guard rings in lightly doped CMOS substrates featuring a P-well layer. Simple expressions for the impedances in the model are derived based on a conformal mapping approach. The model can be used to predict the noise suppression performance of P$^+$ guard rings in terms of S-parameters, which is useful for substrate noise mitigation in mixed-signal SoCs. Validation of the model has been done by both EM simulation and experimental results from guard rings implemented using a standard 0.18 μm CMOS process. In addition, design guidelines have been drawn for minimizing the guard ring size while maintaining the noise suppression performance.**

***Index Terms*—Compact model, mixed-signal IC, guard ring, P$^+$ contact, P-well, substrate noise**

I. Introduction

The increasing demand for powerful electronic devices has resulted in a growing need for large scale mixed-signal System-on-Chips (SoCs), requiring the integration of digital circuits and analog/RF circuits on the same chip [1]. However, analog/RF circuits in mixed-signal SoCs often suffer from performance deterioration due to the substrate noise generated by digital circuits. This is especially the case when CMOS processes with lightly doped substrates are used for the implementation to reduce the cost [2]. P$^+$ guard ring is a layout design approach and one of the most widely used noise suppression methods in modern SoCs as it features low cost and easy implementation [2], [3]. Fig. 1 shows a generic P$^+$ guard ring implemented on a typical lightly doped CMOS substrate. The aggressor contact represents the noise coupling node in digital circuits and the victim contact represents the coupling node of any analog/RF circuits on the same chip. The noise suppression performance of the guard ring is dependent on layout and substrate parameters [2], such as the aggressor-to-guard ring distance (d_{ag}), guard ring-to-victim distance (d_{gv}), guard ring width (w_g), resistivity/permittivity of the substrate ($\rho_{1,2}/\epsilon_{ox,1,2}$) and substrate thicknesses ($t_{ox,1,2}$).

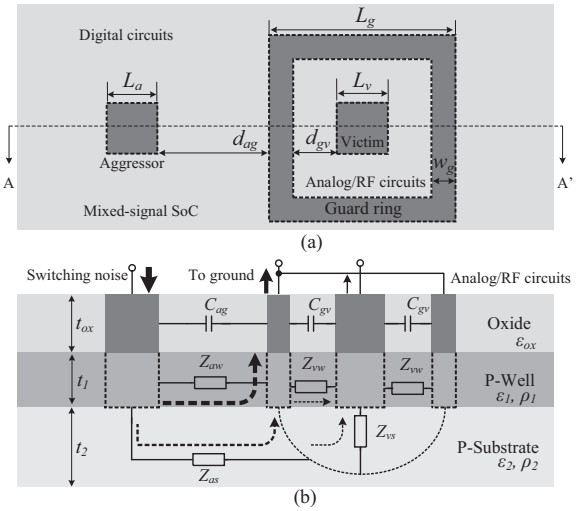

Fig. 1. The (a) top view and (b) cross section view of a generic P$^+$ guard ring implemented on a lightly doped CMOS substrate.

Currently the guard ring parameters are mainly investigated by measurements and designed based on empirical rules-of-thumb [2], [3]. However, the noise suppression level of these designs is usually unpredictable and the chip area could easily be wasted as the dependency of the noise suppression performance on guard ring parameters has not been accurately characterized. Recently, efforts have been made to find compact P$^+$ guard ring models, which provide more insights into the dependency [4]–[7]. However, some of these models require fitting-factors [4], which needs calibration fixtures and therefore are unfeasible for pre-layout predictions. Some of the models characterize the guard ring by dividing the guard ring into numerous small contacts/cells [5], [6], which increases the model complexity significantly. Other models failed to address the constriction resistances as well as capacitive coupling, which makes them valid only for low frequency designs on uniform or epitaxial substrates [7]. Unlike uniform or epitaxial substrates, the lightly doped substrates of standard CMOS processes have a thin P-well layer (Fig. 1(b)). The P-well layer introduces

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This study is supported by the Danish Research Council for Technology and Production Sciences (FTP).

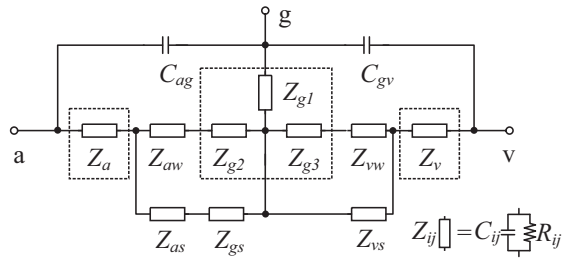

Fig. 2. The proposed circuit model for the P^+ guard ring in Fig.1.

significant current constriction effects at near fields close to the contacts [8]. Such effects can not be effectively characterized by existing guard ring models. To obtain accurate noise suppression predictions and to help SoC designers to manage the noise issues new guard ring models feasible for lightly doped substrates are desired.

This paper proposes a P^+ guard ring model where constriction resistances and capacitive coupling are included. Equations are derived based on a conformal mapping approach to fully characterize the effects of the layout/substrate parameters, eliminating any fitting factors. EM simulation and experimental verifications on DC resistances and S-parameters have been conducted as well. This paper is arranged as follows: Section II presents the proposed model. EM-simulation validation is presented in section III, and the experimental verification as well as design guidelines are discussed in section IV. Section V draws the conclusion.

II. The proposed guard ring model

The proposed three port circuit network model for the guard ring in Fig. 1 is shown in Fig. 2. The proposed model includes both the resistive and capacitive coupling between the aggressor, guard ring and victim, as represented by ports a, g and v, respectively. Please note that the model does not include the interconnection of the guard ring to on-chip ground. In the proposed model, C_{ag}, C_{gv} denote the capacitances between the aggressor, guard ring and victim in the oxide layer, respectively. For typical CMOS processes where the P-well layer is significantly more conductive and 2-3 orders thinner than the P-substrate, the majority of the noise current flows horizontally from the aggressor to the victim in the P-well. This means there is no current flowing into the P-substrate except at the near fields of the aggressor, guard ring and victim. Therefore the impedances between the aggressor/victim and guard ring are divided into two parallel parts in the P-well layer and P-substrate, e.g. Z_{aw}/Z_{vw} and $Z_{as}, Z_{gs}/Z_{vs}$, respectively. It should be noted that Z_{aw}/Z_{vw} and $Z_{as}, Z_{gs}/Z_{vs}$ represent the impedances between the dashed surfaces (Fig.1(b)), which do not include the constriction resistances in the near field of the contacts [8]. In this paper, this error is corrected by adding Z_a, Z_{g1-3} and Z_v to characterize the current constriction effects for the aggressor, guard ring and victim, respectively.

In consistence with the work in [7], the model proposed here approximates the layout of the square contacts and guard rings using circular shapes. The approximation is based on the condition that circular contacts or guard rings have the same area as the corresponding rectangular contacts and guard rings. As has been discussed in [7], the approximation error is acceptable for practical use. Thus $r_{a,v} = L_{a,v}/\sqrt{\pi}$, where r_a and r_v are the radii of the circular contacts approximating the square aggressor and victim contact (with side length $L_{a,v}$), respectively. For a square guard ring with an outer side length of L_g and a width of w_g, it is approximated as a circular guard ring with the outer and inner radius of $r_g = L_g/\sqrt{\pi}$ and $r_{gin} = (L_g - w_g)/\sqrt{\pi}$, respectively.

A. Model components without constriction effects

For a homogeneous medium with resistivity of ρ and permittivity of ϵ there exists the relationship [9]

$$R = \rho\epsilon/C, \tag{1}$$

where R and C are the resistance and capacitance of the medium. Therefore this paper only discusses either R or C in Z_{ij}. The corresponding C or R can be obtained using (1). Based on the square-to-circular layout approximations the capacitance C_{ag} is derived as

$$C_{ag} = 2\pi\epsilon_{ox}t_{ox}/\text{acosh}\left[\frac{1}{2}\left(\frac{D^2}{r_a r_g} - \frac{r_a}{r_g} - \frac{r_g}{r_a}\right)\right], \tag{2}$$

where $D = d_{ag} + r_a + r_g$, and C_{gv} is the capacitance between the lateral surfaces of a cylindric ring with inner radius r_v, outer radius r_{gin} and height t_{ox}

$$C_{gv} = 2\pi\epsilon_{ox}t_{ox}/\ln\frac{r_{gin}}{r_v}, \tag{3}$$

and similarly C_{aw} can be derived as

$$C_{aw} = 2\pi\epsilon_1 t_1/\text{acosh}\left[\frac{1}{2}\left(\frac{D^2}{r_a r_g} - \frac{r_a}{r_g} - \frac{r_g}{r_a}\right)\right]. \tag{4}$$

In practical cases the conductivity in a P-well layer is a function of the distance to the top of the layer (Fig. 3). In this paper, the thickness of the P-well layer is defined as the conductivity drops to 10% of $\sigma_p - \sigma_{sub}$, where σ_p and σ_{sub} are the conductivities of the P-well and P-substrate, respectively. By dividing the P-well into infinitely thin layers, uniform doping can be assumed for each layer and hence it has

$$R_{aw} = \frac{1}{2\pi G}\text{acosh}\left[\frac{1}{2}\left(\frac{D^2}{r_a r_g} - \frac{r_a}{r_g} - \frac{r_g}{r_a}\right)\right], \tag{5}$$

where

$$G = \int_{t_{ox}}^{t_1}\sigma(t)dt. \tag{6}$$

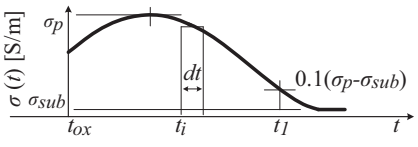

Fig. 3. Typical conductivity profile by ion implantation in P-well layer. The bottom of the oxide layer is set as the origin in the coordinate.

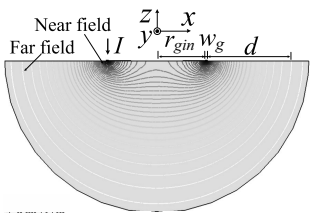

Fig. 4. Simulated electric potential field of a circular ring contact on a thick substrate when a current I is fed into the contact.

Similarly, R_{vw} is derived as

$$R_{vw} = \frac{1}{2\pi G} \ln \frac{r_{gin}}{r_v}. \tag{7}$$

Calculating Z_{as}, Z_{gs} and Z_{vs} is different from that of Z_{aw} and Z_{vw}. This is because the current in the P-substrate is spreading over a much thicker substrate and can not be assumed to be horizontal. The spreading resistance of a circular contact on a semi-infinite substrate has been discussed in [10] and it is given as

$$R_{as} = \frac{\rho_2}{4r_a}\left[1 - \frac{2}{\pi}\text{asin}\left(\frac{r_a}{r_a + d_{ag}}\right)\right]. \tag{8}$$

For a P^+ guard ring on a thick substrate the current spreads like a circular contact at far field [11] (Fig. 4), while the constriction effects at the near field are different. In this paper the far field resistance of the guard ring is calculated by treating the ring as a circular contact with a radius of r_g

$$R_{gs} = \frac{\rho_2}{4r_g}\left[1 - \frac{2}{\pi}\text{asin}\left(\frac{r_g}{r_g + d_{ag}}\right)\right], \tag{9}$$

where $r_g = r_{gin} + w_g$. The near field constriction effects are described by R_{g1-3} (discussed in the following subsection) in Fig. 2. Different from the aggressor, the victim is inside the guard ring. Thus R_{vs} is the resistance between the victim and the equipotential surface at distance of d_{gv}

$$R_{vs} = \frac{\rho_2}{4r_g}\left[1 - \frac{2}{\pi}\text{asin}\left(\frac{r_v}{r_v + d_{gv}}\right)\right]. \tag{10}$$

B. Model components with constriction effects

Z_a, Z_v and Z_{g1-3} that denote the constriction effects are calculated based a conformal mapping approach. The conformal mapping approach was used for 2-D thin film patterns in [12], [13], while recent research has shown its potential in 3-D substrate resistances [14]. Fig. 5(a) shows the cross section view of two back-to-back connected contacts (C-D and C′-D′) in complex plane z. The resistance between the two contacts can not be easily derived since simple closed-form expressions for the current flow lines (dashed lines with arrows) or the equipotential surfaces (dot lines) at the near field are usually unavailable (such as the case in Fig. 1). However, using conformal mapping, the contacts in the z-plane can be mapped to a z1-plane, where the structure is simple and the resistance can be derived. Since the mapping is conformal, the current flow and equipotential surface is kept perpendicular at any places. This guarantees that the resistance between the contacts in the z1-plane is the same as that in the z-plane. In the z1-plane, half of the resistance between the contacts is

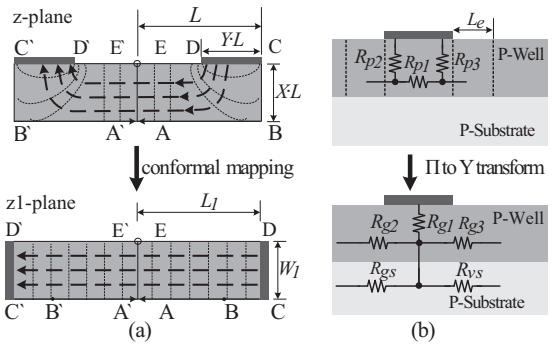

Fig. 5. (a) Conformal mapping for the calculation of the constriction resistance of a contact on a P-well layer, and (b) Π to Y network transform for the constriction resistances at the near field of a contact.

$$R = \frac{\rho}{t} L_1/W_1, \tag{11}$$

where ρ is the resistivity of the medium and t is the thickness (perpendicular to the paper). R can also be represented using the available parameters (layout/substrate parameters) in z-plane with a correction term

$$R = \frac{\rho}{t}[(1-Y)/X + L_e/XL], \tag{12}$$

where L_e is the equivalent length for correction of the neglected constriction resistance. It is clear that

$$L_e = XLL_1/W_1 - (1-Y)L. \tag{13}$$

In the case of $X << 1$, and $Y < 0.5$, L_e can be approximated as [12], [13]

$$L_e = \frac{Y}{X} - \frac{2}{\pi}\ln\left[\sinh(\frac{Y\pi}{2X})\right], \tag{14}$$

and for the case of $X << 1$, and $Y > 0.5$, L_e can be approximated as [13]

$$L_e = K(p)/K'(p) - (1-Y)K(k)/K'(k), \tag{15}$$

where $p = \tanh[\pi(1-Y)/2X]$. K is the complete

elliptic integral of first kind, and $K'(k) = K(\sqrt{1-k^2})$.

Given that R_{p2} and R_{p3} are the lateral constriction resistances of the contact (Fig. 5(b)), they can be easily calculated by extending the lateral length by L_e. R_{p1} represents the resistance between the inner two dashed lines beneath the contact. For circular aggressor and victim, the inner dashed lines represent the same equipotential surface around the contact and thus $R_{p1} = 0$. Thus the values for R_a and R_v in Fig. 2 can be found by

$$R_a = \frac{1}{2\pi G}\text{acosh}\left[\frac{1}{2}\left(\frac{(D+L_{ea})^2}{r_a r_g} - \frac{r_a}{r_g} - \frac{r_g}{r_a}\right)\right] - \frac{1}{2\pi G}\text{acosh}\left[\frac{1}{2}\left(\frac{D^2}{r_a r_g} - \frac{r_a}{r_g} - \frac{r_g}{r_a}\right)\right], \quad (16)$$

where L_{ea} is the equivalent length for calculating the constriction resistances of the aggressor. Similarly,

$$R_v = \frac{1}{2\pi G}\ln\frac{r_v + L_{ev}}{r_v}, \quad (17)$$

where L_{ev} is the equivalent length for calculating the constriction resistances of the victim. For guard rings, the inner dashed lines are not necessarily on the same equipotential surface as they are at the side facing the aggressor and victim, respectively. Hence R_{p1} is not necessarily zero and it can be calculated by

$$R_{p1} = \frac{1}{2\pi G}\ln\frac{r_g}{r_{gin}}. \quad (18)$$

Assuming R_{p2} of the guard ring is at the aggressor side, then it can be calculated by

$$R_{p2} = \frac{1}{2\pi G}\ln\frac{r_g + L_{eag}}{r_g}, \quad (19)$$

where L_{eag} is the equivalent length of the constriction resistance. R_{p3} is the lateral resistance of a ring with inner radius of $r_{gin} - L_{egv}$ and outer radius of r_{gin}

$$R_{p3} = \frac{1}{2\pi G}\ln\frac{r_{gin}}{r_{gin} - L_{egv}}, \quad (20)$$

where L_{egv} is the equivalent length of the constriction resistance at the victim side. The Π network in Fig. 5(b) is transferred to a Y-network to obtain R_{g1-g3}: $R_{g1} = R_{p2}R_{p3}/(R_{p1}+R_{p2}+R_{p3})$, $R_{g2} = R_{p2}R_{p1}/(R_{p1}+R_{p2}+R_{p3})$ and $R_{g3} = R_{p3}R_{p1}/(R_{p1}+R_{p2}+R_{p3})$.

III. EM SIMULATION VALIDATIONS

The proposed model is based on the approximation of horizontal current flow in the P-well layer, which is valid for thin P-Wells but less so for thicker P-wells. EM simulation has been done to validate the model and to illustrate the applicable range of the model in processes with different P-well resistivity and thickness. The schematic in Fig. 1 and EM simulation software CST STUDIO SUITE™ were used for the simulation. To simplify the simulation uniform conductivity is used for the P-well layer since non-uniform conductivity profile can not be defined in the EM simulator. Fig. 6(a) and (b) show the calculated and simulated R_{gv} and R_{ag}, respectively. Here, $R_{ag} = R_a + R_{g1} + (R_{aw}+R_{g2})//(R_{as}+R_{gs})$, and $R_{gv} = R_v + R_{g1} + (R_{vw}+R_{g3})//R_{vs}$. It can be seen that the calculated resistances match the simulated results well, especially for small thicknesses (error $< 5\%$ for $t_1 < 5\,\mu$m). As most CMOS processes fall within this range the proposed model is widely applicable.

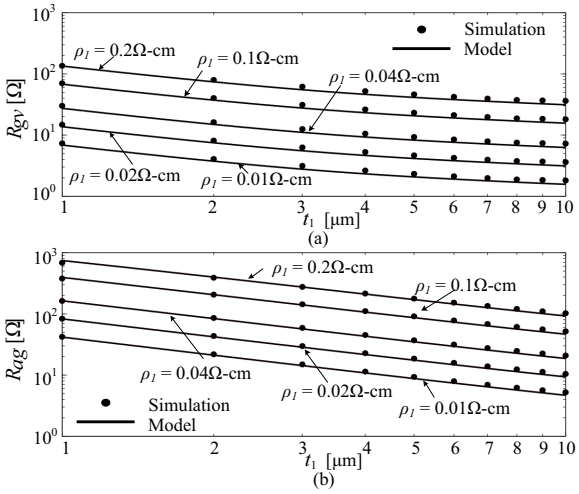

Fig. 6. The modeled and simulated (a) guard ring-victim resistance and (b) aggressor-guard ring resistance versus P-well thickness. The used parameters are: $L_a = L_v = 20\,\mu$m, $L_g = 40\,\mu$m, $w_g = 5\,\mu$m, $d_{ag} = 20\,\mu$m, $t_2 = 200\,\mu$m and $\rho_2 = 20\,\Omega$−cm.

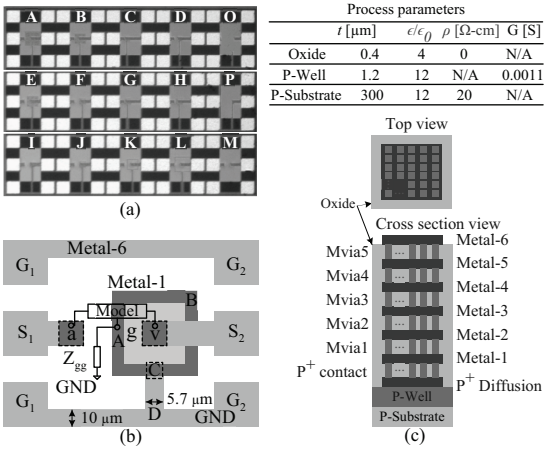

Fig. 7. The (a) microphotograph of the fabricated guard ring testing fixtures, (b) an example fixture with equivalent circuit, and (c) the P^+ diffusion to top metal connection using a large number of vias.

IV. EXPERIMENTS

Fig. 7(a) shows the guard ring testing fixtures (denoted by A-L) that have been fabricated using a standard

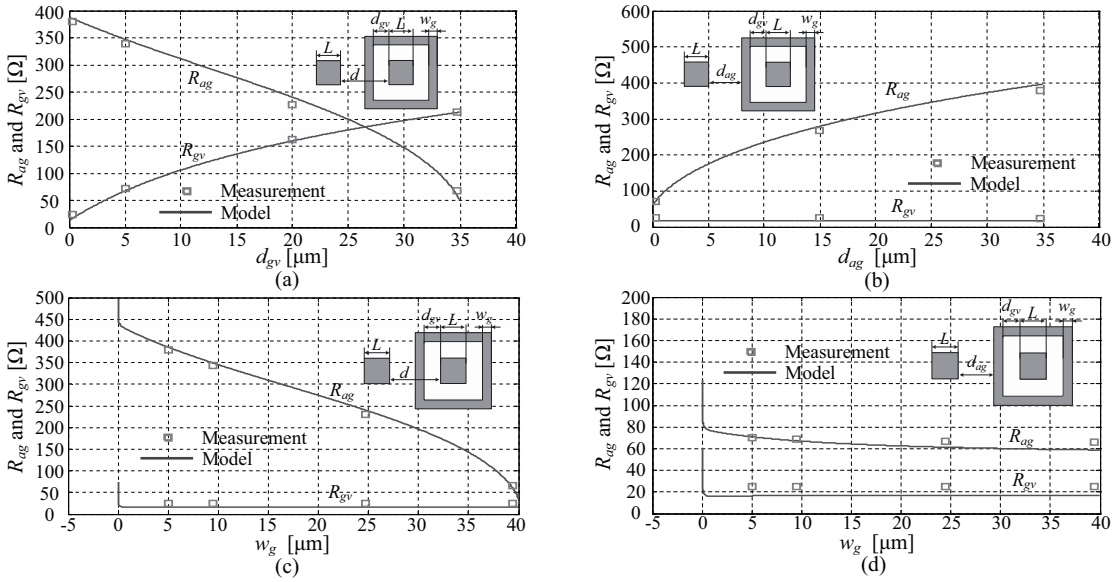

Fig. 8. Measured and calculated aggressor-to-guard ring and guard ring-to-victim resistances versus (a) guard ring-to-victim distance ($d = 40$ μm, and $w_g = 5$ μm), (b) aggressor-to-guard ring distance ($d_{gv} = 0.28$ μm, and $w_g = 5$ μm), (c) guard ring width with fixed d ($d_{gv} = 0.28$ μm, and $d = 40$ μm) and (d) guard ring width with fixed d_{ag} and d_{gv} ($d_{gv} = d_{ag} = 0.28$ μm). $L = 20$ μm for all the cases.

0.18 μm 6-metal CMOS process to verify the proposed model. The process is aluminum and silicon dioxide based and the process parameters are given in Fig. 7. The value for G is calculated using (6) based on the ion implantation profile of the process.

The reference fixture M has no guard ring and the circuit model for it is a two-port network (port g is removed and so the components related to guard ring.). The calculation of remaining impedance components are the same as the calculation in fixtures A-L except that R_{vw} is calculated using the same equation (5) as R_{aw} instead of equation (7) [14]. Fixtures O and P are the open and short fixtures for de-embedding. Fixture O has the same layout as fixtures A-L except that the guard ring, the aggressor contact, the victim contact and their connections to the top metal are removed (Metal-6 straps are kept). Fixture P has the same layout as O but with signal pads connected to the ground pads on the top metal layer. The side length of all the aggressor and victim contacts was chosen to 20 μm.

G-S-G pads are used for on-wafer resistance and S-parameter measurements. An example fixture and the simplified three-port model of Fig. 2 are shown in Fig. 7(b). The aggressor and victim contacts are connected to the signal pads using vias and metal1-6 (Fig. 7(c)). The P^+ guard ring is connected to metal-1, and then connected to the top metal layer, metal-6 using vias at point C. A strap on metal-6 is connecting point C to the reference ground (point GND). Due to the non-zero resistivity the metal straps add on more impedance in the path from the guard ring to ground, which can not be de-embedded. As shown in Fig. 7(b) an impedance Z_{gg} is used to include this effect into the equivalent circuit of the guard ring as $Z_{gg} = R_{gg} + j\omega L_{gg} = R_{ring} + R_{st} + j\omega L_{l1} + j\omega L_{l2}$, where R_{ring} is the resistance between point A and point C. Two metal-1 straps A-C, and A-B-C are connected in parallel. R_{ring} can be calculated based on the resistance of each strap using their lengths and sheet resistivity of metal-1. R_{st} is the resistance of the strap connecting the guard ring and the ground (GND). L_{l1} and L_{l2} are the inductance of the straps C-D and D-GND, respectively. R_{st} is calculated in the similar way as R_{ring} but using the sheet resistivity of metal-6. $L_{l1,2}$ (in nH) are given by the equation of the self inductance for a l-meter long strap [15]

$$L_l = \frac{l}{5}\left[\ln\left(\frac{2{\cdot}l}{(w+t)}\right) + \frac{0.223(w+t)}{l} + 0.5\right], \quad (21)$$

where w and t are the width and thickness of the metal strap C-D and D-GND, respectively.

A. DC resistance verification

In the verification. R_{ag} and R_{gv} and R_{av} are used to represent the resistance between point S_1-GND, S_2-GND and S_1-S_2 respectively. Hence, $R_{ag} = R_a + R_{g1} + (R_{aw} + R_{g2})//(R_{as} + R_{gs}) + R_{gg}$; $R_{gv} = R_v + R_{g1} + (R_{vw} + R_{g3})//R_{vs} + R_{gg}$ and $R_{av} = R_a + R_v + (R_{vw} + R_{g3})//R_{vs} + (R_{aw} + R_{g2})//(R_{as} + R_{gs})$. Further, the sum $R_{g1} + R_{gg}$, has been extracted from the measured results using $R_{g1} + R_{gg} = (R_{ag} + R_{gv} - R_{av})/2$.

The measured and calculated R_{ag} and R_{gv} of guard ring fixtures with varying d_{gv} are shown in Fig. 8(a).

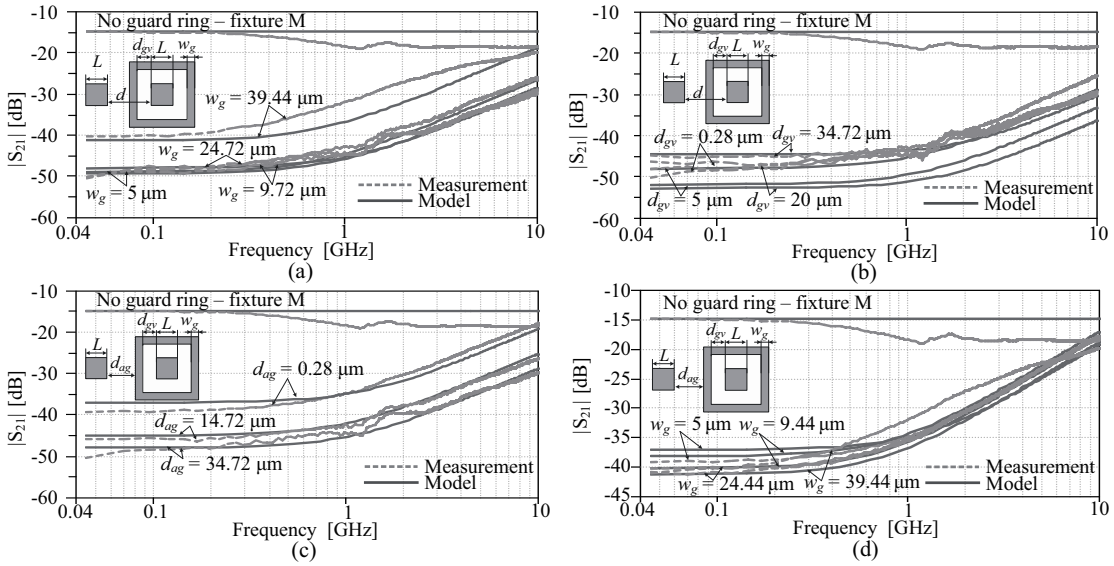

Fig. 9. Measured and calculated S_{21}-magnitudes versus frequency with varying (a) guard ring width ($d_{gv} = 0.28$ μm, and $d = 40$ μm), (b) guard ring-to-victim distances ($w_g = 5$ μm, and $d = 40$ μm), (c) aggressor-to-guard ring distances ($w_g = 5$ μm, and $d_{gv} = 0.28$ μm) and (d) aggressor-to-victim distances and guard ring width ($d_{ag} = 0.28$ μm, and $d_{gv} = 0.28$ μm). $L = 20$ μm in all the cases.

It can be seen that the calculated results match the measured results very well. It should be noted that R_{gv} is still about 20 Ω even when the guard ring is very close to the victim contact ($d_{gv} = 0.28$ μm). In this case the constriction resistances at the near field of the victim and guard ring (R_{g1}, R_v) dominate the value of R_{gv}.

The measured and calculated R_{ag} and R_{gv} of guard ring fixtures with varying d_{ag} are shown in Fig. 8(b). It can be seen that the measured and calculated R_{gv} is almost constant. This is because only d_{ag} is varying but not the guard ring layout in this test. It can also be seen that R_{ag} increases as d_{ag} is increasing. In addition a saturation effect can be observed for longer distances.

Guard ring fixtures with varying w_g and fixed aggressor-to-victim distance are also investigated. The measured and calculated R_{ag} and R_{gv} are shown in Fig. 8(c). It can be seen that R_{ag} decreases as the guard ring widens and approaches the aggressor. R_{gv} is almost constant for most of the width values. This is because the charge distribution is mainly at the edge of the contact. Thus the guard ring spreading resistance is close to the resistance of a circular contact with the same radius [11]. When w_g is close to zero, both R_{ag} and R_{gv} increase drastically due to the significantly increased constriction resistance of the guard ring (R_{g1}). When $w_g = 0$, which is the case of no guard ring (fixture M), $R_{g1} = \infty$, and $R_{g2} = R_{g3} = 0$. In this scenario, there is no resistive coupling between port a and port g.

Another study focuses on guard rings with varied w_g and fixed d_{ag} and d_{gv}. Results show that both R_{ag} and R_{gv} are almost constant when the width of the guard ring is increasing (Fig. 8(d)). This is because the near field constriction resistance is dominating the total values of R_{ag} and R_{gv} for the fixtures in this test. Similar to the case in Fig. 8(c) R_{ag} and R_{gv} increase remarkably when the width of the guard ring is close to zero.

B. S-parameter verification

The proposed model has been verified by S-parameter measurements. Fig. 9(a) shows the measured and calculated $|S_{21}|$s of the reference fixture and guard rings with varying guard ring width. Good match between the modeled and the measured results is shown. In addition, stronger coupling in the guard ring fixtures is observed at higher frequencies. This is mainly due to L_{gg} (Fig. 7(b)) and parasitical capacitances between the aggressor, guard ring and victims. A decreased coupling in the reference fixture is observed at higher frequencies. This is mainly due to the aggressor-to-ground and victim-to-ground capacitances [16]. It can be seen that the noise suppression level decreases drastically when the guard ring is wide and close to the aggressor. This indicates that a wide guard ring may lead to deteriorations of the noise suppression performance.

Fig. 9(b) shows the measured and calculated $|S_{21}|$s of guard rings with varying guard ring-to-victim distances. Apart from the good agreement between the measured and calculated results, it can also be seen that the coupling strength increases when the distance between the guard ring and victim increases. This indicates that the guard ring should be placed close to the victim to

TABLE I
PARAMETERS OF THE GUARD RING TESTING FIXTURES AND THE MEASURED AND CALCULATED MODEL COMPONENTS

	A	B	C	D	E	F	G	H	I	J	K	L
d_{ag} [μm]	0.28	0.28	0.28	14.72	15.00	30.00	0.28	10.00	34.72	30.00	15.00	0.28
d_{gv} [μm]	0.28	0.28	0.28	0.28	0.28	0.28	0.28	5.00	0.28	5.00	20.00	34.72
w_g [μm]	39.44	24.44	5.00	5.00	24.72	9.72	9.44	5.00	5.00	5.00	5.00	5.00
R_{ag}-meas. [Ω]	66.3	66.9	70.3	267.4	230.6	343.8	68.7	209.8	379.5	338.4	226.3	67.5
R_{ag}-calc. [Ω]	59.4	62.1	72.6	278.7	240.7	354.0	68.7	223.3	396.3	354.3	242.0	60.3
R_{gv}-meas. [Ω]	25.1	25.1	24.9	25.3	25.2	25.1	25.1	72.3	24.6	72.4	161.9	213.7
R_{gv}-calc. [Ω]	17.6	17.7	17.5	17.5	17.6	17.7	17.7	68.9	17.8	69.1	161.4	211.6
$R_{g1}+R_{gg}$-meas. [Ω]	0.58	0.59	0.92	1.25	0.63	0.93	0.63	1.75	1.10	1.86	2.67	1.26
$R_{g1}+R_{gg}$-calc. [Ω]	0.65	0.76	1.20	1.28	0.71	0.96	1.02	1.29	1.24	1.25	1.44	1.73
L_{gg}-calc. [nH]	0.14	0.16	0.15	0.20	0.15	0.17	0.19	0.19	0.18	0.17	0.15	0.14
Area/Iso [μm^2/dB]	299	154	39	40	154	73	59	61	54	75	159	267

achieve a better suppression of the substrate noise when the distance between aggressor and victim is fixed.

Fig. 9(c) shows the measured and calculated $|S_{21}|$s of guard ring fixtures with varying aggressor-to-guard ring distances. A clear enhancement of the noise suppression level can be obtained as d_{ag} is increasing. But the enhancement is saturated for longer distances, which is consistent with the results in Fig. 8(b).

The measured and calculated S-parameters of guard rings with varying W_g and fixed d_{ag} and d_{gv} are shown in Fig. 9(d). It can be seen that the suppression levels of the fixtures are close to each other even though the guard ring widths are drastically different. This feature is accurately predicted by the calculated results based on the proposed model. This indicates that increasing the guard ring width can not guarantee an improved noise suppression performance.

C. Discussion and design guidelines

As shown in Fig. 9 the predicted S-parameters well match the experimental results in a broad frequency band ranging from 45 MHz to 10 GHz. Therefore the proposed model is of interest not only for narrow-band mixed-signal ICs, in which the interested noise frequency band is usually at a few hundreds MHz [17], but also for broad band systems such as UWB ICs [18]. In addition, the proposed model reveals the area effectivenesses of different guard ring designs. Here an area effectiveness factor is defined by Area/Iso, where Area is calculated by multiplying the length and width of the guard ring fixture and Iso is the measured $|S_{21}|$ at 100 MHz of each guard ring fixture. A small area effectiveness value indicates a chip area-saving design. As shown in Table I, the guard ring with small w_g and small d_{gv} (fixture C and D) provides the best area effectiveness among all the fixtures. When d_{ag} increases (fixture I), the area effectiveness drops, but is still better than other fixtures. Based on the proposed model design guidelines for chip area efficient P^+ guard rings can be concludes as below:

1) Determine w_g. Guard ring widths of a few μm, e.g. 5 μm, should be appropriate for most cases.
2) Determine d_{gv}. The guard ring should be placed close to the victim. The minimum P^+-P^+ distance in layout design constrain could be used.
3) Determine d_{ag}. d_{ag} should be less than the side length of the contacts, as the enhancement in noise suppression saturates for large d_{ag} values.
4) S-parameter calculation. The components in the model can be calculated using (2) to (20) with the designed parameters. Then the S-parameters can be calculated using SPICE simulations.

For designs aiming at optimum noise suppression level instead of layout area efficiency, the design guidelines for w_g and d_{gv} are still applicable. But d_{ag} should be as large as possible (Fig. 9(c)). Besides, the guard ring should always be well connected to the closest ground to minimize $Z_{gg} = R_{gg}+jwL_{gg}$ in practical designs. It can help maximize the noise suppression performance and improve the performance at higher frequencies. However it is difficult to achieve a zero Z_{gg} due to the non-zero resistivity of interconnects. Using the proposed model achievable values of Z_{gg} can be included in the calculation, which is useful to obtain more accurate predictions of the noise suppression performance.

V. CONCLUSION

This paper presents a compact P^+ guard ring model for substrate noise analysis. Different from existing compact models, the proposed model can handle P^+ guard rings implemented using lightly doped CMOS substrates with a P-well layer. The model is scalable to guard ring parameters and requires no fitting factors. Based on the proposed model the substrate noise suppression performance of P^+ guard rings in terms of S-parameters can be efficiently predicted in a broad frequency band up to at least 10 GHz. The model has been validated by EM simulations and experimental measurements using a standard 0.18 μm CMOS process. In addition, design guidelines of P^+ guard rings have been provided to miniaturize the chip area occupied by guard rings, while maintaining a desired noise suppression level. The

approach used to obtain the model of P^+ guard rings in this paper can also be helpful for other guard ring designs such as N^+ guard rings.

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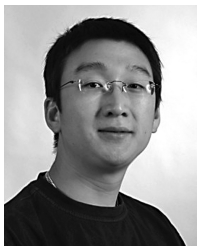

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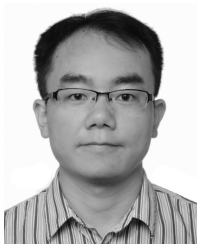

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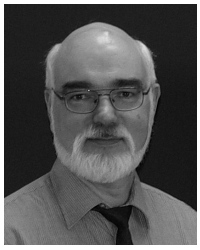

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