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A CMOS Power Amplifier using Ground Separation Technique

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***Abstract*— This work presents an on-chip ground separation technique for power amplifiers. The ground separation technique is based on separating the grounds of the amplifier stages on the chip and thus any parasitic feedback paths are removed. Simulation and experimental results show that the technique makes the amplifier less sensitive to bondwire inductance, and consequently improves the stability and performance.**

A two-stage CMOS RF power amplifier for WCDMA mobile phones is designed using the proposed on-chip ground separation technique. The power amplifier is fabricated in a $0.25\,\mu$m CMOS process. It has a measured 1-dB compression point between 1920MHz and 1980MHz of 21.3 ± 0.5dBm with a maximum PAE of 24%. The amplifier has sufficiently low ACLR for WCDMA (-33 dB) at an output power of 20 dBm.

I. Introduction

Most modern digital modulation forms with high spectral efficiency present a varying envelope, which requires RF circuits with high linearity to prevent signal degradation. Efficient but nonlinear power amplifiers are thus not suitable for such linear modulations. The use of linearization techniques can help alleviate this issue, but at the price of high complexity and additional power consumption, which may be critical in the case of low or medium power amplifiers [1]. In order to satisfy the linearity requirement for preserving modulation accuracy with minimum spectral regrowth, such power amplifiers are typically operated in highly linear Class-A or Class-AB configurations. However, high linearity, particularly in CMOS technology, comes at the cost of poor efficiency. Stability requirements place restrictions on PA characteristics, and limitations of CMOS technology such as low breakdown voltage introduce additional challenges for PA realization.

Stability is a key issue in amplifier design. RF oscillations are especially common in single-ended multi-stage designs [2]. The instability occurs when some of the output energy is fed back to the input port with a phase that makes negative resistance appear at the output or input of the amplifier [3]. Ground bounce inductance plays an important role on the amplifier stability. If all stages in a multi-stage amplifier share the same on-chip ground, they will also share the same inductance to PCB ground. Signal current in the output stage converted to voltage by this inductance will thus be fed back to the input with a risk of instability. Using the proposed ground separation technique this feedback path is removed.

The paper is organized as follows: In Section II, the brief design procedure of the amplifier is given, and then interconnection models of the amplifier are investigated. How the amplifier performance improved with ground separation is also discussed in this section. Simulation and measurement results demonstrating the PA performance are offered in Section III. Section IV describes the chip layout, and Section V concludes.

II. Circuit Design

The reported amplifier is designed as a single-ended two stage common source amplifier. It is biased in Class-AB to get high linearity and reasonable efficiency. Simulations are performed using the $0.25\ \mu$m CMOS process library components with Agilent-ADS. Figure 1 shows the schematic of the CMOS PA which is designed to operate from a single 2.5 V supply.

A. Core Amplifier

To achieve about 23 dBm output power with a 2.5 V supply, a transistor width of $2870\,\mu$m was used in the output stage. The estimation of the required transistor size is an iterative process using the DC characteristics of the transistor. The length of the transistor was set to minimum ($0.24\ \mu$m) to maximize its high frequency gain. The load impedance for optimum power output was determined to approximately $10-j11\,\Omega$. The gate bias voltage was set to 0.75 V in the output stage.

The driver stage transistor size is established after simulation of the output stage. To ensure that the driver stage doesn't enter saturation before the output stage, a transistor width of $1120\,\mu$m was chosen. The bias voltage for the driver stage was set to 0.85 V.

The input and output matching networks were designed using passive network synthesis techniques to achieve optimum VSWR characteristics over the desired frequency band ($1920-1980$ MHz). An output impedance transformation network including the MOS output capacitance and interconnection elements (bond wires, pad capacitances, and PCB board traces) is designed to transform the $50\,\Omega$ load into the $10-j11\,\Omega$ optimum load. The network includes the MOS output capacitance, 6 nH off-chip load inductance, 6 pF on-chip DC blocking capacitance, and interconnection elements (see Figure 1).

To improve the stability and performance of the amplifier, driver and output stage grounds are separated on the chip. This is described in more detail in the following section.

B. Interconnection Models

In the circuit simulations, two interconnection models are used; one is from chip signal/bias pad to PCB signal/bias pad,

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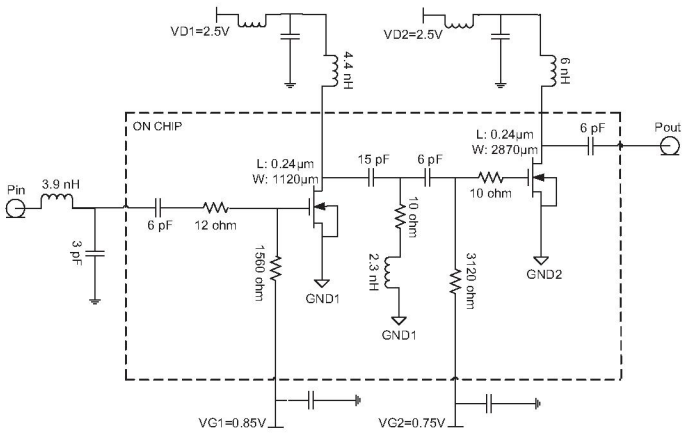

Fig. 1. Schematic of the CMOS power amplifier.

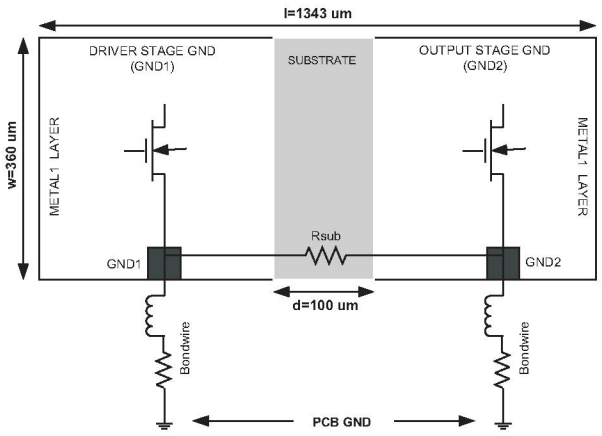

Fig. 3. Interconnection model for chip ground pad to PCB ground pad.

and the other is from chip ground pad to PCB ground pad. These models are shown in Figures 2 and 3. The models are suitable for the chip-on-board technique used in the measurements.

The inductance value of the bondwires is assumed to equal approximately 1 nH/mm [4]. Multiple bondwires are used in order to reduce the bondwire inductance both in output and ground connections. It is assumed that three parallel connected bondwires has about 0.4 nH/mm inductance [5].

On the chip, 85 μm $\times$ 85 μm pads are used for all connections. The shunt capacitance of a single pad was found to be approximately 65 fF in prior measurements. The PCB track capacitance was roughly estimated to 1.5 pF for simulations.

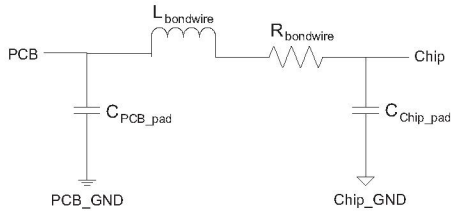

Fig. 2. Interconnection model for chip signal/bias pad to PCB signal/bias pad.

Figure 3 shows the interconnection model for chip ground pad to PCB ground pad. Different chip grounds are assigned for driver and output stages, GND1 and GND2. PCB ground is assumed to be a perfect ground and is denoted by GND. Driver and output stage grounds are isolated from each other by the substrate resistivity.

Investigations showed that when driver and output stage grounds are separated, the stability and performance were improved. Figure 4 shows the simulated stability factor of the amplifier with and without ground separation. As can be seen the PA with the ground separation technique is stable, whereas without the technique the amplifier is potentially unstable and malfunctioning.

To quantify the stability of the amplifier, the Rollet Stability criteria is used. The Rollet Stability criteria can be expressed

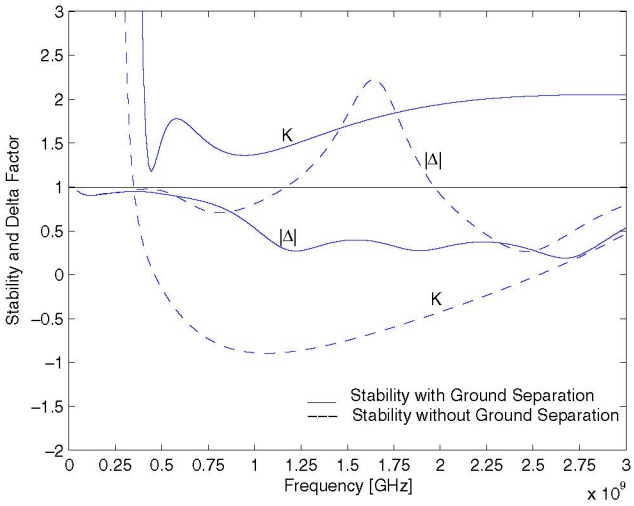

Fig. 4. Simulated stability factor with and without ground separation technique.

as follows [6]:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{1}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \tag{2}$$

- Stable: $K > 1$ and $|\Delta| < 1$
  - Unconditionally stable:

$$||c_s| - r_s| > 1 \text{ for } |S_{22}| < 1 \tag{3}$$

$$||c_l| - r_l| > 1 \text{ for } |S_{11}| < 1 \tag{4}$$

  - Conditionally stable:

$$||c_s| - r_s| < 1 \text{ for } |S_{22}| < 1 \tag{5}$$

$$||c_l| - r_l| < 1 \text{ for } |S_{11}| < 1 \tag{6}$$

- Unstable (potentially): $K > 1$ & $|\Delta| > 1$ and $K < 1$ & $|\Delta| < 1$,

where c_s, c_l, r_s, and r_l parameters represent the center and radius of the source and load stability circles respectively.

Simulations show that 12 Ω resistance between GND1 and GND2 is enough to sufficiently isolate them from each other. In the 0.25 μm CMOS process, the substrate resistivity (R) is 20 $\Omega \cdot$ cm and the substrate thickness (T) is 29 mils. The substrate resistance between GND1 and GND2 can be roughly estimated using the formula:

$$R_{Sub} = R[\Omega \cdot \mathrm{m}] \times \frac{d[\mathrm{m}]}{A[\mathrm{m}^2]}, \tag{7}$$

where the substrate distance (d) between the GND1 and GND2 is 100μm (See Figure 3) and the substrate cross-section area (A) can be found as follow:

$$A = T[\mathrm{m}] \times W[\mathrm{m}] = 36 \times 10^{-9}\mathrm{m}^2, \tag{8}$$

where the chip width (W) is 360 μm. Using Eq. (7), the resistance (R_{Sub}) between GND1 and GND2 is roughly estimated to 76 Ω, which is much larger than the 12 Ω which is needed. This means that the simple calculation is sufficient in this case, and that there will be no problem to achieve the isolation.

III. Simulation and Measurement Results

The CMOS power amplifier was tested using chip on board assembly. Measurements were performed to find the S-parameters, 1-dB compression point, power added efficiency (PAE), third order intercept point (IP3), adjacent channel leakage ratio (ACLR), and error vector magnitude (EVM).

A. Frequency Response

The measured and simulated forward and reverse gain characteristics ($|S_{21}|$ & $|S_{12}|$) and input and output reflection characteristics ($|S_{11}|$ & $|S_{22}|$) of the PA are shown in Figures 5 and 6. In Table I, some measured values in the WCDMA band are listed.

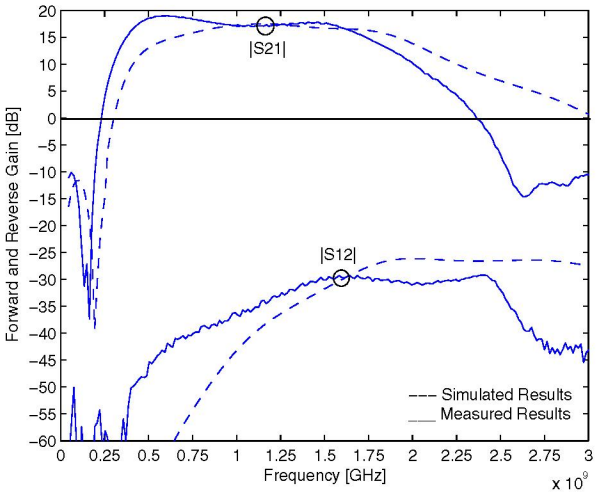

Fig. 5. Simulated and measured forward and reverse gain characteristics.

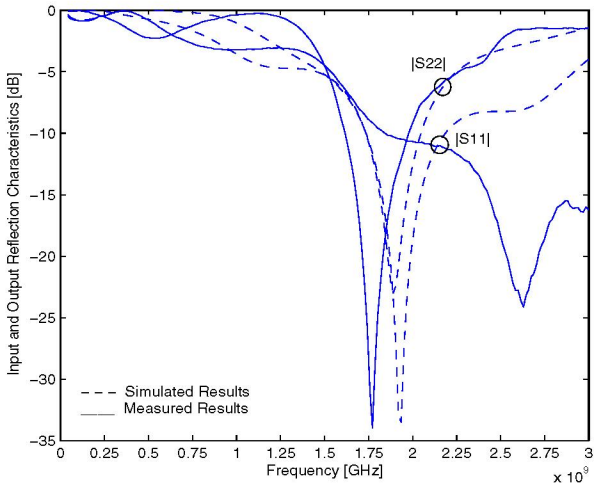

Fig. 6. Simulated and measured input and output reflection characteristics.

TABLE I
Measured S-parameters in the WCDMA Band.

Freq. [MHz]	$\lvert S_{21}\rvert$ dB	$\lvert S_{11}\rvert$ dB	$\lvert S_{22}\rvert$ dB
1920	11.8	−10.4	−12.7
1950	11.2	−10.5	−11.4
1980	10.7	−10.6	−10

While the simulated gain is 14dB at 1.95GHz, the measured gain is only 11.2 dB. Differences between simulation and measurement results are due to imperfections of parasitic models used in simulations, on-chip and off-chip component tolerances, and also measurement inaccuracy.

B. Efficiency

The measured 1-dB output compression point is 21.8 dBm with 24% PAE at 1920 MHz, it is 20.8 dBm with 20.4% PAE at 1950 MHz, and it is 21.4 dBm with 22.4% PAE at 1980 MHz. At the compression point, the current drawn from the 2.5 V supply voltage is 232 mA, 216 mA, and 222 mA respectively. The simulated 1-dB compression point at 1950 MHz is 22.7 dBm with 32% PAE. The difference between the simulated and measured results is related to the measured gain being lower than the simulated one. Simulated and measured PAE are illustrated in Figure 7.

C. Linearity

The linearity performance of the amplifier was analyzed according to the WCDMA/3GPP user equipment requirements [7]. Third order output intercept point (OIP_3), ACLR, and EVM measurements are performed.

For two-tone measurement the frequencies (tones) are set at $f_c \pm 500$ kHz. The measured third order intercept points are 30.9 dBm, 30 dBm, and 30.1 dBm for 1920 MHz, 1950 MHz, and 1980 MHz center frequencies.

In Figure 8, ACLR measurement is illustrated. The measurement has been performed at 1950 MHz with 20 dBm PA output power.

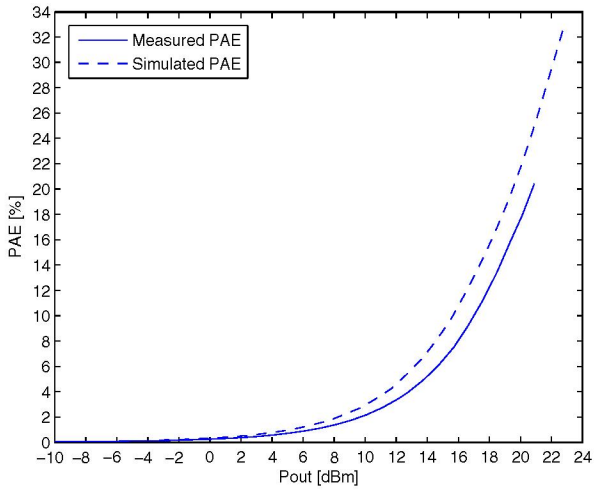

Fig. 7. Simulated and measured power added efficiency.

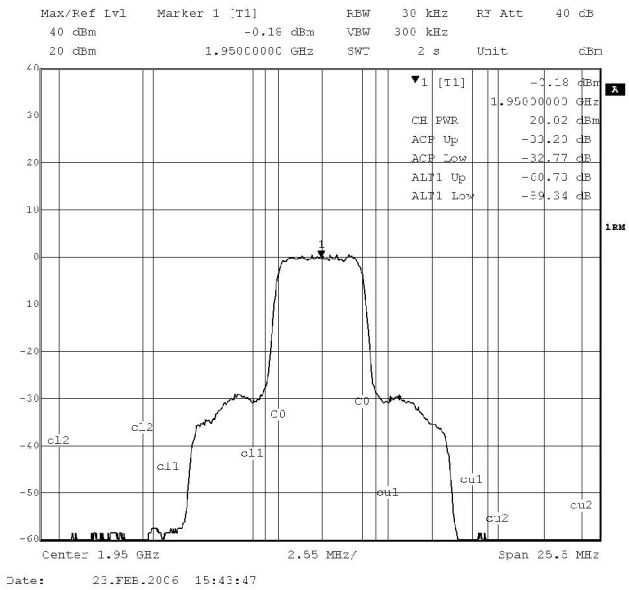

Fig. 8. The ACLR performance of the amplifier output signal.

In Table II, all measured results are listed and compared to system requirements. In WCDMA 3GPP UE document, transmitter characteristics are specified at the antenna connector of the UE. There will likely be some devices between the PA output and the antenna terminals such as circulator, duplex filter, and switch(es) with several dB of loss. When making the comparison, these losses also have to be taken into account.

IV. Chip Layout

A microphotograph of the CMOS PA is shown in Figure 9. The chip was fabricated in a $0.25\,\mu$m 2.5 V single poly 5-metal layer (1P5M) CMOS technology. The chip size is 1343 μm $\times$ 360 μm. Driver and output stage layouts are separated with 100 μm distance. Each block is connected to PCB ground with different GND pads. Ground separation increases the overall

TABLE II

Measured performance and WCDMA/3GPP Specifications.

Parameter	Measured	WCDMA/3GPP Specs
Output Power & PAE		Class 3:
1920 MHz	21.8 dBm & 24%	23dBm $+1/-3$dB
1950 MHz	20.8 dBm & 20.4%	Class 4:
1980 MHz	21.4 dBm & 22.4%	21dBm $\pm$2dB
ACLR Performance		
1950 $\pm$5MHz	-33.2 dB	< -33 dB
1950 $\pm$10MHz	-60.7 dB	< -43 dB
RMS EVM	4%	$< 17.5\%$
Peak EVM	10.7%	

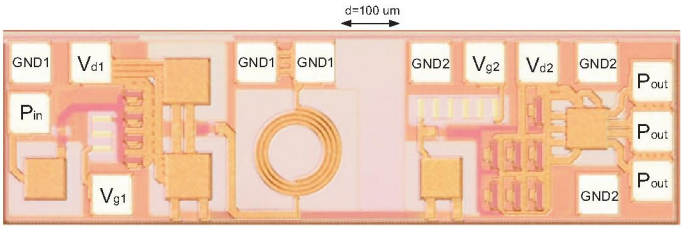

Fig. 9. Die photo.

area of the chip with 0.036 mm^2.

V. Conclusion

The inductance of the ground bondwires is one of the most serious problems in single-ended integrated amplifier design. The inductance creates parasitic feedback which can cause the amplifier to self-oscillate. In this work it is demonstrated that the parasitic feedback path can be broken using a ground separation technique, and consequently amplifier's stability and performance can be improved.

To demonstrate the technique, a CMOS RF power amplifier with ground separation has been realized. With 2.5 V supply voltage, 21.3 $\pm$ 0.5 dBm output power with maximum 24% PAE, and a good linearity were measured. At 20dBm it fulfills the WCDMA/3GPP requirements on ACLR and EVM.

VI. Acknowledgment

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