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Embedded EZ-Source Inverters

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***Abstract*— Z-source inverters are recent topological options proposed for buck-boost energy conversion with a number of possible voltage and current-type circuitries already reported in the literature. Comparing them, a common feature noted is their inclusion of a LC impedance network, placed between the dc input source and inverter bridge. This impedance network allows the output end of a voltage-type Z-source inverter to be shorted for voltage-boosting without causing a large current flow, and the terminal current of a current-type inverter to be interrupted for current boosting without introducing over-voltage oscillations to the system. Therefore, Z-source inverters are in effect safer and less complex, and can be implemented using only passive elements with no additional active semiconductor needed. Believing in the prospects of Z-source inverters, this paper contributes by introducing a new family of embedded EZ-source inverters that can produce the same gain as the Z-source inverters, but with smoother and smaller current / voltage maintained across the dc input source and within the impedance network. These latter features are attained without using any additional passive filter, which surely is a favorable advantage since an added filter will raise the system cost, and at times can complicate the dynamic tuning and resonant consideration of the inverters. The same embedded concept can also be used for designing a full range of voltage and current-type inverters with each of them tested experimentally using a number of scaled down laboratory prototypes.**

Keywords-EZ-source inverters; Z-source inverters; neutral-point-clamped inverters; pulse-width-modulation

I. INTRODUCTION

Z-source inverters, first proposed in [1] and drawn in Fig. 1(a), are viewed as a new class of single-stage converters that can perform buck-boost energy conversion using only a simple LC impedance network. To date, various Z-source topological options have since been developed with either voltage or current-type conversion ability [1, 2]. Among them, the voltage-type inverters are more popular with them tested for applications in motor drives, photovoltaic and fuel cell powered systems, where the dc voltages generated by the sources are constantly varying, determined solely by the prevailing atmospheric conditions (e.g. intensity of solar irradiation). Although traditional voltage-source inverters (VSIs) can also be used for such applications, their sole voltage step-down operation forces them to operate at a relatively low modulation depth, and hence poor harmonic performance in most cases. The reason for using a low nominal operating ratio is because their upper modulation range must be reserved for riding through any surge in energy demand. On the other hand, Z-source inverters can be designed with their maximum modulation ratio set to the prevailing nominal case. Any surge in energy demand is then managed by varying the inverter shoot-through time duration, which in effect is a third state introduced for gaining voltage boosting in Z-source inverters, in addition to their voltage-buck operation inherited from traditional VSI.

For controlling the Z-source inverters, many pulse-width modulation schemes [3, 4] have also been reported with some achieving a lower switching loss and others realizing an optimized harmonic performance. Although these schemes do have some differences in features, they are mostly developed by introducing shoot-through states to the traditional VSI state sequences with more states likely to surface under low load or small inductance conditions [5]. The added states are shown to influence the produced voltage gain, which is now load-dependent, and therefore harder to control. For minimizing this load influence, proper parametric tuning must be done to minimize the amount of high frequency current ripple within the circuit when compared with the supplied load level. Although effective in stabilizing the gain, parametric tuning cannot remove the chopping current flowing into the dc source, which might degrade the source characteristic response. The reason for its ineffectiveness is linked to the high frequency operation of the input diode D, shown in Fig. 1(a), during voltage-boost operation, which no doubt can be filtered by placing a second order LC filter before D. But including an additional filter might raise the overall cost of the system slightly, and might introduce unnecessary dynamic and resonant complications to the system if not designed properly. The dual scenario is also experienced by the current-type Z-source inverters, where now a chopping voltage is imposed across the input current source. The chopping voltage can again be filtered by introducing a second order LC filter with the same dynamic and resonant complications experienced if not implemented correctly.

Therefore, instead of using an external LC filter, this paper proposes an alternative family of embedded Z-source (referred to as EZ-source in short) inverters, which adopts the concept of embedding the input dc sources within the LC impedance network, using its existing inductive elements for current filtering in voltage-type EZ-source inverters, and its capacitive elements for voltage filtering in current-type EZ-source inverters. Despite these modifications, the voltage or current gain of the inverters is kept unchanged, as can be proven

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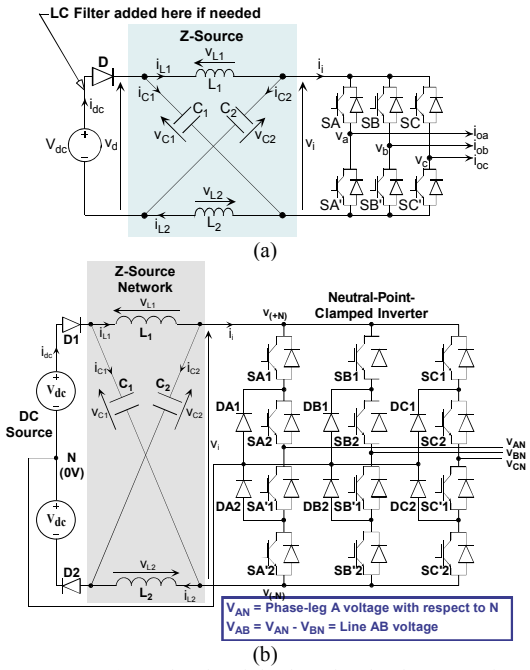

Fig. 1. Z-source (a) two-level and (b) three-level voltage-type inverters.

mathematically. The proposed EZ-source inverters are therefore competitive alternatives that can be used for cases, where implicit source filtering is critical. The concepts have been tested extensively in the laboratory using experimentally constructed two-level and three-level neutral-point-clamped (NPC) inverters.

II. Voltage-Type Z-Source Inverters

A. Two-Level Voltage-Type Inverter

The two-level voltage-type Z-source inverter is shown in Fig. 1(a), where a X-shaped LC impedance network is connected between the input dc source and three-phase inverter bridge. With the impedance network added, any two switches from the same phase-leg can now be turned ON safely to introduce a shoot-through or short-circuit state with no surge in current observed since all current paths in the dc front-end are effectively limited by at least an inductive element (L_1, L_2 or both). In response to the inserted shoot-through state, the Z-source inverter can then be proven to exhibit voltage-boosting capability, whose corresponding gain expression is derived by considering the inverter state equations during shoot-through and non-shoot-through states, expressed from (1) to (4) with a balanced network assumed ($L_1 = L_2 = L$ and $C_1 = C_2 = C$). Note that for the case of non-shoot-through state, it can represent any of the six traditional active states ($i_i \neq 0$) or the remaining two null states ($i_i = 0$), solely determined by the modulation process.

Shoot-Through (Sx = Sx' = ON, x = A, B or C; D = OFF)

$$v_L = V_C\ ;\ v_i = 0\ ;\ v_d = 2V_C\ ;\ v_D = V_{dc} - 2V_C \tag{1}$$

$$i_L = -i_C\ ;\ i_i = i_L - i_C\ ;\ i_{dc} = 0 \tag{2}$$

Non-Shoot-Through (Sx ≠ Sx', x = A, B or C; D = ON)

$$v_L = V_{dc} - V_C\ ;\ v_i = 2V_C - V_{dc}\ ;\ v_d = V_{dc}\ ;\ v_D = 0 \tag{3}$$

$$i_{dc} = i_L + i_C\ ;\ i_i = i_L - i_C\ ;\ i_{dc} \neq 0 \tag{4}$$

Performing state-space averaging on (1) and (3) then results in the following expressions derived for the capacitive voltage V_C, peak dc-link voltage $\hat{v}_i$ and peak ac output voltage $\hat{v}_x$ (the latter two happen during the non-shoot-through state).

$$V_C = \frac{1 - T_0/T}{1 - 2T_0/T} V_{dc}\ ;\ \hat{v}_i = \frac{V_{dc}}{1 - 2T_0/T} = BV_{dc}$$

$$\hat{v}_x = M\frac{\hat{v}_i}{2} = B\left(M\frac{V_{dc}}{2}\right) \tag{5}$$

where T_0/T refers to the shoot-through ratio ($T_0/T < 0.5$) per switching period, M represents the modulation index used for traditional inverter control, and $B = 1/(1\text{-}2T_0/T)$ is the boost factor. Clearly, the term enclosed by the parentheses in the expression for $\hat{v}_x$ represents the output amplitude produced by a traditional VSI, which can be boosted by raising B above unity and adjusting M accordingly. In addition to (5), other expressions governing the voltage-type Z-source inverter operation can be written as:

Diode Blocking Voltage

$$v_D = -V_{dc}/(1 - 2T_0/T) \tag{6}$$

Inductor Voltage

$$\begin{cases} v_L = V_{dc}(1 - T_0/T)/(1 - 2T_0/T), & \text{during shoot - through} \\ v_L = -V_{dc}(T_0/T)/(1 - 2T_0/T), & \text{during non - shoot - through} \end{cases} \tag{7}$$

B. Three-Level Voltage-Type Inverter

Extending from the two-level voltage-type inverter, expressions for the three-level Z-source NPC inverter shown in Fig. 1(b) can similarly be derived by applying state space averaging to give:

Full-Shoot-Through (Sx1 = Sx2 = Sx'1 = Sx'2 = ON, x = A, B or C; D1 = D2 = OFF)

$$v_L = V_C\ ;\ v_i = 0\ ;\ v_D = V_{dc} - V_C \tag{8}$$

$$i_L = -i_C\ ;\ i_i = i_L - i_C\ ;\ i_{dc} = 0 \tag{9}$$

Upper-Shoot-Through (Sx1 = Sx2 = Sx'1 = Dx2 = ON, x = A, B or C; D1 = ON, D2 = OFF)

$$v_L = V_{dc}\ ;\ v_i = V_C - V_{dc}\ ;\ v_D = V_{dc} - V_C \tag{10}$$

Lower-Shoot-Through (Sx2 = Sx'1 = Sx'2 = Dx1 = ON, x = A, B or C; D1 = OFF, D2 = ON)

$$v_L = V_{dc}\ ;\ v_i = V_C - V_{dc}\ ;\ v_D = V_{dc} - V_C \tag{11}$$

Non-Shoot-Through (Sx1 ≠ Sx'1, Sx2 ≠ Sx'2, x = A, B or C; D1 = D2 = ON)

$$v_L = 2V_{dc} - V_C\ ;\ v_i = 2V_C - 2V_{dc}\ ;\ v_D = 0 \tag{12}$$

$$i_{dc} = i_L + i_C\ ;\ i_i = i_L - i_C\ ;\ i_{dc} \neq 0 \tag{13}$$

where the middle two states are new states specially associated with the Z-source NPC inverter [6], whose current expressions are not written explicitly because of their asymmetrical current flow. Also noted from [6] is that two modulation schemes for controlling the Z-source NPC inverter are available with the first (FST) using only the full and non-shoot-through states, and the second (ULST) using only upper,

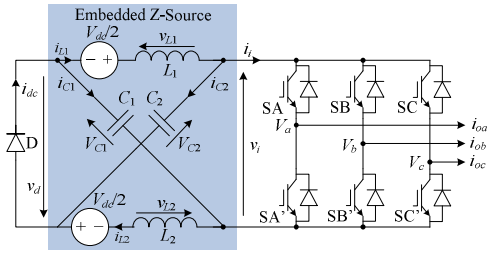

Fig. 2. Two-level embedded EZ-source inverter.

lower and non-shoot-through states. For the latter, an additional factor to note is that the time durations assumed by the upper and lower shoot-through states must be equal so as to balance out the dc symmetrical impedance network. Performing state space averaging on these two modulation methods then gives rise to:

Full-Shoot-Through Scheme

$$V_C = \frac{2V_{dc}\left(1-T_0/T\right)}{1-2T_0/T}$$

$$\hat{v}_i = \frac{2V_{dc}}{1-2T_0/T} = 2BV_{dc}\ ;\ \hat{v}_x = M\,\hat{v}_i/2 = MBV_{dc}$$

$$v_D = -V_{dc}/(1-2T_0/T)$$

$$\begin{cases} v_L = 2V_{dc}(1-T_0/T)/(1-2T_0/T), & \text{during shoot - through} \\ v_L = -2V_{dc}(T_0/T)/(1-2T_0/T), & \text{during non - shoot - through} \end{cases} \tag{14}$$

Upper and Lower Shoot-Through Scheme

$$V_C = \frac{2V_{dc}\left(1-T_0'/(2T)\right)}{1-T_0'/T}$$

$$\hat{v}_i = \frac{2V_{dc}}{1-T_0'/T} = 2B'V_{dc}\ ;\ \hat{v}_x = M\,\hat{v}_i/2 = MB'V_{dc}$$

$$v_D = -V_{dc}/(1-T_0'/T)$$

$$\begin{cases} v_L = V_{dc}, & \text{during upper or lower - shoot - through} \\ v_L = -V_{dc}(T_0'/T)/(1-T_0'/T), & \text{during non - shoot - through} \end{cases} \tag{15}$$

where T_0'/T represents the normalized sum of upper and lower-shoot-through state durations, whose value must be set to $T_0'/T = 2T_0/T$ to produce the same boost factor and diode blocking voltage for the two Z-source NPC modulation schemes ($B = B'$). Although not that obvious, an advantage noted with this second scheme is that its inductive current ripple in the impedance network is expected to be lower, which can easily be proven by writing down the ratio of inductive current increments ΔI_L for the two schemes during the shoot-through interval:

$$\frac{(\Delta I_L)_{ULST}}{(\Delta I_L)_{FST}} = \frac{T_0'(1-2T_0/T)}{2(1-T_0/T)T_0} = \frac{1-2T_0/T}{1-T_0/T} \le 1$$
$$\text{for} \quad T_0/T = T_0'/(2T) \le 0.5 \tag{16}$$

Having a smaller inductive current ripple would then allow the ULST-controlled Z-source inverter to remain longer in the typical shoot-through and non-shoot-through states without entering those atypical states deduced from [5]. To be more specific, those atypical modes surface only upon either diode

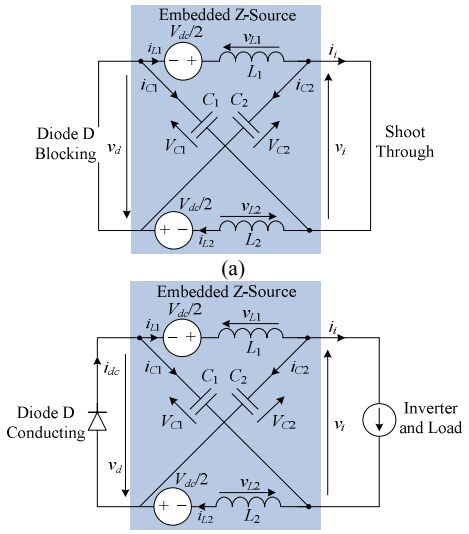

Fig. 3. Equivalent circuits of two-level EZ-source inverter when in (a) shoot-through and (b) non-shoot-through states.

D1 or D2 (or both) becomes reverse-biased even when in the non-shoot-through state. This happens when $i_{dc} = i_{L1} + i_{C1} = i_{L1} + (i_{L2} - i_i) = 2i_L - i_i \le 0$, implying $i_L \le 0.5 i_i$, which obviously will be reached earlier by the FSL scheme because of its higher ripple content, assuming the same average inductive current is flowing for both schemes. In brief, it is also commented that the mathematical proving of a lower ripple or harmonic content for the ULST scheme in (16) has not been previously demonstrated. Although the lower harmonic content of the ULST scheme has qualitatively been mentioned by the authors in [6], it is based solely on classical three-level modulation theory, which does not provide a quantitative foundation needed for further analysis, unlike that expressed in (16).

III. Voltage-Type EZ-Source Inverters

A. Two-Level Voltage-Type Inverter

Comparing with Fig. 1(a), the voltage-type EZ-source inverter shown in Fig. 2 has its dc sources embedded within the X-shaped LC impedance network with its inductive elements L_1 and L_2 now respectively used for filtering the currents drawn from the two dc sources without using any external LC filter. Quite obviously, the immediate disadvantage noted from Fig. 2 is that two dc-sources of $V_{dc}/2$, instead of the single dc source in Fig. 1(a), are needed for the EZ-source inverter. Although this requirement can at times translate to a slightly higher cost, it is not a major issue for photovoltaic or even fuel cell applications, where the Z-source inverter is originally designed for usage, since the isolated sources can simply be obtained by re-routing the existing panels or cell units already needed for producing the required voltage and current ratings. Therefore, it is not viewed as a serious limitation (and in fact is not a limitation for the NPC EZ-source inverter discussed in Section III(B)), and can definitely be outweighed by advantages exhibited by the EZ-source inverter, including its inherent filtering ability. These advantages are more clearly illustrated by analyzing the inverter operating principle, which again

involves shoot-through and non-shoot-through states produced by a modulator that can equally be used for controlling EZ-source and Z-source inverters.

Noting that there is again an inductive element placed along all current paths in the dc front-end, the switches from the same phase-leg can as usual be turned ON simultaneously to introduce a shoot-through state without damaging semiconductor devices. The resulting equivalent circuit is shown in Fig. 3(a), where it is shown that when the inverter bridge is shot through, the front-end diode D is reverse biased with its blocking voltage expression and other state equations written as:

Shoot-Through (Sx = Sx' = ON, x = A, B or C; D = OFF)

$$v_L = V_C + V_{dc}/2\ ;\ v_i = 0\ ;\ v_d = v_D = -2V_C \tag{17}$$

$$i_L = -i_C\ ;\ i_i = i_L - i_C\ ;\ i_{dc} = 0 \tag{18}$$

Assuming now that the inverter returns back to its non-shoot-through active or null state, the redrawn equivalent circuit is shown in Fig. 3(b) with diode D conducting, and the inverter bridge and external (usually inductive) load replaced by a current source, whose value is non-zero for active state and zero for null state. Using this equivalent circuit, the second set of state equations is derived as:

Non-Shoot-Through (E.g. Sx ≠ Sx', x = A, B or C; D = ON)

$$v_L = V_{dc}/2 - V_C\ ;\ v_i = 2V_C\ ;\ v_d = v_D = 0 \tag{19}$$

$$i_{dc} = i_L + i_C\ ;\ i_i = i_L - i_C\ ;\ i_{dc} \neq 0 \tag{20}$$

Performing state space averaging then results in:

$$V_C = \frac{V_{dc}/2}{1 - 2T_0/T}$$

$$\hat{v}_i = \frac{V_{dc}}{1 - 2T_0/T} = BV_{dc}\ ;\ \hat{v}_x = M\frac{\hat{v}_i}{2} = B\left(M\frac{V_{dc}}{2}\right) \tag{21}$$

where (21), when compared with (5), clearly shows that both Z-source and EZ-source inverters produce the same transfer gain even though the EZ-source inverter has its dc sources embedded within the impedance network for achieving inherent filtering. Observing carefully, a second advantage is also noted in (21), when comparing its capacitive voltage V_C with that expressed in (5). To be specific, V_C in (21) is only a fraction of that in (5) with their ratio mathematically expressed as:

$$\frac{V_{C(21)}}{V_{C(5)}} = \frac{1}{2(1 - T_0/T)} \tag{22}$$

where the subscripts in (22) represent the numberings of the respective V_C expressions. Noting that T_0/T is always smaller than 0.5, the ratio in (22) is calculated to span from 0.5 to 1 as T_0/T rises from 0 to 0.5, inferring that the second advantage introduced by embedding the sources is a significant reduction of the capacitor sizing (voltage rating). The reduction is as much as 50% under nominal condition during which M is set close to unity (or 1.15 if triplen offset is injected) and T_0/T is kept small. Qualitatively, the gaining of this favorable feature can also be explained by understanding that the embedded sources now help to partially maintain the needed voltage level within the impedance network, allowing the X-shaped

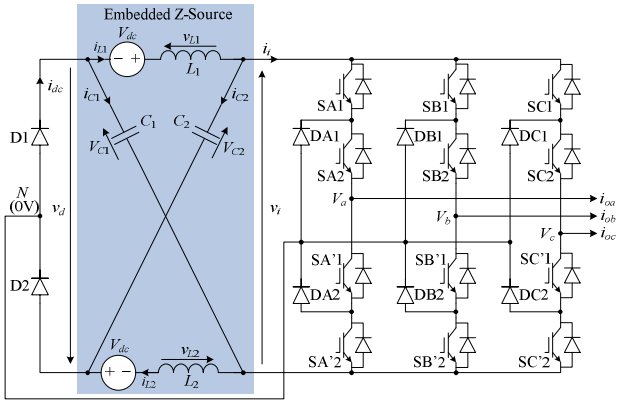

Fig. 4. Three-level embedded EZ-source inverter.

capacitors to carry a lower voltage than that found in the Z-source network reviewed in Section II.

Proceeding on to identify other characteristic features of the EZ-source inverter, (21) is substituted into (17) to (20) to derive the following set of additional equations.

Diode Blocking Voltage

$$v_D = -V_{dc}/(1 - 2T_0/T) \tag{23}$$

Inductor Voltage

$$\begin{cases} v_L = V_{dc}(1 - T_0/T)/(1 - 2T_0/T), & \text{during shoot - through} \\ v_L = -V_{dc}(T_0/T)/(1 - 2T_0/T), & \text{during non - shoot - through} \end{cases} \tag{24}$$

Comparing with (6) and (7), it is obvious that the EZ-source inverter does not need a diode with higher blocking voltage, and does not incur any changes to its inductive current ripple for the same commanded shoot-through duration T_0/T. Noting also that the average inductive current $I_L = I_i = I_{dc}$ (where uppercase "I" represents average value) is the same for both Z-source and EZ-source inverters, the same design criteria are expected to indifferently apply on them if those atypical modes stated in [5] are to be avoided.

B. Three-Level Voltage-Type Inverter

When the inverter bridge shown in Fig. 2 is replaced by a NPC bridge with slight modifications introduced, the EZ-source NPC inverter is developed with improved three-level output voltage switching. Viewing the NPC inverter in Fig. 4 and comparing it with its two-level precedent shown in Fig. 2, a unique feature observed with the NPC circuit is the inclusion of a second input diode (not source) for forming the point of neutral potential, to which all the clamping diodes are tied. Also noted in the figure is the same number of components and sources used by the EZ-source NPC inverter, as compared to its Z-source counterpart shown in Fig. 1(b). Therefore, unlike its two-level precedent, the EZ-source NPC inverter proposed here is not penalized to any extent since the same two sources are needed for both the EZ-source and Z-source networks with the only visible difference noted being their placements within their respective impedance networks. Needless to say, the sources of the EZ-source network are better filtered since they are embedded in series with the network inductances, unlike those of the Z-source inverter where chopping currents caused

by diode switching are expected to flow during voltage boosting operation.

In addition to that, other advantages of the EZ-source inverter can similarly be deduced by analyzing its state equations in four different topological states, named again as full-shoot-through, upper-shoot-through, lower-shoot-through and non-shoot-through states. For the full-shoot-through state, a number of methods is available for initiating it with the simplest being to turn ON all four switches from a phase-leg (SA1, SA2 SA'1 and SA'2) simultaneously to create a short-circuit across the inverter dc-link. The resulting circuit is shown in Fig. 5(a), where the two input diodes are indicated as reverse-biased. Using this equivalent circuit, the inverter state equations are then written as:

Full-Shoot-Through (Sx1 = Sx2 = Sx'1 = Sx'2 = ON, x = A, B or C; D1 = D2 = OFF)

$$v_L = V_C + V_{dc};\ v_i = 0;\ v_d = 2v_D = -2V_C \tag{25}$$

$$i_L = -i_C;\ i_i = i_L - i_C;\ i_{dc} = 0 \tag{26}$$

Instead of the full-shoot-through state, the inverter can assume either the upper or lower-shoot-through states with their equivalent circuits shown in Fig. 5(b) and (c). Analyzing these figures and noting that the upper-shoot-through state is initiated by turning ON (e.g.) SA1, SA2 and SA'1 with DA2 naturally ON to short the positive dc rail to the neutral terminal *N* (SA2=SA'1=SA'2=DA1=ON for lower-shoot-through), the resulting state equations for the voltages are written as:

Upper-Shoot-Through (Sx1 = Sx2 = Sx'1 = Dx2 = ON, x = A, B or C; D1 = ON, D2 = OFF)

$$v_L = V_{dc};\ v_i = V_C;\ v_d = v_D = -V_C \tag{27}$$

Lower-Shoot-Through (Sx2 = Sx'1 = Sx'2 = Dx1 = ON, x = A, B or C; D1 = OFF, D2 = ON)

$$v_L = V_{dc};\ v_i = V_C;\ v_d = v_D = -V_C \tag{28}$$

For the currents, no simple form of expressing them is available because of the asymmetry introduced to the impedance network when in these two partial shoot-through states. Performing the analysis once more for the non-shoot-through state then gives rise to the last set of state equations, expressed as:

Non-Shoot-Through (E.g. Sx1 ≠ Sx'1, Sx2 ≠ Sx'2, x = A, B or C; D1 = D2 = ON)

$$v_L = V_{dc} - V_C;\ v_i = 2V_C;\ v_D = 0 \tag{29}$$

$$i_{dc} = i_L + i_C;\ i_i = i_L - i_C;\ i_{dc} \neq 0 \tag{30}$$

Similar to the Z-source NPC inverter discussed in Section II, two modulation schemes, labeled as FST and ULST, can be used for controlling the EZ-source inverter. Performing state space averaging on both schemes then gives rise to the following gain and voltage expressions, written as:

Full-Shoot-Through Scheme

$$V_C = \frac{V_{dc}}{1 - 2T_0/T}$$

$$\hat{v}_i = \frac{2V_{dc}}{1 - 2T_0/T} = 2BV_{dc};\ \hat{v}_x = M\,\hat{v}_i/2 = MBV_{dc}$$

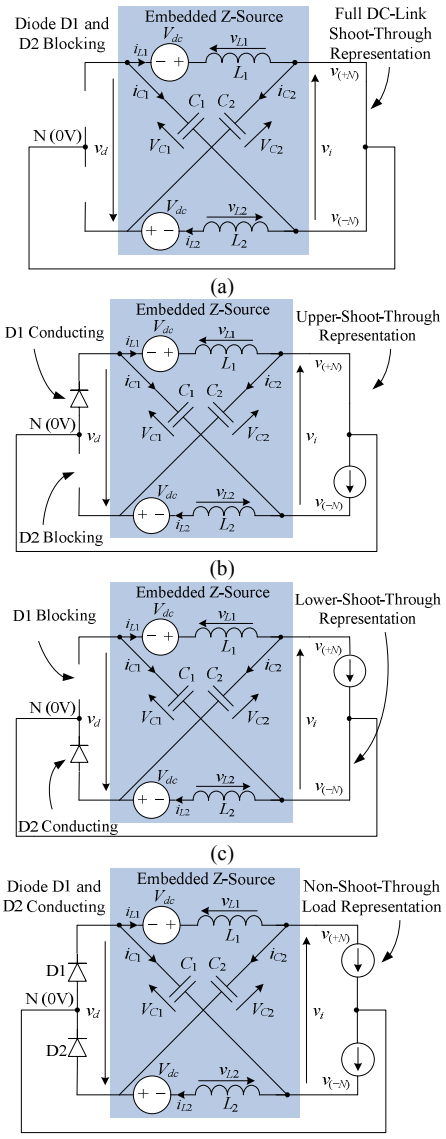

Fig. 5. Equivalent circuits of three-level EZ-source inverter when in (a) full-shoot-through, (b) upper-shoot-through, (c) lower-shoot-through and (d) non-shoot-through states.

$$v_D = -V_{dc}/(1 - 2T_0/T)$$

$$\begin{cases} v_L = 2V_{dc}(1 - T_0/T)/(1 - 2T_0/T), & \text{during shoot - through} \\ v_L = -2V_{dc}(T_0/T)/(1 - 2T_0/T), & \text{during non - shoot - through} \end{cases} \tag{31}$$

Upper and Lower Shoot-Through Scheme

$$V_C = \frac{V_{dc}}{1 - T_0'/T}$$

$$\hat{v}_i = \frac{2V_{dc}}{1 - T_0'/T} = 2B'V_{dc};\ \hat{v}_x = M\,\hat{v}_i/2 = MB'V_{dc}$$

$$v_D = -V_{dc}/(1 - T_0'/T)$$

$$\begin{cases} v_L = V_{dc}, & \text{during upper or lower - shoot - through} \\ v_L = -V_{dc}(T_0'/T)/(1 - T_0'/T), & \text{during non - shoot - through} \end{cases} \tag{32}$$

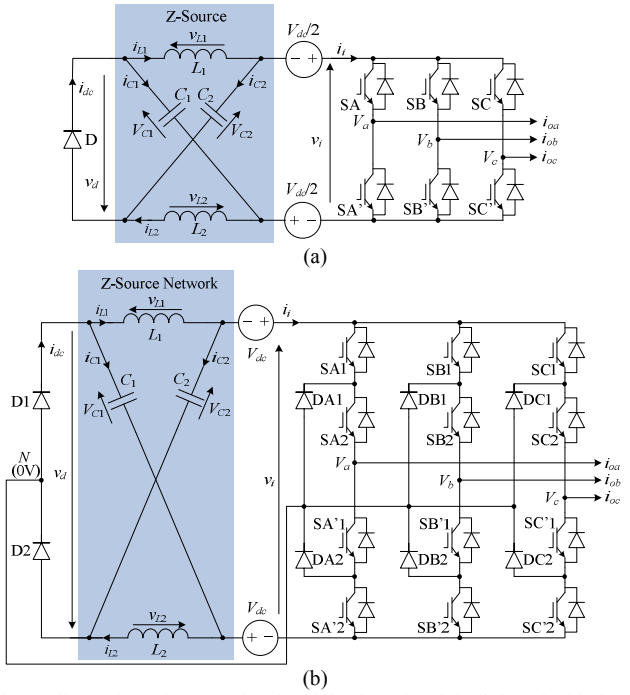

Fig. 6. Illustration of (a) two-level and (b) three-level dc-link embedded EZ-source inverters.

Using (31) and (32), the same ratio as in (16) can be derived for proving that the ULST scheme has a lower steady-state current ripple than the FST scheme even when used with the EZ-source impedance network. That again means that the chances of entering those atypical modes deduced from [5] are lower when the ULST scheme is used, assuming the same average inductive current is produced by both modulation schemes. In addition, by comparing (14) with (31) and (15) with (32), it is noted that the EZ-source NPC inverter needs to withstand a lower capacitive rated voltage V_C, which in effect is a factor of $1/(2(1-T_0/T)) = 1/(2(1-T_0'/(2T)))$ smaller than that of the Z-source inverter, regardless of whether the FST or ULST scheme is used. Clearly, this is an added advantage complementing the source filtering ability of the EZ-source network without compromising the inverter gain, diode blocking voltage, peak-to-peak current ripple of each modulation scheme, and overall component count. The family of EZ-source inverters presented here is therefore viewed as competitive variants that can be used in place of their Z-source counterparts depending on the particular cases under consideration.

IV. Voltage-Type DC-Link EZ-Source Inverters

Instead of embedding the dc sources within the impedance network, an alternative placement is shown in Fig. 6 for the two-level and three-level voltage-type inverters, where the dc sources are now embedded within the inverter dc-link (the dc sources in Fig. 6(a) can be replaced by a single source with voltage of V_{dc}, if desired). Operating these alternative dc-link EZ-source inverters based on the same modulation principles discussed in Section III would then lead to the same equivalent circuits shown in Fig. 3 and Fig. 5, except with their dc sources shifted to the inverter dc-link. Applying the same state-space averaging principles to the equivalent circuits would then

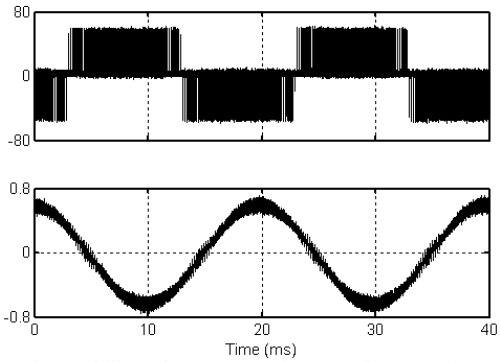

Fig. 7. Experimental line voltage (top) and current (bottom) of two-level EZ-source inverter with M=1.15×0.7 and T_0/T=0.

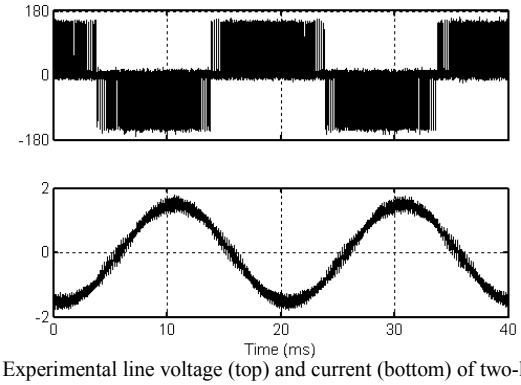

Fig. 8. Experimental line voltage (top) and current (bottom) of two-level EZ-source inverter with M=1.15×0.7 and T_0/T=0.3.

reveal that the same sets of equations derived in Section III for governing the EZ-source inverters can equally be applied to the dc-link EZ-source inverters, except for some differences in their capacitive voltages noted and expressed as:

Two-Level Voltage-Type Inverter

$$V_C = \frac{V_{dc}T_0/T}{1-2T_0/T} \tag{33}$$

Three-Level Voltage-Type Inverter

$$V_{C(FSL)} = \frac{2V_{dc}T_0/T}{1-2T_0/T};\quad V_{C(ULST)} = \frac{V_{dc}T_0'/T}{1-T_0'/T} \tag{34}$$

where the subscripts in (34) represent the modulation schemes considered. For a simple illustration of how the presented inverters compare with each other, the ratios among (5) for Z-source inverter, (21) for EZ-source inverter and (33) for dc-link EZ-source inverter are computed and expressed as:

$$\frac{V_{C(33)}}{V_{C(21)}} = \frac{2T_0}{T};\quad \frac{V_{C(33)}}{V_{C(5)}} = \frac{T_0/T}{1-T_0/T} \tag{35}$$

where $V_{C(33)}$ is observed to be the lowest among the three for T_0/T varying between 0 and 0.5. This obviously is an advantage but its prominence will diminish as T_0/T approaches 0.5. It also is attained at the expense of a noisier current drawn from the dc sources since no inductive element is now connected in series for filtering, and the choppy source current is now caused by the transition between active and null states, rather than between non-shoot-through and shoot-through states, meaning that it will flow even under no voltage-boost

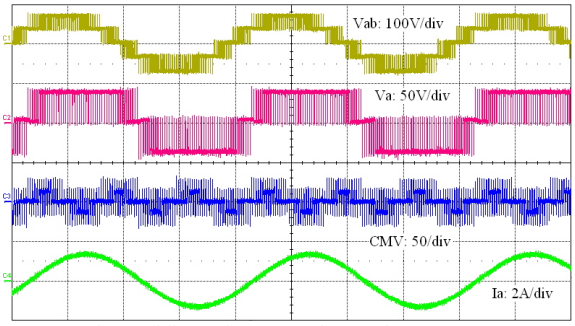

Fig. 9. Experimental line voltage V_{ab}, phase voltage V_a, common-mode voltage *CMV*, and line current I_a of ULST-controlled NPC EZ-source inverter with M=1.15 and T_0/T=0 (5 ms/div).

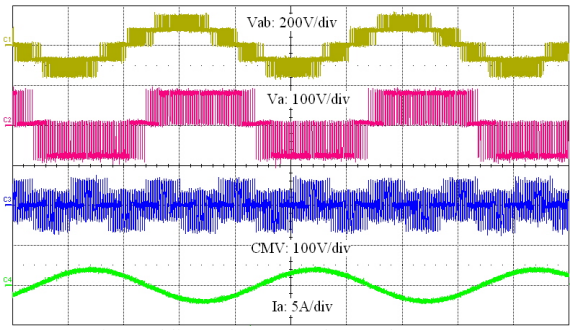

Fig. 10. Experimental line voltage V_{ab}, phase voltage V_a, common-mode voltage *CMV*, and line current I_a of ULST-controlled NPC EZ-source inverter with M=1.15×0.7 and T_0/T=0.3 (5 ms/div).

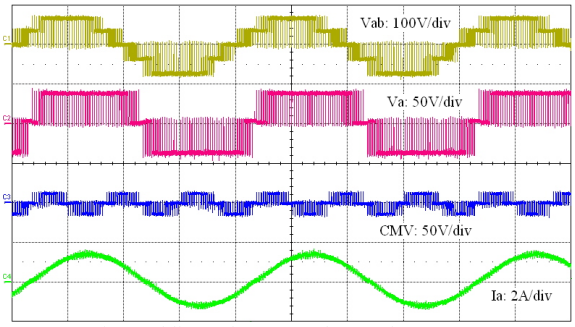

Fig. 11. Experimental line voltage V_{ab}, phase voltage V_a, common-mode voltage *CMV*, and line current I_a of FST-controlled NPC EZ-source inverter with M=1.15 and T_0/T=0 (5 ms/div).

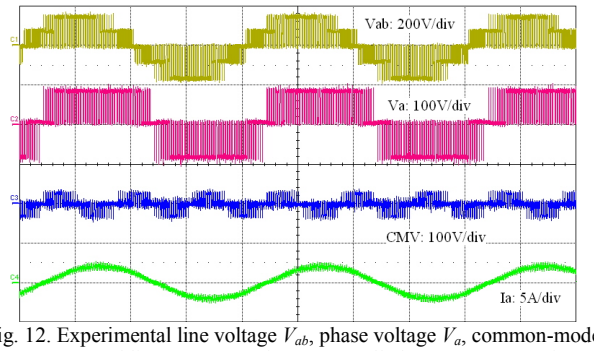

Fig. 12. Experimental line voltage V_{ab}, phase voltage V_a, common-mode voltage *CMV*, and line current I_a of FST-controlled NPC EZ-source inverter with M=1.15×0.7 and T_0/T=0.3 (5 ms/div).

condition. Last but not least, a less obvious feature that needs emphasis for the dc-link EZ-source inverter is that although (33) and (34) give rise to zero capacitive voltage under no shoot-through condition, the physical capacitive voltage is likely to still have a slight negative dc offset voltage appearing across it, introduced by the conducting diode D in Fig. 6(a), or D1 and D2 in Fig. 6(b). This negative offset voltage needs to be taken into consideration when choosing the appropriate capacitor type.

V. Experimental Results

The embedded inverters proposed in the paper were verified experimentally using a hardware platform that can flexibly be configured to any desired topology for testing. Upon completing the tests, most of the captured results were observed to be the same, as proven conceptually in earlier sections. Therefore, to avoid excessive duplication and to meet the specified page limit, only results for the EZ-source inverters are presented here for illustration purposes. With an EZ-source network constructed using L = 5 mH, C = 2200 μF and $V_{dc} \approx$ 60 V, and connected to a two-level voltage-type inverter controlled by a digital signal processor (DSP), Fig. 7 shows the relevant waveforms obtained by setting the relevant control parameters to M = 1.15×0.7 and T_0/T = 0 for no shoot-through state insertion. From the figure, it is obvious that the output current is sinusoidal, and the measured line voltage pulse height produced by the inverter, which corresponds to its dc-link voltage of v_i, matches the un-boosted theoretical value of ≈ 60 V calculated using (4). Next with M kept constant and a shoot-through duration of T_0/T = 0.3 added to the inverter state sequence, Fig. 8 clearly shows the boosting of line voltage pulse height (corresponding to v_i) from 60 V to 150 V, and the boosting of output current by 2.5 times to ≈1.75 A.

Next, reloading the DSP with the ULST code and reconfiguring the experimental platform to a NPC EZ-source inverter, Fig. 9 shows the waveforms captured with no shoot-through state inserted (T_0/T = 0) and the modulation ratio M set to the maximum of 1.15 with triplen offset added. This represents the maximum output electrical quantities that can be produced by a traditional NPC inverter, whose peak current is noted to be 1.2 A and maximum line voltage pulse height noted to correspond to the sum of two dc source voltages (80 V in total). With T_0/T now set to 0.3 and M reduced accordingly to 1.15×0.7, the recaptured experimental results are shown in Fig. 10, where the maximum current is boosted to 2 A, which is a factor of 0.7/(1–2×0.3) = 1.75 times higher than that shown in Fig. 9. Alternatively, these results mean that even if the input dc voltage (e.g. from renewable sources) dips by 43%, the proposed EZ-source inverter can still kept its output at the pre-sag level. Performing the testing again with the FST scheme downloaded to the DSP, Fig. 11 and Fig. 12 show the recaptured experimental waveforms, where the same observations are noted, except for a slightly degraded output waveform quality with non-adjacent line voltage switching (obvious when comparing (e.g.) the centers of the positive line voltage cycles in Fig. 10 and Fig. 12).

For illustrating the filtering advantage of the NPC EZ-source inverter, Fig. 13 and Fig. 14 show waveforms captured at the dc front-end when the inverter is controlled using the ULST and FSL schemes respectively. From the fourth traces in both figures, it is clear that the illustrated network inductive currents i_L are relatively smooth even when the dc-link and

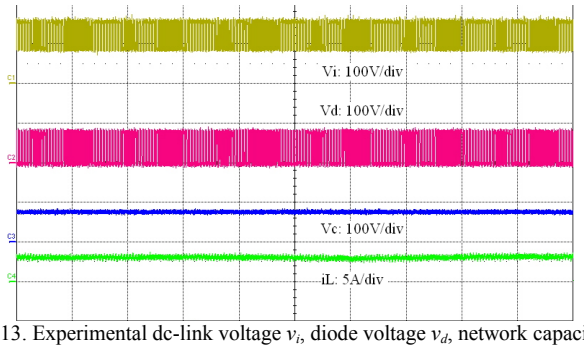

Fig. 13. Experimental dc-link voltage v_i, diode voltage v_d, network capacitive voltage V_C, and inductive current i_L of ULST-controlled NPC EZ-source inverter with M=1.15×0.7 and T_0/T=0.3 (2 ms/div).

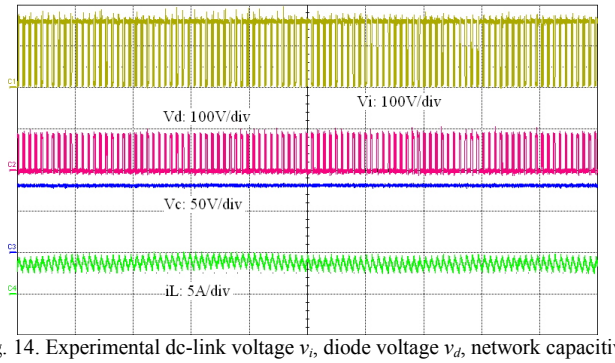

Fig. 14. Experimental dc-link voltage v_i, diode voltage v_d, network capacitive voltage V_C, and inductive current i_L of FST-controlled NPC EZ-source inverter with M=1.15×0.7 and T_0/T=0.3 (2 ms/div).

other voltages are chopping rapidly during the voltage-boosting mode. Also noted is the relatively smaller ripple of i_L for the ULST scheme, as compared to the FST scheme, where two reasons can be provided to explain this phenomenon. The first is deduced from (16) (valid for all presented X-shaped NPC inverters), which states that the ripple of the ULST scheme is a factor of 4/7 smaller than that of the FSL scheme. The second reason is linked to the findings reported in [6], where it is noted that the dc front-end switching frequency of the ULST scheme is a factor of two higher than that of the FSL scheme assuming the same set carrier frequency. This gives rise to a smaller ripple for the ULST scheme and a set of highly-dense chopping waveforms in Fig. 13. Another feature noted in Fig. 13 is that the dc-link voltage v_i does not collapse to zero, unlike that in Fig. 14, where full collision of voltage to zero is observed. This is expected since as deduced from Fig. 5(b) and (c), the partial upper and lower shoot-through states used for obtaining Fig. 13 do not short the inverter dc-link fully, and hence will result in a finite dc-link voltage.

VI. Conclusion

This paper proposes a new family of EZ-source inverters implemented using an impedance network with the relevant dc sources embedded within. Comparing with the Z-source inverters, the embedded EZ-source inverters have the advantages of drawing a smoother current from the dc input sources without using external second-order filters, and a lower required capacitive voltage. These advantages are attained with no degradation in gain, diode blocking voltage and other characteristic properties of the X-shaped impedance network

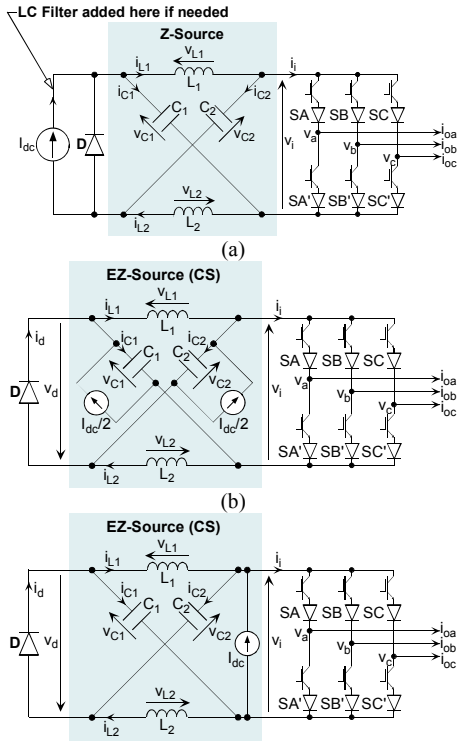

Fig. 15. Illustration of (a) Z-source, (b) EZ-source and (c) dc-link EZ-source current-type inverters.

for the same specified shoot-through duration. With slight modification introduced, an alternative family of dc-link EZ-source inverters can also be implemented with an even lower network capacitive voltage attained at the expenses of no inherent inductive filtering, a noisier source current waveform even under no voltage-boosting condition, and the presence of a small negative capacitive voltage. The testing of the inverters has been performed experimentally with favorable results obtained, hence confirming the practicality of the new EZ-source inverters. Needless to say, the embedded concepts can also be applied to the current-type inverter with its possible variants shown in Fig. 15. Details of these new current-type inverters are left for printing in a future publication.

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