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An Improved Design of Virtual Output Impedance Loop for Droop-Controlled Parallel Three-Phase Voltage Source Inverters

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***Abstract*—The virtual output impedance loop is known as an effective way to enhance the load sharing stability and quality of droop-controlled parallel inverters. This paper proposes an improved design of virtual output impedance loop for parallel three-phase voltage source inverters. In the approach, a virtual output impedance loop based on the decomposition of inverter output current is developed, where the positive- and negative-sequence virtual impedances are synthesized separately. Thus, the negative-sequence circulating current among the parallel inverters can be minimized by using a large negative-sequence virtual resistance even in the case of feeding a balanced three-phase load. Furthermore, to adapt to the variety of unbalanced loads, a dynamically-tuned negative-sequence resistance loop is designed, such that a good compromise between the quality of inverter output voltage and the performance of load sharing can be obtained. Finally, laboratory test results of two parallel three-phase voltage source inverters are shown to confirm the validity of the proposed method.**

I. INTRODUCTION

The power electronic-based distributed power generation has undergone a rapid development in recent years. A wide spread use of voltage source inverters as grid interfaces for distributed energy resources (DER) can be envisioned in the near future [1]. To accommodate the increased penetration of DER units, the microgrid concept that can operate in grid-connected and islanded modes is emerging as an attractive way. The intentional and non-intentional islanded operations of microgrids provide more reliable electricity service during abnormal disturbances in the upstream grid [2]. To preserve the stability and power quality of a microgrid, particularly in the dynamic islanding operations, the cooperative control of inverter-interfaced DER units plays an essential role. Hence, there is an increasing concern over the paralleled operation of voltage source inverters, and in such systems, the damping of circulating current among inverters is important for the stability and quality of load sharing [3].

A number of control approaches have been developed to achieve a good load sharing among parallel inverters [4]. The droop control schemes, among other options, have shown superior performances in terms of the reliability and costs, thanks to the absence of communication links [5]. However, due to the impact of line impedance and load characteristics, several limitations are imposed on directly using the active power-frequency (P-ω) droop and the reactive power-voltage (Q-V) droop controllers. For example, the high R/X ratio of distribution feeders couples the control of active power and reactive power flows, while on the other hand the frequency- and voltage-dependent load characteristics limit to use the opposite droop relationships, i.e. Q-ω and P-V droops [6]. To overcome such effects, the closed-loop output impedance of the inverter is adjusted by, either changing the bandwidth of the voltage control loop [7], or inserting a virtual impedance loop [8]. Since the injection of noncharacteristic frequency signal is needed in [7], it requires advanced signal processing techniques which complicate the control system. In contrast, the virtual impedance loop is much easier to implement and has become more popular.

It is well known that the virtual output impedance loop is mainly inductive to reshape the R/X ratio of interconnected impedances among inverters. For a three-phase inverter, the virtual inductance can be easily realized using the complex number calculation in the stationary $\alpha\beta$-frame, thus the time derivative of the output current can be avoided [9]. However, only the positive-sequence virtual inductance is synthesized in this way. For parallel three-phase inverters with separate DC-links, the circulating current among them comprises the negative-sequence circulating current (NSCC) in addition to the positive-sequence circulating current (PSCC) [10]. Thus, the conventional inductive virtual impedance has little effect on the damping of the NSCC, and the output currents of the parallel inverters become unbalanced even in the presence of balanced three-phase loads. To solve this problem, instead of synthesizing virtual inductance, a virtual resistance loop is applied with a resonant voltage controller in [11]. Thus, the virtual resistance takes the same effect on the positive- and negative-sequence output currents. Nevertheless, this method

is in capable of damping the NSCC when feeding balanced or slightly unbalanced three-phase loads, due to the coupling between the sharing of active power and negative-sequence load current. In [12], a negative-sequence conductance loop based on the output voltage decomposition is reported, where a droop relationship between the negative-sequence reactive power (Q^-) and the negative-sequence conductance (G) is built. Thus, a better sharing of the unbalanced compensation burdens can be obtained in comparison to the fixed virtual resistance scheme. However, the performance of the $Q^- - G$ droop method is still restricted on reducing the NSCC when feeding balanced three-phase loads, since the NSCC in this case is gradually reduced with the decrease of G.

In order to overcome the aforementioned drawbacks, an improved design of virtual output impedance loop for three-phase inverters is proposed in this paper. In the approach, the inverter output current is decomposed into the positive- and negative-sequence components. A virtual resistance loop for the negative-sequence output current is developed, together with the conventional inductive virtual impedance loop for the positive-sequence output current. Thus, the NSCC among parallel inverters can be effectively damped by adjusting the negative-sequence virtual resistance. Compared with the PI-based NSCC control schemes in [10], the negative-sequence virtual resistance can be furnished in each inverter without using any additional interconnection circuit, which is more suitable for scattered DER inverters. Furthermore, to adapt to the unbalanced load variation, a dynamically-tuned negative-sequence virtual resistance loop is designed, such that a good compromise between the performance of sharing negative-sequence currents and the inverter output voltage quality can be obtained. Finally, laboratory tests on two parallel three-phase voltage source inverters are performed to confirm the validity of the proposed method.

II. Circulating Current in Parallel Voltage-Controlled DER Inverters

Fig. 1 shows an example of an islanded three-phase low-voltage microgrid, where n parallel DER units are interfaced with three-phase voltage source inverters and connected to a common AC bus through distribution feeders, respectively. The DC-links of DER inverters are assumed to be controlled by the separate, isolated energy sources and kept constant.

A. Definition of Circulating Current

The circulating current of a three-phase inverter is termed as the difference between the actual output current and the assigned load current, which is given by [13]

$$c_{k,i} = \sum_{m=1}^{n}\left(h_m i_{ok,i} - h_i i_{ok,m}\right), \quad \begin{matrix} k \in \{a,b,c\} \\ i,m \in \{1,2,\ldots,n\} \end{matrix} \tag{1}$$

$$\sum_{m=1}^{n} h_m = 1 \tag{2}$$

where $c_{k,i}$ is the circulating current of the i-th DER inverter and k denotes the inverter phase. $i_{ok,i}$ and $i_{ok,m}$ are the output currents of the i-th and m-th inverters, respectively. h_m and h_i are the load current distribution factors for the i-th and m-th inverter, respectively, and the sum of all distribution factors equals to 1.

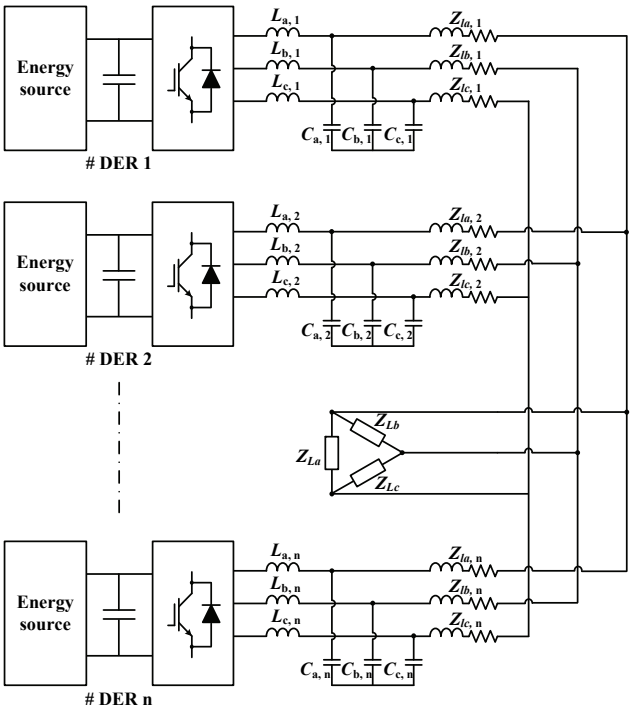


Fig. 1. An example of an islanded three-phase low-voltage microgrid.

Fig. 2 shows a path for the circulating current between two parallel DER inverters. Since the DC-links of inverters are isolated, there is no zero-sequence circulating current in the inverters. However, due to the component tolerance, and the parameters drifts of sensors, the asynchronous switching patterns of the inverters are inevitably generated [14]. As a consequence, the path for the non-zero-sequence circulating current, which is also termed as the 'cross current' in [15], is formed whenever the inverters are in the different switching state. Furthermore, it can be seen that the non-zero-sequence circulating current flowing through one phase is dependent on the circulating current in the other two phases. In such case, the parallel DER inverters can be further simplified as a set of parallel-connected three-phase voltage sources [16].

B. Small-Signal Modeling of DER Inverter

Within the islanded microgrid DER inverters are usually controlled as voltage sources. Notice that the inverter output impedance has an important effect on the characteristic of circulating current. Thus, the closed-loop dynamic behavior of inverter output voltage control loop has to be considered in order to derive the circulating current of a DER inverter.

Fig. 3 illustrates the block diagram of the output voltage control scheme adopted for the i-th DER inverter. It consists of two loops, where an inner inductor current controller with a proportional term, $K_{pc,i}$, is used for over-current protection

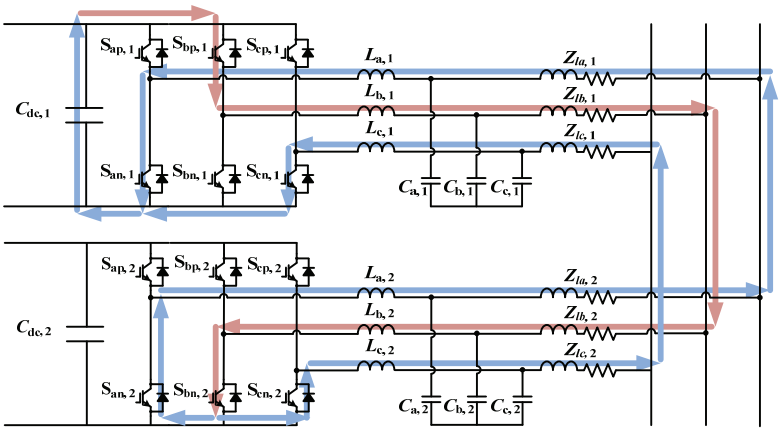


Fig. 2. A non-zero-sequence circulating current path between two parallel DER inverters.

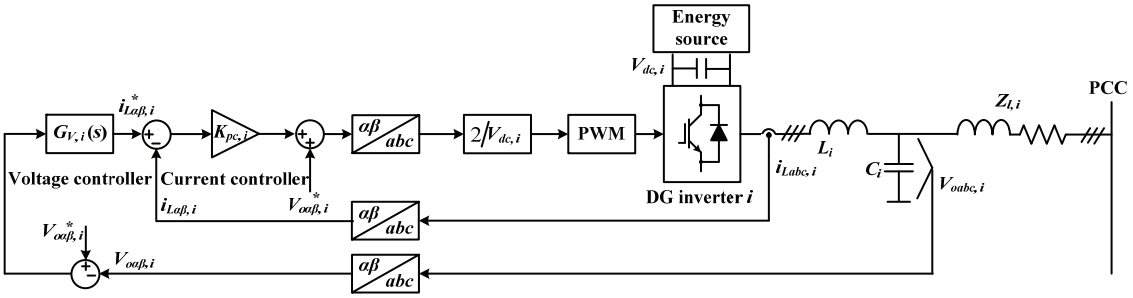


Fig. 3. Block diagram of output voltage control scheme adopted by the *i*-th DER inverter

and filter resonance damping, and an outer capacitor voltage control loop using the proportional plus resonant controller, which can be given by

$$G_{V,i}(s) = K_{pv,i} + \frac{K_{iv,i}s}{s^2 + \omega_i^2} \tag{3}$$

Notice that the inverter with a constant DC-link voltage is a linear system [17]. The closed-loop dynamic behavior of DER inverter can be equivalent as a Thevenin equivalent circuit, which are derived as follows

$$V_{o,i}(s) = G_{cl,i}(s)V^*_{o,i}(s) - Z_{o,i}(s)i_{o,i}(s) \tag{4}$$

$$G_{cl,i}(s) = \left.\frac{V_{o,i}(s)}{V^*_{o,i}(s)}\right|_{i_{o,i}(s)=0} = \frac{K_{pc,i}G_{d,i}(s)G_{V,i}(s)}{L_{f,i}C_{f,i}s^2 + \left(K_{pc,i}G_{d,i}(s) + r_{f,i}\right)C_{f,i}s + K_{pc,i}G_{d,i}(s)G_{V,i}(s)} \tag{5}$$

$$Z_{o,i}(s) = \left.\frac{V_{o,i}(s)}{i_{o,i}(s)}\right|_{V^*_{o,i}(s)=0} = \frac{L_{f,i}s + r_{f,i} + K_{pc,i}G_{d,i}(s)}{L_{f,i}C_{f,i}s^2 + \left(K_{pc,i}G_{d,i}(s) + r_{f,i}\right)C_{f,i}s + K_{pc,i}G_{d,i}(s)G_{V,i}(s)} \tag{6}$$

where $V_o(s)$ and $V^*_{o,i}(s)$ are the actual and command inverter output voltages, repectively. $G_{cl,i}(s)$ denotes the closed-loop transfer function of the voltage control loops, and $Z_{o,i}(s)$ is the output impedance. $r_{f,i}$ is the parasitic resistance of the filter inductance $L_{f,i}$. $G_{d,i}(s)$ is the 1.5 sampling period (T_s) delay including the computational delay (T_s) and the PWM delay ($0.5T_s$).

C. Analysis of Circulating Current

Fig. 4 illustrates the small-signal model of parallel three-phase DER inverters in the stationary $\alpha\beta$ frame. Notice that any differences among the amplitudes of voltage sources may result in circulating currents. Since the output current of the *i*-th inverter can be easily derived by

$$i_{o,i}(s) = \frac{G_{cl,i}(s)V^*_{o,i}(s) - V_{pcc}}{Z_{l,i}(s) + Z_{o,i}(s)} \tag{7}$$

where V_{pcc} is the voltage at the common AC bus and $Z_{l,i}(s)$ is the line impedance. Under the circulating current definition in (1), the circulating current of the *i*-th DER inverter can be obtained in (8), shown at the bottom of next page, where δ_{ij} is defined as

$$\delta_{ij} = \begin{cases} 1 & i = j \\ 0, & i \neq j \end{cases} \tag{9}$$

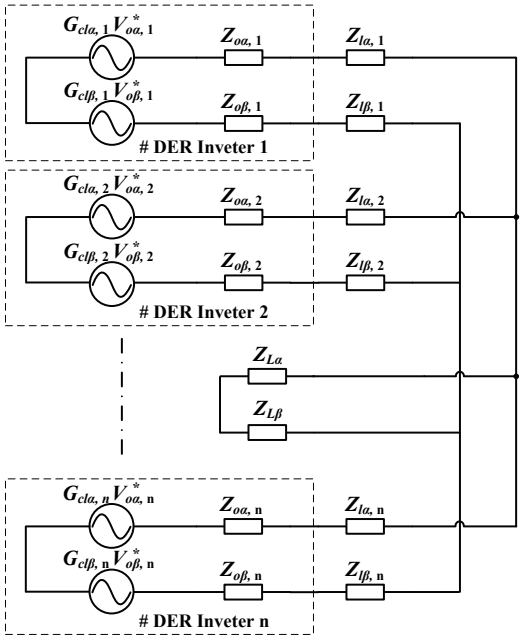


Fig. 4. The small-signal model of parallel three-phase DER inverters in the stationary $\alpha\beta$ frame.

From (8), it is seen that the circulating current is not only affected by the voltage differences of DER inverters, but also subjected to the load condition at the common AC bus. Also, the presence of any unbalanced parameters drifts will cause unbalanced voltage differences among the inverters, and the unbalanced circulating current loop are consequently formed. Hence, different from the parallel single-phase inverters, the circulating current in the three-phase inverters consists of the PSCC and the NSCC.

Under the certain voltage differences, the magnitudes of circulating currents are dependent on the line impedance and the inverter output impedance. Thus, by actively controlling the inverter output impedance, the circulating current can be damped effectively. However, in the presence of different electrical constants, like the different line impedance and the unbalanced load, a good compromise between the quality of the inverter output voltage and the suppression level of the circulating current is needed.

III. Proposed Control Method

Fig. 5 illustrates the diagram of the droop-based power control scheme and the proposed virtual impedance loop for the *i*-th DER inverter. The approach employs a multi-loop control scheme, which includes 1) the inner voltage control loops, as shown in Fig. 3, 2) the outer droop-based power controller, and 3) the intermediate virtual output impedance loop.

A. Limits of Droop Control

Considering the frequency- and voltage-dependent loads effects [6], the standard active power-frequency (P-ω) and the reactive power-voltage (Q-V) droop controllers are used, which can be given by

$$\omega_i = \omega_0 - m_i P_i \tag{10}$$

$$V_i = V_0 - n_i Q_i \tag{11}$$

where ω_0 and V_0 are the nominal frequency and magnitude of the *i*-th inverter output voltage at no load. m_i and n_i are the frequency and voltage droop coefficients, respectively, and the following conditions are needed to determine the load distribution factors of inverters.

$$m_1 P_1 = m_2 P_2 = \cdots = m_n P_n \tag{12}$$

$$n_1 Q_1 = n_2 Q_2 = \cdots = n_n Q_n \tag{13}$$

Since there is an integral relationship between the power angle and the frequency, the zero steady-state error of active power sharing can be achieved by using the P-ω droop [18]. In contrast, the Q-V droop controller depends heavily on the characteristics of power transfer impedances among parallel inverters. The high R/X ratio of the low-voltage distribution line impedance degrades the performance of reactive power sharing. Furthermore, the droop controller only takes effect on the PSCC, whereas the NSCC still remain in the output currents of inverters.

B. Proposed Virtual Output Impedance Loop

The design of the virtual output impedance loop has two main purposes, i.e. 1) to enhance the stability and quality of using the P-ω and Q-V droop control, and 2) to suppress the NSCC in parallel inverters. To achieve these objectives, a virtual output impedance loop based on the decomposition of the output current is developed. Thus, both the positive- and negative-sequence virtual impedances can be synthesized, as shown in Fig. 5.

Fig. 6 shows the diagrams of the inverter voltage and current sequence detector. The double synchronous reference frames are used to detect the positive- and negative-sequence components. The first-order low-pass filter with 1 Hz cut-off frequency is adopted in each reference frame. It is worth to mention that the feedforward decoupling terms are less effective in such case, since the transient changes of the

$$\begin{bmatrix} c_{\alpha,i} \\ c_{\beta,i} \end{bmatrix} = \begin{bmatrix} G_{cl\alpha,1}V^*_{o\alpha,1} & G_{cl\alpha,2}V^*_{o\alpha,2} & \cdots & G_{cl\alpha,n}V^*_{o\alpha,n} \\ G_{cl\beta,1}V^*_{o\beta,1} & G_{cl\beta,2}V^*_{o\beta,2} & \cdots & G_{cl\beta,n}V^*_{o\beta,n} \end{bmatrix} \begin{bmatrix} \left(\delta_{1j} - h_1\right)/\left(Z_{l,1} + Z_{o,1}\right) \\ \left(\delta_{2j} - h_2\right)/\left(Z_{l,2} + Z_{o,2}\right) \\ \vdots \\ \left(\delta_{nj} - h_n\right)/\left(Z_{l,n} + Z_{o,n}\right) \end{bmatrix} - \begin{bmatrix} \sum_{j=1}^{n} \dfrac{\left(\delta_{ij} - h_i\right)}{Z_{l,j} + Z_{o,j}} \end{bmatrix} \begin{bmatrix} V_{pcc\alpha} \\ V_{pcc\beta} \end{bmatrix} \tag{8}$$

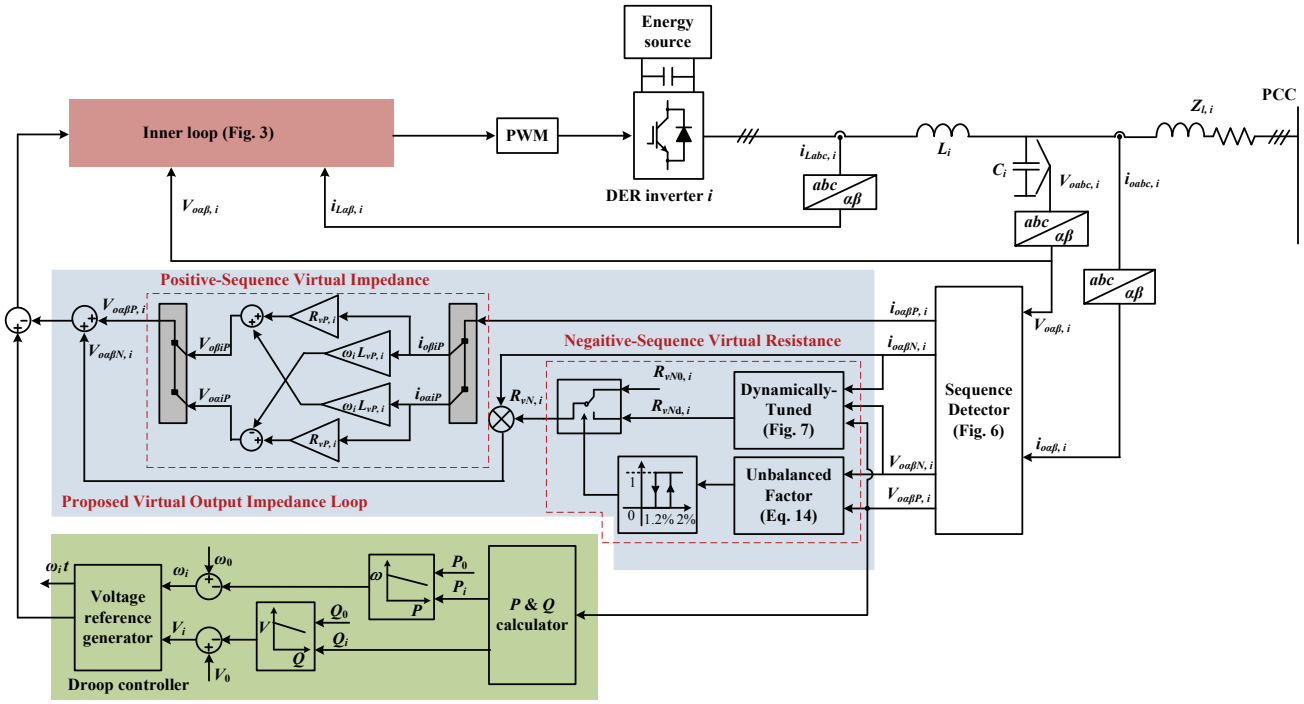


Fig. 5. Block diagram of the droop-based power control scheme and the proposed virtual output impedance loop

output current can aggravate the interactions between the different sequence components.

For the positive-sequence virtual output impedance loop, the inductive impedance is designed to mitigate the effect of high R/X ratio of distribution lines and to reduce the error of sharing reactive power among the inverters [9]. On the other hand, for the negative-sequence virtual impedance loop, an adaptive resistance is synthesized to damp the NSCC. Notice that the negative-sequence inductance can also be used here, but with lower stability margin due to the 90 degrees phase shift.

Depending on the presence of the unbalanced loads, the negative-sequence resistance is adaptively switched between a static large resistance and a dynamically-tuned one. The NSCC itself is dynamically reduced with the increase of negative-sequence virtual resistance. Thus, little unbalanced voltage distortion is caused at the output of the inverter. Hence, the voltage unbalanced factor can be used to detect the presence of unbalanced loads [19], which is defined as

$$U_{N,i} = \sqrt{V_{o\alpha N,i}^2 + V_{o\beta N,i}^2} \Big/ \sqrt{V_{o\alpha P,i}^2 + V_{o\beta P,i}^2} \tag{14}$$

The negative-sequence resistance is initially fixed with a large value at the start of the inverter. When the unbalanced loads are absent, the NSCC can be damped effectively by the large negative-sequence resistance. The voltage unbalanced factor is kept below a certain value 1.2%, which is dependent on the parameters deviations of voltage sensors. Based on the hysteresis control in Fig. 5, the negative-sequence resistance is kept as R_{vN0}. In the case that unbalanced loads are present,

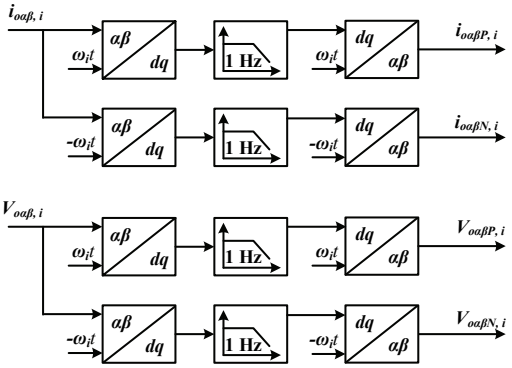


Fig. 6. Block diagram of the adopted sequence detector.

once the negative-sequence load current causes the voltage unbalanced factor higher than the limit, 2%, the negative-sequence virtual resistance are switched from the fixed value to a dynamically-tuned one.

Fig. 7 shows the block diagram of the dynamically-tuned negative resistance loop. A proportional relationship between the negative-sequence reactive power $Q_{N,\ i}$ [20] and the negative-sequence virtual resistance is introduced, so that the inverter with higher negative-sequence reactive power can furnish a higher negative-sequence resistance. The values of proportional coefficients for all inverters need to meet the following condition

$$k_1 Q_{N,1} = k_2 Q_{N,2} = \cdots = k_n Q_{N,n} \tag{15}$$

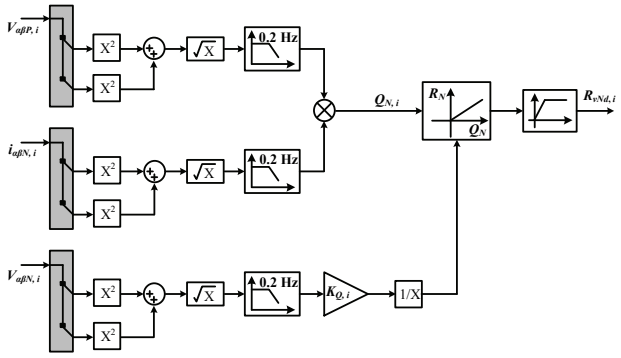


Fig. 7. Block diagram of the dynamically-tuned negative-sequence virtual resistance.

where k_i is the coefficient of the proportional relationships in the i-th inverter.

Furthermore, with the increase of the unbalanced loads, the negative-sequence inverter output voltage will inevitably increase. Thus, a smaller negative-sequence virtual resistance is generally needed to get a good load sharing. To adapt to the increase of unbalanced loads, the proportional coefficient is dynamically reduced according to the negative-sequence voltage at the output of inverter.

IV. Laboratory Test Results

To evaluate the performance of the proposed approach, two 5.5 kW Danfoss frequency converters powered by two separate, isolated DC sources are used as the DER inverters. Fig. 8 shows the schematic of the test system built in the lab. Two inductances, $L_{l,1}$ and $L_{l,2}$, are used to represent the line impedances in the laboratory tests, respectively. The control system for parallel inverters is implemented in the DS1006 dSPACE system with the 10 kHz sampling frequency and a half-period interrupt shift. The main circuit constants and the control system parameters are summarized in Table I and II, respectively.

To clearly see the adverse effect of the NSCC, a balanced three-phase parallel R-L load is tested at the first step. Fig. 9 (a) shows the tested output current waveforms for the case of only using the conventional virtual output impedance loop. It is seen that the output current of the inverters are unbalanced even feeding balanced three-phase loads, which validates the presence of the NSCC between parallel inverters. Also, the circulating current can be observed through the difference in the phase-A output currents of two inverters. In contrast, the inverter output current waveforms with the proposed virtual output impedance are shown in Fig. 9 (b). It is obvious that the NSCC is effectively damped by the negative-sequence virtual resistance loop.

Fig. 10 shows the steady-state waveforms in the presence of an unbalanced load. Fig. 10 (a) shows the output voltages and phase-A output currents of inverters when the negative-sequence virtual resistances are kept as R_{vN0}. It is clearly seen that the current differences are almost zero, while the output voltages are obviously unbalanced. It indicates that the fixed

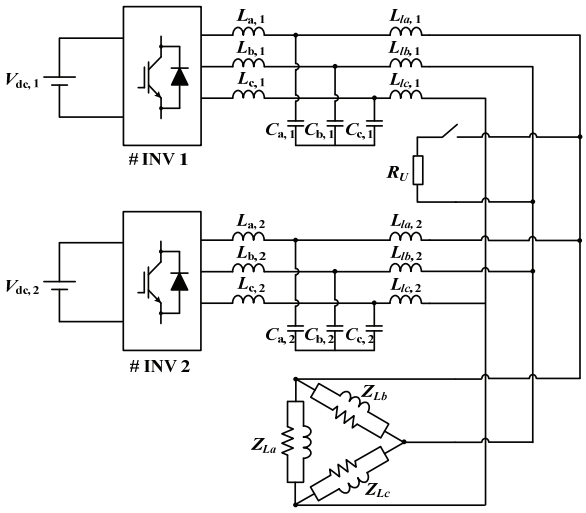


Fig. 8. Schematic of the laboratory test system.

TABLE I. Main Circuit Constants

Circuit Constants		Values
LC-filters of inverters	$L_1 = L_2$	1.5 mH
	$C_1 = C_2$	25 μF
DC voltages of inverters	$V_{dc,1} = V_{dc,2}$	750 V
Line inductance	$L_{l,1} = L_{l,2}$	3 mH
Parallel R-L load	R_L	40 Ω
	L_L	160 mH
Unbalanced load	R_U	80 Ω
System voltage	V_0	380 V
System frequency	ω_0	314 rad/s

TABLE II. Control System Parameters

Controller Parameters		Values
Current controller	$K_{pc,1} = K_{pc,2}$	10
Voltage controller	$K_{pv,1} = K_{pv,2}$	0.2
	$K_{iv,1} = K_{iv,2}$	50
Droop controller	$m_1 = m_2$	10^{-4}
	$n_1 = n_2$	10^{-3}
Positive-sequence virtual impedance loop	$R_{vP,1} = R_{vP,2}$	0
	$L_{vP,1} = L_{vP,2}$	6 mH
Negative-sequence virtual resistance loop	$R_{vN0,1} = R_{vN0,2}$	20 Ω
	$K_{Q,1} = K_{Q,2}$	30

negative-sequence virtual resistances tend to aggravate the unbalanced voltage distortions when the unbalanced loads increases. Thus it is needed to adaptively adjust the negative-sequence virtual resistance. Fig 10 (b) shows the measured waveforms after activating the dynamically-tuned negative-sequence resistance loop. Compared to Fig. 10 (a), the output voltages are clearly improved, whereas the difference of the phase-A output currents is slightly increased. It implies that a

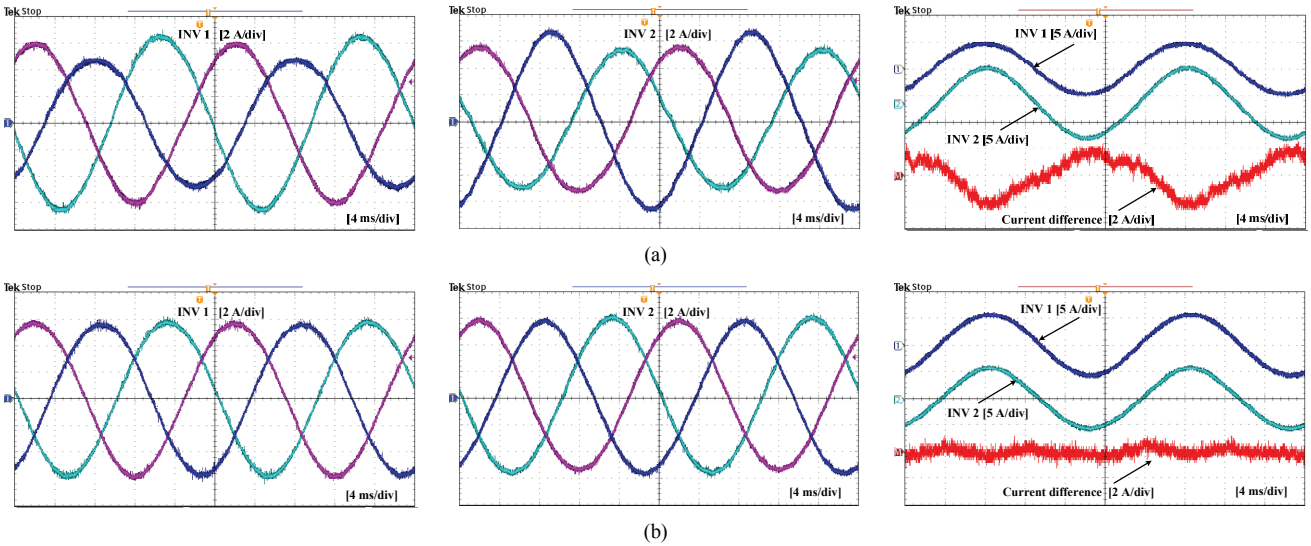


Fig. 9. Measured output current waveforms of the inverters feeding a balanced three-phase load.

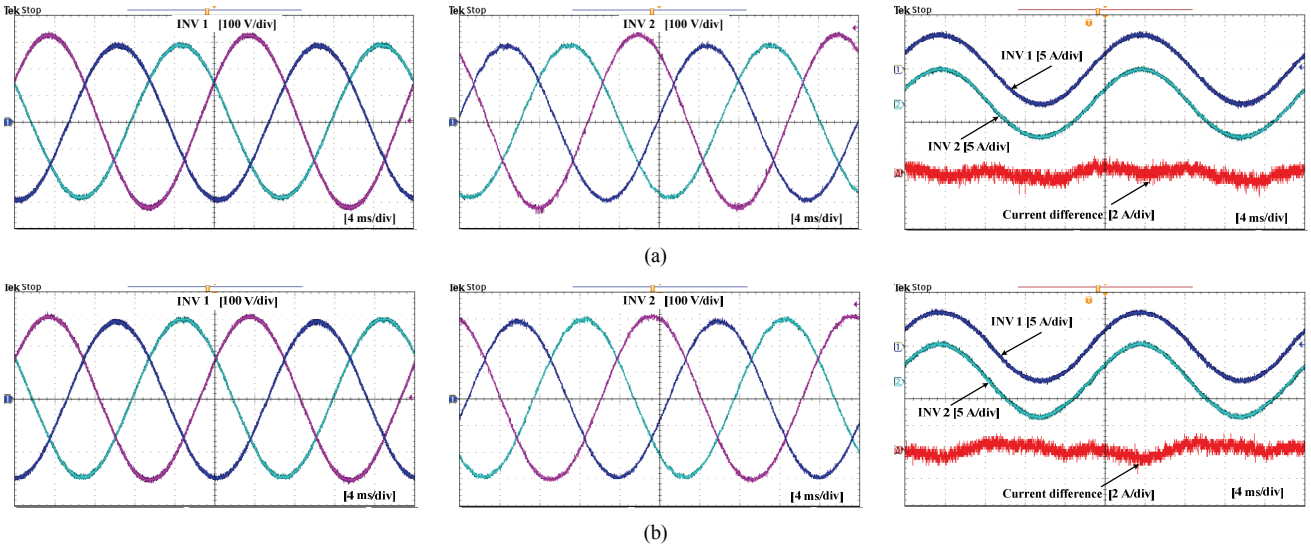
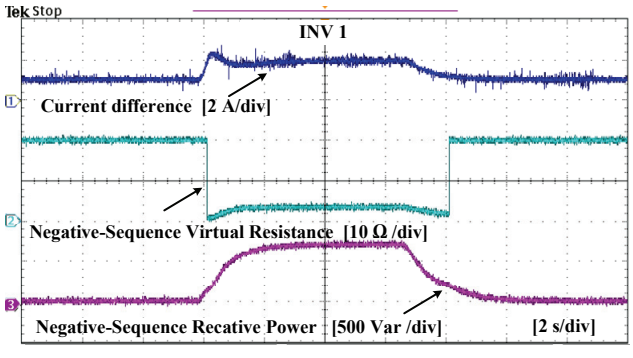
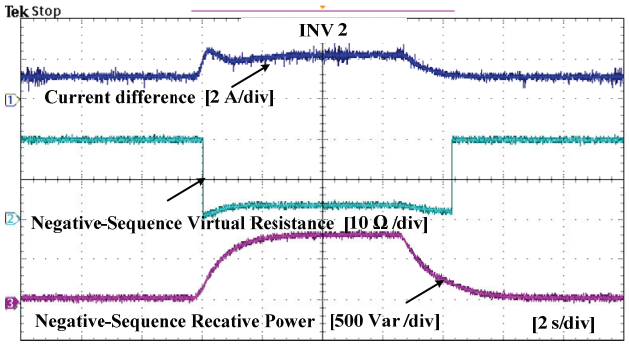


Fig. 10. Measured output voltage and current waveforms of the inverters in the presence of an unbalanced three-phase load.

good trade-off between the performance of unbalanced load sharing and the unbalanced voltage distortion is achieved.

Fig. 11 shows the measured transient waveforms when the unbalanced load is switched on and off. To confirm the performance of the negative-sequence virtual resistance loop, the changes of the voltage unbalanced factor, the negative-sequence reactive power, and the negative-sequence virtual resistance are evaluated. It is seen that before the unbalanced load is switched on, the negative-sequence reactive power is almost zero, the voltage unbalanced factor is lower than the threshold, 2 %, and the negative-sequence virtual resistance is kept as R_{vN0}. Once the unbalanced load is switched on, the voltage unbalanced factor increases to be higher than 2 %, the negative-sequence virtual resistance is switched from the R_{vN0} to be a dynamically-tuned resistance, which drops down rapidly, since the negative-sequence reactive power increases slowly. At the instant of switching off the unbalanced load, the voltage unbalanced factor starts to reduce gradually to be





(b)

Fig. 11. Measured transient waveforms when the unbalanced load is switched on and off.

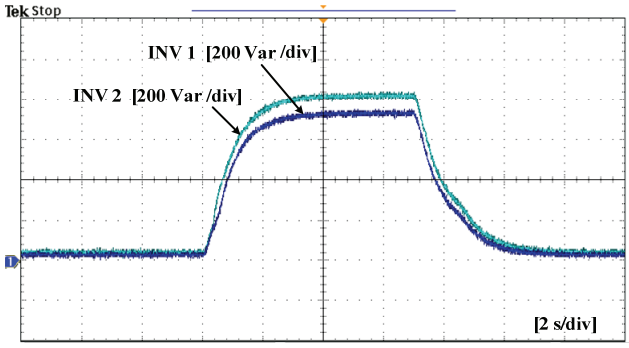


Fig. 12. Measured transient waveforms when the unbalanced load is switched on and off.

lower than the threshold, 1.2 %, and then negative-sequence virtual resistance is switched back to R_{vN0}. Fig. 12 compares the negative-sequence reactive powers of two inverters when the dynamically-tuned resistance loop is used. It indicates that a good unbalanced load sharing during the transients is achieved.

V. CONCLUSIONS

This paper has discussed an improved design method of the virtual output impedance loop for the droop-controlled parallel voltage source inverters. The circulating current in the parallel inverters are first modeled considering the effect of the closed-loop output impedances of inverters. Then, a virtual impedance loop for damping the NSCC is proposed. In the approach, a virtual impedance loop that is based on the decomposition of the output current is developed, thus the positive- and negative-sequence virtual impedance can be designed separately. As a consequence, the NSCC can be effectively damped using the negative-sequence resistance. Furthermore, in the case that unbalanced loads present, an adaptive negative-sequence virtual resistance is designed, so that the negative-sequence virtual resistance can be changed automatically according to the output voltage unbalanced factors. Finally, laboratory test results have been shown to confirm the performance of the proposed control method.

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