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Synthesis of Variable Harmonic Impedance in Inverter-Interfaced Distributed Generation Unit for Harmonic Damping Throughout a Distribution Network

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***Abstract*—This paper proposes a harmonic impedance synthesis technique for voltage-controlled distributed generation inverter in order to damp harmonic voltage distortion on a distribution network. The approach employs a multiloop control scheme, where a selective load harmonic current feedforward loop based on band-pass filter is developed in addition to the inner inductor current and the outer capacitor voltage control loops. Together with the use of multiple resonant integrators in the voltage control loop, the negative harmonic inductances and positive harmonic resistances are synthesized at dominant harmonic frequencies. Thus, the harmonic voltage drop and harmonic resonances throughout a distribution line with multiple shunt-connected capacitors can be effectively attenuated. Simulation and laboratory test results are shown to verify the performance of the proposed control method.**

I. INTRODUCTION

A widespread deployment of distributed generation (DG) units is envisioned in the near future, driven by the increasing environmental concerns, the diversification of energy sources, and the energy security challenge [1]. Thanks to the rapidly developed power electronics technology, the voltage-sourced DC-AC inverter is gaining a wide acceptance as an efficient interface for DG units connected to the grid [2]. On the other hand, harmonic distortion stems from the increased use of nonlinear electronic devices that may degrade the grid power quality [3]. Furthermore, due to the widely used *LC*-filters in the grid-connected converters, harmonic resonances resulting from the aggregated shunt-connected capacitors for a number of *LC*-filters, the capacitive loads, as well as the Power Factor Correction (PFC) capacitors are becoming a power quality challenge [4]. In turn, the *LC* resonance between the paralleled converters coupled through the grid impedance degrades the performance of converters in the microgrid system [5].

To attenuate the aforementioned harmonic interactions and harmonic resonances, a harmonic voltage detection based on current control was implemented in DG inverters for harmonic damping in a distribution network [6]. In this method, the DG inverter is programmed to behave as a resistive load at harmonic frequencies so that the harmonic voltage distortion can be damped. However, since there is no voltage control loop in this scheme, it is difficult to be applied in grid-interactive applications. To overcome this limit, an improved solution with the fundamental voltage control loop was developed in [7]. But the output voltage rather than the voltage at the Point of Connection (PoC) of DG unit was controlled in this method. Thus, even though it can achieve grid-interactive operation, the harmonic voltage distortion at the PoC of DG inverter may tend to be underdamped in the presence of large coupling inductance. In recent proposals, a harmonic voltage compensation approach based on the voltage-controlled DG inverters was reported [8], where a PoC voltage feedforward loop with a positive gain G was introduced. Consequently, the harmonic impedance of the DG inverter is scaled down by a factor of $1/(1+G)$, such that the harmonic voltage distortion at the PoC of DG inverter can be compensated. Nevertheless, the performance of this scheme on harmonic resonance damping is limited due to the absence of damping resistance.

In this paper, a variable harmonic impedance synthesis technique in voltage-controlled DG inverters is proposed for harmonic damping on a distribution network. The approach employs a multiloop control scheme, where a selective load harmonic current feedforward loop based on band-pass filter is developed in addition to the inner inductor current and the outer voltage control loops. Together with the use of multiple resonant integrators in the voltage control loop, the negative harmonic inductances and the positive harmonic resistances are synthesized at the dominant harmonic frequencies. Thus, the harmonic voltage drop on the coupling inductance and the harmonic amplification along a distribution feeder installing with multiple shunt-connected capacitors can effectively be attenuated. Simulations and laboratory tests results are shown to confirm the performance of the proposed control method.

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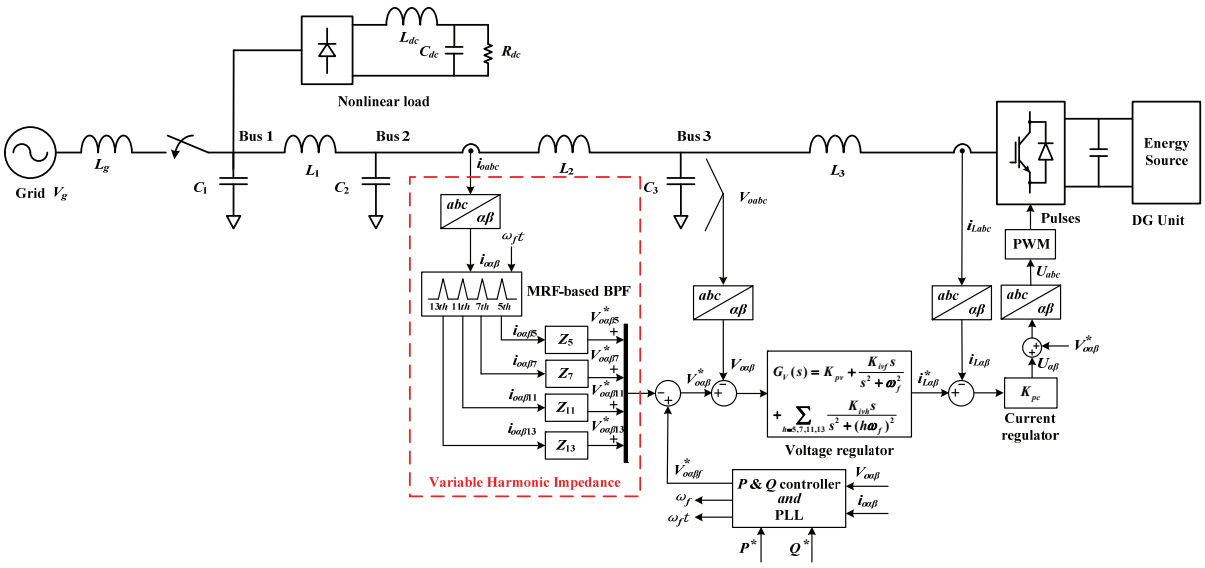


Figure 1. A simplified one-line diagram of a three-phase distribution system and the associated control schemes.

II. Variable Harmonic Impedance Concept

Fig. 1 illustrates a simplified one-line diagram of a three-phase distribution system and the associated control schemes. The inverter-interfaced DG unit is connected to the grid with an *LC*-filter (L_3 and C_3). Two shunt-connected capacitors (C_1 and C_2) are introduced to represent the aggregated capacitors for the *LC*-filters in a number of grid-connected converters and capacitive household loads [4]. A three-phase diode rectifier is connected at Bus 1 which disturbs with harmonic current. A static switch is adopted to switch the distribution system between grid-connected and islanded operation. In general, the bus voltages of distribution system are distorted due to the harmonic current from the diode rectifier load. The harmonic resonances between the shunt-connected capacitors and the line inductances occur at different conditions.

To make the DG unit operate in both grid-connected and islanded operation, the output voltage of DG inverter needs to be controlled. Then, the dynamic behavior of the closed-loop output voltage control system has an important effect on the harmonic distortions of distribution system. The closed-loop output impedance of DG inverter not only affects the output voltage distortion but also shifts the harmonic resonance frequencies of the distribution line. Thus, a variable harmonic impedance concept is proposed, which allows reshaping the output impedance at the dominant harmonic frequencies, such that the harmonic voltages throughout the distribution system can be suppressed.

In order to synthesize variable harmonic impedance of the DG inverter, a multiloop control scheme is employed, which includes i) an inner proportional inductor (L_3) current control loop for overcurrent protection and better *LC*-filter resonance damping [9], ii) an outer capacitor (C_3) voltage control loop using the proportional plus multiple resonant regulators for selective harmonic compensation, and iii) a selective load harmonic current feedforward loop by adopting Multiple Reference Frame (MRF)-based Band-Pass Filter (BPF) [10]. Fig. 2 gives the block diagram of MRF-based BPF. A first-order Low-Pass Filter (LPF) with the 1 Hz cut-off frequency is used in each reference frame to extract the dc component. Fig. 3 shows the performance of the MRF-based BPF for a nonlinear input current. The dc-link voltage is controlled by the energy source side, and a constant dc voltage is assumed.

Fig. 4 shows the block diagram of the proposed variable harmonic impedances. Different from the conventional virtual impedance schemes for nonlinear loads sharing in parallel-connected inverters [11], [12], the output impedance of the DG inverter is synthesized with negative inductances and positive resistances at the dominant harmonic frequencies, which can be given by

$$\begin{pmatrix} V^*_{o\alpha hp} \\ V^*_{o\beta hp} \end{pmatrix} = \begin{pmatrix} R_{hp} & j\omega_{hp}L_{hp} \\ -j\omega_{hp}L_{hp} & R_{hp} \end{pmatrix} \begin{pmatrix} i_{o\alpha hp} \\ i_{o\beta hp} \end{pmatrix} \tag{1}$$

$$\begin{pmatrix} V^*_{o\alpha hn} \\ V^*_{o\beta hn} \end{pmatrix} = \begin{pmatrix} R_{hn} & -j\omega_{hn}L_{hn} \\ j\omega_{hn}L_{hn} & R_{hn} \end{pmatrix} \begin{pmatrix} i_{o\alpha hn} \\ i_{o\beta hn} \end{pmatrix} \tag{2}$$

where the term '*hp*' and '*hn*' are used to denote the positive-sequence (+7th and +13th) harmonic components and the negative-sequence (-5th and -11th) harmonic components, respectively.

To see the effect of the synthesized harmonic impedances, a single-phase equivalent circuit for distribution system at the dominant harmonic frequencies is illustrated in Fig. 5. The DG inverter is equivalent to the harmonic impedance, due to the use of multiple resonant regulators. The diode rectifier is represented as a harmonic current source for simplicity, while

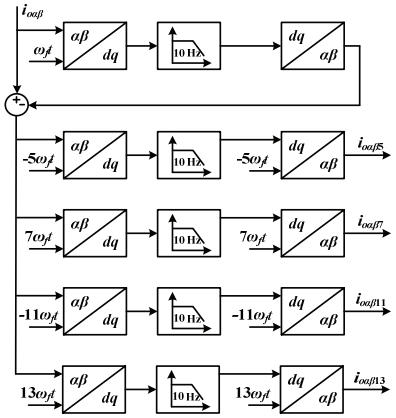


Figure 2. Block diagram of the multiple reference frame-based band-pass filter.

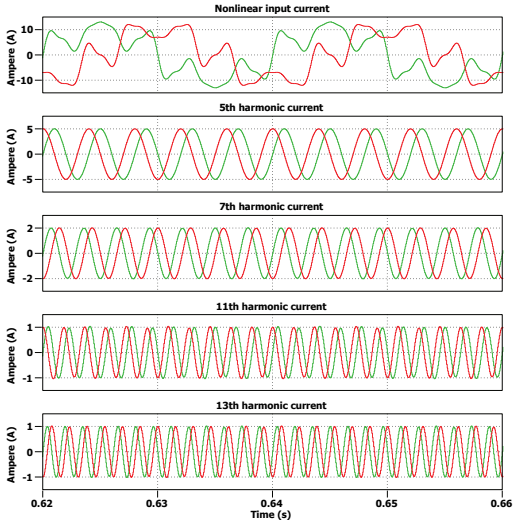
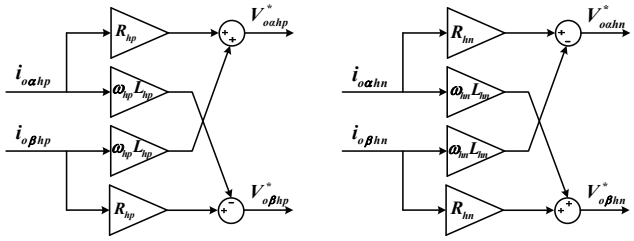


Figure 3. Performance of the multiple reference frame-based band-pass filter for a nonlinear input current.



(a) (b)

Figure 4. Block diagrams of the proposed variable harmonic impedances. (a) Positive-sequence harmonic impedances (Z_7, Z_{13}). (b) Negative-sequence harmonic impedances (Z_5, Z_{11}).

the background harmonic distortion is modeled as a harmonic voltage source connected with a harmonic impedance. Z_{C1h}, Z_{C2h}, Z_{L1h}, and Z_{L2h} denote the harmonic impedance for the C_1, C_2, L_1 and L_2, respectively. The harmonic voltage distortion at the PoC of inverter V_{2h} can be given by

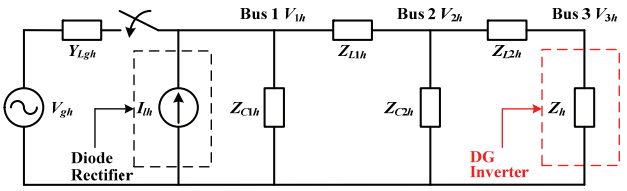


Figure 5. Single-phase equivalent circuit of the distribution system at the dominant harmonic frequencies.

$$V_{2h} = I_{oh}(Z_{L2h} + Z_h) \tag{3}$$

where I_{oh} is the output harmonic current. It can be seen that the negative harmonic inductances can compensate harmonic voltage drops on the coupling inductance L_2, which shows the same effect as the PoC voltage feedforward control scheme reported in [8]. However, it is noted that the size of negative inductance needs to be less than the coupling inductance, because the negative inductance alone will result in circuit instability [13]. Furthermore, it is known that a low resistance installed on the end bus of a distribution line can suppress harmonic amplification on the distribution line [14]. Hence, the synthesis of positive resistance can be used to perform harmonic damping in the case that the harmonic resonance occurs at the low-order harmonic frequencies.

III. Output Impedance Analysis of DG Inverter

It is worth to note that the characteristics of the variable harmonic impedances depend on the dynamic behavior of the closed-loop output voltage control system. The inner inductor current and outer voltage control loops can be modeled as a Thevenin equivalent circuit, which is expressed by

$$V_o(s) = G(s)V_o^*(s) - Z_o(s)I_o(s) \tag{4}$$

where $G(s)$ is the inverter reference-to-output voltage transfer function, and $Z_o(s)$ is the closed-loop output impedance of the inverter, which are derived from Fig. 1, respectively, as

$$G(s) = \frac{V_o(s)}{V_o^*(s)} = \frac{K_{pc}G_d(s)G_V(s)}{L_3C_3s^2 + C_3(K_{pc}G_d(s) + R_3)s + K_{pc}G_d(s)G_V(s)} \tag{5}$$

$$Z_o(s) = \frac{V_o(s)}{-I_o(s)} = \frac{L_3s + R_3 + K_{pc}G_d(s)}{L_3C_3s^2 + C_3(K_{pc}G_d(s) + R_3)s + K_{pc}G_d(s)G_V(s)} \tag{6}$$

$$G_d(s) = \frac{1}{1 + 1.5T_Ss} \tag{7}$$

where R_3 is the parasitic resistance of inductance L_3, K_{pc} and $G_V(s)$ are the current and voltage regulators, respectively, as shown in Fig. 1. $G_d(s)$ denotes 1.5 sampling period (T_S) delay

which comprises the computational delay (T_S) and the PWM (0.5 T_S) delay [15].

$$G_V(s) = K_{pv} + \frac{K_{ivf}s}{s^2+\omega_f{}^2} + \frac{K_{iv5}s}{s^2+(5\omega_f)^2} + \frac{K_{iv7}s}{s^2+(7\omega_f)^2} + \frac{K_{iv11}s}{s^2+(11\omega_f)^2} + \frac{K_{iv13}s}{s^2+(13\omega_f)^2} \quad (8)$$

Taking the load current feedforward loop into account, the output voltage reference for DG inverter is given by

$$V_o^*(s) = V_{of}^*(s) - Z_h(s)I_o(s) \quad (9)$$

$$V_o(s) = G(s)V_{of}^*(s) - (G(s)Z_h(s) + Z_o(s))I_o(s) \quad (10)$$

$$Z_{to}(s) = G(s)Z_h(s) + Z_o(s) \quad (11)$$

where $Z_{to}(s)$ is the total output impedance with synthesized harmonic impedance, $Z_h(s)$ is the proposed variable harmonic impedances, which can be described as

$$Z_h(s) = \sum_{h=5,7,11,13} \frac{2\omega_c(R_h s - (h\omega_f)^2 L_h)}{s^2 + 2\omega_c s + (h\omega_f)^2} \quad (12)$$

where ω_c is the cut-off frequency with 2π rad/s.

Table I summarizes the parameters of the DG inverter and the designed control system. Based on these parameters, the bode diagrams of closed-loop output voltage transfer function $G(s)$ is shown in Fig. 6. It can be observed that a good reference tracking at the dominant harmonic frequencies is achieved by using multiple voltage resonant integrators.

TABLE I. PARAMETERS FOR DG INVERTER AND THE DESIGNED CONTROLLER

Parameters		Values
Output *LC*-filters	L_3	1.5 mH
	R_3	0.04 Ω
	C_3	25 μF
Coupling inductance	L_2	3 mH
Sampling period	T_S	50 μs
Current controller	K_{pc}	20
Voltage controller (G_V)	K_{pv}	0.1
	K_{ivf}	300
	K_{iv5}= K_{iv7}	60
	K_{iv11}= K_{iv13}	30
	ω_f	100π rad/s
Synthesized harmonic impedance (Z_h)	R_5= R_7= R_{11}= R_{13}	4 Ω
	L_5= L_7= L_{11}= L_{13}	-2 mH

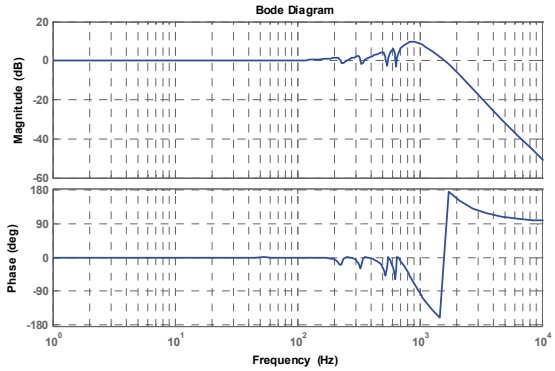


Figure 6. Bode diagrams of inverter reference-to-output voltage transfer function $G(s)$.

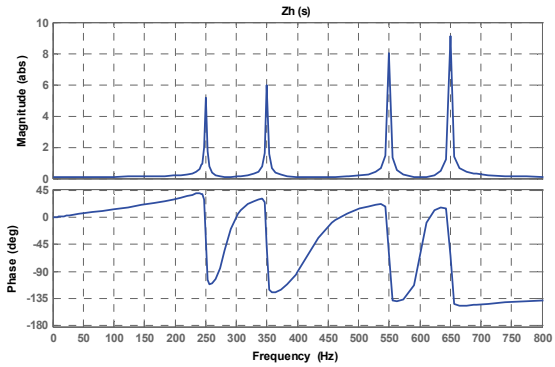


Figure 7. Frequency domain response of proposed variable harmonic impedances $Z_h(s)$.

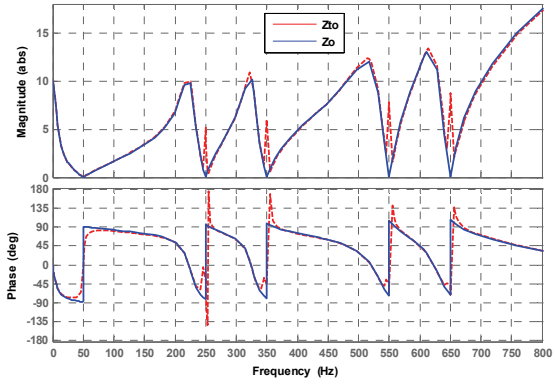


Figure 8. Frequency domain response of output impedance $Z_o(s)$ (blue solid line) and total output impedance $Z_{to}(s)$ (red dash line).

The frequency domain response of the proposed variable harmonic impedance $Z_h(s)$ is shown in Fig.7. It can be seen that $|Z_h(s)|$ at the dominant harmonic frequencies are equal to

$$|Z_h(s)| = \sqrt{R_h^2 + (h\omega_f L_h)^2} \quad (13)$$

TABLE II. PARAMETERS OF THE ANALYTED DISTRIBUTION SYSTEM

Parameters		Values
Line inductance	L_g	3.8 mH
	L_1	1.8 mH
Shunt-connected capacitor	$C_1 = C_2$	50 μF
Diode rectifier	L_{dc}	84 μH
	C_{dc}	235 μF
	R_{dc}	192 Ω
Injected power of inverter (Grid-connected mode)	P	1 kW
	Q	0.3 kVar

Since the synthesized inductance is negative, the phase angle of $Z_h(s)$ is negative at the dominant harmonic frequencies.

In order to see the effect of variable harmonic impedance, a comparison between the characteristics of output impedance $Z_o(s)$ and total output impedance $Z_{to}(s)$ is depicted in Fig. 8. It is obvious that the total output impedance is reshaped at the dominant harmonic frequencies. Furthermore, it is noted that the synthesized harmonic impedances in $Z_{to}(s)$ are the same as the variable harmonic impedance $Z_h(s)$. This is because the $Z_o(s)$ becomes zero and $G(s)$ has a unity gain and zero phase-shift at the dominant harmonic frequencies. Hence, from (11) it is clear that the $Z_h(s)$ determines the harmonic impedances of the DG inverter.

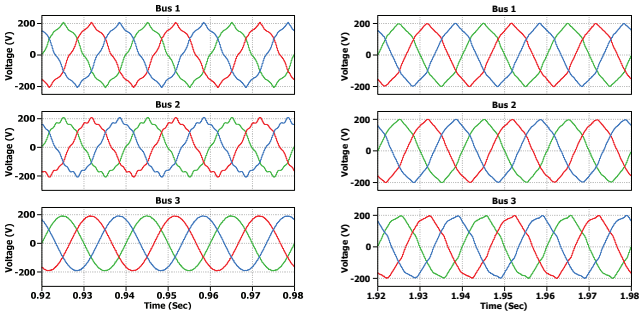
IV. SIMULATION RESULTS

To evaluate the performance of the proposed controller, the three-phase distribution system shown in Fig. 1 is built both in simulations and laboratory. Table II summarizes the circuit parameters of the built distribution system, and the DG inverter is built using the parameters listed in Table I.

A. Grid-Connected Operation

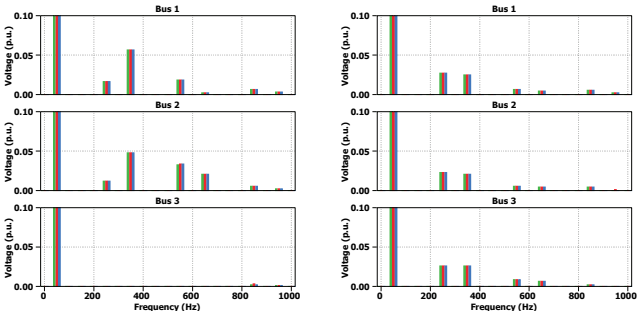
Fig. 9 shows the simulated bus voltages before and after using the proposed variable harmonic impedances in the grid-connected operation. In this case, the grid voltage is assumed to be sinusoidal, only the diode rectifier load is the harmonic source. It can be seen that the output voltage of inverter (Bus 3) is sinusoidal before applying harmonic impedances, which justifies the output impedance analysis depicted in Fig. 6 and Fig. 8. After using harmonic impedances, the output voltage of the inverter becomes distorted, whereas the other bus voltages are improved, as shown in Fig. 9 (b). The effect of harmonic impedances on harmonic damping can be observed by the corresponding harmonic spectrums of bus voltages, as shown in Fig. 10.

Fig. 11 shows the simulated bus voltages under distorted grid condition, where the grid voltage is distorted with the 2% fifth and 2% seventh harmonics. The harmonic spectrums for bus voltages are shown in Fig. 12. Similar to Fig. 10, the fifth harmonic voltage is slightly increased after using the variable harmonic impedances. It is because the reduction of seventh harmonic voltage will result in an increase of fifth harmonic voltage. Fig. 13 shows the simulated bus voltages and related harmonic spectrums of bus voltages in the case that zero fifth



(a) (b)

Figure 9. Simulated bus voltages before and after using the proposed variable harmonic impedances in the grid-connected operation (sinusoidal grid voltage). (a) Without the harmonic impedances. (b) With the harmonic impedances.



(a) (b)

Figure 10. Harmonic spectrums of simulated bus voltages in the grid-connected operation. (a) Without the harmonic impedances. (b) With the harmonic impedances.

harmonic impedance is synthesized. It is obvious that the fifth harmonic voltage in Fig. 13 is higher than the fifth harmonic voltage using the fifth harmonic impedance shown in Fig. 12. Table III summarizes the magnitudes of harmonic voltages simulated under both sinusoidal and distorted grid conditions. The changes of harmonic voltage brought by the proposed variable harmonic impedances can be seen.

B. Islanded Operation

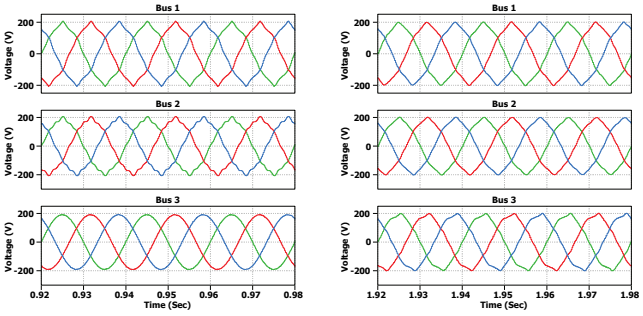
Fig. 14 shows the simulated bus voltages before and after applying the harmonic impedances in the islanded operation, and the corresponding harmonic spectrums of bus voltages is shown in Fig. 15. It can be seen that harmonic amplification occurs at the fifth harmonic frequency in islanded operation, which is effectively suppressed by the synthesized harmonic impedances. Table IV lists the magnitudes of the dominant harmonic harmonics and bus voltage THDs.

V. EXPERIMENTAL RESULTS

In the experimental setup, a 5.5 kW Danfoss frequency converter with a constant DC voltage source is adopted as the DG inverter. The switching frequency of the inverter is 10 kHz. The designed controller with the parameters given in Table I is implemented in the DS1006 dSPACE system.

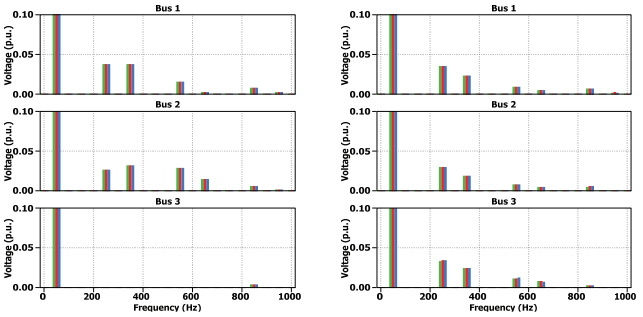
TABLE III. MAGNITUDES OF SIMULATED HARMONIC VOLTAGES AND THD AT EACH BUS IN THE GRID-CONNECTED OPERATION

Grid condition	Bus No.	V_{5th} (%)		V_{7th} (%)		V_{11th} (%)		V_{13th} (%)		THD (%)	
		Without	*With*	*Without*	*With*	*Without*	*With*	*Without*	*With*	*Without*	*With*
Sinusoidal grid	Bus 1	1.6	2.7	5.7	2.5	1.8	0.7	0.3	0.4	6.3	3.7
	Bus 2	1.2	2.3	4.8	2.0	3.3	0.5	2	0.5	6.3	3.1
	Bus 3	0	2.6	0	2.6	0	0.9	0	0.6	0.6	3
Distorted grid	Bus 1	3.6	3.5	3.7	2.3	1.5	0.9	0.2	0.4	5.5	4.1
	Bus 2	2.6	2.9	3.2	1.8	2.8	0.7	1.4	0.4	5.2	3.4
	Bus 3	0	3.3	0	2.3	0	1.1	0	0.7	0.6	4.4



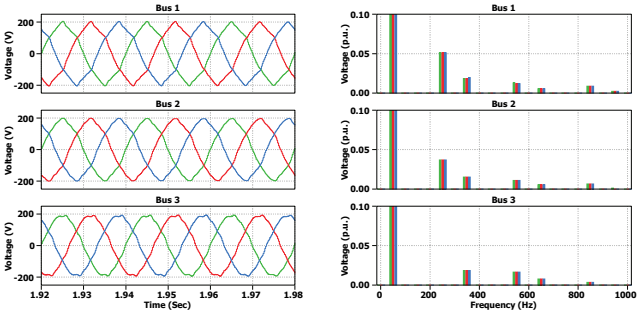
(a) (b)

Figure 11. Simulated bus voltages under distorted grid condition. (a) Without the harmonic impedances. (b) With the harmonic impedances.



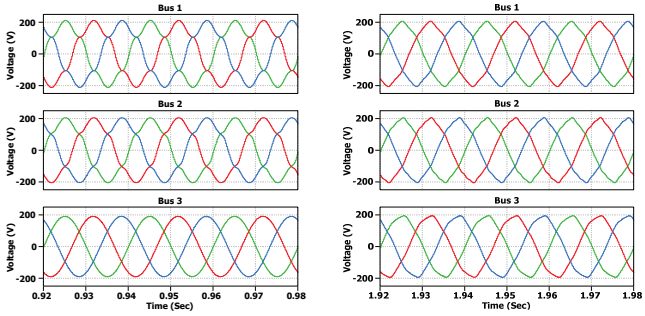
(a) (b)

Figure 12. Harmonic spectrums of simulated bus voltages under the distorted grid condition. (a) Without the harmonic impedances. (b) With the harmonic impedances.



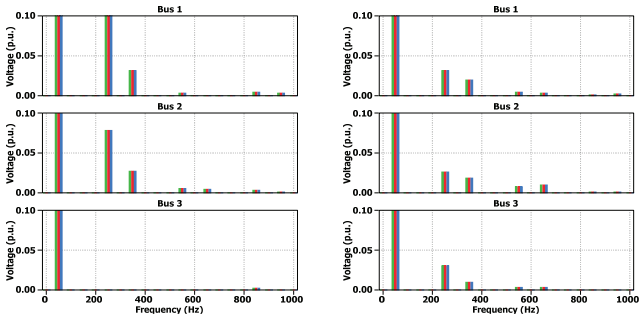
(a) (b)

Figure 13. Simulated bus voltages and the associated harmonic spectrums in the case that zero fifth harmonic impedance is synthesized.



(a) (b)

Figure 14. Simulated bus voltages in the islanded operation. (a) Without the harmonic impedances. (b) With the harmonic impedances.



(a) (b)

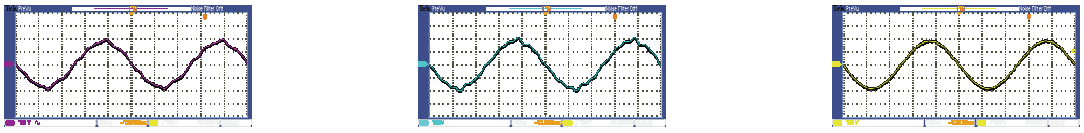
Figure 15. Harmonic spectrums of simulated bus voltages in the islanded operation. (a) Without the harmonic impedances. (b) With the harmonic impedances.

Fig. 16 shows the measured per-phase bus voltages before and after applying variable harmonic impedances in the grid-connected operation. It can be seen that the output voltage of inverter is sinusoidal before using the harmonic impedances, which is same as the simulation result depicted in Fig. 9. The corresponding harmonic spectrums are shown in Fig. 17. The harmonic voltage distortion at the PoC of inverter (Bus 2) is significantly reduced.

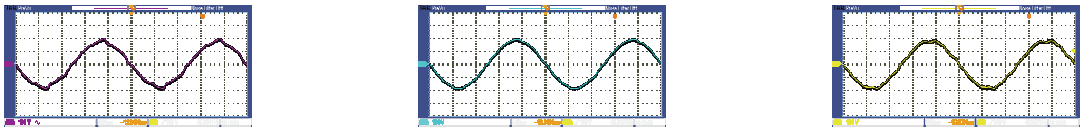
Fig. 18 shows the measured per-phase bus voltages during the islanded operation, and the associated harmonic spectrums are depicted in Fig. 19. Similar to the simulation results in the islanded operation, the fifth harmonic voltage is amplified on the distribution line and well damped after using harmonic impedances. Table V summarizes the magnitudes of measured harmonic voltages in grid-connected and islanded operation.

TABLE IV. MAGNITUDES OF SIMULATED HARMONIC VOLTAGES AND THD AT EACH BUS IN THE ISLANDED OPERATION

Bus No.	V_{5th} (%)		V_{7th} (%)		V_{11th} (%)		V_{13th} (%)		THD (%)	
	Without	*With*	*Without*	*With*	*Without*	*With*	*Without*	*With*	*Without*	*With*
Bus 1	10.7	3.2	3.1	1.9	0.3	0.4	0	0.2	11.2	3.7
Bus 2	7.8	2.7	2.7	1.8	0.5	0.8	0.4	1.0	8.3	3.5
Bus 3	0	3.1	0	1.0	0	0.3	0	0.3	0.5	3.3

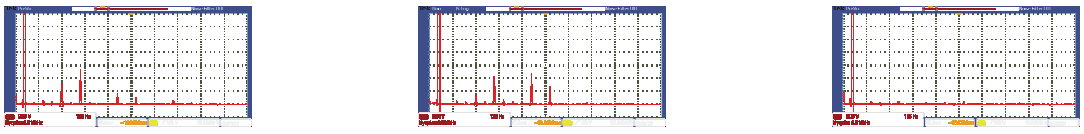


(a-1) Bus 1 (a-2) Bus 2 (a-3) Bus 3

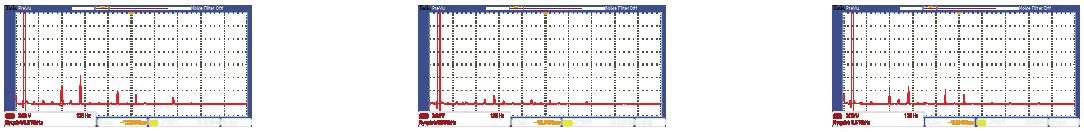


(b-1) Bus 1 (b-2) Bus 2 (b-3) Bus 3

Figure 16. Measured per-phase bus voltages during the grid-connected operation (4 ms/div, 100 V/div). (a) Without the synthesized harmonic impedances. (b) With the synthesized harmonic impedances.

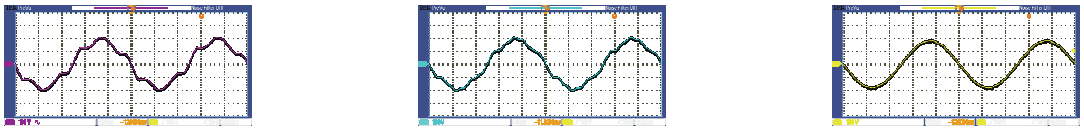


(a-1) Bus 1 (a-2) Bus 2 (a-3) Bus 3

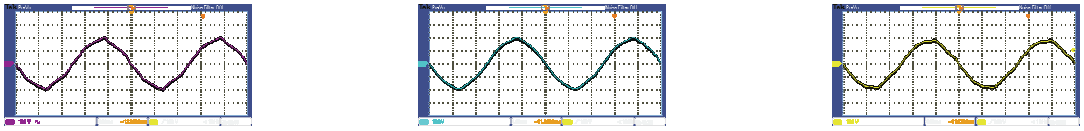


(b-1) Bus 1 (b-2) Bus 2 (b-3) Bus 3

Figure 17. Harmonic spectrums of the measured per-phase bus voltages during the grid-connected operation (125 Hz/div, 2V/div). (a) Without the synthesized harmonic impedances. (b) With the synthesized harmonic impedances.



(a-1) Bus 1 (a-2) Bus 2 (a-3) Bus 3

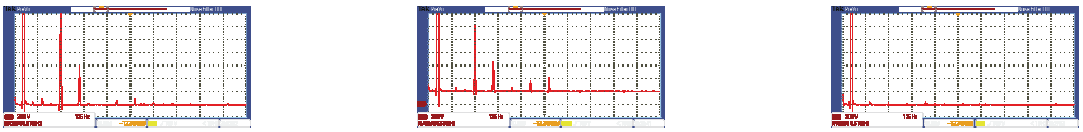


(b-1) Bus 1 (b-2) Bus 2 (b-3) Bus 3

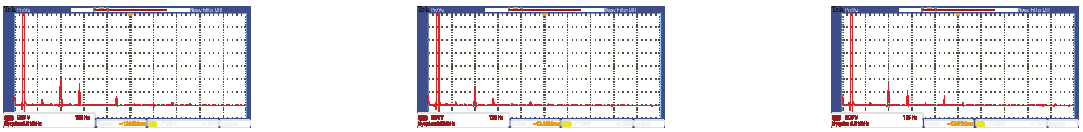
Figure 18. Measured per-phase bus voltages during the islanded operation (4 ms/div, 100 V/div). (a) Without the synthesized harmonic impedances. (b) With the synthesized harmonic impedances.

TABLE V. MAGNITUDES OF MEASURED HARMONIC VOLTAGES AT EACH BUS IN LABORATORY TESTS

Operation mode	Bus No.	V_{5th} (V)		V_{7th} (V)		V_{11th} (V)		V_{13th} (V)	
		Without	***With***	***Without***	***With***	***Without***	***With***	***Without***	***With***
Grid-connected	Bus 1	3.2	2.8	5.6	4.2	1.8	2.0	0.8	1.6
	Bus 2	1.6	0.4	4.2	1.2	4.6	0.6	2.8	0.4
	Bus 3	0	2.2	0	2.8	0	2.0	0	1.4
Islanded	Bus 1	20	4.4	6	3.2	0.4	1.2	0.8	0
	Bus 2	10	2.8	4.6	0.8	1.8	0.4	2.0	0
	Bus 3	0	3.4	0	2.0	0	1.6	0	0.4



(a-1) Bus 1 (a-2) Bus 2 (a-3) Bus 3



(b-1) Bus 1 (b-2) Bus 2 (b-3) Bus 3

Figure 19. Harmonic spectrums of the measured per-phase bus voltages during islanded operation (125 Hz/div, 2V/div). (a) Without the synthesized harmonic impedances. (b) With the synthesized harmonic impedances.

CONCLUSIONS

This paper has discussed a variable harmonic impedance synthesis method for voltage-controlled DG inverters in order to perform harmonic damping throughout a distribution line. In the proposed scheme, the negative inductances and positive resistances are synthesized by using the selective load current feedforward loop. Thus, the harmonic voltage compensation in the presence of large coupling inductance and the harmonic voltage amplification caused by shunt-connected capacitors can be achieved at the same time. The theoretical analysis and the expected performance of proposed control scheme have been verified through simulations and laboratory tests.

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