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Synthesis of Variable Harmonic Impedance in Inverter-Interfaced Distributed Generation Unit for Harmonic Damping Throughout a Distribution Network

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***Abstract*—This paper proposes a harmonic impedance synthesis technique for voltage-controlled distributed generation inverters in order to damp harmonic voltage distortion on a distribution network. The approach employs a multiloop control scheme, where a selective harmonic load current feedforward loop based on the bandpass filter is developed, in addition to the inner inductor current and the outer capacitor voltage control loops. Together with the use of multiple resonant integrators in the voltage control loop, the negative harmonic inductances and positive harmonic resistances are synthesized at the dominant harmonic frequencies. Thus, the harmonic voltage drop on the grid-side inductance and the harmonic resonances throughout a distribution feeder with multiple shunt-connected capacitors can be effectively attenuated. Simulation and laboratory test results validate the performance of the proposed control method.**

***Index Terms*—Distributed generation (DG), distribution network, harmonic resonance, negative harmonic inductance, variable harmonic impedance.**

I. Introduction

A WIDESPREAD deployment of distributed generation (DG) units is envisioned in the near future, driven by the increasing environmental concerns, the diversification of energy sources, and the energy security challenge [1]. Thanks to the rapidly developed power electronics technology, the voltage-sourced dc-ac inverter is gaining a wide acceptance as an efficient interface for DG units connected to the grid [2]. On the other hand, harmonic distortion that stems from the increased use of nonlinear electronic devices may degrade the grid power quality [3]. Furthermore, due to the widely used LC-filters in the grid-connected converters, harmonic resonances resulting from the aggregated shunt-connected capacitors for a number of LC-filters, the capacitive loads, as well as the power factor correction capacitors are becoming a power quality challenge [4]. On the other hand, the LC-filter resonances between the paralleled converters coupled through the grid impedance degrade the performance of converters in the microgrid system [5].

To attenuate the aforementioned harmonic interactions and harmonic resonances, a harmonic voltage detection based on current control was applied in DG inverters for harmonic damping on a distribution network [6]. In this method, the DG inverter is programmed to behave as a resistive load at the harmonic frequencies so that the harmonic voltage distortion can be damped. However, since there is no voltage control loop in this scheme, it is difficult to be implemented in grid-interactive microgrid applications [7]. To overcome this limit, an improved solution with the fundamental voltage control loop was developed in [8]. However, the output voltage rather than the voltage at the point of connection (PoC) of DG unit was controlled in this scheme. Thus, even though it can achieve grid-interactive operation, the harmonic voltage distortion at the PoC of DG inverter may tend to be underdamped in the presence of large grid-side inductance. In recent proposals, a harmonic voltage reduction approach based on the voltage-controlled DG inverters was reported, in which a PoC voltage feedforward loop with a positive gain G was introduced [9]. As a consequence, the harmonic impedance at the PoC of DG unit is scaled down by a factor of $1/(1+G)$, such that the harmonic voltage distortion at the PoC of DG inverter can be effectively compensated. Nevertheless, the performance of this scheme on harmonic resonance damping is limited due to the absence of damping resistance.

In this paper, a variable harmonic impedance synthesis technique in voltage-controlled DG inverters is proposed for harmonic damping on a distribution network. The approach employs a multiloop control scheme, where a selective load harmonic current feedforward loop based on the bandpass filter is developed in addition to the inner inductor current and the outer voltage control loops. Together with the use of multiple resonant integrators in the voltage control loop, the negative harmonic inductances and the positive harmonic resistances are synthesized at the dominant harmonic frequencies. Thus, the harmonic voltages drop across the grid-side inductance can be counteracted by the negative harmonic inductances, whereas the harmonic resonances and propagation along a distribution feeder installing with multiple shunt-connected capacitors can

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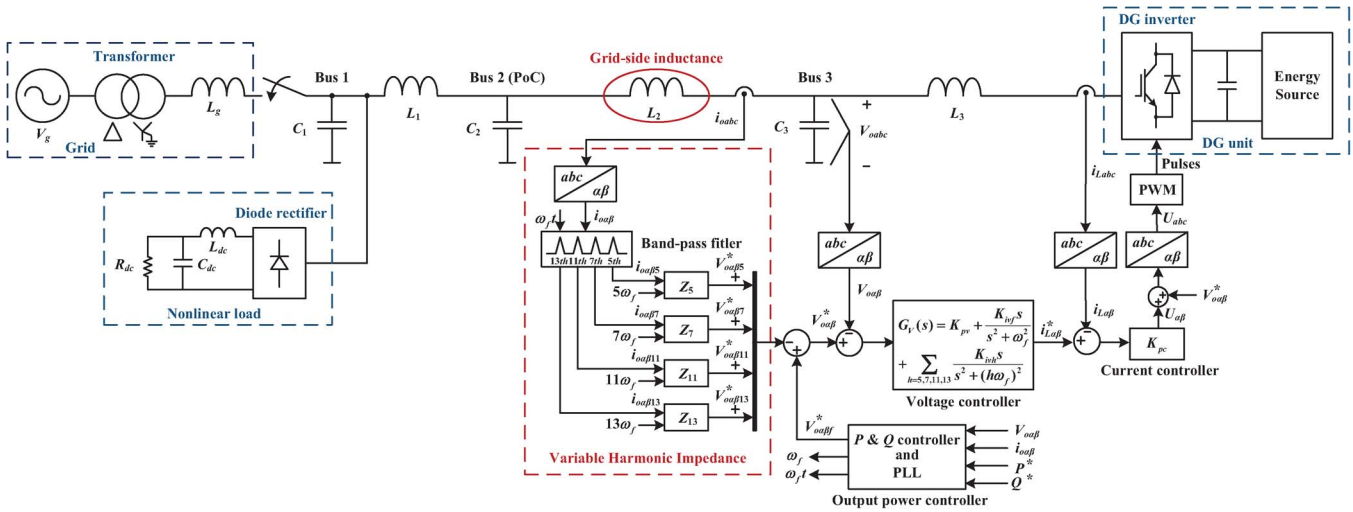


Fig. 1. Simplified one-line diagram of a three-phase distribution system and the associated control scheme.

be effectively attenuated by the positive harmonic resistances. Simulation and laboratory test results are shown to confirm the performance of the proposed control method.

II. Variable Harmonic Impedance Concept

Fig. 1 shows a simplified one-line diagram of a three-phase distribution system and the associated control scheme. The inverter-interfaced DG unit is connected to the grid with an LC-filter (L_3 and C_3), whereas L_2 denotes the grid-side inductance of the DG inverter including the distribution line inductance to the PoC of the DG unit (Bus 2). The dc-link voltage of the DG inverter is controlled by the energy source side, and a constant dc voltage is assumed. A static switch is used to switch the distribution system between grid-connected and islanded operations. Two shunt-connected capacitors (C_1 and C_2) are introduced to represent the aggregated capacitors for the LC-filters in a number of grid-connected converters and the capacitive household loads [4]. A three-phase diode rectifier load is fed from the point of common coupling of the distribution system, Bus 1, which disturbs bus voltages with harmonic current. The harmonic resonances between the line inductances and shunt-connected capacitors arise at different conditions.

To allow the DG unit to operate in both grid-connected and islanded modes, the output voltage of DG inverter needs to be controlled. Thus, the closed-loop dynamic behavior of the voltage control loops of the DG inverter has an important effect on the harmonic distortions of distribution system. The closed-loop output impedance of the DG inverter not only affects the output voltage distortion but also shifts the harmonic resonant points of the distribution line. Hence, to enable the DG inverter to suppress harmonic voltages throughout a distribution line, a variable harmonic impedance concept that allows the DG inverter to reshape the output impedance at the dominant harmonic frequencies is proposed.

In order to synthesize the variable harmonic impedance for a voltage-controlled DG inverter, a multiloop control scheme is employed, which includes 1) an inner proportional inductor

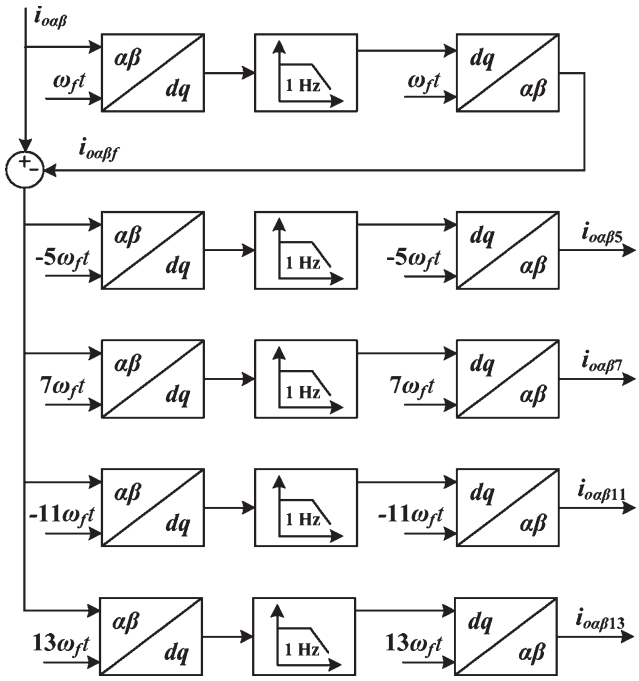


Fig. 2. Block diagram of the multiple reference frame-based bandpass filters.

(L_3) current control loop for overcurrent protection and better LC-filter resonance damping [10], 2) an outer capacitor (C_3) voltage control loop using the proportional plus multiple resonant regulators for selective harmonic compensation, and 3) a selective load harmonic current feedforward loop based on the use of the multiple reference frame (MRF)-based band-pass filters (BPF) [11].

Fig. 2 shows the block diagram of MRF-based BPF. A first-order low-pass filter (LPF) with 1-Hz cutoff frequency is used in each reference frame to extract the dc component. Fig. 3 shows the time response of the MRF-based BPF for a distorted input current in the $\alpha\beta$-frame.

Fig. 4 shows the block diagrams of the proposed variable harmonic impedance. Different from the conventional virtual impedance schemes for the sharing of nonlinear loads among parallel-connected inverters [12], [13], the proposed variable

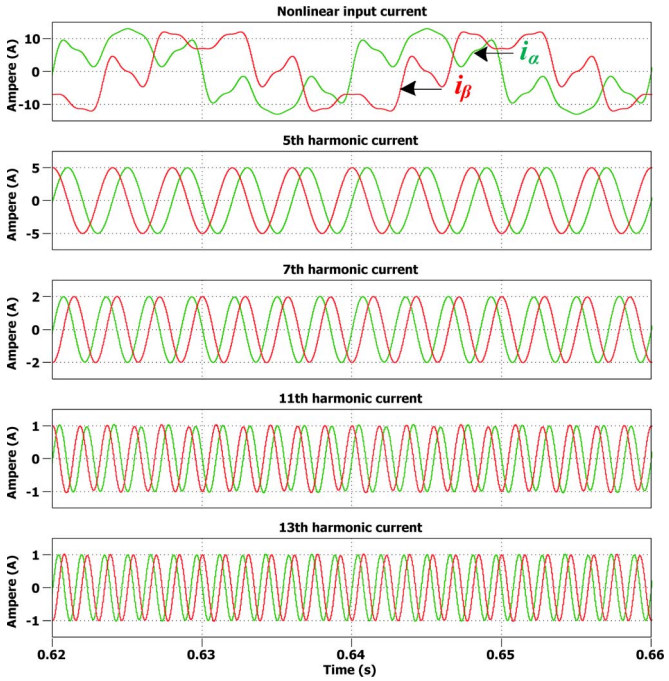


Fig. 3. Performance of the multiple reference frame-based bandpass filters for a distorted input current in the $\alpha\beta$-frame.

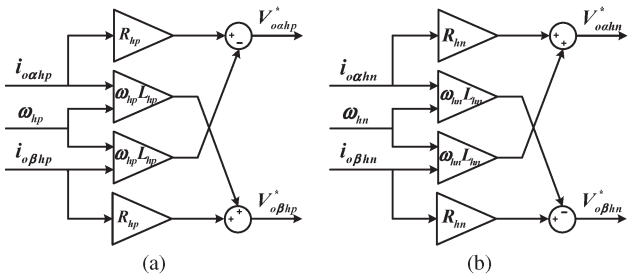


Fig. 4. Block diagrams of the proposed variable harmonic impedance. (a) Positive-sequence harmonic impedances (Z_7, Z_{13}). (b) Negative-sequence harmonic impedances (Z_5, Z_{11}).

harmonic impedance consists of the negative inductances and the positive resistances at the dominant harmonic frequencies, which can be given by

$$\begin{pmatrix} V^*_{o\alpha hp} \\ V^*_{o\beta hp} \end{pmatrix} = \begin{pmatrix} R_{hp} & -\omega_{hp}L_{hp} \\ \omega_{hp}L_{hp} & R_{hp} \end{pmatrix} \begin{pmatrix} i_{o\alpha hp} \\ i_{o\beta hp} \end{pmatrix} \quad (1)$$

$$\begin{pmatrix} V^*_{o\alpha hn} \\ V^*_{o\beta hn} \end{pmatrix} = \begin{pmatrix} R_{hn} & \omega_{hn}L_{hn} \\ -\omega_{hn}L_{hn} & R_{hn} \end{pmatrix} \begin{pmatrix} i_{o\alpha hn} \\ i_{o\beta hn} \end{pmatrix} \quad (2)$$

where the terms "hp" and "hn" are used to denote the positive-sequence ($+$7th and $+$13th) harmonic components and the negative-sequence ($-$5th and $-$11th) harmonic components, respectively. Notice that the proposed harmonic impedances for the positive-sequence harmonic currents are conjugated to the ones for the negative-sequence harmonic currents.

With the synthesized harmonic impedance, the closed-loop output impedance of the DG inverter can be reshaped with the negative inductances and positive resistances at the dominant harmonic frequencies. Thus, the harmonic voltage drop across the grid-side inductance can be counteracted to a large extent by the synthesized negative inductances, which has the same effect as the PoC voltage feedforward control reported in [9]. On the other hand, it is known that a low resistance installed at the end bus of a distribution feeder can damp the harmonic resonance propagation [14]. Hence, in addition to the reduction of the harmonic inductances, the synthesized positive resistances can terminate the harmonic voltage amplifications at the PoC of DG inverter when harmonic resonance occurs around the low-order harmonic frequencies.

Furthermore, in the case that multiple DG units are spread in a long-distance distribution feeder, a centralized harmonic resonance damping controller enabled by the low-bandwidth communication technique can be adopted in combination with the variable harmonic impedance concept [15].

III. Variable Harmonic Impedance Implementation

A. Output Impedance Analysis of DG Inverter

From Fig. 1, it can be seen that the synthesis of variable harmonic impedance not only relies on the decomposition of the load current, but also depends on the dynamic behavior of the voltage control loops of the DG inverter. Similar to the conventional virtual impedance loop, the closed-loop transfer function of the output voltage control affects the shape of the synthesized harmonic impedance [16].

Fig. 5 shows the per-phase Thevenin equivalent circuit for the DG inverter. Based on the control diagram given in Fig. 1, the closed-loop dynamic behavior of inverter voltage control system can be described as follows:

$$V_o(s) = G_{cl}(s)V_o^*(s) - Z_o(s)I_o(s) \quad (3)$$

where $V_o(s)$ and $V_o^*(s)$ are the actual and reference inverter output voltages, respectively, $G_{cl}(s)$ is the voltage reference-to-output transfer function, $I_o(s)$ is the load current, and $Z_o(s)$ is the output impedance of DG inverter

$$G_{cl}(s) = \frac{V_o(s)}{V_o^*(s)}\Big|_{I_o(s)=0} = \frac{K_{pc}G_d(s)G_V(s)}{L_3C_3s^2 + C_3\left(K_{pc}G_d(s)+R_3\right)s + K_{pc}G_d(s)G_V(s)} \quad (4)$$

$$Z_o(s) = \frac{V_o(s)}{-I_o(s)}\Big|_{V_o^*(s)=0} = \frac{L_3s + R_3 + K_{pc}G_d(s)}{L_3C_3s^2 + C_3\left(K_{pc}G_d(s)+R_3\right)s + K_{pc}G_d(s)G_V(s)} \quad (5)$$

$$G_d(s) = \frac{1}{1+1.5T_Ss} \quad (6)$$

where R_3 is the inner parasitic resistance of inductance L_3, K_{pc}, and $G_V(s)$ are the current and voltage regulators, respectively. $G_d(s)$ denotes 1.5 sampling period (T_S) delay including the computational delay (T_S) and the PWM $(0.5T_S)$ delay [17].

Taking the load current feedforward loop into account, the inverter output voltage reference can be derived by

$$V_o^*(s) = V_{of}^*(s) - Z_h(s)I_o(s) \quad (7)$$

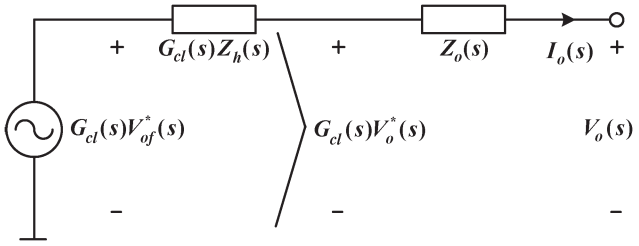


Fig. 5. Per-phase Thevenin equivalent circuit for the closed-loop voltage-controlled DG inverter.

TABLE I
PARAMETERS FOR DG INVERTER AND THE DESIGNED CONTROLLER

Parameters		Values
Output *LC*-filters	L_3	1.5 mH
	R_3	0.04 Ω
	C_3	25 μF
Grid-side inductance	L_2	3 mH
Sampling period	T_S	50 μs
Current controller	K_{pc}	20
Voltage controller $G_V(s)$	K_{pv}	0.1
	K_{ivf}	300
	K_{iv5}= K_{iv7}	60
	K_{iv11}= K_{iv13}	30
	ω_f	100π rad/s
Variable harmonic impedance Z_h=R_h+$jh\omega_f L_h$ (h=5, 7, 11, 13)	R_h	4 Ω
	L_h	-2 mH

where $V_{of}^*(s)$ is the fundamental frequency voltage reference derived from the output power controller, as shown in Fig. 1. $Z_h(s)$ is the synthesized harmonic impedance, which can be described in the stationary frame as

$$Z_h(s) = \sum_{h=5,7,11,13} \frac{2\omega_c \left(R_h s - (h\omega_f)^2 L_h\right)}{s^2 + 2\omega_c s + (h\omega_f)^2} \tag{8}$$

where the MRF-BPF is transformed into the stationary frame using the following equivalence [18]:

$$H_{BPF}(s) = H_{LPF}\left(\frac{s^2 + (h\omega_f)^2}{2s}\right) = \frac{2\omega_c s}{s^2 + 2\omega_c s + (h\omega_f)^2} \tag{9}$$

where ω_c is the cutoff frequency of the LPF in the multiple rotating reference frames, which in this case has a bandwidth of 1 Hz (see Fig. 2). With this transformation, the effect of the $Z_h(s)$ can be analyzed in the closed-loop transfer function.

Substituting (7) into (3), the closed-loop transfer function of the inverter voltage control system becomes

$$V_o(s) = G_{cl}(s)V_{of}^*(s) - G_{cl}(s)Z_h(s)I_o(s) - Z_o(s)I_o(s). \tag{10}$$

Thus, with the load current feedforward loop, the total output impedance of the DG inverter $Z_{to}(s)$ can be given by

$$Z_{to}(s) = G_{cl}(s)Z_h(s) + Z_o(s) \tag{11}$$

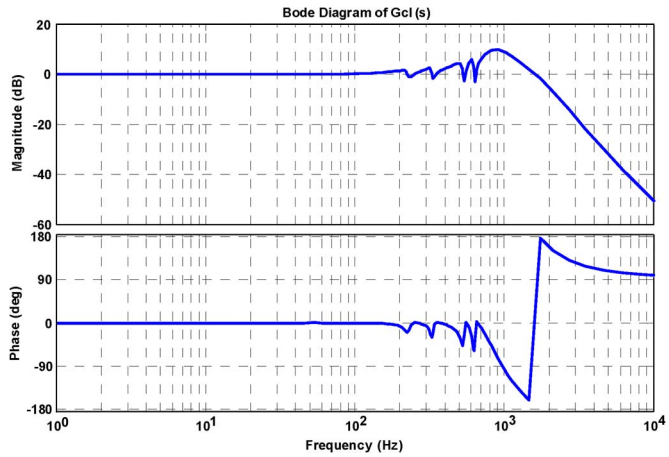


Fig. 6. Bode diagram of the inverter reference-to-output voltage transfer function $G_{cl}(s)$.

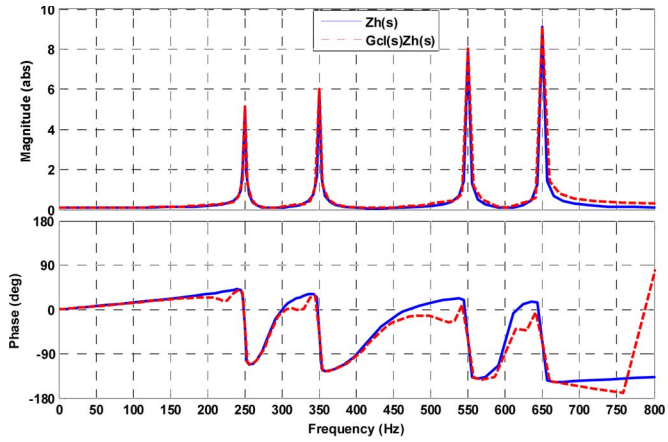


Fig. 7. Frequency-domain responses of the designed harmonic impedances $Z_h(s)$ (blue solid line) and the actual harmonic impedance $G_{cl}(s)Z_h(s)$ (red dash line) of DG inverter.

which implies the term $G_{cl}(s)Z_h(s)$ is the actual harmonic impedance that reshapes the output impedance of the inverter. Therefore, the multiple resonant voltage regulators are needed to ensure the $G_{cl}(s)$ with unity gains and zero phase shifts at the dominant harmonic frequencies, such that the synthesized harmonic impedance can reflect the output impedance at the dominant harmonic frequencies. Furthermore, to enable the DG inverter to operate in the microgrid applications where the system frequency deviates slightly, the frequency adaptive resonant regulators with two integrators are used in the output voltage controller of the DG inverter [19].

Table I summarizes the parameters of the DG inverter and the designed control system. Based on these parameters, the Bode diagram of the $G_{cl}(s)$ is shown in Fig. 6, from which a good reference tracking at the dominant harmonic frequencies can be observed.

Fig. 7 shows a comparison between the frequency-domain responses of the synthesized harmonic impedance $Z_h(s)$ and the harmonic impedance $G_{cl}(s)Z_h(s)$. It can be seen that no magnitude and phase divergences exit between the $Z_h(s)$ and $G_{cl}(s)Z_h(s)$ at the dominant harmonic frequencies.

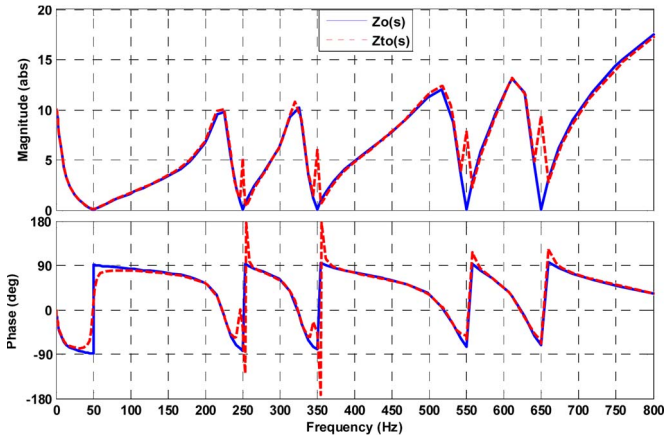


Fig. 8. Frequency-domain responses of the output impedance $Z_o(s)$ (blue solid line) and the total output impedance $Z_{to}(s)$ (red dash line).

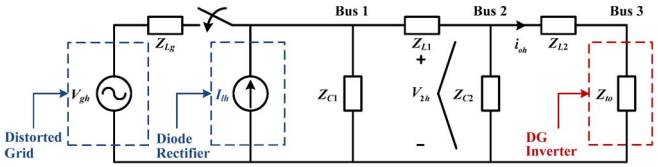


Fig. 9. Per-phase equivalent circuit of the distribution system at harmonic frequencies.

TABLE II
PARAMETERS OF THE ANALYZED DISTRIBUTION SYSTEM

Parameters		Values
Line inductance	L_g	3.8 mH
	L_1	1.8 mH
Shunt-connected capacitor	$C_1 = C_2$	50 μF
Diode rectifier	L_{dc}	84 μH
	C_{dc}	235 μF
	R_{dc}	192 Ω
Injected power of inverter (Grid-connected mode)	P	1 kW
	Q	0.3 kVar

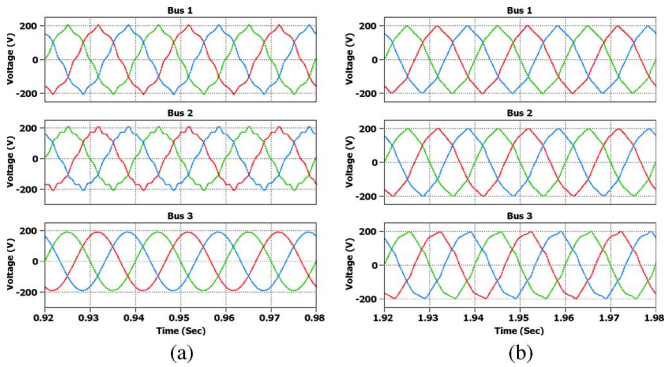


Fig. 10. Simulated bus voltages under the sinusoidal grid condition. (a) Without the synthesized harmonic impedance. (b) With the synthesized harmonic impedance.

The magnitude of the $Z_h(s)$ can be obtained by

$$|Z_h(s)| = \sqrt{R_h^2 + (h\omega_f L_h)^2}. \quad (12)$$

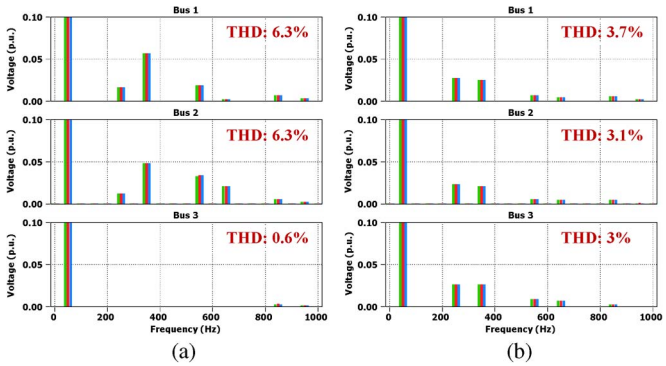


Fig. 11. Simulated harmonic spectra of bus voltages under the sinusoidal grid condition. (a) Without the synthesized harmonic impedance. (b) With the synthesized harmonic impedance.

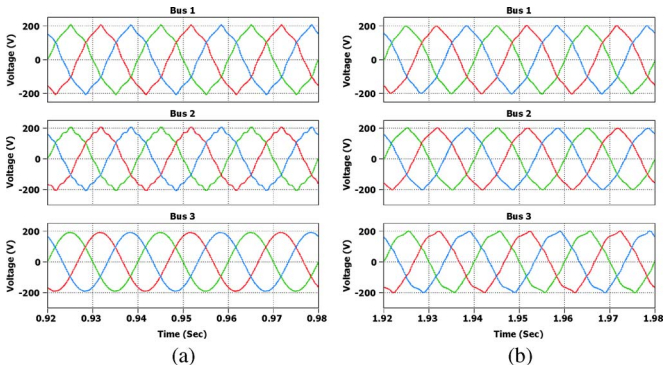


Fig. 12. Simulated bus voltages under the distorted grid condition. (a) Without the synthesized harmonic impedance. (b) With the synthesized harmonic impedance.

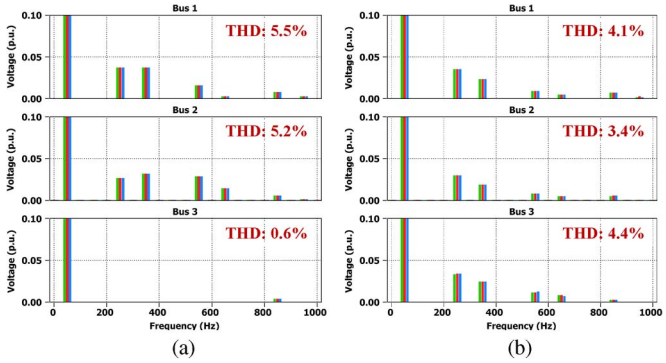


Fig. 13. Simulated harmonic spectra of bus voltages under the distorted grid condition. (a) Without the synthesized harmonic impedance. (b) With the synthesized harmonic impedance.

Since the synthesized inductance is negative, the phase angle of the $Z_h(s)$ is negative at the dominant harmonic frequencies.

Fig. 8 shows the difference between the output impedance $Z_o(s)$ and the total output impedance $Z_{to}(s)$ of DG inverter. It can be seen that the inverter output impedance is reshaped by the synthesized harmonic impedance $Z_h(s)$ at the dominant harmonic frequencies.

B. Design of Negative Harmonic Inductance

Fig. 9 gives the per-phase equivalent circuit of the analyzed distribution system shown in Fig. 1 at harmonic frequencies. As

TABLE III
MAGNITUDES OF SIMULATED HARMONIC VOLTAGES AND THD AT EACH BUS IN THE GRID-CONNECTED OPERATION

Grid condition	Bus No.	V_{5th} (%)		V_{7th} (%)		V_{11th} (%)		V_{13th} (%)		THD (%)	
		Without	*With*	*Without*	*With*	*Without*	*With*	*Without*	*With*	*Without*	*With*
Sinusoidal grid	Bus 1	1.6	2.7	5.7	2.5	1.8	0.7	0.3	0.4	6.3	3.7
	Bus 2	1.2	2.3	4.8	2.0	3.3	0.5	2	0.5	6.3	3.1
	Bus 3	0	2.6	0	2.6	0	0.9	0	0.6	0.6	3
Distorted grid	Bus 1	3.6	3.5	3.7	2.3	1.5	0.9	0.2	0.4	5.5	4.1
	Bus 2	2.6	2.9	3.2	1.8	2.8	0.7	1.4	0.4	5.2	3.4
	Bus 3	0	3.3	0	2.3	0	1.1	0	0.7	0.6	4.4

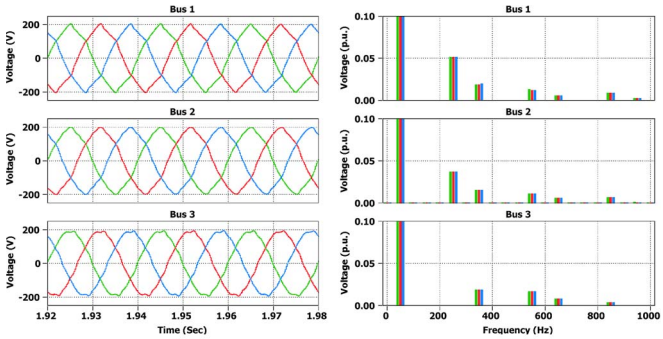


Fig. 14. Simulated bus voltages and the associated harmonic spectra in the case that zero fifth harmonic impedance is synthesized.

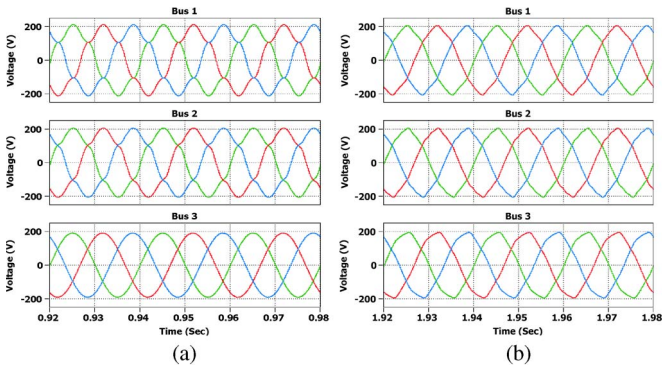


Fig. 15. Simulated bus voltages during the islanded operation. (a) Without the synthesized harmonic impedance. (b) With the synthesized harmonic impedance.

discussed above, the DG inverter can be simply equivalent as the total output impedance Z_{to}. Z_{C1}, Z_{C2}, Z_{L1}, and Z_{L2} denote the harmonic impedances for C_1, C_2, L_1, and L_2, respectively. The background grid distortion can be modeled as a harmonic voltage source in series with the grid impedance Z_{Lg}, whereas the diode rectifier is equivalent as a harmonic current source for simplicity.

Since the synthesized harmonic impedance Z_h reshapes the total output impedance at the dominant harmonic frequencies, the dominant harmonic voltages at the PoC of DG inverter (Bus 2), V_{2h}, can be obtained as follows:

$$V_{2h} = i_{oh}\left(R_h + jh\omega_f(L_h + L_2)\right) \tag{13}$$

where i_{oh} denotes the load current at the dominant harmonic frequencies. Thus, the transient harmonic load current can be

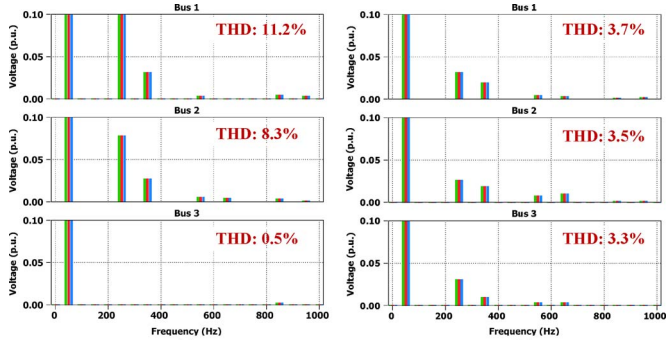


Fig. 16. Simulated harmonic spectra of bus voltages during the islanded operation. (a) Without the synthesized harmonic impedance. (b) With the synthesized harmonic impedance.

given by

$$i_{oh} = \frac{V_{2h}}{R_h} - \frac{V_{2h}}{R_h} e^{-R_h t/(L_h + L_2)}. \tag{14}$$

Thus, to preserve a stable transient response of the harmonic load current, the following condition should be met:

$$L_h + L_2 > 0 \tag{15}$$

where $L_h < 0$ and $L_2 > 0$.

Furthermore, taking into account a 20% variation of the grid-side inductance in practical applications, the size of the L_h can be designed as

$$0.3L_2 \le |L_h| \le 0.8L_2. \tag{16}$$

If the $|L_h|$ is higher than 80% of the grid-side inductance, the closed control loop tends to be unstable, whereas selecting the $|L_h|$ less than 30% will be hard to obtain an apparent effect on reducing the harmonic inductance at the PoC of DG inverter.

IV. SIMULATION RESULTS

To evaluate the performance of the proposed controller, the three-phase distribution system shown in Fig. 1 is built both in simulations and laboratory. Table II summarizes the circuit parameters of the built distribution system, whereas the DG inverter is built using the parameters listed in Table I.

A. Grid-Connected Operation

Fig. 10 shows the simulated bus voltages before and after using the proposed variable harmonic impedance under the

TABLE IV
MAGNITUDES OF SIMULATED HARMONIC VOLTAGES AND THD AT EACH BUS IN THE ISLANDED OPERATION

Bus No.	V_{5th}(%)		V_{7th}(%)		V_{11th}(%)		V_{13th}(%)		THD (%)	
	Without	*With*	*Without*	*With*	*Without*	*With*	*Without*	*With*	*Without*	*With*
Bus 1	10.7	3.2	3.1	1.9	0.3	0.4	0	0.2	11.2	3.7
Bus 2	7.8	2.7	2.7	1.8	0.5	0.8	0.4	1.0	8.3	3.5
Bus 3	0	3.1	0	1.0	0	0.3	0	0.3	0.5	3.3

sinusoidal grid condition. Only the diode rectifier load is the harmonic source, and the grid voltage in Fig. 9 can be short-circuited. Fig. 11 shows the corresponding harmonic spectra of bus voltages.

Fig. 10(a) shows the bus voltages without the synthesized harmonic impedance. The output voltage of the DG inverter (Bus 3) is sinusoidal which justifies the frequency responses shown in Fig. 6. Thus, the Bus 3 in Fig. 9 can be short-circuited. Consequently, the dominant harmonic voltages at the PoC of DG inverter (Bus 2) are the harmonic voltage drops across the grid-side inductance. From Fig. 11(a), it can be seen that the harmonic voltage is amplified around the seventh harmonic frequency.

The bus voltages with the synthesized harmonic impedance are shown in Fig. 10(b). The voltage at the Bus 3 is distorted, due to the harmonic currents flowing through the synthesized harmonic impedance. However, the equivalent impedance at the Bus 2 is then dominated by the positive resistances at the dominant harmonic frequencies. Thus, the seventh harmonic voltages can be effectively damped, as shown in Fig. 11(b).

Fig. 12 shows the simulated bus voltages under distorted grid condition, where the grid voltage is distorted with the 2% fifth and 2% seventh harmonics. The corresponding harmonic spectra of the bus voltages are depicted in Fig. 13. In this case both the distorted grid voltage source and the nonlinear load current source shown in Fig. 9 affect the harmonic distortions of bus voltages. From Fig. 13(a), it can be seen that both the fifth and the seventh harmonic voltages are amplified without the synthesized harmonic impedance. It implies the harmonic resonant point is shifted toward the fifth harmonic frequency due to the presence of the background grid distortion. Similar to the sinusoidal grid condition, the voltage at Bus 3 becomes distorted with the synthesized harmonic impedance, whereas the other bus voltages are improved.

Table III shows the magnitudes of the dominant harmonic voltages and the total harmonic distortion (THD) for each bus under both sinusoidal and distorted grid conditions. The changes brought by the variable harmonic impedances can be seen.

It is interesting to note that the fifth harmonic voltages are slightly increased in both cases. To see the damping effect of the synthesized impedance at the fifth harmonic frequency, Fig. 14 shows the simulated bus voltages and the associated harmonic spectra under the distorted grid condition, where the fifth harmonic impedance is set zero. Compared Fig. 14(b) to Fig. 13(b), it can be observed that the fifth harmonic voltage is actually reduced by the synthesized impedance. However, the reason for the less reduction of the fifth harmonic voltage lies in the mismatch between the characteristic impedance of distribution feeder and the synthesized harmonic resistance. This phenomenon is also named as the "whack-a-mole" effect in [20]. To avoid such undesired effect, the variable harmonic impedance can be separately designed for each dominant harmonic load current, but this is not adopted in this paper for the sake of simplicity.

B. Islanded Operation

Fig. 15 shows the simulated bus voltages before and after applying the harmonic impedances in the islanded operation. In this case, the grid model in Fig. 9 is open-circuited. Only the diode rectifier load is the harmonic source. Fig. 16 shows the corresponding harmonic spectra of bus voltages.

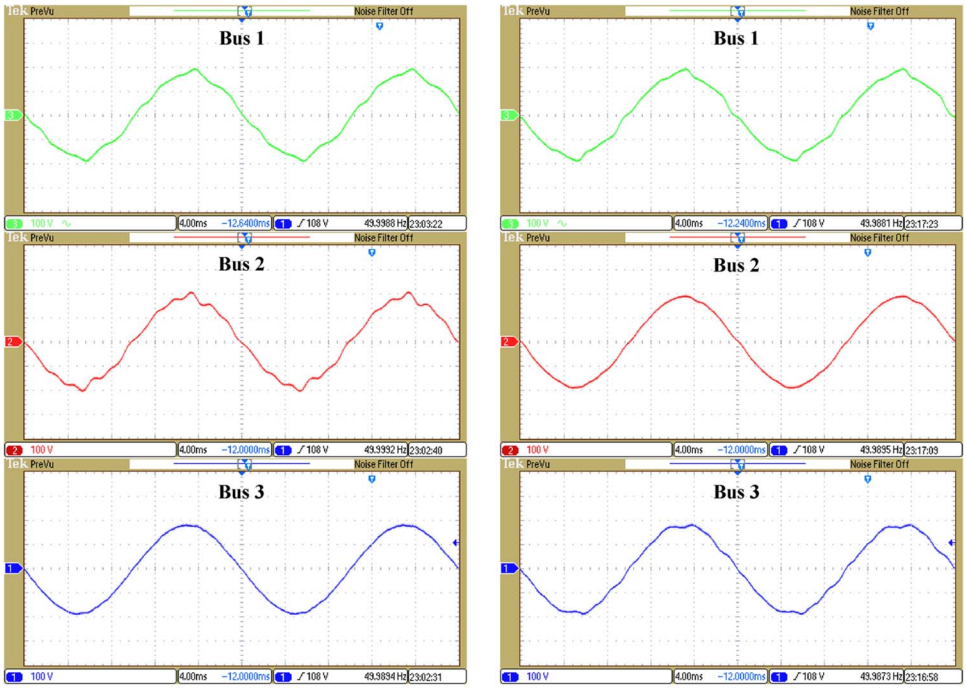
Fig. 15(a) shows the bus voltages without the synthesized harmonic impedance. The Bus 3 in Fig. 9 is short-circuited. The harmonic current generated from the diode rectifier flows through the distribution feeder and causes harmonic voltage distortions at the Bus 1 and Bus 2. Furthermore, from Fig. 16(a), it is obvious that the fifth harmonic voltage amplification occurs due to the resonances between the line inductance and shunt-connected capacitors.

With the synthesized harmonic impedance, the bus voltages are shown in Fig. 15(b). Compared to Fig. 15(a), it can be seen that the voltage waveforms are improved significantly. Fig. 16(b) depicts the corresponding harmonic spectra of bus voltages, where it is obvious that the fifth harmonic resonance propagation is effectively damped by the positive resistances. Also, the seventh harmonic voltages are counteracted by the negative inductances. Since the absence of grid impedance Z_{Lg} changes the characteristic impedance of the distribution feeder, there is no mismatch between the synthesized fifth harmonic resistance and the characteristic impedance. Table IV lists the magnitudes of the dominant harmonic voltages and the bus voltage THDs.

V. EXPERIMENTAL RESULTS

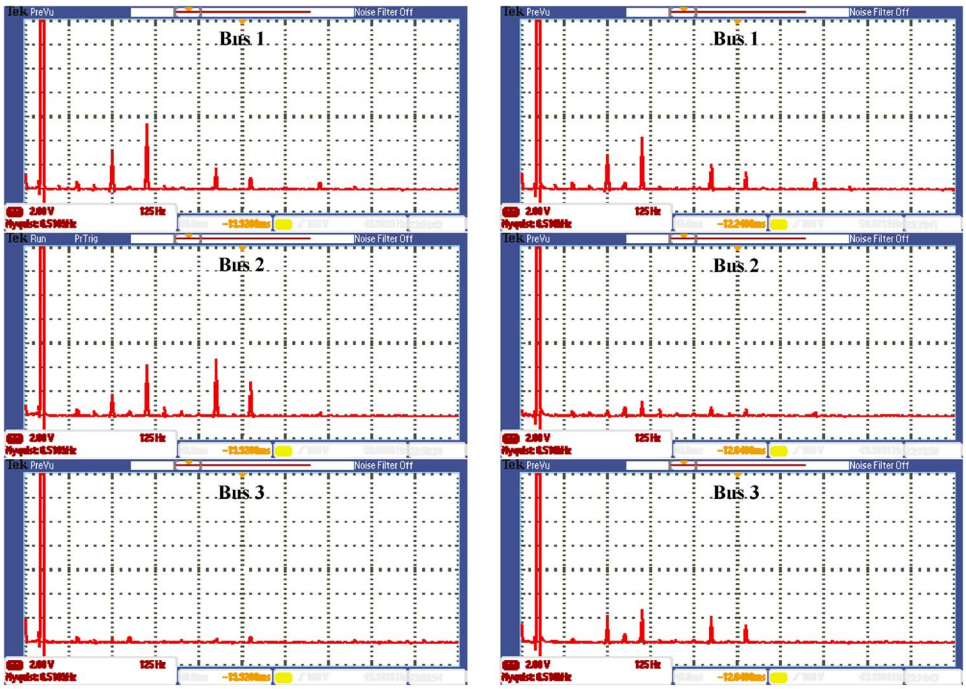
In the laboratory test setup, a 5.5-kW Danfoss frequency converter with a constant dc voltage source is adopted as the DG inverter. The switching frequency of the inverter is 10 kHz. The designed controller with the parameters given in Table I is implemented in the DS1006 dSPACE system.

Fig. 17 shows the measured per-phase bus voltages before and after applying variable harmonic impedances in the grid-connected operation. The corresponding harmonic spectra are shown in Fig. 18. Fig. 17(a) shows the bus voltages without the synthesized harmonic impedance. It can be observed that the output voltage of inverter is sinusoidal and the other buses



(a) (b)

Fig. 17. Measured per-phase bus voltages during the grid-connected operation (4 ms/div, 100 V/div). (a) Without the synthesized harmonic impedances. (b) With the synthesized harmonic impedances.



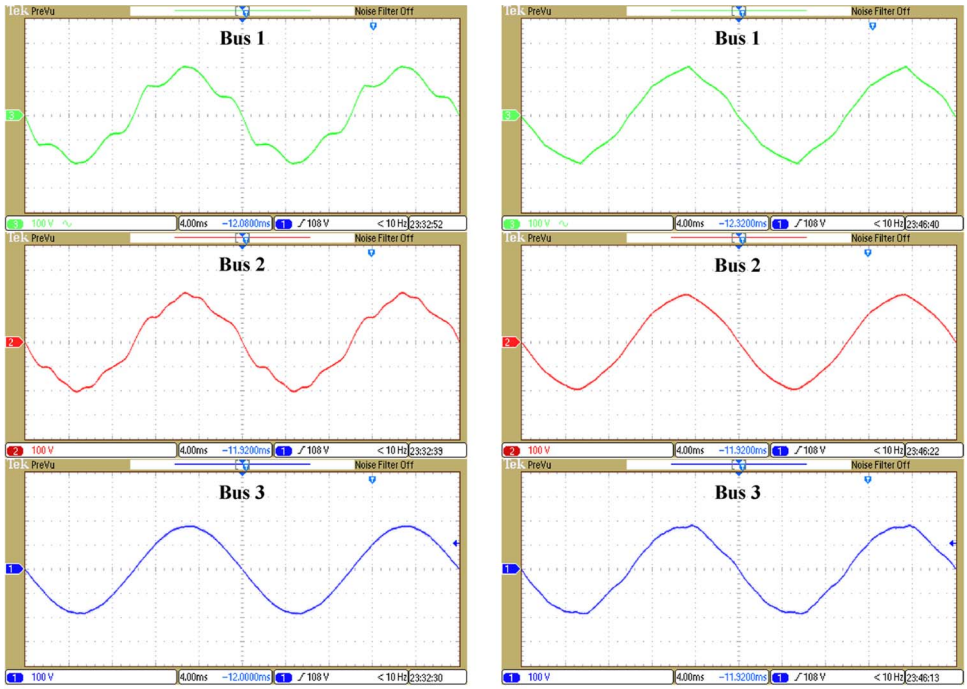
(a) (b)

Fig. 18. Harmonic spectra of the measured per-phase bus voltages during the grid-connected operation (125 Hz/div, 2 V_{RMS}/div). (a) Without the synthesized harmonic impedances. (b) With the synthesized harmonic impedances.

are distorted, which is similar to the simulation results shown in Fig. 12(a). Also, from the measured harmonic spectra in Fig. 18(a), it is seen that the harmonic voltage amplification arises around the seventh harmonic frequency.

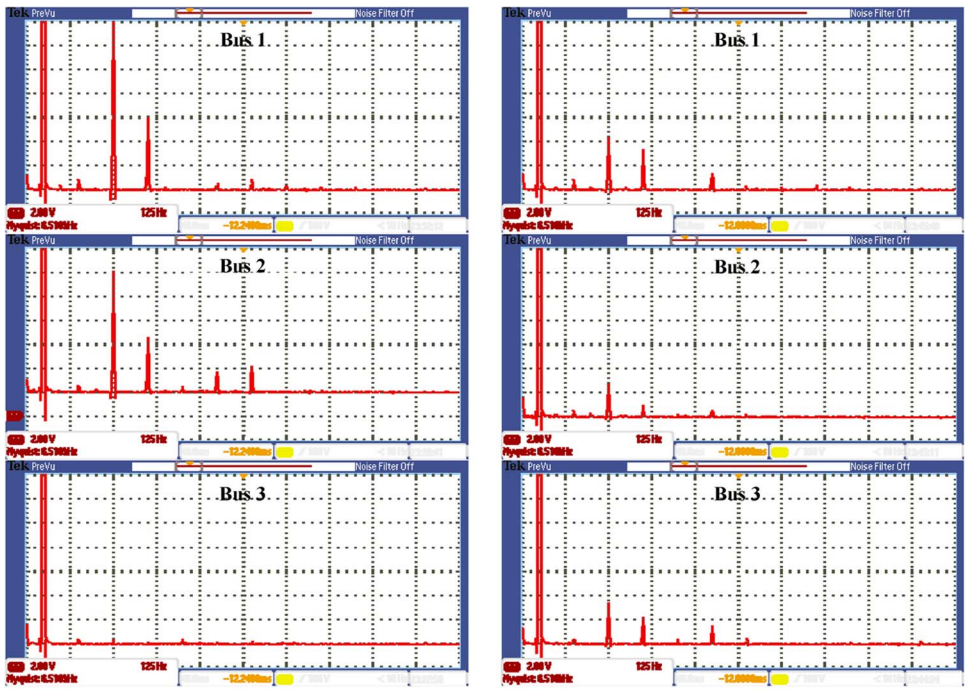
Fig. 17(b) shows the measured voltage waveforms with the synthesized harmonic impedance. It is seen that the voltage at the Bus 3 becomes distorted while the voltage at the Bus 2 is significantly improved. Also, the seventh harmonic resonance is damped as shown in Fig. 18(b).

Fig. 19 shows the measured per-phase bus voltages during the islanded operation, and the associated harmonic spectra of the bus voltages are shown in Fig. 20. Fig. 19(a) shows the



(a) (b)

Fig. 19. Measured per-phase bus voltages during the islanded operation (4 ms/div, 100 V/div). (a) Without the synthesized harmonic impedances. (b) With the synthesized harmonic impedances.



(a) (b)

Fig. 20. Harmonic spectra of the measured per-phase bus voltages during islanded operation (125 Hz/div, 2 V_{RMS}/div). (a) Without the synthesized harmonic impedances. (b) With the synthesized harmonic impedances.

measured voltage waveforms before the synthesized harmonic impedance is applied. It is seen that the voltage at the Bus 3 is sinusoidal while the other bus voltages are severely distorted. From Fig. 20(a), it is obvious that the harmonic resonance propagation occurs at the fifth harmonic frequency, which is similar to the simulation results shown in Fig. 16(a). With the synthesized harmonic impedance, the voltage at the Bus 3 is distorted while the voltages at the other buses are significantly improved, as shown in Fig. 19(b). Also, from Fig. 20(b), it is clearly seen that the fifth harmonic voltage amplifications are effectively damped. Table V summarizes the magnitudes of measured harmonic voltages in grid-connected and islanded

TABLE V
MAGNITUDES OF MEASURED HARMONIC VOLTAGES AT EACH BUS IN LABORATORY TESTS

Operation mode	Bus No.	V_{5th} (V)		V_{7th} (V)		V_{11th} (V)		V_{13th} (V)	
		Without	*With*	*Without*	*With*	*Without*	*With*	*Without*	*With*
Grid-connected	Bus 1	3.2	2.8	5.6	4.2	1.8	2.0	0.8	1.6
	Bus 2	1.6	0.4	4.2	1.2	4.6	0.6	2.8	0.4
	Bus 3	0	2.2	0	2.8	0	2.0	0	1.4
Islanded	Bus 1	20	4.4	6	3.2	0.4	1.2	0.8	0
	Bus 2	10	2.8	4.6	0.8	1.8	0.4	2.0	0
	Bus 3	0	3.4	0	2.0	0	1.6	0	0.4

operation. Notice that the magnitudes of the harmonic voltage depicted in the harmonic spectra are RMS values.

VI. CONCLUSION

This paper has discussed a variable harmonic impedance synthesis method for voltage-controlled DG inverters in order to perform harmonic damping on a distribution feeder. In the approach, the negative inductances and positive resistances are synthesized based on a selective load current feedforward loop. Thus, the harmonic voltage reduction in the presence of large grid-side inductance, and the damping of the harmonic resonances caused by the multiple shunt-connected capacitors can be achieved at the same time. The theoretical analysis and the expected performance of the control scheme have been validated through simulations and laboratory tests.

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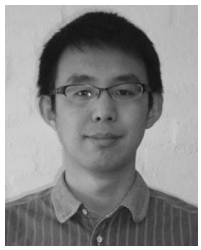

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