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High efficiency battery converter with SiC devices for residential PV systems

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Keywords

«SiC VJFETs», «SiC MOSFETs», «Bidirectional DC-DC converter», «High efficiency», «Battery storage converter».

Abstract

The demand for high efficiency and higher power density is a challenge for Si-based semiconductors due to the physical characteristics of material. These can be overcome by employing wide-band-gap materials like SiC. This paper compares a second generation SiC MOSFETs against a normally-on Trench JFETs and their performances in a high efficiency battery converter for residential photovoltaic systems. The prototypes are 3 kW converters with more than 98% efficiency and high simplicity and power density.

1. Introduction

Photovoltaic (PV) converters are some of those applications which are demanding for power electronic converters with high efficiency and power density. This is a challenge for Si-based power switches and to overcome the limitations given by the material of this semiconductor device, compound materials with wide-band-gap (WBG) like SiC can be used [1]. The high efficiency is a very important factor for the PV industry, where the generated energy price is relatively high. Smart PV systems with internal battery storage as shown in Figure 1 enable maximization of self-consumption and support the grid by storing overproduction or injecting power during peak load. World leader in terms of cumulative PV installation, Germany, who is showing a constant commitment from policymakers to support the integration of PV, has recently launched a financial support program for residential PV systems with battery storage [2]. Furthermore the potential for the end users to trading electricity with spot price and maximize the system and shorter the payback time, thus a high efficiency bidirectional converter is essential, due to the energy is processed twice; during storing and discharging. The structure of the paper is following: Chapter 1 introduces the application, Chapter 2 presents the topology and design specifications of the battery converter using either SiC MOSFET or JFET switches to obtain high

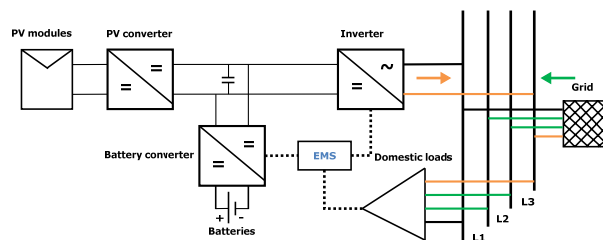


Figure1: Block overview of Smart PV systems.

efficiency, Chapter 3 is the design and loss calculations of the 3 kW bidirectional converter, including the inductor design and practical considerations, Chapter 4 presents the results and Chapter 5 concludes the work.

2. Converter topology and operation

Bidirectional DC-DC converters can basically be divided into two groups; galvanic isolated and non-isolated. In many applications galvanic isolation is mandatory, however, this adds more complexity to the converter topology. On the other hand, the efficiency of the converter is tight related to the components which process the power and the number of devices. For non-isolated applications with high efficiency, a simple buck-boost bidirectional DC-DC converter topology with very few components, as sketched in Figure 2, can be used.

When the energy is fed from the battery, by S1 and L1 the battery voltage can be boosted and S2 and C2 will rectify/block and smooth the DC link voltage. To store the energy, S2 will buck the DC link voltage, S1 will provide the freewheeling current path and L1 and C1 filter the switched

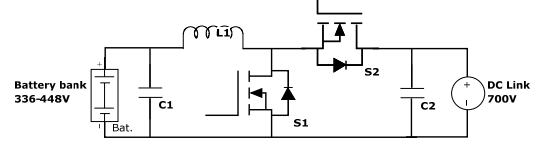


Figure 2: A simple bidirectional DC-DC converter.

voltage. Since the current is flowing in both directions, unipolar transistors like MOSFETs and JFETs which enable third quadrant conduction can be used to reduce the numbers of components. Furthermore, active freewheeling and synchronous rectifying can be implemented to yield higher efficiency. For a three phase system a DC link voltage of 700 V DC is required, in order to be able to feed energy back to the grid. To keep inside the safe operating area (SOA) of the devices, 1200 V switches are often used for 700 V applications. The commercially 1200V Si devices are not preferable for implementation in this case, due to poor conduction and switching characteristics. To have high performances the DC-link voltage can be split into +350V and -350V and use 600/650 V Si super junction devices. By using SiC devices with 1200V blocking capability and low switching losses, the more simple topology can be used without dc-bus split and fewer components.

2.1. SiC semiconductors

Among the WBG semiconductors, SiC technology based devices are now available as Diodes, BJTs, MOSFETs and JFETs (both normally-on and normally-off). In terms of semiconductor properties, Table 1 highlights some important physical characteristics of Si and 4H-SiC polytype. With higher energy gap SiC devices can operate at higher temperature and higher thermal conductivity, the heat is removed more efficient than Si. Furthermore with higher breakdown field, the on-resistance is smaller; for the same blocking voltage level, and higher drift velocity gives a faster switching device. These

Table 1: Physical characteristics of Si and 4H-SiC [1].

Property	Si	4H-SiC
Bandgap (eV)	1.12	3.26
Dielectric constant	11.9	10.1
Electric breakdown field (kV/cm)	300	2.200
Saturated electron drift velocity (10^7 cm/s)	1	2
Thermal conductivity (W/cm·K)	1.5	4.9

remarkable properties lead to higher blocking voltage devices with lower switching and conduction losses and can be operated in higher ambient temperatures. Realizing the converter with SiC can reduce the number of devices, increase the efficiency, enable higher switching frequency which reduces the size of the output filter and magnetic components. Compare to Si at the same switching frequency and power output, this will ease the thermal management due to lower power losses and higher thermal conductivity. To find the best available SiC transistor, Rubino et. al. [3] have compared the performances of a SiC BJT, a normally-off trench JFET and a MOSFET in the 1200 V class. In terms of main static and dynamic characteristics as function of temperature and the driving requirements, the MOSFET seems to have better performance than the BJT and the normally-off Trench JFET, but the question is: are SiC MOSFETs also better than SiC normally-on JFETs? To answer this question, these two devices will be compared and implement in a 3 kW bidirectional DC-

DC converter with very high efficiency for PV application, one using the second generation SiC MOSFETs and the other with SiC normally-on trench JFETs. The converter design specifications can be seen in Table 2 and the power capability can be increased by interleaved switching another phase, thus this will not worsening the efficiency.

Table 2: Design specifications of the DC-DC converters.

Power	Vin	Vout	Switching topology scheme	Max η
3 kW	Boost: 336-448 V	Boost: 700 V	Hard switching with active freewheeling/rectification	> 0.98
	Buck: 700 V	Buck: 336-448 V		

2.2. SiC MOSFETs and normally-on JFETs

JFET has more advantages as a normally-on device, however recently normally-off devices were also available. The designing of the normally-off JFETs implies sacrificing some on-state resistance [4] and require a dedicate gate drive, which is relative complex in the design [5]. Normally-on switches are not easily accepted in power electronic applications due to system safety requirements, for example during power up or loss of gate driver supply, where they act as a short circuit. To have the normally-off behavior with normally-on devices, cascode configuration can be used, where a normally-off low voltage MOSFET is series connected as shown in Figure 3. This has the inherently off-behavior, for example during power up, the JFET is normally-on and the MOSFET is normally-off, this brings the potential at the source of JFET to the same as at the Drain. The Gate of the JFET is tied to the GND, thus gate-source potential difference becomes now negative and the JFET switches to off-state. Off-the-shelf MOSFET gate drives can be used in this configuration and another advantage is the freewheeling and rectification functionality without additional antiparallel diode, this is possible due to the reverse current flow through body-diode of the low voltage MOSFET. The voltage at the source of JFET will be negative biased; and is equal to the voltage drop across the body-diode, this positive gate-source biased of the JFET will turn on the JFET. Other variation of this configuration is also implemented to drive JFETs, like the Capacitive Clamped Cascode, which gives the controllability over the JFET [6] and Direct Driver approach, where the MOSFET only switches off during startup and fault situations. During normal operation of Direct Driver, the JFET is driven direct by the gate circuitry and thus eliminating the additional switching losses of the MOSFET and reduce the possibility of repetitive avalanche during switching off. Furthermore both gate drivers are integrated in an IC, which helps to reduce parasitic components in the gate circuitry [7][8]. SiC MOSFETs are on the other hand normally-off devices, but cannot be direct drop-in of existing design due to the wider gate voltage swing. To have the low on-resistance, it is common to biased the gate +20V during turn-on and like SJ Si MOSFETs, the threshold voltage is in the range of 2V, thus negative bias the devices during turn-off will increase the gate noise immunity, especially at higher junction temperature where the threshold voltage will decrease.

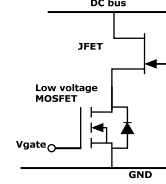


Figure 3: Conventional cascode.

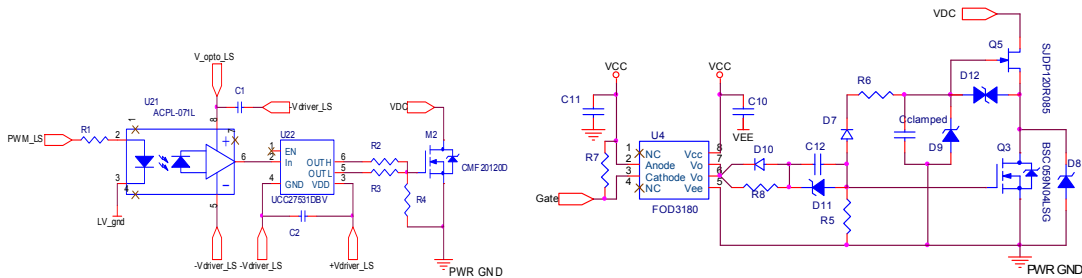


Figure 4: Gate driver solutions; on the left, a gate drive IC solution for SiC MOSFETs and on the right the Capacitive Clamped Cascode driver for normally-on VJFET.

A fast gate driver is needed to utilize the switching speed of the SiC MOSFETs. The transistors which will be used for comparison are C2M0080120D SiC MOSFET against SJDP120R085 normally-on trench JFET (VJFET) in series with BSC059N04LSG Si MOSFET. All switches are unipolar devices and can conduct the current in reverse direction without additional antiparallel diode. Compare to the first generation of SiC MOSFET used in [3], the second generation is cheaper, has lower switching loss, extended the minus gate voltage for improve the immunity, but the on-resistance is more temperature sensitive. The gate driver circuitry for the MOSFETs and the VJFETs are shown in Figure4. Both use off-the-shelf gate driver and are easy to implement. The remarkable difference is that, SiC MOSFET solution needs a negative gate supply to improve the immunity during off-state as mentioned earlier.

Table 3 highlights some key parameters of the devices, as a note the conduction data for the VJFET is including the Si MOSFET.

Table 3: Key parameters of C2M0080120D and SJDP120R085 + BSC059N04LSG.

Parameter	CMF0080120D	SJDP120R085 + BSC059N04LSG
$V_{DS, \min.}$	1200 V	1200 V
$I_{DS@25^{\circ}C, \max.}$	31.6 A	27 A
$I_{DS@100^{\circ}C, \max.}$	20 A	17 A
I_{DS} degradation	36.7 %	37.1 %
$R_{DS(on)} @25^{\circ}C, \text{typ.}$	80 m Ω @20 A I_{DS}	75 m Ω +4.8 m Ω @17 A I_{DS}
$R_{DS(on)} @150^{\circ}C, \text{typ.}$	150 m Ω @20 A I_{DS}	147 m Ω +7.5 m Ω @17 A I_{DS}
$R_{DS(on)}$ Increment	87.5 %	93.6%
Operation temperature range	-55 $^{\circ}C$ - 150 $^{\circ}C$	-55 $^{\circ}C$ - 150 $^{\circ}C$
$R_{thJC}, \max.$	0.65 K/W	1.1 K/W
$Q_g, \text{typ.}$	49.2 nC	32 nC
$E_{sw, \text{tot}} @25^{\circ}C, \text{typ.}$	330 uJ @800V, @17 A I_{DS}	290 uJ @600V, @17 A I_{DS}
Diode Voltage drop@25 $^{\circ}C$, typ.	3.5 V@10 A I_F	1.03 V@10 A I_F

The temperature sensitivity of these devices are higher than Si based, but the conduction and switching losses are still much lower than Si-based; even compare to the SJ technology. The noticeable differences between these devices are; the SiC MOSFET has lower junction-case thermal resistance, lower switching loss but the voltage drop over the intrinsic body diode of the SiC MOSFET is relatively high. The Trench designed JFET does not have this body diode and thus only the body diode of the Si MOSFET is in series, which is much lower than the SiC MOSFET. However if third quadrant conduction can be implemented, this difference of voltage drop across the body diodes is insignificant and the efficiency of the converter will be higher and. With smaller static and dynamic losses, simple gate driver, the SiC MOSFET similar to the well know MOSFET and thus it is the prefer device to use.

3. Converter design

In the converter, shown in Figure 2, the dominant sources of losses are: ESR of the capacitors, core and copper losses in the inductors, switching and conduction losses of the semiconductors.

As shown in Table 1 the converter will process 3 kW. The inductor is used in both boost and buck mode, but the inductance should be designed for boost mode, where it is used as an energy storage element, the energy storage number can be computed as [9]:

$$W_L = 0.5 \cdot L_{boost} \cdot I_L^2 \quad [J] \quad (1)$$

Where L is the inductance in [H] and I_L is its rms current in [A].

Multiply Eq(1) hence the power storage number:

$$P_L = W_L \cdot f_{sw} \quad [W] \quad (2)$$

Where f_{sw} is the switching frequency.

The inductance can be calculated by solving Eq(1) and Eq(2) for the required output power and voltages:

$$L_{boost} = \frac{V_{in}^2 \cdot D_{boost} \cdot 2 \cdot V_{out}}{(V_{out} \cdot I_L \cdot P_{out}) \cdot f_{sw}} \quad [H] \quad (3)$$

Where, V_{in} is the input voltage in [V], D_{boost} is the duty cycle during boost mode [-], V_{out} is the output voltage in [V], I_L is the rms current of the inductor in [A], P_{out} is the output power in [W] and f_{sw} is the switching frequency in [Hz].

The inductance in Eq.1 to Eq.3 is not the required value, but it is used to fulfill another design specification, namely the peak to peak current ripple of the inductor, which can be found as:

$$\Delta I_L = \frac{D_{boost} \cdot V_{in}}{L_{boost} \cdot f_{sw}} \quad [A] \quad (4)$$

The peak current can now be found and the current capability of components is clarified. The core loss in the inductor is determined by the current ripple. From Eq.4 both the inductance and/or the switching frequency can be modified to fulfill the current ripple requirement. By increasing the inductance, more turns can be added, however the copper loss will increase, but this allows the switching frequency to be reduced, which lower the switching losses of the semiconductors and core loss and vice versa, so an optimum can be found between the copper loss and core loss of the inductor.

Since switching losses of SiC devices are relative low and fast switching enable the designer to utilize the SOA of the devices, reduce the size of magnetic and filter components thus fast switching is a better approach. A further utilization is to designed the converter to operate in continuous conduction mode (CCM) with small current ripple; $I_{ac} \ll I_{DC}$, thus this avoid selecting the devices with overrated current capability and due to small current ripple the losses caused by this ac current component; skin effect and core losses is reduced.

Minimize the losses require an optimisation process, for each switches, inductor cores and switching frequency. To demonstrate relatively the high efficiency with SiC transistor, a low cost high permeability core from Micrometals is selected. Switching frequency of 80 kHz is selected and applying this to Eq. 3 gives an inductance of 950μH. Based on this, a 3" toroidal powder core of from 200C series with -63D material from is selected[10], μ_r of this core at 1 OES is 35 and is 31.85 at the maximum operation point; 54 OES. An extra turn is added as a safety margin and the design data of the 969μH@10A inductance is listed in Table 3. It can be seen that 1% of power loss in the converter is caused by the inductor, at rated power.

Table 3: Data for the boost inductor.

Inductance	Stacking	N turns	Winding	DCR	Core loss	Copper loss
969μH	2 x T300-63D	85	30 x 0.2 mm litz	218 mΩ	12.3 W	17.4 W@40°C

With this switching frequency, the reliability of the converter can be improved by using bipolar film capacitors instead of electrolytic capacitors [11]. The main selection criteria here are the rated voltage and ripple current capability. Assuming a it is an ideal converter, in worst case the ripple current can be as much as the peak current at the inductor during the boost mode, which is:

$$\hat{I}_L = I_L + \frac{\Delta I_L}{2} = \frac{P_{out}}{V_{in}} + \frac{D_{boost} \cdot V_{in}}{L_{boost} \cdot f_{sw} \cdot 2} = \frac{3000}{336} + \frac{(1 - \frac{336}{950 \cdot 10^{-6} \cdot 800 \cdot 10^3 \cdot 2}) \cdot 336}{950 \cdot 10^{-6} \cdot 800 \cdot 10^3 \cdot 2} = 10.1 \quad [A] \quad (5)$$

Based on this, a 20μF MKP film capacitor from Epcos is selected, which can handle 12 A and has an ESR of 3.5 mΩ, which causes very low loss and in this case can be neglected.

Eq. 5 can now be used to select the current capability of the switches. With the duty cycle of 0.52 and the switching time of 12.5μs, this gives a pulse length of 6.5us and similar must be done for buck mode. The SOA of CMF0080120D[12] and SJDP120R085[13] verify that both devices can handle more than this current.

3.2 Losses calculation

To estimate the efficiency of the converter, power losses of the semiconductors must be calculated. The losses mechanism in SiC devices are the same as Si based and thus the losses can be estimated as [14]:

$$P_{conduction, MOSFET} = R_{DS, on} \cdot I_{D, on}^2 \quad [W] \quad (6)$$

$$P_{sw, on, MOSFET} = E_{sw, on} \cdot f_{sw} = (V_{DD} \cdot I_{D, on} \cdot \frac{t_{ri} + t_{fu}}{2} + Q_{rr} \cdot V_{DD}) \cdot f_{sw} \quad [W] \quad (7)$$

$$P_{sw, off, MOSFET} = E_{sw, off} \cdot f_{sw} = (V_{DD} \cdot I_{D, off} \cdot \frac{t_{ru} + t_{fi}}{2}) \cdot f_{sw} \quad [W] \quad (8)$$

$$P_{conduction,Diode} = V_{F,0A} \cdot I_{F,average} + R_{Dynamic} \cdot I_{F,rms}^2 \quad [W] \quad (9)$$

$$P_{sw,Diode} = \frac{1}{4} \cdot Q_{rr} \cdot V_{rr} \cdot f_{sw} \quad [W] \quad (10)$$

Where $R_{DS,on}$ is the on-resistance of the MOSFET, $I_{D,on}$ is the on-current through the MOSFET, V_{DD} is the DC link voltage, t_{ri} is the current rise time, t_{fu} is the voltage fall time, Q_{rr} is the reverse recovery charge of the diode, t_{ru} is the voltage rise time, t_{fi} is the current fall time, $V_{F,0A}$ is the forward voltage of the diode at zero current, $I_{F,average}$ is the average forward current of the diode, $R_{Dynamic}$ is the dynamic resistance of the diode, $I_{F,rms}$ is the rms forward current of the diode and V_{rr} is the voltage across the diode during reverse recovery.

Since JFET is also a unipolar device, the formulas for MOSFET can also be used for JFET, in this special case, the VJFET does not have the body diode and the diode relate part should be removed. Due to the strong dependency of junction temperature, the losses functions can be very complex. By taking advantages of the datasheets, the conduction and switching losses of the devices can be inserted in look-up tables and using software to calculate the losses. The implementation is done in PLECS for the same gate driver resistance and supply as used in the converter. In between and outside of the prescribed values, the software will linear interpolate/extrapolate the losses.

The estimated efficiency for the modelled converters using the same heat sink; 3.2 K/W and operate at 30°C ambient temperature is shown in Figure 6 for boost mode. Since the ESR loss of the capacitor is neglect able, the efficiency plot is generated based on the sum of semiconductors and inductors losses. It can be seen, that 98% efficiency can be obtained with both converters.

3.1 Heat sink design

To keep the semiconductor within the maximum allowed temperature, the generated heat must be removed. An electrical analogy of the thermal process is shown below [14].

In Figure.5, P_d is the heat source, T_j is the maximum allowable junction temperature (specified by the device manufacturer), R_{jc} is the thermal resistance junction to case (specified by the device manufacturer), T_c is the case temperature, R_{cs} is the thermal resistance case to sink (insulate pad and/or thermal compound), T_s is the sink temperature, R_{sa} is the thermal resistance sink to ambient (the heat sink) and T_a is the ambient temperature.

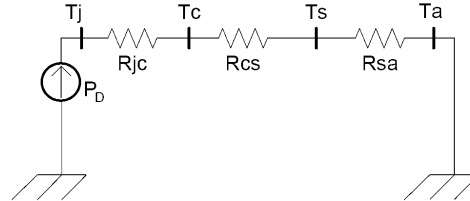


Figure 5: Electrical analogy of the thermal process.

Rearrange the circuit above the thermal resistances of the heat sink can be expressed as:

$$R_{sa} = \frac{T_j - T_a}{P_d} - R_{jc} - R_{cs} \quad [K/W] \quad (4)$$

Eq. 4 indicates the maximum allowable thermal resistance of the heat sink.

For the sake of fair comparison, the same switching frequency is used, the same inductor is used, the same capacitors are used and thus the same heat sink of 3.2 k/W; designed for 40°C ambient, will also be used for both converters.

3.2 Practical design considerations for SiC MOSFET

To utilize the extremely fast switching capability of SiC switches, the designer should be extra careful to the parasitic components around the switch as well as the parallel capacitance in the inductor for this topology. Together with the parasitic inductance of the package plus the PCB track, these parasitic inductances and the parallel capacitance of the inductor will oscillate at turn on and turn off. The ringing can be reduced, by limit to a single layer winding configuration [15]

To minimize the ringing cause by the gate drive loop, Kelvin connection for the gate drive is recommend, if the package has this pin, otherwise the gate driver should be located as close as possible to the MOSFET [15]. Furthermore, due to the physical size of some components there will be a long track and thus a high parasitic inductance, for example between the input/output capacitors and

the switches; high voltage ceramic capacitors can be distributed along this path to buffer/reduce the effective stray inductance. To reduce the parasitic Gate-Drain, Gate-Source and Drain-Source capacitances, the respective Gate-Drain, Gate-Source and Drain-Source tracks should not route in parallel. The interconnection of the boost MOSFET and the buck MOSFET should also be tried to keep as short as possible. To compromise with the parasitic capacitances and the single heat sink design, the pins are benched 90 degrees as shown in Figure 8 (left).

3.2 Practical design considerations for VJFET

Common sense design rules should also be applied for VJFET design. Unlike the SiC MOSFET, the VJFET use the Capacitive clamped driver. To reduce the parasitic inductances between the low voltage MOSFET and the normally-on JFET, package with integrated low voltage MOSFET is preferred. For discrete devices solution as used, the low voltage MOSFET, TVSs(D8, D9, D12) and the clamped capacitor from Figure 5, should be placed as close as possible to the JFET. The clamped capacitor should be tuned for optimal performances and 1uF has been used in the prototype.

4. Experimental results

The prototypes can be seen on Figure 6, the SiC MOSFET is on the left and the VJFET is on the right. The weight of both is close to 1.5kg, where the inductor itself is 1kg and the heat sink is 230g. The size of the MOSFETs prototype is 100 x 160 x 110 mm and the VJFETs prototype is 115 x 285 x 80mm.

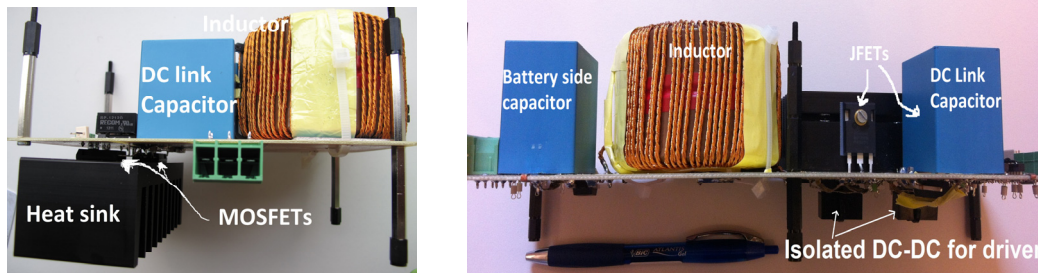


Figure 6: The prototypes; SiC MOSFETs converter on the left and SiC VJFET on the right.

4.1 Results of VJFET

To emphasis the important of third quadrant operation, not only to obtain higher efficiency, but also ease the thermal design. The hot spot in Figure 7 is caused by the current, conduct through the body diode of the low voltage MOSFET. Due to a high thermal resistance of the package, the device reached more than 100 °C at 800mA reversed conduction and it prevents the power to increase further.

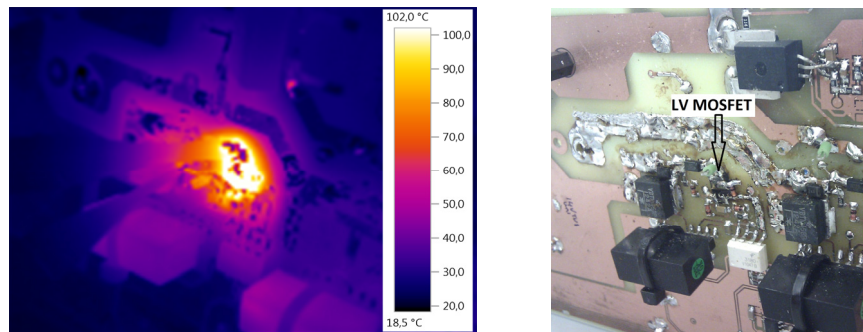


Figure 7: Low voltage MOSFET without third quadrant operation, left with thermal camera and right with photo camera.

Switch on the MOSFET, thus sharing the current between the MOSFET on-resistance and the body diode, makes the effective on conduction even lower than first quadrant operation and thus reduce power losses. This can be seen in Figure 8, where the converter operates at nominal load under boost mode. The temperature different is clear; the current is more than 11 times higher and the temperature is roughly 50% lower.

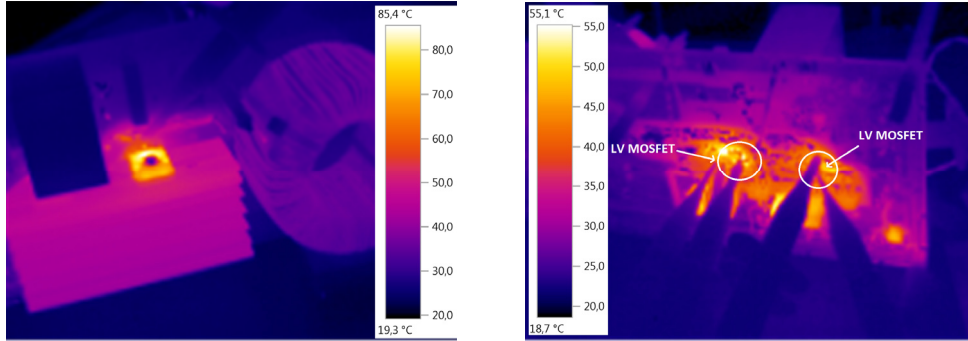


Figure 8: Thermal pictures of the VJFET converter under boost mode at rated power.

The efficiency measuring was carried out in a cabinet at 30°C with a Newtons 4th PPA5530 precision power analyzer with accuracy <0.15% up to 400 Hz. The efficiencies of the converter are plot in Figure 9. Compare to the simulation results, this is 1% lower at 0.6 kW and 0.5% lower at nominal load, equivalent to 6W and 15 W, respectively.

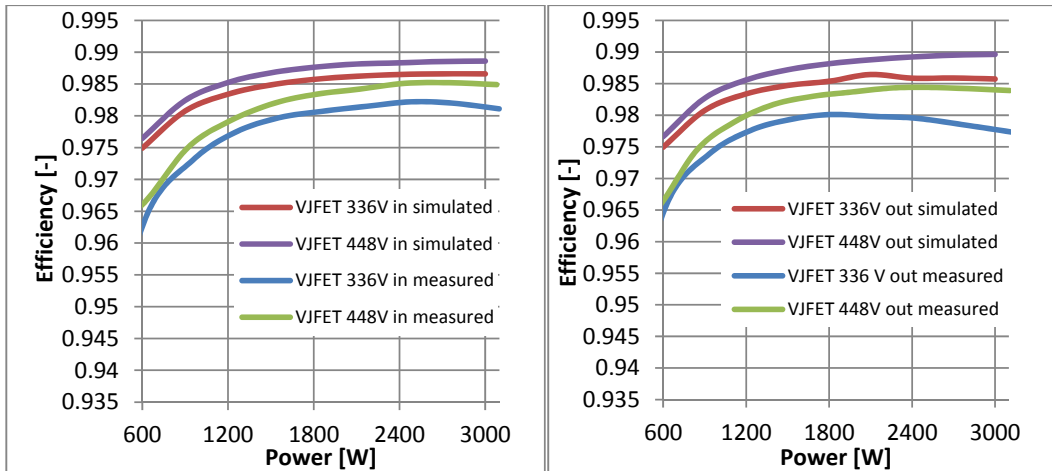


Figure 9: The recorded efficiency of the prototype.

The target efficiency of 98% is obtainable, except when the converter bucks from 700 V to 336 V, where the efficiency is 97.7%. The lower efficiency could partly be explained by other type of losses in the converter which has not been taken into account, like ESR loss in the capacitors and skin effect in the winding. More details need to be included to improve the accuracy and thus match the simulation results.

With the Capacitive Clamped driver scheme, the switching speed of the JFETs can be controlled and thus avoid overvoltage stressing the low MOSFETs. The scope waveform in Figure 12 show, that the 40V LV MOSFET are far away from its breakdown, where Channel 1(yellow) is voltage at the boost VJFET Drian (refer to GND), Channel 2(green) is across the boost LV Drain-

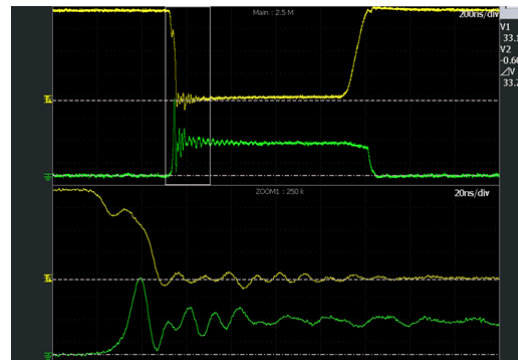


Figure 12. The scope waveform in boost mode (448V) at 3.1 kW.

Source MOSFET. Furthermore fast switching can be obtained with SiC as shown here for the VJFET, where the switching transition (0-100%) is over after approximate 40ns.

To improve the efficiency, one can replace the inductor core with a higher permeability. With a higher permeability powder core, the inductance is higher, even though this might only be at light load and in the heavy load the effective permeability is the same, but this higher inductance will give lower current ripple, which then gives lower core loss and improve weighted efficiency.

4.2 Results of MOSFET

A similar fast switching speed can also be obtain with SiC MOSFETs, which is shown in Figure 14 during boost mode where Channel1 (yellow) is across the Drain-Source of the boost switch, Channel 3(green) is the gate signal of the boost, Channel 3(magenta) is across the Drain-Source of the buck switch and Channel 4 (cyan) is the gate signal of the buck switch. One can see 7V peak spike in the gate signal of the buck (cyan), when the boost switch turning on. Compare to the first generation MOSFET, where the gate can only negative bias to -5V, the second generation can be biased to -10, which improve the noise immunity. In this case the switch is negative biased with -5V during turn-off and this keep the switch off, even if the is a small oscillation due to parasitic components.

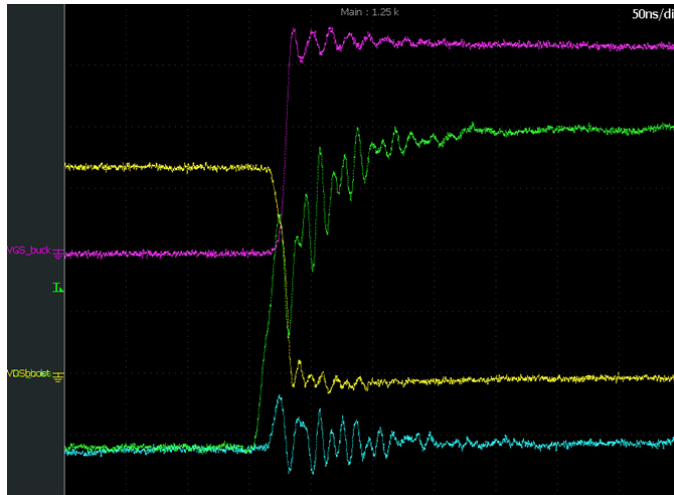


Figure 13: Switching waveform of the SiC MOSFET in boost mode.

Figure 14 show the simulation results of the SiC MOSFETs converter at 30°C ambient. Compare to the simulation results of the VJFET, the SiC MOSFET has marginal better efficiency.

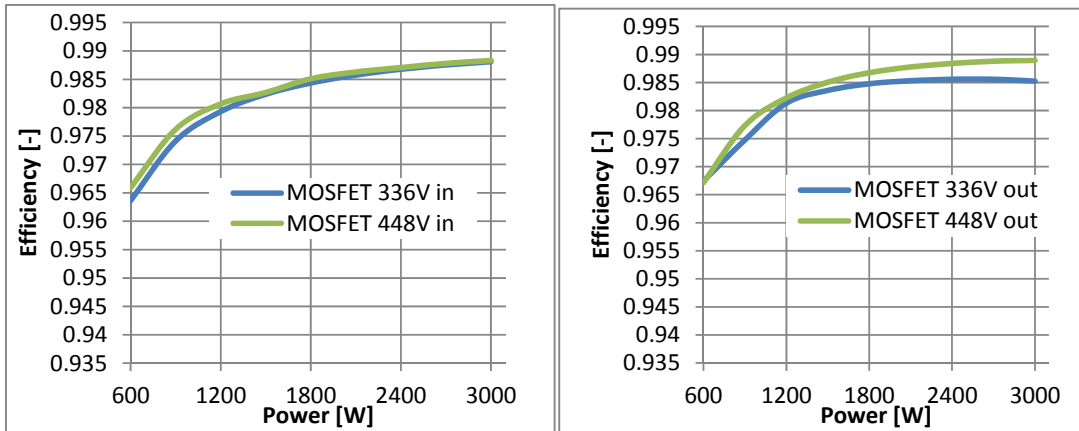


Figure 14: Simulated efficiency of the SiC MOSFETs converter.

5. Conclusion

There is a demand for power electronics with higher efficiency and/or higher power density. WBG semiconductors like SiC have higher breakdown voltage and superior statics as well as dynamic characteristics can meet these challenges. In this paper a simple topology for bidirectional DC-DC converter for smart PV battery storage built with SiC components has been analysed. The second generation SiC MOSFET and the VJFET are two devices which are very close in performances. Using unipolar SiC switches this can reduce the number of components and by active turn-on the MOSFET during reversed current conduction can reduce power losses. By switch with high switching frequency, the electrolytic capacitors can be replaced with bipolar film capacitors and reduce the size of magnetic components. The efficiency of the 3 kW converter with normally-on JFETs has been measured, up to 98,5% efficiency has been recorded, from which 1% is caused by the losses in the inductor. Fast switching and high efficiency can be obtained with relatively little effort, as it has been demonstrated. From the driving circuitry, the SiC MOSFETs are not much different from the well known MOSFET. SiC normally-on VJFET are on the other hand a new device in power electronics, which in this converter has also shown high performances

References

- [1] B. Ozpineci, L.M. Tolbert, "COMPARISON OF WIDE-BANDGAP SEMICONDUCTORS FOR POWER ELECTRONICS APPLICATIONS", 2003, ORNL/TM-2003/257, Oak Ridge National Laboratory
- [2] http://www.pv-magazine.com/news/details/beitrag/germanys-pv-storage-incentive-program-will-come-into-force-on-may-1_100010946/#axzz2RwUhddxz
- [3] B. Rubino, M. Macaudo, M. Nania, S. Buonomo, Direct comparison among different technologies in Silicon Carbide, PCIM 2012
- [4] Mietek Bakowski, "Prospects and Development of Vertical Normally-off JFETs in SiC"
- [5] /SGDR600P1 datasheet, Semisouth
- [6] Application Note AN-SS7, SSJH12R085-1 Half-Bridge Demo Board User's Guide, SemiSouth
- [7] Siemieniec, R.; Kirchner, U.; , "The 1200V direct-driven SiC JFET power switch," *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on* , vol., no., pp.1-10, Aug. 30 2011-Sept. 1 2011
- [8] Wolfgang Bergner, Fanny Bjoerk, Daniel Domes, Gerald Deboy, "Infineon's 1200V SiC JFET – The New Way of Efficient and Reliable High Voltages Switching", Infineon
- [9] Abraham I. Pressman, Keith Billings, Taylor Morey, "Switching Power Supply Design, 3rd Ed", ISBN: 978-0-07-159432-5
- [10] 200C Series datasheet, Micrometals Inc.
- [11] Salcone, M.; Bond, J.; , "Selecting film bus link capacitors for high performance inverter applications," *Electric Machines and Drives Conference, 2009. IEMDC '09. IEEE International* , vol., no., pp.1692-1699, 3-6 May 2009
doi: 10.1109/IEMDC.2009.5075431
- [12] CMF0080120D datasheet, Cree Inc.
- [13] SJDP120R085 datasheet, SemiSouth.
- [14] Dusan Graovac, Marco Pürschel, Andreas Kiep, " MOSET Power Losses Calculation Using the Datasheet Parameters", Infineon.
- [15] B. Callanan, Application considerations for Silicon Carbide MOSFETs, Cree Inc
- [16] Adel S. Sedra and Kenneth C. Smith. *Microelectronic Circuits*. Oxford University Press, fourth edition, ISBN: 0195116909
- [17] J. Liu, K. Lap and P. Kierstad, Increase Efficiency and Lower System Cost with 100KHz, 10kW Silicon Carbide (SiC) Interleaved Boost Circuit Design, PCIM 2013.