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SiC-based High Efficiency Bidirectional Battery Converter for Smart PV Residential Systems

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Abstract

Smart PV inverters are essential components of future grids. Beside conventional functionalities they can communicate with the grid, supports the grid with reactive power and with active power from internal battery storage. To maximize internal consumption, a high efficiency bidirectional DC-DC converter for the battery storage is necessary, as energy will be processed twice. Realisation of the battery converter with silicon carbide (SiC) semiconductors offers many advantages compared to Silicon (Si), included higher power density and higher efficiency. In this paper the design of a simple high efficiency 3kW hard switching bidirectional converter based on normally-on SiC JFET is presented, 98.5% maximum efficiency has been obtained with the prototype and a comparison with SiC MOSFet 1st generation is performed.

1. Introduction

Photovoltaics (PV) is one of those applications that are demanding for power electronics with higher efficiency and power density. This is a challenge for Si-based semiconductors and to overcome these limitations wide-band-gap (WBG) materials like SiC can be used. The physical characteristics of Si and 4H-SiC are listed in Table 1. With higher energy bandgap, the devices are able to operate at higher temperature, higher breakdown field allows higher doping density and gives smaller drift region resistances (for ´the same voltage level), higher drift velocity allows faster switching devices and allow charge in the depletion region of diode to be removed faster and thus reduce the reverse recovery current and shorter the reverse recovery time. At last with higher thermal conductivity the generated heat can be removed more effective [1]. All these can simplify the converter design, boost the efficiency, reduce the cooling requirement and with higher switching frequency the bulky electrolyte capacitor can be replaced with the more reliable bipolar film capacitors and extend the service lifetime of the products [2]. Aiming for the highest efficiency is the PV industry, where the generated energy price is relatively high and to balance the mismatch between generation and demand and to support the grid, like Smart PV systems, a battery storage is needed. To

Tab. 1. Physical characteristics of Si and 4H-SiC [1].

Property	**Si**	**4H-SiC**
Bandgap (eV)	1.12	3.26
Dielectric constant	11.9	10.1
Electric breakdown field (kV/cm)	300	2.200
Saturated electron drift velocity (10^7 cm/s)	1	2
Thermal conductivity (W/cm·K)	1.5	4.9

utilize the system and reduce the payback time, a high efficiency bidirectional converter for battery is essential, due to the energy is processed twice; charging and discharging.

1.1. Topology and specifications

The battery converter will be realised with a simple bidirectional boost buck converter as shown in Figure 1 and the specifications are listed in Table 1. From left to right, the battery voltage boosts to DC bus and from right to left it bucks the DC bus to charge the battery. To generate up to 700V DC which is the typical DC bus of a three-phase grid connected PV inverter, 1200V semiconductors are often used in order to ensure safe operation. At this voltage, Si-based semiconductors like MOSFETs/IGBTs are not able to show good performances compared with the 600V devices. The 700V DC bus can be obtained by split technology (±350V) and thus the use of 600V devices is possible [3] but the high number of components lead to limited reliability and low power density.

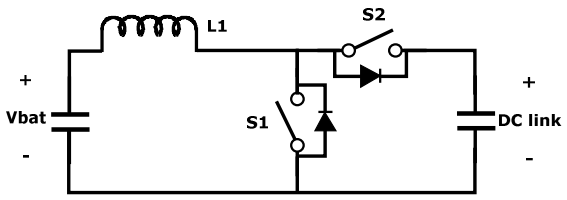

Fig. 1. The bidirectional DC-DC converter.

Tab. 1: Design specifications of the bidirectional DC-DC converter.

Power	Vin	Vout	Switching topology scheme	Target η
3kW	Boost: 336-448V Buck: 700V	700V 336-448V	Hard switching with active freewheeling/rectification	> 0.98

Building the battery converter with SiC semiconductors can simplify the converter design, boosts the efficiency and power density, as it will be demonstrated by a 3 kW converter module with >98% max. efficiency. Power capacity can be increased by interleaving of modules, without reducing the efficiency.

2. SiC power switches

Power switches based on SiC such as BJTs, MOSFETs and JFETs (both normally-on and normally-off) are now available. Normally-on switches are not easily accepted in power electronic applications due to system safety requirements, for example during power up or loss of gate driver supply. The designing of the normally-off JFETs implies sacrificing some on-state resistance [4] of the device and to drive normally-off JFETs with the highest static and dynamic performances, a dedicate two-stages gate driver is needed. The first stage is optimized for switching and the second stage feeds the gate a constant current to keep the device on within a specified on-state resistance [5]. For BJTs, the current controlled characteristic has a negative impact on the efficiency of the converter, especially at few kW power ranges. The drawback of normally-on JFET can easily be overcome with cascode configuration, where a low voltage normally-off MOSFET is series connected to the source of the JFET as shown in Figure 2. The inherently off behavior is obtained as the JFET is normally-on and the low voltage MOSFET is normally-off, this lifts the potential of the JFET source to the same as at the drain. Since the gate of the JFET is tied to the GND, thus gate-source potential difference becomes now negative and the JFET switches to off-state and the off-behavior is obtained. Another advantage of the cascode is the freewheeling/rectification functionality without additional anti-parallel diode, this is possible due to the reverse current flow through body-diode of the low voltage MOSFET. The voltage at the source of JFET will be negative biased and is equal to the voltage drop across the body-diode, positive gate-source biased of the JFET will turn the JFET on.

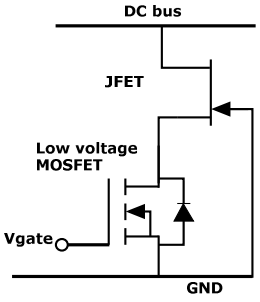

Fig. 2. Conventional cascode.

The advantages of using MOSFET in this configuration is that of-the-shelf gate driver can be used indirectly to drive the JFET. Some other variation of this configuration are, the Capacitive Clamped Cascode, which gives the controllability over the JFET [6] and Direct Driver approach, where the MOSFET only switches off during startup and fault situations. During normal operation of Direct Driver, the JFET is driven direct by the gate circuitry and thus eliminating the additional switching losses of the MOSFET and the possibility of repetitive avalanche during switching off. Furthermore the gate driver is integrated in an IC, which helps to reduce parasitic components in the gate circuitry [7-8].
SiC MOSFETs are also well suited and off-the-shelf driver can be used to drive directly. From the gate driver point of view, the main difference compared to Si is a wider gate voltage swing, where driving with 20V is recommended to have optimal on-state performance [9].

2.1. SiC MOSFET vs. Capacitive clamped cascode with normally-on JFETs

Two solutions will be used for comparison, those are CMF2012D SiC MOSFET against SJDP120R085 normally-on Vertical Trench JFET (VJFET) with BSC059N04LSG Si MOSFET. Some key parameters are shown in Table 2 and the driver circuitry for MOSFET and for VJFET are shown in Figure 3 and Figure 4, respectively.

Tab. 2. Key parameters of CMF2012D and SJDP120R085 + BSC059N04LSG [9-11].

Parameter	CMF2012D	SJDP120R085 + BSC059N04LSG
$V_{DS,}$ min.	1200V	1200V
I_{DS}@25°C, max.	42A	27A
I_{DS}@100°C, max.	24A	17A
I_{DS} degradation	42.9 %	37.1%
$R_{DS(on)}$ @25°C, typ.	80mΩ@20A I_{DS}	75mΩ + 4.8mΩ@17A I_{DS}
$R_{DS(on)}$ @100°C, typ.	-	110mΩ + 6.2mΩ@17A I_{DS}
$R_{DS(on)}$ @135°C, typ.	95mΩ@20A I_{DS}	-
$R_{DS(on)}$ @150°C, typ.	-	147mΩ + 7.5mΩ@17A I_{DS}
Operation temperature	-55°C - 135°C	-55°C - 150°C
R_{thJC}, max.	0.7K/W	1.1K/W
Q_g, typ.	90.8nC	32nC
E_{tot}@25°C, typ.	859uJ@800V,@20A I_{DS}	290uJ@600V,@17A I_{DS}
Diode Voltage drop@25°C, typ.	3.5V@10A I_F	0.88V@50 A I_F

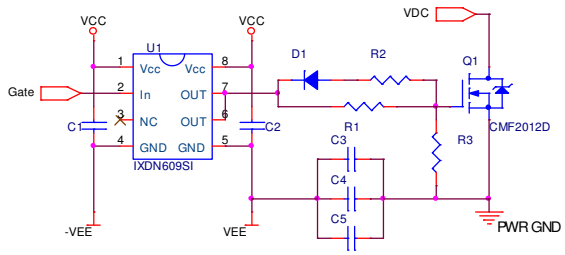

Fig. 3. SiC MOSFET driver circuitry.

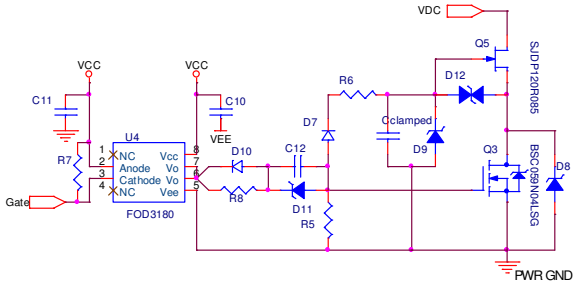

Fig. 4. Capacitive clamped cascode driver.

Both driver circuits are simple and easy to design as it is for the case of Si based.
In Capacitive clamped cascode, to prevent voltage spikes that can lead the low voltage MOSFET into avalanche, the switching speed of JFET can be controlled by adjust the clamped capacitor. From Table 2, the conduction losses of the devices are roughly the same, but the switching losses of the JFET is lower than the SiC MOSFET. Thus in high switching frequency applications, this JFET will give lower losses and the capacitive clamped cascode with VJFET will be implemented to demonstrate the high efficiency.

3. Converter design

When the low voltage MOSFETs are switched on during freewheeling/rectification and using low ESR capacitors in the converter as shown in Figure 5, the dominant sources of losses

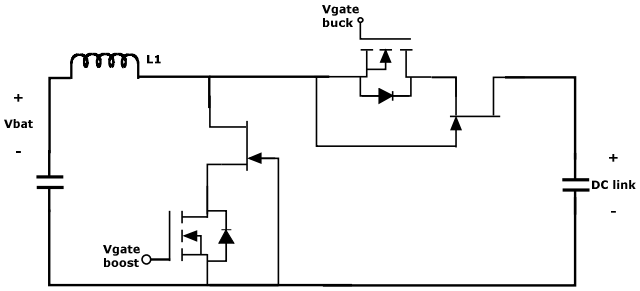

Figure 5: Bidirectional DC-DC converter with Normally-on JFETs.

are: core and copper losses in the inductors and switching and conduction losses of the semiconductors. Thus optimize the magnetic is also essential for high efficiency. As shown in Table 1, the converter will process 3kW. The inductor is used in both modes; buck and boost and is designed for boost mode, where it is used to store energy, which is defined as [12]:

$$W_L = ½ \cdot L \cdot I^2 \tag{1}$$

Where *L* is the inductance and *I* is the rms current.
Multiplying Eq.(1) with the switching frequency, f_{sw}, the stored power is calculated. By solving Eq. 2 for the battery window voltage, the first design constraint is defined:

$$L \cdot f_{sw} = \frac{2 \cdot V_{in}{}^2}{P_{out}} \Rightarrow 76 \wedge 139 \tag{2}$$

From the left hand side, both inductance and switching frequency can be adjusted to fulfill the right hand side of Eq. 2. By increasing the inductance with the same core, more turns are added and the copper loss will increase, but this allows the switching frequency to be reduced, which lower the switching losses of the semiconductors and core losses and vice versa. Furthermore the converter could operate in continuous conduction mode (CCM) with small current ripple; $I_{ac} << I_{DC}$. Due to this, the skin effect is reduced, copper loss can also be reduced by using thicker copper wire and core losses is reduced follow by less utilization of the B-H hysteresis. The ripple current can be calculated as:

$$\Delta I_{L,boost} = \frac{D_{boost} \cdot V_{in}}{L \cdot f_{sw}} \tag{3}$$

Both the inductance and switching frequency appear in Eq. 2 and Eq.3, thus an optimisation process is necessary. In practical design, starting with high permeability and high saturated flux density core is a reasonable approach. Switching frequency of 80 kHz is selected and applying this to Eq. 2 gives an inductance of 950µH. Based on this, a 3" toroidal power core of type 200C with -63D material is selected [13]. An extra turn is added as a safety margin and the design data of the 969µH@10A inductance is listed in Table 3.

Tab. 3. Design data for the boost inductances.

Inductance	Stacking	turns	Winding	DCR	Core loss	Copper loss
969µH	2	85	30 x 0.2mm litz	218mΩ	12.3W	21.8W@40°C

Notice that the inductor is responsible for roughly 1% of losses at rated power, thus a better core or more winding can be added to improve the efficiency.

At 80 kHz switching frequency, bipolar film capacitors are more preferred than electrolytic capacitors due higher reliability and higher power density [2]. The main selection criteria here are the rated voltage and ripple current capability. In worst case the ripple current can be as much as the peak current for the inductor during the boost mode, which is:

$$\hat{I}_{L,boost} = I_{L,boost} + \frac{\Delta I_{L,boost}}{2} = \frac{P_{out}}{V_{in}} + \frac{D_{boost} \cdot V_{in}}{L \cdot f_{sw} \cdot 2} = \frac{3000}{336} + \frac{(1 - \frac{336}{700}) \cdot 336}{950 \cdot 10^{-6} \cdot 80 \cdot 10^{3} \cdot 2} = 10.1\,\mathrm{A} \qquad (4)$$

Based on this, a 20µF/1100V MKP film capacitor selected, which can handle 12 A and with ESR of 3.5 mΩ [14], the ESR losses can be neglected.
To estimate the efficiency of the converter, power losses of the semiconductors must be calculated. Losses estimation formulas for MOSFET can also apply for JFET. Due to the strong dependency of junction temperature, the losses functions can be complex. Take advantages of the datasheets, the conduction and switching losses of the devices can be inserted in look-up tables and using software to calculate the power losses. The implementation is done in PLECS and simulated in the case where the JFETs are mounted on a single heat sink of 3.2ºK/W and operate at 25ºC ambient temperature. The efficiency based on the inductor and semiconductors losses is plotted in Figure 6.

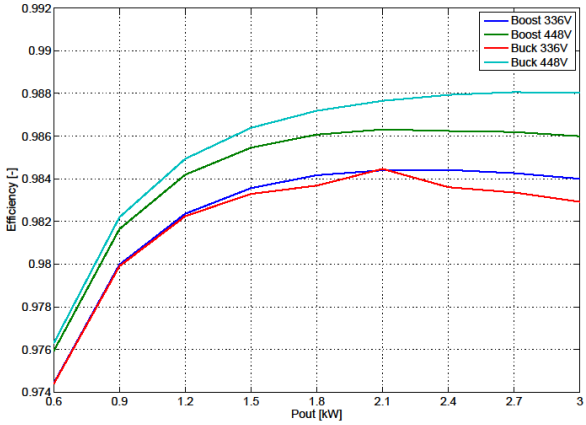

Fig. 6. The estimated efficiency of the bidirectional DC-DC converter.

The target efficiency of 98% at rated power is obtainable in boost mode as well in buck mode and a prototype will be built to verify the high efficiency.

4. Experiment results

The prototype is shown in Figure 7, without optimization the physical size is 11.5 x 28.5 x 8 cm and weigh 1.5 kg, out of this the inductor weigh 1 kg and the heat sink is 230 g.

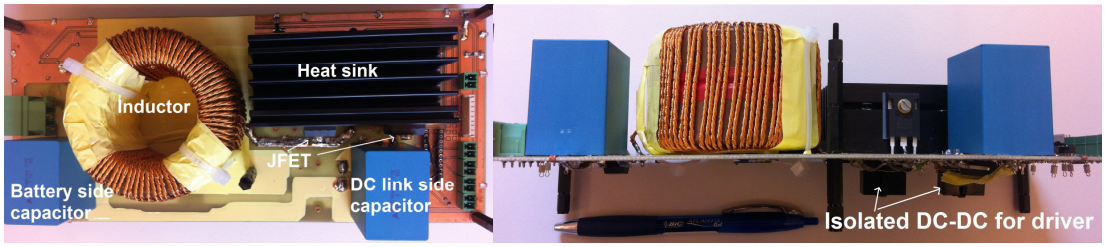

Fig. 7. The prototype of the battery converter.

The efficiency measuring was carried out in a cabinet at 30°C with the Newtons 4th PPA5530 precision power analyzer with accuracy <0.15% up to 400 Hz, as shown in Figure 8. Thermal

pictures of the converter in boost mode at 3 kW are shown in Figure 9 and Figure 10, where both pictures indicate a stable temperature of the JFET as well as the low voltage MOSFETs.

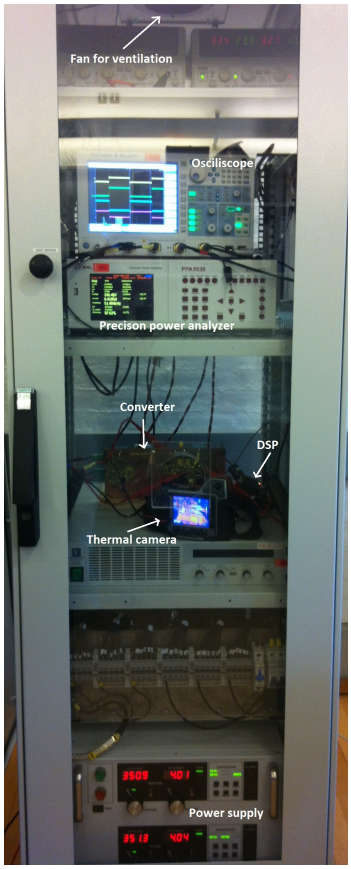

Fig. 8. The test setup.

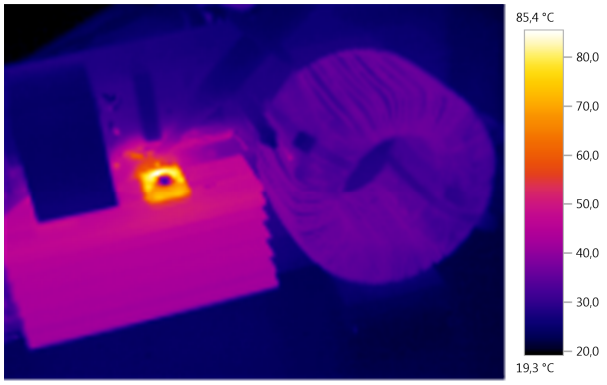

Fig. 9. Thermal picture of top side of the converter.

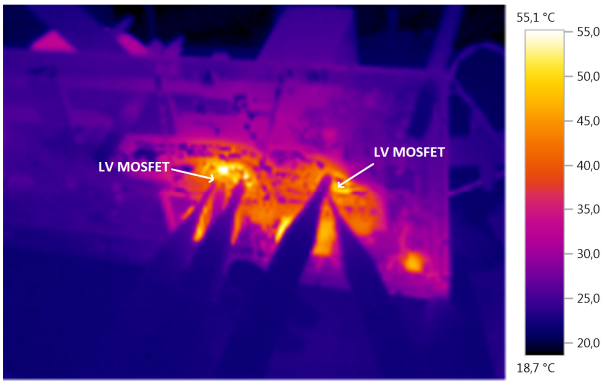

Fig. 10. Thermal picture of the bottom side.

The measured efficiency is plotted in Figure 11 and compare to the simulation this is a deviation of roughly 1% at 0.6kW and 0.5% at rated power, which is equivalent to 6W and 15W, respectively.

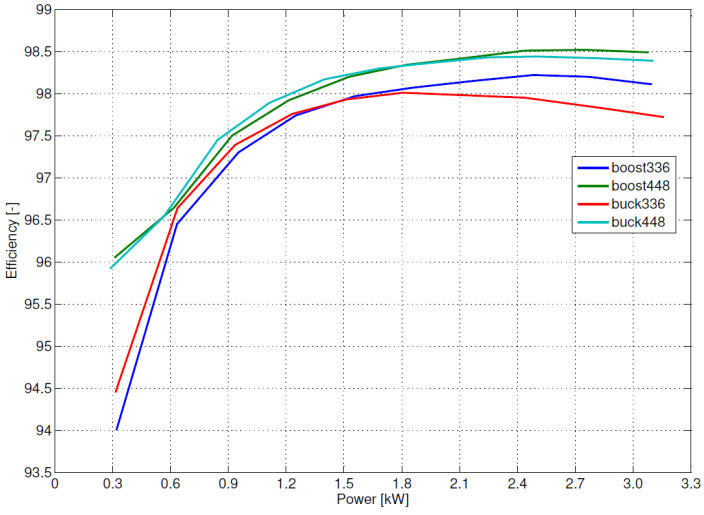

Fig. 11. The recorded efficiency of the prototype.

With the Capacitive Clamped driver scheme, the switching speed of the JFETs can be controlled and thus avoid stressing the low voltage MOSFETs. The scope waveform verify that the 40V (low voltage) MOSFET are far away from its breakdown voltage as shown in Figure 12, where channel 1(yellow) is across $LV_{Drain\text{-}Source}$ boost MOSFET, channel 2(green) is across LV_{Source} to boost $JFET_{Drain}$, channel 3(cyan) is across $LV_{Drain\text{-}Source}$ buck MOSFET and channel 4(magenta) is across LV_{Source} to buck $JFET_{Drain}$. Furthermore fast switching can be

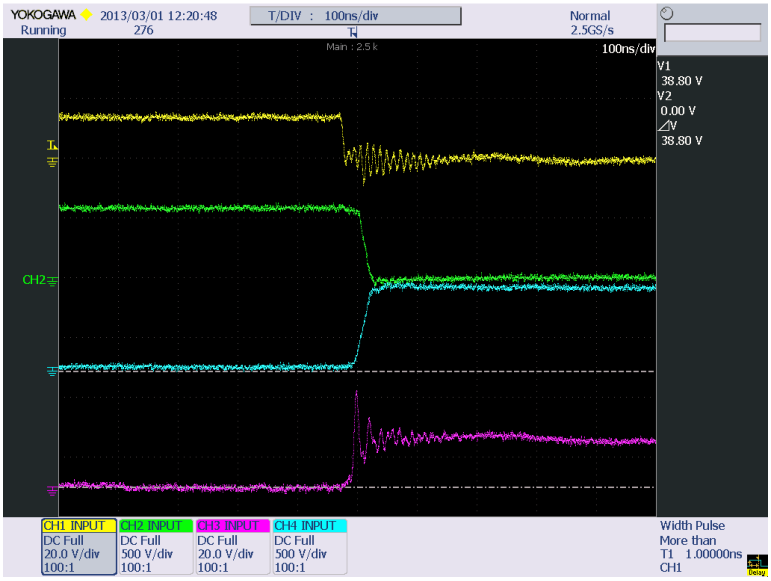

Fig. 12. The scope waveform in boost mode (448V) at 3.1 kW.

obtained with SiC as shown here for this JFET, where the switching transition (0-100%) is over after approximate 40ns.

5. Conclusion

There is a demand for power electronics with higher efficiency and/or higher power density, smart PV inverters is one of them. WBG semiconductors like SiC have higher breakdown voltage and superior statics as well as dynamic characteristics can meet these challenges. In this paper a simple bidirectional DC-DC converter using SiC normally-on JFET has been demonstrated that fast switching and high efficiency can be obtained with relatively little effort, as up to 98.5% efficiency has been recorded for a 3kW module, which can be interleaved control to get higher power output.

6. Acknowledgment

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