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A Simple Autonomous Current-Sharing Control Strategy for Fast Dynamic Response of Parallel Inverters in Islanded Microgrids

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Abstract—This paper proposed a novel control strategy based on a virtual resistance and a phase locked loop for parallel three-phase inverters. The proposed controller can overcome the drawbacks of the conventional droop control such as slow transient response, complex design, and limited stability margins. The load sharing capability can be also obtained under asymmetrical output impedances in which the conventional droop controller was not properly working. The proposed approach has been verified by means of simulations and experimental results in a laboratory-scale prototype.

Keywords: Parallel inverters, droop control, phase-locked loop, virtual resistance.

I. INTRODUCTION

Droop control method emulates the behavior of a synchronous generators by measuring active and adjusting frequency accordingly. In a similar way, reactive power can also be controlled by adjusting voltage amplitude [1]. These droop schemes are often named P - f and Q - V droops [2]. They have been usually preferred for the autonomous control of parallel inverters in the last decade in islanded applications such as distributed uninterruptible power systems or microgrids [2], [3].

The conventional droop control presents active and reactive power coupling and poor transient response [4]. In order to improve the active and reactive power decoupling performance, improved droop controllers are reported in [5] and [6]. Also, an enhanced droop controller featuring transient droop performance is proposed in [7]. The improved controllers are proposed based on the static droop characteristics combined with a derivative terms which can yield to a two degrees of freedom (2-DOF) tunable control in [8-10].

It is also well known that the performance of the conventional droop control is seriously affected by the inductance-to-resistance (X/R) ratio of output and the line impedance. Microgrids, similarly as electrical distribution networks, present a low X/R ratio, so that voltage amplitude is generally used to control active power, while the angle dominates reactive power so that can be controlled by the

system frequency. This scheme is also named P - V and Q - f droop. In order to control active and reactive power according to the power line X/R ratio, resistive virtual impedance loops has been added to the droop control. In this sense, we can have a control framework that includes three control loops [11], [12]: (i) virtual resistance; (ii) P - V droop; and (iii) Q - f droop. However it is complex to design the virtual resistance and the P - V droop coefficients since both affect voltage amplitude regulation with control loops that present different control bandwidths.

Further, an orthogonal linear rotational transformation matrix T can be employed to transform active and reactive power and to a new transformed active and reactive powers when both X and R need to be considered [13]. However this method requires precise line impedance value estimation, which is difficult to known. In order to reduce the influence of the R/X ratio on droop controller and improve the active and reactive power decoupling performance, a fast control loop named virtual impedance is added into the droop controller [14], [15].

However, all abovementioned improved approaches present the inherent drawback of needing to calculate instantaneous active and reactive powers, thus needing for low-pass filters to average values which bandwidth will impact the system transient response [16]. Even in the case of three-phase systems that the active and reactive power can be calculated by using the instantaneous power theory, a post-filter processing is necessary in order to eliminate the distorted power components [17]. Furthermore, in practical situations the load sharing performance of the conventional droop control is degraded when using short lines with small impedance, especially in low voltage networks. In this case, a very small deviation in voltage frequency and amplitude will result in large power oscillation and even instabilities [16].

With the aim to overcome the aforementioned problems, a control strategy by using a different view point is proposed in this paper. The approach is based on using a virtual resistance loop and to substitute the whole droop control by a phase locked loop (PLL). This way, the PLL adjust the phase of the inverter, and the system is controlled by a virtual resistance controlling current as in a dc electrical system, in a sharp

contrast as in ac systems, in which active and reactive power sharing is required. In comparison with the traditional virtual resistance plus P - V and Q - f droop control framework, the proposed controller endows a faster dynamic response to the paralleled system, allowing higher stability margins and easy to implement and to design. The proposed approach has been verified by using simulation and experimental results in laboratory prototypes.

II. A REVIEW OF THE POWER FLOW ANALYSIS IN DROOP CONTROLLED MICROGRIDS

Fig. 1 shows the equivalent circuit of two inverters connected in parallel sharing a common load, which can be considered as a subset of the distributed power network operating in autonomous islanded mode. The system model consist of two voltage sources connected through a series equivalent impedance ($Z_1 \angle \varphi_1$ and $Z_2 \angle \varphi_2$), which encompasses the inverter output impedance ($Z_{o1} \angle \varphi_{oZ1}$ and $Z_{o2} \angle \varphi_{oZ2}$) and the line impedance ($Z_{line1} \angle \varphi_{line1}$ and $Z_{line2} \angle \varphi_{line2}$). The output voltage of each inverter is denoted by $V_{o1} \angle \varphi_{o1}$ and $V_{o2} \angle \varphi_{o2}$ and the voltage for point of common coupling by $V_{bus} \angle \varphi_{bus}$.

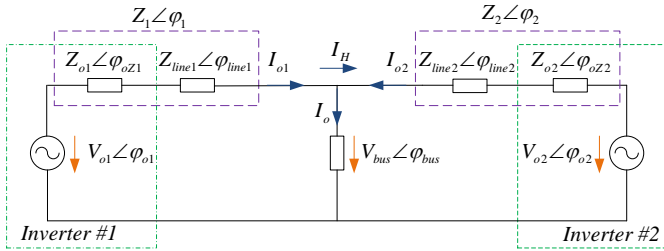


Fig. 1. Equivalent circuit of two inverters operating in autonomous mode.

In traditional power systems, the equivalent impedances between the paralleled inverters present high X/R ratio, that means $\varphi_{line} \cong 90^\circ$. Thus the output active and reactive powers (P_n and Q_n) of inverter n ($n=1, 2$) can be presented as follows

$$P_n = \frac{V_{on} V_{bus} \sin(\varphi_{on} - \varphi_{bus})}{Z_n} \quad (1)$$

$$Q_n = \frac{V_{on}^2 - V_n V_{bus} \cos(\varphi_{on} - \varphi_{bus})}{Z_n} \quad (2)$$

From equations (1) and (2), a set of partial differential equations can be derived as follows:

$$\frac{\partial P_n}{\partial \varphi_n} = \frac{V_{on} V_{bus} \cos(\varphi_{on} - \varphi_{bus})}{Z_n} \quad (3)$$

$$\frac{\partial P_n}{\partial U_n} = \frac{V_{bus} \sin(\varphi_{on} - \varphi_{bus})}{Z_n} \quad (4)$$

$$\frac{\partial Q_n}{\partial \varphi_n} = \frac{V_{on} V_{bus} \sin(\varphi_{on} - \varphi_{bus})}{Z_n} \quad (5)$$

$$\frac{\partial Q_n}{\partial U_n} = \frac{2V_{on} - V_{bus} \cos(\varphi_{on} - \varphi_{bus})}{Z_n} \quad (6)$$

By considering $\varphi_{on} - \varphi_{bus} \approx 0$ and Z_n large enough, we can easily adjust active power P_n with the output voltage angle φ_{on} and reactive power Q_n with the output voltage amplitude V_{on} . Based on this power flow analysis, the droop control law can be expressed as:

$$\omega_n = \omega_n^* + k_{p\omega} (P_n^* - P_n) \quad (7)$$

$$V_n = V_n^* + k_{qV} (Q_n^* - Q_n) \quad (8)$$

where, ω_n^* and V_n^* are the normal output frequency and voltage amplitude, respectively.

However, in a practical situation the load sharing performance of the conventional droop control is degraded when using short lines with small impedances, especially in low voltage networks. The reason of this is that since $[\sin(\varphi_{on} - \varphi_{bus})]/Z_n \approx (\varphi_{on} - \varphi_{bus})/Z_n$ will not be neglect when $\varphi_n - \varphi_{com} \neq 0$ or Z_n is too small. In this case, each equation from (3) to (6) cannot be well approximated to zero, so that the output power (P_n and Q_n), output voltage amplitude (V_n) and frequency (ω_n) are coupled, which will result in imprecise power control. Furthermore, conventional droop controlled systems may present instabilities since small voltage frequency or amplitude deviations may result in large power oscillations when Z_n is very small.

III. CURRENT FLOW ANALYSIS – THE CHANGE OF PARADIGM

Fig. 1 can be further simplified to an equivalent circuit of a two-paralleled inverter system including output voltages (V_{o1} and V_{o2}), output impedances (Z_{o1} and Z_{o2}), virtual resistances (R_{vir1} and R_{vir2}), and line impedances (Z_{line1} and Z_{line2}) of each inverter as shown in Fig. 2.

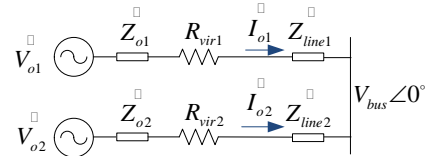


Fig. 2. Equivalent circuit of a parallel inverter system with virtual resistances.

This way, each inverter can be modeled by a two-terminal Thévenin equivalent circuit as follows

$$V_{bus}(s) = G(s) \cdot V_{ref}(s) - [Z_o(s) + Z_{line}(s) + R_{vir}] \cdot I_o(s) \quad (9)$$

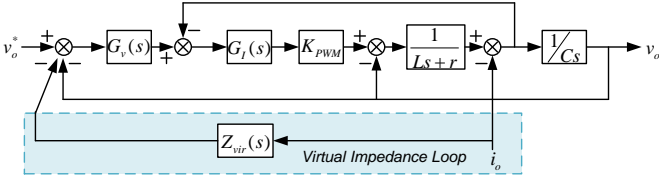
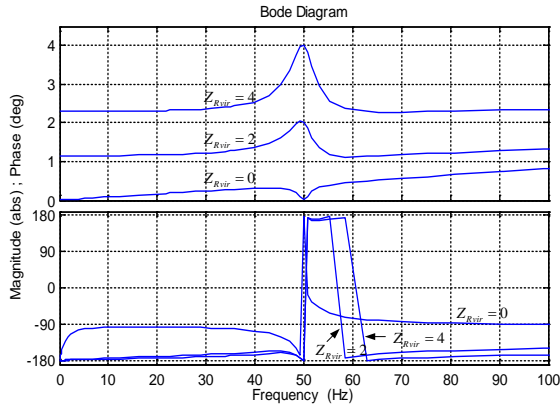


Fig. 3. Block diagram of the closed loop system including virtual impedance.

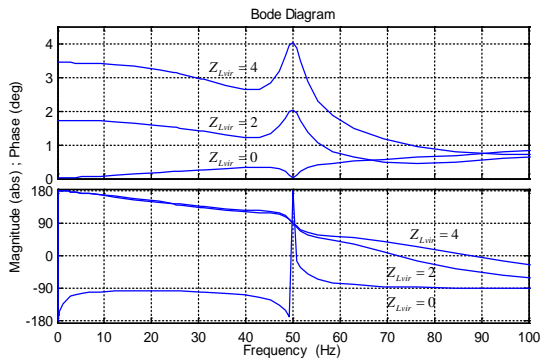
where $V_{ref}(s)$ is the output voltage reference and $G(s)$ is the voltage tracking gain, $G(s) \cdot V_{ref}(s)$ presents the generate voltage of the inverter V_o .

The output impedance of inverter $Z_o(s)$ is not only affected by the filter parameters but also influenced by the controller structure and parameters. The inner current and voltage loops will be responsible to make $Z_o(s)$ as small as possible. In this paper, proportional-resonant (PR) controllers tuned at the line frequency are used to make $Z_o(s)$ equals to zero at 50Hz. The block diagram of inner current and voltage loop with virtual impedance is shown in Fig. 3.

From Fig. 3, the closed loop output impedance $Z_o'(s)$ which is modified by virtual impedance $Z_{vir}(s)$ can be obtained as follows:



(a) Virtual resistance



(b) Virtual inductance

Fig. 4. Bode diagram of the closed-loop output impedance with virtual impedance.

$$Z_o'(s) = -\frac{u_o(s)}{i_o(s)} = \frac{Ls+r+Z_{vir}(s)K_{PWM}G_u(s)G_i(s)}{LCs^2+[r+K_{PWM}G_i(s)]Cs+K_{PWM}G_u(s)G_i(s)+1} \quad (10)$$

where $Z_{vir}(s)$ is the virtual impedance, K_{PWM} is the gain of the pulse width modulation (PWM), $G_u(s)$ is the voltage loop PR controller, $G_i(s)$ is the Proportional controller of the current loop, and L and C are the LC output filter parameters.

The frequency response of the closed-loop output impedance $Z_o'(s)$ for $Z_{vir}(s) = R_{vir}$ and $Z_{vir}(s) = jX_{vir}$ cases are both shown in Fig. 4. From this figure it can be seen that $|Z_o'(s)|$ is highly dependent on the virtual impedance magnitude and angle.

In addition, since $Z_{line}(s)$ is practically very small in low scale electrical systems such as microgrids, R_{vir} becomes the predominant component, so that (1) can be expressed in Laplace domain as

$$V_{bus}(s) = G(s) \cdot V_{ref}(s) - R_{vir} \cdot I_o(s) \quad (11)$$

which corresponds to a Thévenin equivalent circuit, as illustrated in Fig. 5.

In this paper, proportional-resonant (PR) controllers are used to make $G(s)$ equals to 1 at 50Hz. Hence, the relationship of the common bus voltage (V_{bus}), reference voltage (V_{ref}), and output current (I_o) vectors can be expressed in Euler form as follows:

$$\begin{aligned} V_{bus} &= V_{ref} - I_o \cdot R_{vir} \\ &= (V_{ref} \cos \varphi - I_o \cdot R_{vir} \cdot \cos \phi) + j(V_{ref} \sin \varphi - I_o \cdot R_{vir} \cdot \sin \phi) \end{aligned} \quad (12)$$

being φ the voltage reference angle and ϕ the output current angle.

From Fig. 6 we can see that when varying R_{vir} will result in different output current vectors (I_o). We can also express the vectors in a synchronous reference frame by decomposing direct and quadrature components as follows

$$V_{bus} = V_{refd} - R_{vir} \cdot I_{od} \quad (13a)$$

$$0 = V_{refq} - R_{vir} \cdot I_{oq} \quad (13b)$$

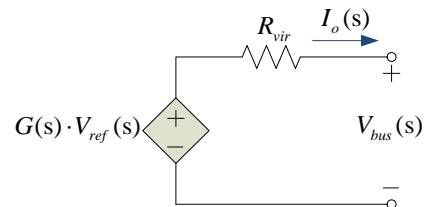


Fig. 5. Inverter closed-loop equivalent Thévenin circuit.

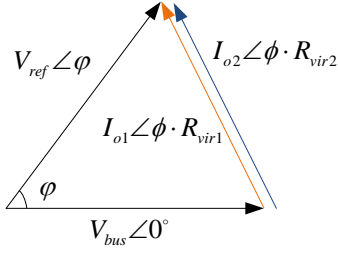


Fig. 6. Vector diagram of the concept.

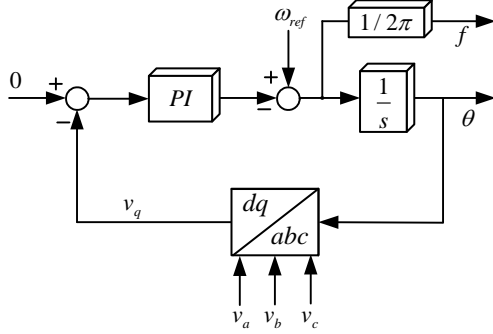


Fig. 8. Detail of the block diagram of the SRF-PLL.

where V_{refd} and V_{refq} are the d axis and q axis component of each inverter's output-voltage references separately. I_{od} and I_{oq} are d axis and q axis components of output current.

Thus, the relationship between I_{od} , I_{oq} and R_{vir} can be generalized and expressed for a number N of converters as

$$I_{od1}R_{vir1} = I_{od2}R_{vir2} = \dots = I_{odN}R_{virN} \quad (14a)$$

$$I_{oq1}R_{vir1} = I_{oq2}R_{vir2} = \dots = I_{oqN}R_{virN} \quad (14b)$$

Note that output d and q axis output currents of paralleled inverters are inversely proportional to their virtual resistances. It can be easily observed that current sharing performance is just influenced by the output impedance ratio instead of the output impedance value of the two inverter modules. Thus, the controller is very suitable for the low voltage microgrid applications.

IV. PROPOSED CONTROL STRATEGY

Based on the above analysis, the proposed control strategy is shown in Fig. 7. The power stage consists of a three-leg three-phase inverter connected to a DC link, loaded by an L_f - C_f filter, and connected to the ac bus by means of a power line (Z_{line}).

The controller includes a synchronous reference frame-based phase locked loop (SRF-PLL) which substitutes the two loops droop control, a virtual resistance loop (R_v), a DC link voltage feed-forward loop, and the conventional PR inner current and voltage loops (G_i and G_v) that generates a PWM signal to drive the IGBTs the inverter. Capacitor currents and voltages are transformed to the stationary reference frame ($i_{ca\beta}$ and $v_{ca\beta}$).

The voltage reference V_{ref} is generated by using the amplitude reference ($|V_{ref}|$) and the phase generated by the PLL. A detailed block diagram of the SRF-PLL is shown in Fig. 8. Even though the PLL is trying to synchronize the inverter with the common AC bus, in case of supplying reactive loads, the quadrature current flowing through the virtual resistance will create unavoidable quadrature voltage drop that will cause an increase of frequency in the PLL. This way the mechanism inherently endows an I_{oq} - f droop characteristic in each inverter.

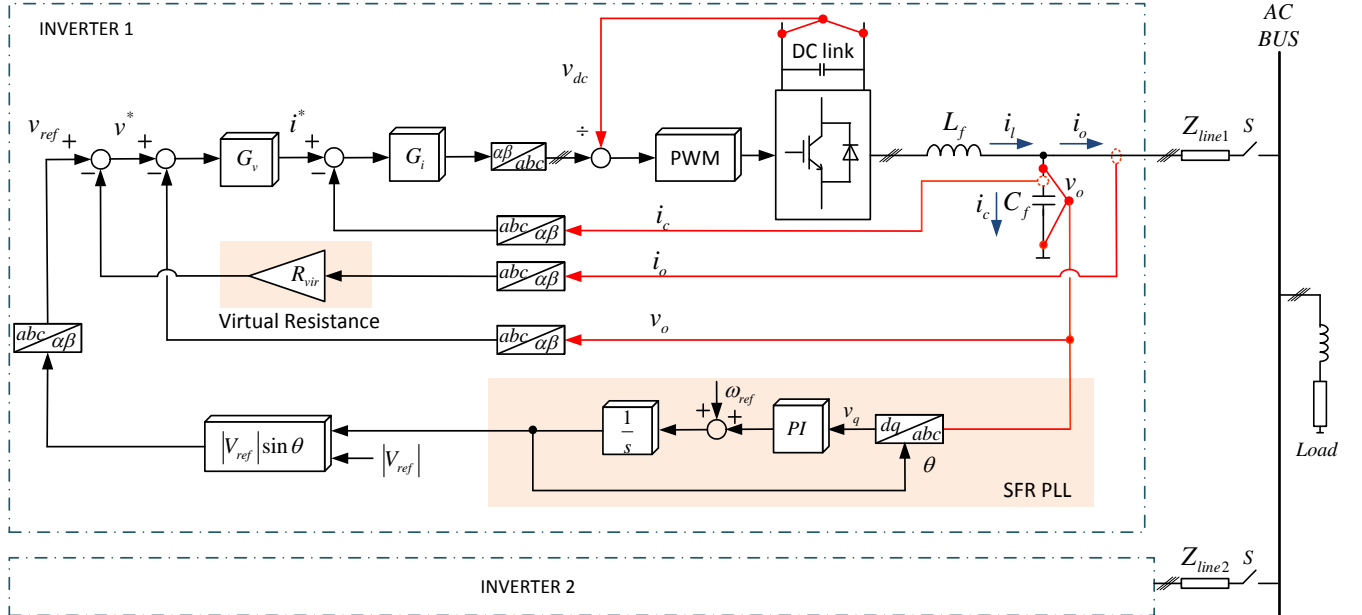


Fig. 7. Block diagram of the proposed control method.

V. EXPERIMENTAL RESULTS AND PERFORMANCE COMPARISON

In order to compare and evaluate the performance of the proposed control scheme with the conventional droop control, a scale-down laboratory prototype is built according to Fig.7. The time-domain model of the proposed control scheme is evaluated in Matlab/Simulink environment. The TMS320F2812 DSP based platform has been chosen for the real-time digital experimental tests. The system parameters are given in Table I and II.

TABLE I
SYSTEM PARAMETERS OF PROPOSED CONTROLLER

Parameters	Values	Parameters	Values
U_{dc}	250 V	C_f	9.9 μ F
k_{pi}	0.603	k_i	18.47
R_{load}	20 Ω	f_c	40 kHz
L_f	3 mH	ω_c	30 rad/s
k_p	0.053	R_{vir}	3 Ω
f_s	20 kHz	L_{line}	7/3.5/0 mH

TABLE III
SYSTEM PARAMETERS OF CONVENTIONAL DROOP CONTROLLER

Parameters	Values	Parameters	Values
U_{dc}	250 V	C_f	9.9 μ F
k_{pi}	0.603	k_i	18.47
k_{qV}	0.001	f_c	40 kHz
R_{load}	20 Ω	P^*	750 W
L_f	3 mH	ω_c	30 rd/s
k_p	0.053	$k_{p\omega}$	4×10^{-3}
f_s	20 kHz	L_{line}	7/3.5/0 mH
R_{start}	2 Ω	Q^*	750 var

Fig. 9 shows the simulation results of the paralleled inverter system by using the proposed control scheme. We can see that the active and reactive powers can be precisely controlled according to the ratio of the virtual resistance (1:2). In order to verify the feasibility of the proposed controller, different operating conditions have been considered in the experimental tests.

A. Experimental tests comparison for large line impedance ($L_{line} = 7mH$)

Fig. 10 shows the output voltages and currents transient response for both the conventional droop control and the proposed controller when sharing a pure resistive load. Firstly, inverter #2 works standalone and then inverter #1 is plugged to the point of common coupling (PCC) to share the load with inverter #2. In order to damp the initial transient current and achieve the hot-swappable performance, a 2 Ω virtual resistance R_{start} used by inverter #2, lasting for 2 s when employing conventional droop control. It can be observed that the proposed controller can provide higher speed, and better

damping and precision performance power control than those in conventional droop control.

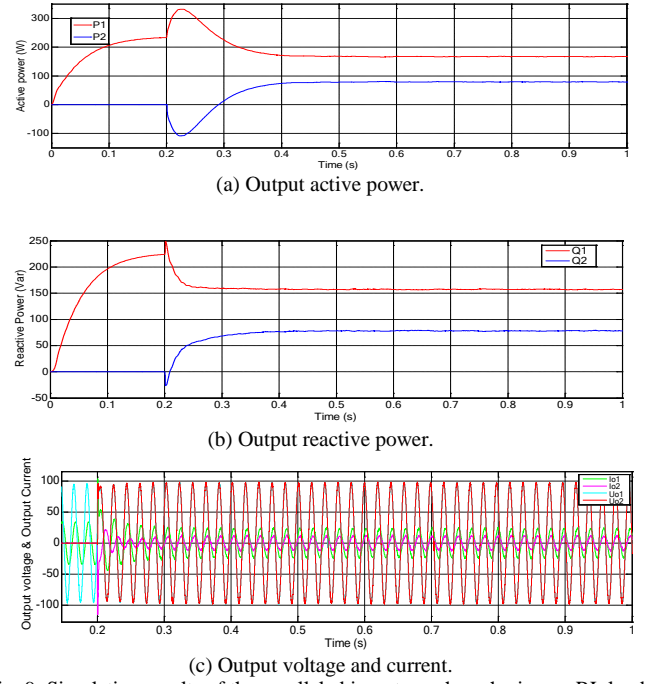
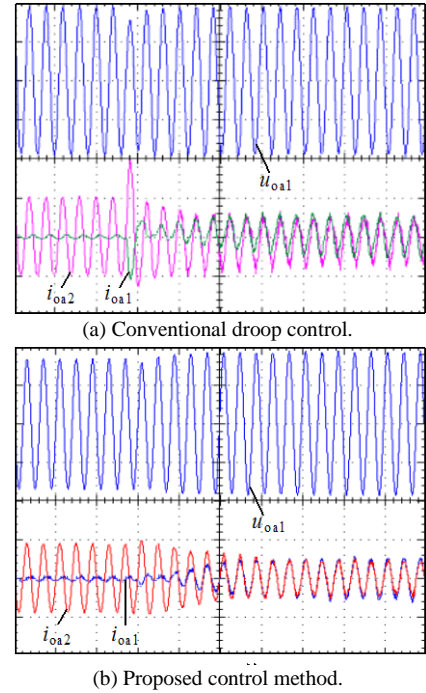


Fig. 9. Simulation results of the paralleled inverters when sharing an RL load.

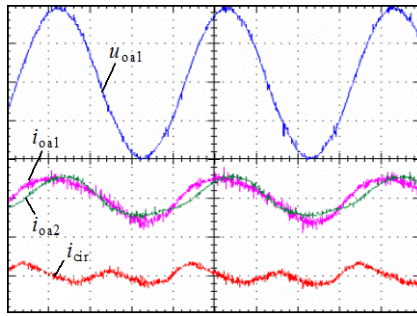


(X-axis: time (a) 50 ms/div, (b) 5 ms/div, Y-axis: U 50V/div, i 5A/div)
Fig. 10. Compared experimental results of transient responses for parallel inverters.

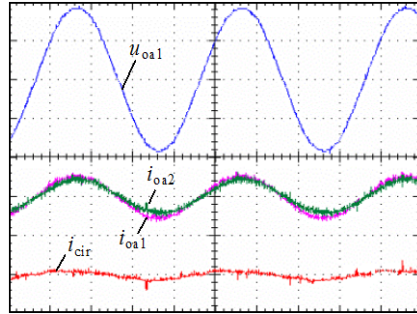
Fig.11 shows the steady output voltage waveform of inverter #1, output currents of both inverters and the circulating current based for both conventional droop and proposed controller. From Fig. 11, it can be observed that the

conventional droop control strategy can achieve load-sharing capability between the parallel inverters, but the circulating current is still large. The peak value of circulating current is nearly 2 A, which represents almost half of the inverter rated output current. The reason leading to this phenomenon is the presence of high-frequency harmonics in the capacitor current. This current is used as feed-forward of the internal current loop to improve the dynamic response and its harmonics result in waveform quality deterioration and increase of the circulating current. However the current sharing performance is quite good when employing the proposed controller in comparison with the droop control. The maximum value of circulating current is just 0.4 A.

Fig.12 shows the cut-off responses when inverter#1 disconnects from the PCC for the case of using conventional droop controller and the proposed one. It can be observed that when the inverter #1 is disconnected from the PCC, the output current of inverter #2 increases immediately to supply the load.



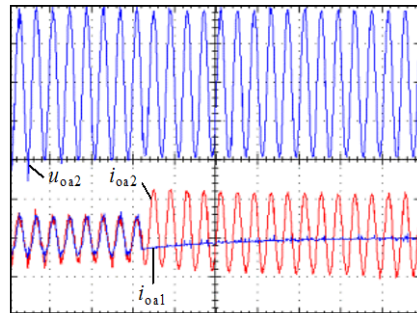
(a) Conventional droop control.



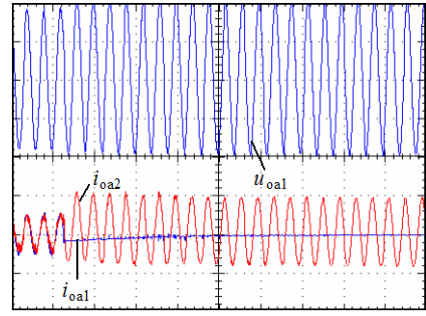
(b) Proposed control method.

(X-axis: time 5 ms/div, Y-axis: U 50V/div, i 5A/div)

Fig. 11. Experimental results comparison of the steady state waveforms.



(a) Conventional droop control.



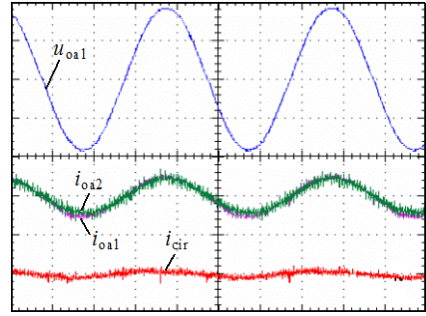
(b) Proposed control method.

(X-axis: time 50 ms/div, Y-axis: U 50V/div, i 5A/div)

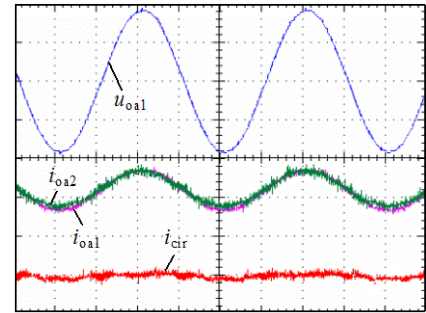
Fig. 12. Experimental results comparison between transient responses.

B. Experimental tests comparison for small line impedance ($L_{line} = 3.5 \text{ mH}$ and $L_{line} = 0 \text{ mH}$)

The paralleled inverter system becomes unstable when using droop control with same parameters when the line impedance is reduced to 3.5 mH. The large transient over current results in activating the protection system when both inverters were connected. In contrast, the proposed controller can maintain the load sharing capability with $L_{line} = 3.5 \text{ mH}$ and even 0 mH, as shown in Fig. 13, while the droop control was not able to endow a stable operation in such conditions.



(a) $L_{line} = 3.5 \text{ mH}$.



(b) $L_{line} = 0 \text{ mH}$.

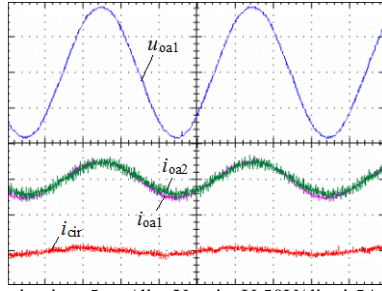
(X-axis: time 5 ms/div, Y-axis: U 50V/div, i 5A/div)

Fig. 13. Steady waveforms of the parallel inverters using the proposed controller under small line impedance.

C. Experimental tests with asymmetrical line impedance ($L_{line1} = 7 \text{ mH}$, $L_{line2} = 3.5 \text{ mH}$)

Fig. 14 shows the current-sharing performance under asymmetrical line impedance when using the proposed controller. It can be observed that the proposed controller can

enlarge system stability margin, while obtaining a good load-sharing capability even under asymmetrical line impedance as shown in Fig. 14, even when the droop controller was not able to provide system stability.



(X-axis: time 5 ms/div, Y-axis: U 50V/div, i 5A/div)

Fig. 14. Steady waveforms of the parallel inverters with the U-I droop controller under different Line impedance.

The performance comparisons between both controllers are summarized in Table I. The proposed controller is faster than droop method since it does not require P/Q calculations, which limit the bandwidth of the system. Further, the use of filters, especially finite impulse response (FIR) requires increase the computational burden. Note that the conventional droop control requires for additional virtual impedance if we want to improve the aforementioned problems. In addition, conventional droop control is more complex to design since we need to adjust two droop coefficients plus the virtual impedance value. So that two terms (R_v and $Q-V$ droop gain value) has to be considered at the same time to respect both maximum voltage deviation and proper transient response. The proposed controller solves the trade-off by only using the parameter R_v . There is a tradeoff between the power sharing accuracy and the voltage amplitude.

VI. CONCLUSION

This paper proposed a novel control strategy which based on a virtual impedance and phase locked loop, which substitutes the conventional two droop control loops, for a parallel three-phase inverters. The load sharing performance of this controller just depends on output impedance ratio instead of the output impedance value of the two inverter modules which makes it quiet suitable applied in low-voltage microgrids with small line impedance values. In comparison to the traditional droop controller, the proposed controller could obtain faster dynamic response, extended stability margin, and simple control parameters design.

TABLE III
PERFORMANCE COMPARISON

Performances	P-V/Q-V droop	Proposed control
Transient response	Slow	Fast
Control design	Complex	Simple
Computational load	High	Low
Control parameters	m, n, R_v	R_v

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