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Fast and Accurate Icepak-PSpice Co-Simulation of IGBTs under Short-Circuit with an Advanced PSpice Model

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Abstract

A basic problem in the IGBT short-circuit failure mechanism study is to obtain realistic temperature distribution inside the chip, which demands accurate electrical simulation to obtain power loss distribution as well as detailed IGBT geometry and material information. This paper describes an unprecedented fast and accurate approach to electro-thermal simulation of power IGBTs suitable to simulate normal as well as abnormal conditions based on an advanced physics-based PSpice model together with ANSYS/Icepak FEM thermal simulator in a closed loop. Through this approach, significantly faster simulation speed with respect to conventional double-physics simulations, together with very accurate results can be achieved. A case study is given which presents the detailed electrical and thermal simulation results of an IGBT module under short circuit conditions. Furthermore, thermal maps in the case of non-uniform threshold voltage/ solder resistance/ gate resistance among the cells are presented in comparison with the case of uniform distribution, evidencing the capabilities of studying short-circuit of aged devices by the presented technique.

1 Introduction

In modern power electronic systems, one of the challenges is to design robust and reliable power electronic products while avoiding over-sized design margins [1]. Meanwhile, simulation tools have played an important role in researching and optimized designing of power semiconductors and power electronic systems. One of the trends of simulation technologies in power electronics is toward multi-disciplinary design platform which includes electrical, thermal, magnetic and mechanical simulations [2]. For instance, the phenomena of current constriction and thermal runaway, which are responsible for failures of IGBT modules during heavy loads and short circuits, are usually connected with a critically high junction temperature. To well study these issues, a precise electro-thermal simulation is needed to accurately estimate the junction temperature of IGBT modules in order to determine the robustness margins and prevent potential failures with high confidence levels.

There is already plenty of research work on electrical-thermal co-simulation of power electronic devices and packages. C.-

H. Lin obtained hot spots caused by high current density crowding in Printed Circuit Board (PCB) packages by using commercial electrical-thermal co-simulating Finite-Element Method (FEM) tools. The difference between co-simulation and infrared camera measurement was less than 10%, however the computing time is not mentioned and could be very slow for a more complicated system, for example power semiconductors [3]. J. Xie and M. Swaminathan utilized a comprehensive finite volume modelling of electric potential distribution equations and heat equations to implement electrical-thermal co-simulations of electronic packages [4]. Similarly, T. Lu and J. Jin improved traditional electrical-thermal FEM co-simulation to gain faster speed of electronic packages (e.g. PCB board) [5]. Proposed co-simulations are aimed at integrated circuit (IC) simulations and optimizations, which are hard to extend to power semiconductor study since advanced electrical model is absent.

Concerning power semiconductor study, some researchers attempted to extend widely-used very accurate electrical simulation tools (e.g. Spice, Saber) to electrical-thermal simulations by introducing lumped thermal impedance, but they cannot provide accurate junction temperature as well as temperature distribution and hot spots in power semiconductors because of the intrinsic limitation of such tools in the number of nodes to few thousands [6-8]. There are also commercial multi-discipline tools, e.g. SystemVision [9], which can connect multiple domain-specific tools (MathWorks Simulink, National Instruments LabVIEW, SystemC, C/C++, Java, and Spice) and processes, together in a single simulation environment, but still lacking of accuracy due to using lumped thermal impedance.

On the other hand, FEM software are very specialized to single physics, e.g. electromagnetic physics, thermal physics, semiconductor physics, etc., but they lack in optimization when a multi-physics approach is used, so that a dramatic worsening in simulation times and sometimes in accuracy is obtained. For instance, thermal simulation with Icepak [10] can be connected to circuit-level simulator Simplorer [11] in ANSYS, but the process is heavy and slow (seconds per simulation point). Besides slowness, a lot of information is unavoidably omitted by this intrinsically-single-cell approximation method, e.g. uneven fast junction temperature variation and hot spots dynamics in the semiconductor chips, which strongly limit the prediction of imbalances among the cells of the real device. This issue becomes even more critical for power semiconductors under abnormal conditions (e.g. short-circuit, overload), where two physics at high accuracy

levels are required. There, it is vital to determine the precise distributed dynamic power density input to thermal FEM simulation. Of course, a compact electrical model can be integrated into FEM thermal simulators [12-13], which can reduce the computing time but also the accuracy. Another way is physical cell-level (i.e. in the scale of few square microns) FEM simulation, like TCAD, which can hardly predict the temperature distribution among several cells [14], which is critical for studying short-circuit behavior, especially for aged device.

A novel perspective could be connecting a physics-based, device-level, distributed electrical simulation tool, to a thermal FEM simulation. This could gain flexibility on the electrical side without losing accuracy on the thermal side. A physics-based IGBT model in PSpice which has shown accurate results, high modularity and fast simulating speed as well is a good candidate to this aim [15].

This paper discusses the aforementioned co-simulation approach to the electro-thermal simulation of power IGBTs adopting the model presented in [15], which is suitable to simulate normal as well as abnormal conditions. Moreover, among other things, one large advantage of such approach is that independent time steps can be adopted for the electrical and thermal parts, thus gaining huge calculation efficiency. A case study is given which will present the detailed electrical and thermal simulation results of an IGBT module under short circuit conditions based on such advanced PSpice model. Furthermore, thermal maps in the case of non-uniform threshold voltage/solder contact resistance/ gate resistance among the cells have been achieved together with the case of uniform distribution, evidencing the new approach's capabilities of studying the impact of variations of geometry and electrical parameters due to manufacturing process and/or material degradation on short-circuit in aged devices.

2 IGBT electro-thermal simulation setup

The proposed electro-thermal co-simulation method includes three major parts: IGBT electrical model in PSpice, IGBT thermal analysis model in ANSYS/Icepak, and a monitoring program in MATLAB. Based on the electrical simulation, a map of power loss distribution inside the chip is obtained and sent to the ANSYS thermal simulation, then ANSYS/Icepak thermal simulation feeds back the temperature distribution to the PSpice electrical simulation, so finally the chip temperature distribution can be achieved. The simulation

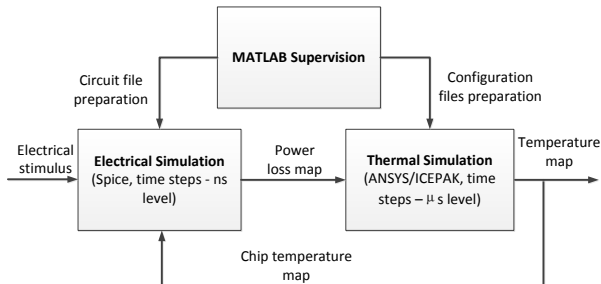


Fig. 1. Structure of the proposal simulation setup

setup structure is shown in Fig. 1, whose details will be illustrated as follows.

2.1 PSpice model preparation

The physics-based lumped charge IGBT model proposed in [15] shows more accurate results and comparable simulation speed for high voltage IGBTs than the PSpice IGBT native model. Here its operating principle is briefly described. The basic idea is subdividing the device into a few regions characterized by constant doping and/or carrier lifetime, and the behaviour of each region is described by means of few lumped charges placed in proper aggregation points, which is shown in Fig. 2, resulting in a very compact model.

In such model, few parameters must be identified [15]: chip area, transconductance, stray resistance, stray inductance, and gate capacitances, most of them directly obtainable from the datasheet. In the co-simulation, the IGBT chip is simulated as a PSpice circuit containing an arbitrary number of cells, each of whose is a model like the one of Fig. 2, whose area is opportunely scaled.

2.2 Icepak model preparation

A detailed Icepak geometry model is necessary for thermal simulation. In the case study, the geometry of the considered setup is shown in Fig. 3(a), and the cross section in the vertical plane is shown in Fig. 3(b): one 12.5mm wide square IGBT chip and one 9mm wide square diode chip are mounted together in a module, whose ratings are 1700V/25A. Apart from the chips, the module consists of standard DCB sections soldered to a Cu baseplate.

All geometry and material information are included in the Icepak “model” file, in which the power loss information is blank and will be updated by the PSpice simulation later. All thermal simulation setting information are included in the Icepak “problem” file, in which the monitoring points,

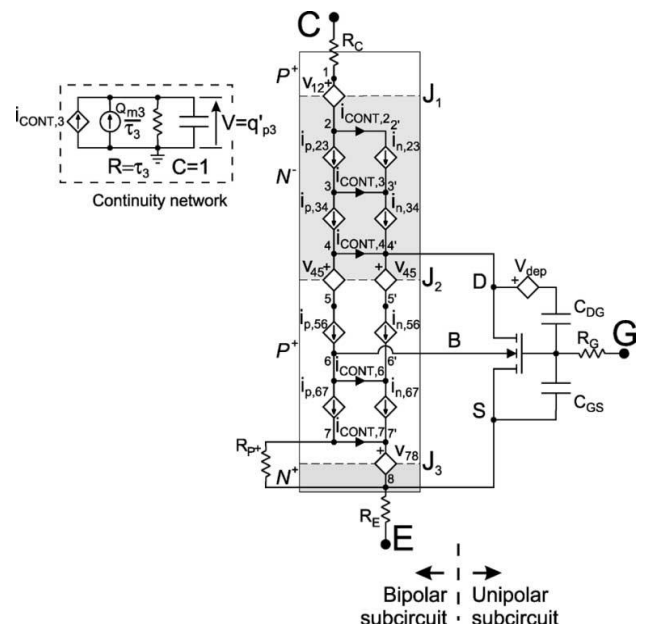


Fig. 2. Overall IGBT lumped charge model [15].

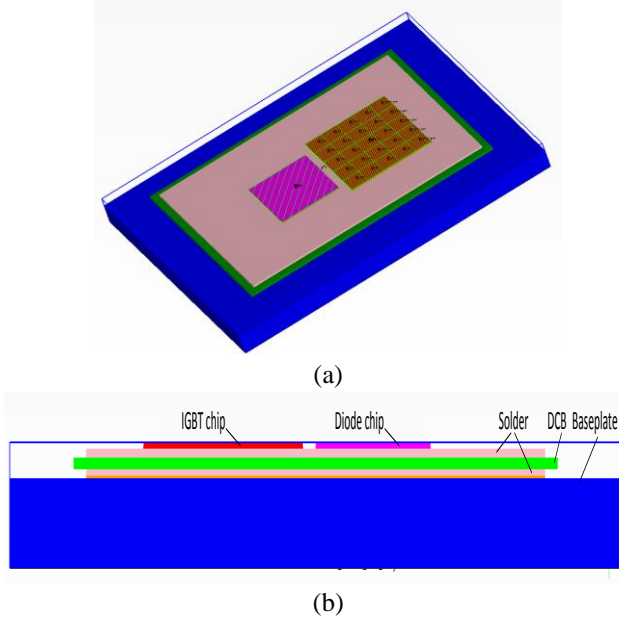


Fig. 3. (a) Geometry of the considered setup; (b) details of the cross section on the vertical plane together with simulation step and end times are defined.

2.3 MATLAB co-simulation script

The presented approach is implemented as a Matlab script which coordinates the above two software at each thermal simulation step. Operations are divided in preparation time and simulation time.

At the preparation time, the Matlab script automatically divides the device under test (i.e. the IGBT) in an arbitrary number of virtual cells. The only condition required is that it should be rectangle-shaped. In the study case, a 5-by-5 array of cells has been adopted (see Fig. 3.a). Cells include power sources placed on a layer at the surface of the IGBT chip. One PSpice subcircuit is automatically generated for each cell

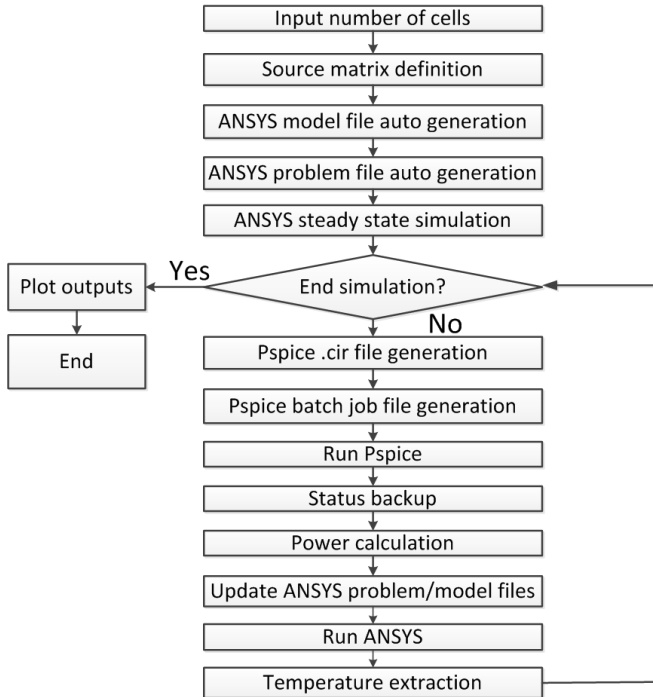


Fig. 4. Matlab Script Flow chart.

starting from a circuit template file, that includes the parameter identified for the considered device, and all of them are connected in parallel. The user-defined external PSpice circuit provides the required electrical stimuli.

At the simulation time, power loss of each cell is calculated by the PSpice circuit with arbitrary time accuracy (typically nanoseconds) for a given constant temperature map. The Pspice simulation lasts a thermal time step (typically in the range of microseconds) and it is stopped. At this point, dissipated power losses are given to the thermal block – the “model” and “problem” files in Icepak are updated accordingly, and the thermal simulation in Icepak is run. Afterwards, temperatures are input back to the PSpice model and so forth. This process is illustrated in Fig. 4 and continues until the end of simulation.

3 Results and discussion

In the case study we propose, the setup shown in Fig. 3 is subject to several short circuit tests. The IGBT chip is divided into 5 by 5 cells, and the typical simulation duration is 16 μ s, including 8 steps, 2 μ s each. It is worth to note that the diode does not operate in this case. Short-circuit happens at 5 μ s, and ends at 9 μ s. Each step takes around 90 s to be evaluated (12 minutes in total for 4*17 cores@ 2.6Ghz, 4Gb RAM DDR3), including automatic power loss loading, thermal initial condition setting, Icepak thermal simulation, temperature data saving, cell temperature loading, electrical

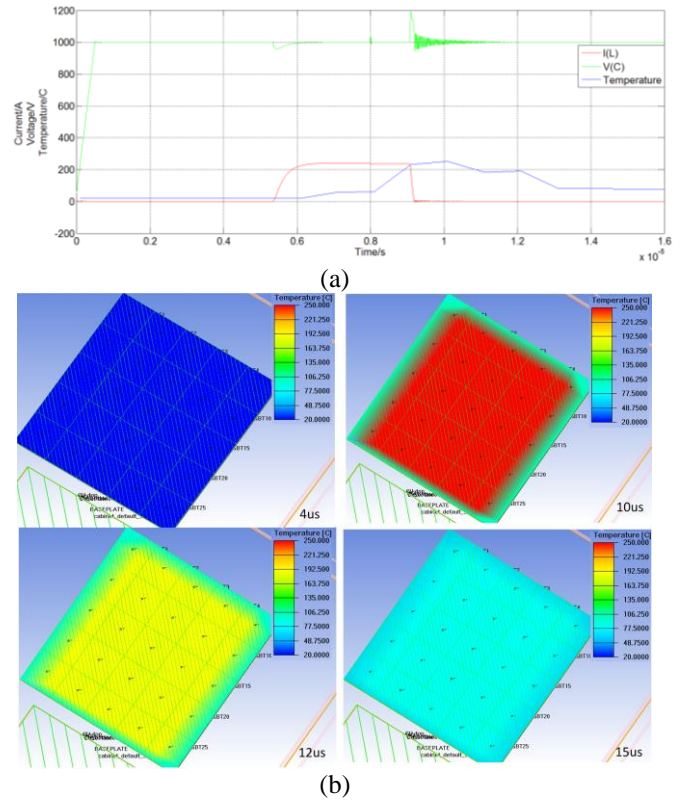


Fig. 5. (a) Short-circuit current/voltage PSPICE waveforms; (b) IGBT chip temperature map in ICEPAK during short-circuit at 4/10/12/15 μ s (times bottom right of each image)

initial condition setting, PSpice simulation and power loss data saving.

3.1 Balanced short-circuit simulation

When short-circuit happens during IGBT turn-on (at time=5 μ s), collector current I_c rises rapidly until reaching saturated value - 230A, as shown in Fig. 5(a). On the same picture the simulated temperature is reported. As the reader can see, sampling time has been arbitrary set to 1 μ s, and IGBT chip's temperature rise as high as 250 $^{\circ}$ C at 10 μ s. After the short-circuit turn-off, the chip temperature falls to normal value again. Temperature rises and falls uniformly on the whole chip but the periphery, where cells are cooler than the central ones.

3.2 Short-circuit simulation on imbalanced V_{th}

As announced before, the proposed electro-thermal co-simulation method has been used to simulate imbalances among the cells in the chip. In fact, due to aging and/or stresses in the real lifetime of the module, degradations and deviations of electrical parameters (e.g. collector resistance R_c , gate resistance R_g , and threshold voltage V_{th}) are

common among the several cells inside the IGBT chip.

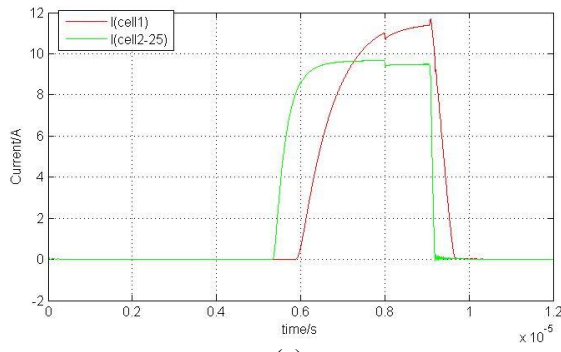
A case study of imbalance in V_{th} is here given. In the PSpice model, the upper-left-corner cell V_{th} is lower than the other cells, which leads to the imbalanced short-circuit current as shown in Fig. 6(a).

Between 10 μ s and 11 μ s, a hot spot formation is evidenced by the temperature rising back, as shown in Fig. 6(b). This is confirmed by Fig. 6(a), where the current of the sole cell increases without control up to the turn off time.

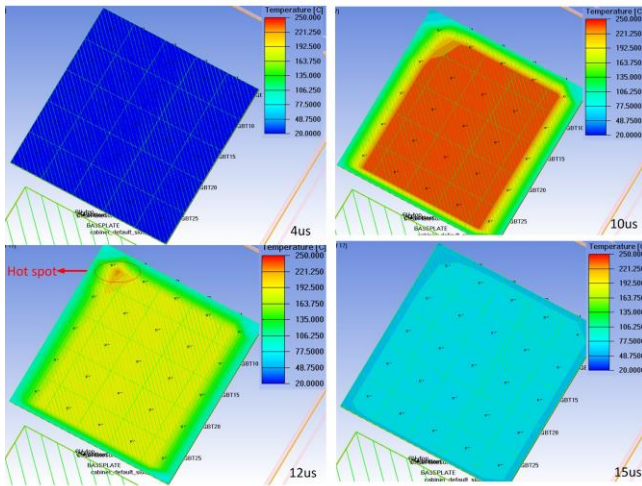
3.3 Short-circuit simulation on imbalanced R_c

In the real lifetime of IGBT module, the solder degradation will unavoidably happen to some parts of the chip. Consequently, there will be imbalanced R_c inside the chip. The proposed electro-thermal co-simulation supplies capability to analyse the impact of this material degradation.

A case study is here given. In Fig. 7(a) the green cells are characterized by higher R_c than the other cells, in order to simulate contact degradation of such cells. Poor contacts lead to the higher R_c and lower current, therefore to imbalanced short-circuit current densities. During the short-circuit, the unequal temperature distribution is effectively predicted, as shown in Fig. 7(b).

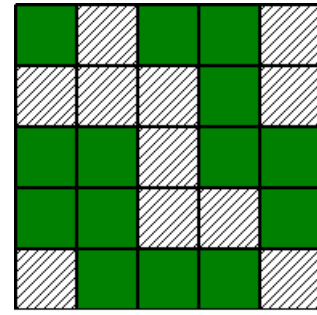


(a)

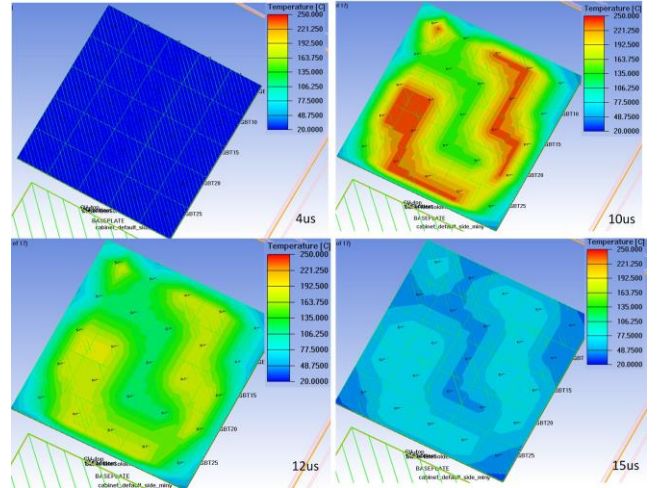


(b)

Fig. 6. (a) Unbalanced short-circuit current in PSPICE; (b) IGBT chip temperature map due to unbalanced V_{th} at 4/10/12/15 μ s (times bottom right of each image)



(a)



(b)

Fig. 7. (a) Unbalanced R_c inside the chip, green cells with normal contacts, hatched are degraded cells; (b) IGBT chip temperature map due to unbalanced R_c at 4/10/12/15 μ s (times bottom right of each image)

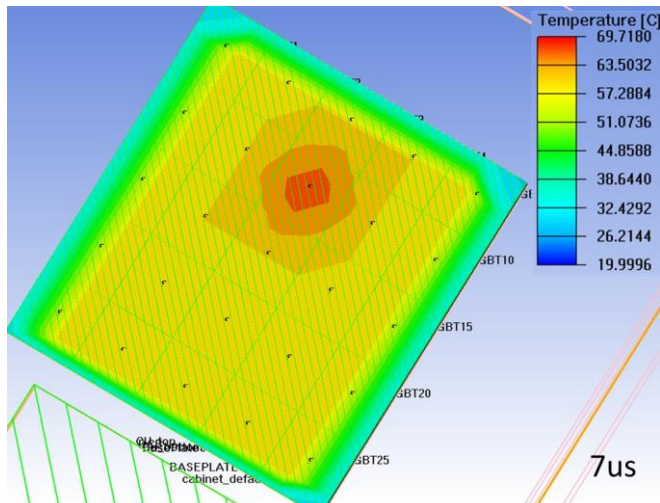


Fig. 8. Unbalanced R_g leads to IGBT chip temperature map during short-circuit turn-on at 7 μ s

3.4 Short-circuit simulation on imbalanced R_g

The proposed electro-thermal co-simulation also supplies capability to analyse the impact of variations of geometry parameters, for example the imbalanced R_g due to location. In this latter case study, the cell under the gate bond wire has much smaller gate resistance, which leads to faster turn-on than the other cells. Consequently, a hot spot during turn-on is correctly predicted, as shown in Fig. 8, although it doesn't lead to instability.

4 Conclusions

A new approach involving ANSYS/Icepak and an advanced IGBT PSpice model has been presented, that exhibits an unprecedented compromise between accuracy of results and simulation speed. The approach successfully predicts abnormal operating conditions like hot spots due to variations of the electrical and geometrical parameters among the device cells, for example threshold voltage and solder resistance.

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