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Design and Implementation of a 1-5 GHz UWB Low Noise Amplifier in 0.18 μm CMOS

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Abstract This paper presents a compact two-stage ultra-wideband low-noise amplifier (LNA). A common-gate topology is adopted for the input stage to achieve wideband input matching, while a cascode stage is used as the second stage to provide power gain at high frequencies. A low power consumption and a small chip area are obtained by optimizing the performance of the LNA with tight constraint on biasing current and reducing the number of inductors to two. The LNA has been fabricated in a standard 0.18 μm CMOS technology for experimental verification. The LNA achieves a power gain of 11-13.7 dB and a noise figure of 5.0-6.5 dB in the frequency band 1-5 GHz. The measured third order (two-tone) input intercept point (IIP3) is -9.8 dBm at 4 GHz. The LNA consumes 9 mW with a 1.8 V supply, and it occupies an area of 0.78 mm^2.

Keywords Ultra-wideband · low noise amplifier · CMOS

1 Introduction

In 2002, the Federal Communication Committee (FCC) authorized the unlicensed use of the ultra wideband (UWB) frequency band from 3.1 to 10.6 GHz for indoor and handheld systems [1]. Since then, a considerable effort has been put into the development of devices suitable for UWB applications. As one of the essential components, UWB low noise amplifiers (LNAs) have attracted significant research interest and various approaches to the design of UWB LNAs have been proposed [2–14]. Due to FCC's limitations on the broad bandwidth (no less than 500 MHz) and low power emission (EIRP lower than -41.3 dBm/MHz) of an UWB system, an UWB LNA must fulfill several challenging requirements. The LNA must provide a good input matching over a band more than 500 MHz. A high gain is also preferred to amplify the weak signal at the receiver and overcome the noise effects from subsequent stages. In addition, the noise figure of the LNA must be low since it plays a major role in defining the receiver's sensitivity. Moreover, the LNA has to be power efficient and physically small to save power and reduce the cost, respectively.

Cascode configured UWB LNAs using LC bandpass filters to achieve a broad band input matching have previously been reported [2]. However, such designs depend on the use of five inductors which in turn increases the size of the circuit (1.1 mm^2). A 0-11 GHz distributed LNA has also been proposed [3]. However, the feasibility of this design is also limited by its large size (1.44 mm^2) and high power consumption (100 mW). An UWB LNA with a stop band at 5-6 GHz to reject the in-band WLAN signals (such as IEEE 802.11a with the lower band of 5.15-5.35 GHz and higher band of 5.725-5.825 GHz) has been proposed [7]. But this design suffers the shortcoming of degraded noise performance in the upper passband (NF$>$7 dB). Aiming at using only the lower UWB band, a 3-6 GHz UWB LNA has been proposed [6]. But its power consumption is relatively high (59.4 mW).

From published literature it is clear that simultaneously fulfilling all requirements for an UWB LNA is a difficult task. This work presents the design of an UWB LNA that aims to meet all performance requirements simultaneously. A second application of this LNA is for the study on impact evaluation of substrate noise on broadband circuits. For that reason the lower bound of the operation band in this design is set to 1 GHz. This is done while maintaining the performance desired in the UWB band of 3-5 GHz. Moreover, the 1-5 GHz operation band also allows a broadband substrate

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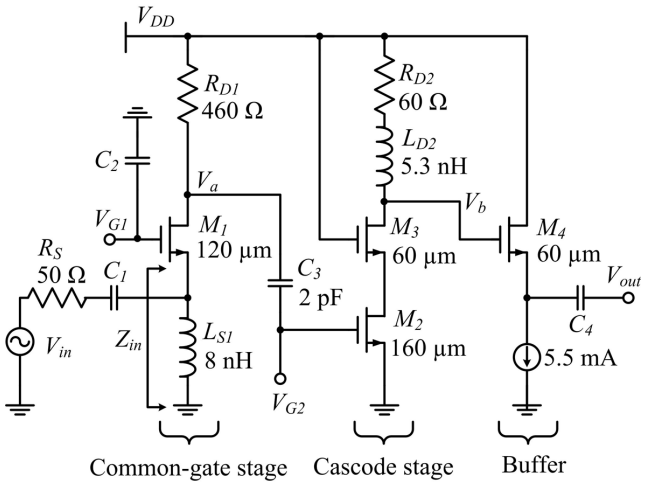

Fig. 1 The schematic for the proposed UWB LNA, including an output buffer for measurement purposes. V_{G1} and V_{G2} are the biasing voltage for the common-gate stage and cascode stage, respectively. V_a, V_b and V_{out} are the output voltages for the common-gate stage, cascode stage and buffer, respectively. $C_1 = C_2 = C_4 = 10$ pF.

noise analysis in a controllable testing environment. Using the available literature as references, the specific goal here is to achieve a low-power (<10 mW) operation, small size (smaller than 1 mm^2) and medium gain (power gain>10 dB) UWB LNA, providing an $|S_{11}|$ less than -10 dB over the lower UWB passband. A small noise figure and an IIP3 higher than -10 dBm are also targeted. An UWB LNA with a common-gate stage as the first stage, and a cascode stage as the second stage is proposed. This topology holds the good potential for wide band applications. But its application for UWB has not been fully explored by previous work, and thus deserves more study. Different from conventional common-gate LNAs that use an inductor as the drain load of the transistor [9], a resistor is used as the load to reduce chip area. Comprehensive analysis on the gain and matching of the LNA has been presented. A test chip using a standard 0.18 μm CMOS technology has been fabricated for experimental verification, and good results were measured.

2 Analysis and design of the UWB LNA

The proposed UWB LNA is shown in Fig. 1. To achieve a wideband input matching, a common-gate stage is used as the first stage since it holds superior potential for wideband design than other configurations, such as inductive source degeneration, direct resistor termination and shunt series feedback [9]. A cascode stage is used as the second stage to provide gain at higher frequencies. In addition an output buffer is added for measurement purposes [2, 4, 8, 10–14].

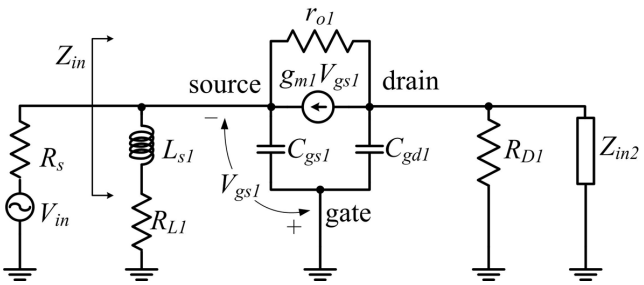

Fig. 2 The small-signal equivalent circuit used for calculating the input impedance of the common-gate stage in Fig. 1.

2.1 Matching and gain of the common-gate stage

The small-signal equivalent circuit of the common-gate stage is shown in Fig. 2, where g_{m1} is the transconductance of M_1. L_{s1} is used to obtain a wideband input matching together with the gate-source capacitor C_{gs1}. R_{L1} is the series resistance of L_{s1}. r_{o1} and C_{gd1} are the output resistance and the gate-drain capacitor of the transistor, respectively. R_{D1} is the load at the drain of the transistor, and Z_{in2} is the input impedance of the next stage. Based on Fig. 2, the input impedance Z_{in} of the common-gate stage can be derived as

$$Z_{in}(s) = 1/\left[\frac{1+(g_{m1}+sC_{gs1})(R_{L_1}+sL_{s1})}{R_{L_1}+sL_{s1}} + \frac{1-g_{m1}Z_o(s)}{r_{o1}+Z_o(s)}\right], \quad (1)$$

where

$$Z_o(s) = R_{D1} \parallel Z_{in2} \parallel \frac{1}{sC_{gd1}}. \quad (2)$$

Assuming $r_{o1} \gg |1-g_{m1}Z_o(s)|$ and neglecting the loading effect of the second stage which will be included in Section 3, Eq. (1) can be simplified as

$$Z_{in}(s) = \frac{R_{L_1}+sL_{s1}}{1+(g_{m1}+sC_{gs1})(R_{L_1}+sL_{s1})}. \quad (3)$$

Using Eq. (3), the effects of the circuit parameters on Z_{in} can be analyzed, and values of the parameters for the desired input matching can be optimized. It is easy to see that at low frequencies, where $|(g_{m1}+sC_{gs1})(R_{L_1}+sL_{s1})|$ is much smaller than 1, Eq. (3) can be approximated as $Z_{in} \approx R_{L_1}+sL_{s1}$. For higher frequencies where $|(g_{m1}+sC_{gs1})(R_{L_1}+sL_{s1})|$ is relatively large and $|sC_{gs1}|$ is still small compared to g_{m1}, Eq. (3) approximates as $Z_{in} \approx 1/g_{m1}$. For very high frequencies where $|(g_{m1}+sC_{gs1})(R_{L_1}+sL_{s1})|$ is relatively large and $|sC_{gs1}|$ is considerably larger than g_{m1}, Eq. (3) approximates as $Z_{in} \approx 1/sC_{gs1}$. This indicates that $1/g_{m1}$ only determines the matching level, and that the location of the optimum matching frequency is determined by L_{s1} and C_{gs1}.

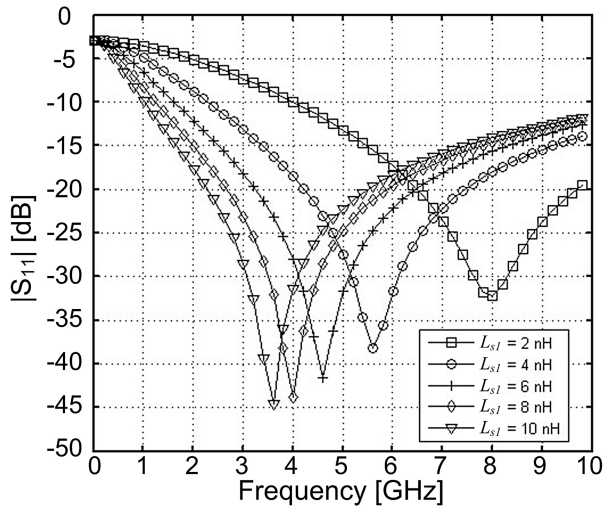

Fig. 3 Calculated $|S_{11}|$ versus frequency with varied L_{s1}. Other parameters used in this figure are: $1/g_{m1} = 50\,\Omega$, $R_{L_1} = 10\,\Omega$ and $C_{gs1} = 200$ fF.

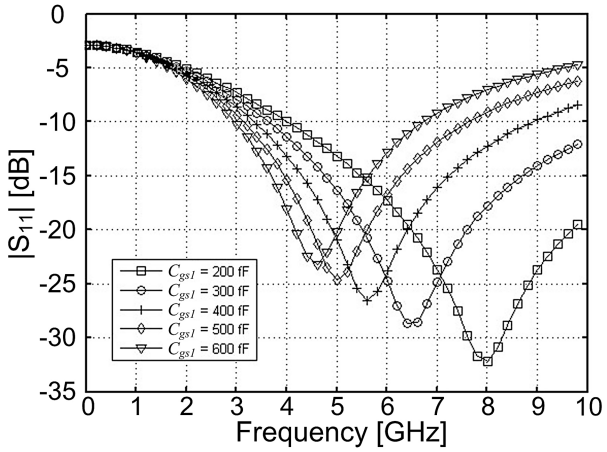

Fig. 4 Calculated $|S_{11}|$ versus frequency with varied C_{gs1}. Other parameters used in this figure are: $1/g_{m1} = 50\,\Omega$, $R_{L_1} = 10\,\Omega$ and $L_{s1} = 2$ nH.

In order to obtain a good input matching at the desired frequency band, the effects of L_{s1} and C_{gs1} on the input matching have been studied. Based on Eq. (3), the calculated $|S_{11}|$s of the common-gate stage with five different values of L_{s1} are shown in Fig. 3. In the calculation, other parameters are kept as constants. It can be seen that the effect of L_{s1} is much stronger at lower frequencies than higher frequencies. This means that a relatively large inductor should be used to ensure a good input matching at lower frequencies. In this design, L_{s1} is chosen to 8 nH to ensure that $|S_{11}|$ is lower than -10 dB at 3 GHz. Moreover, the calculated $|S_{11}|$s of the common-gate stage with five different values of C_{gs1} are shown in Fig. 4. In the calculation, C_{gs1} is varied as other parameters are kept as constants. It is shown that the effects of C_{gs1} on S_{11} are much more obvious at higher frequencies, which indicates that a relatively small C_{gs1} should be used to achieve a good input matching at high frequencies. However, an increased drain current is needed to have a proper g_{m1} for optimum input matching while using a small sized M_1. To avoid a dramatic increase in power consumption, the minimum size of M_1 is limited by the targeted DC biasing current in this stage. In order to fulfill the target of a power consumption less than 10 mW at a 1.8 V supply, the total biasing current for the LNA should be less than 5.5 mA. In this design, about half of this budget (2.4 mA) is used in the common-gate stage. In addition, at the frequency where the input impedance of the common-gate amplifier is largely resistive and g_{m1} is 20 mS, the noise factor of the common-gate stage can be obtained as

$$F = 1 + \frac{\gamma}{\alpha}, \tag{4}$$

where γ is the coefficient of channel thermal noise and α is the ratio of the transconductance and the zero-bias drain conductance [15]. γ is process-dependent and hence it is not a circuit design parameter. Then increasing g_{m1} might be an effective way to reduce the noise factor [9]. However, with the target of a $|S_{11}|$ lower than -10 dB over a broad frequency band, g_{m1} must be chosen between 10.4 mS to 38 mS ($|S_{11}|$ is -10 dB when $1/g_{m1} = 26\,\Omega$ or $1/g_{m1} = 96\,\Omega$). To make full use of the margin provided by g_{m1} to reduce the noise figure while maintaining a low biasing current, a relatively large M_1 can be used. In this design, the width of M_1 is chosen to 120 μm, such that g_{m1} is 24 mS to guarantee a $|S_{11}|$ lower than -10 dB while the DC biasing current in this stage is tightly controlled at 2.4 mA.

Different from conventional common-gate LNAs that use an inductor as the drain load of the transistor [9], a resistor, R_{D1} is used here as the load at the drain of M_1. As a result, the chip area needed for the design can be reduced. Owing to the high output impedance of the transistor, R_{D1} has insignificant impact on the input matching performance. The noise figure might be increased by doing so. But as shown by the simulated noise figure of the proposed LNA in Section 3, a noise figure of 4.3 dB can be maintained. Neglecting the loading effects from the second stage for convenient analysis, the voltage gain of the common-gate stage is derived as

$$\frac{V_a(s)}{V_{in}(s)} = (1+g_{m1}r_{o1})R_{D1}/\Bigg[\Bigg(1+\frac{R_s}{R_{L1}+sL_{s1}}+sR_sC_{gs1}+\frac{R_s(1+g_{m1}r_{o1})}{r_{o1}}\Bigg)(r_{o1}+R_{D1}+sC_{gd1}r_{o1}R_{D1}) - (1+g_{m1}r_{o1})R_{D1}R_s/r_{o1}\Bigg], \tag{5}$$

where V_a and V_{in} are the output and input voltages of the common-gate stage shown in Fig. 1, respectively. The load-

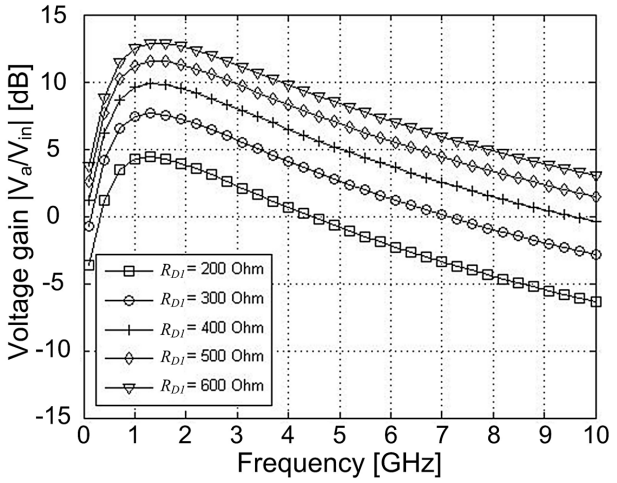

Fig. 5 Calculated voltage gain (Eq. (5)) versus frequency for the common gate stage in Fig. 1. The parameters used in this figure are: $g_{m1} = 24$ mS, $L_{s1} = 8$ nH, $R_{L_1} = 10\ \Omega$, $C_{gs1} = 200$ fF, $C_{gd1} = 150$ fF, $r_{o1} = 1$k Ω, and $R_s = 50\ \Omega$.

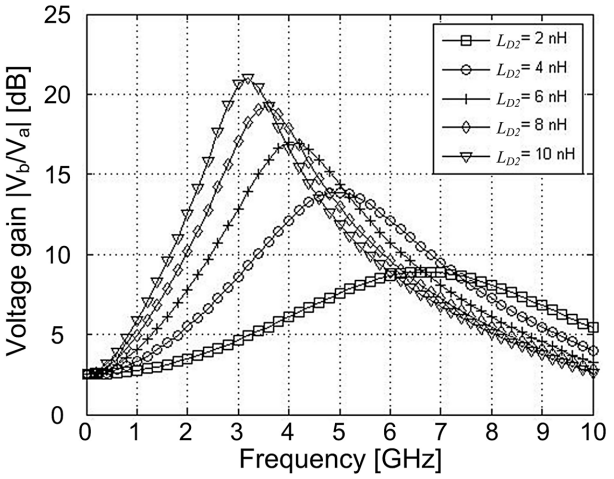

Fig. 6 Calculated voltage gain (Eq. (6)) versus frequency for the cascode stage. The parameters used in this figure are: $g_{m2} = g_{m3} = 20$ mS, $r_{o2} = r_{o3} = 1$k Ω, $R_{D_2} = 60\ \Omega$, $R_{L_2} = 10\ \Omega$, and $C_{D3} = 250$ fF.

ing effect from the next stage will be included in the SPICE simulation in Section 3.

Fig. 5 shows the calculated voltage gain of the common gate stage using Eq. (5) with five different values of R_{D1} while other parameters are kept as constants. From Fig. 5 it can be seen that R_{D1} plays a major role in determining the voltage gain, and an R_{D1} with a value of 400-600 Ω should be used to have a voltage gain of around 10 dB at 3 GHz. It should be noticed that the calculation shown here is not the power gain and the matching between the first stage and the second stage is not taken into account. But the parameter values chosen in this section provide a good starting point for the performance optimization of the complete LNA using SPICE simulations.

2.2 The cascode stage and buffer

The second stage of the UWB LNA is a cascode topology. This stage is adopted to provide gain at high frequencies. M_3 also help improve the isolation between the output and the input. L_{D2} is used for output matching. To extend the bandwidth of the cascode stage a resistor, R_{D2}, is connected in series with L_{D2} to reduce the Q factor of the inductance at the drain of M_3. In this design, the biasing current for both M_2 and M_3 is 2.6 mA to comply with the targeted power consumption of less than 10 mW. M_2 is chosen to 160 μm to optimize the matching with the first stage. M_3 is chosen relatively small, 60 μm, to reduce parasitic capacitance. The voltage gain of the cascode stage is derived as

$$\frac{V_b(s)}{V_a(s)} = \frac{-g_{m2}(1 - r_{o3}/R_N)}{1/R_N + sC_{D3} + 1/(sL_{D2} + R_{D2} + R_{L2})}, \tag{6}$$

while

$$R_N = g_{m3} r_{o2} r_{o3} + r_{o2} + r_{o3}, \tag{7}$$

where g_{m2} and g_{m3} are the transconductance of M_2 and M_3, respectively. V_b and V_a are the output and input voltages of the cascode stage shown in Fig. 1, respectively. R_{L2} is the series resistance of L_{D2}. r_{o2} and r_{o3} are the output resistances of M_2 and M_3, respectively. C_{D3} is the total capacitance at the drain of M_3. Fig. 6 shows the calculated voltage gain of the cascode stage using Eq. (6) for five different values of L_{D2} while other parameters are kept as constants. It can be seen that L_{D2} plays a major role in determining the location of the matching as well as the voltage gain, and that an L_{D2} around 4 nH should be used to have a voltage gain higher than 10 dB at 5 GHz. This gain is chosen similar to that of the common-gate stage in magnitude aiming to obtain a flat gain over the operation band. This is also the reason why a larger inductance for a higher gain is not used.

The measurement buffer is implemented as a simple source follower. It has a voltage gain of

$$\frac{V_{out}(s)}{V_b(s)} = \frac{g_{m4} R_L}{1 + g_{m4} R_L}, \tag{8}$$

where V_{out} and V_b are the output and input voltages of the buffer shown in Fig. 1, respectively. R_L is the load of the buffer, and its value is 50 Ω in this study. The width of M_4 is chosen to 60 μm to reduce parasitic effects. The DC current of M_4 is chosen to 5.5 mA, such that $1/g_{m4} \approx R_L$ and the source follower has a 6 dB loss in the output power [2].

Eq. (1) to Eq. (8) have been validated by SPICE simulations on corresponding equivalent circuits. Using the parameters previously chosen in this section, SPICE simulations on the complete UWB LNA and the buffer using device models of a standard 0.18 μm CMOS process are conducted

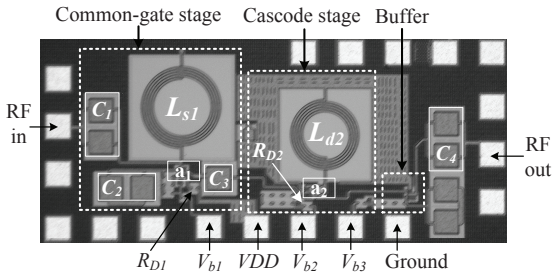

Fig. 7 The micro-photograph of the test chip. V_{b1}, V_{b2} and V_{b3} are the DC supply voltages for the biasing networks. a_1 and a_2 are the active areas of the common-gate stage and the cascode stage, respectively.

and minor modifications of the parameters are made to optimize the design to meet the desired specifications. Since the Q-values of the inductors are not critical in this case, inductors with smaller inner diameters and larger numbers of turns are used to save more areas. With a metal width of 6 μm, the inner diameter and number of turns for L_{s1} are 198 μm and 4.5, respectively. For L_{D2}, the inner diameter and number of turns are 138 μm and 4.5, respectively. The complete schematic and parameters of the designed UWB LNA with the buffer are shown in Fig. 1.

3 Test chip and measurement results

The proposed LNA has been fabricated using a standard 0.18 μm CMOS process. The entire design has a compact size of only 1.48 mm by 0.53 mm including measurement pads and on-chip DC-blocking capacitors. Fig. 7 shows the micro-photograph of the test chip. Experimental verification was carried out by on-wafer measurements.

In this design the common-gate stage and the cascode stage consume 5 mA in total, and the buffer consumes 5.5 mA at a supply voltage of 1.8 V. The simulated and measured S-parameters are shown in Fig. 8. It can be seen that the measured magnitudes of S-parameters match the simulations well. Fig. 8 also shows that the measured gain is 11-13.7 dB in 1-5 GHz. The measured $|S_{11}|$ is less than -12 dB from 1 GHz to 5 GHz, and $|S_{22}|$ is less than -10 dB from 1 GHz to 5 GHz. The deviation between the measured and simulated results of $|S_{21}|$ and $|S_{22}|$ might be caused by parasitic components. A protruding gain peak can be clearly seen at around 3 GHz, which increases the gain variance. This is due to the boost effect of the inductor at the drain of the cascode stage, indicating that a relative smaller L_{D2} should be used for a better gain variance.

The simulated and measured NFs are shown in Fig. 9 and the measured NF is 5.0-6.5 dB from 1 to 5 GHz. The deterioration of the measured NF compared with the simulated results might be a result of the series resistance introduced by interconnects and measurement pads at the input of the LNA. The relatively narrow metal interconnection

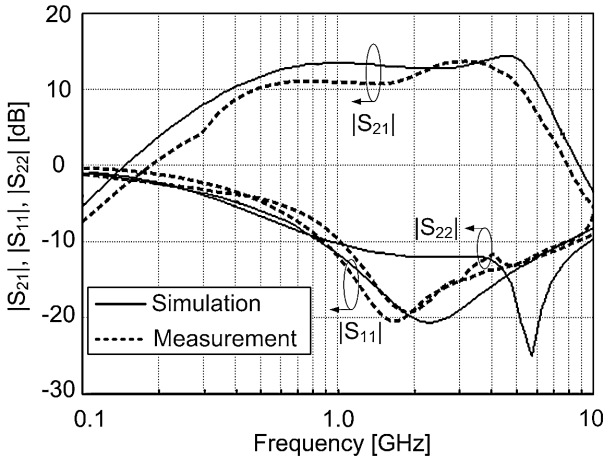

Fig. 8 Simulated and measured magnitudes of S-parameters versus frequency for the circuit in Fig. 1 using a standard 0.18 μm CMOS process.

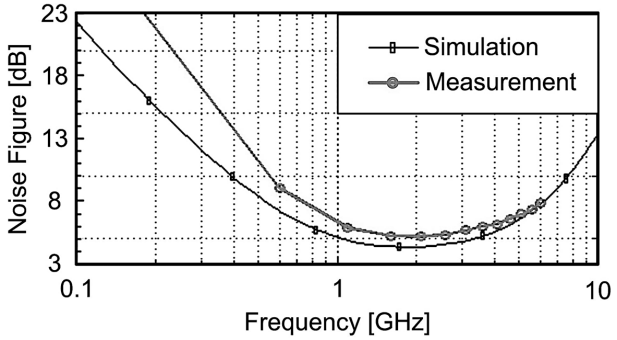

Fig. 9 Simulated and measured noise figures versus frequency for the circuit in Fig. 1 using a standard 0.18 μm CMOS process.

at the input has small capacitances but increases the series resistance. A third-order intermodulation distortion test is conducted using a 4 GHz signal and a 4.04 GHz signal. The measured IIP3 shown in Fig. 10 is -9.8 dBm and the measured 1-dB compression point is -19.5 dBm. From the measured results it is clear that the proposed LNA fulfills the desired performance described in Section 1.

Table 1 summarizes the performance of the presented UWB LNA, with comparison to previously published LNAs. The LNAs in [2–11] are based on 0.18 μm CMOS technologies, while the rest are based on deeper submicron processes. Similar to this work, buffers are used in [2, 4, 8, 10–14] for measurement purpose. For these LNAs, including this work, the performance except power consumption are measured with buffer, while the reported power consumptions do not include buffers or biasing circuits except for [4, 11]. From the comparison, it can be seen that the present UWB LNA offers the smallest physical size of only 0.78 mm^2 compared to other designs using 0.18 μm CMOS processes. It should be noticed that the chip area of this work includes all the measurement pads, on-chip DC-blocking capacitors and biasing networks. Smaller chip sizes can be

Table 1 Performance Summary of the Present UWB LNA, and Comparison with Previously Proposed UWB LNAs

Spec.	$\|S_{11}\|$	Max $\|S_{21}\|$	Band	Max NF	IIP3	Area	Power	CMOS Process	Topology
Unit	[dB]	[dB]	[GHz]	[dB]	[dBm]	[mm^2]	[mW]		
This work	<-10	13.7	1-5	6.5	-9.8	0.78	9	0.18 μm	CG+Cascode
[2]*	<-9.4	10.4	2.4-9.5	9	-8.8	1.1	9	0.18 μm	LC filter+CS
[3]**	<-20	16	0-11	6	N/A	1.44	100	0.18 μm	Distributed CS
[4]	<-9.8	18.6	3-6	5	-10.2	N/A	25.2$^+$	0.18 μm	Noncascode
[6]	<-12.19	15.91	3-6	6.7	-5	1.1	59.4	0.18 μm	Resistive feedback CS
[7]	<-10	19.7	3-5, 6-10	>7***	-12.2	1.43	24	0.18 μm	CS+CG+notch filter
[8]	<-9	9.8	2-4.6	5.2^{++}	-7	0.9	12.6	0.18 μm	Resistive feedback Cascode
[10]	<-10	13.2	3.1-10.6	6.2	-1.4	1.42	23	0.18 μm	CG+Cascode+notch filter
[11]	<-10	30	3-5	3	N/A	1.62	24$^+$	0.18 μm	Differential
[12]	<-15	19	0.5-5.6	4.3	-12	0.73	8	0.13 μm	NMOS feedback CS
[13]	<-7.5	10	3-11	3.6	9.5	0.38	2.4	0.13 μm	Single transistor CG
[13]	<-9	12.6	0.8-8.4	5.5	8.5	0.58	2.6	0.13 μm	Cascode CG
[13]	<-9	11.7	1.5-8.1	6	14.1	0.58	2.62	0.13 μm	Linearized CG
[14]	<-9.6	21.5	3.1-5	5.4	-6.4	0.24	8	65 nm	CG+CS

* TW type; ** HP mode; + With buffer; ++ At 5 GHz; *** Upper band.

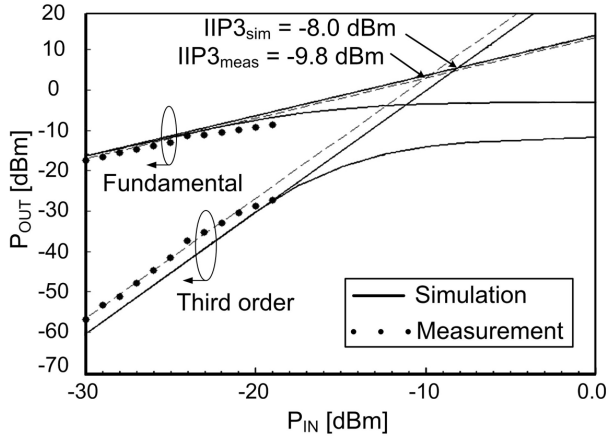

Fig. 10 Simulated and measured output power versus input power to determine the 3rd order two-tone input intercept point for the circuit in Fig. 1 using a standard 0.18 μm CMOS process. The frequencies of the two input signals are 4 GHz and 4.04 GHz, respectively.

found in [12–14]. But DC-blocking capacitors are not included in these designs. On-chip biasing circuits are not presented in [13, 14] either. This work also provides the lowest power consumption of 9 mW (the same as [2]) among the designs using 0.18 μm CMOS processes. If power consumption in the buffer is included, the LNA in this work still consumes less power (18.9 mW) than [3,4,6,7,10,11]. Apart from the advantages in the comparison on size and power consumption, it also can be seen that this work maintains a good performance in other parameters.

4 Conclusion

A two-stage UWB LNA is proposed and implemented in a standard 0.18 μm CMOS process. Theoretical analysis on the gain and matching of the LNA has been presented. The design uses only two inductors and as a result a small chip area of 0.78 mm^2 is achieved. The DC biasing current in this design is tightly controlled and the power consumption of the core LNA is only 9 mW with a 1.8 V DC supply. This is obtained by making full use of the space for performance optimization provided by circuit parameters. Apart from the size and power consumption, the LNA has a measured maximum power gain of 13.7 dB and a NF of 5.0-6.5 dB in 1-5 GHz, in which the measured $|S_{11}|$ and $|S_{22}|$ are below -12 dB and -10 dB, respectively. Compared with previously proposed UWB LNAs implemented in 0.18 μm CMOS processes, the proposed UWB LNA features low power consumption, small size and superior overall performance.

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