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Modelling of Substrate Noise and Mitigation Schemes for UWB Systems

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Chapter 7

Modeling of Substrate Noise and Mitigation Schemes for UWB Systems

Ming Shen, Jan H. Mikkelsen & Torben Larsen

7.1 Introduction

The concept of Internet of Things (IoT) has, since initially being coined back in 1999 by Kevin Ashton (1), been one of the driving factors behind much of the research and development within the area of wireless communication. From initially being thought of as formation of a link between the then-new idea of RFID and the then-explosively growing Internet, IoT has spawned into a very diverse range of wireless communication system scenarios. Examples of systems descending from IoT are Near Field Communication (NFC), Personal Area Networks (PAN), Body Area Networks (BAN), to mention but a few. On basis of shared characteristics many of these systems can be contained within the concept of Wireless Sensor Networks (WSN) as illustrated in Figure 7.1.1.
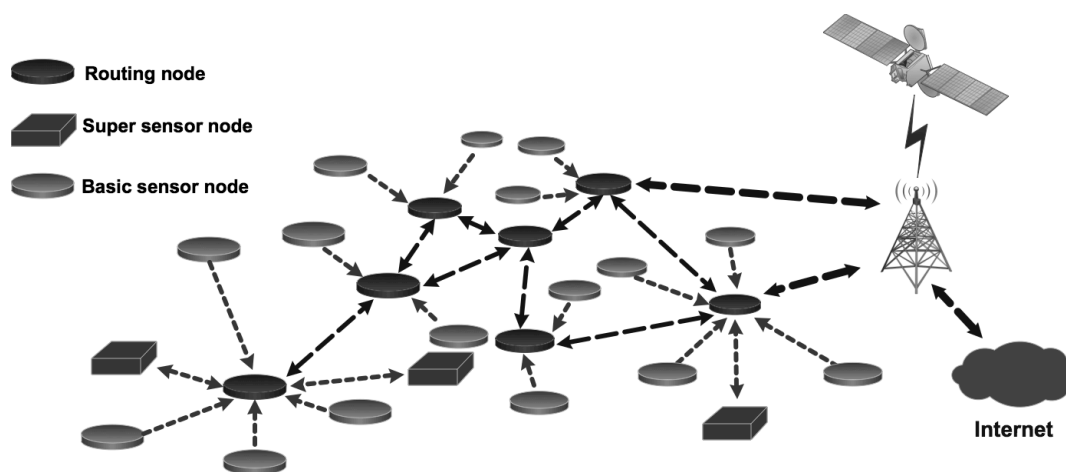
Figure 7.1.1: Overall concept of a Wireless Sensor Network (WSN).

The WSN concept plays host to an immensely broad range of applications and the revenue forecasts estimates that the WSN market is to reach 2.0 billion USD in 2021 (2). With all its diverse application areas WSN's are going to have significant impact on the ICT infrastructure and how we as humans interact with ICT systems.

One of the areas where the application of WSN based technologies is expected to have the most significant societal impact is within the health care system. It is a generally accepted fact that one of the key challenges faced by modern welfare societies relates to human health care. The increasing life expectancy of people combined with a significantly greater prevalence of chronic illnesses causes health expenses to increase with age, which places tremendous demands on the health system. One way to reduce cost is to use home health care scenarios for some of the more tedious tasks, such as screening and monitoring of people. In many cases specific patient groups, especially disposed to certain deceases, such as cancer, are being monitored. To meet these challenges it is necessary to develop new technologies that can reduce the cost burden of the health care system. One example of a costly monitoring procedure is the screening of women for breast cancer. Second only to lung cancer, breast cancer is the most frequent form of cancer among women. It has been estimated that in the year 2000 there was a total of 350.000 new cases of breast cancer in Europe. This number amounted to more than 25% of all new cancer cases in Europa in 2000. In addition it is estimated that breast cancer is responsible for more than 17% of all cancer related deaths across Europe. It would clearly be of great societal value with a cost effective monitoring scheme that could provide an early detection of tumors that potentially could develop into breast cancer. Existing scanning systems, such as X-ray and MR, both require huge setups and involve powerful magnetic fields and/or dangerous radiation. In addition, running such systems require trained staff, which adds to the operational expenses.

Scanning systems based on Ultra Wide Band (UWB) technologies have recently been applied in experimental setups aiming at detection of breast tumors, knee tissue tears and build-up of water/fluids in the body. Owing to its wide frequency range UWB systems provide for very fine temporal resolution, which offers unique detection capabilities. UWB systems are ideal for miniaturization making a whole new range of non-invasive medical applications possible. In addition UWB makes use of non-ionized electromagnetic waves, which at the envisioned power levels are harmless to the human body. From a medical point of view UWB-based detection technologies offer features that are ideal for home health care implementation. Consequently UWB-based systems potentially could become one of the absolute key technologies in leveraging the burden of the health care systems.

7.1.1 Ultra Wide Band Systems – Developments and Challenges

During past years the semiconductor industry has continued its impressive progress. This development, which is largely driven by market demands for more powerful functionality at lower cost has resulted in a device density that still obeys to Moore's law, which states that the transistor density of integrated circuits doubles every 2 years (3). This continued technology scaling has enabled the integration of more and more functionalities on a single chip. However, as the complexity of the systems increases so does the challenge of designing the required mixed-signal system-on-chips (SoCs). One of the more severe challenges relates to disturbances caused by substrate noise. Since SoCs integrate sensitive analog/RF circuits on the same die as high-speed digital processing circuits, the switching noise produced by the digital circuits can

easily propagate through substrate and power supply rails to the analog/RF circuits, degrading their performance.

The design issues related to substrate noise are expected to become even more challenging in the future. The reason behind this is twofold; i) the trend is towards more and more digital functionality in the systems which inevitably will generate more noise, and ii) to meet the ever increasing need for higher data rates wireless systems have to turn to more bandwidth efficient transmission schemes which inevitably increases sensitivity towards noise.

Considering UWB-based systems, then due to the ultra-wideband nature of such systems combined with a very low power spectral density of the signal, the impact of substrate noise on UWB circuits is expected to be more detrimental than narrow band circuits. To overcome these problems, the substrate noise has to be characterized and subsequently efficient strategies for cancellation/suppression have to be developed.

7.1.2 Switching Noise – Origin and Coupling Mechanisms

In trying to understand the substrate noise generation and injection mechanisms of integrated circuits it is quite informative to first consider a single CMOS inverter. When implemented using a lightly doped CMOS process the coupling and injection mechanisms of the basic inverter are as illustrated in Fig. 7.1.2. These mechanisms include; (1) power/ground contacts to bulk coupling,

(2) source/drain to bulk capacitive coupling and (3) impact ionization. A lumped element circuit model describing the electrical characteristics of the substrate is also given in the figure.
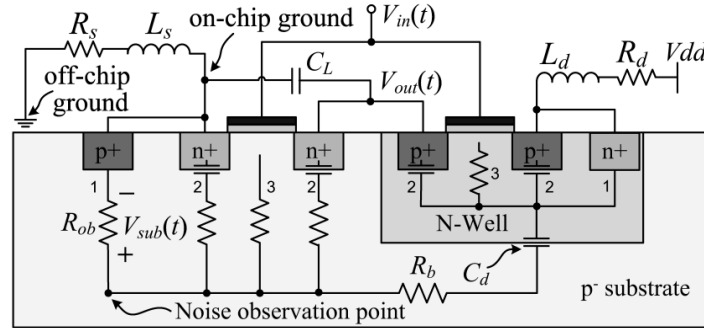

Figure 7.1.2: Cross-section view of a CMOS inverter stage and the equivalent circuit of the coupling mechanisms of the substrate noise.

Unlike heavily doped substrates, where the substrate can be treated as a single node, lightly doped bulk substrates have to be modeled using a resistive network representation (4-6). The N-well is, however, still modeled as a single node owing to its comparatively higher conductivity than the bulk. Among the coupling mechanisms shown in Fig. 7.1.2, the couplings through the power supply and ground contacts - the n+ node of the PMOS and the p+ node of the NMOS respectively - dominate the injection effects (4,7).

Apart from just revealing the basic underlying noise generation and coupling mechanisms the inverter is also quite instrumental in describing the noise behavior of large-scale digital designs. Most digital blocks include large-sized inverter stages to act as output buffers. During switching the comparatively larger buffer circuits are likely to dominate the switching noise contribution. Moreover, with many digital blocks integrated on the same die, there is a higher probability for

these inverters to switch simultaneously. All of these switching noise contributions are injected either into the substrate or propagate via interconnects. Fig. 7.1.3 illustrates how the switching noise may couple from the digital blocks to the sensitive analog/RF circuits.
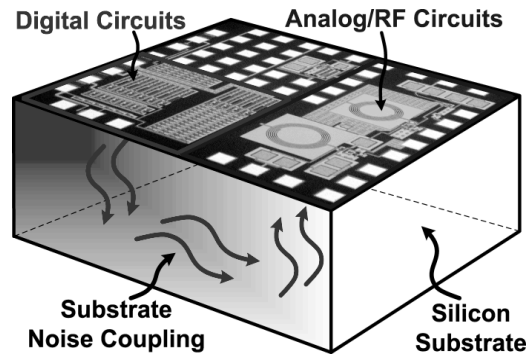
Figure 7.1.3: Illustration of the coupling mechanisms of substrate noise from digital block to sensitive analog/RF circuits.

As analog/RF circuits share the same die and in some cases even the same on-chip ground, the substrate noise can couple from areas with digital circuits either via the substrate or via the power rails to reach and disturb analog/RF circuits. The coupled substrate noise could therefore lead to a significant performance deterioration of the analog/RF circuit, such as degraded noise figures of low noise amplifiers.

To mitigate the effects of switching noise in mixed-signal integrated ultra wide band systems it is therefore highly important to study substrate noise related issues in circuits and to come up with suitable mitigation solutions for those issues. To reach this goal a number of tasks need to be accomplished: (1) impact evaluation, (2) modeling and (3) suppression of substrate noise.

7.2 Impact evaluation of substrate noise

For the previously reported work on the effects of substrate noise on analog/RF integrated circuits, almost all of them are focusing on narrow band applications (6,8,9). It has not been fully investigated if substrate noise is a severe issue for wide band systems. It is also unclear how the substrate noise affects the wide band sensitive circuits. This section experimentally investigates the features of substrate noise in a wide frequency band from DC to 10 GHz, and attempts to evaluate the impact of substrate noise on the performance of wide band RF circuits. The vehicle used for the investigation is a 1-5 GHz low-noise amplifier (LNA) for UWB systems (10).

7.2.1 Experimental impact evaluation on an UWB LNA

The schematic used for the experiment is shown in Fig. 7.2.1. It consists of a digital block, a substrate noise detector array and an UWB LNA. The digital block plays the role of a substrate noise generator. The substrate noise detector array is used in the experiment for substrate noise measurements. The UWB LNA is used as a victim circuit for the experiment.
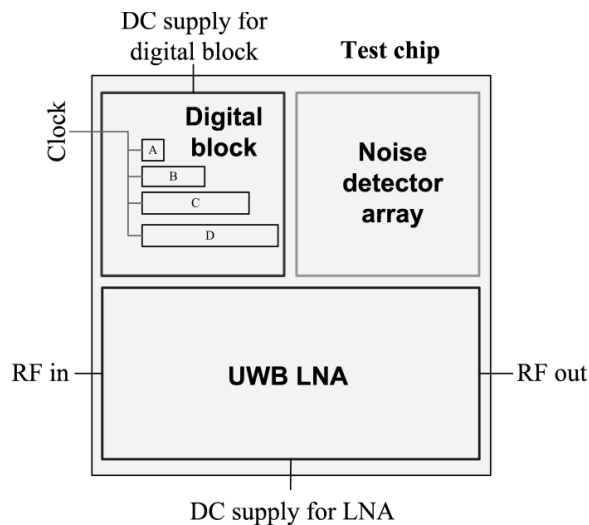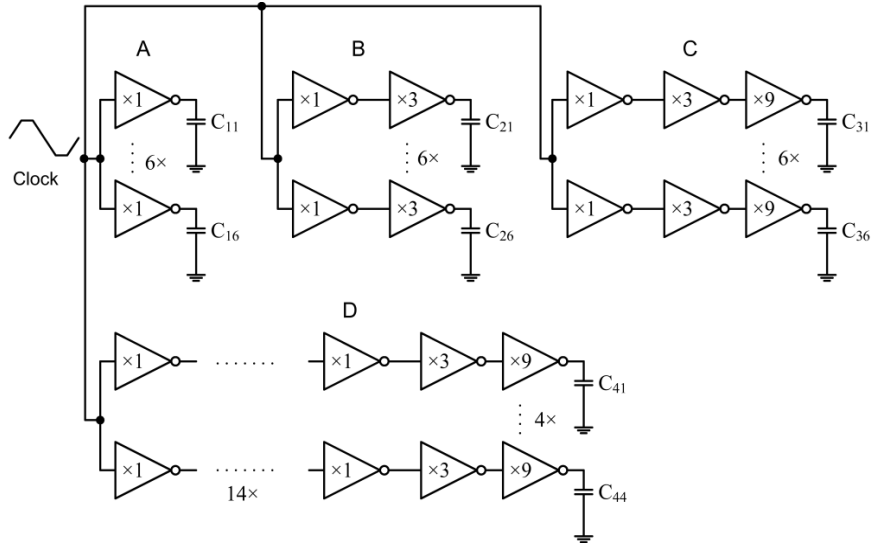

Figure 7.2.1: The schematic of the integrated circuit for the experiment.

The detailed schematic of the digital block consisting of four buffer chains is shown in Fig. 7.2.2. The buffer chain A contains six one-stage inverters.

Figure 7.2.2: The schematic of the digital block consisting of four buffer chains for the generation of switching noise.

The width/length ratios of the NMOS and PMOS transistors of each inverter are 25 μm/0.18 μm and 50 μm/0.18 μm, respectively. The buffer chain B, C and D are multistage buffer chains with different stage numbers and sizing factors shown in Fig. 7.2.2. C_{ij} represents the parasitic capacitance at the output of each buffer chain.

Fig 7.2.3 shows the schematic of the UWB LNA. It is a 1-5 GHz two-stage single ended amplifier with a source follower buffer for measurement purpose. In previously reported work, the study of substrate noise above 1 GHz is rare. For that reason the lower bound of the operation band in this design is set to 1 GHz aiming to obtain more results. This is done while maintaining the desired performance in the UWB band of 3-5 GHz.
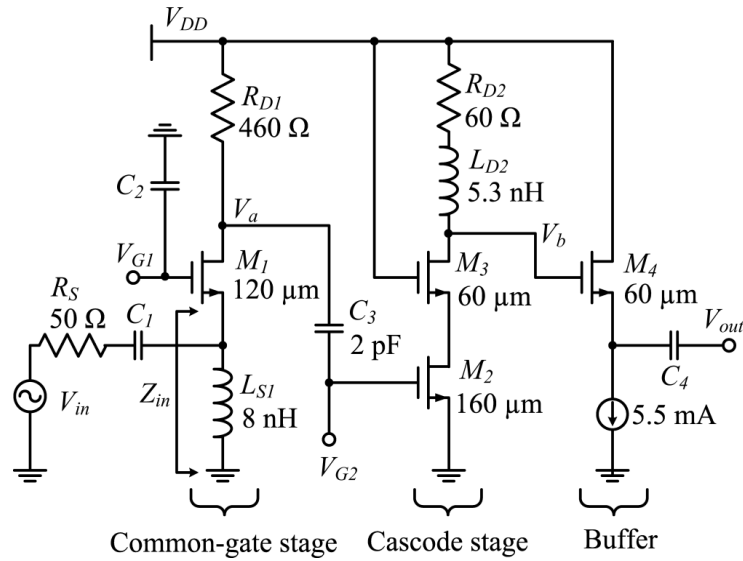
Figure 7.2.3: The schematic of the UWB LNA for noise impact evaluation.

7.2.1.1 Test chip

The fabricated test chip is shown in Fig. 7.2.4, and the PCB with the bonded chip for the measurements is shown in Fig. 7.2.5.
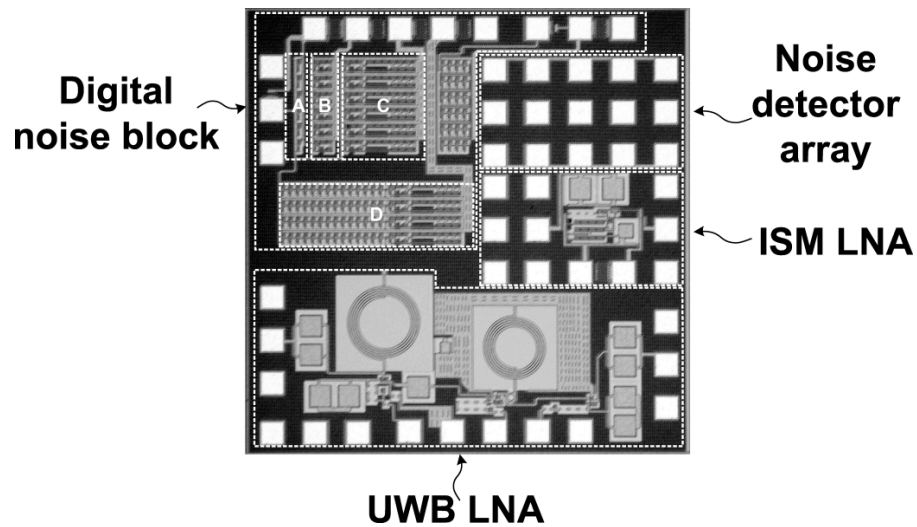
Figure 7.2.4: The microphotograph of the test chip.
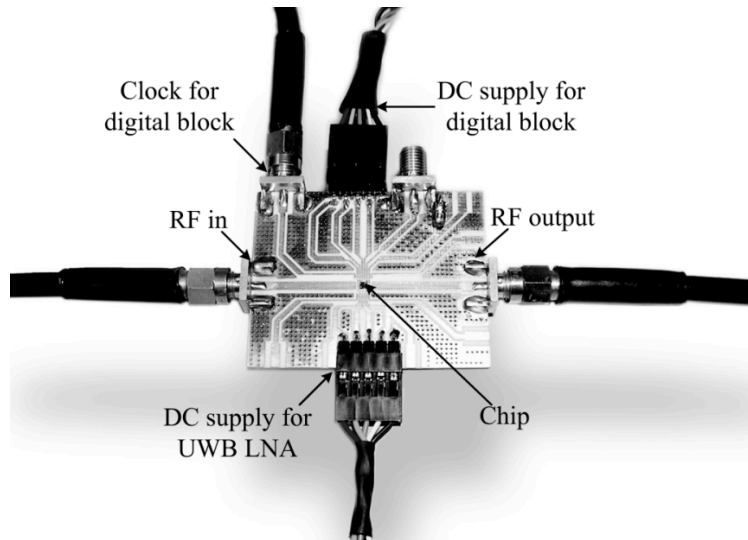
Figure 7.2.5: The PCB with the bonded chip for the measurements.

7.2.1.2 UWB LNA

The UWB LNA is measured to make sure that it has a proper overall performance. The common-gate stage and the cascode stage consume 5 mA in total at a supply voltage of 1.8 V. The simulated and measured S-parameters are shown in Fig. 7.2.6.
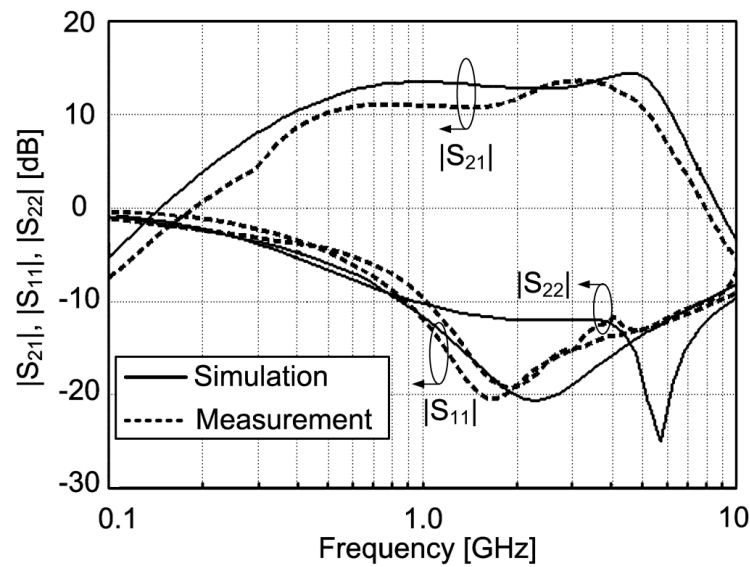
Figure 7.2.6: Measured and simulated S parameters versus frequency of the UWB LNA.

It can be seen that the measured gain is 11-13.7 dB, the measured $|S_{11}|$ is less than -12 dB and the measured $|S_{22}|$ is less than -10 dB in the frequency band of 1-5 GHz. The simulated and measured noise figures are shown in Fig. 7.2.7 and the measured NF is 5.0-6.5 dB in 1-5 GHz. It can be seen that this UWB LNA has fairly good overall performance.

Figure 7.2.7: Measured and simulated noise figure versus frequency of the UWB LNA.

7.2.2 Results and discussion

In the experiment, square waves from a function generator Agilent 33250a are used as the clock to drive the digital block. The substrate noise due to the switching noise generated by th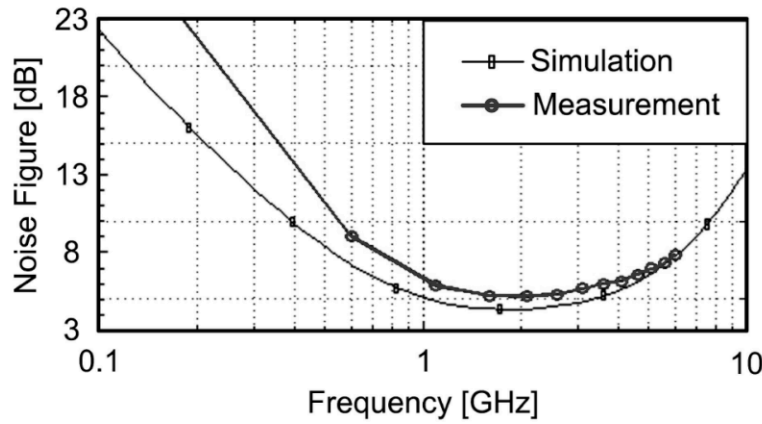e digital block is measured at the noise detector array as shown in Fig. 7.2.8(a). It can be seen that the major part of the substrate noise is located in the frequency band from DC to 2 GHz. But there are also noise tones in the frequency band up to 10 GHz with magnitudes about 10 dB higher than the noise floor. The spectrum of the RF output of the LNA is also measured with the LNA turned on. In this case the LNA is fed with a sinusoidal input of -50 dBm at 3.88 GHz and the resulting spectrum is illustrated in Fig. 7.2.8(b).
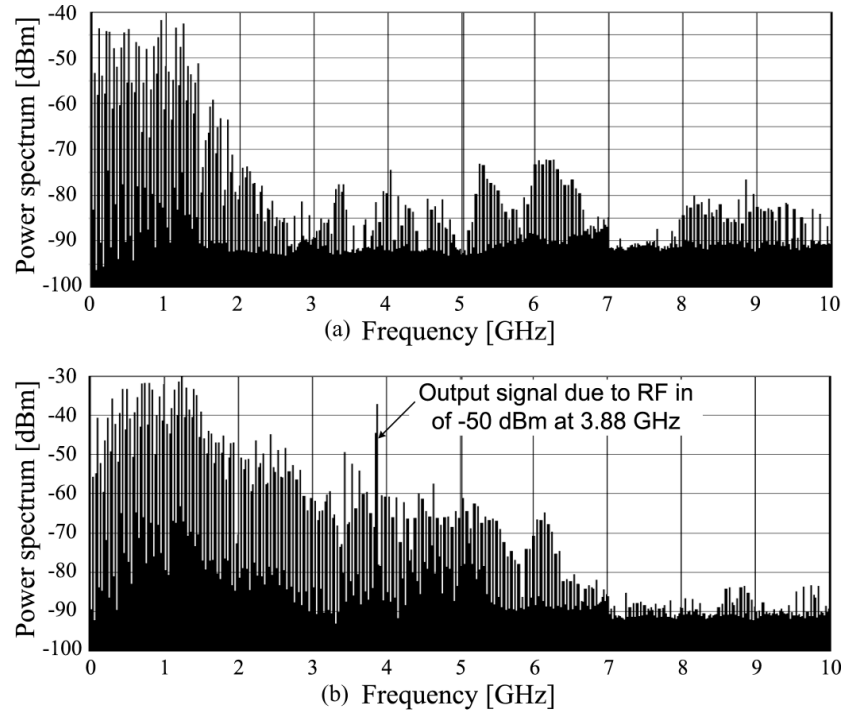
Figure 7.2.8: Measured power spectrum (a) from the substrate noise detector and (b) from RF out of the UWB LNA. f_{clock} is 50 MHz and the rising and falling time of the clock is 5 ns.

It is clear that the magnitudes of the substrate noise in 2-5 GHz are much higher than those measured at the noise detector. This indicates that the in band substrate noise coupled at the input of the LNA has been amplified by the LNA. In practical applications the magnitude of the received UWB signal could be significantly lower than the magnitude of the substrate noise as the allocated EIRP of an UWB signal is lower than -41.3 dBm/MHz (11). The effects of the clock frequency on the substrate noise is investigated by measuring the spectrum at the RF out of the LNA, while varying the frequency of the digital clock. The measured results are shown in Fig. 7.2.9, zoomed in into the frequency band of 3.5-4.5 GHz for more detailed information. It can be seen that the magnitude of the substrate noise is increased when f_{clock} is increased from 10 MHz to 50 MHz. This is due to the fact that the digital circuit switches faster (generates and injects

more switching noise) with a higher clock frequency. This effect will be discussed with more detail in the subsequent subsection.
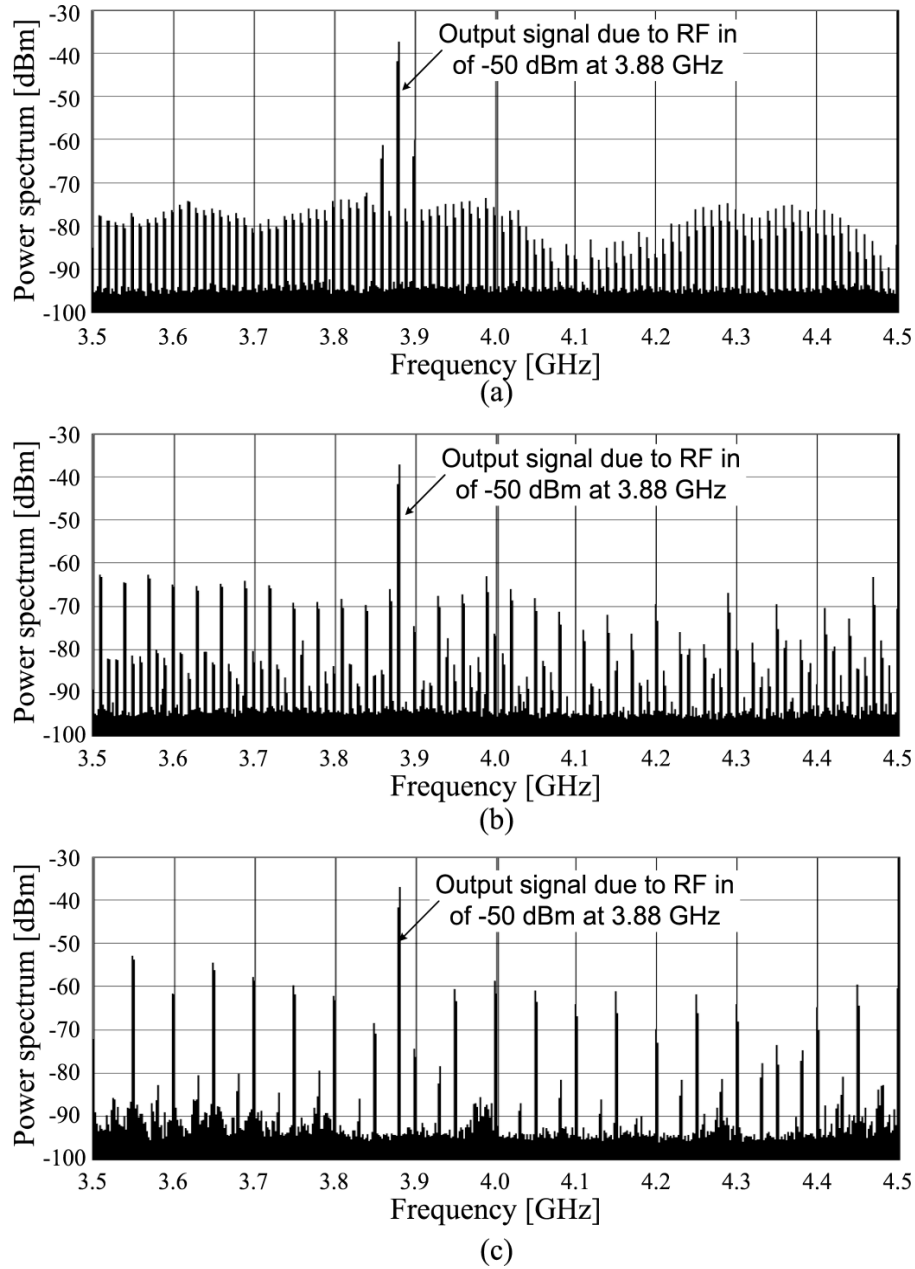
Figure 7.2.9: Measured power spectrum from RF out of the UWB LNA, while the digital block is driven with three different clock frequencies. The parameters for the clock are: (a) f_{clock}=10 MHz, (b) f_{clock}=30 MHz, (c) f_{clock}=50 MHz. The rising and falling times of the clocks are 5 ns for all of the three cases.

Apart from the original harmonics of the substrate noise, it can be seen in Fig. 7.2.9 that some extra frequency components are also present. These components are caused by the intermodulation between the RF input signal and the substrate noise at the fundamental and higher order harmonics. To confirm this, the intermodulation components with two different RF input frequencies are measured and marked by circle symbols shown in Fig. 7.2.10. It can be seen that the noises at the harmonics of f_{clock} remain with insignificant changes, while the noise components due to intermodulation shift along with the RF input signal.
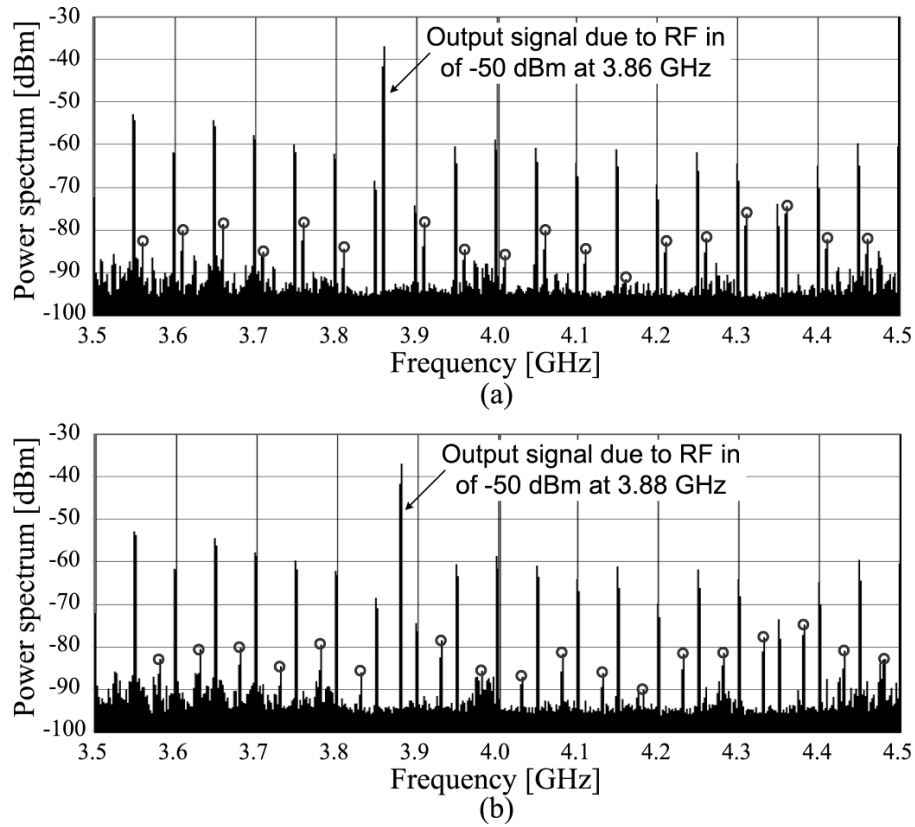
Figure 7.2.10: Measured power spectrum from RF out of the UWB LNA with two different RF input frequencies. The parameters for the RF input signal are: (a) f_{RF} =3.86 GHz, (b) f_{RF} =3.88 GHz. The magnitude of the RF input signal is -50 dBm. f_{clock} is 50 MHz and the rising and falling time of the clock is 5 ns. The circle symbols mark the intermodulation components.

The impact of the substrate noise on the UWB LNA is studied by comparing the measured noise figure of the LNA when the digital block is turned off and turned on with three different values of f_{clock}. The measured results are shown in Fig. 7.2.11.
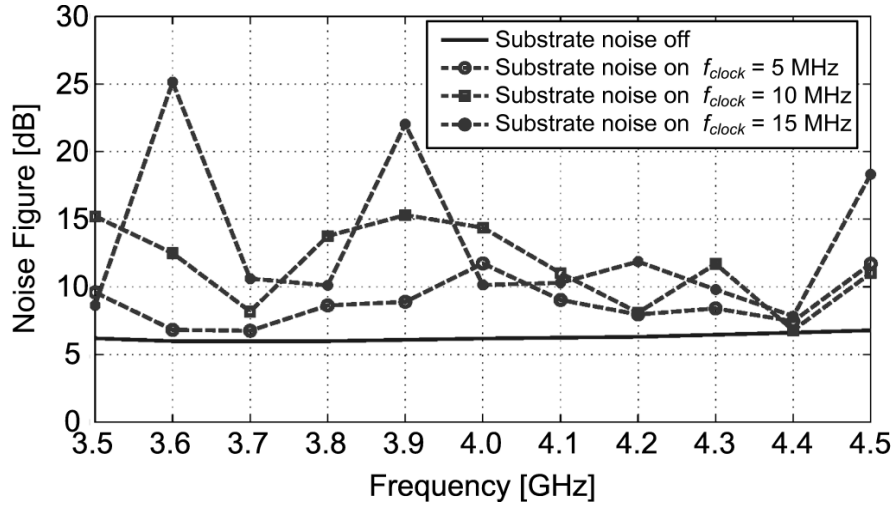
Figure 7.2.11: Measured noise figure versus frequency of the UWB LNA when the digital block is turned off and turned on with three different values of f_{clock}.

It can be seen that the LNA has a smooth and flat noise figure around 6 dB in the measured frequency band when the digital block is turned off. When the digital block is turned on, significant deterioration of the noise figure is seen. It also can be seen that the deterioration is stronger for higher f_{clock}, which is consistent with the results shown in Fig. 7.2.9.

7.2.3 Conclusion

In this section, the impact of substrate noise on UWB LNA is experimentally evaluated. Significant substrate noise is observed in the frequency band of DC to 10 GHz. It is shown by the results that the substrate noise can drastically deteriorate the performance of the UWB LNA in terms of noise figure. The results clearly indicate the need for a good understanding of the

generation and propagation of the substrate noise, as well as the need of effective approaches for reducing the substrate noise in the design of wide band mixed-signal ICs.

7.3 Analytical Modeling of Switching Noise in Lightly Doped Substrate

7.3.1 Introduction

Switching noise produced in digital circuits has gradually become one of the most important concerns in IC design due to increasingly higher density of digital design. The root cause here being the need for more and more digital functionalities combined with tight requirements for area in mixed signal integrated circuits. As illustrated in Fig. 7.3.1, the switching noise generated by digital circuits can propagate through the substrate to reach sensitive analog/RF circuits and deteriorate their performance.
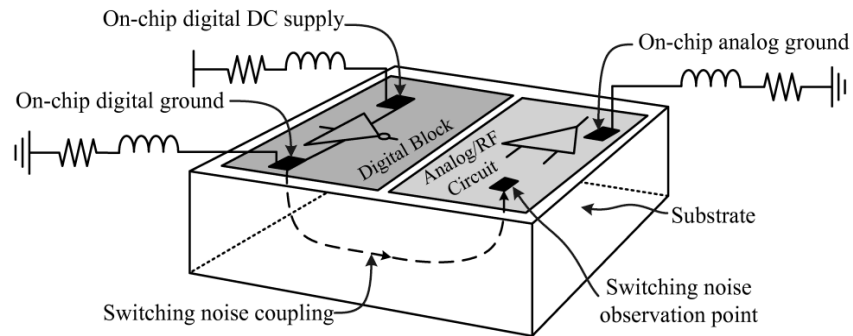
Figure 7.3.1: Switching noise coupling mechanism in mixed-signal circuits.

A number of methods have been proposed for achieving an efficient model that is able to capture the main features of the switching noise (4-7,12-18). For heavily doped substrates the substrate is simplified as one electrical node due to their low resistivity, and switching noise modeling methods using this simplification have been proposed (13,14). Featuring higher resistivity and

better noise isolation properties, lightly doped substrates are widely used in mixed-signal designs (7,12,15). Since the resistivity of lightly doped substrates is much higher than that of heavily doped substrates, the substrate can no longer be treated as a single electrical node. Hence, modeling methods applicable for heavily doped substrate fall short when lightly doped substrates are considered.

Conventional approaches to characterize switching noise in lightly doped substrate are typically highly dependent on SPICE simulations. One example is the computationally extensive approach where digital circuit blocks are simulated directly together with an extracted substrate network (4,5). While this approach may lead to accurate results it involves lengthy and time-consuming simulations. Therefore, in an attempt to reduce simulation complexity the use of macro models has been proposed (6,7,12,15,16). Here the switching current from digital blocks is typically represented using an asymmetrical triangular waveform which, when combined with a lumped element equivalent network representing the substrate, allows for fast generation of SPICE simulations results. Both of the above approaches rely heavily on simulations but despite providing for accurate results neither offer sufficient insight into switching noise generation and propagation.

A slightly different approach is to make use of analytical methods where, based on mathematical analysis of waveform functions characterizing the switching current and a transfer function model of the switching noise propagation, closed-form expressions for the switching noise can be derived (18,19). While this method provides more insight into the propagation of switching noise the switching current source still needs to be characterized through SPICE simulations.

Further, layout extractions are still needed to identify the resistances needed to derive the noise propagation transfer function.

To avoid the need for layout extractions the use of compact models to characterize the spreading resistance between arbitrary sized diffusion contacts on lightly doped substrates has been proposed (19). By doing so the transfer function describing the propagation of the switching noise can be determined without the need for cumbersome layout extractions. The combination of such a compact model of the propagation transfer function and an analytic closed-form expression for the switching noise would provide the mixed-signal designer with a very powerful noise estimation tool and allow for proper measures to be taken early in the design flow. Such a tool would clearly be advantageous, however, at current a feasible analytical model characterizing the switching current source is still unavailable.

This section presents two modeling methods aiming to provide feasible models for the switching noise of simple digital circuits and large-scale digital blocks, respectively. The switching noise generated by individual inverters is analytically investigated. An analytical model, named the GAP model is proposed to characterize the switching noise of individual inverters. The model is validated by both SPICE simulations and measured results obtained from a test chip fabricated in a lightly doped CMOS process. The simulated and measured results are in good agreement with the proposed model. The GAP model is suitable only for simple circuits and to extend its usability to include large-scale circuits also, the GAP model is complimented by a statistical analysis method. The extended method is verified by SPICE simulation results.

7.3.2 The GAP Model

The reason for focusing on the analysis of individual inverters is based on two facts:

a) The inverter is a basic and often used building block in digital circuits.

b) A typical large scale digital circuit usually contains big size inverters that act as buffers. Due to the large sizes, these inverters generate significant switching noise, and therefore usually dominate the total generation of the switching noise in the digital circuit (17).

Thus, analyzing the switching noise in an individual inverter is considered a good starting point for obtaining detailed understanding of the generation and injection of switching noise. The proposed model approximates the switching current using a Gaussian pulse (GAP) function. The key parameters in the model are derived by solving the differential equation describing the output voltage of a capacitively loaded inverter. Combining the switching current model and the transfer function, which models the propagation of the switching current, the spectrum of the switching noise can be predicted.
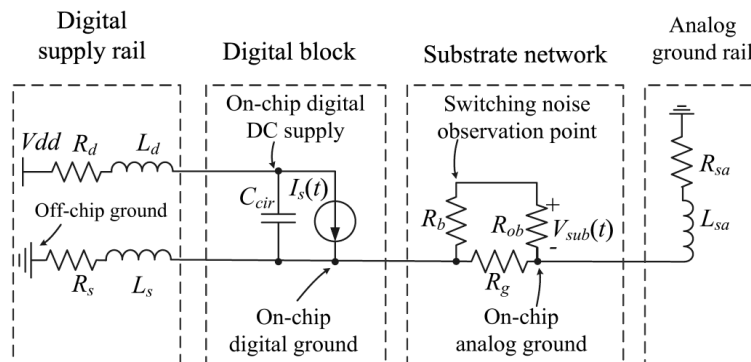
Figure 7.3.2: The switching noise coupling network.

The simplified switching noise coupling mechanisms involved in Fig. 7.3.1 are illustrated by four blocks in Fig. 7.3.2. The digital supply rail block and the digital block in Fig. 7.3.2 are

similar in structure to the coupling network used in (6). In the digital block, $I_s(t)$ represents the switching current generated by the digital block. C_{cir} is the circuit capacitance between the on-chip digital DC supply and the on-chip digital ground. The substrate network block and the analog ground rail block are used to model the switching noise coupling to analog circuits. R_d and L_d are the resistance and inductance of the bonding wire and interconnect connecting the on/off-chip digital DC supply, respectively. R_s, R_{sa}, L_s and L_{sa} are the resistances and inductances of the interconnects and bonding wires connecting the off-chip ground to the on-chip digital and analog ground, respectively. R_g is the resistance between the on-chip digital and analog grounds. R_{ob} is the substrate resistor between the noise observation point and the on-chip analog ground. R_b is used to model the spreading resistance between the on-chip digital ground and the observation point on the substrate. Based on Fig. 7.3.2 the resulting noise voltage at the observation point can be derived as

$$V_{sub}(j\omega) = H(j\omega) \cdot I_s(j\omega) = \frac{R_g R_{ob} Z_L I_s(j\omega)}{(j\omega C_{cir}(\frac{Z_L Z_{ea}}{Z_L + Z_{ea}} + Z_D) + 1)(Z_{ea} + Z_L)(R_b + R_{ob} + R_g)}, \quad (7.3.1)$$

where $Z_D = R_d + j\omega L_d$, $Z_L = R_s + j\omega L_s$ and $Z_{ea} = R_{sa} + R_g(R_d + R_{ob})/(R_g + R_d + R_{ob}) + j\omega L_{sa}$. How to find the parameters in the transfer function $H(j\omega)$, has been provided in previous studies (6,18). The remaining challenge is to find a scalable analytical model for I_s.

7.3.2.1 The switching current of individual inverters

A typical schematic of a capacitively loaded inverter is shown in Fig. 7.3.3(a).
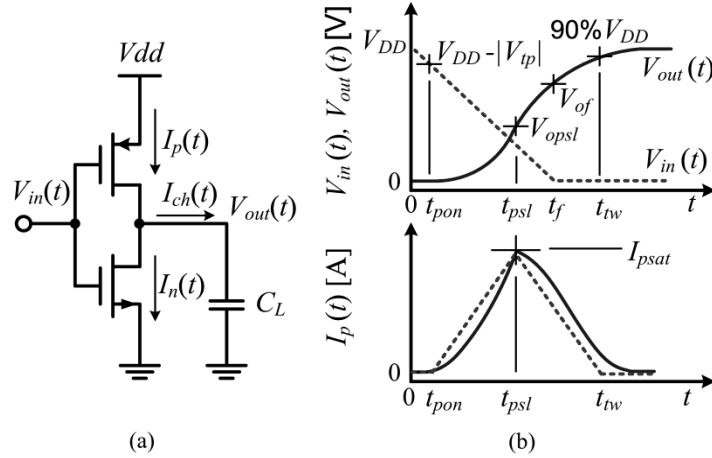
Figure 7.3.3: (a) The schematic of a capacitively loaded inverter, and (b) the input/output voltage (dash/solid line in the top figure) and switching current (bottom figure) of a falling input transient.

Here, $I_p(t)$ is the drain current of the PMOS device, $I_n(t)$ is the drain current of the NMOS device and $I_{ch}(t)$ is the charging/discharging current. The input voltage (dash line) and output voltage (solid line) in a falling input transient of the inverter are shown in the top figure of Fig. 7.3.3(b). As V_{in} falls, the PMOS is turned on at time t_{pon}, and the capacitor load is charged towards a higher voltage. When $V_{out}(t)$ reaches V_{opsl} at t_{psl} and $V_{out}(t_{psl}) - V_{in}(t_{psl}) = |V_{tp}|$, where V_{tp} is the threshold voltage, the PMOS leaves the saturation region and enters the linear region. V_{of} is defined as the output voltage at the falling time t_f. The time when the output reaches 90% of the final value is defined as t_{tw}. The switching current I_p during the transient is shown by the solid line at the bottom of Fig. 7.3.3(b). A number of modeling approaches of the output response and switching currents in CMOS inverters have been reported (20,21). However, to derive the expression of the switching current is no trivial task, and no comprehensive

expressions for the switching current have been presented. To simplify the analysis task, a triangular waveform is often used to model the switching current as shown by the dash line in the bottom figure in Fig. 7.3.3(b) (18). The triangular model has a peak value of of I_{psat} at t_{psl}, and its magnitude is zero at $t \le t_{pon}$ and $t \ge t_{tw}$. This model is simple and accurate for estimating the Power Spectral Density (PSD) of the switching noise at low frequencies. However, this approach leads to significant estimation errors at high frequencies due to the abrupt simplifications of the switching current (6,18). Moreover, the expressions of the key parameters such as t_{psl} and t_{tw} are not provided. In this study, Gaussian pulse equations are used to model the switching currents. The resulting GAP model is thus described by the following equation

$$
I_p(t) = \begin{cases}
I_{psat} \times \exp\left[\dfrac{-2\pi(t - t_{psl})^2}{(1.45 \times (t_{psl} - t_{pon}))^2}\right] & \text{for } 0 \le t \le t_{psl} \\[4mm]
I_{psat} \times \exp\left[\dfrac{-2\pi(t - t_{psl})^2}{(2.0 \times (t_{tw} - t_{psl}))^2}\right] & \text{for } t > t_{psl},
\end{cases}
\qquad (7.3.2)
$$

The GAP model has the same peak current value as the triangular model at t_{psl}, and its magnitude is 10% and 20% of I_{psat} at t_{pon} and t_{tw}, respectively. Compared with the triangular model, the GAP model has smoother transitions at the peak and bottom of the waveform. As a result, the GAP model produces less predicting errors at high frequencies. The expressions of the parameters in the GAP model are derived in the following part of this section. The expressions also can be used in the conventional triangular model.

In this analysis, the short circuit current during switching transients is neglected. This approximation is based on the fact that the charging/discharging currents contribute the major part of the switching current for capacitively loaded inverters in most of the present CMOS

processes (20-22). Under this assumption, the NMOS and PMOS are assumed off during a falling input transient and a rising input transient, respectively, and $I_s(t)$ only consists of $I_p(t)$ generated at the falling input transient. The discharging current generated at the rising input transient is flowing in the closed loop formed by the NMOS and C_L. Thus it has no contribution to $I_s(t)$ and is consequently neglected. Moreover, the analysis in this study is based on the well-known Square-law MOSFET model. This simplification is necessary since higher-order models are intractable for analytical manipulation. But, as shall be seen in the measurement section, the results derived based on the simple model are sufficiently accurate. In the Square-law model the transistor drain current is expressed as

$$I_D = K_p\left[(V_{gs} - V_t)V_{DS} - \frac{V_{DS}^2}{2}\right]V_{DS} < V_{Dsat} \qquad (7.3.3)$$

$$I_D = \frac{1}{2}K_p(V_{gs} - V_t)^2 V_{DS} \geq V_{Dsat}; \qquad (7.3.4)$$

where $V_{Dsat} = V_{GS} - V_t$, $K_p = \mu C_{ox}\dfrac{W}{L}$, and V_{DS}, V_{GS} are the drain-source, gate-source voltage respectively. For reasons of concise and general expressions, corresponding lowercase letters are used to denote voltages normalized by V_{DD} in the following analysis. For example, $v_{out}(t) = V_{out}(t)/V_{DD}$. The input voltage waveform is approximated to be a falling ramp with a falling time t_f and a slope $s_f = -1/t_f$

$$v_{in}(t) = \begin{cases} s_f \times (t - t_f) & for\ 0 \leq t \leq t_f \\ 0 & for\ t > t_f. \end{cases} \qquad (7.3.5)$$

This approximation is widely used due to its simplicity and effectiveness (20,21). With this t_{psl} and t_{tw} can be derived based on the expression of the output voltage, which can be found by solving the following differential equation

$$C_L \frac{dV_{out}(t)}{dt} = I_p(t), \qquad (7.3.6)$$

where $I_p(t)$ can be replaced by Eq. (7.3.3) or (7.3.4) with corresponding terminal voltages. Categorizing the falling input transient as two cases that $v_{opsl} < v_{of}$ (slow input ramp) or $v_{opsl} \geq v_{of}$ (fast input ramp), the expressions for those parameters for each case are given as

Case A: $v_{opsl} < v_{of}$

$$t_{psl} = (v_{opsl} + p)/s_f, \qquad (7.3.7)$$

where $p = V_{tp}/V_{DD}$, and v_{opsl} can be found by solving the equation

$$v_{opsl} = \frac{K_p V_{DD}}{6 s_f C_L} (v_{opsl} - 1)^3. \qquad (7.3.8)$$

Furthermore, t_{tw} can be formed by

$$t_{tw} = t_f + \Big[\ln((2(1+p) - 0.1)/0.1) -$$

$$\ln\left(\frac{2p + 1 + v_{of}}{1 - v_{of}}\right)\Big] C_L /(K_p V_{DD}(1+p)), \qquad (7.3.9)$$

where v_{of} can be determined from

$$v_{of}(t) = 1 - \exp\left(\frac{K_p V_{DD}(-1-p)^2}{2s_f C_L}\right) \Bigg/ \left[\frac{\exp\left(\frac{K_p V_{DD} v_{opsl}^2}{2s_f C_L}\right)}{v_{opsl}}\right.$$

$$\left. + \sqrt{\frac{K_p V_{DD}\pi}{8s_f C_L}} erf\left(\sqrt{\frac{K_p V_{DD} v_{opsl}^2}{2s_f C_L}}, \sqrt{\frac{K_p V_{DD}(-1-p)^2}{2s_f C_L}}\right)\right]. \tag{7.3.10}$$

Case B: $v_{opsl} \geq v_{of}$

$$t_{psl} = t_f - \frac{2pC_L}{K_p V_{DD}(1+p)^2} + \frac{1+p}{3s_f}, \tag{7.3.11}$$

$$t_{tw} = t_{psl} + \frac{ln\left[(2(1+p)-0.1)/0.1\right]C_L}{K_p V_{DD}(1+p)}. \tag{7.3.12}$$

In addition, it is easy to derive that $I_{psat} = K_p(s_f t_{psl} + v_t)^2/2$, and $t_{pon} = v_{tp}/s_f$. Since the remaining parameters in Eq. (7.3.2) are given by Eq. (7.3.7) to (7.3.12), the expressions for all parameters needed in the models are available.

7.3.2.2 Validation of the model

The proposed GAP model is verified by comparing its predictions with HSPICE simulations on the schematic in Fig. 7.3.3(a). A 0.18 *μm* CMOS process with 0.34 *μm* option is used for the verification. Successful verifications with different capacitive loads, transistor sizes and falling times have been conducted. For the verification shown here, the widths of the PMOS and the NMOS are 0.68 *μm* and 0.34 *μm* respectively, and both of them have the same length of 0.34 *μm*. The HSPICE model used in the verification is level 49. The related parameters are:

$K_p = 4.75 \times 10^{-5}$, $V_{tp} = -0.66\,\text{V}$, $V_{DD} = 3.3\,\text{V}$ and $t_f = 5\,\text{ns}$. To evaluate the model in both the case

A and case B scenarios, C_L is set as 0.3 and 1 pF respectively. It should be noted that Eq. (7.3.7)

to (7.3.12) are functions of the term $K_p V_{DD} / C_L$, which means that the inverters having the same

V_t, input voltages and $K_p V_{DD} / C_L$ generate switching currents with the same t_{pon}, t_{psl} and t_{tw}.

Thus the example shown here represents a group of general scenarios. The simulated and

modeled results for case A and case B are shown in Fig. 7.3.4 and Fig. 7.3.5, respectively.
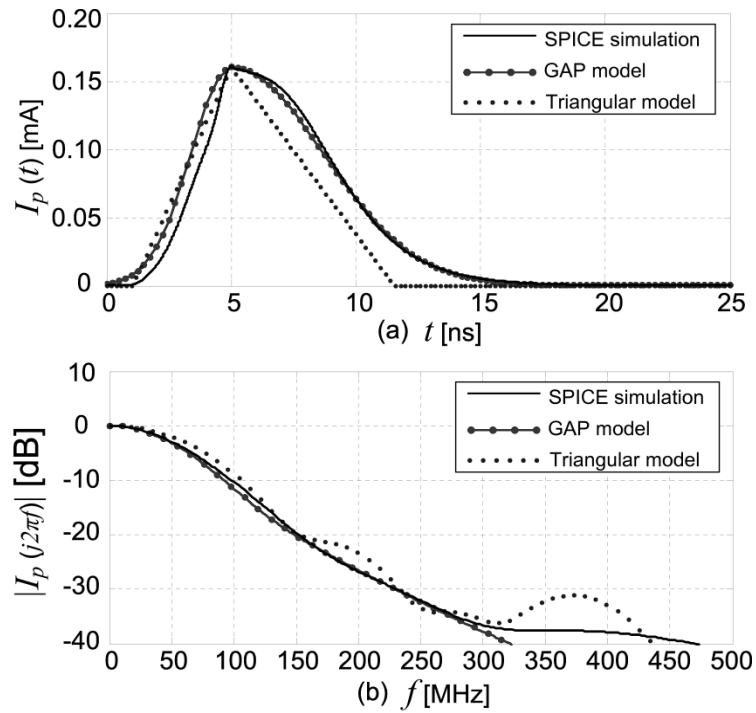
Figure 7.3.4: Modeled and simulated results for the capacitively loaded (C_L = 0.3 pF) inverter in

Case A. (a) time domain, (b) frequency domain.
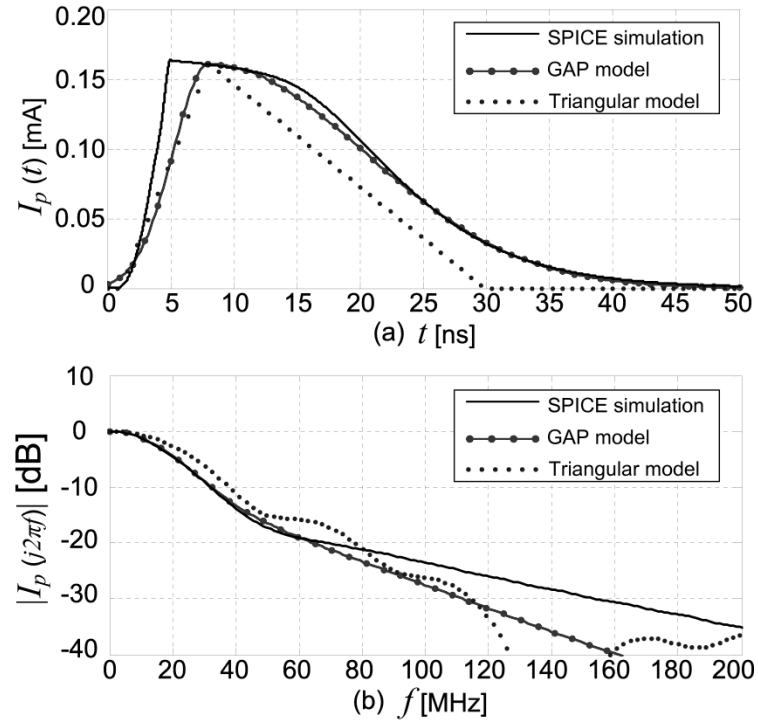
Figure 7.3.5: Case B: (a) The modeled and simulated switching current of the individual inverter in time domain, and (b) frequency domain. $C_L = 1$ pF in this case.

The normalized Fourier transforms of the switching currents are also shown. It can be seen that both the triangular model and the GAP model match the simulation results well at low frequencies, and it is obvious that the estimation errors at high frequencies are clearly reduced in the GAP model as expected.

7.3.2.3 Test chip

To experimentally validate the proposed model, the model has been practically applied to predict the switching noise generated by a capacitively loaded inverter implemented using a lightly doped CMOS process (20 Ω-cm). The microphotograph of the test chip is shown in Fig. 7.3.6.

The PMOS and NMOS devices in the inverter are 600 μm and 300 μm wide respectively, and both transistors have the same length of 0.34 μm. The reason for using such fairly large transistors is to generate enough switching noise to enable measurements. In this case, $K_p = 0.04$, and $V_{tp} = -0.7$ V. A 20 pF capacitor is connected to the output of the inverter as a load. In the measurement, the inverter is driven using an periodic square wave signal as $V_{in}(t)$. It has a high and a low voltage level of 3.3 V and 0 V, and it is fed using a G-S-G probe connected to a signal generator. The DC supply voltage is 3.3 V, and it is fed to the on-chip digital supply and ground using DC probes. When the inverter is switching due to the square wave, the switching noise in the test chip is measured at the noise observation point using a G-S-G probe connected to a spectrum analyzer. The observation point is an ohmic contact connected to the substrate (23).

During the measurements, the spectrum analyzer is set to have a low displayed noise floor (around -90 dBm in this case) to measure as much as possible of the low powered switching noise. Since the input signal is periodic, the switching noise is periodic as well. Thus the switching noise could be represented as a summation of harmonics in frequency domain
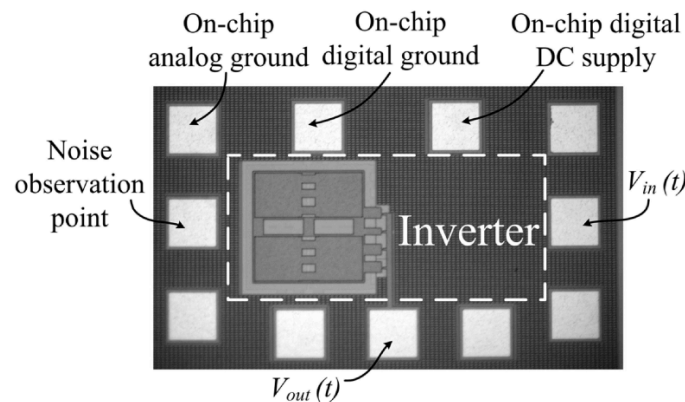
Figure 7.3.6: Microphotograph of the test chip.

$$V_{sub}(j\omega) = \sum_{k=-\infty}^{+\infty} \frac{2\pi H(j\omega)I_p(j\omega)}{T} \delta(\omega - k2\pi/T), \qquad (7.3.13)$$

where $I_p(j\omega)$ is the Fourier transform of $I_p(t)$ in Eq. (7.3.2). $H(j\omega)$ is expressed in Eq. (7.3.1) and it can be derived based on parameters extracted from the layout and bonding wires (6,18). T is the period of the input signal and k is an integer. Based on Parseval's theorem, the term

$$\left| H(jk2\pi/T)I_p(jk2\pi/T)/T \right|^2, \qquad (7.3.14)$$

is the average power of the switching noise at its k (th) harmonic. In this case, $H(j\omega)$ is simplified as a purely resistive network since the measurement is on-wafer and no bonding wires and on-chip decoupling capacitors are used. Hence $H(j\omega)/T$ only effects the magnitude of the switching noise but not the spectral envelope, which is given by the term $I_p(j\omega)$. Thus the measured PSDs of the switching noise can be compared with the calculated magnitudes of the harmonics to verify the proposed model. Measurements with different signal frequencies (from 20 to 50 MHz) and different falling times have been conducted. By comparing v_{opsl} and v_{of} obtained from Eq. (7.3.8) and (7.3.10) respectively, the GAP model of case A is applicable in this test. Thus corresponding equations of case A are used for obtaining $I_p(j\omega)$. A comparison of measurement results, the triangular model and the GAP model is shown in Fig. 7.3.7.

The harmonics with the highest magnitude of the models are normalized to the magnitude of the first harmonic of the measured switching noise. It can be seen that the GAP model matches the measured results quite well as it is within 4 dB for all measured switching noise components in the three cases. Moreover, the GAP model is more accurate than the triangular model at high frequencies. This is shown in Fig. 7.3.7(a) at the frequency of 100 MHz and Fig. 7.3.7(b) at the

frequency of 285 MHz. For higher frequencies, the switching noise drops below the noise floor of the spectrum analyzer. But the harmonics of the triangular model are higher than the noise floor at these frequencies, which also indicates larger estimation errors in the triangular model.
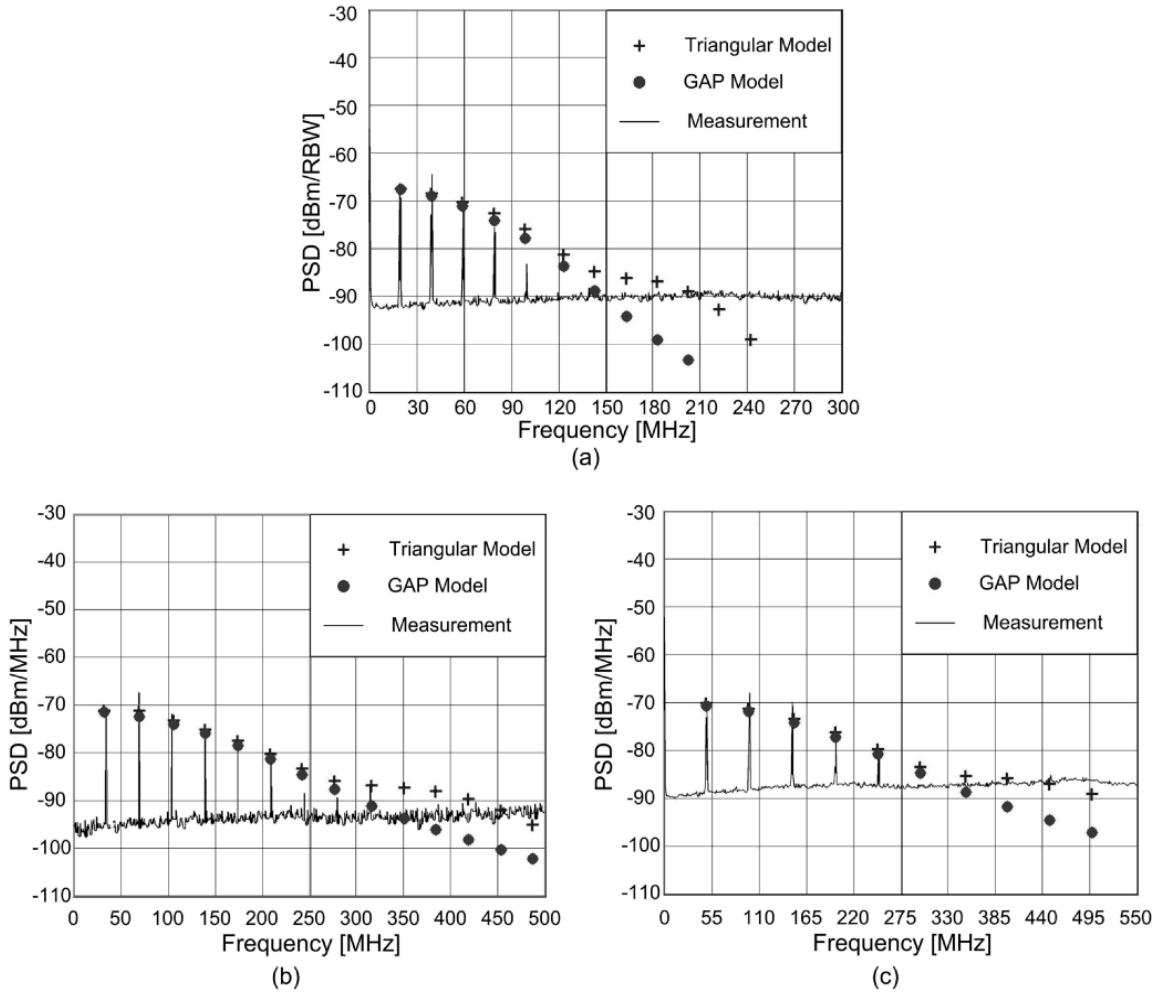

Figure 7.3.7: Measured PSDs and modeled harmonics of the switching noise. (a) f_{clk}=20 MHz, t_f=22 ns, RBW=500 kHz; (b) f_{clk}=35 MHz, t_f=9.3 ns, RBW=100 kHz; (c) f_{clk}=50 MHz, t_f=7.8 ns, RBW=1 MHz.

7.3.3 The statistic model

In large scale digital circuits, there are numerous gates switching with varying delays on the chip. For synchronized digital circuit, the switching currents are aligned at the edge of the clock with

random amplitudes and random time delays. For such a scenario the substrate noise is a sum of these signals, and can not be simply modeled by a periodic current pulse as shown in Fig. 7.3.8.
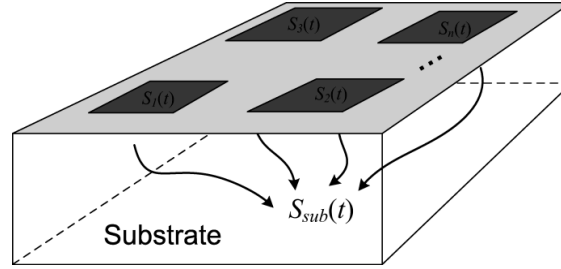
Figure 7.3.8: Coupling mechanism of switching noise in large scale digital blocks.

A statistic model is proposed to solve the problem. This model is based on the assumption that all switching current sources can be represented by a common pulse function yet with random magnitudes and random time delays. This assumption is based on the fact that identically sized inverters are widely used in large scale digital blocks. And the driving signal and load condition for these inverters are usually similar as well. Hence the switching currents generated by these inverters are expected to be similar to each other. Based on the assumption, the noise coupling mechanism shown in Fig. 7.3.9(a) in large scale digital blocks can be approximated as a multi-path coupling model with single noise source as shown in Fig. 7.3.9(b). In the figure, $S_u(t)$ is the mean of the switching noises, and $H_i(t)$ is the sub-transfer function describing the random attenuation and delay of the switching noises.
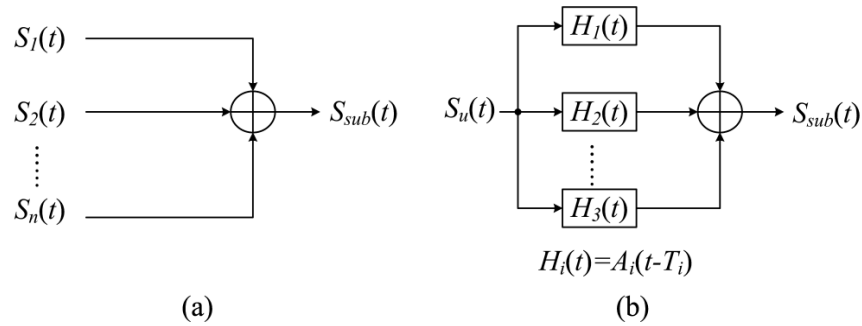
Figure 7.3.9: The (a) original switching noise and (b) the equivalent multi-path coupling model.

Using the equivalent multi-path model, the substrate noise can be expressed as $V_{sub}(f) = S_u(f) \cdot H(f)$, where $H(f)$ is the total transfer function of the coupling. $H(f)$ is the Fourier transform of the impulse response $h(t)$ of the noise coupling model shown in Fig. 7.3.9(b). $h(t)$ can be expressed as

$$h(t) = \sum_{i=0}^{N} A_i \delta(t - T_i), \quad\quad (7.3.15)$$

where A_i and T_i represent the amplitude and the time delay of the i(th) impulse, respectively. N is the number of the noise sources. Thus

$$H(f) = \sum_{i=0}^{N} A_i \exp(-j2\pi f T_i). \quad\quad (7.3.16)$$

The illustrations of $h(t)$ and $H(f)$ are shown in Fig. 7.3.10(a) and Fig. 7.3.10(b), respectively.


(a)   (b)
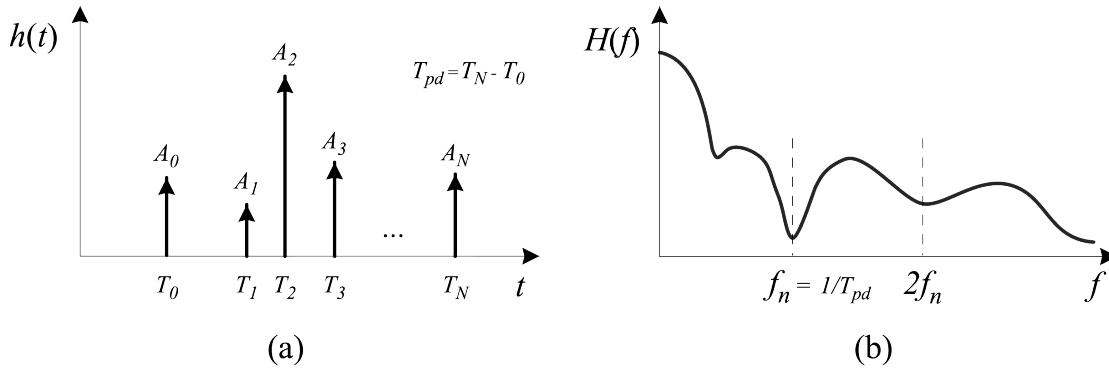
Figure 7.3.10: (a) Impulse response function of the equivalent multipath noise coupling model, and (b) the coupling transfer function.

Due to the time delay, $H(f)$ typically features high magnitudes at lower frequencies and remarkably lower magnitudes at frequency f_n and its multiples. It is easy to derive that

$f_n = 1/T_{pd}$ where T_{pd} is the time delay between the last and the first impulse. This means that the frequency band $(<f_n)$ with the most server substrate noise can be denoted by only one parameter T_{pd}. Comparing f_n with the frequency band where the sensitive analog/RF circuits work, it can be estimated if the sensitive circuits are working in the most noisy frequency band, which is useful information for IC designers. In practical digital designs T_{pd} can be approximated by the maximal propagation delay of the circuits, and usually it can be easily obtained by compact equations or SPICE simulations (no extracted substrate network is needed, which is different from conventional simulation methods).

The equivalent multi-path model is verified by SPICE simulation. An inverter chain block shown in Fig. 7.3.11 is used for the simulation. A 0.18 μm CMOS process is used. Minimum width and length are used for all the NMOS in the inverters. PMOS in all the inverters is twice bigger than the corresponding NMOS. C_{li} represents the parasitical capacitance at the output of the inverters. Fig. 7.3.12 shows the PSD of the switching noise in the inverter chain block. The simulated maximal propagation delay T_{pd} is 216 ps, and the calculated notch location is 4.6 GHz. It can be seen that the calculated notch location is consistent with the simulation results.
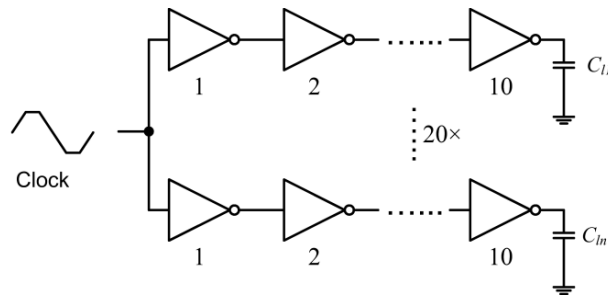
Figure 7.3.11: The schematic of the inverter chain block for the simulation of switching noise.
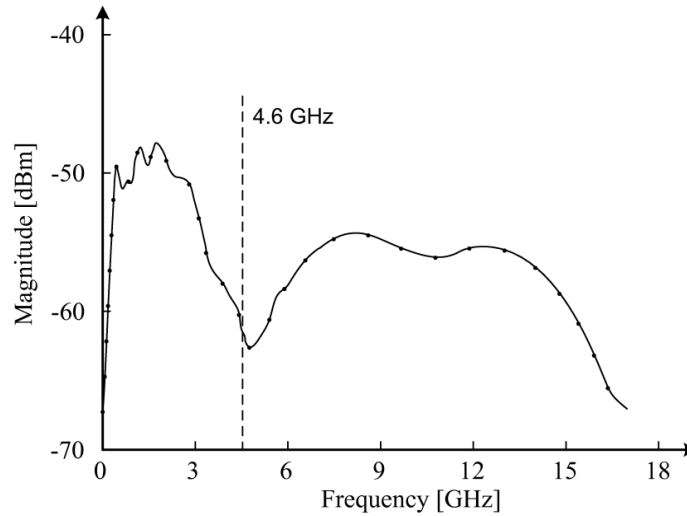
Figure 7.3.12: Simulated PSD of the switching noise generated by the circuit in Fig. 7.3.11.

7.3.4 Conclusion

This section presents two modeling methods for switching noise in both small and large scale digital circuits. The novel analytical model for simple digital circuit provides a detailed understanding of the generation and propagation of switching noise in lightly doped CMOS technologies. The spectral envelope of the switching noise can be easily predicted using the proposed model. Closed-form expressions for calculating the parameters in the conventional triangular model are also provided. The model is validated by both SPICE simulations and measurement results from a test chip fabricated in a lightly doped CMOS process. Good agreement is found between the model and simulations as well as measurement results. With this model, the simulations needed when using traditional approaches can be avoided. This can help to achieve a scalable analytical switching noise model for digital blocks. This model especially holds the advantage for estimating the switching noise when big size buffers are dominating the noise generation. Besides, an equivalent multi-path coupling model is proposed to characterize the switching noise in large scale synchronized digital circuits.

7.4 Substrate Noise Suppression and Isolation for UWB Systems

7.4.1 Introduction

Various methods have been proposed over time for the isolation and suppression of the substrate noise in mixed-signal ICs (24-27). These methods can generally be divided into two categories. One is passive approaches, including physical separation, guard rings or deep N wells. The passive methods are practically feasible. However, they usually suffer the drawbacks of area consuming, uncertainty of the isolation level and high cost. The other method is active cancelation. Active cancelation is proposed to achieve low cost yet effective substrate noise suppression. The basic idea in this method is to cancel the substrate noise at the RF area by injecting an anti-phase signal produced by an active cancelation circuit. As shown in Fig. 7.4.1, $V_{sno}(t)$ is the original substrate noise generated by the digital circuits. $V_{snc}(t)$ is the signal generated by the active cancelation section, and $V_{snt}(t)$ is the total substrate noise beneath the RF circuit. If $V_{snc}(t) = -V_{sno}(t)$ at a location, $V_{sno}(t)$ can be totally canceled and $V_{snt}(t)$ is reduced to zero at such location. However, the result is not as expected. Due to the fact that the signal propagation in the substrate noise is layout dependent, the location where $V_{snt}(t)$ can be reduced is significantly based on the specific layout. If the layout is not properly designed, the substrate noise could be increased other than reduced. This degrades the feasibility of the method. In addition, owing to the limited frequency band of the active cancelation circuit, this method is only feasible for low frequency substrate noise suppressions.
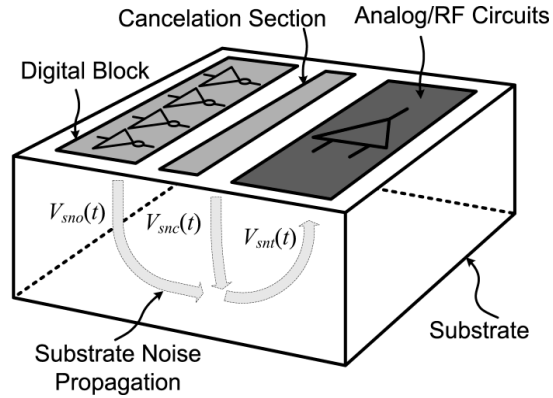
Figure 7.4.1: The propagation mechanism of the substrate noise from the digital block to the analog/RF block, and the illustration of the proposed active suppression technique.

This section presents a novel active suppression technique for substrate noise in mixed-signal ICs. In the proposed active suppression technique, an active spectrum shaping section is used to generate extra switching currents to modify the shape of the original switching noise in both time domain and frequency domain.

The relative time delays of these switching currents to the original switching current are realized by controllable delay lines. The pulse widths and magnitudes of the switching currents are also controllable. By manipulating the extra switching currents, the spectrum of the total switching noise can be shaped to have a suppressed magnitude at desired frequencies. This section is organized as follows. Subsection 7.4.2 presents the active suppression technique for reducing of substrate noise generated by digital circuits.

7.4.2 Active suppression of switching noise in mixed-signal integrated circuits

In the presented technique, an active cancelation section is used to generate an extra switching current. This additional current is introduced with a specific time delay relative to the original

switching current. The pulse width and magnitude of the switching current are also adjustable by biasing voltages. Due to the relative time delay, the extra switching current is out-of-phase with respect to the original switching current at specific frequencies. Thus by adjusting the time delay, pulse width and magnitude of the extra switching current, the original switching current can be suppressed at desired frequencies.

Figure 7.4.2 shows the diagram of the active cancelation section and its connection with clock and DC supply. It comprises three subsections, the delay control unit (DCU), the width control unit (WCU) and the magnitude control unit (MCU). The MCU is used to generate the major part of the extra switching current, and the magnitude of the switching current can be controlled by the controlling voltage V_{mp} and V_{mn}. The DCU and the WCU are used to adjust the time delay and pulse width of the switching current, respectively. V_{dn} is for controlling the time delay, while V_{wn} and V_{wp} are for controlling the pulse width. The active cancelation section is driven by the same clock driving the digital circuit, so that the extra switching current can be aligned to the original switching current with the desired time delay.
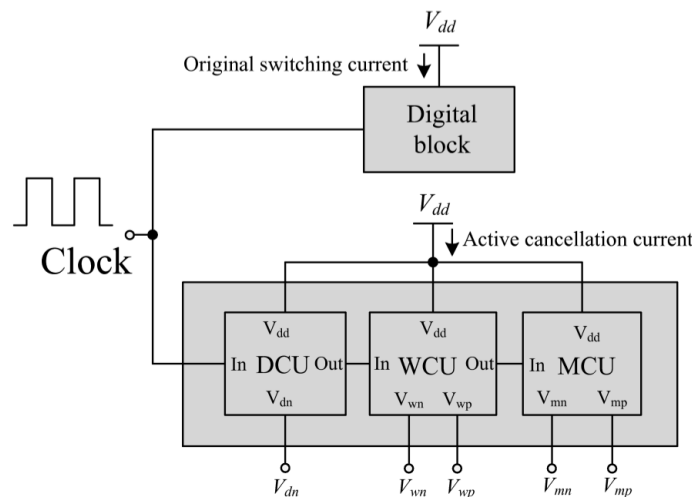
Figure 7.4.2: The circuit diagram of an active suppression circuit for the IC in Figure 7.4.1.

7.4.2.1 Theory

The switching current generated by a digital block could be represented by a triangular waveform. One of such current in a single cycle is shown as $I_{sno}(t)$ in Fig. 7.4.3 The basic idea in this invention is to inject an extra current signal $I_{snc}(t)$ to cancel $I_{sno}(t)$ in desired frequency band. $I_{snc}(t)$ has a relative delay of $T_1 - T_0$. Thus the total switching current is given as:

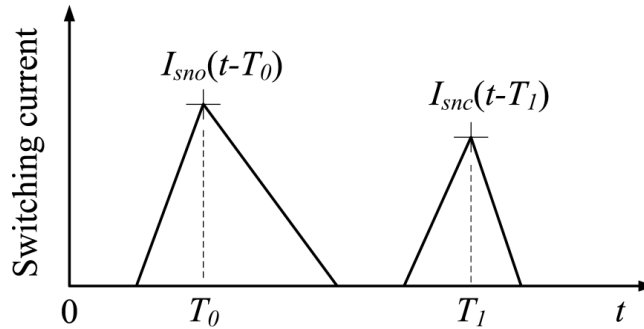$$I_t(t) = I_{sno}(t - T_0) + I_{snc}(t - T_1), \qquad (7.4.1)$$

and its Fourier transform is

$$I_t(j\omega) = I_{sno}(j\omega)e^{-j\omega T_0} + I_{snc}(j\omega)e^{-j\omega T_1}, \qquad (7.4.2)$$

where $I_{sno}(j\omega)$ and $I_{snc}(j\omega)$ are the Fourier transform of $I_{sno}(t)$ and $I_{snc}(t)$, respectively. $I_t(j\omega)$ can be further written as:

$$I_t(j\omega) = e^{-j\omega T_0}[I_{sno}(j\omega) + I_{snc}(j\omega)e^{-j\omega(T_1 - T_0)}]. \qquad (7.4.3)$$

Figure 7.4.3: Illustration of switching currents involved in the proposed suppression method. The original switching current, I_{sno}, is combined with a cancellation current, I_{snc}, to achieve suppression.

At the desired substrate noise suppression frequency

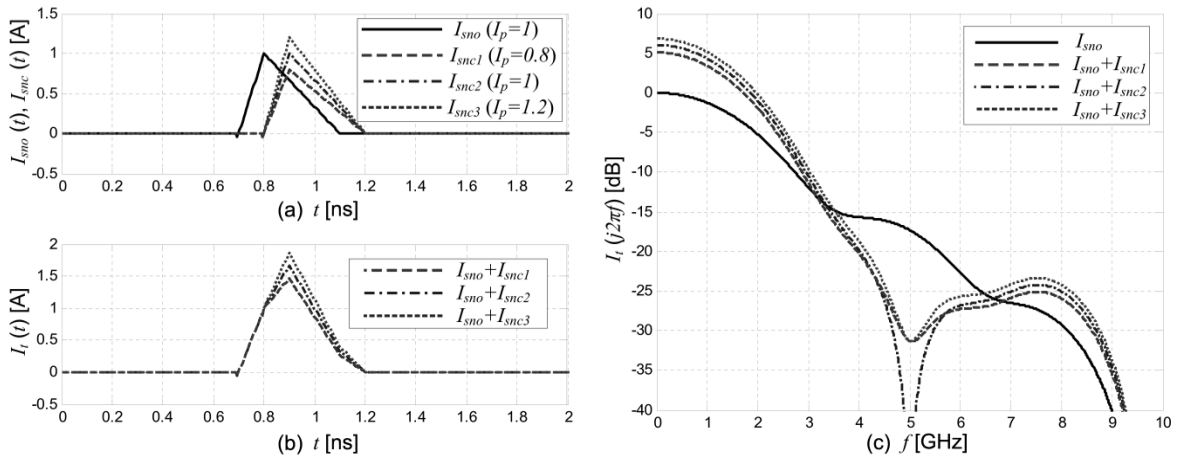$$\omega_0 = (2k+1)\pi / (T_1 - T_0), \quad for \ k = 0, 1, 2... \tag{7.4.4}$$

it has

$$| I_t(j\omega_0) | = | I_{sno}(j\omega_0) - I_{snc}(j\omega_0) |. \tag{7.4.5}$$

Thus if $I_{snc}(j\omega_0)$ has similar magnitude and pulse width as $I_{sno}(j\omega_0)$, I_{sno} could be significantly suppressed at ω_0.

7.4.2.2 Validation of the method in Matlab

The proposed method has been validated by Matlab simulations. One of the simulations is shown in Fig. 7.4.4.
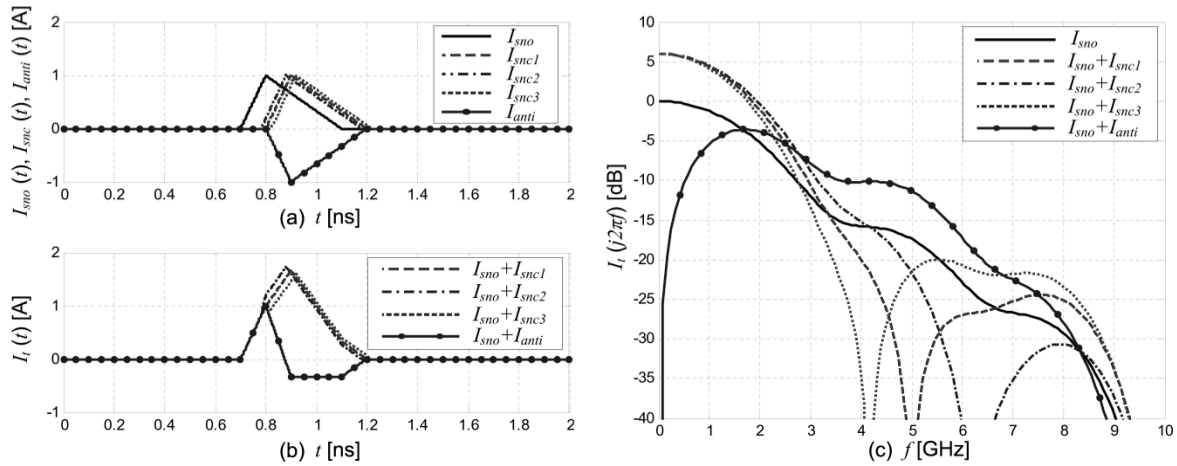

Figure 7.4.4: Simulated results of the suppression of substrate noise using cancelation currents with three different magnitudes.

The original switching current $I_{sno}(t)$ is shown by the solid line in Fig. 7.4.4(a). It has a rising time of 100 ps and a falling time of 300 ps. Its magnitude is normalized to 1 A. The active

cancelation current $I_{snc}(t)$ with three different magnitudes are also shown in Fig. 7.4.4(a). The active cancelation currents have the same rising and falling time as the original current. In this simulation, the desired suppression frequency is at 5 GHz. Thus the relative delay between $I_{snc}(t)$ and $I_{sno}(t)$ is set as 100 ps. Fig. 7.4.4(b) and Fig. 7.4.4(c) show the total switching current with three different cancelation currents in time domain and frequency domain, respectively. It is clear that the original switching current is significantly suppressed at the desired frequency. The -10 dB suppression band is wider than 500 MHz for all the three cases. The scenarios with different relative delays are also studied. The simulation results are shown in Fig. 7.4.5.

Figure 7.4.5: Simulated results of the suppression of substrate noise using cancelation currents with three different relative delays. The time delay between I_{sno} and I_{snc1} to I_{snc3} are 80 ps, 100 ps and 120 ps, respectively. The time delay between I_{sno} and I_{anti} is 100 ps.

The original switching current $I_{sno}(t)$ is shown by the solid line in Fig. 7.4.5(a). It is as the same as that in Fig. 7.4.4(a). The active cancelation current $I_{snc}(t)$ with three different relative delays are also shown in Fig. 7.4.5(a). The active cancelation currents have the same magnitudes as the original current. In this simulation, the desired suppression frequency is also at 5 GHz. Thus the

desired relative delay between $I_{snc}(t)$ and $I_{sno}(t)$ is 100 ps. Fig. 7.4.5(b) and Fig. 7.4.5(c) show the total switching current with three different cancelation currents in time domain and frequency domain, respectively. The suppression of the original switching current is clear even though there are undesired offsets in the relative delay in I_{snc2} and I_{snc3}. A time-delay sensitivity demonstration of the conventional anti-phase cancelation approach with undesired time delay is also shown in Fig. 7.4.5. I_{anti} is the delayed anti-phase current to the original switching current. As the conventional anti-phase cancelation method does not control the time delay, the delay can varies drastically due to different circuit topologies, layouts and interconnects. In Fig. 7.4.5(a), the time delay of I_{anti} is set as the same as the delay of I_{snc2}. It can be seen in Fig. 7.4.5(c) that the magnitude of the total switching current is significantly but undesirably increased in the frequency band of 2-8 GHz, which indicates the poor application potential of the anti-phase method for UWB applications unless the timing can be well controlled.

7.4.2.3 Sub-blocks in the active cancelation section

There can be different circuit implementations of the three control units. The key issue to ensure is that the units must be independent of each other for feasible design and reliable performance. In the following part, some implementation examples are presented and the issue of unit dependency is discussed further.

One possible implementation of a delay control unit consists of a number of delay cells (DSs) as shown in Figure 7.4.6. By controlling the voltage V_{dn}, the propagation delay of the DCU can be adjusted to a desired value. The number of the delay cells is chosen based on the needed total

delay time and the delay that each delay cell can introduce. Small transistors should be used in the delay cells to avoid undesired generation of significant switching currents in this subsection.
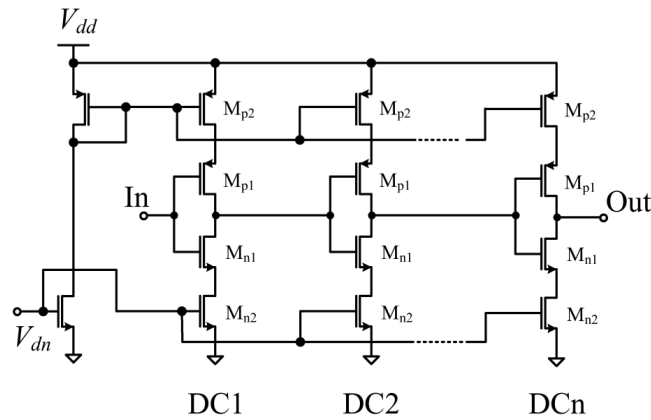
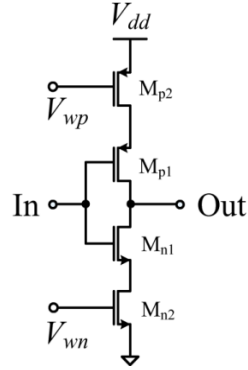**Figure 7.4.6:** Simplified circuit of the delay control unit (DCU).

Another promising DCU implementation consists of a number of inverters with tunable capacitive loads is shown in Figure 7.4.7. By controlling the voltage V_{dn}, the loads of the inverters can be changed and a desired time delay can be obtained. The number of the inverters is chosen based on the needed total time delay. Small transistors should be used in the delay cells to avoid undesired generation of significant switching currents in this subsection.
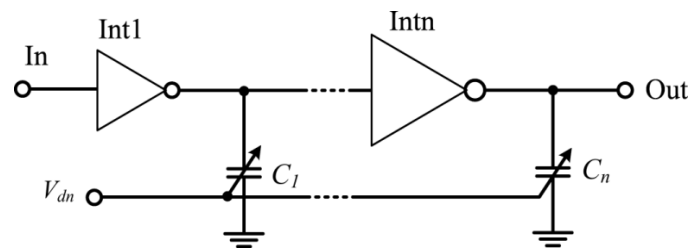
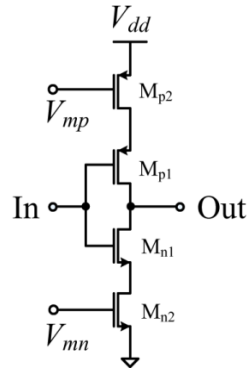**Figure 7.4.7:** Simplified circuit of the delay control unit.

A simple WCU implementation consists of one or a number of delay cells is shown in Figure 7.4.8. By controlling the voltage V_{wn} and V_{wp} the capacity of the WCU to drive the MCU can be adjusted. So that the slop of the input signal to the MCU at the falling or rising edge can be

adjusted. As a result, the pulse width of the switching current generated by the MCU can be adjusted to a desired value. The sizes of the transistors in the WCU are chosen based on the size of the MCU and the desired pulse width of the switching current.

Figure 7.4.8: Simplified circuit of the width control unit (WCU).

A simple MCU implementation is shown in Figure 7.4.9. By controlling the voltage V_{mn} and V_{mp} the magnitude of the generated switching current can be adjusted.


Figure 7.4.9: Simplified circuit of the magnitude control unit (MCU).

7.4.2.4 Validation of the method in SPICE

The proposed method is also validated by SPICE simulations. The schematic shown in Fig. 7.4.2 is used for the simulation and the schematics shown in Fig. 7.4.6, Fig. 7.4.8 and Fig. 7.4.9 are

used for the DCU, WCU and MCU blocks, respectively. The digital block is composed of a number of inverter chains, which acts as a switching noise source. The DCU, WCU and MCU are designed based on the information of the original switching current. The controlling voltages of the units are set such that the suppressed switching noise can be achieved at desired frequencies. The simulated results with and without the active suppression are shown in Fig. 7.4.10 to Fig. 7.4.12. The switching current without active cancelation is probed at the DC supply of the digital block, while the switching current with active cancelation is probed from the main DC supply for both the digital block and the active cancelation circuits. From the simulations, it can be seen that the switching noise at desired frequencies can be significantly suppressed. The minimal suppression is 10 dB observed in Fig. 7.4.10, and the best is 27 dB observed in Fig. 7.4.12. It is also clear that the proposed technique is valid for suppression the switching noise at least from 100 MHz to 3.3 GHz, which is attractive for different applications.
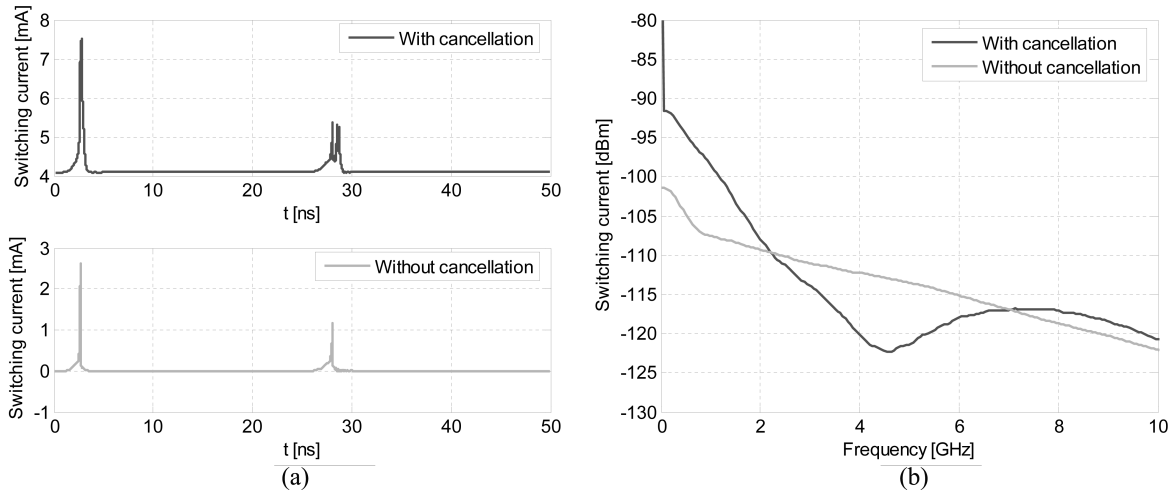
Figure 7.4.10: The simulated one-cycle switching current with and without active suppression in (a) time domain and (b) frequency domain. The designed relative delay in this case is 110 ps, and the desired notch frequency is 4.5 GHz.
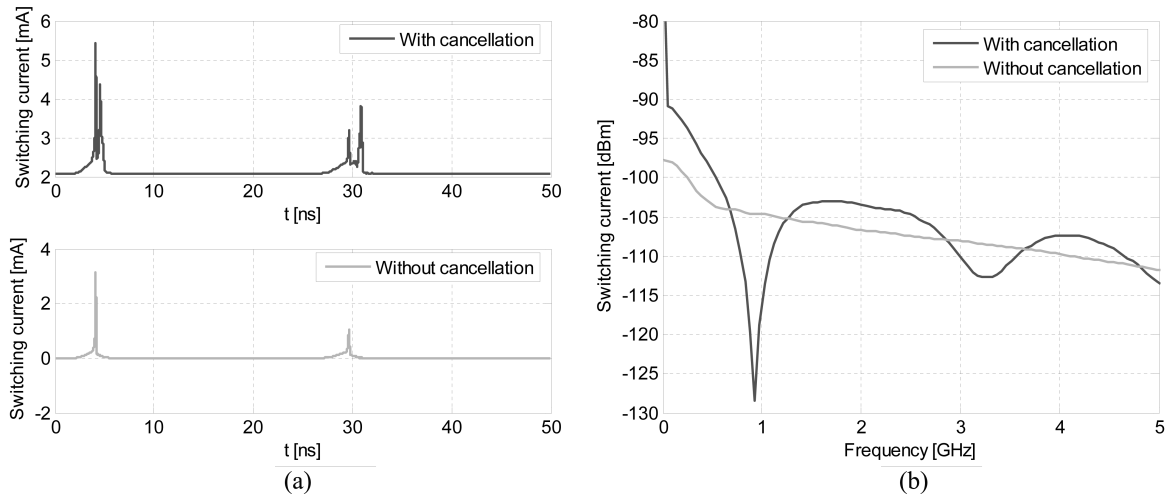
Figure 7.4.11: Simulated one-cycle switching current with and without active suppression in (a) time domain and (b) frequency domain. The designed relative delay in this case is 500 ps, and the desired notch frequency is 1 GHz.
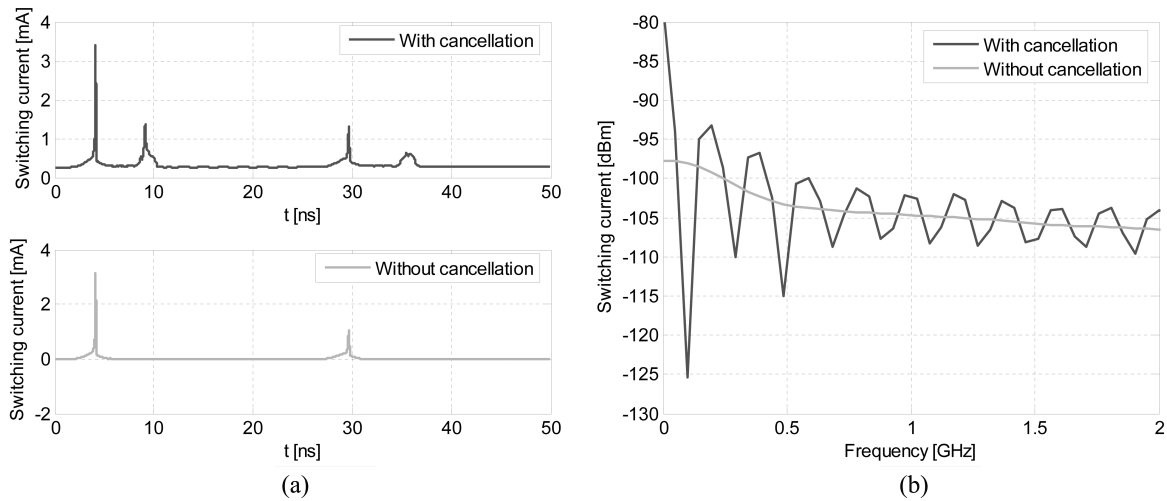

Figure 7.4.12: Simulated one-cycle switching current with and without active suppression in (a) time domain and (b) frequency domain. The designed relative delay in this case is 5 ns, and the desired notch frequency is 0.1 GHz.

7.4.2.5 The mutual effects between the design of DCU, WCU and MCU

When designing the active suppression circuits it is desired and needed to have an insignificant mutual effect between the design of controlling voltages for DCU, WCU and MCU. This subsection investigates these effects using SPICE simulations. The schematic used for the SPICE simulations is the same as that in last subsection.

The performance of DCU, WCU and MCU used for the investigation are defined in Fig. 7.4.13. The relative time delay is defined as the peak to peak time delay between the original switching current and the cancelation current at the falling-input edge. The peak value of the cancelation current is defined as I_p and the pulse width is the time span of the cancelation current at the value of $0.1 \cdot I_p$. It should be noted that the switching current at the falling-input edge of the magnitude controlling unit is much greater than the switching current at the rising-input edge since it consists of both short circuit current and charging current. Thus the greatest concern of this study is at the falling-input edge.
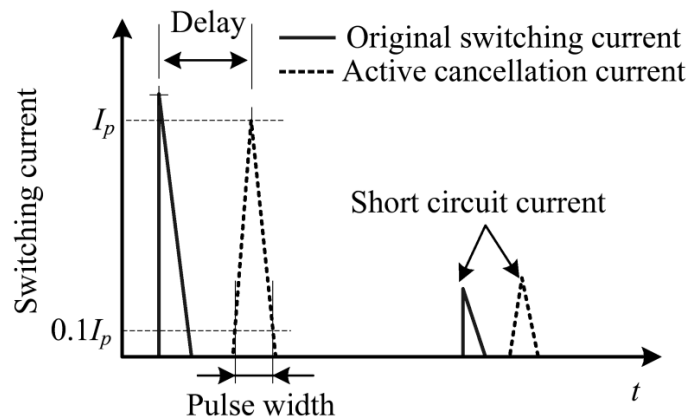
Figure 7.4.13: The parameter definitions in the SPICE simulation for investigating the mutual effects between the design of DCU, WCU and MCU.

Fig. 7.4.14 shows the simulated performance of the active cancelation circuits with different control voltages for DCU, WCU and MCU. It can be seen that V_{wn} has significant effects on the time delay when its value is small (Fig. 7.4.14(b)). The reason for this is that decreasing V_{wn} to a small value close to the threshold voltage greatly reduces the driving capability of the width control unit, so that increases the time delay. V_{wn} also has effects on I_p. The explanation for this can be found in Section 3. It has been shown that changing the value of V_{wn} changes the slope of the signal at the output of WCU (input for MCU) so that affects the magnitude of the active cancelation current. Apart form V_{wn}, other control voltages are shown to have insignificant mutual effects. Based on the SPICE simulation results, the sequence of the design for DCU, WCU and MCU can be proposed, which is design V_{wn} first, and then design V_{mp} and V_{dn}.
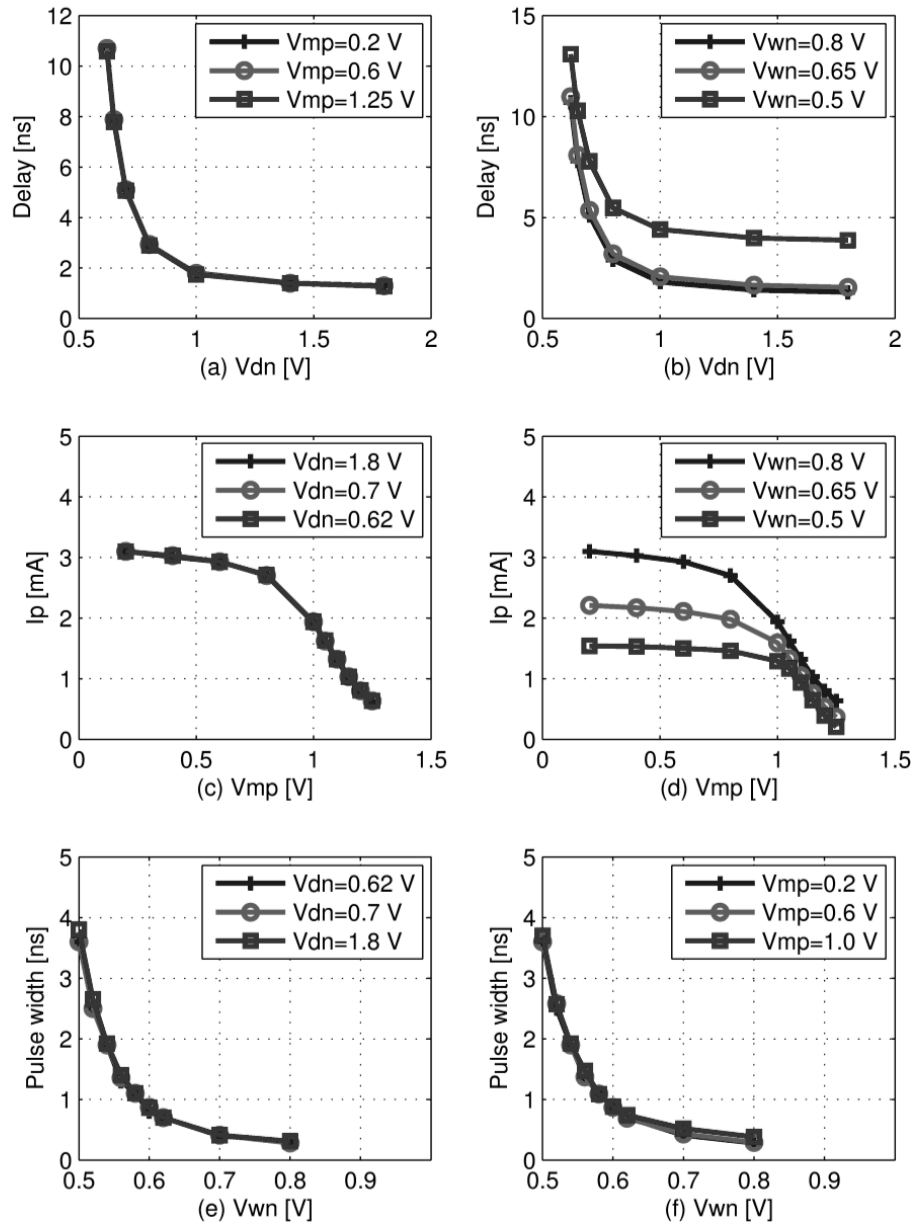
Figure 7.4.14: Simulated performance of the active cancelation circuit with different values of the control voltages for DCU, WCU and MCU. V_{dd} is 1.8 V, the clock frequency is 20 MHz and the rising/falling time of the clock is 5 ns. Other parameters in the simulations are: (a) V_{mn}=0.65 V, V_{wn}=0.8 V, V_{wp}=0.9 V; (b) V_{mn}=0.65 V, V_{mp}=0.2 V, V_{wp}=0.9 V; (c) V_{mn}=0.65 V, V_{wn}=0.8 V, V_{wp}=0.9 V; (d) V_{mn}=0.65 V, V_{dn}=0.7 V, V_{wp}=0.9 V; (e) V_{mn}=0.65 V, V_{mp}=0.2 V, V_{wp}=0.9 V; (f) V_{mn}=0.65 V, V_{dn}=0.7 V, V_{wp}=0.9 V.

7.5 Summary

This chapter focuses on three aspects of the substrate noise issues, the impact evaluation, modeling, and suppression of substrate noise, with special focus on UWB circuits and systems. Efforts have been invested to derive an analytical switching noise model for simple digital circuits and a statistical model for large scale digital blocks. In addition, an active suppression technique for reducing switching noise in digital circuits is also proposed.

The switching noise model presented in this chapter has originally been devised for CMOS technologies with lightly doped substrates. Satisfactory results have been achieved for standard CMOS technologies. The methodology can be applied to heavily doped substrates with lightly doped epitaxial layer, silicon-on-insulator (SOI), and other technologies also. The proposed active suppression technique could potentially be integrated in the design of IP cells. In this way, the substrate noise can be reduced at the very beginning of the entire design flow by setting specific design parameters in the IP cell generation. By doing so the need for area consuming passive noise mitigation schemes is limited whereby the overall cost of the implementation is reduced.

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