A Systematic Method to Synthesize New Transformerless Full-bridge Grid-tied Inverters

Wang, Hongliang; Burton, Sarah; Liu, Yan-Fei; Sen, P. C. ; Guerrero, Josep M.

Published in:
Proceedings of the 2014 IEEE Energy Conversion Congress and Exposition (ECCE)

DOI (link to publication from Publisher):
10.1109/ECCE.2014.6953772

Publication date:
2014

Document Version
Early version, also known as pre-print

A Systematic Method to Synthesize New Transformerless Full-bridge Grid-tied Inverters

Hongliang Wang, Member IEEE, Sarah Burton,
Yan-Fei Liu, Fellow IEEE, P.C.Sen, Life Fellow IEEE
Department of Electrical and Computer Engineering
Queen's University
Kingston, Canada
hongliang.wang@queensu.ca, s.burton@queensu.ca,
yanfei.liu@queensu.ca, senp@queensu.ca

Josep M. Guerrero, Senior Member IEEE
Department of Energy Technology
Aalborg University
Aalborg, Denmark
joz@et.aau.dk

***Abstract*— Many inverter topologies have been proposed to eliminate the leakage current of transformerless Full Bridge Grid-Tied photovoltaic (PV) inverters. These include implementations such as the H5, H6, and HERIC topologies, among others. In this paper, a new full bridge topology synthesis method, called the MN synthesis method, is proposed. The MN method introduces two criteria that can be used to synthesize all of the possible topologies, including the existing topologies as well as new simplified topologies. This method concludes that there are only 15 simplified topologies available. Most simplified topologies from MN method have been verified by existing papers and patents.**

I. INTRODUCTION

In single phase grid-tied inverter systems, the isolation transformer's location is often chosen to achieve a higher system efficiency, while considering the system size, weight, cost and space / volume requirements. However, the resulting configuration can cause the common-mode (CM) ground leakage current to appear on the parasitic capacitor between the PV panels and the ground [1]-[3]. The CM current path for grid-tied transformer-less PV inverter systems is illustrated in Fig.1. It is characterized by a DC power source, power switches, filters, and the parasitic capacitor C_{PV} between the PV panels and the grid ground. According to [4], the leakage current path is equivalent to an LC resonant circuit in

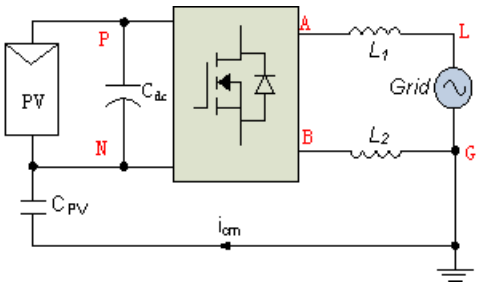


Fig.1 CM current path for the transformerless PV inverter

with the CM voltage. The equivalent common voltage u_{ecm} is defined as:

$$u_{ecm} = \frac{V_{AN} + V_{BN}}{2} + \frac{V_{AN} - V_{BN}}{2} \frac{L_2 - L_1}{L_1 + L_2} \quad (1)$$

Where V_{AN} is the voltage difference between points A and N, V_{BN} is the voltage difference between points B and N, and L_1 and L_2 are the output filter inductors. Fig.2 shows the equivalent circuit for the CM current path.

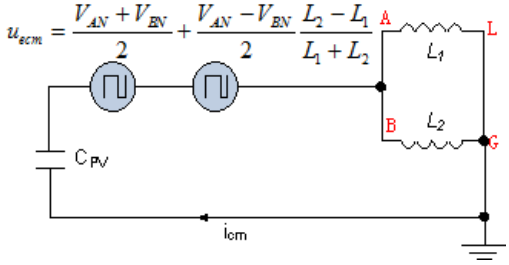


Fig.2 Equivalent circuit for the CM current path

To eliminate leakage currents, the CM voltage must be kept constant. When one inductor is working, such as in half bridge topologies [5] [6], the inductor L_2 is zero. Therefore, (1) is simplified as:

$$u_{ecm} = \frac{V_{AN} + V_{BN}}{2} - \frac{V_{AN} - V_{BN}}{2} = V_{BN} \quad (2)$$

The drawback of half-bridge inverters is that the DC voltage utilization of half-bridge topologies is half of the full-bridge topologies, which means that large quantities of PV panels in series are required, or that a boost DC/DC converter with an extremely high voltage transfer ratio is necessary as the first power conditioning stage and system efficiency may be adversely affected. When two inductors are working whereL_1 is equal to L_2, the system is

considered to have a symmetrical inductive structure. In this case, (1) is simplified as:

$$u_{ecm} = \frac{V_{AN} + V_{BN}}{2} - 0 = \frac{V_{AN} + V_{BN}}{2} \quad (3)$$

From (3), the goal is keep the CM voltage constant for the full bridge topology. When compared to the bipolar SPWM, the unipolar SPWM has better performance in terms of the output current ripple and switching losses, though it cannot maintain a constant CM voltage. Instead, it generates the switching frequency CM voltage. For this reason, some state-of-the art-topologies such as the H5 inverter, HERIC inverter, etc., have been developed from the symmetrical structure [7]-[9].

This paper is organized as follows: Section II describes the operation principles of the proposed method, Section III introduces all simplified topologies from MN principle, Section IV introduces non simplified topologies from MN principle, and Section V provides the results conclusions.

II. OPERATION PRINCIPLES OF THE PROPOSED METHOD

Fig.3 shows the modulation for active power. The grid voltage and reference current are in phase. In the positive half period of the grid voltage, there are two operating modes for the inverter. Mode 1 is the positive conduction (PC) mode. The differential mode voltage V_{AB} is equal to input DC voltage. Mode 2 is the positive freewheeling (PF) mode. The differential mode voltage V_{AB} is equal to zero. In the negative half period of grid voltage, there are also two operating modes. Mode 3 is the negative conduction (NC) mode. Mode 4 is the negative freewheeling (NF) mode.

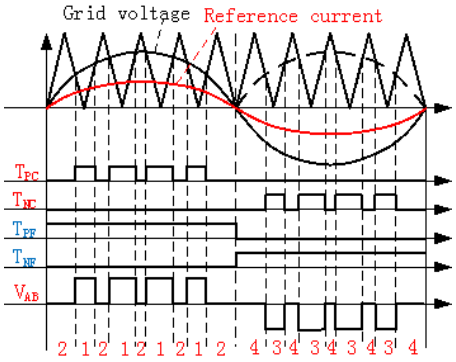


Fig.3 Modulation for active power

Fig.4 shows the full bridge topology and schematic diagram. The point P indicates the positive DC bus, point N indicates negative DC bus, point A indicates the first output of the bridge, and point B indicates the second output of the bridge. From Eq. (3), the CM voltage must be constant in order to minimize the leakage current caused by the high frequency common mode voltage. During PC and NC operating mode, the CM voltage is equal to half of the DC voltage and is a constant.

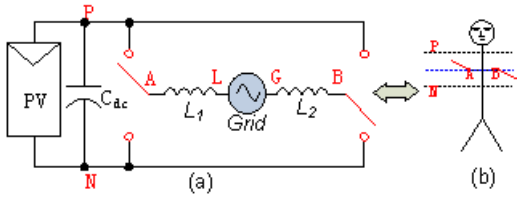


Fig.4 Full bridge (a) full bridge topology (b) schematic diagram of full bridge

Therefore, no leakage current will be generated. The common mode voltage should be kept to half of the DC voltage during PF and NF operating modes in order to minimize the leakage current. This provides an indication of how to construct inverter topologies which consistently minimize the leakage current. Fig.5 shows an illustration for the four desired operating modes of a full bridge inverter with minimized leakage current.

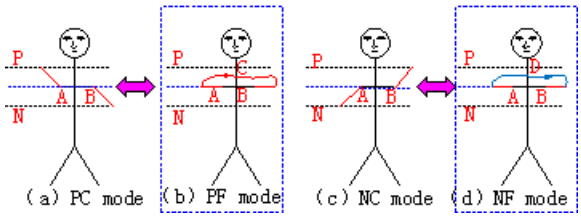


Fig.5 Four modes of improved full bridge (a) PC mode (b) PF mode (c) NC mode (d)NF mode

To best manage the leakage current, the inverter circuit should be constructed according to the following two criteria during PF and NF modes:

Firstly, all switches connected between the positive DC bus (P) and negative DC bus (N) must be off during the PF and NF intervals.

Secondly, it is necessary to provide the new controlled branch for PF mode and NF mode, such as branches C and D, as shown in Fig. 5(b) and (d).

In order to achieve these criteria, the mathematic analysis method called MN principle is been introduced.

It is assumed that M denotes to the total number of switches that are turned on during PC mode. X_1 denotes the number of switches that connect point P to point A in PC mode and X_2 denotes the number of switches that connect point B to point N in PC mode. Thus:

$$M = X_1 + X_2 \quad (4)$$

Similarly, N denotes the total number of switches that are turned on during NC mode. Y_1 denotes the number of switches that connect point P to point B and Y_2 denotes the number of switches that connect point A to point N during NC mode. Thus:

$$N = Y_1 + Y_2 \tag{5}$$

According to the criteria #1, during PF and NF operating mode, four switches should be off. They are the switches between A and P, A and N, B and P and B and N. To acquire the simplified topology (ST), the maximum of the X_1, X_2, Y_1, Y_2 shall be no more than 2. The detailed explain is introduced in Section IV.

$$\mathrm{Max}(X_1, X_2, Y_1, Y_2) \le 2 \tag{6}$$

When equation (6) is not satisfied, the topology is not the simplified topology, and the switches connected in series can be combined. Z_e is defined the simplified switch number. Therefore, only by using Z_e instead of Z according to the eq. (7) can the simplified topology be achieved.

$$Z_e = \begin{cases} Z & Z \le 2 \\ 2 & Z > 2 \end{cases} \qquad Z \in (X_1, X_2, Y_1, Y_2) \tag{7}$$

Tab.1 First family

M:N	X_1+X_2	Y_1+Y_2	
2:2	1+1	1+1	M1
2:3 / 3:2	1+2	1+1	M2
	1+1	1+2	
	2+1	1+1	M3
	1+1	2+1	
3:3	2+1	2+1	M4
	2+1	1+2	M5
	1+2	2+1	
	1+2	1+2	M6
3:4/4:3	2+1	3+1	△
	3+1	2+1	
	2+1	2+2	M7
	2+2	2+1	
	2+1	1+3	△
	1+3	2+1	
	1+2	3+1	△
	3+1	1+2	
	1+2	2+2	M8
	2+2	1+2	
	1+2	1+3	△
	1+3	2+1	
4:4	2+2	2+2	M9
4:4	others		△
3:5/5:3 4:5/5:4	all		△

Tab.2 Second family

M:N	X_1+X_2	Y_1+Y_2	
2:2	1+1	1+1	MD1
2:3 / 3:2	1+2	1+1	MD2
	1+1	1+2	
	2+1	1+1	MD3
	1+1	2+1	
3:3	2+1	2+1	MD4
	2+1	1+2	×
	1+2	2+1	
	1+2	1+2	MD6
3:4/4:3	2+1	3+1	×
	3+1	2+1	
	2+1	2+2	×
	2+2	2+1	
	2+1	1+3	×
	1+3	2+1	
	1+2	3+1	×
	3+1	1+2	
	1+2	2+2	×
	2+2	1+2	
	1+2	1+3	×
	1+3	2+1	
4:4	2+2	2+2	MD7
4:4	others		×or△
3:5/5:3 4:5/5:4	all		×or△

△--No simplified topologies ×--No exist topology

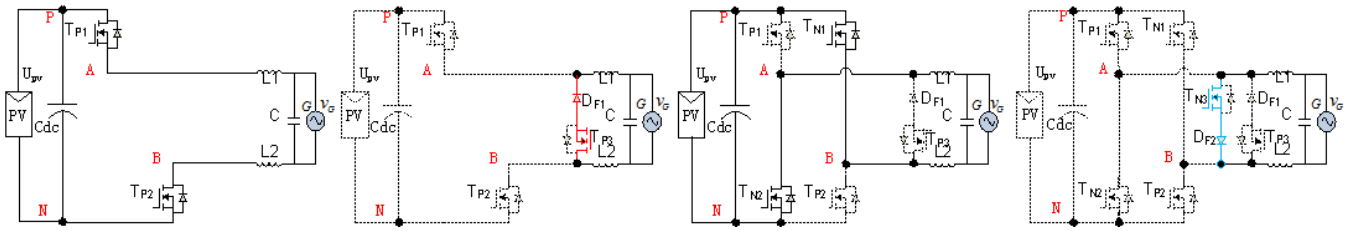
From Fig.5, the two controlled freewheeling branches should be added. Usually, this is achieved by using switch and a diode connected in series. Sometimes, the diode can be implemented by the body diode of an existing switch. Therefore, two topology families can be specified: one which uses external diodes and the other which appropriates the body diode of an existing switch. Table 1 shows the first topology family with external diodes. Table 2 shows the second topology family without external diodes.

III. ALL SIMPLIFIED TOPOLOGIES FROM MN PRINCIPLE

In this section, several examples are provided to show how to use the MN principal to derive a bridge type inverter with minimal leakage currents. In this section, it is assumed that (6) is satisfied.

A. M:N=2:2 or 2:3 or 3:2

Fig.6 shows an example of the M1 topology with external diodes. From tab.1, X_1=1, X_2=1, Y_1=1, Y_2=1. In fig.6 (a), only one switch, Tp1, is used between point P and point A as X_1=1. One switch T_{P2}, is used between point B and point N as X_2=1.In fig.6 (b), the switches T_{P1}, T_{P2} are keeping off as all switches must keep off in freewheeling mode. The controlled branch using switch T_{P3} and diode D_{F1} connects the point B and point A. In fig.6 (c), only one switch T_{N1} is used between point P and point B as Y_1=1. One switch T_{N2} is used between point A and point N as Y_2=1. In fig.6 (d), the switches T_{N1}, T_{N2} are keeping off as all switches must keep off in freewheeling mode. The controlled branch using switchTN3 and diode D_{F2} connects the point A and point B. Similarly, the M2, M3 topology with external diodes and MD1, MD2, MD3 topology without external diodes can also be acquired.



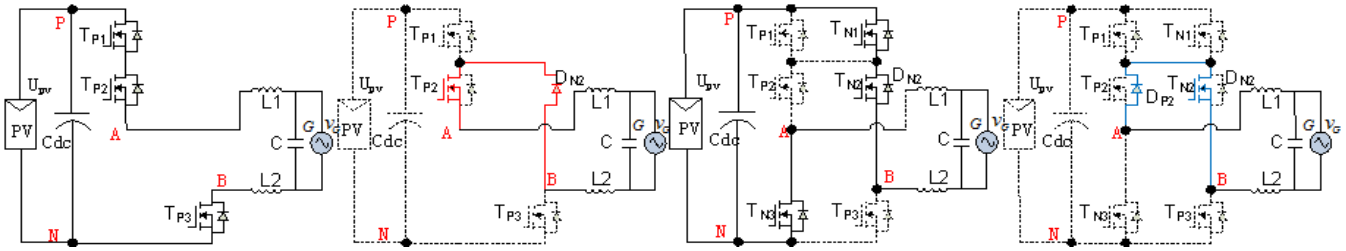
(a) PC mode (b) PF mode (c) NC mode (d) NF mode

Fig.6 Four modes of M1 topology (a) PC mode (b) PF mode (c) NC mode (d) NF mode

B. M:N=3:3

Fig.7 shows one example of the MD4 topology without external diodes. From table.2, X_1=2, X_2=1, Y_1=2, Y_2=1. In fig.7 (a), only two switches Tp1, Tp2 are used between point P and point A as X_1=2. One switch Tp3 is used between point B and point N as X_2=1.In fig.7 (b), the switches T_{P1}, T_{P3} are all off as all switches must stay off in freewheeling mode. The controlled branch using switchTp2

and diode D_{N2} connects the points B and A. In fig.7 (c), two switches T_{N1}, T_{N2} are used between point P and point B as Y_1=2. One switch T_{N3} is used between point A and point N as Y_2=1. In fig.7 (d), the switches T_{N1}, T_{N3} are keeping off as all switches must keep off in freewheeling mode. The controlled branch using switchT_{N2} and anti-diode D_{P2} connects the point A and point B. the topology can be simplified because the parallel switches T_{P1}, T_{N1} can be instead of one switch T_1. Similar analysis, the M4, M5, M6 topologies with external diodes and MD6 without external diodes are also be acquired.

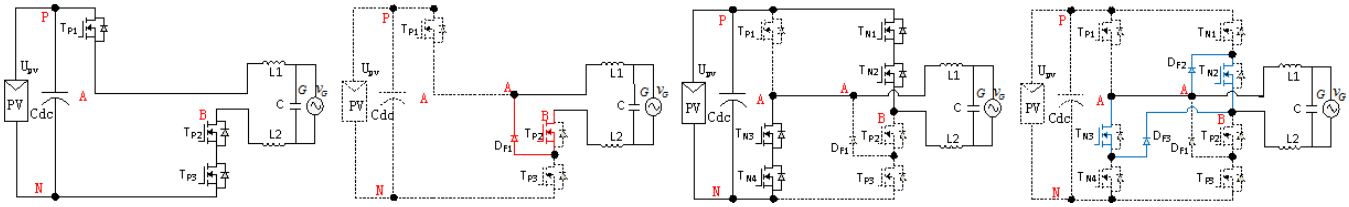


(a) PC mode (b) PF mode (c) NC mode (d) NF mode

Fig.7 Four modes of MD2 topology (a) PC mode (b) PF mode(c) NC mode (d) NF mode

C. *M:N=3:4 or 4:3*

Fig.8 shows an example of the M8 topology with external diodes. From table.1, X_1=1, X_2=2, Y_1=2, Y_2=2. In fig.8 (a), one switch T_{P1} is used between point P and point A as X_1=1. Two switches T_{P2} and T_{P3} are used between point B and point N as X_2=2. In fig.8 (b), the switches T_{P1}, T_{P3} remain off as all switches must again stay off in freewheeling mode. The controlled branch using switchT_{P2} and diode D_{F1} connects point B and point A. In fig.9 (c), two switches, T_{N1} and T_{N2}, are used between point P and point B as Y_1=2. Two switches T_{N3}, T_{N4} are used between point A and point N as Y_2=2. In fig.9 (d), the switches T_{N1} and T_{N4} remain off as they must in freewheeling mode. The controlled branch using switches T_{N2} and T_{N3}, and anti-diodes D_{P2} and D_{P3} connects points A and B. Similarly, the MD6 without external diodes can also be acquired.

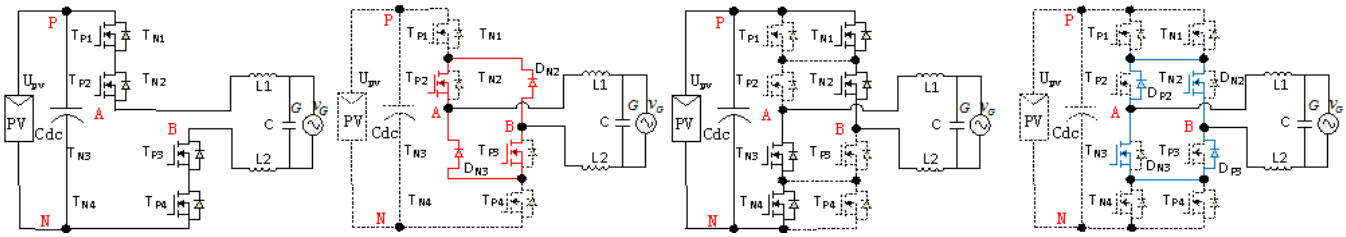


(a) PC mode (b) PF mode (c) NC mode (d) NF mode

Fig.8 Four modes of MD2 topology (a) PC mode (b) PF mode(c) NC mode (d) NF mode

D. *M:N=4:4*

Fig.9 shows an example of the M8 topology with external diodes. From table.1, X_1=2, X_2=2, Y_1=2, Y_2=2. In fig.9 (a), switches Tp1 and Tp2 are used between point P and point A as X_1=2. Two switches T_{P3}, T_{P4}, are used between point B and point N as X_2=2.In fig.9 (b), the switches T_{P1}, T_{P4} again remain off as all expected in freewheeling mode. The controlled branch using switches T_{P2} and T_{P3}, as well as diodes D_{N2} and D_{N3} connect the points B and A. In fig.9 (c), two switches T_{N1} and T_{N2} are used between point P and point B as Y_1=2. Two switches T_{N3}, T_{N4} are used between point A and point N as Y_2=2. In fig.9 (d), the switches T_{N1} and T_{N4} remain off as all switches stay keep off in freewheeling mode. The controlled branch using switch T_{N2}, T_{N3} and anti-diode D_{P2}, D_{P3} connects point A and point B. This topology can be simplified. The parallel switches T_{P1} and T_{N1} can be instead of one switch T_1. Similarly, the parallel switches T_{P4} and T_{N4} can also become the single switch T_4.

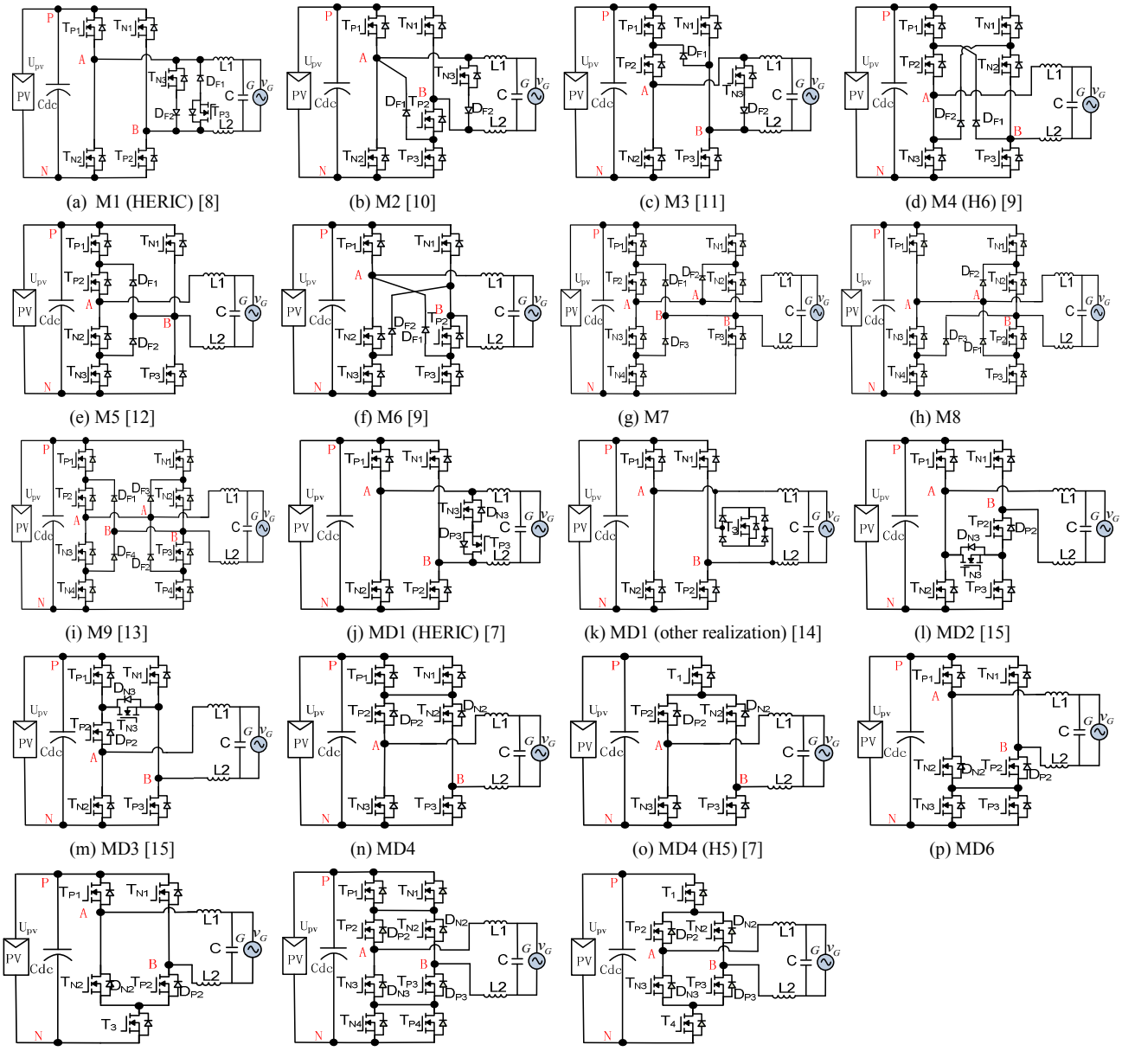


(a) PC mode (b) PF mode (c) NC mode (d) NF mode

Fig.9 Four modes of MD2 topology (a) PC mode (b) PF mode(c) NC mode (d) NF mode

E. *All simplified topology from MN principle*

From the above described analysis method, we may generate the following simplified topologies using the MN principle, as shown in Fig.10 [10]-[16].



(a) M1 (HERIC) [8] (b) M2 [10] (c) M3 [11] (d) M4 (H6) [9]

(e) M5 [12] (f) M6 [9] (g) M7 (h) M8

(i) M9 [13] (j) MD1 (HERIC) [7] (k) MD1 (other realization) [14] (l) MD2 [15]

(m) MD3 [15] (n) MD4 (o) MD4 (H5) [7] (p) MD6

(q) MD6 (H5) [7] (r) MD7 (s) MD7 (DC pass topology) [16]

Fig.10 All simplified topology from MN principle

IV. NON SIMPLIFIED TOPOLOGIES FROM MN PRINCIPLE

In this section, several examples are given to show how to use the MN principal to derive a bridge type inverter with minimum leakage current. This time, it is assumed that (6) is not satisfied. Therefore, the following demonstrated topologies are not the most in their most simplified forms.

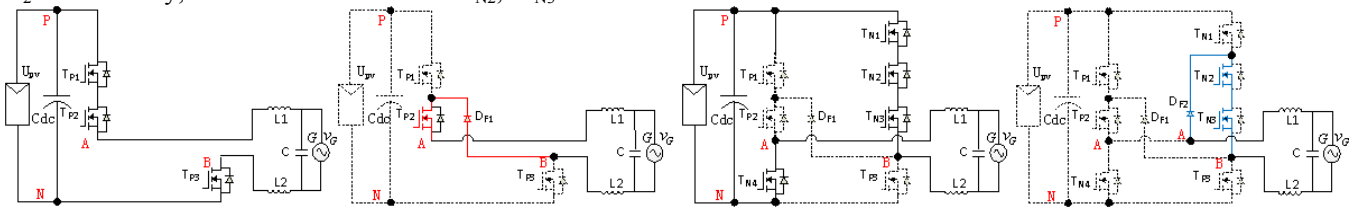
A. *M:N=3:4 or 4:3*

Despite this, we can generate many new topologies from the MN principle. However, in this case some series switches can be combined as necessary. The simplified topologies are that use the Z_e instead of Z according to the Eq. (7).

For example, For M=3 N=4 (or M=4 N=3), there also are four combined types. First, X_1=1, X_2=2, Y_1=3, Y_2=1.

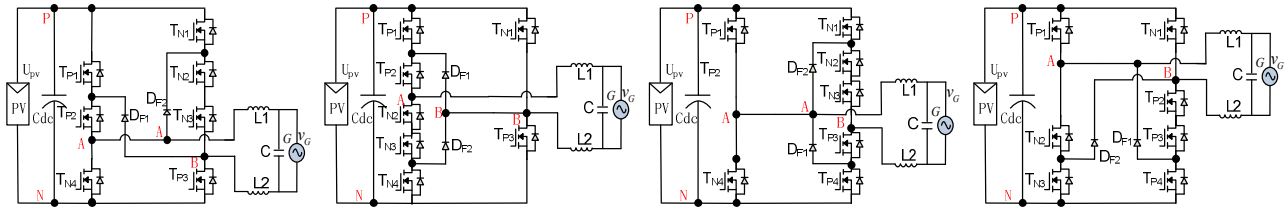
Second, X_1=1, X_2=2, Y_1=1, Y_2=3. Third, X_1=2, X_2=1, Y_1=3, Y_2=1. Fourth, X_1=2, X_2=1, Y_1=1, Y_2=3.

Fig.11 shows one example of X_1=2, X_2=1, Y_1=3, Y_2=1.Obviously, the switches between T_{N2}, T_{N3} can be instead of one switch. Thus, the simplified topology is M4 shown in Fig.10 (d). Fig.12 shows the four non-simplified topologies. Their simplified topologies are M4, M5, M5, and M6 shown in Fig.10 (d), (e), (f).



(a) PC mode (b) PF mode (c) NC mode (d) NF mode

Fig.11 First topology of X_1=1, X_2=2, Y_1=3, Y_2=1 (a) PC mode (b) PF mode(c) NC mode (d) NF mode



(a) (b) (c) (d)

Fig.12 Four topologies of M=3 N=4 or M=4 N=3 (a) X_1=1, X_2=2, Y_1=3, Y_2=1 (b) X_1=1, X_2=2, Y_1=1, Y_2=3 (c), X_1=2, X_2=1, Y_1=3, Y_2=1 (d) X_1=2, X_2=1, Y_1=1, Y_2=3

B. M:N= 3:5 or 5:3 or 4:5 or 5:3 and so on

When M or N is more than 4, such as M=5, the X_1 or X_2 is more than 2. The new topologies include the redundant switches. Their simplified topologies are seen in Fig.10.

For example, When the X_1=2, X_2=1, Y_1=1, Y_2=4, the Y_2 is more than 2, the Y_2 is instead of Y_{e2} according to the Eq. (7). The simplified topology is X_1=2, X_2=1, Y_1=1, Y_{e2}=2, and it is equivalent to M5 topology shown in Fig.10 (e).

V. CONCLUSION

The MN synthesis method is proposed to derive new full bridge inverter with minimum leakage current introduced by common mode voltage. The MN method has two primary criteria. Additionally, examples have been provided to illustrate how to use the MN principal to derive new topologies. It has been demonstrated that there are only 15 full bridge inverter topologies that can minimize the leakage current. The final paper will provide a more detailed analysis and derivation procedure of this method. The two basic criteria shall be seen in more detail, as well as a rigorous analysis of the simplified topologies. Here, 15 simplified topologies have been synthesized according to the MN method. All other possible topologies have been shown to be the non-simplified equivalents, depending on the existence and requirements of external diodes. This paper has also introduced the method to simplify the non-simplified topologies. We have has proven that no new simplified full bridge topologies exist. Notably, most of the simplified topologies from MN method have been verified by existing papers and patents.

REFERENCES

[1] S. B. Kjaer, J. K. Pederson, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep. /Oct. 2005.

[2] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1184–1194, Sep. 2004.

[3] Q. Li and P. Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different dc link configuration,"*IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1320–1333, May.2008.

[4] O. Lopez, F. D. Freijedo, A. G. Yepes, P. Fernandez-Comesana, and so on, "Eliminating ground current in a transformerless photovoltaic application," *IEEE Trans. Energy Convers.*, vol. 25, no. 1, pp. 140–147, Mar. 2010.

[5] R. Gonzalez, E. Gubia, J. Lopez, and L.Marroyo, "Transformerless single phase multilevel-based photovoltaic inverter," *IEEE Trans. Ind. Electron.*,vol. 55, no. 7, pp. 2694–2702, Jul. 2008.

[6] H. Xiao and S. Xie, "Transformerless split-inductor neutral point clamped three-level PV grid-connected inverter," *IEEE Trans. Power Electron.*,vol. 27, no. 4, pp. 1799–1808, Apr. 2012.

[7] M. Victor, F. Greizer, S. Bremicker, and U. H¨ubler, "Method of converting a direct current voltage from a source of direct current voltage, more specifically from a photovoltaic source of direct current voltage, into an alternating current voltage," U.S. Patent 7 411 802, Aug. 12, 2008.

[8] S. Heribert, S. Christoph, and K. Jurgen, "Inverter for transforming a DC voltage into an AC current or an AC voltage," Europe Patent 1 369 985(A2), May 13, 2003.

[9] W. Yu, J. Lai, H. Qian, and C. Hutchens, "High-efficiency MOSFET inverter with H6-type configuration for photovoltaic non-isolated ac-module applications," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1253–1260, Apr. 2011.

[10] G. Hu and Y. Chen, "A new Grid-tied Inverter," China Patent CN201550040U, Aug, 11, 2010.

[11] G. Hu and Y. Chen, "A new Grid-tied Inverter," China Patent CN201515310U, June, 23, 2010.

[12] S. Bremicker, F. Greizer, and M. Victor, "Inverter, More Specifically for Photovoltaic Plants," U.S. Patent 2009/0103340 A1, April 23, 2009.

[13] H.Wang and W. Zhao, "A new single-phase transformerless Inverter," China Patent 201110452074.5(A) Dec, 29, 2011.

[14] T. Kerekes, R. Teodorescu, P. Rodriquez, G. Vazquez and E. Aldabas,"A new high efficiency single-phase transformerless PV inverter topology," *IEEE Trans. on Ind. Elect*., vol.58, no. 1, pp.184-191,Jan.2011.

[15] Z. Özkan and A.M. Hava "Leakage Current Analysis of Grid-connected transformerless Solar Inverters with Zero State Isolation," in Proc. IEEE,ECCE,2011 Conf., pp. 2460-2466, 17-22 Sept. 2011.

[16] B. yang, W. li, Y.Gu and X. He, "Improved Transformerless Inverter with Common-Mode Leakage Current Elimination for a Photovoltaic Grid-Connected Power System," *IEEE Trans. Power Electron.* vol. 27, no. 2, pp. 752–762, Feb. 2012.