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Wang, Huai; Liu, Wenchao; Chung, Henry

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Huai Wang
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Henry Shu-Hung Chung

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Hold-Up Time Analysis of a DC-Link Module With a Series Voltage Compensator

Huai Wang, *IEEE Member*
Centre for Power Electronics
City University of Hong Kong, Kowloon, Hong Kong
Department of Energy Technology
Aalborg University, Aalborg, Denmark
hwa@et.aau.dk

Wenchao Liu, Henry Chung, *IEEE Senior Member*
Centre for Power Electronics
City University of Hong Kong
Kowloon, Hong Kong
wenchao.liu@cityu.edu.hk
eeshc@cityu.edu.hk

***Abstract* - A dc-link module composed of dc-link capacitors and a series voltage compensator has been proposed. It has been verified that the module can reduce the dc-link capacitance to 10-20% while achieving a very low voltage ripple across its output terminals. This paper investigates the required dc-link capacitance when a certain period of hold-up time is considered. Trade-off design conditions are presented and the hold-up time is compared with the solution without the series voltage compensator. The analysis is crucial to power converters connected to critical loads when hold-up time is required. The theoretical predictions have been verified by experimental results.**

I. INTRODUCTION

Dc-link capacitors are used for absorbing instantaneous power difference between the input source and output load, minimizing voltage variation on the dc link, and providing sufficient energy during the hold-up time of the system if required. Many efforts have been devoted to reducing the required dc-link capacitance, providing the opportunity to increase the power density and enhance the reliability of power electronic systems. The concept of active power filters developed for ac-line power conditioning [1]-[3] can be applied in the dc-link side for capacitance reduction. Various kinds of auxiliary circuits in parallel with the dc-link capacitor are proposed in [4]-[9]. The added circuit serves as an active impedance or energy source. The common challenge of all these methods is that the components used in the auxiliary circuit are under a high voltage stress, which could be as high as the dc-link voltage. In [10], a voltage compensator connected in series with the dc-bus line is introduced and applied for different types of capacitor-supported power electronic systems. The compensator processes the voltage ripple across the dc-link capacitor only, allowing the use of components of voltage rating much lower than the dc link.

This paper analyzes the hold-up time of the dc-link module proposed in [10]. On one hand, the impact of the added active filters on the hold-up function of the dc-link is not discussed in [4]-[10]. On the other hand, it is crucial to provide the design guideline for the applications requiring hold-up function [11]. Accordingly, the hold-up time analysis and the trade-off design conditions of the dc-link module are discussed and experimentally verified in the following sections.

II. PROPOSED DC-LINK MODULE

A. Basic Concept

Fig. 1 depicts the basic concept of the module for reducing the dc-link capacitance. The dc-link capacitor is connected to the output of the front-end power conversion stage. The capacitor voltage v_C is composed of dc component V_C and ripple voltage Δv_C. The peak-to-peak value of Δv_C is $2|\Delta v_C|$. A voltage source v_{ab} is connected in series between the dc-link capacitor C and output v_d. It generates a voltage counteracting Δv_C with its dc component equal to zero (i.e., $v_{ab} = \Delta v_C$). Thus, v_d has the same dc value as that across C, but with a zero ripple voltage in the ideal situation. Such architecture allows a high voltage ripple on C, implying that the value of C can be made smaller, but at the expense of increasing the magnitude of v_{ab}.

From energy storage perspective, the dc-link module distributes the energy storage for maintaining output power during hold-up time into the dc-link capacitor C and the voltage compensator.

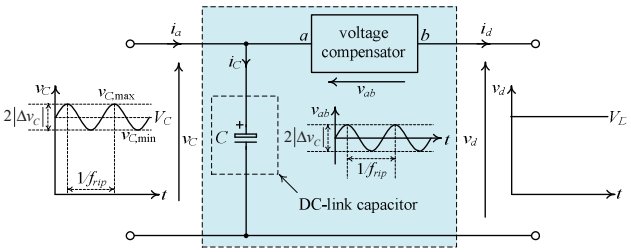


Figure 1. Basic concept of the proposed dc-link module.

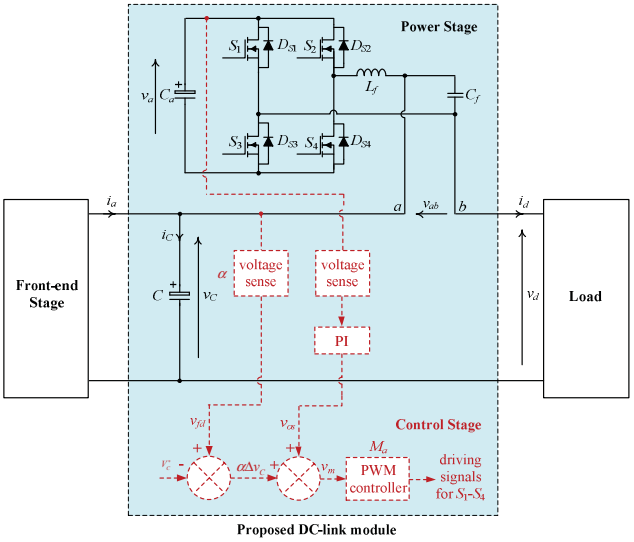


Figure 2. Implementation of the proposed dc-link module.

B. *Implementation of the DC-link Module*

Fig. 2 shows the implementation of v_{ab} and its control method. v_{ab} is generated by a dc-ac converter consisting of a full-bridge (FB) and an output filter formed by the inductor L_f and capacitor C_f. Its dc side is connected to an energy storage device such as a capacitor. The gate signals for the switches S_1-S_4 in the FB are generated by a PWM modulator. It should be noted that the power stage could also be implemented by a half-bridge for loads with unidirectional current flow. The voltage ripple Δv_C on C is sampled by a scaling factor of α. A PI control loop is added to regulate the dc voltage level of the input capacitor of the voltage compensator.

C. *Operation of the DC-link Module*

Figs. 3(a) and (b) present the operating modes of the voltage compensator. When S_2 and S_3 are on, the capacitor C_a is charged by the load current i_d and when S_1 and S_4 are on, the capacitor C_a is discharged. Fig. 3(c) shows the waveforms of the dc-link capacitor voltage v_C, modulating signal v_m, carrier signal v_{tri}, and the voltage across C_a, v_a. It should be noted that the feedback signal v_{fd} may contain multiple frequency components as it is obtained by scaling down Δv_C. t_0 and t_1 in Fig. 3(c) are defined as the two time instants when Δv_C is across zero within one period. During t_0-t_1, the capacitor C_a is being charged by the load current and its voltage increases from minimum to maximum. During t_1-t_2, the capacitor C_a is being discharged by the load current from maximum to minimum. Based on Fig. 3 and SPWM principle discussed in [12], the output of the voltage compensator v_{ab} is in phase with the modulating signal v_m, thus, in phase with voltage ripple across the dc-link capacitor. The detailed derivations of the operation of the proposed dc-link module are presented in [13]. As discussed in [13], the voltage compensator processes only reactive power except for a special case when the ac components of i_a and i_d are of same freqency and in phase.

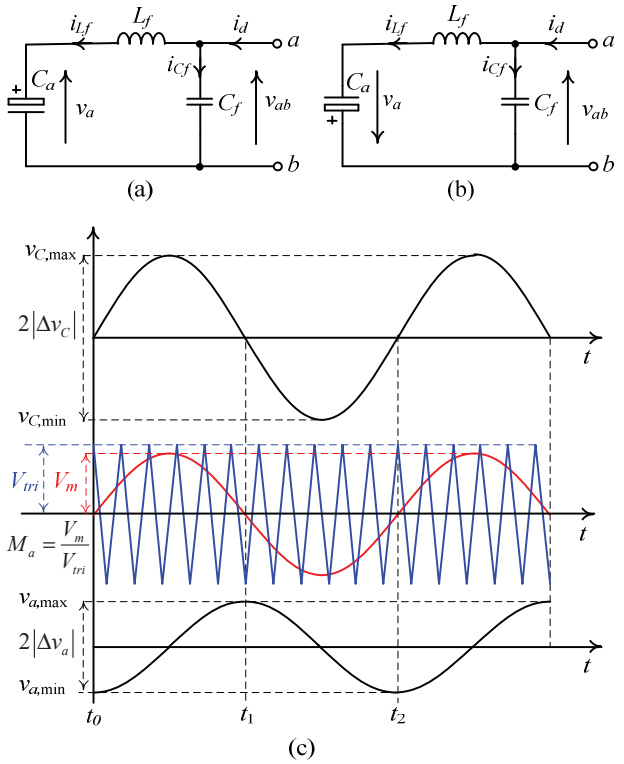


Figure 3. Operation of the voltage compensator: (a) operating when S_2 and S_3 are on, (b) operating when S_1 and S_4 are on and (c) SPWM and the voltage across C_a.

TABLE I DEFINED PARAMETERS FOR HOLD-UP TIME ANALYSIS

Parameters	Descriptions
N	Number of cycles respect to the period of the dc-link voltage ripple.
$\lambda = \frac{C}{C_a}$	Ratio between C and C_a.
$\mu = \frac{\Delta v_C(0)}{V_C}$	Ratio between the ripple voltage (half of peak-to-peak value) and dc voltage across the dc-link capacitor. V_C is the steady-state dc component of v_C.
$\gamma = \frac{v_a(0)}{\Delta v_C(0)} \quad (\gamma \geq 1)$	Ratio between the dc voltage of the auxiliary capacitor and dc-link voltage ripple (half of peak-to-peak value).
$\beta = \frac{\lvert\Delta I_C\rvert}{I_d}$	Ratio between the dc-link capacitor ripple current (half of peak-to-peak value) and the steady-state load current. $\lvert\Delta I_C\rvert$ is the magnitude of i_C and I_d is the steady-state dc component of i_d.
$\rho = \frac{V_{d,\min}}{V_C}$	Ratio between the minimum required dc voltage of the output terminal of the dc bus line and the nominal dc-link voltage. V_d is the steady-state dc component of v_d.
$\Delta v_C(0) = \frac{\lvert\Delta I_C\rvert}{\omega C}$	ω is the angular frequency of the capacitor ripple current $\omega = 2\pi f_{rip}$.
$\frac{v_a(0)}{V_C} = \gamma\mu$	$C\Delta v_C(0) = \frac{\lvert\Delta I_C\rvert}{\omega} = \frac{\beta I_d}{\omega}$
$\frac{CV_C^2}{2P_d} = \frac{CV_C}{2I_d} = \frac{\beta CV_C}{2\lvert\Delta I_C\rvert} = \frac{\beta CV_C}{2\omega C\Delta v_C(0)} = \frac{\beta}{2\omega\mu}$	

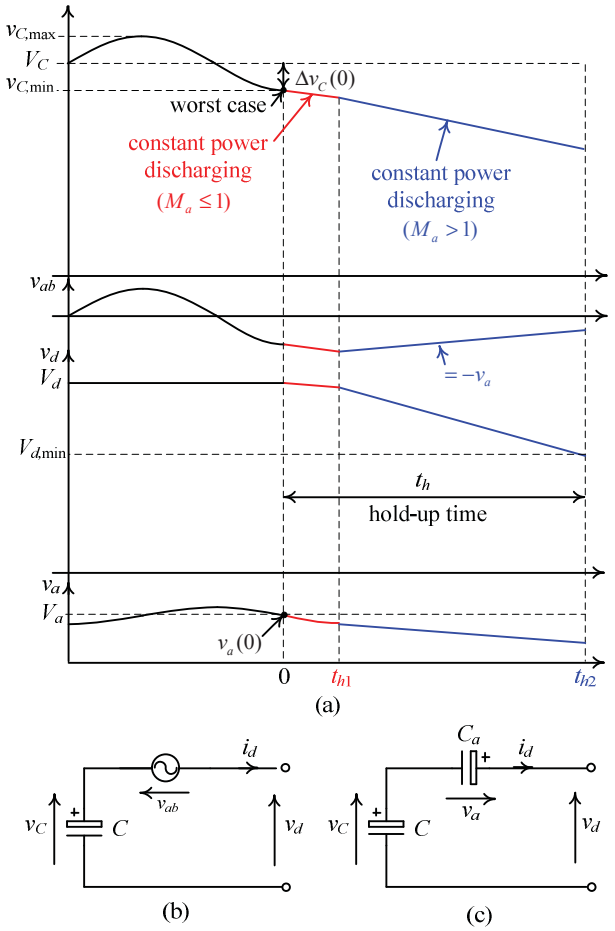


Figure 4. Operating modes during hold-up time: (a) waveforms during the sustained hold-up time intervals, (b) equivalent circuit when $M_a \le 1$ and (c) equivalent circuit when $M_a > 1$.

III. HOLD-UP TIME ANALYSIS

The analysis in this part is crucial for power converters connected to critical loads when the entire system has to meet the hold-up time requirement. After a line dropout, the energy stored in the dc-link module solely delivers power to the load. In the following analysis, the hold-up time is defined as the time duration between the start of the supply outage, i.e., $i_a = 0$ and the voltage v_d reduces to the minimum dc bus voltage $V_{d,min}$. Fig. 4 (a) presents the timing diagram of two consecutive hold-up intervals distinguished by value of the modulation amplitude ratio M_a defined in Fig. 3(c) (i.e., $M_a = V_m/V_{tri}$). Figs. 4(b) and (c) show the equivalent circuits of the two intervals $0\sim t_{h1}$ and t_{h1}-t_{h2}, respectively. Table I defines the parameters used in the following analysis. The power loss of the voltage compensator is neglected and the dc-link module is connected to a constant power load P_d.

(1) Initial state ($t = 0$):

At the time instant t = 0, the voltage across the dc-link capacitor is $v_C(0) = V_C - \Delta v_C(0)$ in the worse-case scenario. The voltage across C_a, $v_a(0)$, is equal to the average value of V_a. The voltage ripple across the dc-link capacitor is fully compensated by v_{ab} during steady-state operation. It implies that

$$v_{ab}(0) = v_a(0)\frac{\alpha \Delta v_C(0)}{V_{tri}} = \Delta v_C(0) \tag{1}$$

(2) Stage I- $M_a \le 1$ (from $t = 0$ to $t = t_{h1}$)

t_{h1} is the time instant at which the amplitude modulation ratio $M_a = 1$. Thus,

$$\frac{\alpha \Delta v_C(t_{h1})}{V_{tri}} = 1 \tag{2}$$

$$v_{ab}(t_{h1}) = -v_a(t_{h1}) \tag{3}$$

According to (1)-(3),

$$\Delta v_C(t_{h1}) = v_a(0) \tag{4}$$

$$v_d(t_{h1}) = V_C + v_a(t_{h1}) - v_a(0) \tag{5}$$

Due to the variation of v_d, the load current I_d is also varying. By neglecting the variation of I_d,

$$\Delta v_C(t_{h1}) = \Delta v_C(0) + \frac{I_d}{C}t_{h1} = v_a(0) \tag{6}$$

$$t_{h1} = \frac{C}{I_d}\left[v_a(0) - \Delta v_C(0)\right] = \frac{C\Delta v_C(0)}{I_d}(\gamma - 1) = \frac{\beta}{\omega}(\gamma - 1) \tag{7}$$

By applying the conservation of energy, it can be obtained that

$$\frac{1}{2}Cv_C^2(0) + \frac{1}{2}C_a v_a^2(0) - \frac{1}{2}Cv_C^2(t_{h1}) - \frac{1}{2}C_a v_a^2(t_{h1}) = P_d t_{h1} \tag{8}$$

It can be derived from (8) that

$$v_a(t_{h1}) = \mu\sqrt{\gamma^2 - \lambda\left(\gamma^2 - 1\right)}\,V_C \tag{9}$$

By substituting (9) into (5),

$$\begin{aligned} v_d(t_{h1}) &= V_C + \mu\sqrt{\lambda + (1-\lambda)\gamma^2}\,V_C - v_a(0) \\ &= \left[1 + \mu\sqrt{\gamma^2 - \lambda\left(\gamma^2 - 1\right)} - \mu\gamma\right]V_C \end{aligned} \tag{10}$$

(3) Stage II- $M_a > 1$ (from $t = t_{h1}$ to $t = t_{h2}$)

The final voltages across the dc-link capacitor and the

input capacitor of the voltage compensator are defined as $v_C(t_{h2})$ and $v_a(t_{h2})$, respectively. The voltage $v_d(t_{h2}) = V_{d,min} = \rho V_C$. As the two capacitors are connected in series, the voltage variations of them are inversely proportional to their capacitances. Therefore,

$$\begin{aligned}\Delta v_C(t_{h2}) &= \Delta v_C(t_{h1}) + \frac{C_a}{C_a + C}\left[v_d(t_{h1}) - v_d(t_{h2})\right] \\ &= \Delta v_C(t_{h1}) + \Delta x V_C\end{aligned} \tag{11}$$

$$\begin{aligned}v_a(t_{h2}) &= v_a(t_{h1}) - \frac{C}{C_a + C}\left[v_d(t_{h1}) - v_d(t_{h2})\right] \\ &= v_a(t_{h1}) - \lambda \Delta x V_{dc}\end{aligned} \tag{12}$$

where

$$\Delta x = \frac{1}{1+\lambda}\left\{(1-\rho) - \mu\left[\gamma - \sqrt{\gamma^2 - \lambda\left(\gamma^2 - 1\right)}\right]\right\} \tag{13}$$

By applying the conservation of energy, it can be obtained that

$$\begin{aligned}&\frac{1}{2}Cv_C^2(t_{h1}) + \frac{1}{2}C_a v_a^2(t_{h1}) - \frac{1}{2}Cv_C^2(t_{h2}) - \frac{1}{2}C_a v_a^2(t_{h2}) \\ &= P_d\left(t_{h2} - t_{h1}\right)\end{aligned} \tag{14}$$

It can be derived from (14) that

$$t_{h2} - t_{h1} = \frac{\beta}{\omega}\left(\frac{\rho}{\mu}\Delta x + \frac{1+\lambda}{2\mu}\Delta x^2\right) \tag{15}$$

Therefore, according to (7) and (15), the sustained hold-up time t_h and corresponding number of hold-up cycle N of the proposed dc-link module are given by

$$t_h = \frac{\beta}{\omega}\left(\frac{\rho}{\mu}\Delta x + \frac{1+\lambda}{2\mu}\Delta x^2 + \gamma - 1\right) \tag{16}$$

$$N = \frac{\beta}{2\pi}\left(\frac{\rho}{\mu}\Delta x + \frac{1+\lambda}{2\mu}\Delta x^2 + \gamma - 1\right) \tag{17}$$

For special case when $\gamma = 1$, $\Delta x\big|_{\gamma=1} = \dfrac{1-\rho}{1+\lambda}$ and $N\big|_{\gamma=1} = \dfrac{\beta}{2\pi}\dfrac{1-\rho^2}{2\mu(1+\lambda)}$.

For the sake of comparison, the hold-up time of a dc-link with the same energy storage and without the voltage compensator is derived. Define the corresponding dc-link capacitance and hold-up time as C' and t_h', respectively. The number of hold-up cycle is N'. Therefore,

$$C' = \frac{CV_C^2/2 + C_a v_a^2(0)/2}{V_C^2/2} = \left(1 + \frac{\gamma^2\mu^2}{\lambda}\right)C \tag{18}$$

By assuming that the ripple currents following through the dc-link capacitors with and without the voltage compensator are the same,

$$\mu' = \frac{\Delta v_C'}{V_C} = \frac{|\Delta I_C|}{\omega C' V_C} = \frac{\beta I_d}{\omega C' V_C} \tag{19}$$

According to (18) and (19),

$$\begin{aligned}t_h' &= \frac{C'\left(V_C - \Delta v_C(0)\right)^2 - C'\left(\rho V_C\right)^2}{2P_d} \\ &= \frac{\beta}{\omega}\frac{\left(\lambda + \gamma^2\mu^2\right)\left[\left(1 - \dfrac{\lambda\mu}{\lambda + \gamma^2\mu^2}\right)^2 - \rho^2\right]}{2\lambda\mu}\end{aligned} \tag{20}$$

$$N' = \frac{\beta}{2\pi}\frac{\left(\lambda + \gamma^2\mu^2\right)\left[\left(1 - \dfrac{\lambda\mu}{\lambda + \gamma^2\mu^2}\right)^2 - \rho^2\right]}{2\lambda\mu} \tag{21}$$

IV. Design Guidelines

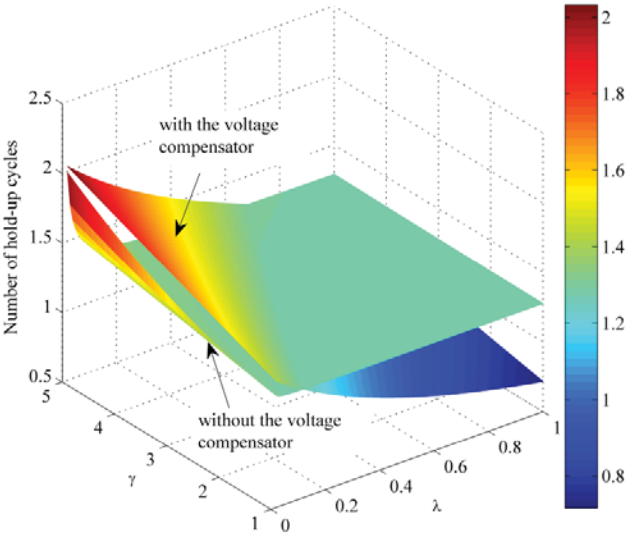


Figure 5. Hold-up time analysis with and without the proposed voltage compensator (Conditions: $\beta = 1$, $\rho = 0.8$, $\mu = 0.02$).

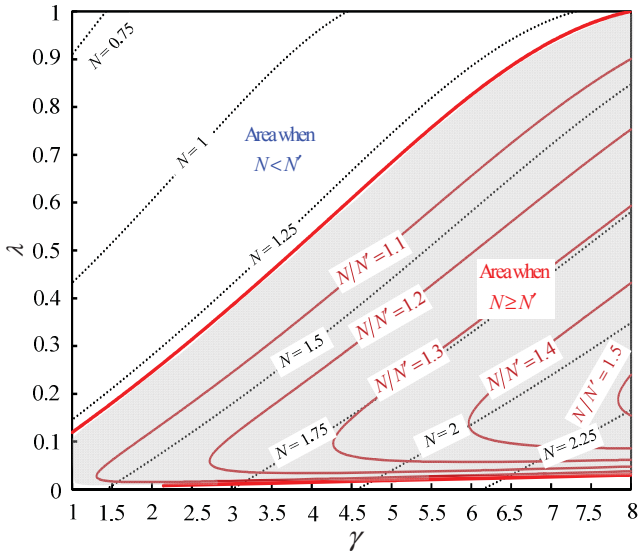


Figure 6. Design curves for selection of λ and γ ($\rho = 0.8$, $\mu = 0.02$).

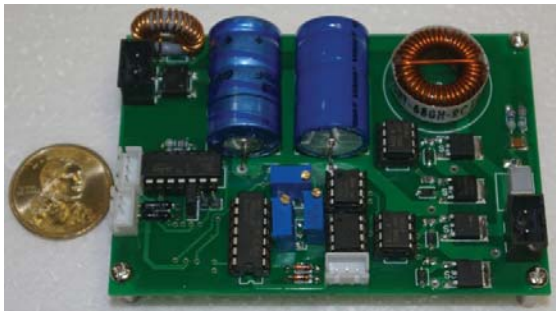
The design guidelines for the applications without hold-up time requirements have been presented in [13]. This paper focuses the design guidelines when the hold-up function is required. For this type of applications, the determining factor for the energy storage is the required hold-up time rather than the voltage ripple specification.

Figs. 5 and 6 graphically represent (17) and (21). It should be noted that λ and γ are only for the proposed dc-link module containing an additional energy storage capacitor C_a. However, they appear in (21) because that the comparison is based on the same energy storage. The λ- γ selection area ensuring extended hold-up time by using the dc-link module is shown by the shaded area in Fig. 6. Various curves of constant number of hold-up cycles and ratios of N/N' are plotted in dot line and solid line, respectively. For $N / N' > 1$, the hold-up time of the dc-link module is longer than dc-link capacitor only.

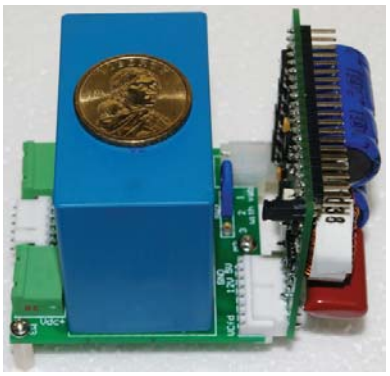
The results shown in Fig. 5 and Fig. 6 are with μ of 0.02, which is corresponding to a determined value of the dc-link capacitance C from the design perspective. Therefore, the trade-off design condition is between maximization of N / N' and minimization of C_a and its voltage stress V_a, meanwhile, achieving the required hold-up cycle N. Different figures can be plotted for other values of μ, corresponding to different value of C. By considering all of the values of λ and γ selected for different value of μ, it allows the selection of the optimal values of μ, λ and γ, thus, the optimal values of C, C_a and the voltage stress of C_a, V_a.

V. Experimental Verifications

The proposed dc-link module can be applied for various capacitor-supported power electronic systems as the verifications shown in [10] and [13]. Two prototypes of the dc-link module have been built and implemented by analog controller and a low cost MCU, respectively, as shown in Fig. 7. The input of the voltage compensator is implemented



(a) Voltage compensator with an analog controller.



(b) Proposed dc-link module with a MCU controller.

Figure 7. Photos of the prototypes.

by two 470 μF/63 V E-Caps with a predicted lifetime of 128,000 hours at nominal voltage and current stresses at 85°C [14]. Their lifetime is comparable with that of the film capacitors used in the prototypes. To reduce the conduction losses, four low voltage (i.e., 100 V) MOSFETs are used in the FB inverter. Therefore, all of the components in the voltage compensator withstand very low voltage stresses.

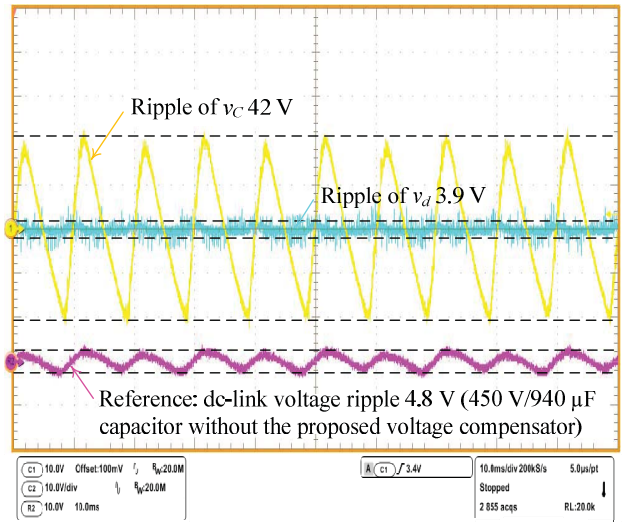


Figure 8. Voltage ripples on the dc-link capacitor and the output of the dc-link module in a 390 V dc-link PFC power converter (C: 450 V/110 μF, C_a: 63 V/940 μF, 500 W load testing, timescale:10ms /div).

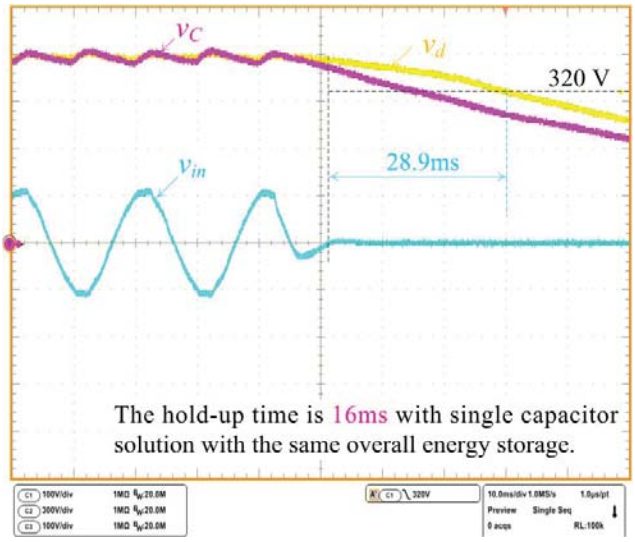


Figure 9. Hold-up time of the dc-link module in a 390 V dc-link PFC power converter (C: 450 V/110 µF, C_a: 63 V/940 µF, 170 W load testing, v_C: 100 V/div, v_d: 100 V/ div, v_{in}: 300 V/ div and timescale: 10ms /div).

Fig. 8 and Fig. 9 present the experimental waveforms. When the hold-up time is not required, the dc-link capacitance is reduced from 940 µF to 110 µF while ensuring a reduction of voltage ripple from 4.8 V to 3.9 V at 500 W load. It can be noted that the voltage ripple across the power film capacitor in the proposed dc-link module is still high, which is cancelled by output voltage of the compensator, resulting in a very low ripple component in the output terminals. As shown in Fig. 9, the same dc-link module achieves a hold-up time of 28.9 ms under a load of 170 W, 1.8 times of that of the single capacitor solution, which has a hold-up time of 16 ms, with the same overall energy storage.

CONCLUSION

The hold-up time of a proposed dc-link module with a series voltage compensator is analyzed. The trade-off design conditions to maximize the hold-up time are presented. Comparisons between solutions with and without the series voltage compensator have been made for a PFC front-end power converter. The experimental results verify that the hold-up time can be extended (e.g., 1.8 times in the testing example) with the same overall energy storage by using the dc-link module.

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