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Published in:
I E E E Transactions on Industrial Electronics

DOI (link to publication from Publisher):
10.1109/TIE.2013.2282607

Publication date:
2014

Document Version
Early version, also known as pre-print

Performance Improvement of a Pre-filtered Synchronous-Reference-Frame PLL By Using a PID-Type Loop Filter

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***Abstract*—Control Parameters design of a three-phase synchronous reference frame phase locked loop (SRF-PLL) with a pre-filtering stage (acting as the sequence separator) is not a trivial task. The conventional way to deal with this problem is to neglect the interaction between the SRF-PLL and pre-filtering stage, and treat them as two separate systems. This approach, although very simple, is not optimum as the pre-filtering stage and the SRF-PLL may have comparable dynamics. The aim of this paper is to develop a systematic and efficient approach to design the control parameters of a SRF-PLL with pre-filtering stage. To this end, the paper first optimizes the performance of the filtering stage in detection of the sequence components. The paper then proceeds to reduce the interaction between the filtering stage and SRF-PLL, which is achieved by employing a derivative-filtered proportional-integral-derivative controller as the loop filter (instead of the commonly adopted proportional-integral controller) and arranging a pole-zero cancellation. The suggested method is simple and efficient, and is applicable to the joint operation of different sequence separation techniques and the SRF-PLL. The effectiveness of the suggested design approach is confirmed through extensive experimental results.**

***Index Terms*—Loop filter, proportional-integral-derivative (PID) controller, synchronization, synchronous-reference-frame phase-locked loop (SRF-PLL).**

I. Introduction

THE three-phase synchronous-reference-frame phase-locked loop (SRF-PLL), also known as the dqPLL, is probably the most widely used synchronization technique in the three-phase power systems [1], [2]. The block diagram description of this PLL is shown in Fig. 1. In the SRF-PLL, the three-phase input voltages are transformed to the synchronous (*dq*) reference frame by applying the Clarke and subsequently the Park transformations. The *dq* reference frame angular position is then regulated using a feedback control loop, which forces v_q to zero in steady-state. Typically, a proportional-integral (PI) controller is used as the loop filter (LF) in this PLL, as it guarantees a zero steady-state phase-error in response to both phase jumps and frequency variations [2]. The SRF-PLL is able to achieve a very high bandwidth and, as a consequence, a very fast dynamic response when the grid voltage is clean and balanced. However, it fails to do so under distorted and/or unbalanced grid conditions: its bandwidth need to be reduced to improve the disturbance rejection capability.

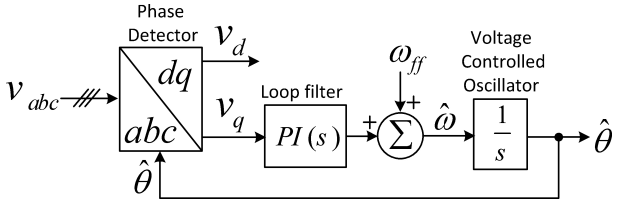

Fig. 1. Block diagram description of the conventional SRF-PLL.

To improve the performance of the SRF-PLL under unbalanced and/or distorted grid conditions, several approaches have been proposed in literature. These approaches are mainly based on adding specific filtering techniques either within the phase control loop of the PLL or prior to its input, here called the in-loop filtering and pre-filtering techniques, respectively.

The notch filters [3]-[4], the moving average filters [3], [5], and the repetitive regulators [6] are the common in-loop filtering techniques, which enable the PLL to achieve a correct estimation of the grid voltage phase and frequency under adverse grid conditions. However, they may not be attractive solutions in applications where accurate estimation of the fundamental frequency positive- and negative-sequence components (hereafter called the FFPS and FFNS components, respectively) are also essential.

The main advantage of the pre-filtering techniques over the in-loop filtering techniques is that they add the sequence detection capability to the PLL. Most often, the pre-filtering techniques can be understood as a set of two or more adaptive filters, working in a collaborative way, each of which is responsible for extracting a selected sequential component from the three-phase input signals. According to the reference frame that they are implemented on, they can be generally classified into three major categories, i.e., the synchronous (dq), the natural (abc), and the stationary ($\alpha\beta$) reference

Manuscript received December 11, 2012; revised April 5, 2013 and July 1, 2013; accepted for publication August 30, 2013. This work was supported in part by the Abadan Branch-Islamic Azad University.

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frames techniques. Some of the well-known techniques in each category are briefly discussed in the next section.

Control parameters design of the SRF-PLL with a pre-filtering stage, particularly when the filtering stage is implemented in either stationary or natural reference frame, is not a trivial task. The conventional way to deal with this problem is to neglect the interaction between the SRF-PLL and pre-filtering stage, and treat them as two separate systems [7], [8]. This approach, although very simple, is not optimum as the filtering stage and the SRF-PLL may have comparable dynamics. Another approach is to use the numerical optimization algorithms to design the control parameters [9]. This approach is time consuming; it requires a large number of simulation iterations. In [10], a design method is proposed which takes into consideration the dynamics of the SRF-PLL and pre-filtering stage simultaneously. This approach results in a better performance than the conventional design approaches.

In this paper, a systematic and efficient approach to design the control parameters of the SRF-PLL with a pre-filtering stage is proposed. Similar to [10], the suggested design approach takes into consideration the dynamics of the SRF-PLL and pre-filtering stage simultaneously. However, it reduces the dynamic interaction between these parts, which improves the whole system performance. This improvement is achieved by employing a derivative-filtered proportional-integral-derivative (PID) controller as the LF (instead of the commonly adopted PI controller) and arranging a pole-zero cancellation. The suggested method is simple and efficient, and is applicable to the joint operation of different sequence separation techniques and the SRF-PLL.

The suggested design approach is performed first on the multiple complex coefficient filters (MCCF) PLL [7], i.e., the SRF-PLL with the MCCF as the pre-filtering stage, and is then extended to other types of filtering techniques such as those presented in [8], [11]-[13].

II. A Brief Overview of Different Sequence Separation Techniques

One of the well-known approaches to extract the FFPS and FFNS components of the utility voltage in the synchronous reference frame is that proposed by Rodriguez *et al.* [14], [15]. This approach, referred to as the decouple double synchronous reference frame (DDSRF) technique, employs two synchronous reference frames rotating at the same angular speed, but in opposite directions, and a decoupling cross-feedback network to extract the FFPS and FFNS components. Another sequence detection technique in the synchronous reference frame is that proposed by Xiao *et al.* [16]. This approach, known as as the multiple reference frame (MRF) technique, utilizes the same idea of the DDSRF technique, except that it benefits from a more straightforward implementation.

The detection of the FFPS and FFNS components in the natural reference frame is mainly based on the symmetrical components theory in the time domain [17], i.e.,

$$\begin{bmatrix} v_a^+ \\ v_b^+ \\ v_c^+ \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} v_a^- \\ v_b^- \\ v_c^- \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & a^2 & a \\ a & 1 & a^2 \\ a^2 & a & 1 \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2}$$

where $a = e^{j120^\circ} = -1/2 + (\sqrt{3}/2)e^{j90^\circ}$, known as the 120° phase shift operator, can be implemented by employing an appropriate filter to generate the phase shift of 90°. Indeed, the main difference among the different sequence detection techniques in the natural reference frame typically lies in how the phase-shift of 90° is realized. Lee *et al.* [18] suggest to employ the all-pass filters (APFs) to generate the 90° phase-shifted version of each phase. The main drawback of this approach is that the APFs cannot block the distortions and harmonics. To overcome this drawback, Karimi-Ghartemani *et al.* [11] suggest to replace the APFs with the enhance PLLs (EPLLs). Each EPLL receives one phase of three-phase voltages, and adaptively extracts the fundamental and the 90° phase shifted version of it. Another approach is that proposed by Yazdani *et al.* [12], in which three adaptive notch filters (ANFs) are employed to extract the fundamental and the 90° phase-shifted version of the three phases.

The sequence detection techniques in the stationary reference frame are typically preferred to the synchronous and natural reference frame techniques, since they do not require the several reference frame transformations, and they operate on a two-phase system instead of a three-phase one. The dual second order generalized integrator (DSOGI) proposed by Rodriguez *et al.* [8] is among the existing well-known sequence detectors in the stationary reference frame. This technique works based on the theory of the symmetrical components in the stationary reference frame. Another successful technique is that proposed by Guo *et al.* [7], in which the MCCF are employed to extract the sequence components. The unique characteristic of the complex coefficient filters (CCFs) is that they can make the distinction between the negative and positive sequences for the same frequency. Another approach is a frequency adaptive discrete filter (FADF) which has been proposed by Jorge *et. al* [13]. The advantage of this technique over the DSOGI and MCCF techniques is its lower computational burden.

Several other sequence separation techniques can be found in [19]-[23].

III. MCCF-PLL

This section deals with the study of MCCF-PLL (i.e, the SRF-PLL with MCCF as its pre-filtering stage). The small-signal modelling of this PLL is also presented in this section.

A. Overview of MCCF-PLL

The complex filters are the key building blocks of the MCCF-PLL. So, the study is started with a brief review of these filters.

Although relatively new in electric power system applications, the complex filters have a long history of use in the field of communications [24]. These filters, contrary to the real filters, are not constraint to have the complex-conjugate

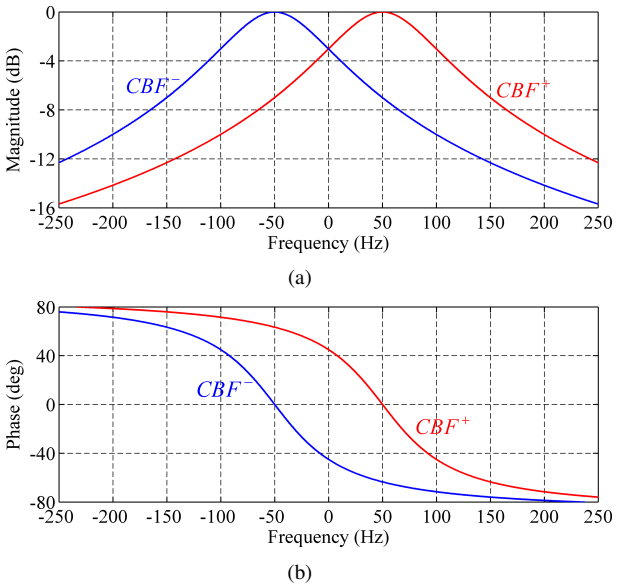


Fig. 2. Bode plots of first-order CBFs of (3) and (4). Parameters: $\omega_p = 2\pi 50$ rad/s and $\omega = 2\pi 50$ rad/s

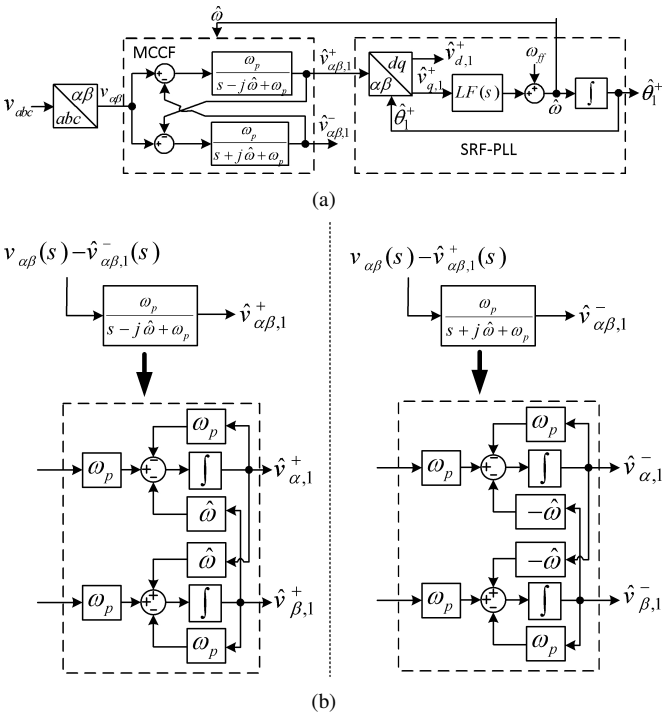


Fig. 3. (a) Block diagram description of MCCF-PLL. (b) implementation block diagram of the CBFs.

poles/zeros. Therefore, they may have an asymmetric frequency response around zero, which enables them to make distinction between negative and positive polarities (sequences) for the same frequency. For example, Fig. 2 shows the Bode plots of two first-order complex bandpass filters (CBFs) of the form

$$CBF^{+}(s) = \frac{\omega_p}{s - j\omega + \omega_p} \tag{3}$$

$$CBF^{-}(s) = \frac{\omega_p}{s + j\omega + \omega_p}. \tag{4}$$

In these plots, the response to negative frequencies can be interpreted as the response to the negative sequence input signal. As expected, the CBFs have asymmetric frequency responses with respect to 0 Hz: CBF^{+} (CBF^{-}) provides a unity gain with zero phase shift at the positive (negative) sequence fundamental frequency, while it provides a certain level of filtering at the same frequency of negative (positive) sequence.

Fig. 3(a) shows a simple block diagram description of the MCCF-PLL [7]. Here, for the sake of simplicity in the analysis, the MCCF is considered to be composed of only two CBFs tuned at the positive- and negative-sequence fundamental frequencies. The implementation block diagram of the CBFs are shown in Fig. 3(b). Notice that the complex operator "j" is realized using the cross-coupling between the $\alpha\beta$ axes.

The *two-modules* MCCF can provide accurate detection of the FFPS and FFNS components under unbalanced yet not distorted (or slightly distorted) grid conditions. However, it fails to do so under highly distorted grid conditions. In such a case, the performance of the MCCF can be simply improved by adding extra CBFs tuned at the harmonic frequencies. To extract the grid voltage phase and frequency, the extracted FFPS voltage vector by the MCCF, i.e., $\hat{v}^{+}_{\alpha\beta,1}$, is fed to the SRF-PLL. The estimated frequency $\hat{\omega}$ is then fed back to the MCCF to make it frequency adaptive.

B. Small-Signal Modeling of MCCF-PLL

From Fig. 3(a), the extracted FFPS and FFNS vectors in the $\alpha\beta$ reference frame can be expressed as

$$\hat{v}^{+}_{\alpha\beta,1}(s) = \overbrace{\frac{\omega_p}{s - j\hat{\omega} + \omega_p}}^{CBF^{+}(s)} \left(v_{\alpha\beta}(s) - \hat{v}^{-}_{\alpha\beta,1}(s)\right) \tag{5}$$

$$\hat{v}^{-}_{\alpha\beta,1}(s) = \underbrace{\frac{\omega_p}{s + j\hat{\omega} + \omega_p}}_{CBF^{-}(s)} \left(v_{\alpha\beta}(s) - \hat{v}^{+}_{\alpha\beta,1}(s)\right) \tag{6}$$

where $v_{\alpha\beta}(s) = v_{\alpha}(s) + jv_{\beta}(s)$, $\hat{v}^{+}_{\alpha\beta,1}(s) = \hat{v}^{+}_{\alpha,1}(s) + j\hat{v}^{+}_{\beta,1}(s)$, and $\hat{v}^{-}_{\alpha\beta,1}(s) = \hat{v}^{-}_{\alpha,1}(s) + j\hat{v}^{-}_{\beta,1}(s)$. Notice that, to obtain (5) and (6), the estimated frequency $\hat{\omega}$ was assumed to be constant. Substituting (5) into (6), and (6) into (5), and performing some mathematical manipulations, yield the complex transfer functions describing the dynamics of the MCCF as

$$\frac{\hat{v}^{+}_{\alpha\beta,1}(s)}{v_{\alpha\beta}(s)} = \overbrace{\frac{\omega_p}{s - j\hat{\omega} + \omega_p}}^{CBF^{+}(s)} \overbrace{\frac{(s + j\hat{\omega})(s - j\hat{\omega} + \omega_p)}{s^2 + 2\omega_p s + \hat{\omega}^2}}^{CNF^{-}(s)} \tag{7}$$

$$\frac{\hat{v}^{-}_{\alpha\beta,1}(s)}{v_{\alpha\beta}(s)} = \underbrace{\frac{\omega_p}{s + j\hat{\omega} + \omega_p}}_{CBF^{-}(s)} \underbrace{\frac{(s - j\hat{\omega})(s + j\hat{\omega} + \omega_p)}{s^2 + 2\omega_p s + \hat{\omega}^2}}_{CNF^{+}(s)} \tag{8}$$

The second term on the right hand side of (7) has a zero at $s = -j\hat{\omega}$, and provides a unity gain with a zero phase shift at $s = +j\hat{\omega}$. So, it can be considered as a complex notch

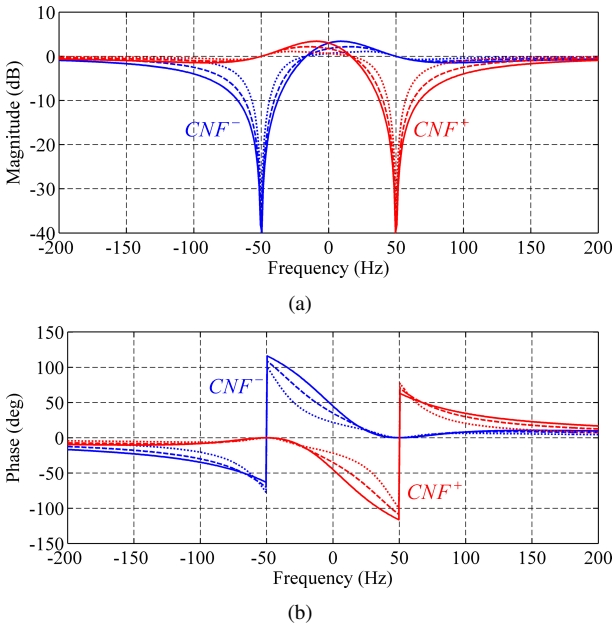


Fig. 4. Bode plots for CNFs for $\hat{\omega} = 2\pi 50$ rad/s and three different values of ω_p: $\omega_p = 0.4\hat{\omega}$ (dotted lines), $\omega_p = 0.7\hat{\omega}$ (dashed lines), and $\omega_p = \hat{\omega}$ (solid lines).

filter (CNF) with notch frequency at $-\hat{\omega}$, which completely blocks the FFNS input vector and does not affect the FFPS input vector. Similarly, the second term on the right hand side of (8) can be considered as a CNF with notch frequency at $+\hat{\omega}$. Fig. 4 shows the frequency response of these CNFs for $\hat{\omega} = 2\pi 50$ rad/s and three different values of ω_p: $\omega_p = 0.4\hat{\omega}$ (dotted lines), $\omega_p = 0.7\hat{\omega}$ (dashed lines), and $\omega_p = \hat{\omega}$ (solid lines). Notice that the width of the notches increase as ω_p increases.

To determine the MCCF-PLL small-signal model, the MCCF dynamics should be transferred to the *dq* coordinates. It is well-known that the coordinate transformation from the stationary reference frame to the synchronous reference frame corresponds to a frequency shift equal to the rotating speed of the synchronous reference frame (here, $\hat{\omega}$) in the frequency domain [25], [26]. Therefore, the complex transfer function (7) can be transformed to the synchronous reference frame as

$$\frac{\hat{v}^+_{dq,1}(s)}{v_{dq}(s)} = \frac{\hat{v}^+_{\alpha\beta,1}(s+j\hat{\omega})}{v_{\alpha\beta}(s+j\hat{\omega})} = \frac{\omega_p}{s+\omega_p}\frac{(s+j2\hat{\omega})(s+\omega_p)}{s^2+2(\omega_p+j\hat{\omega})s+j2\omega_p\hat{\omega}} \tag{9}$$

where $\hat{v}^+_{dq,1}(s) = \hat{v}^+_{d,1}(s) + j\hat{v}^+_{q,1}(s)$, and $v_{dq}(s) = v_d(s) + jv_q(s)$.

The second term on the right hand side of (9) is a CNF with notch frequency at $-2\hat{\omega}$. This term complicates the design procedure. So, the effects of this term is neglected, and the transfer function (9) is approximated by

$$\frac{\hat{v}^+_{dq,1}(s)}{v_{dq}(s)} \approx \frac{\omega_p}{s+\omega_p}. \tag{10}$$

The accuracy of this approximation is evaluated in Fig. 5. In this figure, the solid lines show the frequency response of the complex transfer function (9), and the dashed lines show the frequency response of the approximate transfer function (10). As shown, the accuracy of the approximation depends on the value of ω_p, i.e., the lower the value of ω_p, the more accurate the approximation.

Here, the q-axis component is the voltage of interest because, during locked conditions, it provides the phase-error information in the form [27]

$$v_q(t) \approx V_1^+ \underbrace{(\theta_1^+ - \hat{\theta}_1^+)}_{\theta_e} + D(t) \;\Rightarrow\; v_q(s) \approx V_1^+\theta_e(s) + D(s) \tag{11}$$

where V_1^+ (θ_1^+) is the amplitude (angle) of the FFPS component of the grid voltage, D represents the disturbance terms, and $\hat{}$ denotes the estimated quantity.

By substituting (11) into (10), $\hat{v}^+_{q,1}$, which is the LF input signal, can be obtained as

$$\hat{v}^+_{q,1}(s) \approx \frac{\omega_p}{s+\omega_p} v_q(s) \approx \frac{\omega_p}{s+\omega_p}\left(V_1^+\theta_e(s) + D(s)\right). \tag{12}$$

Using (12) and Fig. 3(a), the small-signal model of the MCCF-PLL can be obtained as shown in Fig. 6. Accuracy of this model will be examined later.

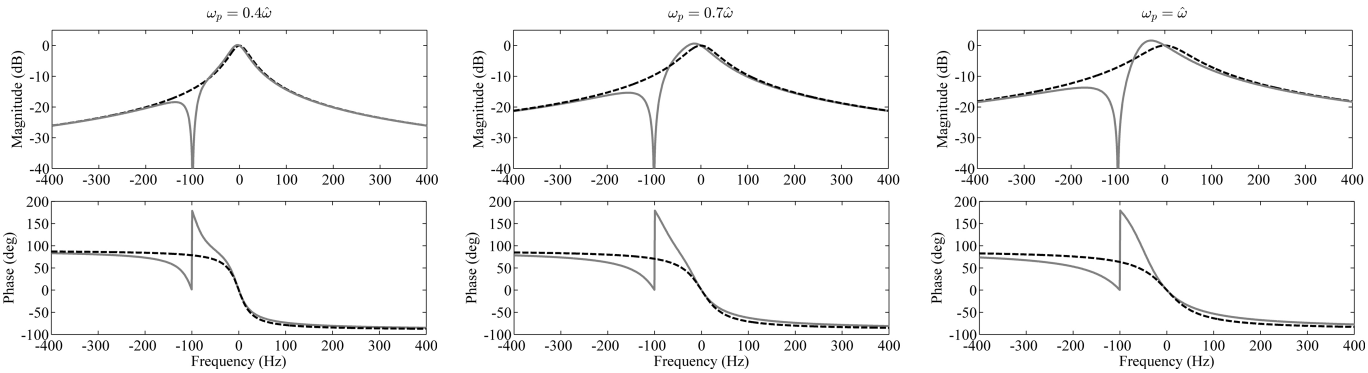


Fig. 5. Frequency responses of the transfer function (9) (solid line) and the approximate transfer function (10) (dashed line) for $\hat{\omega} = 2\pi 50$ rad/s and different values of ω_p.

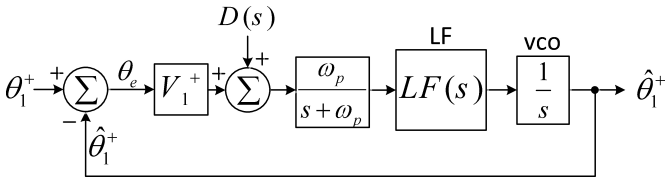


Fig. 6. Small-signal model of the MCCF-PLL.

IV. Proposed Design Method

A. Adjustment of MCCF Parameter

The first step of the suggested design procedure is to optimize the performance of the MCCF in detecting the sequence components. In this stage, the grid frequency is set to its nominal value (i.e., $\omega = \omega_{ff}$), and the effects of variation of ω_p on the dynamic performance of the MCCF is studied by simulation results.

Fig. 7 shows the dynamic performance of the MCCF in extraction of the sequence components when the grid voltage undergoes an unbalanced voltage sag. It can be observed that a high value of ω_p makes the dynamic response oscillatory, while a low value makes it slow and damped. Based on these plots, it sounds reasonable to set ω_p equal to $0.707\omega_{ff}$, as this value makes the dynamic response fast and well-damped.

This selection can also be made using the complex transfer functions describing the dynamics of MCCF, i.e., (7) and (8). These transfer functions can be simplified to

$$\frac{\hat{v}^{+}_{\alpha\beta,1}(s)}{v_{\alpha\beta}(s)} = \frac{\omega_p(s+j\hat{\omega})}{s^2 + \underbrace{2\omega_p}_{2\zeta\omega_n}\, s + \underbrace{\hat{\omega}^2}_{\omega_n^2}} \tag{13}$$

$$\frac{\hat{v}^{-}_{\alpha\beta,1}(s)}{v_{\alpha\beta}(s)} = \frac{\omega_p(s-j\hat{\omega})}{s^2 + \underbrace{2\omega_p}_{2\zeta\omega_n}\, s + \underbrace{\hat{\omega}^2}_{\omega_n^2}}. \tag{14}$$

Notice that (13) and (14) are similar to a standard second order transfer function with the natural frequency of $\hat{\omega}$ and the damping ratio of $\omega_p/\hat{\omega}$. It is well known that the best tradeoff between the settling time and the overshoot is obtained using the damping ratio of 0.707. Therefore, as already shown using simulation results, $\omega_p = 0.707\hat{\omega}$ is the optimum choice.

B. LF Selection

Once the optimum value of ω_p is determined, the next step is to select an appropriate controller as the LF.

In most applications, the PI controller is selected as the LF of the PLL. However, it may not be a suitable choice in our case. The reason is that to compensate the phase delay caused by the MCCF (the MCCF dynamics were modeled by a first order low pass filter (LPF) with cutoff frequency of ω_p in the forward path of the PLL small-signal model) using a PI type LF, the gain crossover frequency ω_c should be sufficiently lower than the cutoff frequency ω_p [10]. As the selected value for ω_p is a rather small value in our case, the crossover frequency will be very small, which slows down the dynamic performance of the PLL. Therefore, in this paper, using a PID-type LF (instead of the PI-type LF) is recommended. Notice

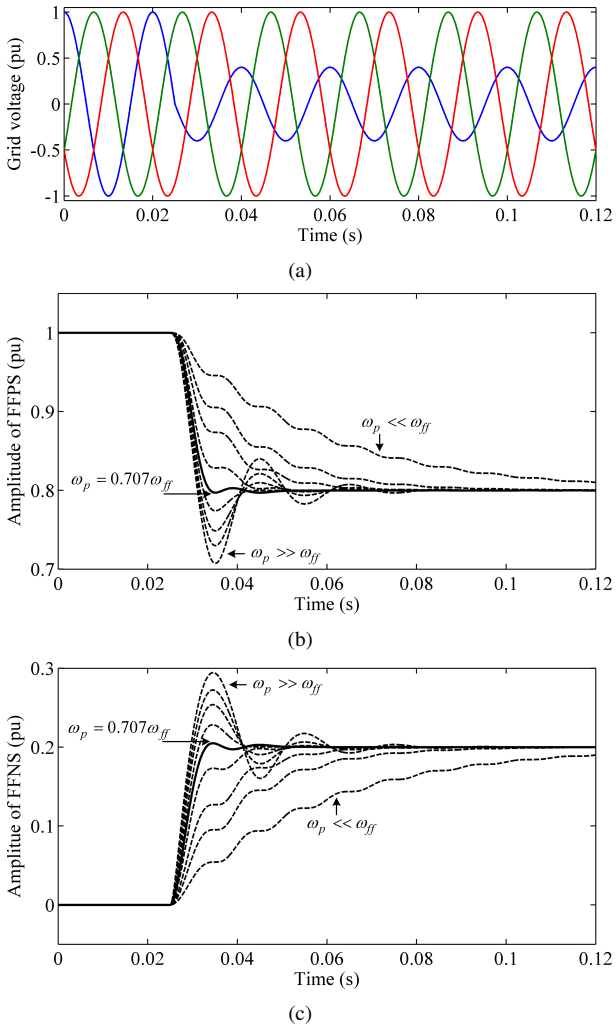


Fig. 7. Dynamic performance of the MCCF in estimation of the sequence components. (a) grid voltage, (b) amplitude of FFPS component, and (c) amplitude of FFNS component.

that the PID-type LF provides an additional degree of freedom which enables the designer to compensate the phase delay caused by the MCCF without reducing the PLL bandwidth.

The transfer function of the PID-type LF is considered to be of the form

$$G_{PID}(s) = k_p \frac{1+\tau_i s}{\tau_i s} \frac{1+\tau_d s}{1+DFF\tau_d s} \tag{15}$$

where k_p is the proportional gain, and τ_i and τ_d are the integral and derivative time constants, respectively. The term $1 + DFF\tau_d s$ in the denominator produces a high frequency pole in order to filter the derivative action of the PID controller. For this reason, it is referred to as the derivative filter, and DFF ($DFF < 1$) denotes the derivative filter factor. Notice that the higher the value of DFF, the higher the filtering capability of the derivative filter will be.

C. Adjustment of LF Parameters

The aim of this section is to design the LF parameters, i.e., k_p, τ_i, τ_d, and DFF, such that the phase delay caused by the MCCF is compensated and a fast and smooth transient

response is achieved. During the design procedure, it should be remembered that there is a CNF which the small-signal model does not include it [see (9)]. Therefore, to ensure the stability, the MCCF-PLL bandwidth should be sufficiently smaller than the notch frequency 2ω, i.e., $2\pi 100$ rad/s in a 50 Hz system.

Considering the LF transfer function as (15), the open-loop transfer function of the MCCF-PLL can be obtained, from the small-signal model of Fig. 6, as

$$G_{ol}(s) = V_1^+ \underbrace{\frac{\omega_p}{s+\omega_p}}_{\text{MCCF}} \times \underbrace{k_p \frac{1+\tau_i s}{\tau_i s} \frac{1+\tau_d s}{1+DFF\tau_d s}}_{\text{LF}} \times \underbrace{\frac{1}{s}}_{\text{VCO}}. \tag{16}$$

In order to compensate the phase delay caused by the MCCF, a pole-zero cancelation is arranged. This cancelation is obtained by selecting the derivative time constant equal to inverse of the cutoff frequency ω_p, i.e., $\tau_d = 1/\omega_p = 1/(0.707\omega_{ff})$. With this selection, and considering that the derivative filter (which corresponds to a high frequency pole) has a relatively small effect on the PLL dynamics, the open-loop transfer function (16) can be simplified to

$$G_{ol}(s) \approx V_1^+ k_p \frac{1+\tau_i s}{\tau_i s} \frac{1}{s}. \tag{17}$$

Using (17), the PLL closed loop transfer function can be obtained as

$$G_{cl}(s) = \frac{G_{ol}(s)}{1+G_{ol}(s)} \approx \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{18}$$

where $\omega_n = \sqrt{\frac{V_1^+ k_p}{\tau_i}}$ and $\zeta = \frac{1}{2}\sqrt{V_1^+ k_p \tau_i}$.

The closed-loop transfer function of (18) is a standard second-order transfer function having a zero, which countless publications cover its properties and discuss its design aspects (see for example [2], [28]). Typically, a damping ratio of 0.707, and selecting the natural frequency ω_n as a trade-off between the bandwidth and the filtering capability are recommended in literature. Following this design procedure, and considering that the MCCF-PLL bandwidth should be sufficiently smaller than 2ω, we select $\zeta = 0.707$ and $\omega_n = 2\pi 20$ rad/s, which yields k_p and τ_i as follows

$$\begin{cases} \tau_i = \frac{2\xi}{\omega_n} = 0.01125 \\ k_p = \frac{2\xi\omega_n}{V_1^+} = 0.5727 \end{cases} \tag{19}$$

Notice that, for the sake of consistency with [7], V_1^+ was considered to be $380\sqrt{\frac{2}{3}}$ V. The DFF is also set to 0.2 to provide a relatively high degree of filtering.

D. Accuracy of Small-Signal Model

In this section, the accuracy of the derived small-signal model (Fig. 6) is shown. To achieve this goal, Figs. 8(a) and (b) provide a performance comparison between the MCCF-PLL (solid black line) and its small-signal model (dashed gray line) under a phase angle-jump of $+10°$ and a frequency step change of $+1$ Hz, respectively. The designed values of control parameters are used in this comparison. As shown, the model is accurate enough in predicting the PLL behavior. It should be noted that the accuracy small-signal model decreases with increasing the MCCF-PLL bandwidth. This error is mainly due to the approximation made during the modeling procedure, i.e., neglecting the CNF effect.

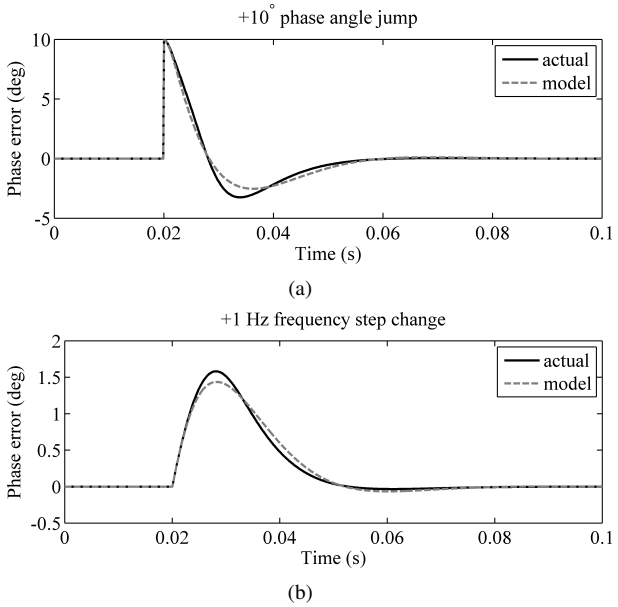


Fig. 8. Performance comparison between the MCCF-PLL and its small-signal model under (a) a phase angle-jump of $+10°$, and (b) a frequency step change of $+1$ Hz. Parameters: $V_1^+ = 380\sqrt{\frac{2}{3}}$ V, $\omega_{ff} = 2\pi 50\,\text{rad/s}$, $k_p = 0.5727, \tau_i = 0.01125$, $\tau_d = 1/\omega_p = 1/(0.707\omega_{ff})$, and $DFF = 0.2$.

E. Summary

The proposed design method can be summarized as follows.

1) Select $\omega_p = 0.707\omega_{ff}$.
2) Consider the LF as a derivative-filtered PID type controller. Select $DFF = 0.2$.
3) Select $\tau_d = 1/\omega_p$.
4) Define $k_p = 2\zeta\omega_n/V_1^+$, and $\tau_i = 2\zeta/\omega_n$.
5) Select $\zeta = 0.707$.
6) Select ω_n as a tradeoff between the bandwidth and the filtering capability. It should be noticed that the value of ω_n cannot be arbitrary increased, as it may cause stability problems. $\omega_n = 2\pi 20$ rad/s is recommended in this paper.
7) Calculate k_p and τ_i from the definition of step 4.

V. Application of the Proposed Method to Other Types of Filtering Techniques

There is a variety of sequence filtering techniques that can be used instead of the MCCF as the pre-filtering stage of the SRF-PLL. It is shown in this section that some of these techniques are mathematically equivalent to the MCCF. Therefore, when they are used as the pre-filtering stage of the SRF-PLL, the obtained small-signal model for the MCCF-PLL, and consequently, the proposed design method are valid for them as well.

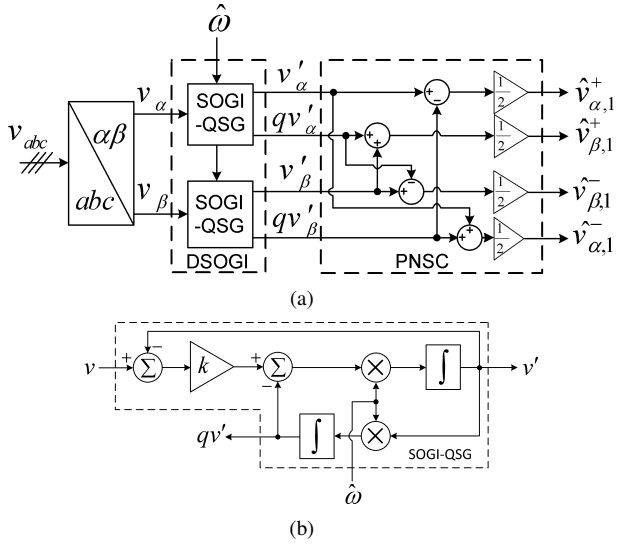


Fig. 9. (a) Block diagram description of the DSOGI-PNSC. (b) implementation of the SOGI-QSG block.

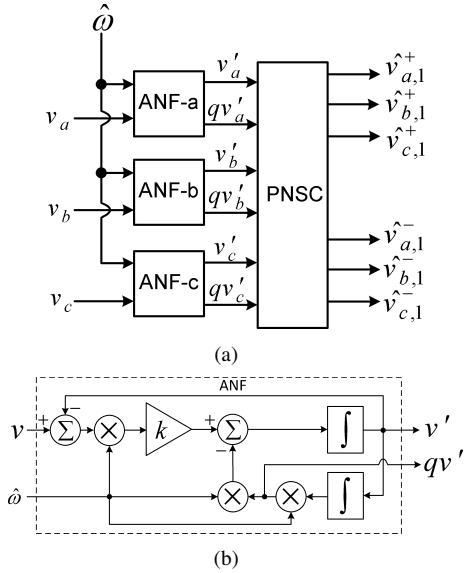


Fig. 10. (a) Block diagram description of the ANF-PNSC. (b) structure of the ANF.

A. DSOGI-PNSC

Fig. 9(a) shows the block diagram description of the DSOGI-PNSC, in which two second order generalized integrators (SOGIs) configured as the quadrature signal generator (QSG) along with a positive/negative sequence calculator (PNSC) are used to extract the FFPS and FFNS components of the grid voltage [8]. The implementation of the SOGI-QSG block is shown in Fig. 9(b), where k is the damping factor, and v' and qv' are the filtered direct and quadrature versions of the input signal v, respectively. The characteristic equations of the SOGI-QSG are

$$D(s) = \frac{v'(s)}{v(s)} = \frac{k\hat{\omega}s}{s^2 + k\hat{\omega}s + \hat{\omega}^2} \tag{20}$$

$$Q(s) = \frac{qv'(s)}{v(s)} = \frac{k\hat{\omega}^2}{s^2 + k\hat{\omega}s + \hat{\omega}^2}. \tag{21}$$

In this approach, the $\alpha\beta$ coordinate voltages, i.e. v_α and v_β, are passed through two SOGI-QSG blocks to obtain the filtered direct and quadrature versions of them, i.e. v'_α, v'_β, qv'_α, and qv'_β. These signals are then applied to the PNSC to calculate the FFPS and FFNS voltage vectors according to the symmetrical components theory in the stationary reference frame, as follows:

$$\begin{bmatrix} \hat{v}^+_{\alpha,1} \\ \hat{v}^+_{\beta,1} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} v'_\alpha - qv'_\beta \\ v'_\beta + qv'_\alpha \end{bmatrix} \tag{22}$$

$$\begin{bmatrix} \hat{v}^-_{\alpha,1} \\ \hat{v}^-_{\beta,1} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} v'_\alpha + qv'_\beta \\ v'_\beta - qv'_\alpha \end{bmatrix}. \tag{23}$$

According to (22) and (23), and considering the characteristic Eqs. of the SOGI-QSG, i.e. (20) and (21), the matrix Eqs. describing the input-output relations of the DSOGI-PNSC can be obtained as

$$\begin{bmatrix} \hat{v}^+_{\alpha,1}(s) \\ \hat{v}^+_{\beta,1}(s) \end{bmatrix} = \frac{1}{2}\frac{k\hat{\omega}}{s^2 + k\hat{\omega}s + \hat{\omega}^2}\begin{bmatrix} s & -\hat{\omega} \\ \hat{\omega} & s \end{bmatrix}\begin{bmatrix} v_\alpha(s) \\ v_\beta(s) \end{bmatrix} \tag{24}$$

$$\begin{bmatrix} \hat{v}^-_{\alpha,1}(s) \\ \hat{v}^-_{\beta,1}(s) \end{bmatrix} = \frac{1}{2}\frac{k\hat{\omega}}{s^2 + k\hat{\omega}s + \hat{\omega}^2}\begin{bmatrix} s & \hat{\omega} \\ -\hat{\omega} & s \end{bmatrix}\begin{bmatrix} v_\alpha(s) \\ v_\beta(s) \end{bmatrix} \tag{25}$$

These matrix Eqs. can be expressed in complex notation as

$$\frac{\hat{v}^+_{\alpha\beta,1}(s)}{v_{\alpha\beta}(s)} = \frac{1}{2}\frac{k\hat{\omega}(s + j\hat{\omega})}{s^2 + k\hat{\omega}s + \hat{\omega}^2} \tag{26}$$

$$\frac{\hat{v}^-_{\alpha\beta,1}(s)}{v_{\alpha\beta}(s)} = \frac{1}{2}\frac{k\hat{\omega}(s - j\hat{\omega})}{s^2 + k\hat{\omega}s + \hat{\omega}^2} \tag{27}$$

Notice that, for $\omega_p = k\hat{\omega}/2$, these complex transfer functions are the same as those of the MCCF, i.e. (13) and (14). Therefore, it can be concluded that, the DSOGI-PNSC and two-module MCCF are mathematically equivalent systems.

B. ANF-PNSC

Fig. 10(a) shows the block diagram description of the ANF-PNSC, in which three ANFs along with a PNSC in the natural reference frame are used to extract the FFPS and FFNS components of the grid voltage [12]. The structure of the ANF is shown in Fig. 10(b).

From Fig. 10(b), the characteristic transfer function describing the dynamics of the ANF can be obtained as

$$D'(s) = \frac{v'(s)}{v(s)} = \frac{k\hat{\omega}s}{s^2 + k\hat{\omega}s + \hat{\omega}^2} \tag{28}$$

$$Q'(s) = \frac{qv'(s)}{v(s)} = \frac{k\hat{\omega}^2}{s^2 + k\hat{\omega}s + \hat{\omega}^2} \tag{29}$$

which are the same as those of the SOGI-QSG, i.e. (20) and (21). On the other hand, the PNSC in Fig. 10(a) is the natural reference frame equivalent of the PNSC in Fig. 9(a). Thus, it can be concluded that, the DSOGI-PNSC and the ANF-PNSC (and as a result, the MCCF and the ANF-PNSC) are mathematically equivalent systems, which perform the same function on the different reference frames.

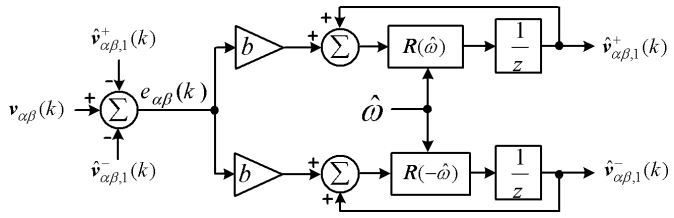


Fig. 11. Block diagram description of the 2-section FADF.

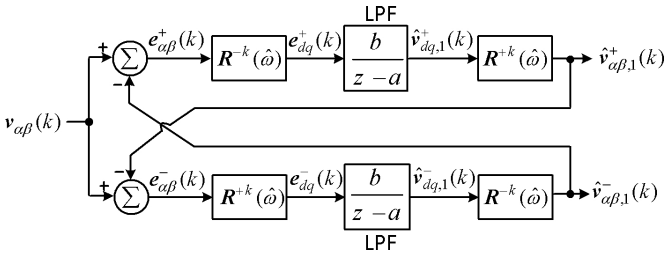


Fig. 12. The synchronous reference frame equivalent of the FDAF.

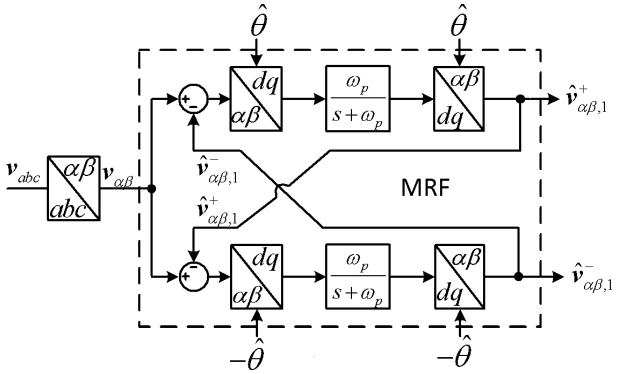


Fig. 13. Block diagram description of the MRF technique.

C. FADF

Fig. 11 shows the block diagram description of the 2-section FADF proposed by Jorge *et al.* [13], in which

$$b = 1 - e^{-\omega_p T_s} \tag{30}$$

$$\boldsymbol{R}(\hat{\omega}) = \begin{bmatrix} \cos(\hat{\omega}T_s) & -\sin(\hat{\omega}T_s) \\ \sin(\hat{\omega}T_s) & \cos(\hat{\omega}T_s) \end{bmatrix} \tag{31}$$

where T_s is the sampling time, ω_p is the design constant, and $\boldsymbol{R}(\hat{\omega})$ is a rotation matrix with rotation angle of $\hat{\omega}T_s$. Notice that $\boldsymbol{R}(-\hat{\omega}) = \boldsymbol{R}^{-1}(\hat{\omega})$.

From Fig. 11, the discrete-time equations describing the dynamics of the FADF can be obtained as

$$\hat{\boldsymbol{v}}^+_{\alpha\beta,1}(k+1) = \boldsymbol{R}(\hat{\omega})\left[\hat{\boldsymbol{v}}^+_{\alpha\beta,1}(k) + b\boldsymbol{e}_{\alpha\beta}(k)\right] \tag{32}$$

$$\hat{\boldsymbol{v}}^-_{\alpha\beta,1}(k+1) = \boldsymbol{R}(-\hat{\omega})\left[\hat{\boldsymbol{v}}^-_{\alpha\beta,1}(k) + b\boldsymbol{e}_{\alpha\beta}(k)\right]. \tag{33}$$

where $\hat{\boldsymbol{v}}^+_{\alpha\beta,1}(k) = [\hat{\boldsymbol{v}}^+_{\alpha,1}(k), \hat{\boldsymbol{v}}^+_{\beta,1}(k)]^T$, $\hat{\boldsymbol{v}}^-_{\alpha\beta,1}(k) = [\hat{\boldsymbol{v}}^-_{\alpha,1}(k), \hat{\boldsymbol{v}}^-_{\beta,1}(k)]^T$, and $\boldsymbol{e}_{\alpha\beta}(k) = [\boldsymbol{e}_{\alpha}(k), \boldsymbol{e}_{\beta}(k)]^T$. Substituting $\boldsymbol{e}_{\alpha\beta}(k) = \boldsymbol{v}_{\alpha\beta}(k) - \hat{\boldsymbol{v}}^+_{\alpha\beta,1}(k) - \hat{\boldsymbol{v}}^-_{\alpha\beta,1}(k)$ into (32) and (33), and performing some simple mathematical manipulations yields

$$\hat{\boldsymbol{v}}^+_{\alpha\beta,1}(k+1) = \boldsymbol{R}(\hat{\omega})\left[a\hat{\boldsymbol{v}}^+_{\alpha\beta,1}(k) + b\boldsymbol{e}^+_{\alpha\beta}(k)\right] \tag{34}$$

$$\hat{\boldsymbol{v}}^-_{\alpha\beta,1}(k+1) = \boldsymbol{R}(-\hat{\omega})\left[a\hat{\boldsymbol{v}}^-_{\alpha\beta,1}(k) + b\boldsymbol{e}^-_{\alpha\beta}(k)\right] \tag{35}$$

where $a = 1 - b = e^{-\omega_p T_s}$, $\boldsymbol{e}^+_{\alpha\beta}(k) = \boldsymbol{v}_{\alpha\beta}(k) - \hat{\boldsymbol{v}}^-_{\alpha\beta,1}(k)$, and $\boldsymbol{e}^-_{\alpha\beta}(k) = \boldsymbol{v}_{\alpha\beta}(k) - \hat{\boldsymbol{v}}^+_{\alpha\beta,1}(k)$.

Multiplying both sides of (34) and (35) with $\boldsymbol{R}^{-(k+1)}(\hat{\omega})$ and $\boldsymbol{R}^{+(k+1)}(\hat{\omega})$, respectively, yields

$$\underbrace{\boldsymbol{R}^{-(k+1)}(\hat{\omega})\hat{\boldsymbol{v}}^+_{\alpha\beta,1}(k+1)}_{\hat{\boldsymbol{v}}^+_{dq,1}(k+1)} = a\underbrace{\boldsymbol{R}^{-k}(\hat{\omega})\hat{\boldsymbol{v}}^+_{\alpha\beta,1}(k)}_{\hat{\boldsymbol{v}}^+_{dq,1}(k)} + b\underbrace{\boldsymbol{R}^{-k}(\hat{\omega})\boldsymbol{e}^+_{\alpha\beta}(k)}_{\boldsymbol{e}^+_{dq}(k)} \tag{36}$$

$$\underbrace{\boldsymbol{R}^{+(k+1)}(\hat{\omega})\hat{\boldsymbol{v}}^-_{\alpha\beta,1}(k+1)}_{\hat{\boldsymbol{v}}^-_{dq,1}(k+1)} = a\underbrace{\boldsymbol{R}^{+k}(\hat{\omega})\hat{\boldsymbol{v}}^-_{\alpha\beta,1}(k)}_{\hat{\boldsymbol{v}}^-_{dq,1}(k)} + b\underbrace{\boldsymbol{R}^{+k}(\hat{\omega})\boldsymbol{e}^-_{\alpha\beta}(k)}_{\boldsymbol{e}^-_{dq}(k)} \tag{37}$$

which can be rewritten as

$$\hat{\boldsymbol{v}}^+_{dq,1}(k) = \frac{b}{z-a}\boldsymbol{e}^+_{dq}(k) \tag{38}$$

$$\hat{\boldsymbol{v}}^-_{dq,1}(k) = \frac{b}{z-a}\boldsymbol{e}^-_{dq}(k). \tag{39}$$

Notice that $b/(z-a)$ is the zero-order hold (ZOH) discrete-time equivalent of continuous filter $LPF(s) = \omega_p/(s+\omega_p)$ [13].

According to (36)-(39), the synchronous reference frame equivalent of the FDAF can be obtained as shown in Fig. 12, which is the discrete-time equivalent of the MRF structure (see Fig. 13) [16]. Considering that the MRF and MCCF are two equivalent systems (see [10] for proof), it can be concluded that the FADF and MCCF are also equivalent.

VI. Experimental Results

In this section, the effectiveness of the suggested design approach is confirmed through extensive experimental studies on the DSOGI-PLL and MCCF-PLL. For each PLL, the obtained results using the conventional design approaches [7], [8] are also shown, and compared with those obtained using the suggested strategy. The experiments are based on a TMS320F28335 digital signal controller (DSC) from the Texas instruments. Throughout the experiments, the nominal frequency is set to $2\pi 50$ rad/s, and the sampling frequency is fixed to 10 kHz.

In order to ensure the discrete accuracy, and to avoid an algebraic loop, the third-order Adams-Bashforth method [7], [30] is used to approximate the continuous-time integrals in both DSOGI and MCCF structures, i.e.,

$$\frac{1}{s} \quad \Leftrightarrow \quad \frac{T_s}{12}\frac{23z^{-1} - 16z^{-2} + 5z^{-3}}{1 - z^{-1}}. \tag{40}$$

The control parameters are summarized in Table I.

In experimental verifications, the three-phase input signals are generated internally in DSP. They are then fed to the

TABLE I
CONTROL PARAMETERS.

MCCF-PLL		DSOGI-PLL	
suggested	**conventional [7]**	**suggested**	**conventional [8]**
$V_1^+ = 380\sqrt{2/3}$ V	$V_1^+ = 380\sqrt{2/3}$ V	$V_1^+ = 100$ V	$V_1^+ = 100$ V
$\omega_p = 2\pi 35.35$ rad/s	$\omega_p = 2\pi 50$ rad/s	$k = \sqrt{2}$	$k = \sqrt{2}$
$k_p = 0.5727$	$k_p = 0.455$	$k_p = 1.777$	$k_p = 2.22$
$\tau_i = 0.01125$ s	$k_i = 32$	$\tau_i = 0.01125$ s	$k_i = 61.69$
$\tau_d = 4.502 \times 10^{-3}$ s		$\tau_d = 4.502 \times 10^{-3}$ s	
$DFF = 0.2$		$DFF = 0.2$	

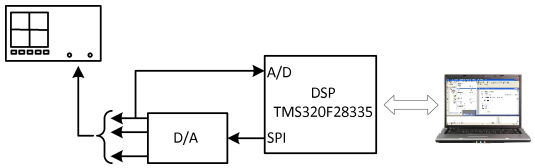


Fig. 14. Experimental setup.

external digital-to-analogue (D/A) converter via the serial peripheral interfaces (SPI) to generate the analog test signals. These signals are acquired by the DSP to perform the PLL algorithms [see Fig. 14].

A. Frequency Step Change

Figs. 15(a) and (b) show the experimental results for the MCCF-PLL and DSOGI-PLL, respectively, when the grid voltage undergoes a frequency step change of +5 Hz. As shown, the suggested design approach provides a more damped transient response with a shorter settling time for both PLLs. The 2% settling time is about 1.75 cycles of the nominal frequency for both PLLs using the suggested design approach, while it is about 2.5 and 2.75 cycles for the MCCF-PLL and the DSOGI-PLL, respectively, using the conventional design approach. The frequency overshoot is about 32% for both PLLs using the suggested design approach, while it is about 50% and 42% for the MCCF-PLL and the DSOGI-PLL, respectively, using the conventional design approach.

B. Phase-Angle Jump

Figs. 16(a) and (b) show the experimental results for the MCCF-PLL and the DSOGI-PLL, respectively, when the grid voltage undergoes a phase-angle jump of $+40°$. Again, the suggested design approach provides a more damped transient response with a shorter settling time for both PLLs. The 2% settling time is about 1.75 cycles of the nominal frequency for both PLLs using the suggested design approach, while it is about 2.5 and 2.75 cycles for the MCCF-PLL and the DSOGI-PLL, respectively, using the conventional design approach. The phase overshoot is about 30% and 28% for the MCCF-PLL and the DSOGI-PLL, respectively, using the suggested design approach, while it is about 47% and 36% for these PLLs using the conventional design approach.

C. Unbalanced and Distorted Grid Condition

Fig. 17 evaluates the detection accuracy of the DSOGI-PLL and the MCCF-PLL under an unbalanced and harmonically distorted grid condition ($\vec{V}_1^+ = 1\angle 0°$, $\vec{V}_1^- = 0.1\angle -90°$, $\vec{V}_5^- = 0.05\angle -90°$, and $\vec{V}_7^+ = 0.05\angle 0°$). As shown, in terms of the amplitude detection accuracy, both approaches yield good results (see Table II for details). In terms of the phase detection accuracy, the obtained results using the suggested design approach are not as good as those obtained with the conventional design approach, however they are acceptable for most applications. Nevertheless, if the application requires, the detection accuracy can be improved by adding extra CBFs and SOGIs (tuned at the harmonic frequencies) to the two-module MCCF and DSOGI-PNSC, respectively.

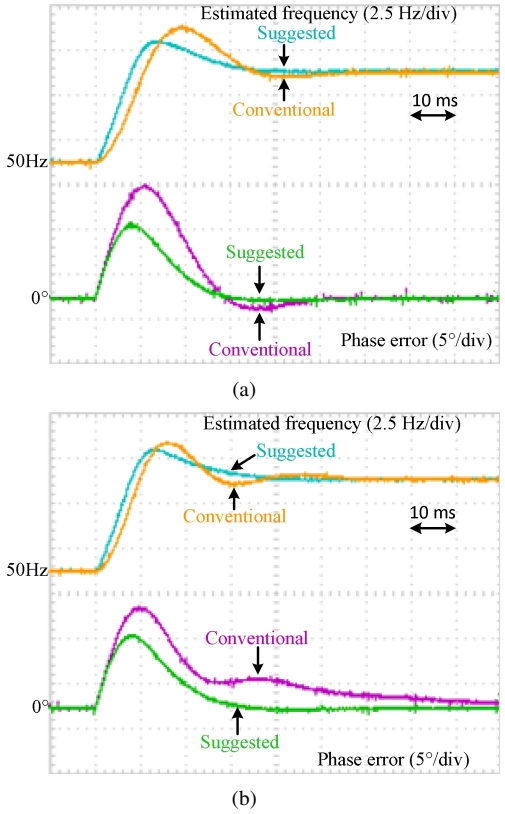
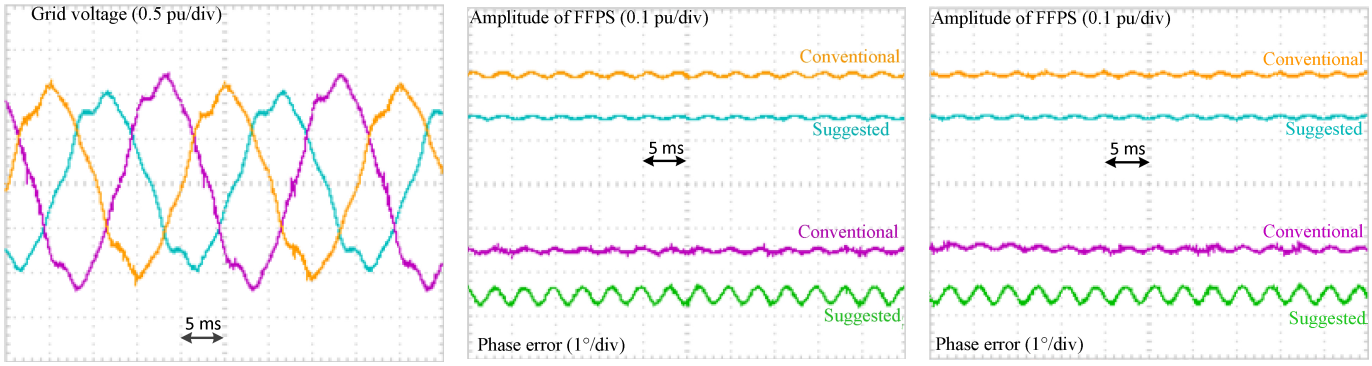


Fig. 15. (a) MCCF-PLL, and (b) DSOGI-PLL performances when the grid voltage undergoes a frequency step change of +5 Hz.

The obtained results along with a comparison between the phase margin of the PLLs using the suggested and the conventional design approaches are summarized in Table II. Notice that the phase margin of the PLLs are obtained using the small-signal model of Fig. 6.

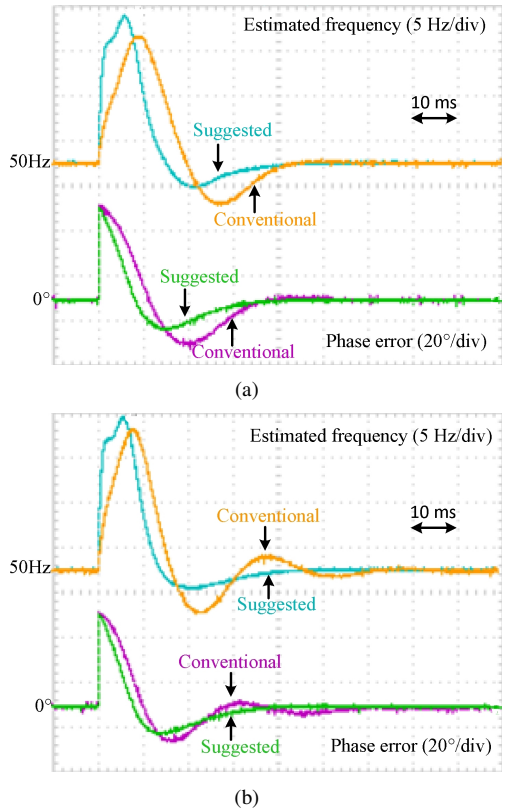
VII. CONCLUSION

In this paper, a systematic design approach for the SRF-PLL with pre-filtering stage was proposed. The suggested design approach was first developed for the MCCF-PLL (i.e., the SRF-PLL with MCCF as the pre-filtering stage), and then extended to the joint operation of several other sequence separation techniques (i.e., DSOGI-PNSC, ANF-PNSC, FADF, and EPLL-PNSC) and the SRF-PLL. The effectiveness of the suggested design approach was confirmed through extensive experimental results.



(a) (b) (c)

Fig. 17. Experimental results under unbalanced and harmonically distorted grid conditions. (a) Input voltages. (b) MCCF-PLL. (c) DSOGI-PLL.



(a)

(b)

Fig. 16. (a) MCCF-PLL, and (b) DSOGI-PLL performances when the grid voltage undergoes a phase-angle jump of $+40°$.

TABLE II
COMPARISON SUMMARY.

	MCCF-PLL suggested / conventional	DSOGI-PLL suggested / conventional
+5 Hz frequency jump		
2% settling time	≈ 1.75 cycles / ≈ 2.5 cycles	≈ 1.75 cycles / ≈ 2.75 cycles
frequency overshoot	≈ 32% / ≈ 50%	≈ 32% / ≈ 42%
+40° phase-angle jump		
2% settling time	≈ 1.75 cycles / ≈ 2.5 cycles	≈ 1.75 cycles / ≈ 2.75 cycles
phase overshoot	≈ 30% / ≈ 47%	≈ 28% / ≈ 36%
Unbalanced and distorted grid condition		
peak-to-peak FFPS amplitude error	≈ 0.015 pu / ≈ 0.02 pu	≈ 0.015 pu / ≈ 0.015 pu
peak-to-peak phase error	≈ 0.4° / ≈ 0.1°	≈ 0.4° / ≈ 0.1°
phase margin	55.4° / 39.3°	55.4° / 42.6°

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