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Abstract—Designing an effective phase-locked loop (PLL) for three-phase applications is the objective of this paper. The designed PLL structure is able to provide an accurate estimation of grid voltage frequency and phase even in the presence of all harmonic components of both positive and negative sequences and dc offset in its input. It addition to offer a high disturbance rejection capability, the suggested PLL structure has a fast transient response and provides a settling time of around two cycles of fundamental frequency. The effectiveness of suggested PLL structure is confirmed using numerical results.

Index Terms—Delay signal cancelation (DSC), moving average filter (MAF), phase detection, phase-locked loop (PLL).

I. INTRODUCTION

The phase-locked loop (PLL) is a circuit or algorithm with three distinct parts, namely the phase detector, the loop filter (LF), and the voltage controlled oscillator, that adjusts the phase of its output signal to follow the phase of its input [1]. The great benefits of PLL such as its robustness and ease of implementation has made it a suitable choice for synchronization and control purposes in grid connected applications [2]-[5].

To ensure a zero average steady-state phase error in the presence of frequency drifts, PLLs often employ a proportional-integral (PI) controller as the LF [6]. The PI controller, however, has a limited capability to mitigate the disturbance components in the PLL control loop. To further improve the disturbance rejection ability of PLLs, cascading additional filters such as the moving average filter (MAF) [7], the *dq*-frame cascaded delayed signal cancellation (DSC) [8], [9], [10], and the notch filters [11] with the PI controller is sometimes recommended. These filters, however, increase the phase delay in the PLL control loop. Therefore, to ensure stability when using these filters, the PLL bandwidth should be significantly reduced, which slows down the transient response.

An effective approach to improve the PLL dynamic behavior when using these filters is to employ a hybrid type-1/type-2 PLL structure, as that proposed in [12]. In this structure, the

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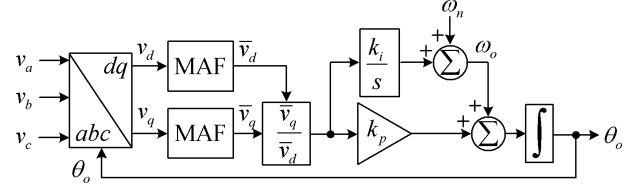

Fig. 1. Structure of the standard MAF-PLL.

PLL acts as a type-1 control system under nominal frequency, and turns to a type-2 control system under off-nominal grid frequencies. This structure removes the coupling between the estimated frequency and phase under phase angle jumps and enables the PLL to achieve a fast dynamic response and high filtering capability.

Another approach is to use a proportional-integral-derivative (PID) controller instead of the PI controller in the PLL control loop [7]. The phase lead induced by the derivative action of PID controller enables the designer to some degree compensate the phase delay caused by the in-loop filtering stage and, therefore, improve the PLL dynamic behavior and enhance its stability margin.

Inspired from the idea of quasi-type-1 PLL (QT1-PLL) [13], a PLL with fast dynamic response and high filtering capability is developed in this paper. The suggested PLL structure is called the hybrid PLL (HPLL), as it is based on a hybrid synchronous/stationary reference frame filtering method. The effectiveness of suggested PLL structure is confirmed through numerical results.

II. QUASI-TYPE-1 PLL

Fig. 1 demonstrates the schematic diagram of the standard MAF-PLL, which is the conventional synchronous reference frame PLL with in-loop MAF [7]. The in-loop MAF, however, as mentioned before, slows down the PLL transient response. To mitigate this problem, the PI controller can be replaced with a simple gain. Removing the integral action of the PI controller, however, makes the PLL incapable of tracking frequency drifts. To tackle this problem, the output signal of the MAF can be added to the estimated phase by the PLL, as highlighted by the coloured line in Fig. 2 [13]. This addition forces the MAF to act like an integrator and, therefore, enables the PLL to achieve a zero average phase-error in the presence of frequency drifts. This PLL structure is called the QT1-PLL [13].

The QT1-PLL provides a fast dynamic behavior (a settling time of around 1.5 cycles of the nominal frequency) and

Fig. 2. Schematic diagram of the QT1-PLL.

Fig. 3. 2% settling time of the QT1-PLL as a function of k_p.

Fig. 4. Bode plot of $\alpha\beta\mathrm{DSC}_2$ operator.

a good disturbance rejection capability, when only blocking the odd-order harmonic components of the PLL input is needed. However, when blocking all harmonics and dc offset is intended, as is the case here, its transient response may not be fast enough for the grid connected applications. To better visualize this fact, Fig. 3 shows the variations of the 2% settling time of QT1-PLL as a function of k_p in response to a phase-angle jump. Notice that in obtaining this plot the MAF window length is set to $T_w = T$ (T is the grid fundamental period), as the objective is to block all harmonics and dc offset. As shown in Fig. 3, the minimum settling time of the QT1-PLL is around three cycles of the nominal frequency, which is obtained for $k_p \approx 50$.
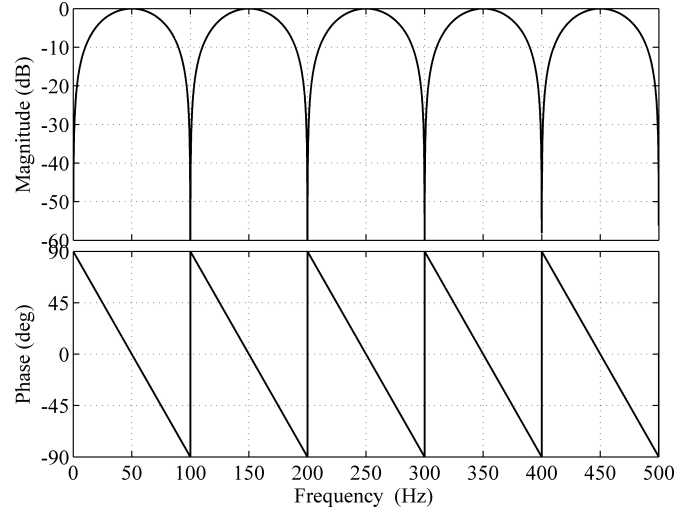
III. SUGGESTED PLL STRUCTURE

The relatively slow transient response of the QT1-PLL (when selecting $T_w = T$) is due to the large phase delay introduced by the MAF in its control. Therefore, to improve its transient response, we change the MAF window length to $T_w = T/2$. In this condition, the MAF can only block the odd-order harmonics of the PLL input, and cannot effectively block the dc offset and even-order harmonic components. To tackle this problem, we use the $\alpha\beta$-frame DSC ($\alpha\beta$DSC) operator in the PLL input. The $\alpha\beta$DSC is a finite impulse response filter that can be defined in the Laplace-domain as [14], [15]

$$\alpha\beta\mathrm{DSC}_n(s) = \frac{1 + e^{j\frac{2\pi}{n}} e^{-\frac{T}{n}s}}{2} \tag{1}$$

where n is the delay factor, and it should be determined according to those components that should be removed.

The $\alpha\beta$DSC operator in the PLL input should block the dc offset and even-order harmonic components. Therefore, $n = 2$ is selected as its delay factor. Fig. 4 shows the Bode plot of $\alpha\beta$DSC$_2$ operator. It can be observed that the $\alpha\beta$DSC$_2$ operator has unity gain at 50 Hz (fundamental frequency), and provides zero gain at zero frequency and all even-order

harmonic frequencies. Incorporating the $\alpha\beta$DSC$_2$ operator into the QT1-PLL structure, which results in the proposed PLL structure, is shown in Fig. 5. We call this structure the hybrid PLL (HPLL), as it uses a hybrid stationary/synchronous reference frame filtering technique.

As shown in Fig. 4, the $\alpha\beta$DSC$_2$ operator passes the fundamental frequency component with no phase shift when the grid frequency is at its nominal value; a phase shift, however, happens in the presence of frequency drifts. To compensate this error, the frequency estimated by the PLL can be fed back to the $\alpha\beta$DSC$_2$ operator to make it frequency adaptive. This feedback loop, however, makes the PLL highly nonlinear. In this condition, it is rather difficult to ensure the PLL stability under all circumstances. To avoid this problem, we compensate this error at the PLL output [16].

Considering $\omega_i = \omega_n + \Delta\omega_i$ as the grid frequency, where $\Delta\omega_i$ denotes the deviation of grid frequency from the nominal frequency ω_n, the phase shift caused by the $\alpha\beta$DSC$_2$ operator at the fundamental frequency can be obtained as

$$\angle\alpha\beta\mathrm{DSC}_2(j\omega_i) = -\frac{T}{4}\Delta\omega_i. \tag{2}$$

Considering that the output signal of the proportional gain k_p is an estimation of $\Delta\omega_i$, this phase-error can be easily compensated as highlighted in Fig. 5, in which $k_\varphi = T/4$.

A. Small-Signal Model

Fig. 6 shows the HPLL small-signal model, in which the dynamics of the $\alpha\beta$DSC operator is modeled by its synchronous reference frame equivalent, i.e. the dq-frame DSC (dqDSC) operator. This model is very useful for analyzing the HPLL stability and tuning its parameters. The procedure of derivation of the model is not presented here for the sake of brevity, however its accuracy is evaluated in the following.

To evaluate the accuracy of this model, a dynamic performance comparison between the actual HPLL and its model is conducted. Fig. 7 shows the results of this comparison. It can be observed that the small-signal model accurately predicts the HPLL dynamic behavior, which confirms its accuracy.
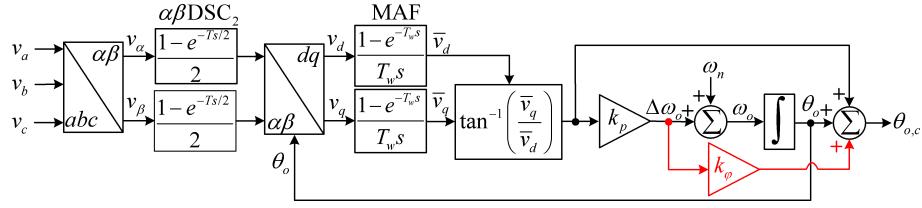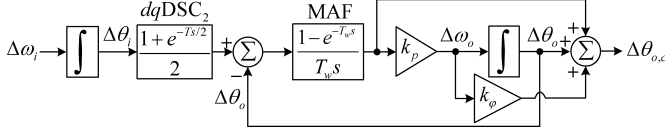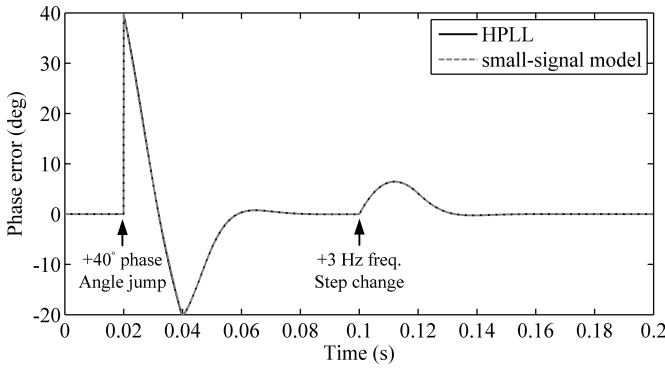
Fig. 5. Schematic diagram of HPLL.

Fig. 6. HPLL small-signal model.

Fig. 7. Accuracy assessment of the small-signal model. Parameters: $T_w = 0.01$ s, and $k_p = 94$.

B. Parameter Design Guidelines

The proportional gain k_p is the only parameter that need to be designed, as the MAF window length and the $\alpha\beta$DSC delay factor have been already selected. Fig. 8(a) and (b) shows the variations of 2% settling time (in response to a phase angle jump) and phase margin (PM) of the HPLL as a function of k_p, respectively. The minimum settling time, which is less than two cycles of the nominal frequency, corresponds to $k_p \approx 94$. This value of k_p also results in PM = 34.8°, which is good enough to ensure the HPLL stability. Therefore, $k_p = 94$ is selected in this paper.

IV. SIMULATION RESULTS

The aim of this section is to evaluate the performance of HPLL through its digital simulation in Matlab/Simulink environment. Throughout the simulation studies, the sampling frequency 10 kHz and the nominal frequency 50 Hz are considered.

For the sake of comparison, the QT1-PLL and the standard MAF-PLL are also implemented and their performance is compared with that of the proposed PLL. The MAF-PLL control parameters are selected using the symmetrical optimum method [7], and the QT1-PLL proportional gain k_p is selected close to 50 to minimize its settling time (see Fig. 3). The control parameters of all PLLs are summarized in I.
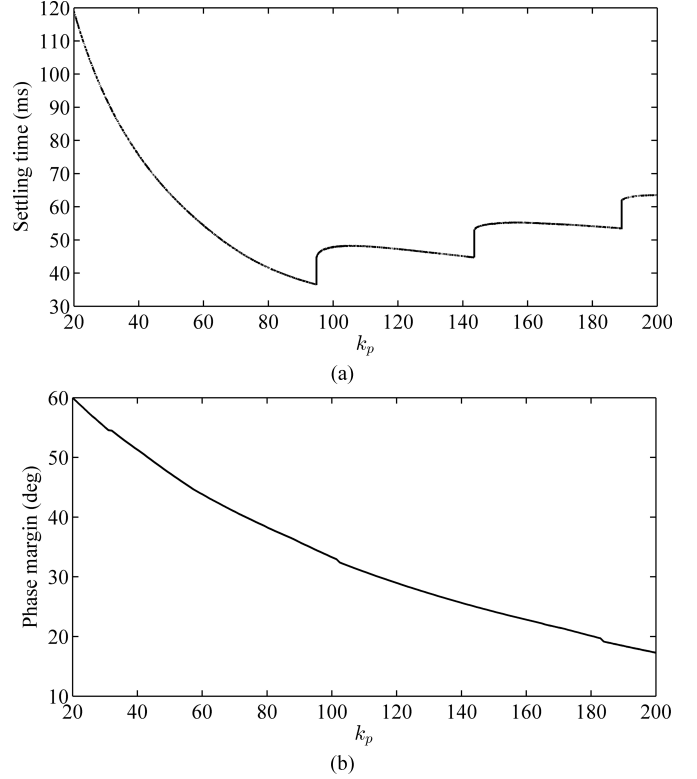
Fig. 8. (a) the 2% settling time of the HPLL as a function of k_p in response to a phase angle jump; (b) the phase margin of the HPLL as a function of k_p.

TABLE I
CONTROL PARAMETERS

	MAF-PLL	QT1-PLL	HPLL
Proportional gain, k_p	41.42	49.8	94
Integral gain, k_i	710.68	——	——
MAF window length, T_w	0.02 s	0.02 s	0.01 s

Fig. 9 and 10 show simulation results under a +40° phase angle jump and +3 Hz frequency step change, respectively. As shown, the HPLL provides the shortest settling time (its settling time is around two cycles of nominal frequency).

Fig. 11 shows the steady-state simulation results under harmonically distorted and unbalanced grid conditions. The grid voltage parameters are $V_1^+ = 1$ pu, $V_1^- = V_5^- = V_7^+ = V_{11}^- = V_{13}^+ = 0.05$ pu, and $V_2^- = V_4^+ = V_8^- = V_{10}^+ = 0.01$ pu. This test is carried out under off-nominal grid frequencies, as the disturbance rejection capability of all PLL is excellent under nominal frequency. As show, the MAF-PLL provides
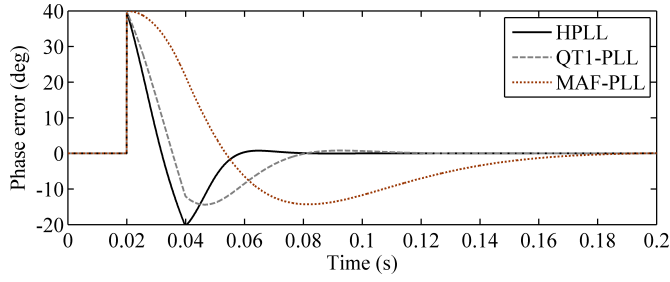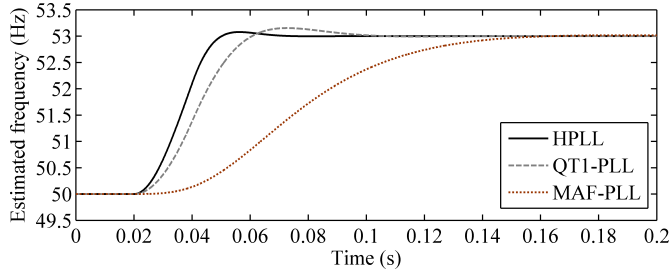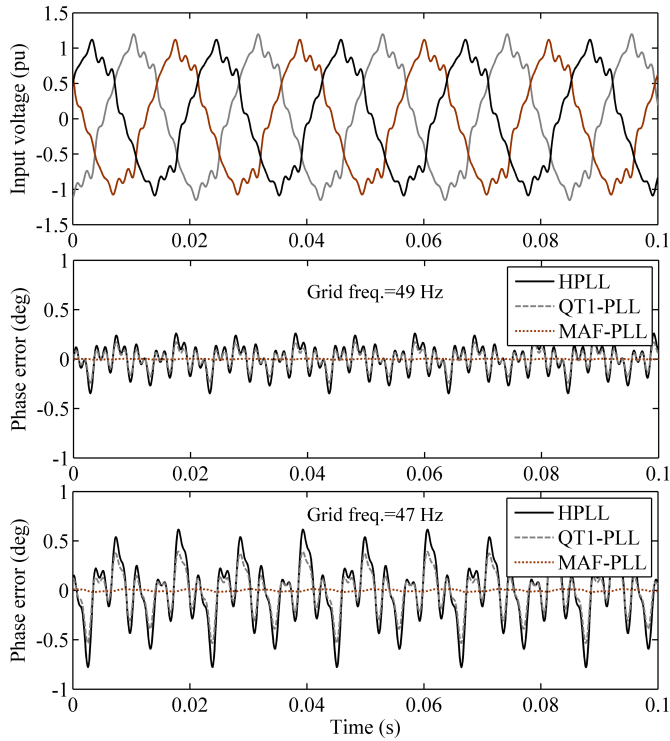
Fig. 9. Simulation results under a $+40°$ phase-angle jump.

Fig. 10. Simulation results under a $+3$ Hz frequency step change.

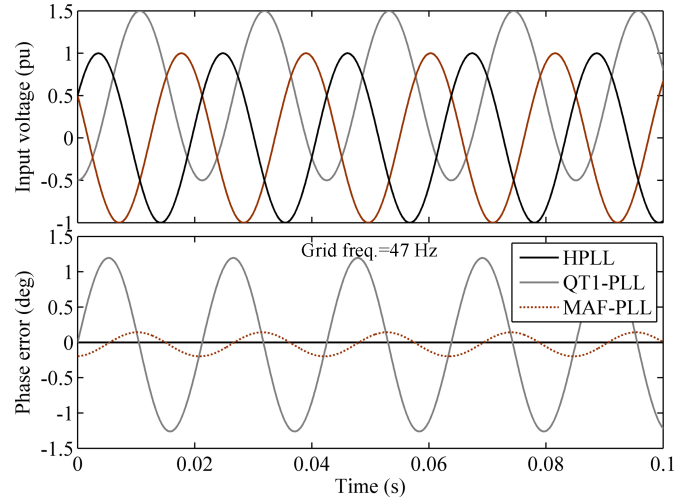Fig. 11. Steady-state simulation results under distorted and unbalanced grid condition.

Fig. 12. Steady-state simulation results when a large dc offset exists in the PLL input.

off-nominal frequency ($f = 47$ Hz), as the dc offset rejection capability of all PLLs is excellent under nominal frequency. It can be observed that the proposed HPLL gives a zero phase error, thanks to the action of the $\alpha\beta\text{DSC}_2$ operator in its input. The dc offset rejection capability of the MAF-PLL is quite good, as shown in Fig. 12. The QT1-PLL, however, is not able to effectively reject the dc offset.

V. CONCLUSION

In this paper an effective PLL, called the HPLL, for fast synchronization under adverse grid conditions was proposed. The suggested PLL structure has a different structure compared to the standard PLLs, which enables it to achieve a high filtering capability and a fast transient response. The effectiveness of the proposed PLL structure was confirmed through numerical results.

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an excellent filtering capability even in the presence of large frequency drifts. The harmonic filtering capability of the proposed HPLL and QT1-PLL, although not as good as that of the MAF-PLL, is quite acceptable, particularly when the grid frequency is close to its nominal value.

Fig. 12 shows the steady-state simulations results in the presence of an exaggeratedly large dc offset (0.5 pu) in the phase A of the grid voltage. This test is carried out under

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