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Five Approaches to Deal With Problem of DC Offset in Phase-Locked Loop Algorithms: Design Considerations and Performance Evaluations

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***Abstract*—The presence of the dc component in the phase-locked loop (PLL) input results in fundamental frequency oscillations in the phase and frequency estimated by the PLL. The removal of these oscillations is a challenging task because of their low frequency. The aim of this paper is to provide a detailed analysis of several approaches that little work has been conducted on their application for addressing the problem of dc offset in the PLL algorithms. These approaches include using the *dq*-frame delayed signal cancellation (DSC) operator and the notch filter as the PLL in-loop filtering stages, and using the $\alpha\beta$-frame DSC operator, the complex coefficient filter, and a cross-feedback network for blocking the dc offset before the PLL input. Design aspects of these methods are presented, some methods to enhance their performances are proposed, and their advantages and disadvantages are evaluated.**

***Index Terms*—DC offset, frequency estimation, phase estimation, phase-locked loop (PLL), synchronization.**

I. Introduction

The phase locked loops (PLLs) are closed-loop feedback control systems that are crucial in the synchronization and control of grid-connected power electronic based equipment [1]-[3]. They are also widely used in the control of electrical machines [4], [5], measuring power quality phenomena and indices [6], [7], implementing robust adaptive filters [8], [9], islanding detection [10], [11], etc.

The presence of the dc offset in the PLL input, which may be due to grid faults [12], measurement devices [13], A/D conversion process [14], [15], dc injection from distributed generation systems [16], [17], geomagnetic phenomena [18], half-wave rectification [19], etc., results in the fundamental frequency oscillations in the estimated quantities by the PLL [20]. Removal of these oscillations is a difficult task due to their low frequency.

In the grid-connected applications, the presence of the dc offset in the PLL input may also result in the dc injection by the grid-tied converters. The reason is that in this condition the PLL unit vector (the sine and cosine of the phase angle estimated by the PLL), which is often used by these converters for creating their reference current, contains a dc component [21]. The international standards, however, have imposed strict limits on the dc injection of the grid-connected converters. For example, the standard IEC61727 [22] limits the dc current injection by the grid-connected photovoltaic inverters to less than 1% of their rated output current, and the standard IEEE 1547-2003 [23] states that the dc injection by the distributed resources should not be more than 0.5% of their rated output current. These strict limits confirm the importance of the dc offset rejection capability for PLLs in the grid-connected applications.

To deal with the problem of the dc offset in PLL algorithms, several solutions have been proposed in literature. In [24]-[26], using a band-pass filter (BPF) before the PLL input is suggested. The BPF effectively blocks the dc offset, but it slows down the PLL dynamic response and causes a phase shift in the PLL input in the presence of frequency drifts. This phase shift can be avoided by using a frequency adaptive BPF, or by compensating the phase shift at the PLL output [27].

In [28], including a high-pass filter (HPF) at the PLL input is suggested. In this technique, the grid voltage is first passed through a low-pass filter (LPF) to estimate its dc component. The LPF output signal is then subtracted from the grid voltage to cancel its dc component. Depending on the LPF order and cutoff frequency, this technique may reduce the harmonic filtering capability of the PLL and also cause a phase error at its output.

In [15], the focus is on rejecting the dc offset in the single-phase synchronous reference frame PLLs. In this method, the input signal of the PLL loop filter is separately integrated over two half-cycles. The obtained results are then subtracted from each other and passed through a proportional-integral (PI) controller. The output of this PI controller, which is an estimation of the input dc component, is subtracted from the PLL input to cancel its dc component.

In [29], the difference between the PLL input and the fundamental component extracted by the PLL is passed through an integrator. The output of the integrator, which is an estimation of the input dc component, is then subtracted from the PLL input to reject this component. Some similar techniques can be found in [21] and [30].

The main aim of this paper is to provide a detailed analysis

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of some less discussed techniques for rejecting the dc offset in the PLL algorithms. These techniques include using the *dq*-frame delayed signal cancelation operator (which will be briefly called the *dq*DSC operator) and the notch filter for rejecting the dc offset inside the PLL control loop, and using the $\alpha\beta$-frame delayed signal cancelation operator (which will be briefly called the $\alpha\beta$DSC operator), the complex coefficient filter (CCF), and a cross-feedback network (CFN) for blocking the dc offset before the PLL input. In addition to the analysis of each technique, design guidelines, techniques to enhance their performance and extension to unbalabced and harmonically distorted grid conditions will be provided and simulation results will be reported and discussed.

II. DC Offset Removal Using *dq*DSC Operator

The *dq*DSC operator is a finite-impulse response filter that is defined in the Laplace domain as [31], [32]

$$dq\mathrm{DSC}_n(s) = \frac{1+e^{-(T/n)s}}{2} \tag{1}$$

where, T is the grid fundamental period and n, which is a positive constant, is called the delay factor.

Substituting $s = j\omega$ into (1) gives the magnitude and phase of the *dq*DSC operator as

$$dq\mathrm{DSC}_n(j\omega) = \left|\cos\left(\frac{\omega T}{2n}\right)\right| \angle -\left(\frac{\omega T}{2n}\right). \tag{2}$$

Using (2), it is easy to show that the *dq*DSC operator blocks frequencies $f = \frac{n}{T}\left(k+\frac{1}{2}\right),\ k \in Z$ in Hertz. Therefore, to block the fundamental frequency component (i.e., $f = 1/T$) in the PLL control loop, the delay factor n should be $n = \frac{2}{2k+1}$. According to this equation, there are infinite values that can be selected for n. The optimum value for n, however, is the highest value, because, according to (2), the phase delay caused by the *dq*DSC operator is inversely proportional to n. Therefore, $n = 2$ (which corresponds to $k = 0$) is selected for the delay factor n.

Fig. 1 shows the frequency response of the $dq\mathrm{DSC}_2$ operator. It can be observed that the $dq\mathrm{DSC}_2$ operator removes the fundamental frequency component and all odd-order harmonic components. Inclusion of this operator into the PLL control loop is shown in Fig. 2. This PLL structure is called the *dq*DSC-PLL. Notice that to make the PLL control loop insensitive to the grid voltage amplitude variations, an amplitude normalization mechanism (ANM) is also included in its control loop. This ANM is realized by passing the *d*-axis voltage component through the $dq\mathrm{DSC}_2$ operator to obtain an estimation of the grid voltage amplitude and dividing the output signal of *q*-axis DSC operator by the estimated amplitude. An additional LPF can also be cascaded with the *d*-axis DSC operator to ensure that the estimated amplitude is free of high frequency noises.

A. Design Considerations

Selecting the *dq*DSC-PLL parameters is based on the small-signal model of this PLL, which can be simply obtained as shown in Fig. 3. In this model, Δ denotes the perturbation around the nominal operating point.

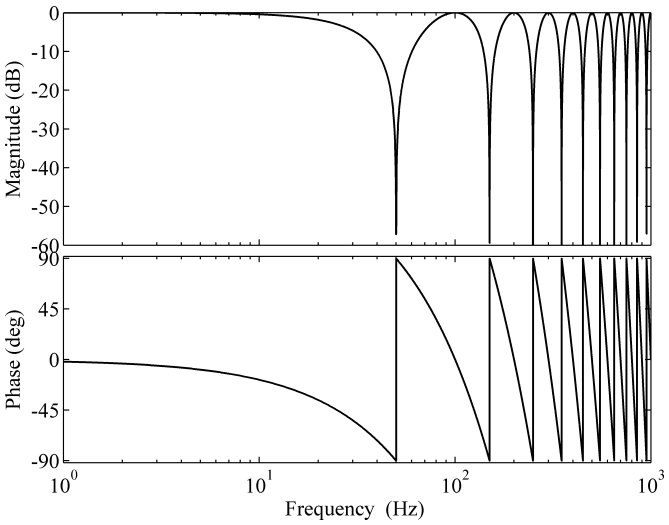

Fig. 1. Frequency response of the $dq\mathrm{DSC}_2$ operator.

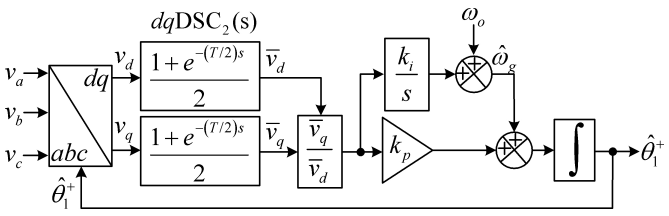

Fig. 2. Schematic diagram of the *dq*DSC-PLL.

Using Fig. 3, the open-loop transfer function can be obtained as

$$G_{ol}(s) = \frac{\Delta\hat{\theta}_1^+(s)}{\Delta\theta_1^+(s) - \Delta\hat{\theta}_1^+(s)} = \frac{1+e^{-\frac{Ts}{2}}}{2}\frac{k_p s + k_i}{s^2}. \tag{3}$$

The presence of the delay term in (3) complicates the analysis and design procedure. To overcome this problem, this delay term is replaced by its first-order Padé approximation, i.e., $e^{-\frac{sT}{2}} \approx \frac{1-sT/4}{1+sT/4}$, which gives

$$G_{ol}(s) \approx \frac{1}{1+s\underbrace{T/4}_{T_d}}\frac{k_p s + k_i}{s^2}. \tag{4}$$

Applying the symmetrical optimum design method [33] to (4) gives the proportional and integral gains as

$$\begin{aligned} k_p &= 1/(bT_d) \\ k_i &= 1/(b^3 T_d^2) \end{aligned} \tag{5}$$

where, b is a design constant that determines the phase margin (PM) of the PLL as $PM \approx \tan^{-1}\left(\frac{b^2-1}{2b}\right)$. $b = 1+\sqrt{2}$, which corresponds to $PM \approx 45°$, is selected in this paper. This selection gives the proportional and integral gains as $k_p = 82.84$, and $k_i = 2842.7$.

Fig. 4 shows the open-loop Bode plot of the *dq*DSC-PLL. Notice that the crossover frequency corresponds to the peak of the phase plot, which is a direct result of the symmetrical optimum design method. As it can be observed, the PM is $43.8°$, which is very close to the intended PM.

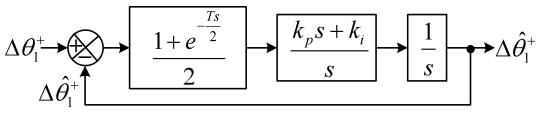

Fig. 3. Small-signal model of the *dq*DSC-PLL.

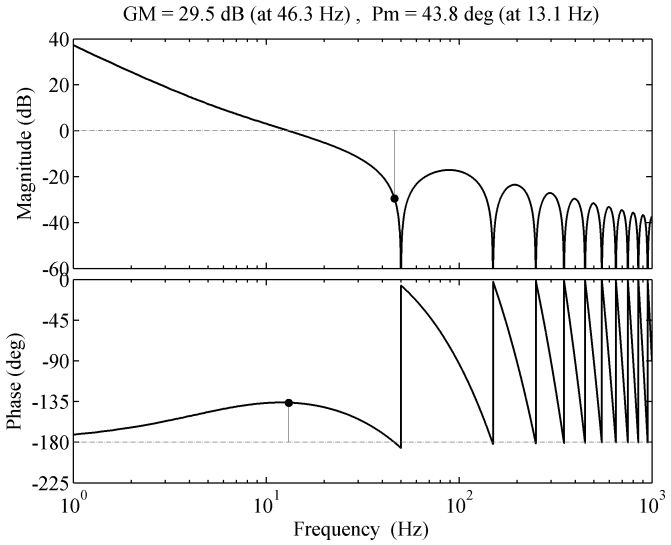

Fig. 4. Open-loop Bode plot of the *dq*DSC-PLL.

B. Performance Evaluation

In this section, the dynamic performance of the *dq*DSC-PLL and its dc offset rejection capability are evaluated through simulation results. To this end, three test cases are designed:

1) **Test case 1**: The grid voltage is contaminated with the dc offset ($v_{a,dc} = -0.05$ pu, $v_{b,dc} = 0.05$ pu, and $v_{c,dc} = 0.025$ pu). The steady-state peak-to-peak value of the fundamental frequency oscillatory error in the estimated phase is considered as the performance index in this test. To take into account the effect of the grid frequency variations on the PLL dc offset rejection capability, this test is carried out under the nominal frequency (i.e., 50 Hz) and off-nominal frequencies 49 and 47 Hz.
2) **Test case 2**: The grid voltage undergoes a $+40°$ phase angle jump. The 2% settling time, i.e., the time after which the PLL phase error reaches and remains within $0.8°$ of neighbourhood of zero, is the main performance index in this test.
3) **Test case 3**: The grid voltage undergoes a $+3$ Hz frequency step change. The 2% settling time, i.e., the time after which the estimated frequency reaches and remains inside the band of 0.06 Hz around its final value, is the main performance index in this test.

The simulations are carried out in the Matlab/Simulink environment. Throughout the simulation studies, the sampling frequency is fixed at 10 kHz. The z-domain transfer function of the $dq\mathrm{DSC}_2$ operator is as follows

$$dq\mathrm{DSC}_2(z) = \frac{1+z^{-N_2}}{2} \tag{6}$$

where, $N_2 = \mathrm{round}\left[(T/2)/T_s\right] = 100$, and T_s is the sampling time.

Fig. 5(a) shows the *dq*DSC-PLL simulation results for the test case 1. It can be observed that the *dq*DSC-PLL provides a good dc offset rejection capability even when the grid frequency deviation from its nominal value is high. Fig. 5(b) and (c) show the *dq*DSC-PLL simulation results under the test case 2 and 3, respectively. The 2% settling time of the *dq*DSC-PLL is around 72 ms and 58.1 ms for these tests, respectively, which indicate a rather slow transient response. Therefore, the *dq*DSC-PLL can be useful in applications where a slow and damped dynamic behavior from the PLL is expected. For those applications where a faster dynamic response is needed, the dynamic performance of the *dq*DSC-PLL can be improved as will be shown in the next section.

C. Dynamic Performance Enhancement

The rather slow dynamic response of the *dq*DSC-PLL is mainly due to the large phase delay induced by the $dq\mathrm{DSC}_2$ operator in the control loop. Therefore, the dynamic response of the *dq*DSC-PLL can be improved by compensating this phase delay. To achieve this goal, we suggest to incorporate a phase-lead compensator (PLC) with a z-domain transfer function of the following form into the *dq*DSC-PLL control loop

$$G_{c2}(z) = \frac{1+r^{N_2}}{1+r^{N_2}z^{-N_2}} \tag{7}$$

where, $r \in [0\ \ 1)$ is called the attenuation factor, and N_2, as defined before, is the number of samples within the the $dq\mathrm{DSC}_2$ delay time $T/2$. Notice that (7) is the inverse of (6) for $r = 1$.

Incorporating the PLC into the *dq*DSC-PLL control-loop is shown in Fig. 6. To better visualize the effect of the PLC, Fig. 7 compares the frequency responses of single $dq\mathrm{DSC}_2$ operator and the cascade connection of $dq\mathrm{DSC}_2$ operator and PLC for different values of r. As shown, the phase delay introduced by the $dq\mathrm{DSC}_2$ operator can be effectively compensated by selecting a close to unity value for the attenuation factor r. In this paper, $r = 0.99$ is selected.

Fig. 8 shows the small-signal model of the *dq*DSC-PLL with PLC. Using this model, the open-loop transfer function can be obtained as

$$G_{ol}(s) = \frac{\Delta\hat{\theta}_1^+}{\Delta\theta_1^+ - \Delta\hat{\theta}_1^+} = \underline{dq\mathrm{DSC}_2(s)G_{c2}(s)}\frac{k_p s+k_i}{s^2}. \tag{8}$$

The underlined term in (8) can be neglected without significantly affecting the accuracy, because this term provides a close to unity gain and small phase delay at low frequency range. Therefore, (8) can be approximated by

$$G_{ol}(s) \approx \frac{k_p s+k_i}{s^2}. \tag{9}$$

Using (9), the closed loop transfer function of the *dq*DSC-PLL with PLC can be obtained as

$$G_{cl}(s) = \frac{G_{ol}(s)}{1+G_{ol}(s)} \approx \frac{k_p s+k_i}{s^2 + \underbrace{k_p}_{2\zeta\omega_n} s + \underbrace{k_i}_{\omega_n^2}} \tag{10}$$

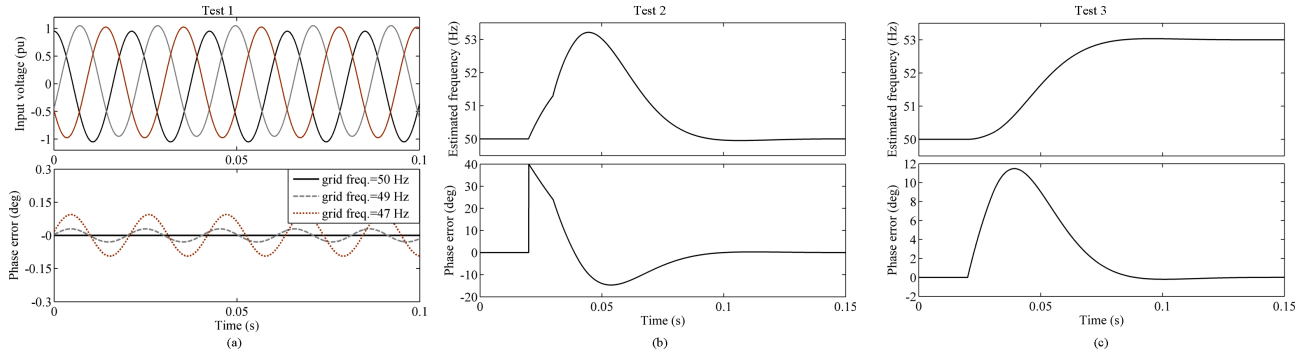

Fig. 5. *dq*DSC-PLL simulation results under (a) test case 1, (b) test case 2, and (c) test case 3.

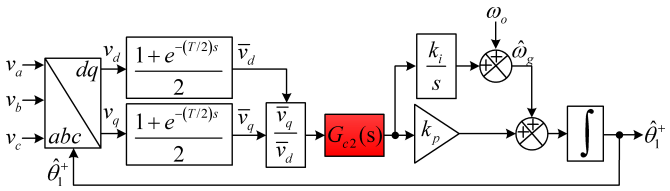

Fig. 6. *dq*DSC-PLL with PLC.

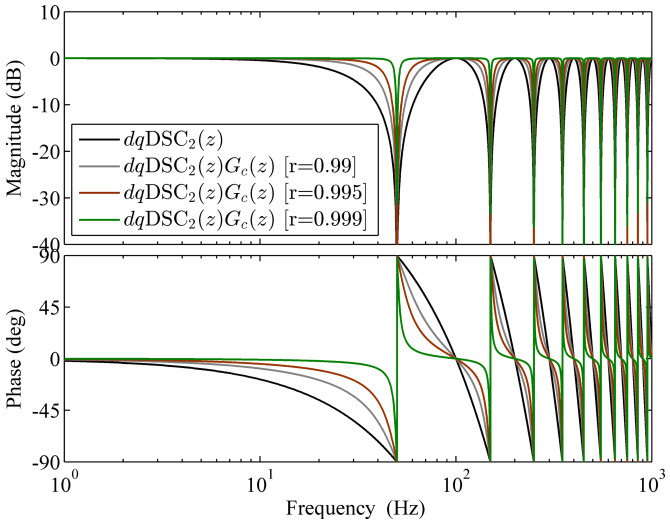

Fig. 7. A comparison between the frequency response of single $dq\text{DSC}_2$ operator and cascade connection of the $dq\text{DSC}_2$ operator and the PLC for three different values of r.

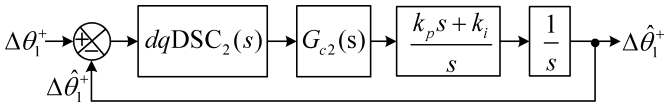

Fig. 8. Small-signal model of the *dq*DSC-PLL with PLC.

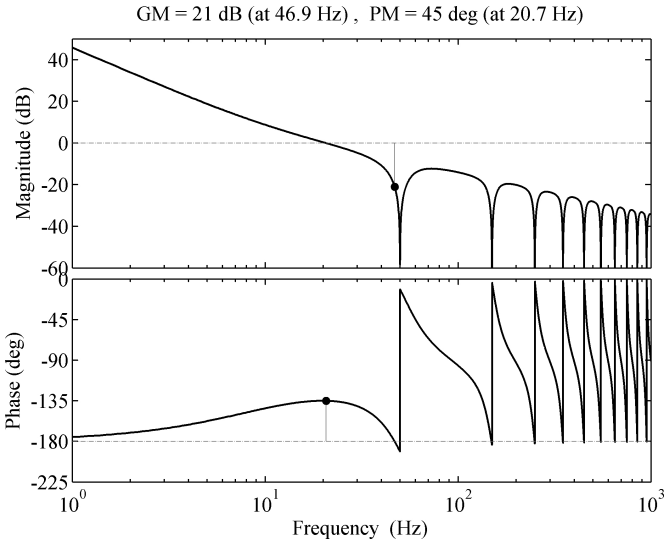

Fig. 9. Open-loop Bode plot of the *dq*DSC-PLL with PLC. Parameters: $k_p = 124.4$, $k_i = 7737.8$, and $r = 0.99$.

where, ζ is the damping factor and ω_n is the natural frequency. Therefore, the proportional and integral gains can be determined by selecting appropriate values for ζ and ω_n. Special care should be taken in selecting ω_n, as a high value for ω_n can result in instability. This fact can be easily shown by calculation of the PM of the PLL as a function of ω_n, as discussed in [34]. To achieve the optimum damping, $\zeta = 1/\sqrt{2}$ is selected, and to obtain a rather fast dynamic response while maintaining an adequate stability margin, $\omega_n = 2\pi 14$ rad/s is chosen. These selections gives $k_p = 124.4$ and $k_i = 7737.8$.

Fig. 9 shows the open-loop Bode plot of the *dq*DSC-PLL with PLC. It can be observed that the PLC enables the *dq*DSC-PLL to achieve a higher bandwidth and, therefore, a faster dynamic response without jeopardizing its stability condition.

To confirm the effectiveness of the PLC in improving the dynamic response of the *dq*DSC-PLL, Fig. 10 evaluate the PLL dynamic performance under the test case 2. The 2% settling time is 47.4 ms which indicates a faster dynamic response compare to the original *dq*DCS-PLL.

This improvement in settling time, however, is at the cost of decreasing the dc offset rejection capability of the *dq*DSC-PLL, particularly when the deviation of grid frequency from its nominal value is high. This fact can be better visualized through Fig. 11, which shows the simulation results under the test case 1. This result was expected, because the PLC reduces the bandwidth of notches in the frequency response of the $dq\text{DSC}_2$ operator (see Fig. 7).

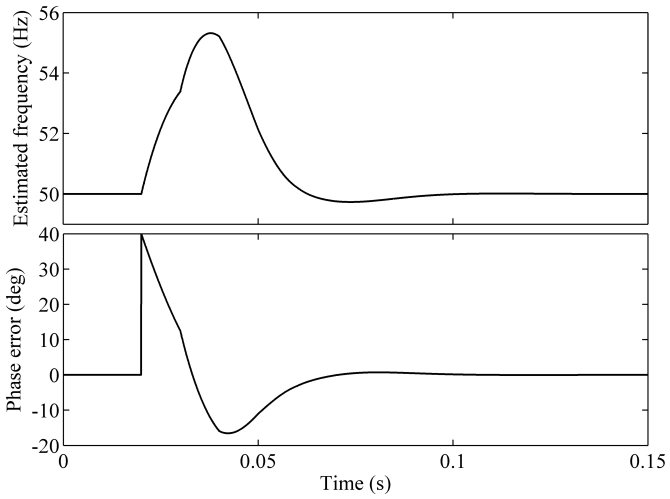

Fig. 10. Simulation results for the *dq*DSC-PLL with PLC under the test case 2.

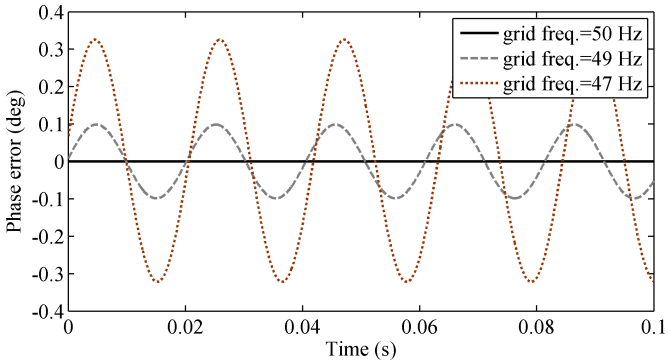

Fig. 11. Simulation results for the *dq*DSC-PLL with phase lead compensator under the test case 1.

D. Extension to the Harmonically Distorted and Unbalanced Grid Condition

Although the focus in this paper is on adding the dc offset rejection capability to the standard PLL structure, the presence of harmonic components in the PLL input cannot be ignored. Therefore, we are going to briefly discuss here how the PLL structure should be extended to take into account the presence of harmonic components and the grid voltage unbalance.

As Fig. 9 shows, the $dq\mathrm{DSC}_2$ operator blocks the even-order harmonic components of the PLL input. Therefore, we should focus on removing the fundamental frequency negative sequence (FFNS) component and odd-order harmonic components. The FFNS component, which appears as a double frequency component in the control loop, can be blocked by including the $dq\mathrm{DSC}_4$ operator into the PLL control loop [34]. In addition to the FFNS component, this operator blocks the harmonics of order -5 and $+7$, which are the most dominant harmonic components in the grid voltage. To block the remaining harmonic components, incorporating the $dq\mathrm{DSC}_8$ and $dq\mathrm{DSC}_{16}$ operators into the PLL control is needed. Finally, to minimize the phase delay caused by these additional *dq*DSC operators, including three extra lead compensators into the PLL control is required, as shown in Fig. 12.

III. DC Offset Removal Using $\alpha\beta$DSC Operator

The $\alpha\beta$DSC operator can be understood as the stationary-reference frame equivalent of the *dq*DSC operator. This operator is defined in the s-domain as [31], [32]

$$\alpha\beta\mathrm{DSC}_n(s) = \frac{1 + e^{\frac{j2\pi}{n}} e^{-\frac{T}{n}s}}{2} \tag{11}$$

where n, as defined before, is the delay factor.

By substituting $s = j\omega$ into (11), the magnitude and phase of the $\alpha\beta$DSC operator can be obtained as

$$\alpha\beta\mathrm{DSC}_n(j\omega) = \left|\cos\left(\frac{\omega T}{2n} - \frac{\pi}{n}\right)\right| \angle - \left(\frac{\omega T}{2n} - \frac{\pi}{n}\right). \tag{12}$$

Using (12), it is easy to show that $n = 2$ is the best choice for our objective, i.e., blocking the dc offset at the PLL input. Fig. 13 shows the frequency response of the $\alpha\beta\mathrm{DSC}_2$ operator. It can be observed that the $\alpha\beta\mathrm{DSC}_2$ operator passes the fundamental component and rejects the dc component and even-order harmonic components.

Fig. 14 shows the basic scheme of the $\alpha\beta$DSC-PLL, which is a standard synchronous reference frame PLL (SRF-PLL) with the $\alpha\beta\mathrm{DSC}_2$ operator as its pre-filtering stage. We have also added an ANM before the SRF-PLL input to make its dynamics insensitive to the grid voltage amplitude variations. A LPF can also be added to the ANM to ensure the estimated amplitude is free from any noises.

A. $\alpha\beta$DSC-PLL with the phase error compensator

From Fig. 13, it can be observed that the $\alpha\beta\mathrm{DSC}_2$ operator provides zero phase shift at the fundamental frequency when the grid frequency is at its nominal value; however, a phase shift happens in the presence of frequency drifts. To compensate this phase shift, which results in a bias error in the estimated phase by the PLL, it is traditionally recommended to feedback the estimated frequency by the PLL and make the $\alpha\beta$DSC operator frequency adaptive [31], [32]. This feedback loop, however, makes the PLL highly nonlinear. In this condition, it is rather difficult to ensure the PLL stability under all circumstances [35]. To avoid this problem, we compensate this error at the PLL output [27].

Considering $\omega_g = \omega_o + \Delta\omega_g$ as the grid frequency, where $\Delta\omega_g$ denotes the deviation of grid frequency from the nominal frequency ω_o, the phase shift caused by the $\alpha\beta\mathrm{DSC}_2$ operator at the fundamental frequency can be obtained using (12) as

$$\angle\alpha\beta\mathrm{DSC}(j\omega_g) = -\frac{T}{4}\Delta\omega_g. \tag{13}$$

Considering that the output signal of the integrator of the PI controller is an estimation of $\Delta\omega_g$, this phase-error can be easily compensated as highlighted in Fig. 15, in which $k_\varphi = T/4$.

B. Design Considerations

Selecting the parameters of the $\alpha\beta$DSC-PLL with phase-error compensator (PEC) is based on the small-signal model of this PLL, which is shown in Fig. 16. Notice that the dynamics of pre-filtering stage of the PLL (i.e., the $\alpha\beta\mathrm{DSC}_2$ operator)

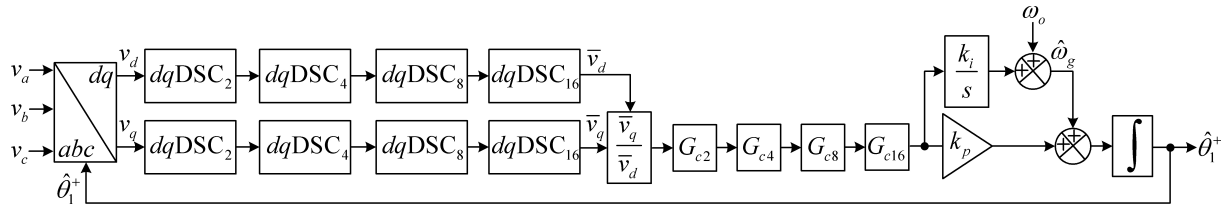

Fig. 12. Extension of *dq*DSC-PLL with phase lead compensator to take into consideration the presence of harmonics and the grid unbalance.

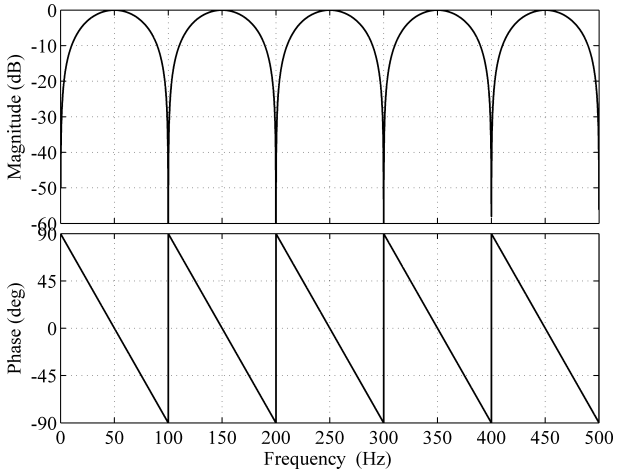

Fig. 13. Frequency response of $\alpha\beta\text{DSC}_2$ operator.

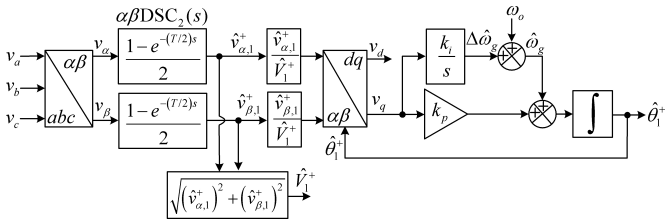

Fig. 14. Block diagram description of $\alpha\beta$DSC-PLL.

is modeled by its synchronous reference frame equivalent, i.e., the $dq\text{DSC}_2$ operator. For the sake of brevity, the procedure of derivation of this model is not presented. Its high accuracy, however, is verified using the simulation results, as shown in Fig. 17.

From Fig. 16, the open-loop[1] and closed loop transfer functions can be obtained as

$$G_{ol}(s) = \frac{(k_p + k_i k_\varphi)\, s + k_i}{s(s - k_i k_\varphi)} \tag{14}$$

$$G_{cl}(s) = \frac{\Delta\hat{\theta}^+_{1,c}}{\Delta\theta^+_1} = \frac{dq\text{DSC}_2(s)\left[(k_p + k_i k_\varphi)\, s + k_i\right]}{s^2 + k_p s + k_i}. \tag{15}$$

As it can be observed, the open-loop transfer function is unstable (it has a right hand side pole), however the closed loop transfer function is stable for $k_p > 0$ and $k_i > 0$. Defining $k_p = 2\zeta\omega_n$ and $k_i = \omega_n^2$, k_p and k_i can be determined by selecting appropriate values for ζ and ω_n.

[1]The open-loop transfer function is the ratio of feedback signal to the error signal in the equivalent classical feedback form of the small-signal model shown in Fig. 16.

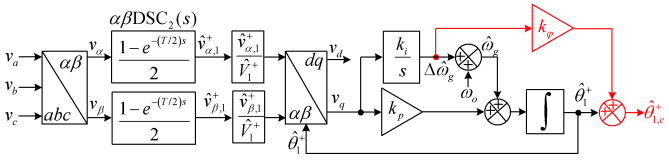

Fig. 15. $\alpha\beta$DSC-PLL with phase-error compensator (PEC).

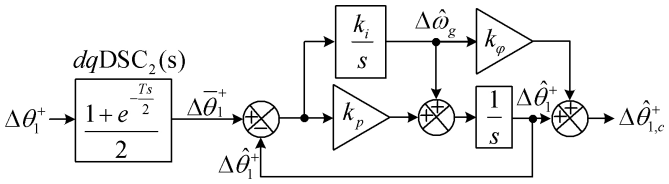

Fig. 16. Small-signal model of $\alpha\beta$DSC-PLL with PEC.

$\zeta = 1/\sqrt{2}$ and $\omega_n = 2\pi 20$ rad/s are chosen in this paper, which ensure a good damping, a rather fast dynamic response, and a sufficient stability margin for the PLL. These selections give the proportional and integral gains as $k_p = 177.71$ and $k_i = 15791$.

Fig. 18 shows the open-loop Bode plot of the $\alpha\beta$DSC-PLL with PEC. It can be observed that the designed control parameters result in $\text{PM} = 58.9°$ and $\omega_c = 40.1$ Hz (ω_c denotes the crossover frequency), which ensures a rather fast transient response and sufficient stability margin for the PLL. The gain margin (GM) of the PLL is $\text{GM} = -10.2$ dB. Notice that the negative GM does not mean instability. It just means that the system may become unstable if the PLL loop gain reduces too much [36]. Fortunately, the ANM in the $\alpha\beta$DSC-PLL prevents the PLL loop gain from reducing during the voltage sags and faults.

C. Performance Evaluation

In this section, the performance of the $\alpha\beta$DSC-PLL with PEC is evaluated through simulation results. The same test cases designed to evaluate the performance of the *dq*DSC-PLL are used for this purpose.

Thanks to the zero gain of $\alpha\beta\text{DSC}_2$ at zero frequency, the $\alpha\beta$DSC-PLL with PEC provides a zero steady-state phase error in the presence of dc offset in its input (test case 1). This result is not shown here to save the space. It is the main advantage of the $\alpha\beta$DSC-PLL over the *dq*DSC-PLL.

Fig. 19 shows the simulations results for the $\alpha\beta$DSC-PLL with PEC under the test case 2. The 2% settling time is 44.4 ms in this test, which indicates a rather fast dynamic response. The PLL presents a similar fast dynamic response under the test case 3.

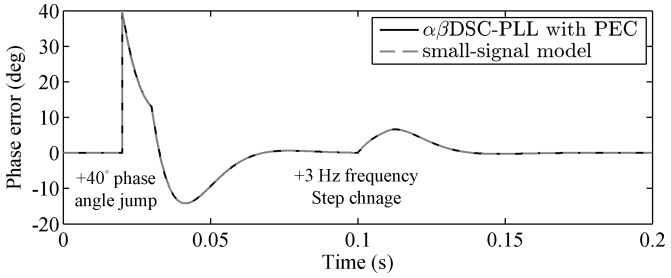

Fig. 17. Accuracy assessment of the small-signal model of the $\alpha\beta$DSC-PLL with PEC.

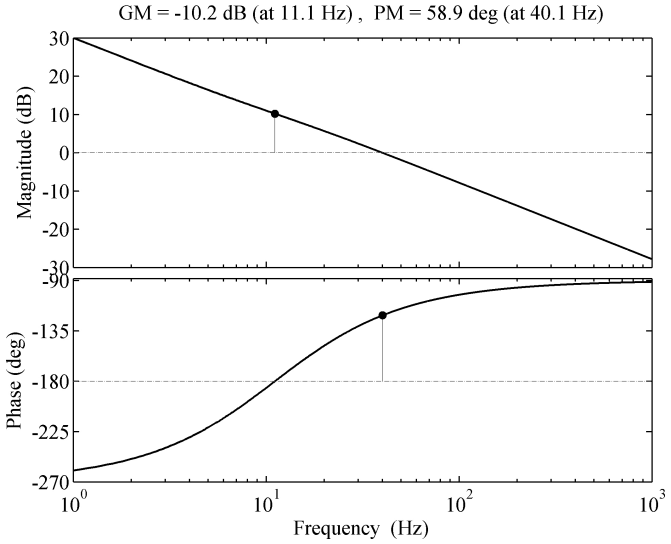

Fig. 18. Open-loop Bode plot of the $\alpha\beta$DSC-PLL with PEC.

D. Extension to the Harmonically Distorted and Unbalanced Grid Condition

The $\alpha\beta\mathrm{DSC}_2$ operator, as clearly shown in Fig. 13, can only block the even-order harmonic components. Therefore, to remove the FFNS component and odd-order harmonic components, three $\alpha\beta$DSC operators with delay factors 4, 8, and 16 should be cascaded with the $\alpha\beta\mathrm{DSC}_2$ operator. In this case, the gain of the PEC should be considered as $k_\varphi = \frac{1}{2}\left(\frac{T}{2}+\frac{T}{4}+\frac{T}{8}+\frac{T}{16}\right) = \frac{15T}{32}$.

IV. DC Offset Removal Using Notch Filter

A notch filter (NF) is a band rejection filter that significantly attenuates the signals within a band of frequencies and passes all other frequencies almost unchanged. The NF can be adaptive or non-adaptive. In this study, we focus on the application of non-adaptive NF in the PLL control loop, but some comments on the application of frequency-adaptive NF is also given at the end of this section.

The non-adaptive NF (hereafter just called the NF) can be defined in the Laplace-domain as

$$\mathrm{NF}(s) = \frac{s^2+\omega_{nf}^2}{s^2+\underbrace{(\omega_{nf}/Q)}_{\mathrm{BW}}s+\omega_{nf}^2} \tag{16}$$

in which ω_{nf} is the notch frequency, Q is the quality factor,

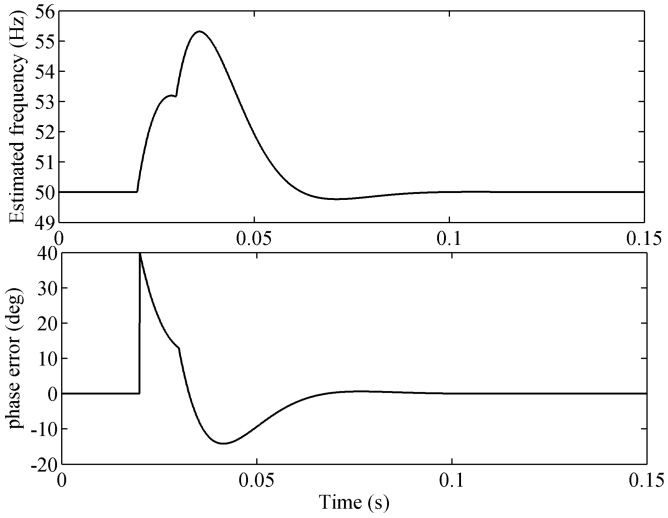

Fig. 19. Simulation results for the $\alpha\beta$DSC-PLL with PEC under the test case 2.

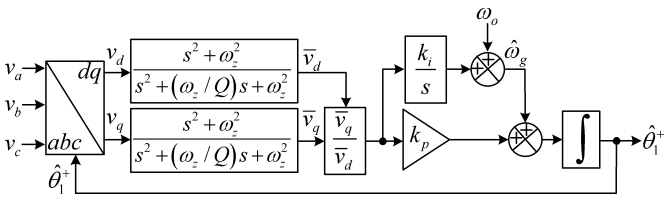

Fig. 20. Block diagram description of the NF-PLL

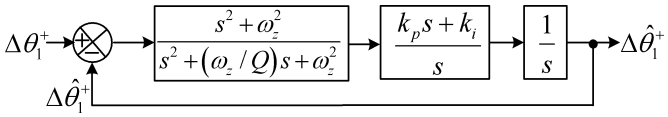

Fig. 21. Small-signal model of the NF-PLL

and BW denotes the 3 dB bandwidth of NF. The structure of NF-PLL and its small-signal model is shown in Fig. 20 and 21, respectively.

A. Design Considerations

Since the dc offset is sensed as the fundamental frequency component in the PLL control loop, the notch frequency of the NF should be set at $\omega_{nf} = 2\pi 50$ rad/s. Selecting the quality factor of the NF, on the other hand, should be made based on the anticipated range of variations for the grid frequency. In this paper, the NF quality factor is selected to be $Q = 1/\sqrt{2}$, which results in $\mathrm{BW} = 50\sqrt{2}$ Hz for the NF. This wide bandwidth NF enables the PLL to effectively block the fundamental frequency disturbance component even in the presence of large variations in the grid frequency. This advantage, however, is at cost of inducing considerable phase delay in the PLL control loop, which may jeopardize the PLL stability unless special care is taken in selecting the proportional and integral gains of the PLL.

From Fig. 21, the open-loop transfer function can be ob-

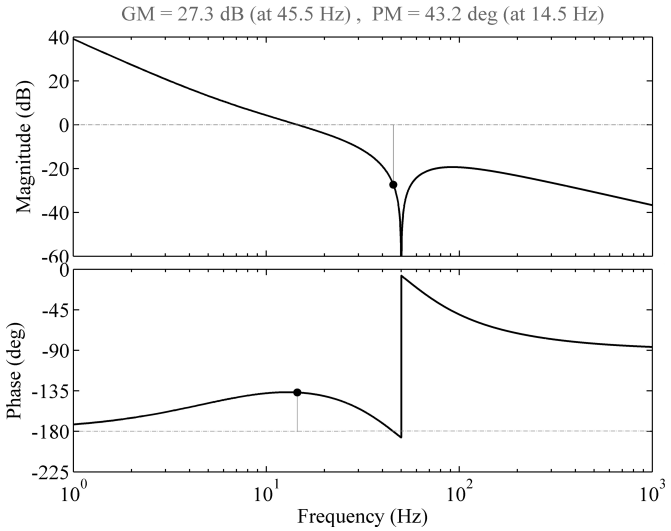

Fig. 22. Open-loop Bode plot of the NF-PLL.

tained as

$$G_{ol}(s) = \frac{s^2 + \omega_{nf}^2}{s^2 + (\omega_{nf}/Q)\, s + \omega_{nf}^2} \frac{k_p s + k_i}{s^2}. \tag{17}$$

Without significantly affecting the accuracy, the NF transfer function can be approximated by (18) at low frequency range.

$$\mathrm{NF}(s) \approx \frac{\omega_{nf}^2}{(\omega_{nf}/Q)\, s + \omega_{nf}^2} = \frac{Q\omega_{nf}}{s + Q\omega_{nf}}. \tag{18}$$

Substituting (18) into (17) gives

$$G_{ol}(s) \approx \frac{Q\omega_{nf}}{s + Q\omega_{nf}} \frac{k_p s + k_i}{s^2}. \tag{19}$$

Applying the symmetrical optimum method to (19) gives the proportional and integral gains as

$$\begin{aligned} k_p &= Q\omega_{nf}/b \\ k_i &= (Q\omega_{nf})^2/b^3 \end{aligned} \tag{20}$$

where, as defined before, b is a design constant that determines the phase margin (PM) as $\mathrm{PM} \approx \tan^{-1}\left(\frac{b^2-1}{2b}\right)$. Like before, we select $b = 1 + \sqrt{2}$, which gives $\mathrm{PM} \approx 45°$. Substituting $Q = 1/\sqrt{2}$, $\omega_{nf} = 2\pi 50$ rad/s, and $b = 1 + \sqrt{2}$ into (20) gives $k_p = 92$ $k_i = 3507.1$.

Fig. 22 shows the open-loop Bode plot of the NF-PLL. It can be observed that the PM of the PLL is close to the intended PM, i.e., $\mathrm{PM} \approx 45°$, which confirms the accuracy of approximation made during the design procedure.

B. Performance Evaluation

Fig. 23 shows the NF-PLL simulation result under the test case 1. It can be observed that the NF-PLL effectively suppresses the dc offset even when the deviation of grid frequency from its nominal value is high.

The NF-PLL dynamic performance is evaluated under the test case 2. The obtained results are shown in Fig. 24. The settling time of the NF-PLL is 63.9 ms, which indicates a rather slow transient response. The slow dynamic response of

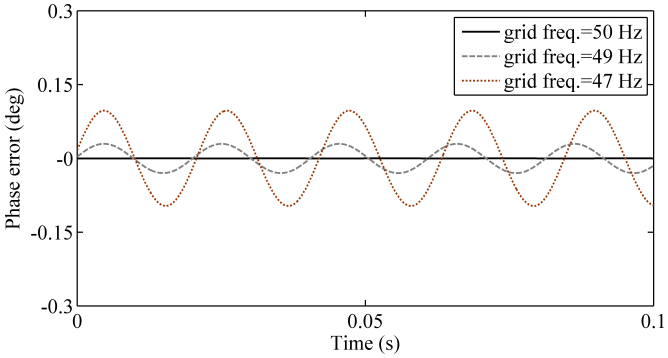

Fig. 23. The NF-PLL simulation results under the test case 1.

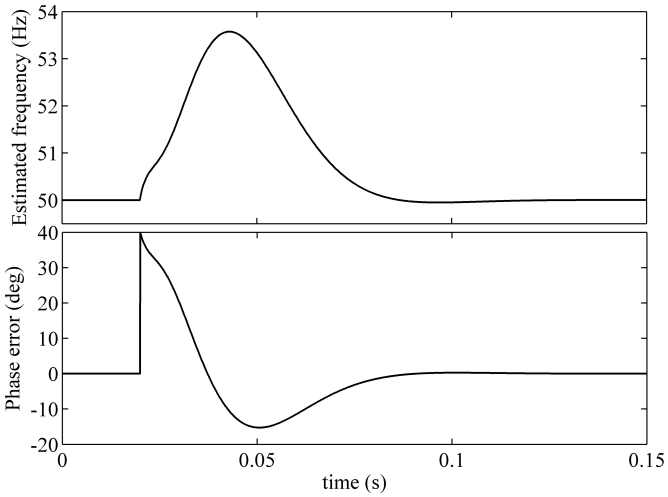

Fig. 24. Simulation results for the NF-PLL under the test case 2.

the NF-PLL is mainly due to the considerable phase delay caused by the wide-bandwidth NF in the PLL control loop. Therefore, depending on the application is hand, the following modifications can be applied to improve the NF-PLL dynamic behavior:

1) For applications where small variations for the grid frequency are expected, the transient behavior of the NF-PLL can be improved by replacing the wide-bandwidth non-adaptive NF by a narrow-bandwidth one.
2) For applications where large frequency variations are anticipated, a narrow-bandwidth adaptive NF can be employed. Different approaches to realize adaptive NFs can be found in [37], [38].

C. Extension to the Harmonically Distorted and Unbalanced Grid Condition

To improve the disturbance rejection capability of the NF-PLL under unbalanced and distorted grid conditions, additional NFs can be included into its control loop. In most practical cases, the harmonic components of order $h = -5, +7, -11, +13$ are dominant harmonic components in the grid voltage. These components are sensed by the PLL control loop as the $h = \pm 6, \pm 12$ order components. On the other hand, the FFNS component in the grid voltage, as mentioned before, is sensed as a double frequency component in the PLL control

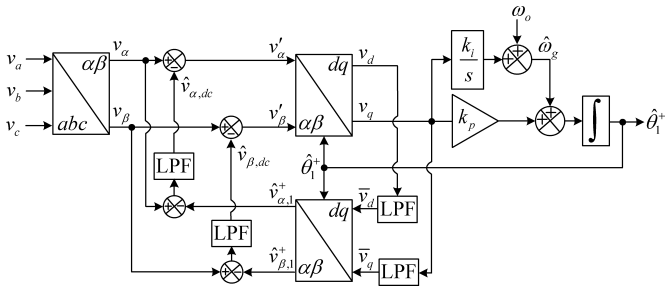

Fig. 25. Schematic diagram of the CFN-PLL.

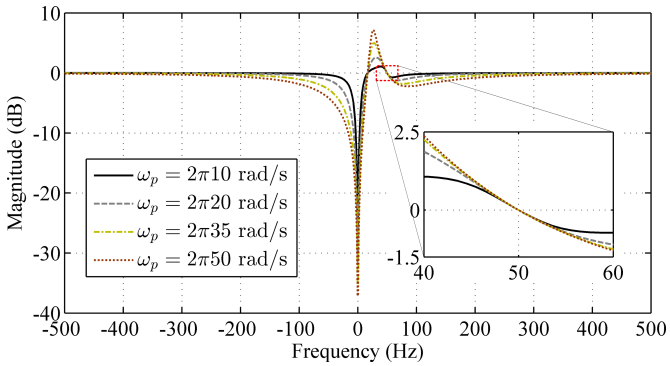

Fig. 26. Bode magnitude plot of the transfer function (23).

loop. Therefore, using three extra NFs with notch frequencies at $2\pi(2{\cdot}50)$, $2\pi(6{\cdot}50)$, and $2\pi(12{\cdot}50)$ rad/s in the PLL control loop is good enough for the most practical cases. Nevertheless, if the rejection of more harmonic components is required, more NFs can be included in the PLL control loop, but at the cost of higher computational effort.

V. DC Offset Removal Using Cross-Feedback Network

Fig. 25 shows the schematic diagram of the conventional SRF-PLL with a cross-feedback network (CFN), which is called the CFN-PLL. The LPF block in this structure can be any kind of LPF. Throughout this paper, it is considered to be a first-order LPF with transfer function of the form $\mathrm{LPF}(s) = \omega_p/(s+\omega_p)$, where ω_p is its cutoff frequency. To ensure the CFN-PLL is insensitive to the grid voltage amplitude variations, the PI controller input, v_q, can be divided by $\bar{v}_d$, which is an estimation of grid voltage amplitude.

The operation principle of the CFN is as follows. First, the d-axis and q-axis voltage components are passed through two LPFs to remove their possible disturbances. The filtered d- and q-axis voltage components are then transformed back to the stationary ($\alpha\beta$) reference frame, which yields an estimation of the grid voltage FFPS components. These components are then subtracted from the grid voltage signals and passed through two LPFs, which gives an estimation of the grid voltage dc components. These dc components are finally subtracted from the grid voltage signals, which removes the dc offset from the SRF-PLL input. To better visualize the effectiveness of CFN, the transfer function relating the SRF-PLL inputs (i.e., v'_α and v'_β) to the grid voltage signals (i.e., v_α and v_β) are derived in the following.

From Fig. 25, the SRF-PLL input and the estimated FFPS component can be described in the space vector notation as

$$\begin{aligned}\boldsymbol{v}'_{\alpha\beta}(s) &= \boldsymbol{v}_{\alpha\beta}(s) - \hat{\boldsymbol{v}}_{\alpha\beta,dc}(s)\\ &= (1-\mathrm{LPF}(s))\,\boldsymbol{v}_{\alpha\beta}(s) + \mathrm{LPF}(s)\hat{\boldsymbol{v}}^+_{\alpha\beta,1}(s)\end{aligned} \quad (21)$$

$$\hat{\boldsymbol{v}}^+_{\alpha\beta,1}(s) = \mathrm{LPF}(s-j\hat{\omega}_g)\boldsymbol{v}'_{\alpha\beta}(s) \quad (22)$$

where, $\hat{\boldsymbol{v}}^+_{\alpha\beta,1}(s) = \hat{v}^+_{\alpha,1} + j\hat{v}^+_{\beta,1}$, $\boldsymbol{v}'_{\alpha\beta}(s) = v'_\alpha + jv'_\beta$, and $\hat{\boldsymbol{v}}_{\alpha\beta,dc}(s) = \hat{v}_{\alpha,dc}(s) + j\hat{v}_{\beta,dc}(s)$. Substituting (22) into (21) gives the transfer function relating the grid voltage and the SRF-PLL input as

$$\frac{\boldsymbol{v}'_{\alpha\beta}(s)}{\boldsymbol{v}_{\alpha\beta}(s)} = \frac{1-\mathrm{LPF}(s)}{1-\mathrm{LPF}(s)\mathrm{LPF}(s-j\hat{\omega}_g)}. \quad (23)$$

Fig. 26 shows the Bode magnitude plot of (23). It can be observed that regardless of the value of the LPF cutoff frequency, the CFN completely blocks the dc component and passes the FFPS component.

A. Design Considerations

Selecting a proper value for the LPF cutoff frequency is the first step of the design procedure. To simplify this task, the transfer function between the dc components estimated by the CFN and the grid voltage signals is first determined. Substituting (21) into (23) and performing some simple mathematical manipulations give this transfer function as

$$\frac{\hat{\boldsymbol{v}}_{dc,\alpha\beta}(s)}{\boldsymbol{v}_{\alpha\beta}(s)} = \frac{\mathrm{LPF}(s)\,[1-\mathrm{LPF}(s-j\hat{\omega}_g)]}{1-\mathrm{LPF}(s)\mathrm{LPF}(s-j\hat{\omega}_g)}. \quad (24)$$

The solid lines in Fig. 27 shows the magnitude frequency response of (24) for different values of the LPF cutoff frequency. To provide a base for comparison, the magnitude frequency response of a first order LPF is also shown in this figure. It can be observed that the frequency response of (24) converges to that of first-order LPF for small values of ω_p, which implies the CFN provides a rather slow and well-damped dynamic response for small values of ω_p. The dynamic response of CFN, however, becomes fast and oscillatory[2] for large values of ω_p. Therefore, selecting the LPF cutoff frequency ω_p involves a tradeoff between the speed of response and damping. To achieve a satisfactory compromise, $\omega_p = 2\pi 15$ rad/s is selected in this paper.

The selected value for the LPF cutoff frequency ensures that the CFN has a rather small effect on the SRF-PLL dynamic behavior. This fact can be confirmed using the simulation results. Therefore, in selecting the proportional and integral gains k_p and k_i, the dynamic interaction between the CFN and the SRF-PLL can be neglected, and the same design approach as that of the conventional SRF-PLL (i.e., defining $k_p = 2\zeta\omega_n$ and $k_i = \omega_n^2$, and selecting appropriate values for ζ and ω_n) can be used for their selection. Like before $\zeta = 1/\sqrt{2}$ is selected which ensures the optimum damping, and $\omega_n = 2\pi 17$ rad/s is chosen, which provides a fast dynamic response (a settling time of around two cycles of the nominal

[2]The oscillatory dynamic response of the CFN when choosing a large value of ω_p can be inferred from relatively large peaks in its frequency response and can be confirmed through numerical results.

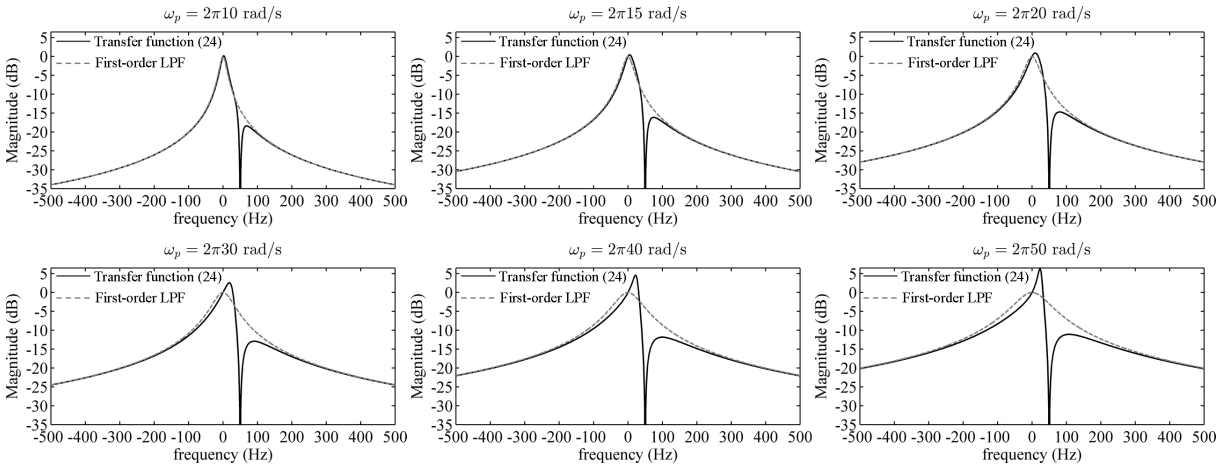

Fig. 27. Magnitude frequency response of (24) and a first-order LPF for different values of the cutoff frequency ω_p.

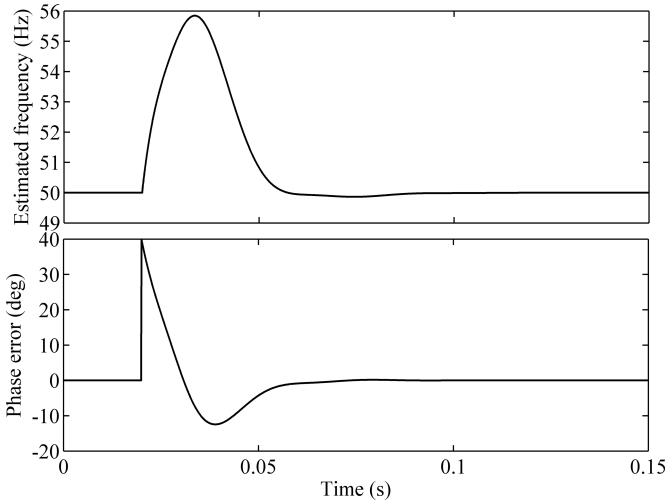

Fig. 28. CFN-PLL simulation under the test case 2.

frequency) for the PLL. These selections result in $k_p = 151$ and $k_i = 11409$.

B. Performance Evaluation

The CFN-PLL can provide a zero steady-state phase error under the test case 1 regardless the value of grid frequency. These results are not shown here due to space limitations. Fig. 28 shows the CFN-PLL simulation results under the test case 2. The settling time of the CFN-PLL is 41 ms, which confirms the fast dynamic response of this PLL. The CFN-PLL fast transient response can also be confirmed under the test case 3.

C. Extension to the Harmonically Distorted and Unbalanced Grid Condition

Extension of the CFN to take into account the low order harmonic components can be carried out by adding extra synchronous reference frames rotating at the desired angular speeds to the standard structure. Considering the extra computational effort that removal of each harmonic component demands (i.e., two LPFs, two trigonometric function calculation,

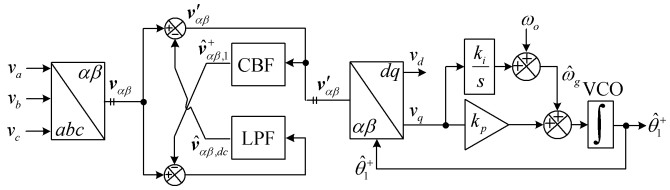

Fig. 29. Block diagram description of the CCF-PLL

and several additions and multiplications), a tradeoff between the computational effort and rejection of harmonics should be found.

VI. DC Offset Removal Using Complex Coefficient Filter

The complex coefficient filters (CCFs) have an asymmetrical frequency response around zero, which enables them to make distinction between the positive and negative polarities (sequences) of the same frequency component. This feature has made them very popular in improving the filtering capability of PLLs [3], [39]-[40].

The removal of dc offset in the PLL input using the CCF is shown in Fig. 29. This PLL structure is called the CCF-PLL. In this approach, the $\alpha\beta$-frame FFPS component is estimated using a complex bandpass filter (CBF) with center frequency at the fundamental frequency of positive sequence. Equation (25) describes the CBF transfer function, Fig 30 shows its Bode magnitude plot, and Fig. 31 shows its s-domain implementation.

$$\mathrm{CBF}(s) = \frac{\omega_p}{s - j\omega_g + \omega_p}. \tag{25}$$

As the Bode plot shows, the CBF only passes the FFPS component and attenuates other frequency components. The extracted FFPS component by the CBF, as shown in Fig. 29, is subtracted from the grid voltage signal and passed through the LPF, which give an estimation of dc component. The dc component is finally subtracted from the grid voltage and fed to the SRF-PLL. Notice that the frequency estimated by the SRF-PLL should be fed back to the CBF to make it frequency

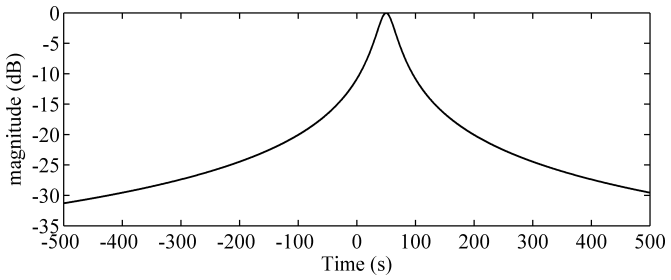

Fig. 30. Bode magnitude plot of (25) for $\omega_g = 2\pi 50$ rad/s and $\omega_p = 2\pi 15$ rad/s.

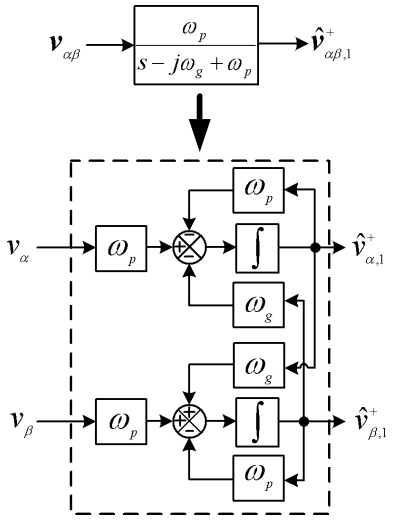

Fig. 31. Implementation of the CBF.

adaptive. The voltage-controlled oscillator (VCO) input, which provides a faster estimate for the grid frequency than the integrator output (within the PI unit), is used for this purpose.

A. Equivalence of the CCF-PLL and CFN-PLL

Here, it is shown that the CCF-PLL and CFN-PLL are mathematically equivalent systems, which implies the same design procedure as that proposed for the CFN-PLL can be applied for selecting the CCF-PLL control parameters. This equivalence also shows that the dynamic performance and disturbance rejection capability of the CCF-PLL are the same as those of the CFN-PLL.

From Fig. 29, the SRF-PLL input signal can be expressed in the space vector notation as

$$\begin{aligned}\boldsymbol{v}'_{\alpha\beta}(s) &= \boldsymbol{v}_{\alpha\beta}(s) - \hat{\boldsymbol{v}}_{\alpha\beta,dc}(s) \\ &= (1-\mathrm{LPF}(s))\,\boldsymbol{v}_{\alpha\beta}(s) + \mathrm{LPF}(s)\hat{\boldsymbol{v}}^{+}_{\alpha\beta,1}(s) \\ &= (1-\mathrm{LPF}(s))\,\boldsymbol{v}_{\alpha\beta}(s) + \mathrm{LPF}(s)\mathrm{CBF}(s)\boldsymbol{v}'_{\alpha\beta}(s). \quad (26)\end{aligned}$$

Using (26), the transfer function relating the SRF-PLL input (i.e., $\boldsymbol{v}'_{\alpha\beta}$) and the grid voltage (i.e., $\boldsymbol{v}_{\alpha\beta}$) can be obtained as

$$\frac{\boldsymbol{v}'_{\alpha\beta}(s)}{\boldsymbol{v}_{\alpha\beta}(s)} = \frac{1-\mathrm{LPF}(s)}{1-\mathrm{LPF}(s)\underbrace{\mathrm{CBF}(s)}_{\mathrm{LPF}(s-j\hat{\omega}_g)}}. \quad (27)$$

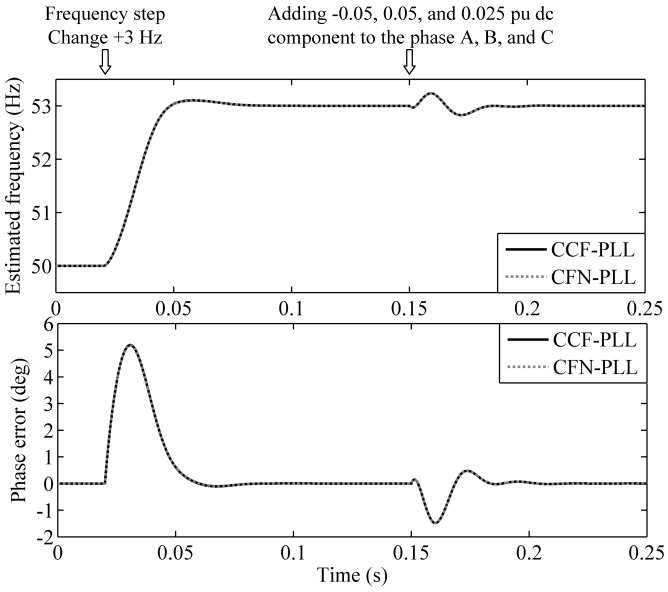

Fig. 32. A comparison between the dynamic performance and dc offset rejection capability of the CCF-PLL and CFN-PLL. Control parameters: $k_p = 151$, $k_i = 11409$, and $\omega_p = 2\pi 15$ rad/s.

It can be observed this transfer function is the same as (23), which confirms the CCF-PLL and CFN-PLL are mathematically equivalent systems.

To support this mathematical analysis, the dynamic performance and dc-offset rejection capability of the CCF-PLL and CFN-PLL are compared through simulation results, as shown in Fig. 32. As expected, both PLLs give well-matched responses.

B. Extension to the Harmonically Distorted and Unbalanced Grid Condition

Extension of this approach to take into account the low order harmonic components can be easily carried out by adding extra CBFs with center frequency at the targeted harmonic components.

VII. Summary of Results

Table I summarizes the obtained results. It can be observed that the *dq*DSC-PLL provides a good dc offset rejection capability particularly when the grid frequency is close to its nominal value; however, it suffers from a rather slow transient response. Using the PLC in the *dq*DSC-PLL control loop, as can be seen, improves the PLL dynamic response, but degrades its dc offset rejection capability. The performance of the NF-PLL is comparable with the *dq*DSC-PLL performance. The $\alpha\beta$DSC-PLL, CFN-PLL, and CCF-PLL, all demonstrate a fast dynamic response and excellent dc offset rejection capability. It should be mentioned that in our appraisal about the PLLs dynamic behavior, more weight has been given to the results of the phase-angle jump test than those of frequency step change test. The reason is that the grid frequency has a stable nature in practice and its step (sudden) variations are not expected.

TABLE I
SUMMARY OF RESULTS.

	***dq*DSC-PLL without PLC / with PLC**	**$\alpha\beta$DSC-PLL with PEC**	**NF-PLL**	**CFN-PLL/CCF-PLL**
dc offset rejection capability				
Peak-to-peak Oscillatory error ($f = 50$ Hz)	0° / 0°	0°	0°	0°
Peak-to-peak Oscillatory error ($f = 49$ Hz)	0.059° / 0.197°	0°	0.059°	0°
Peak-to-peak Oscillatory error ($f = 47$ Hz)	0.188° / 0.647°	0°	0.194°	0°
+40° phase-angle jump				
2% settling-time	72 ms (3.6 cycles) / 47.4 ms (2.37 cycles)	44.4 ms (2.22 cycles)	63.9 ms (3.19 cycles)	41 ms (2.05 cycles)
Phase overshot	14.69° (36.72%) / 16.23° (40.57%)	14.17° (35.43%)	15.26° (38.15%)	12.4° (31%)
Peak frequency error	3.21 Hz / 5.42 Hz	5.32 Hz	3.57 Hz	5.8 Hz
+3 Hz frequency step change				
2% settling-time	58.1 ms (2.9 cycles) / 57.8 ms (2.92 cycles)	52.8 ms (2.64 cycles)	51.8 ms (2.59 cycles)	49.6 ms (2.48 cycles)
Frequency overshoot	0.03 Hz (1%) / 0.13 Hz (4.3%)	0.11 Hz (3.6%)	0.03 Hz (1%)	0.1 Hz (3.33%)
Peak phase error	11.49° / 7.1°	6.65°	10.44°	5.18°
Stability margin				
Phase margin	43.8° / 45°	58.9°	43.2°	—
Gain margin	29.5 dB / 21 dB	−10.2 dB	27.3 dB	—
DC component Estimation	No / No	No	No	Yes

VIII. CONCLUSION

In this paper a detailed analysis of several techniques to deal with the problem of the dc offset in PLL algorithms has been presented. Using the *dq*DSC operator as the PLL in-loop filtering stage was the first technique. It was shown that the *dq*DSC operator can significantly improve the dc offset rejecting capability of the PLL, but at the cost of slowing down its dynamic response. To tackle this issue, incorporating a special lead compensator into the PLL control was suggested. it was shown that the lead compensator effectively compensates the phase delay induced by the *dq*DSC operator and, therefore, enables the *dq*DSC-PLL to achieve a faster dynamic response without jeopardizing its stability margins. The dc offset reaction capability of the *dq*DSC-PLL with phase lead compensator is also acceptable. The control parameter design guidelines were also presented.

Using the $\alpha\beta$DSC operator as the PLL pre-filtering stage was the second technique. It was shown that $\alpha\beta$DSC operator completely blocks the dc offset regardless of the grid voltage frequency value. To eliminate the need for adapting the $\alpha\beta$DSC operator to the grid frequency variations, a simple yet effective method was proposed. The small-signal modeling, the stability analysis, and the design guidelines were other contributions of this part.

Employing the wide-bandwidth NF as the PLL in-loop filtering stage was the third technique. A systematic method to design the control parameters of the NF-PLL was proposed and its performance was analyzed. It was shown that the NF enables the PLL to effectively suppress the fundamental frequency oscillatory errors caused by the dc offset, but at the cost of slowing down its dynamic response. Improving the dynamic performance of the NF-PLL was also briefly discussed.

Using the CFN was the fourth technique. The complete rejection of the dc offset from the PLL input, providing an estimation of the grid voltage dc component, and having a fast dynamic response can be considered as the main advantages of this technique.

Using the CCF was the last technique. It was shown that this technique is mathematically equivalent with the CFN based method. Therefore, it offers the same advantages of the CFN based method.

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