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Design of the Trap Filter for the High Power Converters with Parallel Interleaved VSCs

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***Abstract*—The power handling capability of the state-of-the-art semiconductor devices is limited. Therefore, the Voltage Source Converters (VSCs) are often connected in parallel to realize high power converter. The switching frequency semiconductor devices, used in the high power VSCs, is also limited. Therefore, large filter components are often required in order to meet the stringent grid code requirements imposed by the utility. As a result, the size, weight and cost of the overall system increase. The use of interleaved carriers of the parallel connected VSCs, along with the high order line filter, is proposed to reduce the value of the filter components. The theoretical harmonic spectrum of the average pole voltage of two interleaved VSCs is derived and the reduction in the magnitude of some of the harmonic components due to the carrier interleaving is demonstrated. A shunt LC trap branch is used to sink the dominant harmonic frequency components. The design procedure of the line filter is illustrated and the filter performance is also verified by performing the simulation and the experimental study.**

***Index Terms*—Voltage source converters (VSC), parallel, interleaving, filter design, trap filter**

I. Introduction

The focus on producing electricity from the renewable energy sources is increasing and Wind Energy Conversion System (WECS) is receiving considerable attention [1]. In order to achieve increased penetration of the wind energy sources, better power quality output and the ability to control the inductive/capacitive reactive power is required [2]. The power electronics converters play a vital role in integrating these energy sources to the power system [3]. The wind turbines with a power rating in Megawatts range are often connected to the power system using full power converter. This converter is often realized using a three-phase two-level Pulse Width Modulated (PWM) Voltage Source Converter (VSC) [2].

The switching frequency of the semiconductor devices, employed in the high power converters, is limited and large filters are often required in order to meet the stringent grid code requirements imposed by the utility [4]. These filters occupy significant amount of space in the overall system [5] and hampers the achievable power density. As a result, the cost of the overall converter system including platform cost [1] increases. Due to the limited power handling capability of the semiconductor switches, the VSCs are often connected in parallel [6]–[9] to achieve higher power rating and can be operated with interleaved carriers. The interleaved carriers can help reducing the requirement of both ac line filter and dc-link capacitor [10]–[15].

The phase shift in the respective pole voltages (measured with respect to the center point of the dc link O in Fig. 1) due to the interleaved carriers, give rise to the high frequency circulating current between the parallel connected VSCs. This unwanted current introduces additional losses and increases the stress on both the semiconductor devices and the filter components. Therefore, the circulating current should be suppressed by introducing additional impedance in the circulating current path. Using Coupled Inductor (CI) with inverse coupling can effectively reduce the circulating current [12], [16]–[20]. If the current between the parallel VSCs are shared equally, the fundamental frequency component in flux in the core is zero. As a result, the core is only subjected to the high frequency excitation. The magnetic flux has frequency components concentrated around the odd multiple of the switching frequency. Due to the high frequency operation of the CI, its impact on the power density is minimal.

For the line current filtering, the use of the high order filter is advisable, specially in the high power grid-connected converters. The LCL filter is commonly used in the WECS [2]. The design guidelines for the selection of the LCL filter parameters is discussed in [21]–[23]. The converter-side inductor limits the current ripple through the semiconductor switches and the minimum value of this inductor is determined by the maximum value of the allowable switch current ripple. The high value of converter-side inductor and grid-side inductor cause more voltage drop across them and requires high value of the dc-link voltage. The shunt capacitive branch in the LCL filter draws reactive power, and it should be made as small as possible. Parallel RC damping is often used and selecting the damping capacitor equal to the the filter capacitance is a good design choice [5]. Therefore, small filter capacitance would also result in low reactive current drawn by the damping capacitor and low losses in the damping resistor. Moreover, the value of the filter components can be further reduced by using shunt trap branch, tuned to attenuate the major harmonic components [24], [25].

This paper presents the use of a line filter with LC trap branch for the high power WECS, comprised of two parallel interleaved VSCs. The analysis shows that the substantial reduction in the value of the filter parameters can be achieved. The paper is organized as follows: The operation of the parallel interleaved VSCs is briefly described in Section II. The design constraints are stated in Section III. The design of the line filter is given in Section IV. The simulation and the experimental

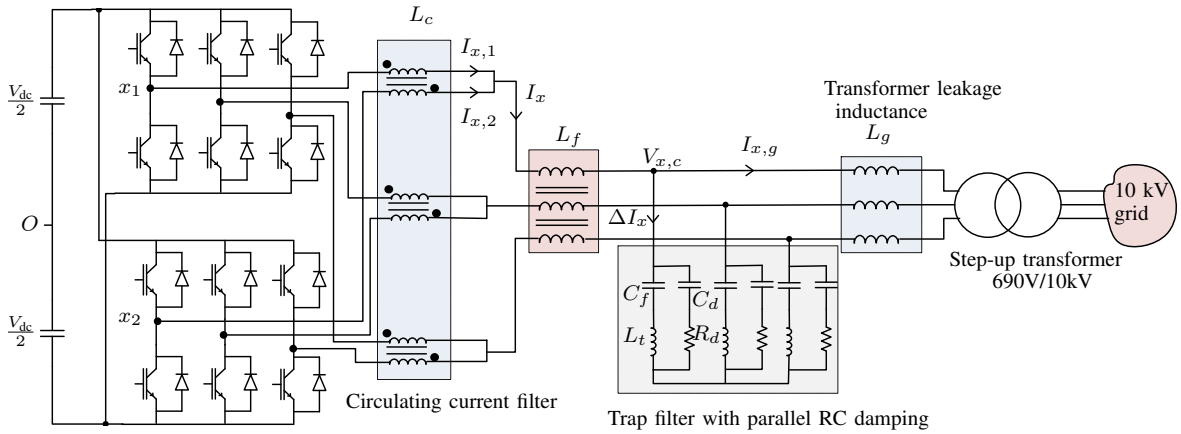

Fig. 1. Parallel interleaved VSCs with circulating current filter and line filter for WECS. A step-up transformer is used for WECS integration to the 10 kV power system. $x = \{A, B, C\}$.

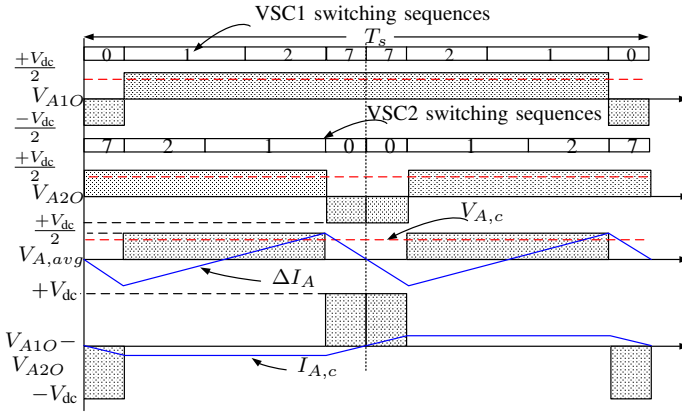

Fig. 2. Pole voltages and currents of phase A of interleaved VSCs: Modulation index=1 and reference vector angle $\psi = 20°$. The interleaving angle is taken to be 180°.

results are finally presented in Section V.

II. System Description

Two parallel interleaved VSCs with a common dc-link is considered for the WECS, and its schematic is shown in Fig. 1. The pole voltages of phase A of both VSCs for center aligned Space Vector Modulation (SVM) are shown in Fig. 2. The pole voltages (V_{A10}, V_{A20}) are phase shifted by an interleaving angle. The resultant pole voltage ($V_{A,avg}$) is an average of the individual pole voltages, and it is also depicted in Fig. 2. The difference between the resultant pole voltage and the voltage across the LC shunt branch appears across the converter side filter inductor L_f. Due to the unipolar nature of the resultant pole voltage, the ripple in the resultant current is small. Moreover, the frequency of the ripple current is two times the switching frequency. As a result the size of the grid side inductor and capacitive filter can be reduced. For a high power, low switching frequency VSCs, this feature greatly helps in meeting the Total Harmonic Distortion (THD) requirement with the small value of the filter components.

A. The Circulating Current

The instantaneous voltage difference between the pole voltages give rise to the circulating current and causes additional loss and stress in the semiconductor switches and the passive components. The phase currents $I_{x,1}$ and $I_{x,2}$ have two distinct components. One contributes to the resultant current (I_x), while the other one is the circulating current. Therefore, the phase current can be decomposed into two components, and it is given as

$$\begin{aligned} I_{x,1} &= I_{x1} + I_{x,c} \\ I_{x,2} &= I_{x2} - I_{x,c} \end{aligned} \tag{1}$$

where, x = Phase $[A, B, C]$. I_{x1} and I_{x2} are the components of the phase currents contributing to the resultant current and $I_{x,c}$ is the circulating current. Neglecting the effect of the hardware/control asymmetry, the current components of both the VSCs, contributing to the resultant current are considered equal (I_{x1}=I_{x2}) and the resultant current is given as

$$I_x = 2I_{x1} \tag{2}$$

The circulating current is given as

$$I_{x,c} = \frac{I_{x,1} - I_{x,2}}{2} \tag{3}$$

and the dynamic behavior of the circulating current is described as

$$\frac{dI_{x,c}}{dt} = \frac{V_{x1O} - V_{x2O}}{L_c} \tag{4}$$

where L_c is the inductance offered to the circulating current. The CI is used as a circulating current filter in this system. The construction of the CI without any intentional air-gap offers high inductance to the circulating current. As a result, the circulating current is suppressed effectively, which is demonstrated in the experimental results in Section V.

B. The Grid Current

The resultant current is given as

$$I_x = I_{x,1} + I_{x,2} = I_{x,f} + \Delta I_x \tag{5}$$

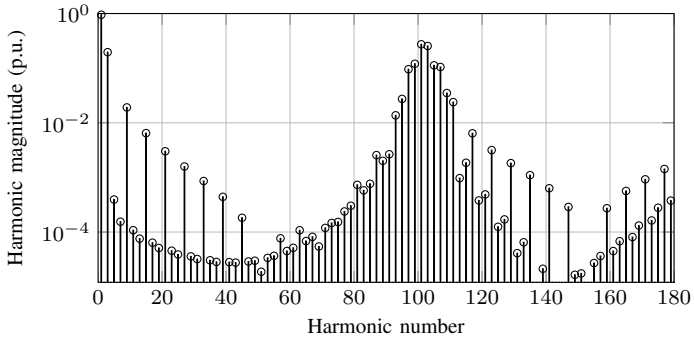

Fig. 3. Theoretical harmonic spectrum of the average pole voltage of the interleaved VSCs with SVM. The interleaving angle is 180°. The modulation index M=0.95 and ω_c/ω_0 = 51.

where $I_{x,f}$ is the fundamental frequency component of the line current and the ΔI_x is the ripple current component. The resultant pole voltage is the average of the individual pole voltages, and it is given as

$$V_{x,avg} = \frac{V_{x1O} + V_{x2O}}{2} \tag{6}$$

This difference between the resultant pole voltage and the grid voltage appears across the line filter. To design the line filter, the harmonic spectrum of the $V_{x,avg}$ for a given modulation strategy is required, and it is derived in the following subsection.

C. Modulation Scheme and the Average Pole Voltage

The SVM scheme is considered. The theoretical harmonic spectra of the $V_{x,avg}$ for the asymmetrical regular sampled SVM is derived for an interleaving angle of 180°. The pole voltages can be represented as a summation series of sinusoids [26], characterized by the carrier index variable m and the baseband index variable n. The harmonic coefficients in the summation series is given by the double Fourier integral, evaluated in each 60°sextant. The closed form solution for the first VSC is given by (7) [26]. The harmonic solution for the second VSC is evaluated for an interleaving angle of 180°. The average of the pole voltages with an interleaving angle of 180°is given by (8). From (8), it is evident that the contribution to the individual harmonic components from the odd multiple of the carrier frequency components is zero. This is evident from (8), where each summation term has a multiplication factor of $\cos(m\frac{\pi}{2})$. The theoretical harmonic spectra for the average pole voltage is also shown in Fig. 3. The harmonic components in the average pole voltage are mainly concentrated around the even multiple of the carrier frequency. The side-band components of the odd multiple of the carrier frequency harmonics are reduced considerably as a result of the interleaved carriers.

III. Design Constraints

The WECS, connected to the 10 kV medium-voltage network through a step-up transformer, is considered. The grid voltage is assumed to vary by $\pm 10\%$. For grid support functions, the WECS is required to inject inductive/capacitive reactive power within a specified range. An interleaving angle of 180°cancels the dominant first order side band harmonics [14], and it is used in this paper.

A. Limits on the Injected Harmonics

The harmonic injection limit, set by the German Association of Energy and Water Industries (BDEW) standard [4], [23], [27] for the renewable energy sources connected to the medium voltage network, is considered in this paper. Based on the Short-Circuit Ratio (SCR) at the point of common coupling, the individual harmonic current injection limit is specified [4]. The grid filter design should ensure that the individual harmonic component in the grid current meets the specified harmonic injection limits for the given switching frequency and the modulation scheme. The SCR of 20 is taken for the filter design in this paper and the limits on the individual harmonic components are calculated on the low voltage side as per BDEW standard.

B. Peak Switch Current

The semiconductor switch current rating along with the permissible stress on the semiconductor switch determine allowable the maximum switch current ripple. For the VSC modulated using SVM and operating at unity power factor, the maximum ripple current occurs when the fundamental current component is also at its peak. The voltage difference between the resultant pole voltage and the voltage across the LC trap branch appears across the converter side filter L_f. The time integral of this voltage difference, along with the inductance value of L_f, decides the current ripple in the line current. therefore, the current ripple is a function of the dc-link voltage, the switching frequency, the modulation depth and the converter side inductor L_f, and it is derived hereafter.

Due to the use of discrete vectors to synthesize the reference vector, an error between the applied voltage vector and the reference vector exists. The harmonic flux vector, which is a time integral of the error voltage vector, is directly related to the ripple current [28], [29], and it is used to derive the maximum peak-to-peak current ripple. For phase A, the peak current occurs when the reference vector angle is $\psi = 0°$. At this instant, it is sufficient to evaluate only d-axis current component in order to obtain the phase A current. The d-axis harmonic flux vector is given by

$$\overrightarrow{\boldsymbol{Vd}}_{\boldsymbol{err,1}} T_1 = \tfrac{2}{3} V_{\rm dc}[\cos\psi - \tfrac{3}{4}M]T_1 \tag{9a}$$

$$\overrightarrow{\boldsymbol{Vd}}_{\boldsymbol{err,2}} T_2 = \tfrac{2}{3} V_{\rm dc}[\cos(60° - \psi) - \tfrac{3}{4}M]T_2 \tag{9b}$$

$$\overrightarrow{\boldsymbol{Vd}}_{\boldsymbol{err,z}} T_z = -\tfrac{1}{2} V_{\rm dc} M T_z \tag{9c}$$

where T_1, T_2 and T_z are the dwell time of voltage vector $\overrightarrow{\boldsymbol{V_1}}$, $\overrightarrow{\boldsymbol{V_2}}$ and $\overrightarrow{\boldsymbol{V_0}}/\overrightarrow{\boldsymbol{V_7}}$, respectively. $V_{\rm dc}$ is the dc-link voltage and the M is the modulation index. For $\psi = 0°$, the reference space vector is synthesized by applying the voltage vectors $\overrightarrow{\boldsymbol{V_1}}$ and $\overrightarrow{\boldsymbol{V_0}}/\overrightarrow{\boldsymbol{V_7}}$.

$$Amn,1 = \frac{4V_{\text{dc}}}{q\pi^2} \times \begin{pmatrix} \frac{\pi}{6}\sin[(m+n)\frac{\pi}{2}]\{J_n(q\frac{3\pi}{4}M) + 2\cos(\frac{n\pi}{6})J_n(q\frac{\sqrt{3}\pi}{4}M)\} \\ +\frac{1}{n}\sin(\frac{m\pi}{2})\cos(\frac{n\pi}{2})\sin(\frac{n\pi}{6})\{J_0(q\frac{3\pi}{4}M) - J_0(q\frac{\sqrt{3}\pi}{4}M)\}|n \neq 0 \\ + \sum\limits_{\substack{k=1 \\ k\neq -n}}^{\infty} \frac{1}{n+k}\sin\left([m+k]\frac{\pi}{2}\right)\cos\left([n+k]\frac{\pi}{2}\right)\sin\left([n+k]\frac{\pi}{6}\right) \\ \times\left\{J_k(q\frac{3\pi}{4}M) + 2\cos\left([2n+3k]\frac{\pi}{6}\right)\left\{J_k(q\frac{\sqrt{3}\pi}{4}M)\right\}\right. \\ + \sum\limits_{\substack{k=1 \\ k\neq n}}^{\infty} \frac{1}{n-k}\sin\left([m+k]\frac{\pi}{2}\right)\cos\left([n-k]\frac{\pi}{2}\right)\sin\left([n-k]\frac{\pi}{6}\right) \\ \times\left\{J_k(q\frac{3\pi}{4}M) + 2\cos\left([2n-3k]\frac{\pi}{6}\right)\left\{J_k(q\frac{\sqrt{3}\pi}{4}M)\right\}\right. \end{pmatrix} \tag{7}$$

$$Amn,avg = \frac{4V_{\text{dc}}}{q\pi^2} \times \begin{pmatrix} \frac{\pi}{6}\cos(m\frac{\pi}{2})\sin(n\frac{\pi}{2})\{J_n(q\frac{3\pi}{4}M) + 2\cos(\frac{n\pi}{6})J_n(q\frac{\sqrt{3}\pi}{4}M)\} \\ + \sum\limits_{\substack{k=1 \\ k\neq -n}}^{\infty} \frac{1}{n+k}\cos(m\frac{\pi}{2})\sin(k\frac{\pi}{2})\cos\left([n+k]\frac{\pi}{2}\right)\sin\left([n+k]\frac{\pi}{6}\right) \\ \times\left\{J_k(q\frac{3\pi}{4}M) + 2\cos\left([2n+3k]\frac{\pi}{6}\right)\left\{J_k(q\frac{\sqrt{3}\pi}{4}M)\right\}\right. \\ + \sum\limits_{\substack{k=1 \\ k\neq n}}^{\infty} \frac{1}{n-k}\cos(m\frac{\pi}{2})\sin(k\frac{\pi}{2})\cos\left([n-k]\frac{\pi}{2}\right)\sin\left([n-k]\frac{\pi}{6}\right) \\ \times\left\{J_k(q\frac{3\pi}{4}M) + 2\cos\left([2n-3k]\frac{\pi}{6}\right)\left\{J_k(q\frac{\sqrt{3}\pi}{4}M)\right\}\right. \end{pmatrix} \tag{8}$$

where V_{dc} is the dc-link voltage, M is the modulation index, and $q = m + n(\omega_0/\omega_c)$.

The peak-to-peak ripple current is given as,

$$\Delta I_{x1,pp} = \Delta I_{x2,pp} = \frac{V_{\text{dc}}M(1 - \frac{3}{4}M)}{8L_f f_s} \tag{10}$$

where f_s is the switching frequency. For M=2/3, the peak-to-peak ripple current is maximum. However, for the grid-connected applications, the modulation index is close to one in normal operating condition. The M is minimum when the grid voltage is 0.9 pu. Once the range of M is fixed, the minimum converter side inductance $L_{f,min}$ can be obtained for the desired maximum value of the differential peak-to-peak ripple current from (10).

C. Active and Reactive Power Consumption of the Shunt Branch

The grid voltage may vary over a range of 1±0.1 pu. The leakage inductance of the step-up transformer often ranges between 4-6%, and it is considered as a part of the grid side inductance L_g. The voltage across the shunt branch, and therefore the losses and the reactive power consumption also depends on the grid side filter inductance in addition to the grid voltage. The reactive power consumption of the shunt branch is maximum when the grid voltage is 1.1 pu and the constraint on the maximum reactive power consumption is evaluated at this voltage level.

The current injected to the grid is controlled, thus the current flowing through the semiconductor switches, the converter side filter inductor L_f and the circulating current filter L_c can be reduced by reducing the current through the shunt filter branch. The reactive power consumption of the shunt branch is constrained to 0.05 pu with grid voltage of 1.1 pu. The power loss in the damping resistor R_d is also restricted to 0.003 pu.

TABLE I
BASE VALUES FOR PER-UNIT SYSTEM

Parameters	Base Values for analysis	Base Values for experiments
Power	2.2 MVA (2 MW)	11 kVA (10 kW)
Voltage	690 V	400 V
Current	1840 A	15.87 A
Frequency	50 Hz	50 Hz
Inductance	688 μH	46 mH
Capacitance	14709 μF	218 μF

IV. FILTER DESIGN

The filter is designed for a 2.2 MVA system. The analysis and the filter performance is verified by designing a line filter for a small scale setup with a power rating of 11 kVA and performing experiments on the same. The base values for both are given in Table I.

The harmonic coefficients for the average pole voltage of the two interleaved VSCs with an interleaving angle of 180°are given by (8) and the harmonic spectrum is also plotted in Fig. 3. The effect of the sampling on the harmonic distribution is considered in the analytical expression. However, the system unbalances cause odd harmonics, and the dead-time along with the minimum pulse filter generate even harmonics [21]. To consider the effect of these non-ideal conditions, the safety margin of 20% is considered for each harmonic component during the design stage.

For the two parallel interleaved VSCs, the major harmonic

components are concentrated around the 2nd carrier frequency harmonic, as shown in Fig. 3. Considering the safety margin and the dc-link voltage of 1080 V, the admittance required at 2nd carrier frequency harmonic to meet the BDEW standard is -40 dB. The design constraints of 0.1 pu voltage drop across inductors (both converter-side inductor and grid-side inductor) at fundamental frequency and admittance requirement of -40 dB at the double switching frequency translate in the resonant frequency of the LCL filter close to 0.9 kHz. Lower value of the resonant frequency is not desirable, since it requires large value of the filter components and may cause instabilities, if falls within a control bandwidth. Therefore, a LC trap branch tuned to attenuate the 2nd carrier frequency harmonic and its side bands is used, instead of the capacitive branch of the LCL filter to selectively suppress the dominant harmonic components and it is discussed in the following subsection.

A. Trap Filter

In order to provide good attenuation to side bands of the 2nd carrier frequency harmonic, a LC trap branch is used as shown in Fig. 1 and 4. The parameters of the LC trap branch are tuned to resonate at $2 \times f_s$. The choice of values of C_f and L_t affects the quality factor of the trap branch, the peak resonant frequency ω_r, and the reactive power consumption at the fundamental frequency. Assuming the grid to be harmonic free, the filter transfer function for all harmonic components except the fundamental one is given as

$$\frac{I_{x,g}(s)}{V_{x,avg}(s)} = \left(\frac{1}{(L_f + L_g) + \frac{L_f L_g}{L_t}}\right) \frac{s^2 + s\frac{\omega_t}{Q_t} + \omega_t^2}{s(s^2 + s\frac{\omega_r}{Q_r} + \omega_r^2)} \tag{11}$$

The resonant frequency of the trap branch ω_t and the resonant frequency ω_r are

$$\omega_t = \frac{1}{\sqrt{L_t C_f}} = 2f_s, \text{ and } \omega_r = \frac{1}{\sqrt{\left(\frac{L_f L_g}{L_f + L_g} + L_t\right) C_f}} \tag{12}$$

and the quality factors are

$$Q_t = \frac{1}{R_t}\sqrt{\frac{L_t}{C_f}}, \text{ and } Q_r = \frac{1}{R_t}\sqrt{\frac{L_t(L_f + L_g) + L_f L_g}{C_f(L_f + L_g)}} \tag{13}$$

where R_t is the equivalent series resistance of the trap branch. Due to the presence of the complex conjugate poles with the natural frequency of ω_r, the slope of the magnitude plot changes from -20 dB/decade to -60 dB/decade at ω_r. Due to the presence of the complex conjugate zeros with a natural frequency of ω_t, the slope of the magnitude plot again changes to -20 dB/decade. As per the BDEW standard, the limits on the permissible harmonic current injection up to 180$^{\text{th}}$ harmonics are specified. The values of both ω_r and ω_t are chosen to meet the specified harmonic limits. The value of ω_t is taken to be equal to $2 \times f_s$ in order to offer maximum attenuation to 2nd carrier frequency harmonics and its side bands. The selectivity of the trap filter is a measure of its ability to sink any frequencies on either side of the ω_t and the desired selectivity can be obtained by choosing the appropriate values of the LC trap branch. Also the quality factor of the LC trap branch depends on the value of R_t, which is primarily determined by the winding arrangement of the trap inductor L_t.

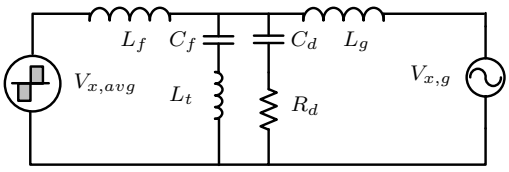

Fig. 4. Trap filter with parallel RC damping.

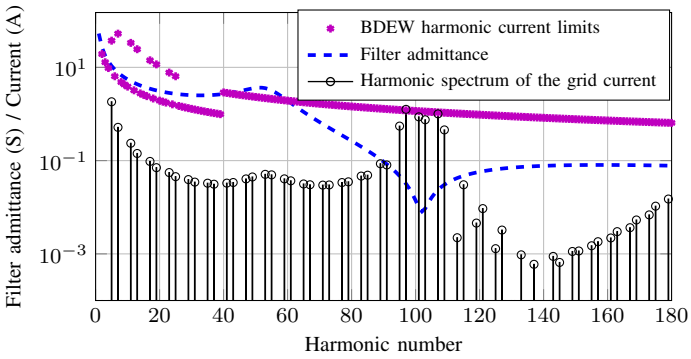

Fig. 5. Trap filter performance: L_f=0.027 pu, L_g=0.06 pu, $C_f + C_d$=0.02 pu, L_t=0.0094 pu.

B. Design

The converter side inductor L_f is selected to comply with the constraint imposed on the peak switch current rating. The peak-to-peak current ripple in the semiconductor switches is to be restricted to 0.4 pu. This maximum switch current restriction translates into the converter-side inductance of L_f = 0.027 pu. The transformer leakage inductance is taken to be 0.06 pu, and it is used as the grid side inductor. This leakage inductance is sufficient enough to meet the harmonic requirements. Thus the use of an additional grid-side inductor is avoided. The value of C_f is taken as 0.01 pu. This results in low reactive power consumption. Also the losses in the damping resistor are small. Due to the use of the trap filter, the grid current harmonics around ω_t are reduced. However, the harmonics around ω_r may get amplified. This may violate the BDEW harmonic limits. Thus passive damping is used to avoid resonance in the line filter.

The $R_d C_d$ parallel damping structure [22] is adopted due to it's easy realization [5], and it is shown in Fig. 4. The selection of the damping branch components affects the reactive power consumption and the power loss. The values of C_d and R_d are optimized to reduce the active and reactive power consumption with the required damping at ω_r. The theoretical harmonic spectrum of the grid current is derived and the filter parameters are chosen to limit the individual harmonic current injection within a specified limit. The magnitude plot of the filter

TABLE II
PARAMETERS FOR SIMULATION AND EXPERIMENTAL STUDY

Parameters	Simulation study	Experiment
Power	2.2 MVA (2 MW)	11 kVA (10 kW)
Switching frequency	2.55 kHz	2.55 kHz
AC voltage (line-to-line)	690 V	400 V
DC-link voltage	1080 V	650 V
L_f	18.6 μH (0.027 pu)	1.3 mH (0.027 pu)
L_g (Transformer leakage)	41.3 μH (0.06 pu)	3.1 mH (0.06 pu)
Filter capacitor C_f	147 μF (0.01 pu)	2.2 μF (0.01 pu)
Trap inductor L_t	6.62 μH (0.0094 pu)	464 μH (0.0094 pu)
Damping capacitor C_d	147 μF (0.01 pu)	2.2 μF (0.01 pu)

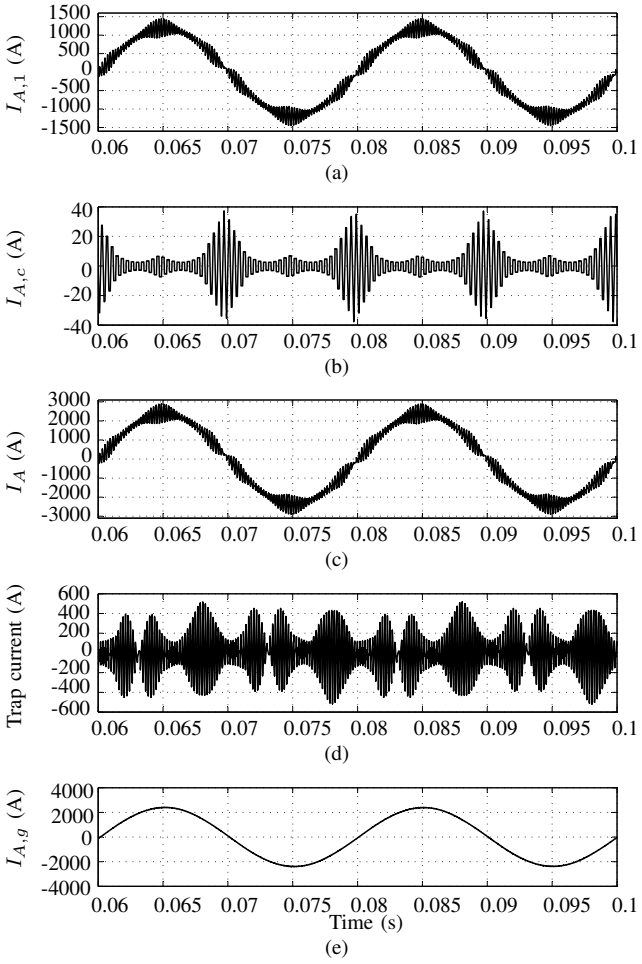

Fig. 6. Simulated VSC currents of phase A with asymmetrical regular sampled SVM. (a) VSC1: Phase A current, (b) Circulating current, (c) Resultant current, (d) Current in trap branch, (e) Grid current.

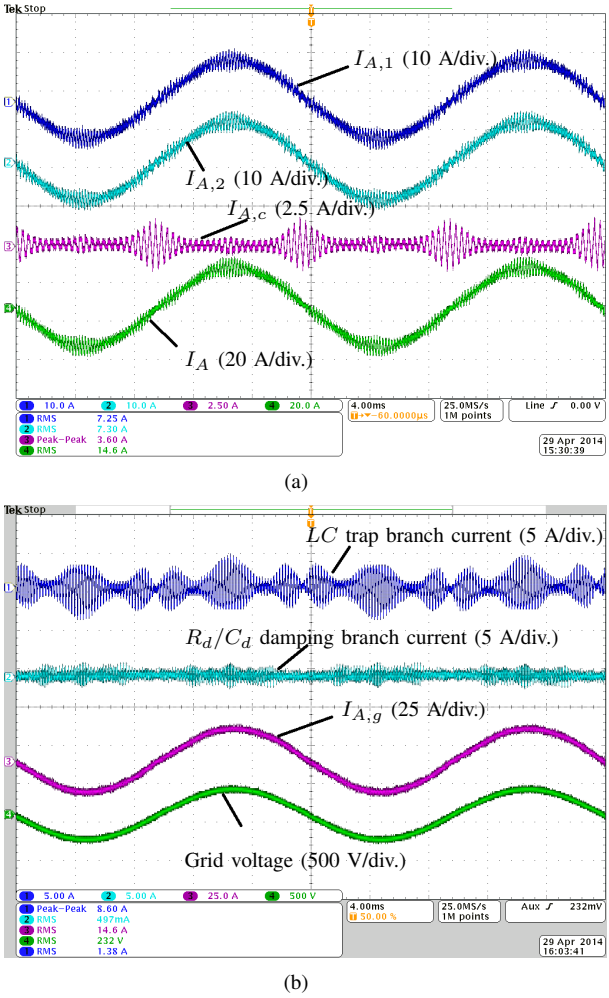

Fig. 7. The experimental results for phase A are obtained at full load with unity power factor.

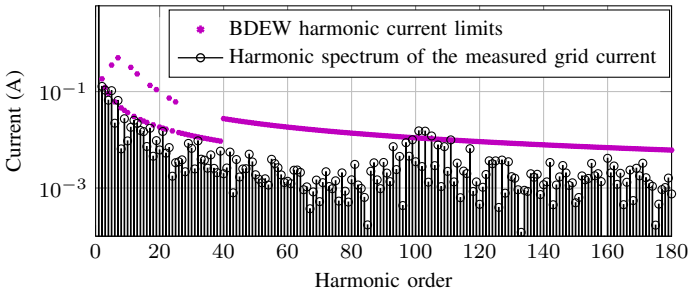

Fig. 8. The filter performance verification: Harmonic spectrum of the measured grid current.

transfer function, along with the theoretical harmonic spectrum of the grid current are plotted in Fig. 5.

V. SIMULATION AND EXPERIMENTAL RESULTS

The parameters used for the simulation and the experimental studies are given in Table II. The simulation results are shown in Fig. 6, where the waveforms corresponding to phase A are depicted. The circulating current is effectively suppressed by using the CI, as shown in Fig. 6(b). Therefore, $I_{A,1} \approx I_{A,2}$ and only phase A current of VSC1 is presented, as shown in Fig. 6(a). The resultant current is the summation of the individual currents, and it is also depicted in Fig. 6(c). The LC trap branch effectively sinks the harmonic frequency components around the $2 \times f_s$. As a result, the desired grid current quality is achieved, as shown in Fig. 6(e).

The experiments have been performed on a small scale

laboratory set-up with the filter parameters specified in Table. II. The AC power source (MX-35) from California Instruments is used as a harmonic free grid emulator. The 3.1 mH inductor is used to mimic the transformer leakage inductance. The rated active power is injected into the grid at the unity power factor. The experimental results are depicted in Fig. 7. The circulating current is effectively suppressed by using the CI, and it is shown in Fig. 7(a). The currents through the trap branch and the damping branch are shown in Fig. 7(b). The THD of the grid current is measured to be 1.9 %. The harmonic spectrum of the measured grid current is shown in Fig. 8 along with the specified harmonic current injection limits. Almost all harmonics are within the allowable limits. However, some of the harmonics around the $2f_s$ are violating the limits due to the high value of ac resistance of the trap branch R_t.

VI. Conclusion

The filter design for the high power converter using parallel interleaved VSCs is demonstrated. The 2.2 MVA, 690V WECS is considered for the analysis. The theoretical harmonic solution of the average pole voltage of two interleaved VSCs, modulated using SVM with an interleaving angle of 180°is derived. Due to the interleaving the major harmonics in the average pole voltage is concentrated around the twice of the carrier frequency. The filter with LC trap branch is designed to restrict the individual harmonic injection within the limit prescribed by the BDEW standard. The desired harmonic performance is achieved with a small value of the converter-side inductor. The transformer leakage inductance is used as a grid-side inductance and the use of any additional inductor on the grid-side is avoided. The capacitor requirement in the shunt branch is 0.02 pu, which results in low reactive power consumption and low losses in the damping branch.

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