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Zhao, Xin; Wu, Xiaohua; Meng, Lexuan; Guerrero, Josep M.; Vasquez, Juan Carlos

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A Direct Voltage Unbalance Compensation Strategy for Islanded Microgrids

Xin Zhao, Xiaohua Wu
School of Automation
Northwestern Polytechnical University
Xi'an, China
zx57@mail.nwpu.edu.cn, wxh@nwpu.edu.cn

Lexuan Meng, Josep M. Guerrero, Juan C. Vasquez
Department of Energy Technology
Aalborg University, Denmark
www.microgrids.et.aau.dk
{lme, joz, juq}@et.aau.dk

***Abstract*—In this paper, a control strategy with low bandwidth communications for paralleled three-phase inverters is proposed to achieve satisfactory voltage unbalance compensation. The proposed control algorithm mainly consists of voltage/current inner loop controllers, a droop controller, a selective virtual impedance loop, and an unbalance compensator. The inner loop controllers are based on the stationary reference frame to better mitigate the voltage distortion under nonlinear loads. Droop control and selective virtual impedance loop achieve accurate current-sharing when supplying both linear and non-linear loads. Moreover, by adjusting voltage references according to the amplitude of the negative sequence voltage, the unbalance factor, which is mainly caused by single phase generators/loads, can be mitigated to an extremely low value. Finally, an AC microgrid which includes three three-phase three-leg inverters was tested in order to validate the proposed control strategy.**

Keywords—Microgrids, voltage unbalance compensation, virtual impedance, droop control.

I. INTRODUCTION

In recent years, dispersed energy resources (DERs), such as wind turbines, photovoltaic systems and micro-turbines, have gain a great increasing interest since they are economic and environment friendly. In general, power electronic converters are used as interfaces between DERs and the grid [1], such that electrical power with good quality and high reliability can be delivered to the load or utility grid, as shown in Fig. 1. This paper focuses on islanded microgrids where the interfacing converters mainly operate as voltage sources to participate on the voltage and frequency regulation while sharing at the same time active and reactive power accurately by adjusting output voltage phase angles and amplitudes. However, it is also preferred that those converters could provide power quality management ability, in such a way that we can take full use of the converters available capacity. It is well known that power quality issues, especially voltage/current unbalances and voltage/current distortions have become more and more serious in modern power system. For instance, in islanded microgrids, the voltage unbalance problem is a salient issue mainly produced by the use of single-phase generators/loads and it can lead to instability and power quality issues.

In order to enhance the voltage waveform quality, several components to deal with the voltage unbalance compensation

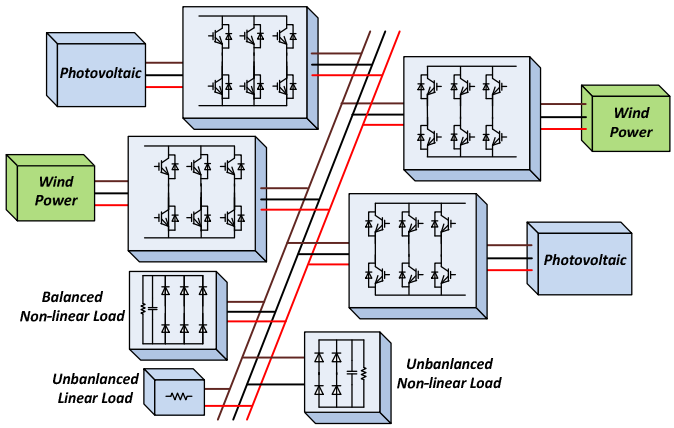


Fig. 1. General architecture of a microgrid.

have been developed, such as static var compensator (STATCOM) [2], series active power filter [3] and shunt active power filter [4]. However, all these compensation methods utilize additional power converters to inject negative sequence reactive power. Only a few works compensate the unbalanced voltage by utilizing the DG interfacing converters. In [5], the DG inverter is controlled to inject negative sequence current to balance the common bus voltage. However, a surplus converter capacity is needed to generate the negative sequence current and the injecting current might be too high under severe unbalance conditions. In the previous work [6], an unbalance compensation method is proposed by sending proper control signals to DGs local controllers. However, the negative sequence component of the common bus voltage is hard to suppress, since the microgrid central controller (MGCC) uses the voltage unbalance factor as a main control variable, which value is reduced by the positive sequence voltage.

In order to overcome these drawbacks, this paper proposes a control scheme located in the MGCC which directly acts over the negative sequence voltage. Section II initially elaborates on the control design of local controllers, mainly including inner voltage/current loops, virtual impedance loop and droop controller, and then the system modeling is introduced. Section III will investigate the strategy of the proposed direct voltage unbalance compensator. Experimental results of a three paralleled inverters system is analyzed and discussed in Section IV. Finally, conclusions are presented in Section V.

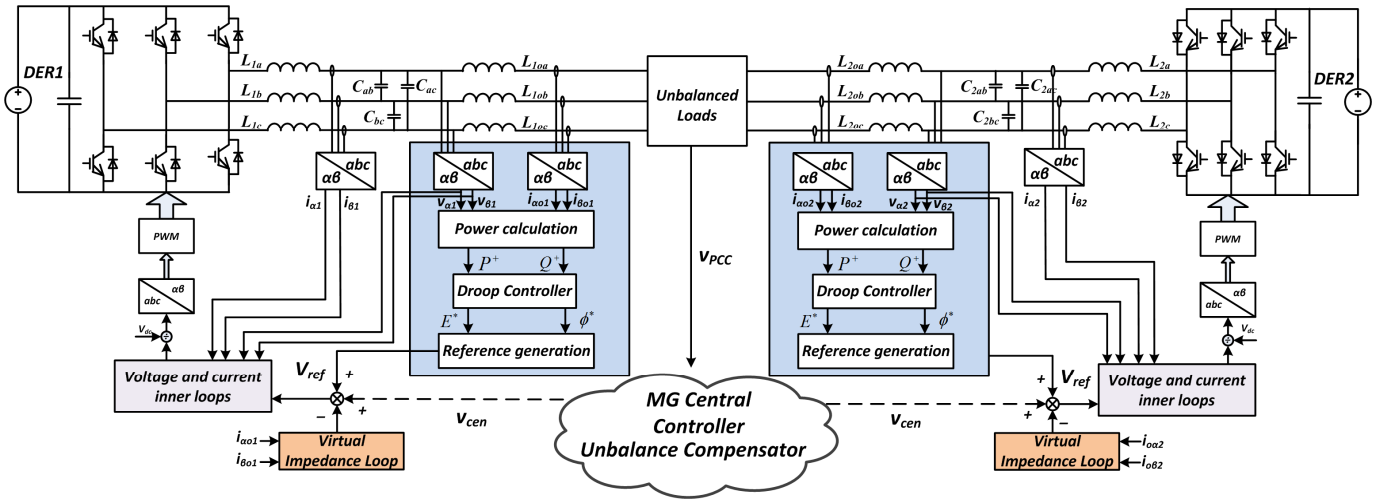


Fig. 2. Implementation of the local controllers.

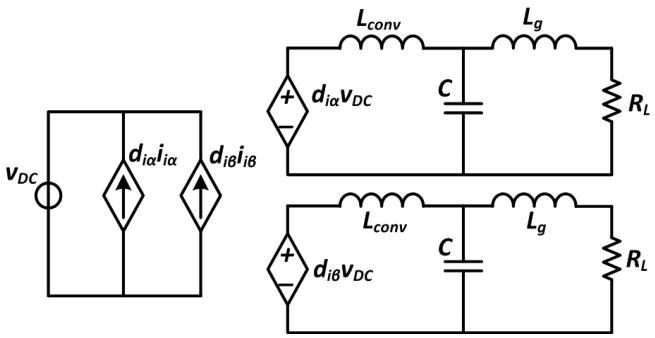


Fig. 3. Small signal model of single inverter.

II. Local Controller Design

Fig. 2 depicts the control strategy of inverter local controllers. LCL filter is adopted here, but it actually operates as a conventional LC filter with a coupling inductor. The main function of the grid side inductor is to optimize the dynamic performance and to shape the output impedance. Also its current is measured for power calculation and virtual impedance which will be explained later.

A. Inner Loop Design

It can be seen from Fig. 2 that the inner loops are implemented in two-phase stationary frame and all the measured voltage and current are transformed from *abc* to *αβ* coordinates, thus the computational burden is reduced significantly. Both voltage and current controllers are based on proportional+resonant (*PR*) controller instead of the conventional proportional+integrator (*PI*) controller. The reason is that *PR* controller can provide infinite gain at the selected resonant frequency to provide satisfactory tracking performance. In other words, the performance of *PR* controller at selected resonant frequency is conceptually similar to the performance of *PI* controller at 0Hz [7-9]. Also, in order to mitigate the voltage and current distortion under nonlinear loads, the *PR* controllers are tuned at fundamental frequency, 3rd, 5th, 7th, 9th and 11th order harmonics.

Modeling of the main power circuit and the inner loop controller in synchronous reference frame is established here to obtain the close loop transfer function. By using *abc/αβ* transformation in the power plant and neglecting the zero quadrature components, the three phase inverter can be expressed as a decoupled two phase system. Fig.3 shows the small signal model of the decoupled two phase system. It is worthy noting that only one inverter is depicted here to simplify the figure.

According to the small signal model, the control scheme can be depicted in Fig. 4. The close loop transfer function is derived in (1):

$$v_c(s) = v_o^*(s) - Z_o(s)i_o(s) = \frac{G_v(s)G_i(s)G_{PWM}(s)}{LCs^2 + CG_i(s)G_{PWM}(s)s + G_v(s)G_i(s)G_{PWM}(s) + 1} v_{ref}(s) - \frac{Ls + G_i(s)G_{PWM}(s)}{LCs^2 + CG_i(s)G_{PWM}(s)s + G_v(s)G_i(s)G_{PWM}(s) + 1} i_o(s) \quad (1)$$

where $v_c(s)$ is the capacitor voltage, $v_o^*(s)$ is the open circuit voltage, $i_o(s)$ is the output current, $Z_o(s)$ is the equivalent output impedance, $v_{ref}(s)$ is the voltage reference, L is the converter side inductor, C is the filter capacitor. $G_v(s)$, $G_i(s)$ and $G_{PWM}(s)$ are the transfer function of voltage controller, current controller and *PWM* delay, respectively. Their transfer function can be expressed as:

$$G(s) = k_{vp} + \sum_{h=1,3,5,7,9,11} k_{hvr} \frac{s}{s^2 + (h\omega)^2} \quad (2)$$

$$G(s) = k_{ip} + \sum_{h=1,3,5,7,9,11} k_{hir} \frac{s}{s^2 + (h\omega)^2} \quad (3)$$

$$G_{PWM}(s) = \frac{1}{1 + 1.5T_s s} \quad (4)$$

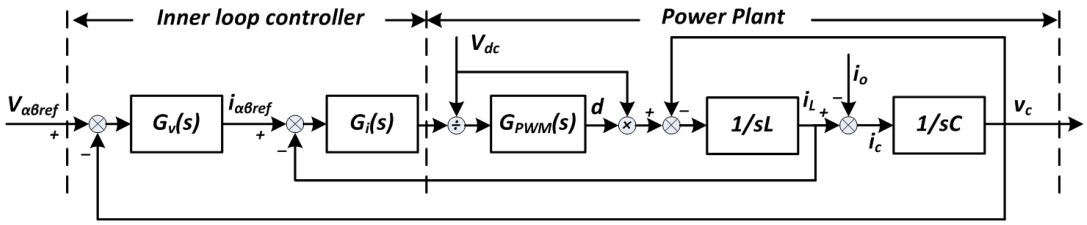


Fig. 4. Equivalent control block diagram of the inverter.

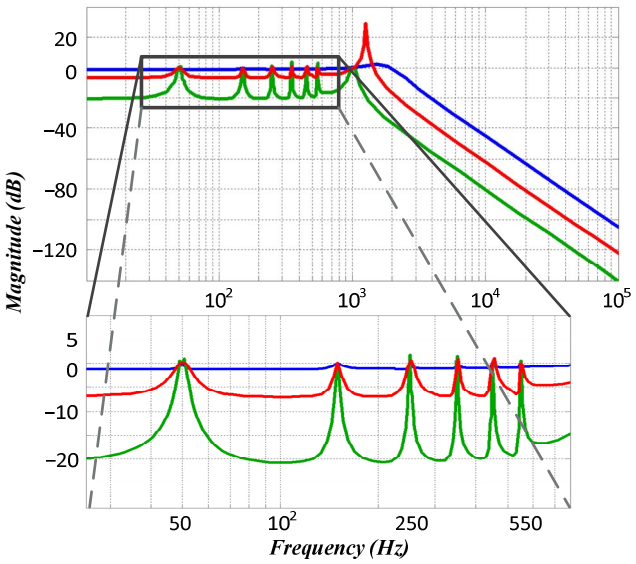


Fig. 5. Bode plot of the close loop transfer function.

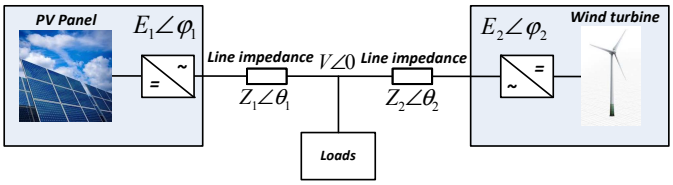


Fig. 6. Equivalent circuit of two parallel DGs.

where k_{vp} and k_{hvr} are the proportional coefficients and resonant coefficients (1st, 3rd, 5th, 7th, 9th and 11th) of voltage controller respectively. k_{ip} and k_{hir} are the proportional coefficients and resonant coefficients (1st, 3rd, 5th, 7th, 9th and 11th) of current controller respectively; ω is the fundamental angular frequency while T_s is the sampling time.

Fig. 5 depicts the Bode plot of the inverter closed-loop transfer function by using different set of parameters. As it can be seen, the gain of the close loop transfer function at fundamental frequency and 3rd, 5th, 7th, 9th, 11th order harmonics is unity while the gains at other frequencies hold at a relatively lower value. Thus, the output voltage can track the reference precisely.

B. Droop Control Implementation

In order to avoid circulating currents among the parallel inverters without using communication link between them, droop control is adopted in this paper. To better illustrates droop control theory, assuming two inverters connected in parallel and sharing loads at the common node. The equivalent circuit is shown in Fig. 6.

From Fig. 6, the active power P and reactive power Q injected by each DG can be express in (5) and (6), respectively.

$$P_i = \left(\frac{E_i V}{Z_i} cos\varphi_i - \frac{V^2}{Z_i}\right) cos\theta + \frac{E_i V}{Z_i} sin\varphi_i sin\theta \tag{5}$$

$$Q_i = \left(\frac{E_i V}{Z_i} cos\varphi_i - \frac{V^2}{Z_i}\right) sin\theta - \frac{E_i V}{Z_i} sin\varphi_i cos\theta \tag{6}$$

where E_i and φ_i are the amplitude and the phase angle of the output voltage of the each inverter, Z_i and θ_i are the amplitude and phase angle of the line impedance of each inverter, respectively. V is the voltage amplitude of common AC bus. Note that phase angle of common AC bus voltage is taken as the phase reference.

In general, the line impedance is mainly inductive, i.e. $Z_i\angle\theta_i \approx X_i\angle 90^\circ$. Furthermore, assuming the phase difference φ_i between inverter voltage and AC bus voltage is small enough, so that $sin\varphi_i$ can be approximately equal to φ_i and $cos\varphi_i$ can be approximately equal to 1. Then, from (5) and (6), the following approximations can be obtained:

$$P_i \approx \frac{E_i V}{X_i} \varphi_i \tag{7}$$

$$Q_i \approx \frac{E_i V}{X_i} sin\theta - \frac{V^2}{X_i} \tag{8}$$

From (7) and (8), it can be seen that active power P_i is dominant by phase angle φ_i while reactive power is mainly depend on inverter voltage E_i. Then, an artificial droop is introduced here to adjust the frequency and amplitude of the output voltage dynamically:

$$\varphi^* = \varphi_0 - \left(m_p + \frac{m_I}{s}\right)\left(P^+ - P^+_{ref}\right) \tag{9}$$

$$E^* = E_0 - n_p\left(Q^+ - Q^+_{ref}\right) \tag{10}$$

where φ^* and E^* are the amplitude and phase angle of the output voltage reference while E_0 and φ_0 are the amplitude and phase angle of the output voltage at no load condition, P^+ and Q^+ are the instantaneous fundamental positive sequence active and reactive power, respectively, and P^+_{ref} are Q^+_{ref} are the reference of fundamental positive sequence active and reactive power, respectively; m_p and m_I are the proportional and integral coefficients of active power controller, respectively. m_I mainly influence the dynamic characteristic of the system since it adds inertia to the system; n_p is the integral coefficients of reactive power controller.

It can be seen from (7)-(10) that the higher the droop coefficients is, the better power sharing can be achieved. However, the voltage and frequency deviation will also become larger when the droop coefficients become bigger. This tradeoff can be compensated by introducing secondary controller, as illustrated in [10]. Hence, both the proportional coefficients should be carefully selected according to (11) and (12):

$$m_p = \frac{\Delta f}{P} \tag{11}$$

$$n_p = \frac{\Delta E}{Q} \tag{12}$$

where Δf and ΔE are the maximum allowable deviation of frequency and amplitude from its nominal value, respectively. P and Q are the rated active and reactive power, respectively.

A positive-negative-sequence harmonic voltage/current component extractor [11-12] based on a second-order generalized integrator (*SOGI*) is implemented to assist the droop controller and the virtual impedance loop, which will be introduced in Section C. Since the fundamental positive sequence component extraction is almost the same with that of the fundamental negative sequence and harmonics, only the fundamental positive sequence voltage extractor is shown here in Fig. 7.

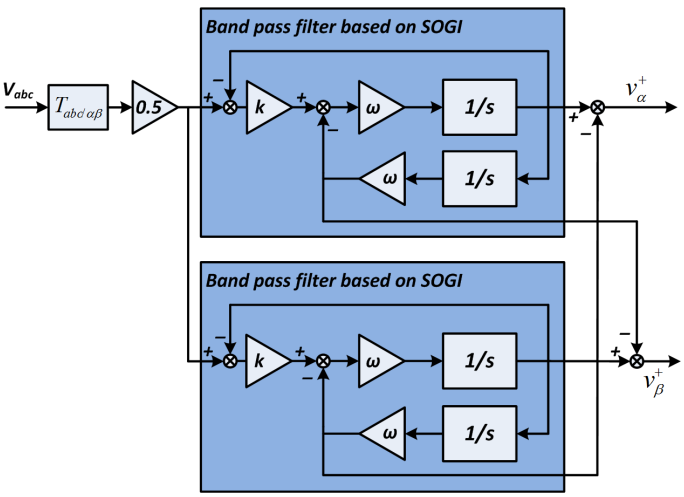


Fig. 7. Fundamental positive sequence component extractor.

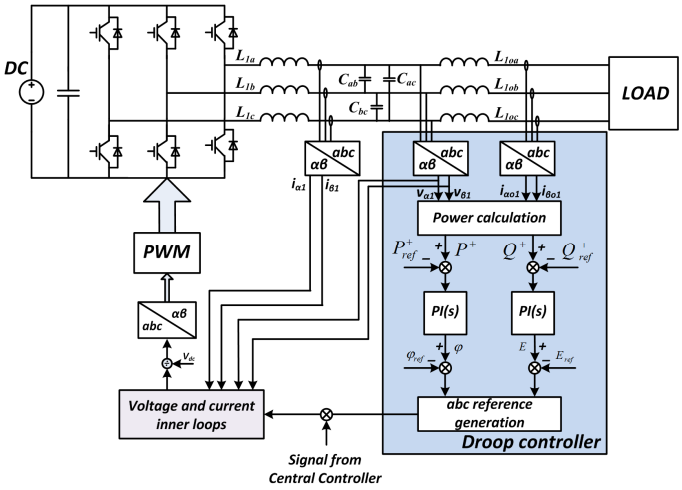


Fig. 8. Implementation of the droop controller.

Fig. 8 depicts the implementation block diagram of the droop controller. The power calculation block, based on the instantaneous reactive power theory [13], is followed by a low pass filter with a 2 Hz cut-off frequency, so that the power oscillation can be filtered out.

C. Virtual Impedance Loop

In order to share the power precisely between the distributed inverters, the output impedance of the inverter must be re-designed to mitigate the influence of control parameters and line impedance on the power sharing accuracy. Here, (1) can be rewritten as:

$$v_c(s) = G(s)v_{ref}(s) - Z_o(s)i_o(s) \tag{13}$$

where $G(s)$ represents the close loop transfer function of the inverter, and $Z_o(s)$ represents the close loop output impedance of the inverter. From the above equation, a two-terminal *Thevenin* equivalent circuit of the close loop inverter can be obtained, as shown in Fig. 9.

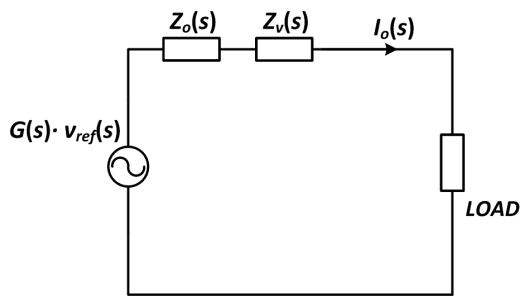


Fig. 9. Thevenin equivalent circuit of the close loop inverter.

If no control loop is implemented to compensate the output impedance, the amplitude of the output impedance at fundamental frequency and 3rd, 5th, 7th, 9th and 11th order harmonics is extremely small, as shown the blue curve in Fig. 10. Thus, a virtual impedance loop must be added in the control block to fix the output impedance.

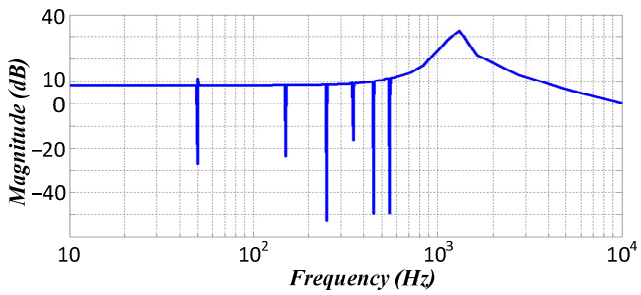


Fig. 10. Bode plot of the output impedance.

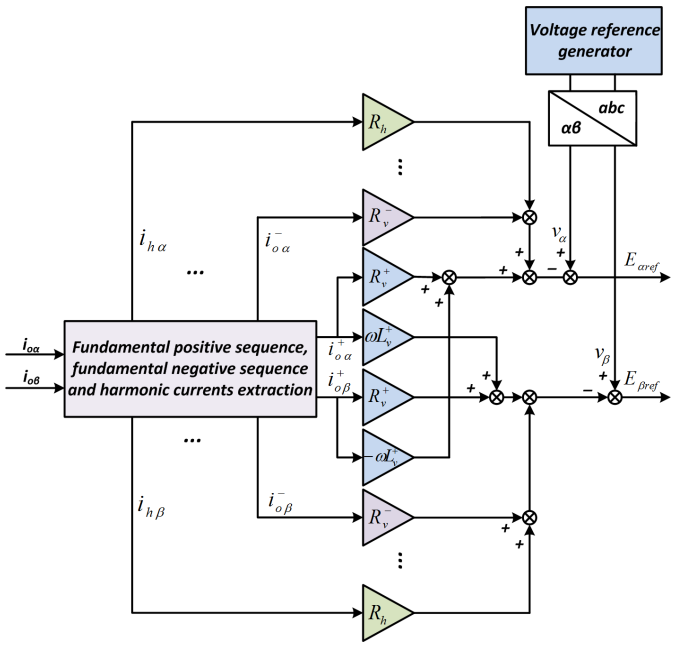


Fig. 11. Implementation of the virtual impedance.

Since the droop law in this paper is guaranteed only when the output impedance is highly inductive. Thus, a positive-sequence virtual inductor L_v^+ is added to make the output impedance more inductive, so a better decoupling of P and Q can be ensured. The purpose of adding the positive-sequence virtual resistor R_v^+ is to make the system more damped, so that the output current can be limited within an acceptable range. For fundamental negative sequence and each order of the harmonics, a resistor is emulated at the output side to enhance the sharing of nonlinear load sharing among the DGs. Compared with using a real resistor, the virtual resistor has the advantage of no power losses and the possibility to select harmonics and sequences.

The implementation scheme of the virtual impedance loop, which consists of three main parts, is illustrated in Fig. 11. The first part is fundamental positive sequence virtual impedance loop, which only introduces virtual resistor R_v^+ and virtual inductor L_v^+ to fundamental positive sequence current. The second part is fundamental negative sequence virtual impedance loop which introduces virtual resistor R_v^- to fundamental negative sequence current. The third part is harmonic virtual impedance loop which introduces virtual resistor R_h to 3rd, 5th, 7th, 9th and 11th order harmonics, respectively. Note that ω is the nominal angular frequency of the system.

It is worth noting that there is a tradeoff between the nonlinear current sharing accuracy and inverters output voltage distortion. This voltage distortion originates from the voltage drop on the virtual impedances. Thus, the value of the virtual impedances must be selected carefully to ensure a well power sharing accuracy, and meanwhile guarantee the voltage Total Harmonic Distortion (*THD*) is limited in an acceptable range. In addition, voltage distortion caused by virtual impedance is also the reason for separating the virtual impedance of harmonic and fundamental negative sequence component with fundamental positive sequence component, so that the virtual impedance of fundamental negative sequence and harmonic components can be set to a larger value.

III. Unbalance Compensator Design

In this paper, the voltage unbalance compensation method is improved in terms of control the negative sequence voltage directly. As shown in Fig. 2, the reference of voltage controller is the superposition of the output of unbalance compensator and droop controller.

The mathematical description of the unbalance compensator implemented in synchronous reference (*dq*) frame is shown in (14):

$$v_{cen} = \left[\left(\left|v^-\right|_{ref} - \sqrt{v_d^- + v_q^-}\right)\cdot PI_1(s) - Q^-\right]\cdot PI_2(s)\cdot \frac{v_{dq}^-}{\sqrt{v_d^- + v_q^-}} \quad (14)$$

where v_{cen} is the control signal send to inverter local controller, $|v^-|_{ref}$ is the reference of negative sequence voltage, Q^- is the negative sequence reactive power at point of common coupling (*PCC*), v_d^- and v_q^- are the *dq* components of negative sequence voltage respectively, $PI_1(s)$ and $PI_2(s)$ are the negative sequence voltage controllers, respectively. It can be seen that the voltage unbalance level is mitigated by controlling the *PCC* voltage directly while the negative sequence reactive power injection is controlled indirectly.

Detailed algorithm of the unbalance compensator is depicted in Fig. 12. As it can be seen, *dq* components of the negative sequence voltage at *PCC* are first extracted by rotating V_{PCC} with negative angular frequency $-\omega$ and then followed by a *low pass filter* (*LPF*). Furthermore, the amplitude of negative sequence voltage $|v^-|$ is calculated with filtered v_d^- and v_q^- and is afterwards send to a *PI* controller to generate the reference of negative sequence reactive power Q_{ref}^-. Another *PI* controller fed with the error of Q_{ref}^- and Q^- is implemented here to enhance the dynamic behavior of the unbalance compensator. Finally, the output of the *PI* controller is multiplied by normalized v^- and transformed to $\alpha\beta$ coordinates to generate the compensation signal which is send to the voltage loop controller.

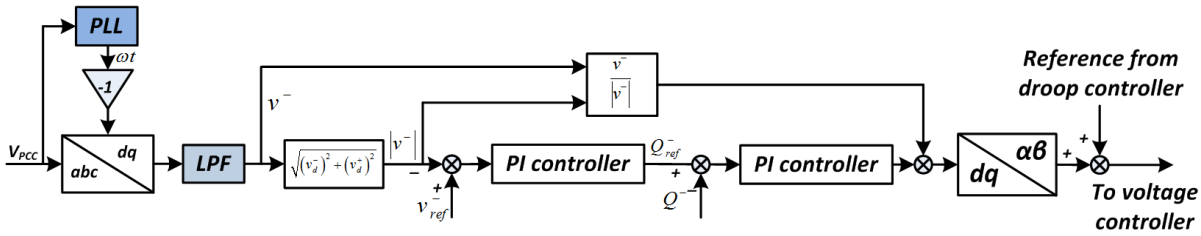


Fig. 12. Block diagram of the proposed unbalance compensator.

TABLE I. PARAMETERS OF POWER PLANTS

Parameters	*Symbol*	*Value*	*Unit*
Converter Side Inductors	L_{con}	*1.8*	*mH*
Grid Side Inductors	L_g	*1.8*	*mH*
Capacitors	C	*9*	*μF*
Nominal Voltage	V	*230*	*V*
Nominal Frequency	f	*50*	*Hz*
DC Voltage	V_{DC}	*650*	*V*
Switching Frequency	f_s	*10*	*kHz*

TABLE II. CONTROL SYSTEM PARAMETERS

Voltage/Current Inner Loop Controllers			
Parameters	*Symbol*	*Value*	
Voltage Loop Controller	k_{vp}, k_{vr}, k_{3vr} k_{5vr}, k_{7vr}, k_{9vr}, k_{11vr}	*0.05, 90, 5, 5, 15, ,10, 20*	
Current Loop Controller	k_{ip}, k_{ir}, k_{3ir},k_{5ir}, k_{7ir}, k_{5ir}, k_{11vr}	*5, 200, 20, 10, 10, 10 10*	
Primary Controller			
Parameters	*Symbol*	*Value*	*Unit*
Proportional Phase Droop	m_P	*0.0005*	*Rad·s/W*
Integral Phase Droop	m_I	*0.00006*	*Rad/W*
Proportional Phase Droop	n_P	*0.002*	*V/Var*
Virtual Resistor	R_v^+, R_v^-, R_3, R_5, R_7, R_9, R_{11}	*1, 4, 4, 5, 5, 5, 5*	Ω
Virtual Inductor	L_v	*4*	*mH*
Secondary Controller			
Parameters	*Symbol*	*Value*	
Negative Sequence Voltage Reference	v_{ref}^-	*0.5*	
Negative Sequence Voltage Controller	K_{p_vneg}, k_{i_vneg}	*5, 0.01*	
Negative Sequence Power Controller	K_{p_Qneg}, k_{i_Qneg}	*0.01, 0.5*	

IV. EXPERIMENTAL RESULTS

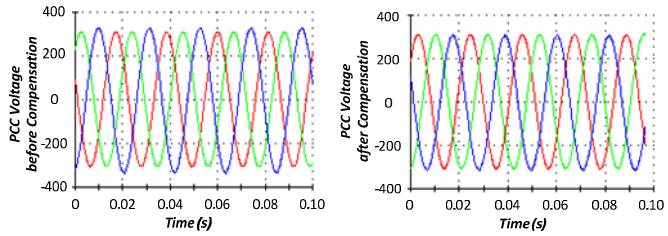
In order to validate the correctness of the proposed control strategy, experiments have been carried out on a MG platform existing in the Microgrid Lab at Aalborg University [14]. The platform consists of three *Danfoss* three-phase DG inverters which share a common AC bus. In addition, the detailed electrical configuration is shown in Fig. 2 as well. An unbalanced resistive load is connected to the common AC bus to emulate unbalanced load conditions. The detailed power stage and control system specifications can be found in Table I and Table II.

Before t=2*s*, an unbalanced linear load is connected to the common AC bus and lead to the flowing of negative sequence current. Thus, voltage unbalance appears on the *PCC* voltage, as shown in Fig. 13(a). At the meantime, the output voltage of the three DGs has a good voltage quality, as illustrated in Fig. 16.

At t=2*s*, the direct unbalance compensation loop is enabled and then the corresponding compensation signal is sent to the DGs local controller. As expected, the unbalance factor significantly reduced from 5% to 0.2% after 10 seconds (as shown in Fig. 14). In addition, it can be seen from Fig. 13(b) and Fig. 16 that the decrease of the *PCC* voltage unbalance factor is achieved by means of deteriorates the DGs output voltage. To better illustrate the effect of the unbalance compensator, the negative sequence voltage at *PCC* is shown in Fig. 15. It is obvious that the PCC negative sequence voltage drops dramatically after the compensation enabled. Note that the unbalance factor (UF) is defined as (15):

$$UF = \sqrt{\frac{(v_d^-)^2 + (v_q^-)^2}{(v_d^+)^2 + (v_q^+)^2}} \cdot 100 \qquad (15)$$

where v_d^+ and v_q^+ are the positive sequence of the *PCC* voltage respectively; v_d^- and v_q^- are the negative sequence of the *PCC* voltage respectively.



(a) (b)

Fig. 13. *PCC* voltages: (a) Before compensation, (b) After compensation.

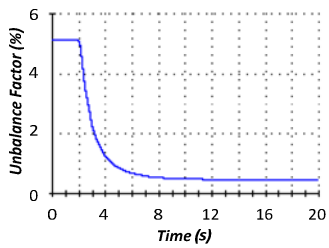


Fig. 14. *PCC* voltage unbalance factor.

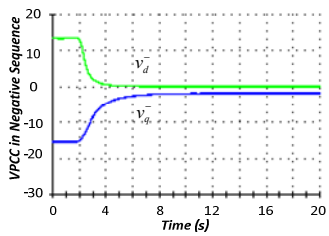


Fig. 15. Negative sequence voltage of *PCC*.

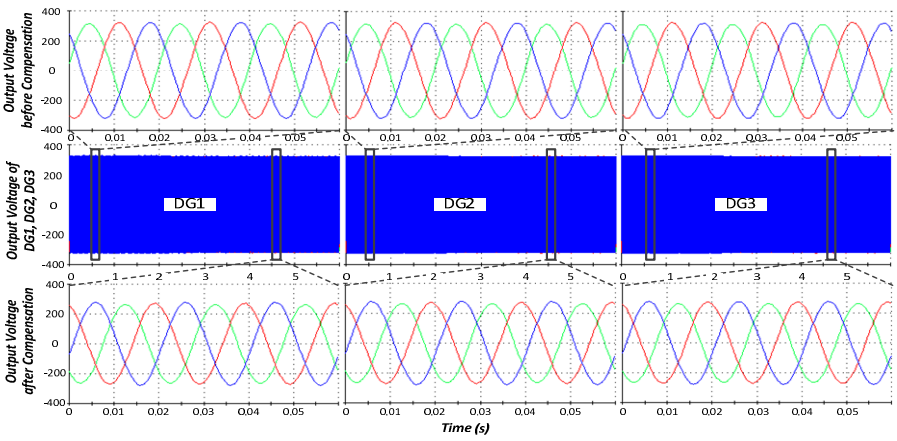


Fig. 16. Ourput voltage of DG1, DG2, and DG3.

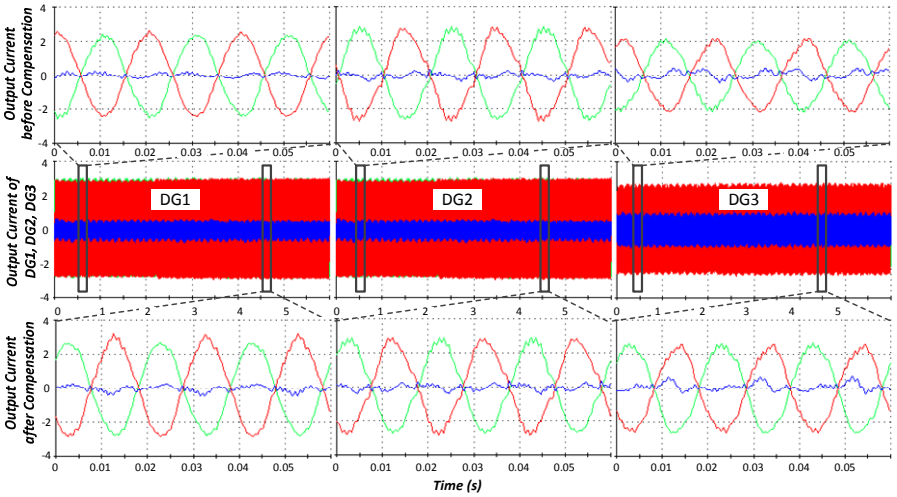


Fig. 17. Ourput current of DG1, DG2, and DG3.

Moreover, in order to investigate the current sharing accuracy, the output current of the three DGs before and after the compensation is depicted in Fig. 17. As it can be seen, the output current can be shared properly among the three DG converters. Also, it is worth noting that the current errors between the three DG converters are caused by the difference in line impedance.

V. Conclusions

In this paper, a novel direct voltage unbalance compensation control strategy for islanded microgrids has been investigated. The control structure includes two levels: a local controller and an direct voltage unbalance compensator. The local controller mainly takes care of the bus voltage regulation and the power sharing accuracy, while the direct voltage unbalance compensator contributes to mitigate the voltage unbalance at the *PCC* by controlling the voltage reference. The effectiveness of the control scheme has been validated with three *LCL* DG converters connected in parallel sharing a common AC bus. The experimental results show that the negative sequence voltage can be well suppressed to the desired value with a satisfied load sharing accuracy.

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