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Space Vector Modulation for DC-Link Current Ripple Reduction in Back-To-Back Current Source Converters for Microgrid Applications

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***Abstract*—Back-to-back converters have been typically used to interconnect the microgrids. For a back-to-back current source converter, the dc-link current ripple is one of the important parameters. A large ripple will cause the electromagnetic interference, undesirable high-frequency losses, and system instability. Conventionally, with a given switching frequency and rated voltage, the current ripple can be reduced by increasing the dc-link inductor, but it leads to bulky size, high cost and slow dynamic response. In order to solve this problem, this paper reveals that the current ripple can be significantly reduced by adjusting the gate patterns of space vector modulation (SVM) between the rectifier and inverter in a back-to-back converter. The experimental results verify the effectiveness of the proposed method.**

***Index terms*—Current source converter, dc-link current ripple, space vector modulation, back-to-back converter**

I. Introduction

Nowadays, microgrids are gaining more and more attentions [1], [2]. Typically, the back-to-back voltage source converters are used to interconnect the microgrids [3]-[6]. However, the voltage source converters require bulky and temperature-limited electrolytic capacitors. The failure in electrolytic capacitors is one of the main causes of breakdowns, and degrades the whole system's lifetime [7]. Besides, there is a potential risk of overcurrent due to the phase-leg short circuit, which reduces the system reliability. On the other hand, the current source converters have the inherent current limiting capability and thus enhance the reliability [8-11]. Furthermore, they allow forbidden states in the case of voltage source converters that may cause short-circuit, being in case of current source a desirable possibility to achieve soft-switching operation [12].

However, one of their disadvantages is the large dc-link inductor, which increases the system volume and limits the dynamic response. An alternative solution is to use the small inductor, but it suffers from a large current ripple. Therefore, the solution to reduce the current ripple in case of small dc-link inductor value needs further investigation.

The objective of this paper is to reduce the current ripple of back-to-back current source converter by optimizing the gate pattern of space vector modulation (SVM). First, the relationship between dc-link current ripple and different SVM pulse patterns is presented in Section II. It is revealed that the gate pattern arrangement has a significant effect on the dc-link current ripple. By coordinating the SVM gate patterns of both rectifier and inverter, the current ripple can be greatly reduced, thus a small dc-link inductor can be used. In Section IV, the experimental tests on a back-to-back converter are carried out to verify the proposed optimization method. Finally, the conclusions are presented in Section V.

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II. Effect of SVM Pattern on DC-Link Current Ripple

The schematic diagram of the back-to-back current source converter illustrated in Fig.1, where two microgrids (MG_1 and MG_2) are connected via the back-to-back converters. The symbol i_L represent the dc-link current. Note that the high-frequency dc-link current ripple is associated with the modulation strategy, and independent on the close-loop control. Therefore, the space vector modulation with open-loop control is discussed in this paper. The closed-loop control associated with the power management of microgrids [13] is out of the scope of this paper. The following will discuss the general effect of the space vector modulation on the DC-link current ripple.

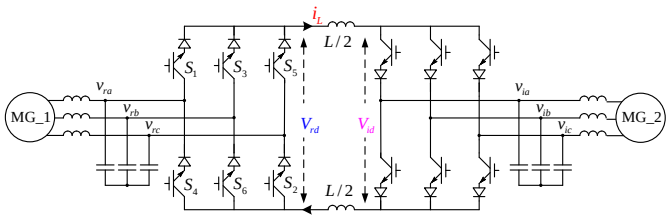


Fig.1 Schematic diagram back-to-back current source converter

First of all, a brief review of the space vector modulation of current source converter is presented. As shown in Table I, there are six active vectors (I_1~I_6) and three zero vectors (I_7~I_9). The current space vector diagram is illustrated in Fig.2, where the reference I_{ref} can be synthesized by two nearest active vectors and one zero vector [14], [15]. The dwell time for three vectors can be determined by (1), where T_s denotes the sampling period, m_a stands for the modulation index, and θ is the vector angle, $-\pi/6 < \theta < \pi/6$.

$$\begin{aligned} T_1 &= T_s \cdot m_a \cdot \sin(\pi/6 - \theta) \\ T_2 &= T_s \cdot m_a \cdot \sin(\pi/6 + \theta) \\ T_0 &= T_s - T_1 - T_2 \end{aligned} \tag{1}$$

TABLE I. Switching Function, Space Vectors and DC-Link Voltage

	S_1	S_4	S_3	S_6	S_5	S_2	V_{rd}
I_1	1	0	0	1	0	0	v_{ab}
I_2	1	0	0	0	0	1	v_{ac}
I_3	0	0	1	0	0	1	v_{bc}
I_4	0	1	1	0	0	0	$-v_{ab}$
I_5	0	1	0	0	1	0	$-v_{ac}$
I_6	0	0	0	1	1	0	$-v_{bc}$
I_7	1	1	0	0	0	0	0
I_8	0	0	1	1	0	0	
I_9	0	0	0	0	1	1	

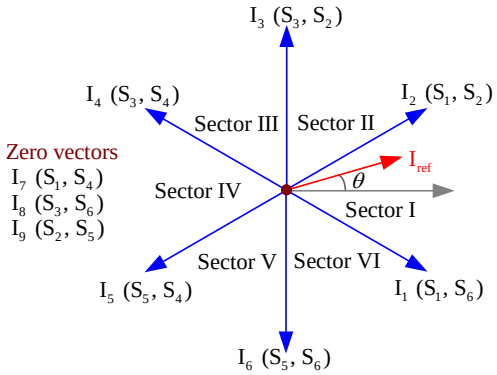


Fig. 2 Current space vector diagram

The dc-link current ripple can be derived from Fig.1 as follows.

$$\Delta i = \frac{V_{rd} - V_{id}}{L}\Delta t \tag{2}$$

where V_{rd} and V_{id} are dc-link voltage of rectifier and inverter respectively. The dc voltages can be expressed as the switching functions of rectifier and inverter in Eq. (3) and (4).

$$V_{rd} = (S_1 - S_4)v_{ra} + (S_3 - S_6)v_{rb} + (S_5 - S_2)v_{rc} \tag{3}$$

$$V_{id} = (S_1^{'} - S_4^{'})v_{ia} + (S_3^{'} - S_6^{'})v_{ib} + (S_5^{'} - S_2^{'})v_{ic} \tag{4}$$

where $S_1 \sim S_6$ are switching functions of the rectifier, and $S_1^{'} \sim S_6^{'}$ are switching functions of the inverter.

From Eq.(2), it can be observed that the inductor current ripple Δi mainly depends on the voltage difference between the rectifier voltage V_{rd} and inverter voltage V_{id}.

As for the rectifier voltage V_{rd} in Eq.(3), it is dependent on the switching functions. The relationship between the switching functions and rectifier voltage V_{rd} is listed in Table I. The inverter voltage V_{id} can also be obtained in the same way and not duplicated here for simplicity.

It is a common practice to configure the switching frequency of rectifier the same as that of inverter in a back-to-back converter. In this case, there are many possible pulse patterns of current space vectors in a switching period. Note that three-segment switching sequences are used in this paper [15]. More segments, e.g. separated I_0 with two or more segments, would be beneficial to the dc-link current ripple reduction, but bring more switching commutations and losses, which is beyond the scope of this paper. Take sector I for example, it is assumed that the rectifier pulse pattern is fixed as 1-2-0 (120), more specifically, the pulse pattern of rectifier is arranged as I_{r1}, I_{r2}, I_{r0} (120). And then, the inverter pulse patterns have six possible arrangements, as shown in Fig.3, where the dwell times for both rectifier and inverter can be expressed as follows.

$$\begin{aligned} T_{r1} &= T_s \cdot m_{ra} \cdot \sin(\pi/6 - \theta_r) \\ T_{r2} &= T_s \cdot m_{ra} \cdot \sin(\pi/6 + \theta_r) \\ T_{r0} &= T_s - T_{r1} - T_{r2} \end{aligned} \tag{5}$$

$$\begin{aligned} T_{i1} &= T_s \cdot m_{ia} \cdot \sin(\pi/6 - \theta_i) \\ T_{i2} &= T_s \cdot m_{ia} \cdot \sin(\pi/6 + \theta_i) \\ T_{i0} &= T_s - T_{i1} - T_{i2} \end{aligned} \tag{6}$$

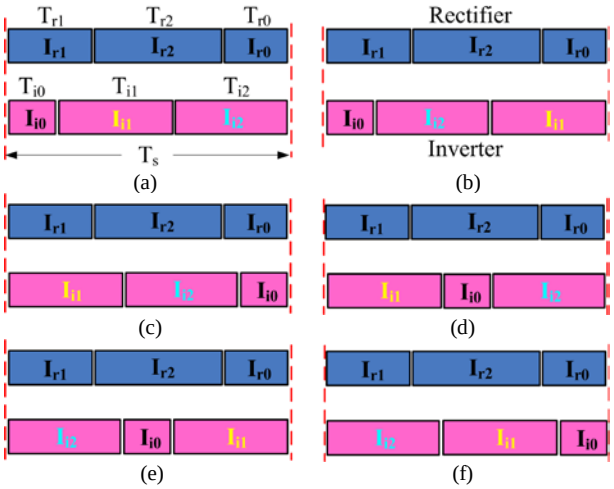


Fig.3 Possible pulse patterns in sector I of rectifier and inverter. (a) 120--012, (b) 120---021, (c) 120---120, (d) 120---102, (e) 120---201, (f) 120---210

On the other hand, if the inverter pulse pattern is fixed, and then the rectifier pulse patterns also have six possible arrangements. In summary, there are $6 \times 6 = 36$ pulse patterns for rectifier and inverter in sector I. It should be noted that there are many possible pulse patterns if we consider the pulse patterns in different six sectors of both rectifier and inverter. For simplicity, the six possible pulse patterns in Fig.3 are firstly discussed. As states above, the dc-link current ripple Δi depends on the voltage difference between the rectifier voltage and inverter voltage.

For simplicity of analysis, it is assumed that the corresponding rectifier voltages of I_{r1}, I_{r2} and I_{r0} are $V_{r1} > V_{r2} > V_{r0}$, while the corresponding inverter voltages of I_{i2}, I_{i1} and I_{i0} are $V_{i2} > V_{i1} > V_{i0}$. In this case, take Fig.3 (a) for example, the pulse pattern, voltage difference and current ripple is shown in Fig. 4.

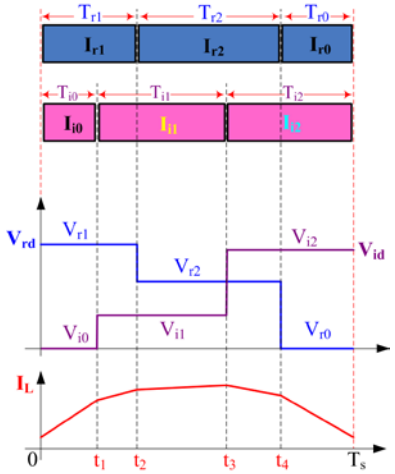


Fig. 4 Pulse pattern in sector I and corresponding dc-link current

From Fig. 4, it can be observed that there are five segments in a switching period. Therefore, the dc-link inductor current is a piecewise function.

a. During time interval $0 \sim t_1$

The inductor current increases with a positive slope due to the positive voltage difference on dc-link inductor. The inductor current is shown in (7), where i_0 is the initial current.

$$i_L = i_0 + \frac{V_{r1} - V_{i0}}{L}t \tag{7}$$

b. During time interval $t_1 \sim t_2$

$$i_L = (i_0 + \frac{V_{r1} - V_{i0}}{L} T_{i0}) + \frac{V_{r1} - V_{i1}}{L}(t - t_1) \quad (8)$$

c. During time interval $t_2 \sim t_3$

$$i_L = i_0 + \frac{V_{r1} - V_{i0}}{L} T_{i0} + \frac{V_{r1} - V_{i1}}{L}(T_{r1} - T_{i0}) + \frac{V_{r2} - V_{i1}}{L}(t - t_2) \quad (9)$$

d. During time interval $t_3 \sim t_4$

$$i_L = i_0 + \frac{V_{r1} - V_{i0}}{L} T_{i0} + \frac{V_{r1} - V_{i1}}{L}(T_{r1} - T_{i0}) + \frac{V_{r2} - V_{i1}}{L}(T_{i1} + T_{i0} - T_{r1}) - \frac{V_{i2} - V_{r2}}{L}(t - t_3) \quad (10)$$

e. During time interval $t_4 \sim T_s$

$$i_L = i_0 + \frac{V_{r1} - V_{i0}}{L} T_{i0} + \frac{V_{r1} - V_{i1}}{L}(T_{r1} - T_{i0}) + \frac{V_{r2} - V_{i1}}{L}(T_{i1} + T_{i0} - T_{r1}) - \frac{V_{i2} - V_{r2}}{L}(T_{r2} + T_{r1} - T_{i1} - T_{i0}) - \frac{V_{i2} - V_{r0}}{L}(t - t_4) \quad (11)$$

From (7) ~ (11) and Fig. 4, it can be observed that the dc-link current increases during $0 \sim t_3$ and decreases during $t_3 \sim T_s$. Therefore, the current ripple can be calculated as

$$\Delta i = \frac{V_{r1} - V_{i0}}{L} T_{i0} + \frac{V_{r1} - V_{i1}}{L}(T_{r1} - T_{i0}) + \frac{V_{r2} - V_{i1}}{L}(T_{i1} + T_{i0} - T_{r1}) \quad (12)$$

For a specified current space vector, the dwell times of T_{i0}, T_{r1} and T_{i1} are constant, which are defined by (5) and (6). Therefore, the current ripple in (12) mainly depends on the voltage difference between rectifier and inverter. It is clear that the pulse pattern arrangement in Fig. 4 leads to a large current ripple, due to high voltage difference at the start and the end of the switching period.

III. Optimized SVM Pulse Pattern

In order to reduce the dc-link current ripple, the voltage difference should be controlled as small as possible. Fig. 5 illustrates the other five pulse pattern arrangements and corresponding dc-link currents. The current vectors (I_{r1}, I_{r2}, I_{r0}, I_{i1}, I_{i2}, and I_{i0}) of both rectifier and inverter are re-classified as **Large (L)**, **Middle (M)**, **Small (S)** vectors according to the corresponding instantaneous voltage amplitude.

Take Fig. 5(a) for example, the current vectors of I_{r1}, I_{r2}, I_{r0} are re-classified as **Large (L)**, **Middle (M)**, **Small (S)** vectors due to their corresponding rectifier voltage amplitude $V_{r1} > V_{r2} > V_{r0}$. And this pulse pattern is defined as **L-M-S** type in this paper. On the other hand, the current vectors of I_{i0}, I_{i2}, I_{i1} are re-classified as **Small (S), Large (L), Middle (M)** vectors due to their corresponding inverter voltage amplitude $V_{i0} < V_{i1} < V_{i2}$. And this pulse pattern is defined as **S-L-M** type.

As mentioned above, the voltage difference should be limited as small as possible to reduce the dc-link current ripple. From five pulse patterns and corresponding voltage differences in Fig. 5. It can be observed that the best pulse pattern arrange is **(L-M-S) ---- (L-M-S)**, as shown in Fig. 5(e). In this case, the dc-link current ripple is minimum due to the minimized voltage difference, compared with other pulse pattern arrangements.

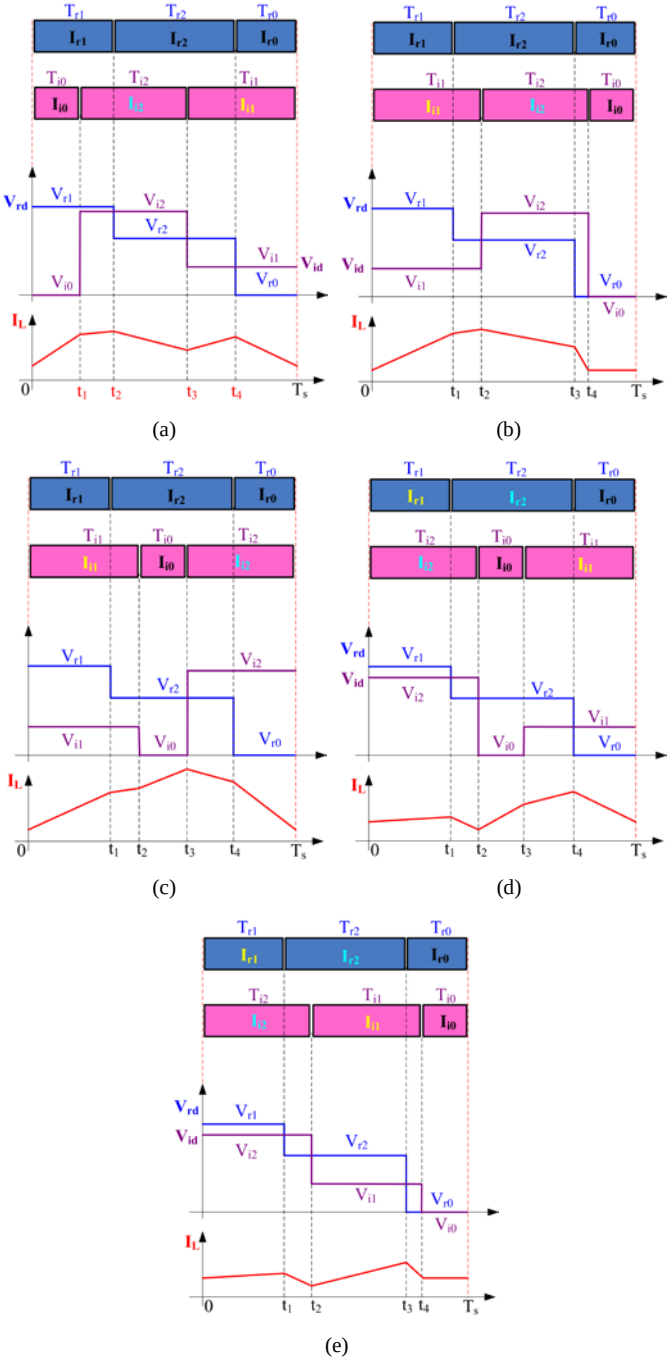
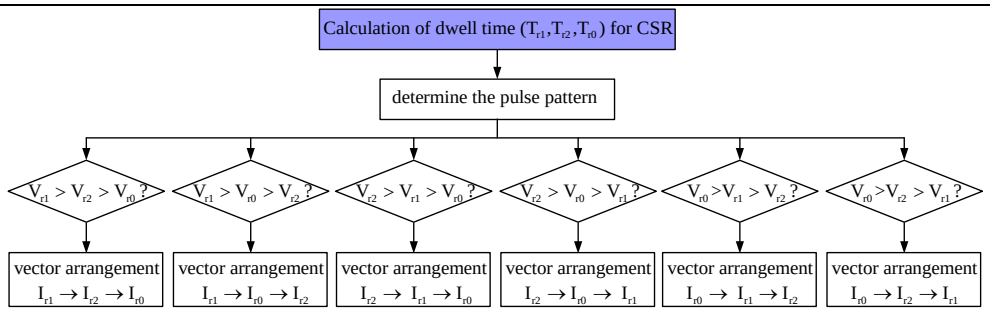
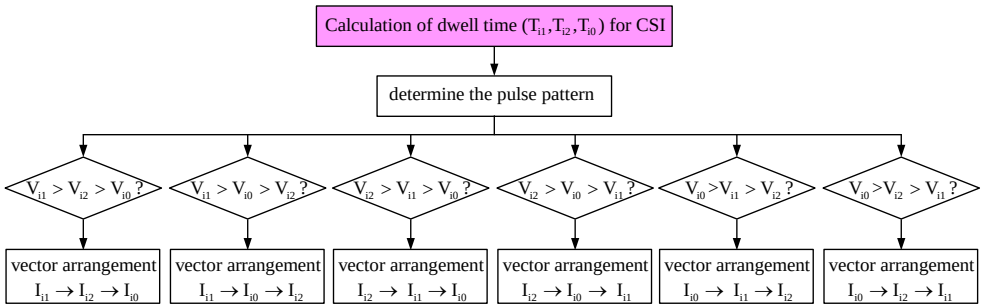


Fig.5 Five other pulse patterns in sector I and corresponding dc-link currents. (a) (L-M-S) ---- (**S-L-M**), (b) (L-M-S) ---- (**M-L-S**), (c) (L-M-S) --- (**M-S-L**), (d) (L-M-S) ---- (**L-S-M**), (e) (L-M-S) ---- (**L-M-S**)

Note that the proposed method doesn't cause any additional commutations at all. Take Fig. 5 (e) for example, the optimized pulse pattern of inverter is (**I_{i2}** [S_1,S_2], **I_{i1}** [S_1,S_6], and **I_{i0}** [S_1,S_4]), which leads to 2 commutations. It has the same commutations as that of the conventional fixed pulse pattern (**I_{i1}** [S_1,S_6], **I_{i2}** [S_1,S_2], and **I_{i0}** [S_1,S_4]). Therefore, the switching loss remains the same as that of the conventional method.



(a)



(b)

Fig.6 Optimized pulse pattern for current ripple reduction in sector I. (a) Optimized pulse pattern arrangement of rectifier, (b) Optimized pulse pattern arrangement of inverter

Fig. 6 shows the flowchart of the proposed optimized pulse pattern for current ripple reduction in sector I. For other sectors, the pulse pattern arrangements are similar. In summary, the pulse patterns of rectifier and inverter should be coordinately arranged with the same type as **(L-M-S) ---- (L-M-S)**, regardless of the same or difference sectors. In this way, the dc-link current ripple can be greatly reduced due to the low voltage difference between rectifier and inverter voltages.

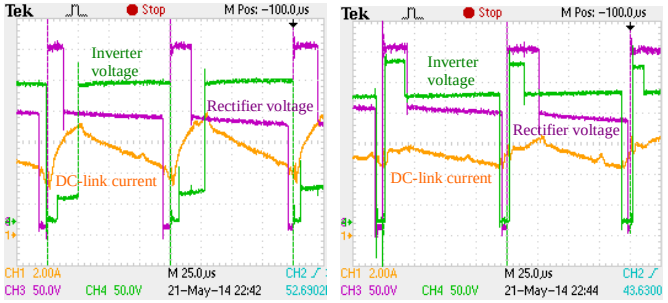
IV. Experimental Results and Discussion

In order to verify the effectiveness of the proposed method, the experimental tests are carried out on a back-to-back current source converter. The switching frequency of back-to-back converter is 10 kHz, and the rated dc-link current is 6A. The system control is implemented on a DSP (TMS320F28335) and FPGA (EP4CE10E22C8). The experimental parameters are listed in Table II.

Fig. 7(a) shows the rectifier/inverter voltage and corresponding dc-link current ripple with un-optimized pulse patterns. It can be observed that, during the time interval of a switching period (100μs), the SVM pulse pattern of rectifier is arranged as **L-M-S** type, while the **S-M-L** type is arranged for inverter. That is to say, the pulse patterns of rectifier and inverter are not coordinately configured, and consequently the dc-link current ripple is large due to high voltage difference.

Table II. System Parameters

Parameters	Experimental Parameters	
	Values	p.u
Grid voltage (L-L rms)	208 V	base value
Nominal power	10 kVA	base value
Grid frequency	60 Hz	base value
DC link inductance	2mH	0.17 p.u
CSR input capacitance	66uF	0.1 p.u
CSI output capacitance	66uF	0.1 p.u

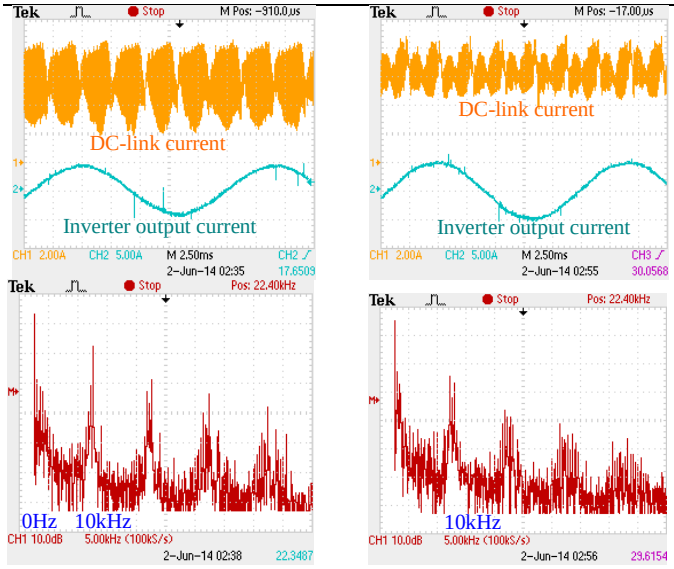


(a) (b)

Fig. 7 Rectifier/inverter voltage and corresponding dc-link current ripple. (a) Non-optimized pulse pattern, (b) Proposed optimized pulse pattern

Fig. 8 shows the experimental results of dc-link current ripple. It can be observed that the current ripple is very large with un-optimized pulse pattern. The dc-link current ripple factor, which is defined as $\Delta i_{rms} / I_{rated}$, is about 0.285. The dominant switching frequency component is about 15.2 dB, and the current ripple RMS is 1.71A.

On the other hand, the current ripple is significantly reduced with the optimized pulse pattern. The dc-link current ripple factor is 0.13. The dominant switching frequency ripple is about 8.9dB, and the current ripple RMS is 0.78A. In addition, the amplitude and THD of inverter output currents are 4.7A, 2.1% and 4.9A, 2.3%, which mean that the proposed optimized pulse pattern does not affect the waveform quality of the inverter output current.



(a) (b)

Fig. 8 Experimental results. (a) Non-optimized pulse pattern, (b) Proposed optimized pulse pattern

This paper mainly focuses on the microgrid applications, where the voltages on both sides are generally controlled within a safe range for critical loads [1]. Additionally, in contrast to the voltage source converter, the modulation index is generally controlled high to reduce the converter loss for the current source converter [11]. In this way, the proposed method is very effective because the voltage difference between rectifier and inverter sides can be minimized. For other applications, where the voltage on one ac side is much lower than the other side (e.g. for the motor drive system, the motor operates at low speed), are out of scope of this paper.

V. Conclusion

Back-to-back current source converters are attractive for the microgrid applications. One of the most important issues is how to reduce the dc-link current ripple. This paper has presented the effect of different SVM pulse patterns on the dc-link current ripple of the back-to-back current source converter. Our findings indicate that the large current ripple will arise if the SVM pulse pattern is not well designed. On the other hand, the dc-link current ripple can be significantly reduced with the proposed optimized SVM gating pattern. Finally, the proposed method has been verified by experimental results on a back-to-back current source converter.

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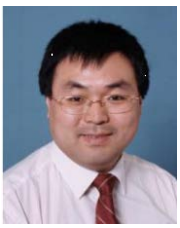

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His research interests is oriented to different microgrid aspects, including

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