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Published in:
Proceedings of the 3rd International Symposium on Environment-Friendly Energies and Applications (EFEA 2014)

DOI (link to publication from Publisher):
10.1109/EFEA.2014.7059947

Publication date:
2014

Document Version
Early version, also known as pre-print

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Abstract—**Stub Series Terminated Logic (SSTL) is an Input/output standard. It is used to match the impedance of line, port and device of our design under consideration. Therefore, selection of energy efficient SSTL I/O standard among available different class of SSTL logic family in FPGA, plays a vital role to achieve energy efficiency in design under test (DUT). Here, DUT is ROM. ROM is an integral part of processor. Therefore, energy efficient design of RAM is a building block of energy efficient processor. We are using Verilog hardware description language, Virtex-6 FPGA, and Xilinx ISE simulator. We are operating ROM with the highest operating frequency of 4th generation i7 processor to test the compatibility of this design with the latest hardware in use. When there is no demand of peak performance, then we can save 74.5% clock power, 75% signal power, and 30.83% I/O power by operating our device with 1GHz frequency in place of 4GHz. There is no change in clock power and signal power but SSTL2_II_DCI having 80.24%, 83.38%, 62.92%, and 76.52% and 83.03% more I/O power consumption with respect to SSTL2_I, SST18_I, SSTL2_I_DCI, SSTL2_II, and SSTL15 respectively at 3.3GHz.**

Keywords—I/O standard; Thermal Analysis; SSTL; Power Optimized Design; I/Os Power,

I. INTRODUCTION

ROM is read only memory. We cannot write in this in memory. But, it is an integral part of processor. In order to design energy efficient processor, it is necessary to design energy efficient ROM. Although ROM has potential to use in the software defined radio [9]. But, there is no research in energy efficient ROM design.

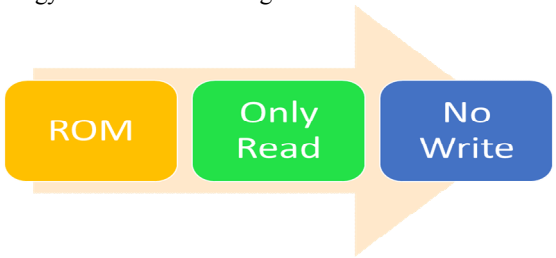

Figure 1: Read Only MEMORY

In order to make energy efficient ROM, we are using SSTL IO Standard. Here, we are going to use six different SSTL IO Standards. These are: SSTL2_I, SST18_I, SSTL2_I_DCI, SSTL2_II, SSTL15 and SSTL2_II_DCI. For each IO standard, we are going to run our ROM design with 1.0GHz, 2.9GHz, 3.3GHz, 3.6GHz, 3.8GHz and 4.0GHz device operating frequency. The primary purpose of using SSTL I/O standard is to avoid transmission line reflection by matching the impedance of transmission line, device, input port and output port. The selection of SSTL IO standard play a significant role in overall power dissipation of our design. There are multiple variety of SSTL I/O standards available in FPGA. In this work, we are the finding the most energy efficient IO standard for our ROM design. Along with that, we are testing the compatibility of this ROM design with latest i7 Processor, we are operating this ROM with same frequency supported by i7 processor as shown in Table.1. The five different series of i7 processor are 4610Y, 4600U, 4600M, 4960HQ and 4790K. In first run, we are operating our design ROM with 2.9GHz (frequency of 4610Y), 3.3GHz (frequency of 4600U), 3.6GHz (frequency of 4960HQ) and 4.0 GHz (frequency of 4790K) as shown in Table 1

Table 1: The Latest Generation i7 Processor

i7 Processor	Cores	Frequency
4610Y	4	2.9Ghz
4600U	2	3.3GHz
4600M	2	3.6GHz
4960HQ	2	3.8GHz
4790K	4	4.0GHz

SSTL is already in use in energy efficient design of parallel integrator [2], fire sensor [3], image ALU [4], VCM [5], Clock gated RAM [6], HSTL based RAM [7]. In this work, we are extending our work from RAM to ROM and HSTL to SSTL. Power dissipation in ROM has two components. One is static and other is dynamic power. Dynamic power is a sum total of clock power, signal and Input/output power. Total power is a sum total of dynamic and leakage power [8]. In section 2, power analysis is done for uniform frequency but with variation in IO standard. It doesn't affect the clock power, and

signal power. But, it shows significant effect on I/O power. In section 3, power analysis is done for variation in frequency with constant I/O standard shows variation in clock power, signal power, I/O power and Total power as well. In section 4, we conclude our project with research finding. In section 5, we are going to discuss, the future scope of our design and its real time implementation.

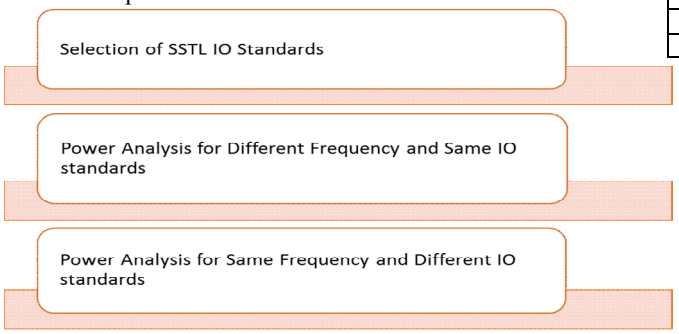

Figure 2: Work Flow in Energy Efficient ROM Design

II. Power Analysis with SSTL IO Standard

Here, we are going to use six different SSTL IO Standards. These are: SSTL2_I, SST18_I, SSTL2_I_DCI, SSTL2_II, SSTL15 and SSTL2_II_DCI. For each IO standard, we are going to run our ROM design with 1.0GHz, 2.9GHz, 3.3GHz, 3.6GHz, 3.8GHz and 4.0GHz device operating frequency as shown in Table 2-7.

A. Power Dissipation With SSTL2-I I/O Standard

Table 2: Power Dissipation with SSTL2_I

Power→ Frequency↓	Clock	Signal	IO	Total
1.0GHz	0.013	0.001	0.471	1.208
2.9GHz	0.037	0.003	0.581	1.348
3.3GHz	0.042	0.004	0.616	1.389
3.6GHz	0.046	0.004	0.0645	1.423
3.8GHz	0.048	0.004	0.664	1.446
4.0GHz	0.051	0.004	0.681	1.466

When there is no demand of peak performance, then we can save 74.5% clock power, 75% signal power, and 30.83% I/O power by operating our device with 1GHz frequency in place of 4GHz as shown in Table 2 and Figure 3.

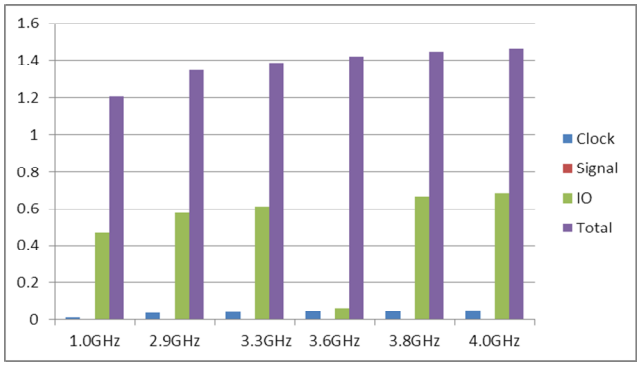

Figure 3: Power Dissipation versus Frequency on SSTL2-I

B. Power Dissipation With SSTL18-I I/O Standard

Table 3: Power Dissipation with SSTL18-I

Power→ Frequency↓	Clock	Signal	IO	Total
1.0GHz	0.013	0.001	0.413	1.148
2.9GHz	0.037	0.003	0.493	1.257
3.3GHz	0.042	0.004	0.518	1.288
3.6GHz	0.046	0.004	0.539	1.314
3.8GHz	0.048	0.004	0.553	1.331
4.0GHz	0.051	0.004	0.565	1.346

When we change the frequency from 4GHz to 2.9GHz, then there is Change in 27.45% clock power, 25% signal power, 12.74% I/O power as shown in Table 3 and Figure 4.

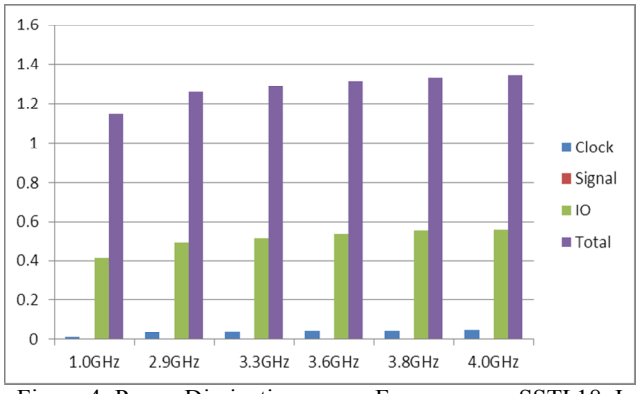

Figure 4: Power Dissipation versus Frequency on SSTL18_I

C. Power Dissipation With SSTL-I-DCI I/O Standard

Table 4: Power Dissipation with SSTL-I-DCI

Power→ Frequency↓	Clock	Signal	IO	Total
1.0GHz	0.013	0.002	1.035	1.786
2.9GHz	0.037	0.005	1.127	1.908
3.3GHz	0.046	0.007	1.179	1.973
3.6GHz	0.048	0.007	1.195	1.993
3.8GHz	0.042	0.006	1.156	1.945
4.0GHz	0.051	0.007	1.209	2.010

When we change the frequency from 4GHz to 3.3GHz , then there is Change in 9.80% clock power,100 % signal power, 2.4% I/o power as shown in Table 4 and Figure 5.

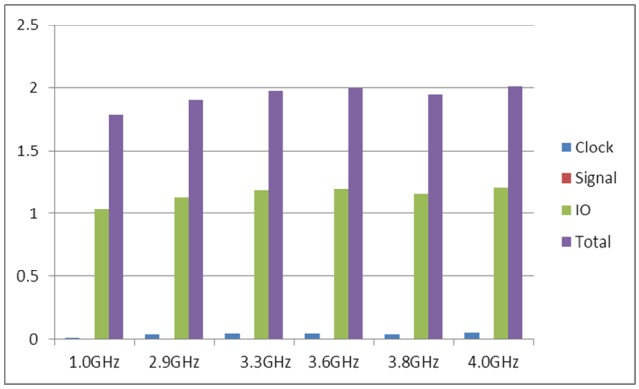

Figure 5: Power Dissipation versus Frequency on SSTL_I_DCI

D. *Power Dissipation with SSTL2_II I/O Standard*

Table 5: Power Dissipation with SSTL2_II

Power→ Frequency↓	Clock	Signal	IO	Total
1GHz	0.013	0.001	0.551	1.290
2.9GHz	0.037	0.003	0.736	1.506
3.3GHz	0.042	0.004	0.795	1.573
3.6GHz	0.046	0.004	0.845	1.628
3.8GHz	0.048	0.004	0.878	1.665
4GHZ	0.051	0.004	0.907	1.698

When we change the frequency from 4GHz to 3.6GHz , then there is Change in 9.8% clock power, 100% signal power, 6,8% I/O power as shown in Table 5 and Figure 6.

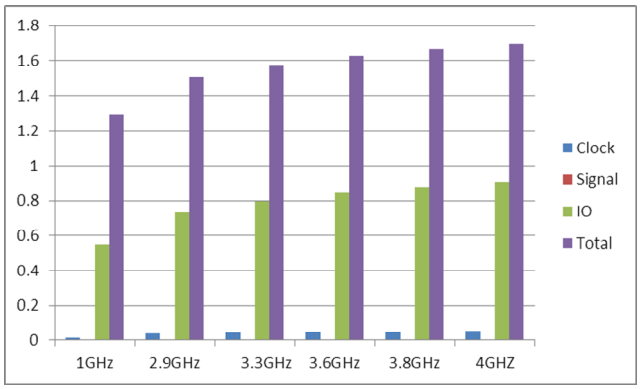

Figure 6: Power Dissipation versus Frequency with SSTL2_II

E. *Power Dissipation with SSTL15 I/O Standard*

Table 6: Power Dissipation with SSTL15

Power→ Frequency↓	Clock	Signal	IO	Total
1GHz	0.013	0.001	0.393	1.127
2.9GHz	0.037	0.003	0.497	1.260
3.3GHz	0.042	0.004	0.529	1.299
3.6GHz	0.046	0.004	0.556	1.331
3.8GHz	0.048	0.004	0.574	1.352
4GHZ	0.051	0.004	0.590	1.372

When we change the frequency from 4GHz to 3.8GHz , then there is Change in 5.8% clock power, 100% signal power, 2.71% I/O power as shown in Table 6 and Figure 7.

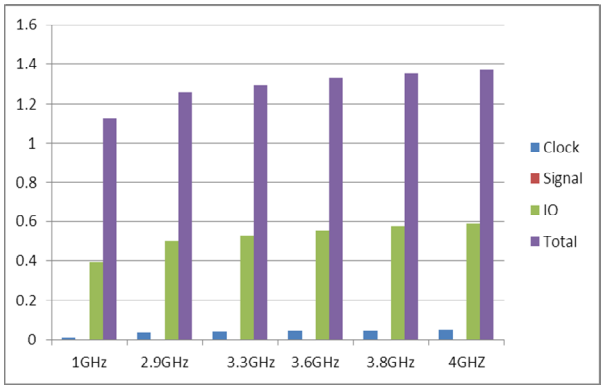

Figure 7: Power Dissipation Versus Frequency using SSTL15

F. *Power Dissipation with SSTL2_II_DCI I/O Standard*

Table 7: Power Dissipation with SSTL2_II_DCI

Power→ Frequency↓	Clock	Signal	IO	Total
1GHz	0.013	0.002	3.014	3.816
2.9GHz	0.037	0.005	3.093	3.926
3.3GHz	0.042	0.006	3.118	3.957
3.6GHz	0.046	0.007	3.138	3.982
3.8GHz	0.048	0.007	3.152	3.999
4GHZ	0.051	0.007	3.164	4.014

When we change the frequency from 4GHz to 1GHz , then there is Change in 74.5% clock power, 71.4 % signal power, 4.74% I/O power as shown in Table 7 and Figure 8.

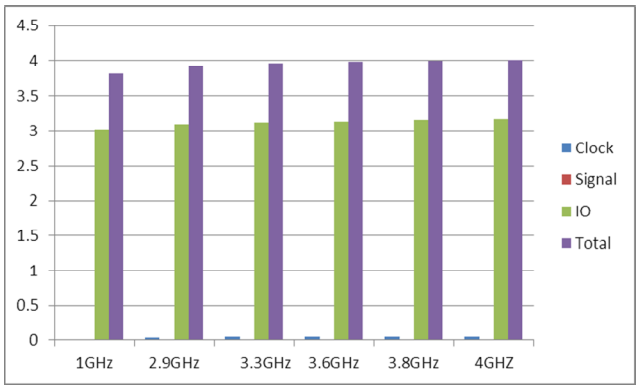

Figure 8: Power Dissipation versus Frequency with SSTLII_DCI.

III. POWERANALYSIS OF ROM FOR DIFFERENT SSTL

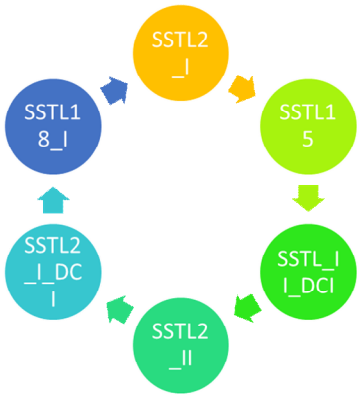

Figure 9: Different Types of SSTL I/O Standard

A. *When Device Operating Frequency is 1 GHz*

Table 8: Power Dissipation with Different SSTL

Power→ SSTL↓	Clock	Signal	IO	Total
SSTL2_I	.013	.001	0.471	1.208
SST18_I	.013	.001	0.413	1.148
SSTL2_I_DCI	.013	.002	1.035	1.786
SSTL2_II	.013	.001	.551	1.290
SSTL15	.013	.001	.393	1.127
SSTL2_II_DCI	.013	.002	3.014	3.816

There is no change in clock power and signal power but SSTL2_II_DCI having 84.43%,86.29%,65.66%,81.71%,86.96% more I/O power consumption with respect to SSTL2_I , SST18_I , SSTL2_I_DCI, SSTL2_II, SSTL15 respectively at 1GHz as shown in Table 8 and Figure 10.

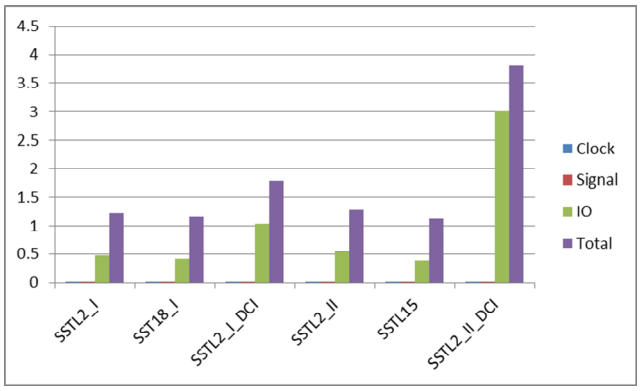

Figure 10: Power Dissipation with Different Class of SSTL

B. When Device Operating Frequency is 2.9 GHz

Table 9: Power Dissipation with Different SSTL

Power→ SSTL↓	Clock	Signal	IO	Total
SSTL2_I	0.037	0.003	0.581	1.348
SST18_I	0.037	0.003	0.493	1.257
SSTL2_I_DCI	0.037	0.005	1.127	1.909
SSTL2_II	0.037	0.003	0.736	1.506
SSTL15	0.037	0.003	0.497	1.260
SSTL2_II_DCI	0.037	0.005	3.093	3.926

There is no change in clock power and signal power but SSTL2_II_DCI having 81.21%, 84.06%, 63.56%, and 76.20% and 83.93% more I/O power consumption with respect to SSTL2_I, SSTL18_I, SSTL2_I_DCI, SSTL2_II, SSTL15 respectively at 2.9GHz as shown in Table 9 and Figure 11.

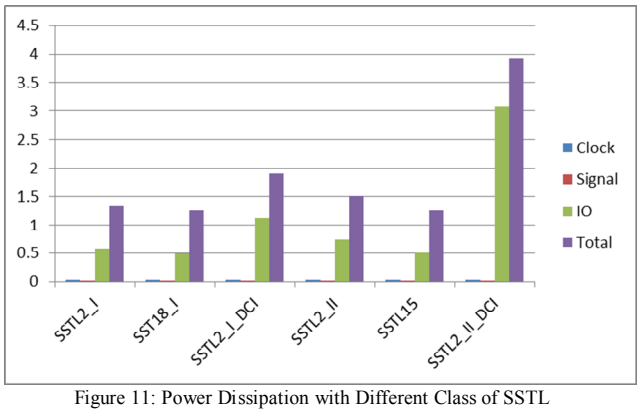

Figure 11: Power Dissipation with Different Class of SSTL

C. When Device Operating Frequency is 3.3 GHz

Table 10: Reduction of Power with Different SSTL

Power→ SSTL↓	Clock	Signal	IO	Total
SSTL2_I	0.042	0.004	0.616	1.389
SST18_I	0.042	0.004	0.518	1.288
SSTL2_I_DCI	0.042	0.006	1.156	1.945
SSTL2_II	0.042	0.004	0.732	1.573
SSTL15	0.042	0.004	0.529	1.299
SSTL2_II_DCI	0.042	0.006	3.118	3.9570

There is no change in clock power and signal power but SSTL2_II_DCI having 80.24%, 83.38%, 62.92%, and 76.52% and 83.03% more I/O power consumption with respect to SSTL2_I, SST18_I, SSTL2_I_DCI, SSTL2_II, SSTL15 respectively at 3.3GHz as shown in Table 10 and Figure 12.

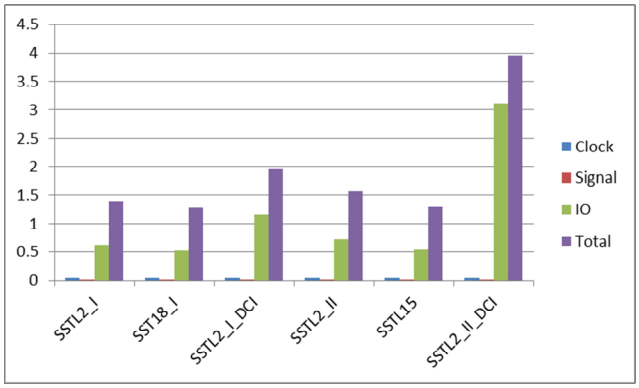

Figure 12: Power Dissipation with Different Classes of SSTL

D. When Device Operating Frequency is 3.6 GHz

Table 11: Reduction of Power with Different SSTL

Power→ SSTL↓	Clock	Signal	IO	Total
SSTL2_I	0.046	0.004	0.645	1.423
SST18_I	0.046	0.004	0.539	1.314
SSTL2_I_DCI	0.046	0.007	1.179	1.973
SSTL2_II	0.046	0.004	0.845	1.628
SSTL15	0.046	0.004	0.556	1.331
SSTL2_II_DCI	0.046	0.007	3.138	3.982

There is no change in clock power and signal power but SSTL2_II_DCI having 82.06%, 82.82%, 62.42%, and 73.07% and 82.28% more I/O power consumption with respect to SSTL2_I, SSTL18_I, SSTL2_I_DCI, SSTL2_II, SSTL15 respectively at 2.9GHz as shown in Table 11 and Figure 13.

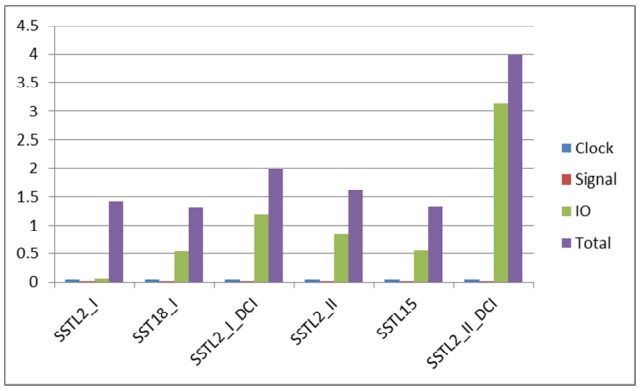

Figure 13: Power Dissipation with Different Class of SSTL

E. *When Device Operating Frequency is 3.8 GHz*

Table 12: Reduction of Power with Different SSTL

Power→ SSTL↓	Clock	Signal	IO	Total
SSTL2_I	0.048	0.004	0.664	1.446
SST18_I	0.048	0.004	0.553	1.331
SSTL2_I_DCI	0.048	0.007	1.195	1.993
SSTL2_II	0.048	0.004	0.878	1.665
SSTL15	0.048	0.004	0.725	1.352
SSTL2_II_DCI	0.048	0.007	1.3152	3.999

There is no change in clock power and signal power but SSTL2_II_DCI having 49.51%, 57.95%, 9.13%, and 33.24% and 44.87% more I/O power consumption with respect to SSTL2_I, SST18_I, SSTL2_I_DCI, SSTL2_II, SSTL15 respectively at 2.9GHz as shown in Table12 and Figure 14.

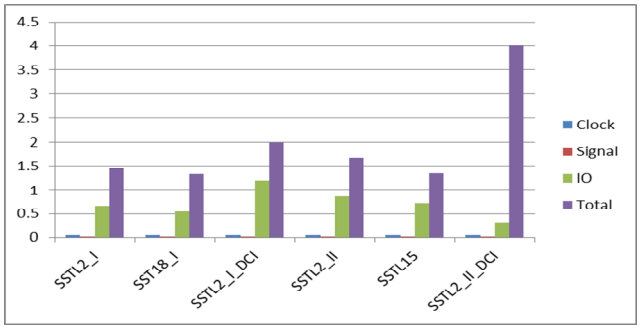

Figure 14: Power Dissipation with Different Class of SSTL

F. *When Device Operating Frequency is 4.0 GHz*

Table 13: Reduction of Power with Different SSTL

Power→ SSTL↓	Clock	Signal	IO	Total
SSTL2_I	0.051	0.004	0.681	1.466
SST18_I	0.051	0.004	0.565	0.726
SSTL2_I_DCI	0.051	0.007	1.209	2.010
SSTL2_II	0.051	0.004	0.907	1.698
SSTL15	0.051	0.004	0.590	1.372
SSTL2_II_DCI	0.051	0.007	3.164	4.014

There is no change in clock power and signal power but SSTL2_II_DCI having 78.47%, 82.14%, 61.78%, and 71.33% and 81.35 more I/O power consumption with respect to SSTL2_I, SST18_I, SSTL2_I_DCI, SSTL2_II, SSTL15 respectively at 2.9GHz as shown in Table 13 and Figure 15.

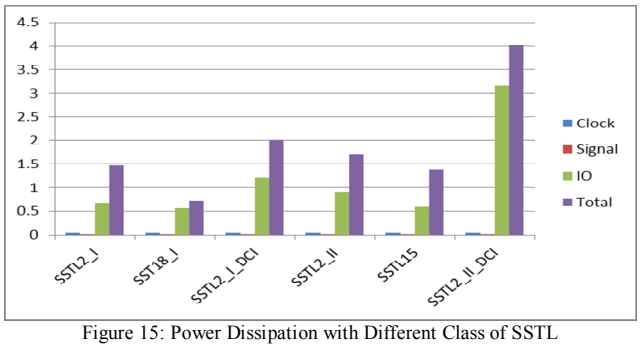

Figure 15: Power Dissipation with Different Class of SSTL

IV. CONCLUSION

The conclusion of the whole research that we have studied is basically, Our ROM is approximately 60% more energy efficient with SSTL18_I IO standard in compare to SSTL2_II_DCI. Besides, our design has passed the compatibility test with highest operating frequency of latest i7 processor. Well It is working properly in range of 1GHz-4GHz device operating frequency. Different IO standard also gives energy efficient result with different frequency.

V. FUTURE SCOPE

This ROM can be re-implemented to 28nm technology based Artix-7, Kintex-7 and Virtex-7 FPGA. We can enlarge the size of ROM from 16-bit address bus and 32-bit data bus to 64-bit architecture and even larger parallel processing. We can design other processor component like ALU, control unit and cache using SSTL IO standard. Here we are using only 5 selected SSTL IO standards, we can extend this work for more than five IO standard available on FPGA. In future, we can also design ROM with other IO standards like LVCMOS, LVTTL, MOBILE DDR, LVDS, LVDCI, and HSTL and so on.

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