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A Synchronization Method for Single-Phase Grid-Tied Inverters

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Abstract—The controllers of single-phase grid-tied inverters require improvements to enable distribution generation systems to meet the grid codes/standards with respect to power quality and the fault ride through capability. In that case, the response of the selected synchronization technique is crucial for the performance of the entire grid-tied inverter. In this paper, a new synchronization method with good dynamics and high accuracy under a highly distorted voltage is proposed. This method uses a Multi-Harmonic Decoupling Cell (MHDC), which thus can cancel out the oscillations on the synchronization signals due to the harmonic voltage distortion while maintaining the dynamic response of the synchronization. Therefore, the accurate and dynamic response of the proposed MHDC-PLL can be beneficial for the performance of the whole single-phase grid-tied inverter.

Index Terms—Harmonic distortion, inverters, phase-locked loops, photovoltaic systems, power system faults, power quality.

I. INTRODUCTION

SINGLE-phase inverters are used for converting direct current (DC) into alternating current (AC). Several grid-tied applications require the conversion of DC power into AC, such as battery storage systems, uninterruptible power supply systems, distributed generation (DG) units, and photovoltaic systems. Single-phase inverters are widely used as Grid Side Converters (GSC) that convert the power from the DC-bus and properly inject this power into the grid, with which the injected current has to be synchronized. In addition, the integration of DG energy into the power grid has to follow the modern grid codes [1]–[5], which require an injection of high quality power in the normal operation mode [1]–[6]. Furthermore, the Fault Ride Through (FRT) capability by the GSC is becoming necessary, even in small single-phase systems, as it is observed in recent studies in Japan [3] and the Italian technical rules issued in 2012 [4]. Hence, the GSC should achieve an accurate and fast response to inject synchronized grid currents of high power quality, and also provide voltage and frequency support immediately when a grid fault occurs.

Consequently, the synchronization method and control

techniques for single-phase GSCs should be enhanced to meet these stringent but essential demands. A typical single-stage single-phase inverter is shown in Fig. 1. For this system, the control of the GSC is based on the PQ controller which generates the reference currents, and the current controller which holds the responsibility for an appropriate current injection as described in [5], [7]–[12]. The PQ controller can be implemented in the stationary or synchronous reference frame as a closed-loop or an open-loop controller. Thus, a Proportional-Resonant (PR) controller in the stationary reference frame or a Proportional-Integral (PI) controller in the synchronous reference frame can be adopted as the current controller. Since the injected current has to be synchronized with the grid voltage, the response of both controllers will be affected by the performance of the synchronization method. Among a large number of reported synchronization techniques, Phase-Locked Loop (PLL) algorithms have become the most widely used solutions. Hence, PLL based synchronization methods in single-phase PV systems require further improvement as depicted in [13]–[15] to ensure a proper operation of the PV systems as aforementioned.

With respect to the PLL synchronization, a common PLL based technique to estimate the phase angle (θ) of the grid voltage (v_s) in single-phase systems is enabled by generating a quadrature voltage vector in the stationary reference frame ($v_{\alpha\beta}$). Then, this vector is transformed into the synchronous reference frame (v_{dq}), where a simple PI controller regulates the voltage v_q to zero and therefore the phase angle is extracted [15]–[16]. In each PLL technique, a different Quadrature Signal Generator (QSG) is used to generate the

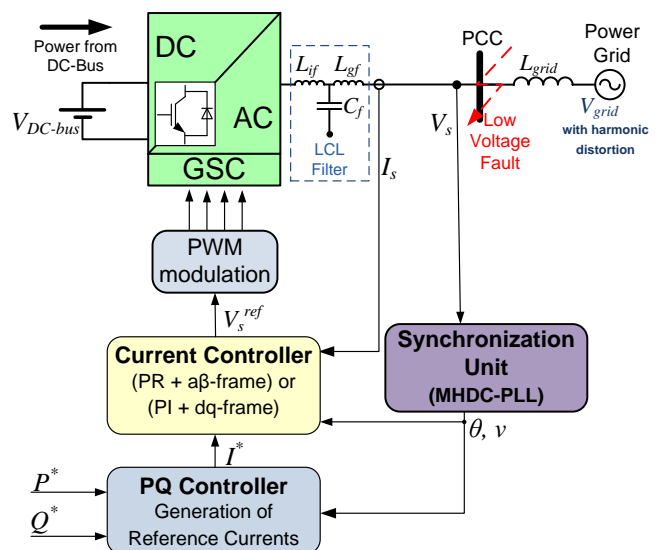


Fig. 1. Control structure of a single-phase grid-tied inverter.

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vector $v_{\alpha\beta}$. A straightforward $T/4$ delay transport technique is used in [5], [15]-[16] as a QSG, where T is the fundamental period of the grid voltage. Inaccuracy in the case of low or high order harmonics is the main drawback of this PLL system due to the lack of filtering. In contrast, the Inverse Park Transform (IPT) based PLL method [16]-[17] can filter high frequency harmonics. Moreover, some interesting techniques based on adaptive filtering and generalized integrators, such as the enhanced PLL and a Second Order Generalized Integrator (SOGI) based PLL are presented in [15]-[16], [18]-[20], which present similar filtering response with the IPT-PLL, where, however, the low frequency harmonics are not eliminated. Finally, [21] present a Hilbert based PLL technique. The harmonics effect is eliminated by this method, but unfortunately, it has practical implementation problems in the case of a real-time application with time-dependent signals.

More advanced PLL techniques have been presented in the recent literature, which enable the robustness of the synchronization against low-order harmonics. Those techniques are based on adaptive or notch filters [22]-[23], or applied repetitive and multi resonant controllers on the PLL and/or the current controller [24]-[25] of the PV system. Although these techniques achieve to overcome the harmonics effect, the dynamic response of the synchronization is slightly affected. Therefore, the harmonic robustness comes at the expense of performance deceleration of the PV system, which is undesired, especially in the case of grid faults.

In light of the above issues, this paper presents a novel PLL-based synchronization method, which can achieve accurate and dynamic synchronization performance under several grid voltage disturbances and also when the distribution grid contains both low- and high-order harmonics. The QSG of the proposed method is presented in Section II.A and it is based on a combination of an IPT and a $T/4$ delay transportation to attenuate the high-order harmonics. Then, a new Multi-Harmonic Decoupling Cell (MHDC) is proposed in Section II.B, which is designed in multiple synchronous reference frames to dynamically cancel out the oscillations due to low-order harmonics of the grid voltage. A thorough theoretical analysis of the proposed MHDC has been performed in Section II.C, proving its immunity to low-order harmonics while maintaining fast dynamics. The designed MHDC has a recursive filtering characteristic with a fast dynamic response similar to the decoupling networks presented in [26]-[30] for three-phase systems and thus, the proposed MHDC-PLL, as presented in Section II.D, can enable a fast cancellation of both low- and high-order harmonic oscillations. The accurate and dynamic response of the proposed MHDC-PLL has been verified through simulation and experiments in Section III. The performance of the proposed synchronization has been tested under several grid conditions and under several grid disturbances. The proposed MHDC-PLL is an ideal synchronization method for grid-tied inverter applications due to the high immunity against voltage harmonic distortion and the fast dynamic response under grid disturbances.

II. PROPOSED SYNCHRONIZATION METHOD

The proposed synchronization is based on three modules:

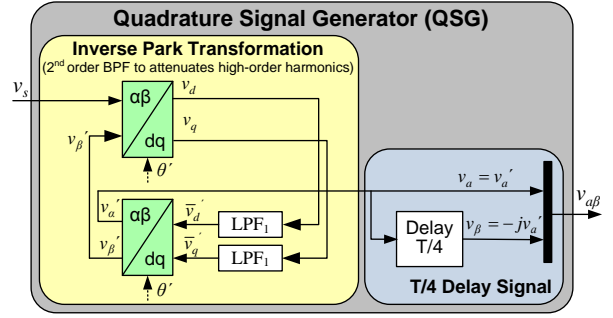


Fig. 2. The structure of the quadrature signal generator (QSG) that is used in the proposed MHDC-PLL.

the QSG, the MHDC and the dq -PLL algorithm. The QSG generates the quadrature voltage vector ($v_{\alpha\beta}$) and filters the high-order harmonics of the voltage. The MHDC module achieves the fast and accurate decoupling of the fundamental voltage vector from the oscillations caused by the low-order harmonics. Finally, the almost harmonic-free voltage signal is used by the dq -PLL technique to extract the voltage phase.

A. Quadrature Signal Generator (QSG)

The QSG used in the proposed synchronization is a combination of an IPT [5], [16]-[17], which can be considered as a band pass filter, and a $T/4$ delay transportation [15]-[16] as it is shown in Fig. 2. The voltage (v_a) is produced by using one forward and one inverse Park transformation and two first-order Low Pass Filters (LPFs), as shown in Fig. 2. The forward and inverse Park transformation can be achieved by setting the $n-m$ equal to +1 and -1 respectively in (1) and the transfer function of the LPFs is presented in (2).

$$\begin{bmatrix} T_{dq^{n-m}} \end{bmatrix} = \begin{bmatrix} \cos(n-m)\omega't & \sin(n-m)\omega't \\ -\sin(n-m)\omega't & \cos(n-m)\omega't \end{bmatrix} \quad (1)$$

$$\bar{v}_{dq} = \frac{\omega_{f1}}{s + \omega_{f1}} v_{dq} \quad (2)$$

ω' is the estimated frequency by the PLL and ω_{f1} is the cut-off frequency of the LPF. In order to derive the transfer function of the IPT, it is necessary to express (1) in terms of the Euler formula as shown below.

$$\begin{bmatrix} T_{dq^{n-m}} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} (e^{j(n-m)\omega't} + e^{-j(n-m)\omega't}) & -j(e^{j(n-m)\omega't} - e^{-j(n-m)\omega't}) \\ j(e^{j(n-m)\omega't} - e^{-j(n-m)\omega't}) & (e^{j(n-m)\omega't} + e^{-j(n-m)\omega't}) \end{bmatrix} \quad (3)$$

Now, by using the Laplace property for frequency shifting ($e^{at} = F(s-a)$), the voltage vectors v_{dq} and $v_{\alpha\beta}$ can be expressed in the complex-frequency domain as shown in (4) and (5), respectively.

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \frac{1}{2} \begin{bmatrix} (v_s(s-j\omega') + v_s(s+j\omega')) & -j(v_\beta'(s-j\omega') - v_\beta'(s+j\omega')) \\ j(v_s(s-j\omega') - v_s(s+j\omega')) & (v_\beta'(s-j\omega') + v_\beta'(s+j\omega')) \end{bmatrix} \quad (4)$$

$$\begin{bmatrix} v_\alpha' \\ v_\beta' \end{bmatrix} = \frac{1}{2} \begin{bmatrix} (\bar{v}_d(s-j\omega') + \bar{v}_d(s+j\omega')) & j(\bar{v}_q(s-j\omega') - \bar{v}_q(s+j\omega')) \\ -j(\bar{v}_d(s-j\omega') - \bar{v}_d(s+j\omega')) & (\bar{v}_q(s-j\omega') + \bar{v}_q(s+j\omega')) \end{bmatrix} \quad (5)$$

The transfer functions v_a'/v_s and v_β'/v_s can be derived as shown in (6) and (7) respectively, by substituting (4) into (2) and then (2) into (5).

$$\frac{v_{\alpha}'}{v_s} = \frac{s \cdot k \cdot \omega'}{s^2 + s \cdot k \cdot \omega' + \omega'^2}; \quad k = \frac{\omega_{f1}}{\omega'} \quad (6)$$

$$\frac{v_{\beta}'}{v_s} = \frac{k \cdot \omega'^2}{s^2 + s \cdot k \cdot \omega' + \omega'^2}; \quad k = \frac{\omega_{f1}}{\omega'} \quad (7)$$

The second-order transfer functions of (6) and (7) represent a band-pass and a low-pass filter respectively. Therefore, for optimally damped second-order filters, the factor k is set to $\sqrt{2}$ and therefore, ω_{f1} is set to $2\pi \cdot f_N \cdot \sqrt{2}$ rad/s since ω' represents the estimation of the operating angular frequency of the grid (normally at $2\pi \cdot f_N$ rad/s). f_N is the nominal system frequency (50 or 60 Hz). The transfer function in (6) is actually a second-order band pass filter, which attenuates the zero-frequency (DC offset) and the high-order frequency harmonics without affecting the amplitude and phase angle of the fundamental voltage at the nominal frequency, as it can be observed by the Bode diagram shown in Fig. 4 of section II.C. The generated voltage v_{β}' is a 90° -shifted voltage with respect to the measured voltage v_s according to (7), but v_{α}' and v_{β}' present different harmonic attenuation to the grid voltage due to the different filtering capability of (6) and (7).

Distinguished from the IPT-PLL, the use of v_{β}' is avoided in the proposed PLL, since the different harmonic filtering effects of v_{α}' and v_{β}' require a more complicated design for the MHDC. Instead, in the proposed QSG, the generation of the quadrature signal $v_{\alpha\beta}$ is obtained by the $T/4$ delay transportation of the filtered v_{α}' as shown in Fig. 2, which makes the voltages v_{α} and v_{β} to present identical low order harmonic distortions. Therefore, the transfer function of the proposed QSG is given by considering that $v_{\alpha}=v_{\alpha}'$ and $v_{\beta}=-jv_{\alpha}'$ in (6).

B. Multi Harmonic Decoupling Cell (MHDC)

The voltage vector $v_{\alpha\beta} = [v_{\alpha} \ v_{\beta}]^T$ is free of any zero or high frequency oscillations due to the QSG. The QSG acts as a second-order low-pass filter, but the low-order harmonics remain in the in-quadrature voltages. In order to cancel out the oscillations caused by the low-order harmonic through the proposed MHDC, a comprehensive analysis of the in-quadrature voltages is conducted as following. Since the v_{β} is $T/4$ delayed from v_{α} , the $v_{\alpha\beta}$ can be expressed as a summation of the fundamental component ($n=1$) and the low-order odd harmonics ($n=3, 5, 7, 9, \dots$),

$$v_{\alpha\beta} = V^1 \begin{bmatrix} \cos(\omega t + \theta_1) \\ \cos(\omega(t - \frac{T}{4}) + \theta_1) \end{bmatrix} + \sum_{n=3,5,7,9,\dots} V^n \begin{bmatrix} \cos(n\omega t + \theta_n) \\ \cos(n\omega(t - \frac{T}{4}) + \theta_n) \end{bmatrix} \quad (8)$$

$$\Leftrightarrow v_{\alpha\beta} = V^1 \begin{bmatrix} \cos(\omega t + \theta_1) \\ \cos(\omega t - \frac{\pi}{2} + \theta_1) \end{bmatrix} + \sum_{n=3,5,7,9,\dots} V^n \begin{bmatrix} \cos(n\omega t + \theta_n) \\ \cos(n\omega t - \frac{n\pi}{2} + \theta_n) \end{bmatrix}$$

where V^n and θ_n represent the amplitude and the initial phase angle respectively of the corresponding voltage component.

The voltage vector of (8) can be rewritten as shown in (9), where the summation of the harmonics can be divided into two groups according to the harmonic-order (i.e., $4l-1$ and $4l+1$ with l being 1, 2, 3, ...).

$$v_{\alpha\beta} = \begin{bmatrix} v_{\alpha} \\ v_{\beta} \end{bmatrix} = V^1 \begin{bmatrix} \cos(\omega t + \theta_1) \\ \sin(\omega t + \theta_1) \end{bmatrix} + \sum_{n=3,7,11,\dots} V^n \begin{bmatrix} \cos(n\omega t + \theta_n) \\ \cos(n\omega t - \frac{3\pi}{2} + \theta_n) \end{bmatrix} \quad (9)$$

$$+ \sum_{n=5,9,13,\dots} V^n \begin{bmatrix} \cos(n\omega t + \theta_n) \\ \cos(n\omega t - \frac{\pi}{2} + \theta_n) \end{bmatrix}$$

Using basic trigonometric identities, (9) can be expressed as (10), where it is clear that the sign of the angular speed of each component depends on the harmonic order (i.e., $4l \pm 1$).

$$v_{\alpha\beta} = V^1 \begin{bmatrix} \cos(\omega t + \theta_1) \\ \sin(\omega t + \theta_1) \end{bmatrix} + \sum_{n=3,7,11,\dots} V^n \begin{bmatrix} \cos(-n\omega t - \theta_n) \\ \sin(-n\omega t - \theta_n) \end{bmatrix} \quad (10)$$

$$+ \sum_{n=5,9,13,\dots} V^n \begin{bmatrix} \cos(n\omega t + \theta_n) \\ \sin(n\omega t + \theta_n) \end{bmatrix}$$

Therefore, the voltage vector $v_{\alpha\beta}$ can be expressed by (11), in which $\text{sgn}(n)$ defines the speed direction of each harmonic component.

$$\begin{bmatrix} v_{\alpha} \\ v_{\beta} \end{bmatrix} = V^n \begin{bmatrix} \cos(\omega t + \theta_1) \\ \sin(\omega t + \theta_1) \end{bmatrix} + \sum_{n=3,5,7,9,\dots} V^n \begin{bmatrix} \cos(\text{sgn}(n) \cdot (n\omega t + \theta_n)) \\ \sin(\text{sgn}(n) \cdot (n\omega t + \theta_n)) \end{bmatrix} \quad (11)$$

$$\text{where } \text{sgn}(n) = \sin n \frac{\pi}{2} = \begin{cases} +1 & \text{for } n = 1, 5, 9, \dots \\ -1 & \text{for } n = 3, 7, 11, \dots \end{cases}$$

The voltage vector $v_{\alpha\beta}$ can then be translated into any n^{th} synchronous reference frame ($dq^{n\text{sgn}(n)}$ -frame) with a rotating speed equal to $n\text{sgn}(n)\omega$, where ω is the fundamental angular frequency. The voltage vector expressed to the $dq^{n\text{sgn}(n)}$ -frame ($v_{dq^{n\text{sgn}(n)}}$) can be calculated by multiplying the $v_{\alpha\beta}$ with the transformation matrix $[T_{dq^{n\text{sgn}(n)}}]$ of (1) as shown in (12). The voltage vector $v_{dq^{n\text{sgn}(n)}}$ in (12) contains an oscillation-free $V_{dq^{n\text{sgn}(n)}}^n$ term, which is actually the voltage component V^n rotating at the corresponding synchronous $\text{sgn}(n)n\omega$ speed. Furthermore, it contains some oscillation terms ($V_{dq^{n\text{sgn}(n)}}^m = [T_{dq^{n\text{sgn}(n)-m\text{sgn}(m)}}] V_{dq^{m\text{sgn}(m)}}^m$) based on the effect of the rest of the voltage components.

$$v_{dq^{n\text{sgn}(n)}} = \begin{bmatrix} v_{d^n} \\ v_{q^n} \end{bmatrix} = [T_{dq^{n\text{sgn}(n)}}] \cdot v_{\alpha\beta} = V^n \begin{bmatrix} \cos(\text{sgn}(n) \cdot \theta_n) \\ \sin(\text{sgn}(n) \cdot \theta_n) \end{bmatrix} \quad (12)$$

$$+ \sum_{m \neq n} \left\{ V^m [T_{dq^{n\text{sgn}(n)-m\text{sgn}(m)}}] \begin{bmatrix} \cos(\theta_m) \\ \sin(\theta_m) \end{bmatrix} \right\}$$

$$\Leftrightarrow v_{dq^{n\text{sgn}(n)}} = \underbrace{V_{dq^{n\text{sgn}(n)}}^n}_{\text{Oscillations free term}} + \sum_{m \neq n} \underbrace{\left\{ [T_{dq^{n\text{sgn}(n)-m\text{sgn}(m)}}] V_{dq^{m\text{sgn}(m)}}^m \right\}}_{\text{Oscillation Terms}}$$

To enable the design of the proposed MHDC, the voltage vector should be expressed in all reference frames of the existing frequency components. Since the QSG has eliminated the effect of high frequency harmonics (as it behaves like a second-order low-pass filter), the proposed method only deals with the effect of the four most significant low-order harmonics. Therefore, the voltage vector should be expressed in the fundamental (+1) and the most significant harmonics (+3, +5, +7, +9) reference frames as shown in (13), where Z represents a 2×2 zero matrix.

complex-frequency domain as shown in (20), by using a lengthy mathematical analysis (similar to the one presented in Section II.A). This analysis is based on the Park's Transformations in terms of the Euler formula as defined in (3), on the Laplace property for frequency shifting ($e^{at} = F(s - a)$), and on the fact that $v_b = -jv_a$ as shown in Section II.A. Therefore, the analysis concludes into the complex first-order transfer function:

$$TFT_h = T_{dq^{-h}} \cdot [F(s)] \cdot T_{dq^{+h}} = \begin{cases} \frac{\omega_{f2}}{s + (\omega_{f2} + j \cdot h \cdot \omega')} & \text{for } h = -3, -7 \\ \frac{\omega_{f2}}{s + (\omega_{f2} - j \cdot h \cdot \omega')} & \text{for } h = 1, 5, 9 \end{cases} \quad (20)$$

Thus, substituting $TFT_h = T_{dq^{-h}} \cdot [F(s)] \cdot T_{dq^{+h}}$ of (20) into (19) yields,

$$V_{a\beta}^{*(1)} = v_{a\beta} - (TFT_{-3} + TFT_{+5} + TFT_{-7} + TFT_{+9}) (v_{a\beta} - TFT_{+1} \cdot V_{a\beta}^{*(1)}) \quad (21)$$

Finally, the transfer function of the MHDC can be derived as,

$$\frac{V_{a\beta}^{*(1)}}{v_{a\beta}} = \frac{1 - (TFT_{-3} + TFT_{+5} + TFT_{-7} + TFT_{+9})}{1 + TFT_{+1} \cdot (TFT_{-3} + TFT_{+5} + TFT_{-7} + TFT_{+9})} \quad (22)$$

If the corresponding TFT_h terms of (22) are substituted according to (20), then the eleventh-order complex transfer function of the proposed MHDC can be extracted. The $v_{a\beta}$ consists of the input voltage vector of the MHDC (as is calculated from the QSG) and $V_{a\beta}^{*(+1)} = T_{dq^{-1}} V_{dq^{+1}}^{*(+1)}$ is the equivalent output of the MHDC expressed in the stationary reference frame.

For developing the proposed MHDC-PLL, the QSG proposed in Section II.A will be connected in series with the proposed MHDC in order to dynamically extract the fundamental component of the grid voltage as shown in Fig. 3 and then a simple PLL algorithm will be used in order to extract the phase angle. Thus, the transfer function of QSG in series with the MHDC can be defined as the multiplication of the transfer function of (6) and (22):

$$\frac{V_a^{*(1)}}{v_s} = \left(\frac{v_a}{v_s} \right) \cdot \left(\frac{V_a^{*(1)}}{v_a} \right), \quad \frac{V_\beta^{*(1)}}{v_s} = \left(\frac{v_\beta}{v_s} \right) \cdot \left(\frac{V_\beta^{*(1)}}{v_\beta} \right) \quad (23)$$

Therefore, in order to investigate the response of the proposed PLL and also to design the parameter ω_{f2} of the proposed MHDC, the Bode diagrams in terms of voltage v_a of the QSG, the proposed MHDC, and the series combination of the two are presented in Fig. 4. The results for v_β are similar with a 90°-delay on the output signal. The results of Fig. 4 verify that the proposed MHDC according to (22) does not affect the dynamic estimation of the amplitude and the phase angle of the fundamental voltage component at 50 Hz. Furthermore, the MHDC can effectively eliminate the low-order harmonic components considered in the decoupling network, but it cannot affect the high order harmonics. The third and seventh harmonics are presented as negative frequency harmonics in the Bode diagram according to the construction of the voltage vector $v_{a\beta}$ as explained in Section II.B. The Bode diagram regarding the QSG is actually a band

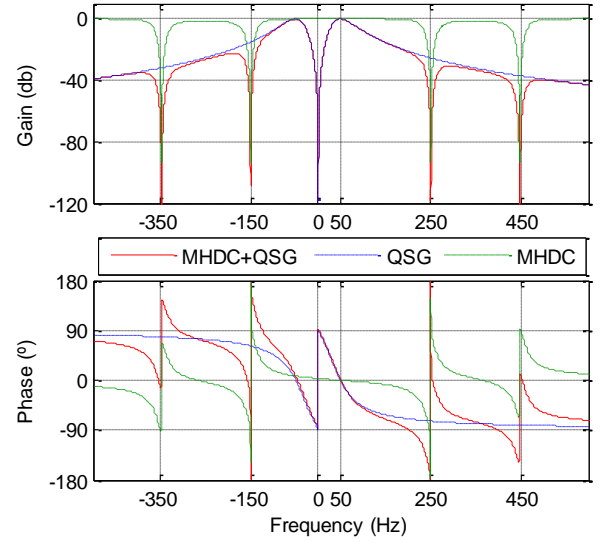


Fig. 4. Bode diagram of the proposed QSG, MHDC, and the series combination of the two.

pass second-order filter according to (6) as mentioned in Section II.A, which can eliminate the effect of the zero- and high-order harmonics. The series combination of the proposed QSG and MHDC (QSG+MHDC) represent the response of the proposed PLL according to (23). As it can be observed in the Bode diagram, the QSG+MHDC inherits the benefits of both units and therefore, the desired accurate response can be achieved since the low-order harmonics are completely eliminated by the MHDC and the zero- and high-order harmonics are minimized by the QSG. Furthermore, a dynamic response can be guaranteed since the MHDC decouples the effect of the low-order harmonics without affecting the dynamics of the estimation.

The design parameter ω_{f2} can affect the quality factor of the filter, the oscillation damping, and the time performance of the proposed MHDC. Therefore, an investigation through simulation results shows that a reasonable trade-off can be achieved by setting $\omega_{f2} = \omega_n/3$, where ω_n is the nominal angular frequency of the grid at $2\pi \cdot 50$ rad/s. For $\omega_{f2} < \omega'/3$ the response of the MHDC can present some unwanted oscillations and for $\omega_{f2} > \omega'/3$ the response of the MHDC is overdamped.

The step response regarding the estimation of the input voltage according to QSG + MHDC of the proposed PLL is presented in Fig. 5. The response of QSG+MHDC is presented in Fig. 5(a) for a step sinusoidal input in the fundamental frequency. The results verify the fast dynamic response of the proposed PLL since the input voltage is estimated with a settling time less than 0.014 s. Fig. 5(b) presents the step response for a sinusoidal step input with a 5% amplitude in the frequency of the fifth harmonic. The results show an immediate and complete elimination of the harmonic.

D. PLL Algorithm Designed in the Synchronous Reference Frame (dq-PLL)

The produced voltage vector $V_{dq^{+1}}^{*+1}$ by the MHDC is free of any harmonic oscillations as discussed in Section II.C and can be considered as a good approximation of the fundamental

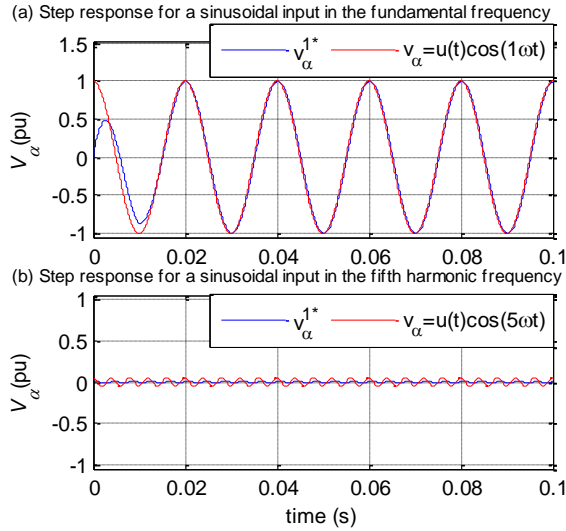


Fig. 5. The step response of the series combination of the QSG and the MHDC.

component of the grid voltage expressed in the dq^{+l} -frame as shown below,

$$\begin{aligned} V_{dq^{+l}}^{*+l} &\approx V_{dq^{+l}}^{+l} = \begin{bmatrix} T_{dq^{+l}}(\theta') \end{bmatrix} \cdot v_{\alpha\beta}^{+l} \\ &= \begin{bmatrix} \cos\theta' & \sin\theta' \\ -\sin\theta' & \cos\theta' \end{bmatrix} \begin{bmatrix} V^1 \cdot \cos\theta \\ V^1 \cdot \cos(\theta - T/4) \end{bmatrix} = \begin{bmatrix} V^1 \cdot \cos(\theta - \theta') \\ V^1 \cdot \sin(\theta - \theta') \end{bmatrix} \approx \begin{bmatrix} V^1 \\ V^1 \Delta\theta \end{bmatrix} \end{aligned} \quad (24)$$

where θ' is the estimated phase angle by the proposed PLL and θ is the real phase angle of the fundamental component of the grid voltage. Since the error $\Delta\theta = \theta - \theta'$ is very small in steady state, then $V_{dq^{+l}}^{*+l}$ can be assumed as a linearized approximation of $\Delta\theta$ as shown in (24).

Therefore, the estimated $V_{dq^{+l}}^{*+l}$ represents the amplitude of the grid voltage and the $V_{dq^{+l}}^{*+l}$ can be considered by a simple PLL algorithm, such as the dq -PLL, in order to lock the phase angle of the grid voltage as shown in Fig. 3. The structure of the dq -PLL is presented in Fig. 3, where a PI controller is used in the synchronous reference frame to extract the phase angle of the fundamental voltage. The tuning process of such a PLL is based on the linearized small signal analysis of the PLL as presented in [5], [26]-[30]. In the case that the transfer function of the PI controller is given by $K_p + 1/(T_i s)$, the closed-loop transfer function of the PLL can be simplified to the second order transfer function of (25) when the PLL is designed for a per unit voltage. The tuning parameters k_p and T_i can be calculated according to (26), where ζ should be set to $1/\sqrt{2}$ for an optimally damped PLL response and the Settling Time (ST) for the MHDC-PLL has been set to 100 ms.

$$\frac{\theta'}{\theta} = \frac{k_p \cdot s + 1/T_i}{s^2 + k_p \cdot s + 1/T_i} \quad (25)$$

$$\text{where } k_p = \frac{9.2}{ST} \text{ and } T_i = 0.047 \cdot \zeta^2 \cdot ST^2 \quad (26)$$

To sum up, the proposed MHDC-PLL consists of three main modules: the proposed QSG in Section II.A, the MHDC as proposed in Section II.B, and the PLL algorithm of Section II.D. The structure of the new MHDC-PLL with all the

TABLE I PARAMETERS FOR THE EXPERIMENTAL SETUP	
Nominal conditions	$V_N=230$ Vrms, $f_N=50$ Hz, $S_N=1$ kVA, $V_{PV}=400$ V
Sampling and PWM	$f_{\text{SAMPLING}} = f_{\text{PWM}} = 10$ kHz
Design guidelines for the MHDC-PLL	$k_p=92$, $T_i=0.000235$ $\omega_{f1}=2\pi 50\sqrt{2}$ rad/s, $\omega_{f2}=2\pi 50/3$ rad/s
LCL filter	$L_{gf}=3.6$ mH, $C_f=2.35$ μ F, $L_{gf}=4$ mH
Hardware in the loop	DS1103 dSPACE
DC Source	Delta Elektronika SM 600-10
AC Source	California Instrument MX-30
Inverter	Semikron SEMITeach (B6CI)

modules is presented in Fig. 3 and the designed parameters for the MHDC-PLL are presented in Table I. The proposed synchronization technique can achieve an accurate and dynamic response under distorted voltage and under any grid disturbances as demonstrated in Section III. The accuracy and the fast performance of the proposed PLL can potentially affect the response of the GSC controller and as a result, the performance of the whole grid-tied inverter in terms of power quality and in terms of fast FRT operations.

III. SIMULATION AND EXPERIMENTAL RESULTS

The performance of the proposed PLL requires verification through simulation and experimental results. Therefore, an experimental setup and an identical simulation model (in MATLAB/Simulink) have been implemented according to the structure of the single-phase grid-tied inverter as presented in Fig. 1. All the parameters of the implemented experimental setup are listed in Table I. The proposed synchronization method claims an outstanding performance in terms of accuracy under harmonic distorted grid voltage. Therefore, the proper response of the MHDC-PLL should be tested under harmonic distorted voltage and under other several grid voltage disturbances, such as phase jump, voltage sag, and frequency variation.

The simulation results for the response of the two PLLs (SOGI-PLL [15]-[16] and proposed MHDC-PLL with the same tuning parameters according to Table I) are presented in Fig. 6 under several voltage conditions. The voltage at the beginning of the simulation is purely sinusoidal. A significant low-order voltage harmonic distortion ($\text{THD}_v=2.93\%$) is injected by the grid at $t=0.3$ s with $|V_5|=2\%$ and $|V_7|=2\%$ relative to the fundamental and 0.75% of high-order harmonics. It is clearly observed in Fig. 6 that, for low-order harmonic distorted voltage ($t > 0.3$ s) the SOGI-PLL presents significant oscillations due to the harmonics effect, while the proposed MHDC-PLL achieves a very accurate response and is robust against harmonics due to the multi-frequency notch filtering character of the MHDC on the selected harmonics (as presented in Fig. 4). The PLLs are also tested under several voltage disturbances. For example, the MHDC-PLL presents a very accurate and dynamic response when subjected under the following sequence of events: a -30° phase change at 0.4 s, a 25% voltage sag at 0.6 s, and a 0.8 Hz frequency step at 0.8 s, despite the voltage harmonic distortion. A higher overshoot on the synchronization signals is presented by the proposed PLL due to the fast dynamic response of the MHDC regarding the fundamental frequency voltage component. Some very small but negligible oscillations on the proposed PLL are presented

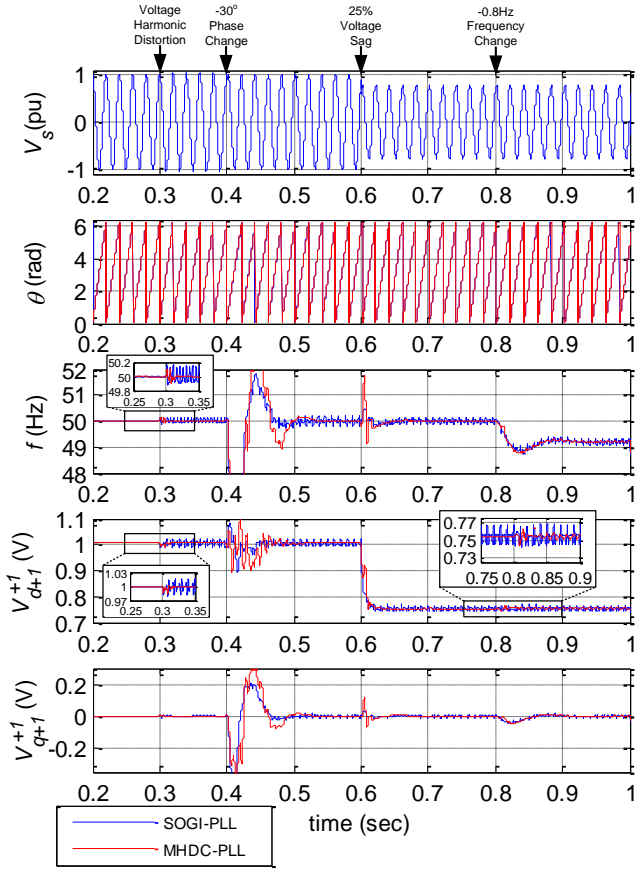


Fig. 6. Simulation results for the response of SOGI-PLL and the proposed MHDC-PLL under harmonic distorted voltage and phase step change, voltage sag, and frequency step change.

for $t > 0.8$ s due to the imperfect response of the T/4 delay component used in QSG under frequencies which are different from the nominal one.

The robust performance of the proposed PLL is also validated according to the experimental results of Fig. 7. The experimental synchronization signals are depicted in the channels 1-4 of the oscilloscope by using the Digital to Analogue Converter (DAC) of the dSPACE board. The monitoring signals θ' , f' , v_q' and v_d' of Fig. 7 represent the synchronization signals that are estimated by the two PLLs. The responses of the SOGI-PLL (left side) and the proposed MHDC-PLL (right side) are presented in Fig. 7 under several grid conditions: (a) under normal operating conditions, (b) when a harmonic distortion ($|V_5|=2\%$ and $|V_7|=2\%$ relative to the fundamental and 0.12% of high-order harmonics) is applied on the grid voltage, (c) under a 25% voltage sag, (d) under a -30° phase jump, and (e) under a -0.8 Hz frequency step change. The proposed PLL presents immunity against harmonic distortion according to Fig. 7(b). Moreover, the MHDC-PLL presents equivalent dynamic response compared to the SOGI-PLL under several grid disturbances (without any harmonic distortion) as shown in Fig. 7(c)-(e). Therefore, the harmonic robustness and a fast dynamic response is achieved by the proposed synchronization method. The only disadvantage of the proposed PLL is demonstrated in Fig. 7(e), where the MHDC-PLL presents some small oscillation on the synchronization signals under a non-nominal frequency due to the imperfect response of the discrete implemented T/4

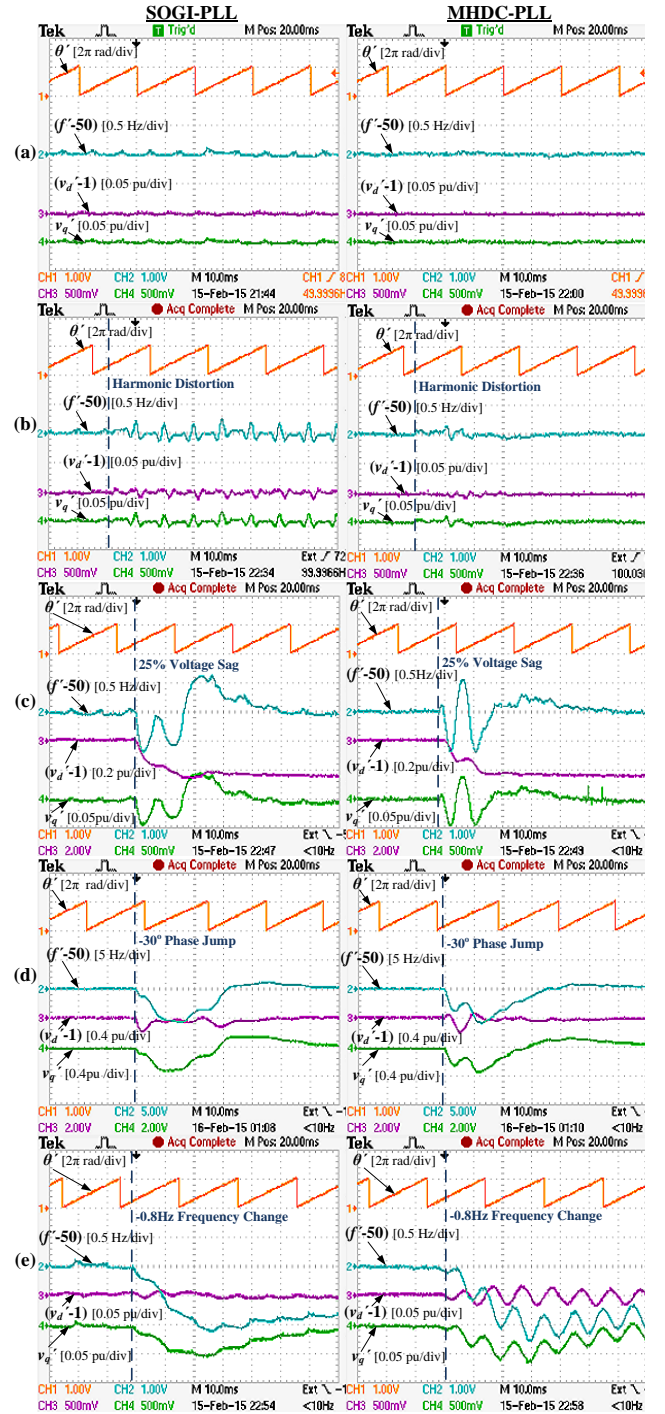


Fig. 7. Experimental results for the synchronization response of the SOGI-PLL (left hand side) and of the MHDC-PLL (right hand side). The performance of PLLs are presented (a) under normal grid conditions, (b) when harmonic distortion is applied on grid voltage, (c) under a voltage sag, (d) under a phase jump and (e) under a frequency step change.

delay component. It should be noted that these oscillations can be minimized by rounding the number of samples considered in the T/4 delay component to the nearest integer or can be completely eliminated by using a variable sampling rate (if this is not restricted by the rest of the control algorithm of the GSC) similar to the methods described in [31]. Furthermore, the oscillations under non-nominal frequency can completely be eliminated if the T/4 delay component is developed

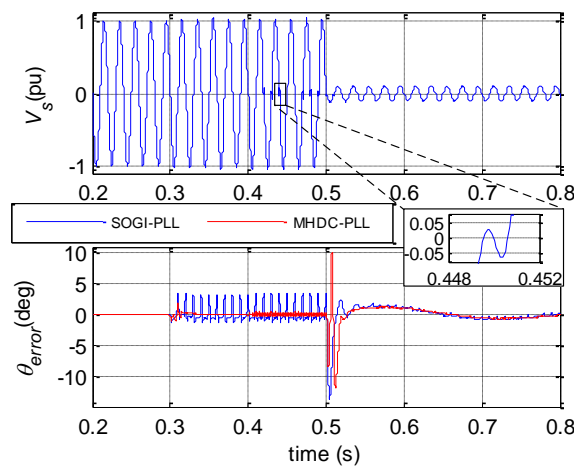


Fig. 8. Simulation results for the response of the SOGI-PLL and the proposed MHDC-PLL under the worst-case harmonic distortion and under a worst-case voltage sag (90%).

according to the fractional-order delay method of [32]. It is to be noted that the disturbances during the experimental tests were manually recreated by a programmable AC source. Therefore, the same disturbance was recreated for each PLL as shown in Fig. 7, but the moment of fault was not a controllable variable and thus, the voltage phase at the instant of fault (and the initial disturbance) is different for each PLL.

To further verify the performance of the proposed PLL in terms of a high harmonic immunity, the proposed PLL needs to be tested under the worst-case harmonic distortion. Therefore, the simulation results in Fig. 8 demonstrate the responses of SOGI-PLL and MHDC-PLL under several harmonic distorted grid voltages. For $t < 0.3$ s, the grid voltage is a purely sinusoidal voltage (with a voltage THD_v equal to 0.75% due to high order harmonics). For $0.3 \text{ s} < t < 0.4$ s, the voltage harmonic distortion includes only 3rd, 5th, 7th and 9th harmonics ($|V_3|=5\%$, $|V_5|=6\%$, $|V_7|=5\%$, $|V_9|=1.5\%$ relative to the fundamental and the same high-order harmonics). For $t > 0.4$ s, the harmonic distortion of the grid voltage is according to the worst-case scenario as defined by the Standard EN50160 [6] ($|V_3|=5\%$, $|V_5|=6\%$, $|V_7|=5\%$, $|V_9|=1.5\%$, $|V_{11}|=3.5\%$, $|V_{13}|=3\%$, $|V_{15}|=0.5\%$, $|V_{17}|=2\%$, $|V_{19}|=1.5\%$, $|V_{21}|=0.5\%$, $|V_{23}|=1.5\%$, $|V_{25}|=1.5\%$ relative to the fundamental and including multiple zero-crossings). The results of Fig. 8 show that when the harmonic components are considered in the decoupling network, then the proposed PLL achieves an accurate response. However, under the worst-case harmonic distortion some small oscillations are present on the phase angle estimation of the MHDC-PLL due to harmonics that are not considered by the MHDC and are not completely eliminated by the QSG of the proposed PLL. Nevertheless, the estimation error of the proposed PLL is significantly minimized to 0.3° compared with the 3.5° of the SOGI-PLL and is within the acceptable accuracy. The proposed PLL can enhance its accuracy if the proposed decoupling network (MHDC) is expanded in order to consider the 11th and 13th harmonic orders too. In such a case, the phase estimation error can be minimized to 0.07° under the worst case harmonic distortion. Furthermore, the performance of the two PLLs under the worst-case voltage sag is also presented in Fig. 8, where a 90% voltage sag occurs at $t=0.5$ s. Both

synchronization methods present a similar dynamic performance since they require the same settling time for tracking the phase angle of the grid voltage under the worst-case voltage sag.

Therefore, the proposed MHDC-PLL presents an accurate and fast response under any grid disturbances with immunity against harmonics distortion. This outstanding response of the synchronization method can be beneficial for single-phase grid-tied inverter systems since an accurate synchronization can enhance its dynamic response under normal and FRT operation, and can improve the power quality of the injected current to the grid as has been shown in [30].

IV. CONCLUSIONS

This paper has proposed a novel single-phase MHDC-PLL, which can achieve a fast and accurate synchronization under a distorted grid voltage. The estimation accuracy of the synchronization signals is enabled by the proposed MHDC, which can cancel out the oscillations induced by low-order harmonics, but without affecting the transient response of the PLL. Simulation and experimental results have verified the accurate and dynamic response of the proposed PLL under highly distorted grid voltages and under several grid disturbances (e.g., voltage sag, phase jump). The only disadvantages of the proposed PLL are the small oscillation on the synchronization signals under non-nominal frequency, which can be overcome using an advanced fractional-order delay method, and the increased implementation complexity. Thus, the dynamic response and the immunity against voltage harmonic distortion of the proposed synchronization method can beneficially affect the performance of grid-tied inverters, especially in terms of power quality improvement.

REFERENCES

- [1] IEEE Standard for interconnecting distributed resources with electric power systems, IEEE Std 1547-2003, 2003, pp. 1–27.
- [2] B.-I. Craciun, T. Kerekes, D. Sera, and R. Teodorescu, "Overview of recent grid codes for PV power integration," in *Proc. OPTIM*, 2012, pp. 959–965.
- [3] H. Kobayashi, "Fault ride through requirements and measures of distributed PV systems in Japan", in *Proc. IEEE-PES General Meeting*, pp.1–6, 22–26 Jul 2012.
- [4] CEI 0-21: Reference technical rules for connecting users to the active and passive LV distribution companies of electricity, Comitato Elettrotecnico Italiano, 2012.
- [5] R. Teodorescu, M. Liserre, and P. Rodriguez, *Grid converters for photovoltaic and wind power systems*. John Wiley & Sons, 2011.
- [6] Standard EN 50160, Voltage characteristics of public distribution system, CENELEC: European Committee for Electrotechnical Standardization, Brussels, Belgium, November 1999.
- [7] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Industrial Electronics*, vol. 53, no. 5, pp. 1398–1409, Oct. 2006.
- [8] H. Haibing, S. Harb, N. Kutkut, I. Batarseh, and Z.J. Shen, "A review of power decoupling techniques for microinverters with three different decoupling capacitor locations in PV Systems," *IEEE Trans. Power Electronics*, vol. 28, no.6, pp. 2711–2726, June 2013.
- [9] R. A. Mastromauro, M. Liserre, and A. Dell'Aquila, "Control issues in single-stage photovoltaic systems: MPPT, current and voltage control," *IEEE Trans. Industrial Inform.*, vol. 8, no. 2, pp. 241–254, May 2012.
- [10] Y. Yang, H. Wang, and F. Blaabjerg, "Reactive power injection strategies for single-phase photovoltaic systems considering grid requirements," *IEEE Trans. Industry Applications*, vol. 50, no. 6, pp. 1–12, Nov-Dec. 2014.

[11] L. Zhang, K. Sun, H. Hu, and Y. Xing, "A system-level control strategy of photovoltaic grid-tied generation systems for European efficiency enhancement," *IEEE Trans. Power Electronics*, vol. 29, no. 7, pp. 3445–3453, July 2014.

[12] L. Hadjidemetriou, E. Kyriakides, and F. Blaabjerg, "A grid side converter current controller for accurate current injection under normal and fault ride through operation," in *Proc. IEEE IECON*, 2013, pp. 1454–1459.

[13] A. Nicastrì and A. Nagliero, "Comparison and evaluation of the PLL techniques for the design of the grid-connected inverter systems," in *Proc. IEEE ISIE*, 2010, pp. 3865–3870.

[14] S. Golestan, M. Monfared, F. D. Freijedo, and J.M. Guerrero, "Design and tuning of a modified power-based PLL for single-phase grid-connected power conditioning systems," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3639–3650, Aug. 2012.

[15] Y. Yang, F. Blaabjerg, and Z. Zou, "Benchmarking of grid fault modes in single-phase grid-connected photovoltaic systems," *IEEE Trans. Industry Applications*, vol. 49, no. 5, pp. 2167–2176, Sep.-Oct. 2013.

[16] Y. Yang and F. Blaabjerg, "Synchronization in single-phase grid-connected photovoltaic systems under grid faults," in *Proc. IEEE PEDG*, 2012, pp. 476–482.

[17] L. N. Arruda, S. M. Silva, and B. J. C. Filho, "PLL structures for utility connected systems," in *Proc. IEEE IAS Annual Meeting*, 2001, vol. 4, pp. 2655–2660.

[18] P. Rodriguez, A. Luna, R. Munoz-Aguilar, I. Etxeberria-Otadui, R. Teodorescu, and F. Blaabjerg, "A stationary reference frame gridsynchronization system for three-phase grid-connected power converters under adverse grid conditions," *IEEE Trans. Power Electronics*, vol. 27, no. 1, pp. 99–112, Jan. 2012.

[19] M. K. Ghartemani, S. A. Khajehodini, P. K. Jain, and A. Bakhshai, "Problems of startup and phase jumps in PLL systems," *IEEE Trans. Power Electronics*, vol. 27, no. 4, pp. 1830–1838, Apr. 2012.

[20] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A new single-phase PLL structure based on second order generalized integrator," in *Proc. PESC*, pp. 1–6, June 2006.

[21] S. Nakoto, M. Mobuyuki, and S. Toshihisa, "A control strategy of single-phase active filter using a novel d-q transformation," in *Proc. IEEE IAS Annual Meeting*, 2003, vol. 2, pp. 1222–1227.

[22] F. Gonzalez-Espin, G. Garcera, I. Patrao, and E. Figueres, "An adaptive control system for three-phase photovoltaic inverters working in a polluted and variable frequency electric grid," *IEEE Trans. Power Electronics*, vol. 27, no. 10, pp. 4248–4261, Oct. 2012.

[23] K.-J. Lee, J.-P. Lee, D. Shin, D.-W. Yoo, and H.-J. Kim, "A novel grid synchronization PLL method based on adaptive low-pass notch filter for grid-connected PCS," *IEEE Trans. Industrial Electronics*, vol. 61, no. 1, pp. 292–301, Jan. 2014.

[24] M. Rashid, C. Klumpner, and G. Asher, "Repetitive and resonant control for a single-phase grid-connected hybrid cascaded multilevel converter," *IEEE Trans. Power Electronics*, vol. 28, no. 5, pp. 2224–2234, May 2013.

[25] B. Zhang, K. Zhou, and D. Wang, "Multirate Repetitive Control for PWM DC/AC Converters," *IEEE Trans. Industrial Electronics*, vol. 61, no. 6, pp. 2883–2890, June 2014.

[26] L. Hadjidemetriou, F. Blaabjerg, and E. Kyriakides, "A new hybrid PLL for interconnecting renewable energy systems to the grid," *IEEE Trans. Industry Applications*, vol. 49, no. 6, pp. 2709–2719, Nov. 2013.

[27] L. Hadjidemetriou, F. Blaabjerg, and E. Kyriakides, "An adaptive tuning mechanism for phase-locked loop algorithms for faster time performance of interconnected renewable energy sources," *IEEE Trans. Industry Applications*, vol. 51, no. 2, pp. 1792–1804, Apr. 2015.

[28] P. Rodriguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos, and D. Boroyevich, "Decoupled double synchronous reference frame PLL for power converters control," *IEEE Trans. Power Electronics*, vol. 22, no. 2, pp. 584–592, Mar. 2007.

[29] L. Hadjidemetriou, E. Kyriakides, and F. Blaabjerg, "Synchronization of grid-connected renewable energy sources under highly distorted voltages and unbalanced grid faults," in *Proc. IEEE IECON*, 2013, pp. 1887–92.

[30] L. Hadjidemetriou, E. Kyriakides, and F. Blaabjerg, "A Robust synchronization to enhance the power quality of renewable energy systems," *IEEE Trans. Industrial Electronics*, vol. 62, pp. 1–11, 2015.

[31] S. Golestan, M. Ramezani, J.M. Guerrero, F.D. Freijedo, and M. Monfared, "Moving average filter based phase-locked loops: Performance analysis and design guidelines," *IEEE Trans. Power Electronics*, vol. 29, no. 6, pp. 2750–2763, June 2014.

[32] Y. Yang, K. Zhou, H. Wang, F. Blaabjerg, D. Wang, and B. Zhang, "Frequency adaptive selective harmonic control for grid-connected inverters," *IEEE Trans. Power Electronics*, vol. 30, no. 7, pp. 3912–3924, July 2015.



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