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Design of *LLCL*-filter for Grid-Connected Converter to Improve Stability and Robustness

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***Abstract* — The *LLCL*-filter has recently emerged into grid-connected converters due to the improved filtering capability which ensuring a smaller physical size. An *LLCL* -based grid-connected converter has almost the same frequency-response characteristic as that with the traditional *LCL*-filter within half of the switching frequency range. The resonance frequencies of the *LLCL*-filters based grid-connected converters are sensitive to the grid impedance as well as cable capacitance, which may influence the stability of the overall system. This paper proposes a new parameter design method for *LLCL*-filter from the point of stability and robustness of the overall system, when the grid-side current control is used. Based on this design method, the system can be stable without damping and also robust to the grid parameters variation. The influence of delay and parameter variations is analyzed in details. Last, a design example for *LLCL*-filter is given. Both simulations and experimental results are provided through a 5 kW, 380V/50 Hz grid-connected inverter model to validate the theoretical analysis in this paper.**

Keywords—LLCL-filter;robustness; stablility;delay; impedance variation;filter design

I. INTRODUCTION

Most renewable energy sources and distributed generation (DG) resources are connected to the power grid through a grid-connected inverter [1]. However, the use of Pulse Width Modulation (PWM) scheme introduces undesirable harmonics that may disturb other sensitive loads/equipment on the grid and also result in extra power losses. Hence, a low-pass power filter is required between the voltage source inverter (VSI) and the grid to attenuate the high-frequency PWM harmonics to limit the harmonic content of the grid-injected current [2].

Fig. 1 shows four different filter structures. Typically, a simple series inductor L is used as the filter interface between power converters in the renewable energy system. But it only has 20*dB*/*dec* attenuation around the switching frequency, so a high value of inductance needs to be adopted to reduce the current harmonics, which would lead to a poor dynamic response of the system and a higher power loss. In contrast to the typical *L*-filter, the high order *LCL*-filter can achieve a 60 *dB*/*dec* harmonic attenuation performance with less total inductance, significantly smaller size and cost, especially for applications above several kilowatts [3]. Recently, the trap filter which is also called *LLCL*-filter is becoming attractive for industrial applications [4]-[7], as shown in Fig. 1(c). Compared to the *LCL* filter, a small inductor is inserted in the branch loop of the capacitor, composing an L_f–C_f series resonant circuit at the switching frequency to eliminate this major harmonic component. Hence, the total inductance or capacitance of the filter can be reduced. In order to further reduce the size of the filter, a multi-tuned filter was proposed [8], but it brings the complexity to the circuit and has possible parallel resonances between the multi-tuned traps.

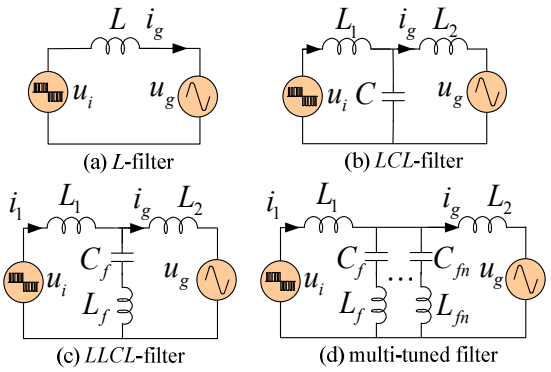

Fig. 1. Topologies of different filters for voltage source converter.

Similarly to the *LCL*-filter, the *LLCL*-filter resonance is challenging the stability of the grid-connected VSI. Hence, the high order resonance should be properly damped either passively or actively [9]-[15]. The *LLCL*-filter does not bring any extra control difficulties because an *LLCL*-based grid-connected converter has almost the same frequency-response characteristic as that with the traditional *LCL*-filter within half of the switching frequency range. In digital-controlled systems, sampling and transport delays caused by controller and the PWM modulation will affect the system stability and should be taken into account [9]-[11]. The stability of the *LLCL*-filter considering the delay effect was studied in [7]. Ref. [7] comes to the conclusion that one-sixth of the sampling frequency (f_s /6) is regarded as a critical *LLCL*-filter resonance frequency and the system can be stable, if the resonance frequency is higher than f_s /6 without damping method.

However, long distance distribution lines will introduce inductive impedance to the grid. The resonance frequency of the *LLCL*-filter is sensitive to the grid impedance. What's more, distribution cables and interaction between multi-converters also influence the stability of the system with the multiple resonance frequencies [16]-[19]. A system is robust if

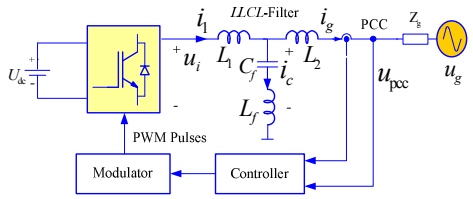

Fig. 2. *LLCL*-filter based grid-connected voltage source inverter with single-loop control.

TABLE I
PARAMETERS OF THE SYSTEM

Symbol	Definition	Value
U_{dc}	DC link voltage	650 V
U_g	Grid phase voltage	220 V
f_o	Grid frequency	50 Hz
T_s	Sampling period	100 μs
f_{sw}	Switching frequency	10 kHz

it is not very sensitive to grid and converter parameter variation. For this reason, a novel parameter design method of the *LLCL* filter for stabilizing the system operation and improving system robustness is proposed and validated. In section II the *LLCL*-filter based grid-connected inverter is modelled using the Norton equivalent model with grid current control. Section III analyzes the stability and robustness of the system considering the transmission cables. Then, a novel *LLCL*-filter design method is proposed and parameters variation is analyzed in section IV. Finally, the experiments of a 5 kW grid-connected converter are carried out to verify the theoretical analysis.

II. MODELING OF THE *LLCL* –FILTER BASED GRID-CONNECTED INVERTER

A. System Description

Fig. 2 illustrates a *LLCL*-filter based grid-connected voltage source inverter with single-loop control. The inverter output voltage and current are represented as u_i and i_1, and the grid voltage and current are represented as u_g and i_g. The voltage u_{pcc} is the voltage at the Point of Common Coupling (PCC). Z_g is the grid impedance, which can be inductive or capacitive. U_{dc} is the DC voltage. Table I shows the main parameters of the system which is used as an example for this study.

When the grid current is controlled, the corresponding control block diagram is shown in Fig. 3. G_c (s) is the implemented current controller using a Proportional Resonant (PR) controller and harmonic compensator, expressed as:

$$G_c(s) = K_p + \sum_{h=1,5,7} \frac{K_{ih} s}{s^2 + (\omega_0 h)^2} \tag{1}$$

where $\omega_o = 2\pi f_o$ is the fundamental angular frequency, K_p is the proportional gain, and K_{ih} is the integral gain of the individual resonant frequency h.

$G_d(s)$ is the computational and Pulse Width Modulation (PWM) delays.

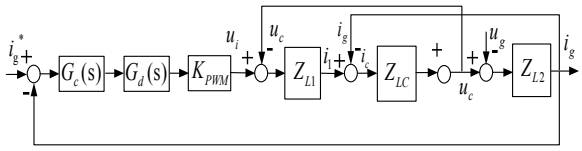

Fig. 3. Block diagram of grid current control of grid-connected converter.

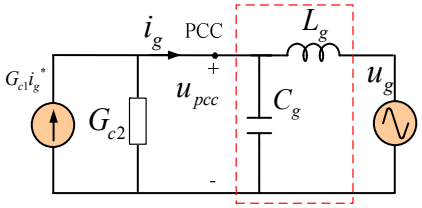

Fig. 4. Norton equivalent model of grid-connected converter with grid current control.

$$G_d(s) = e^{-\lambda T_s s} \tag{2}$$

where T_s is the sampling period of control system and λT_s is delay time, K_{PWM} is the transfer function of the inverter. Z_{L1} is the impedance of the inverter-side inductor. Z_{LC} is the impedance of the L_f-C_f circuit. Z_{L2} is the impedance of the grid-side inductor. i_g* is the reference grid current.

B. Norton Equivalent Model

Fig. 4 shows the Norton equivalent model of grid-connected converter with grid current control [19]. The dotted block is the cable capacitance C_g and line impedance L_g. The derivations of the terminal behavior of the grid current control are shown below.

The open loop transfer functions from i_g to u_i and i_g to u_{pcc} are expressed in (3) and (4), respectively.

$$G_1 = \left.\frac{i_g}{u_i}\right|_{u_{pcc}=0} = \frac{Z_{CL}}{Z_{L1}Z_{L2} + Z_{L1}Z_{CL} + Z_{L2}Z_{CL}} \tag{3}$$

$$G_2 = \left.\frac{i_g}{u_{pcc}}\right|_{u_i=0} = \frac{Z_{L1} + Z_{CL}}{Z_{L1}Z_{L2} + Z_{L1}Z_{CL} + Z_{L2}Z_{CL}} \tag{4}$$

T and G_{cl} are the open-loop and closed-loop gains of the grid current control loop, which are expressed as:

$$T = K_{PWM} G_c G_d G_1 \tag{5}$$

$$G_{c1} = \frac{T}{1+T} \tag{6}$$

The closed-loop output admittance G_{c2} can be derived as:

$$G_{c2} = \frac{G_2}{1+T} = 1/\left(\frac{1}{G_2} + \frac{T}{G_2}\right) \tag{7}$$

Hence, the closed loop expression of the grid current i_g is expressed as:

$$i_g = G_{c1} i_g^* - G_{c2} u_{pcc} \tag{8}$$

The grid voltage is seen as the disturbance term in the design of the current loop controller. The resonance at the grid side will also influence the stability of the whole system. The resonance frequency of the *LLCL*-filter ω_r ($\omega_r=2\pi f_r$) is derived as:

$$\omega_r = \frac{1}{\sqrt{\left(\frac{L_1(L_2+L_g)}{L_1+L_2+L_g}+L_f\right)C_f}} \tag{9}$$

III. Stability and Robustness Analysis

A. Concept of Passivity of the System

Given a linear and continuous system $G(s)$, two requirements should be met in order to obtain the passivity [20]:

1) $G(s)$ has no Right Half Plane poles.
2) $\mathrm{Re}\{G(j\omega)\} \geq 0 \Leftrightarrow \arg\{G(j\omega)\} \in [-90^\circ, 90^\circ], \forall \omega > 0.$

For the grid-connected converter system, the cables and *LLCL*-filters are passive if the closed-loop output admittance G_{c2} has non-negative real parts the interactions among the current control and the resonant grids will be stable [19]. But due to the presence of the delay time in the sampling and updating of PWM, a negative part could be introduced in G_{c2}. According to (3) – (6), the part of G_{c2} containing a delay can be expressed as:

$$\begin{aligned} G_{2T} &= \frac{G_2}{T} = \frac{1-(L_1+L_f)C_f\omega^2}{K_{PWM}K_p(1-C_fL_f\omega^2)}e^{j\lambda T_s\omega} \\ &= \frac{1-(L_1+L_f)C_f\omega^2}{K_{PWM}K_p(1-C_fL_f\omega^2)}[\cos(\lambda T_s\omega)+j\sin(\lambda T_s\omega)] \end{aligned} \tag{10}$$

It can be clearly seen from (10) that a negative part is probably be presented in the closed-loop output admittance G_{c2}. Hence, the passivity of the system is dependent on the filter parameters and the delay time.

According to (10), the frequency boundaries of the positive or negative are expressed in (11), (12)

$$f_{rc} = \frac{1}{2\pi\sqrt{(L_1+L_f)C_f}} \tag{11}$$

$$f_{sw} = 1/\left(2\pi\sqrt{L_fC_f}\right) \tag{12}$$

$$f_{rd} = \frac{f_s}{4\lambda} \tag{13}$$

where f_{sw} is the switching frequency and $(1-C_fL_f\omega^2)$ is always larger than zero before switching frequency. f_{rc} is the resonance frequency of L_1, $L_f$and C_f. Hence, it can be deduced that:

When $0< f_{rc} < f_s/(4\lambda)$, the system has a negative real part in the frequency interval $[f_{rc}, f_s/(4\lambda)]$.

When $f_s/(4\lambda) < f_{rc} < f_r$, the system has negative real part in the frequency interval $[f_s/(4\lambda), f_{rc}]$.

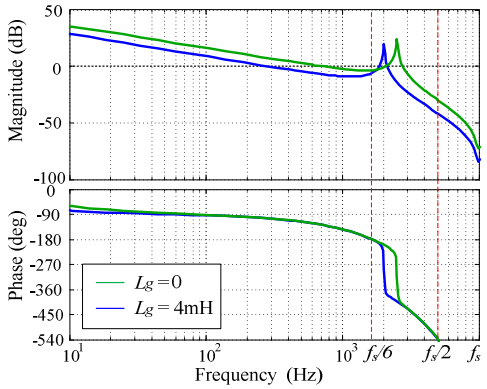

Fig. 5. Bode plots of the open-loop control gain T of different grid inductance.

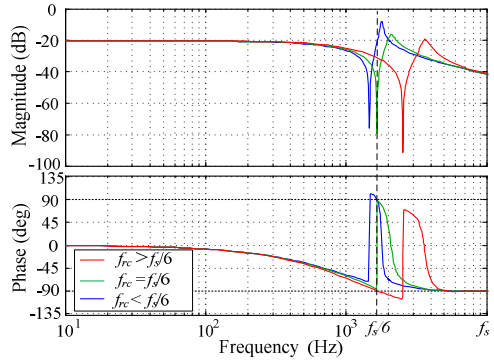

Fig. 6. Bode plots of the closed-loop output admittance G_{c2} for different resonance frequencies f_{rc}.

When $f_{rc}=f_s/(4\lambda)$, the system has no negative real part and it is the critical state.

B. Stability and Robustness Analysis

When λ=1.5, the delay is $1.5T_s$ and f_{rd} is $f_s/6$. Fig. 5 shows the Bode plots of the open-loop gain T. The system is stable at the PCC point because the phase crosses -180º before f_r due to the delay effect. Ref. [7] shows that if the resonance frequency is higher than $f_s/6$, the resonance peak is not required to be damped below 0 dB and if f_r is the resonance frequency is lower than $f_s/6$, damping method is necessary to make the system stable.

However, the real grid contains the grid impedance. If the grid impedance is inductive and only the grid impedance variation is considered, the resonance frequency will be reduced. As shown in Fig. 5, when L_g=4 mH, the resonance frequency gets close to $f_s/6$. Since L_2 is paralleled with L_1, f_r is always larger than $f_s/6$ if f_{rc} is larger than $f_s/6$ no matter how the grid inductance varies.

Fig. 6 shows the Bode plots of the closed-loop output admittance G_{c2} for different f_{rc}. It can be seen from Fig. 6 if $f_{rc} < f_s/6$ the phase of the output admittance is out of [-90□, 90□] in the frequency period $[f_{rc}, f_s/6]$. If $f_s/6< f_{rc}$ the phase of the output admittance is out of [-90□, 90□] in the frequency period $[f_s/6, f_{rc}]$. If $f_s/6= f_{rc}$ the phase of the output admittance is always between [-90□, 90□]. This is in good agreement with the negative analysis above. As shown in Fig. 4, if the grid contains cable and the resonant grid L_g-C_g interacts with

TABLE II
Maximum Harmonic Current Distortion in Percent of I_g

Individual Harmonic Order (Odd Harmonics) [%]						
I_{SC}/I_L	<11	11≤h<17	17≤h<23	23≤h<35	35<h	THD
<20	4.0	2.0	1.5	0.6	0.3	5.0

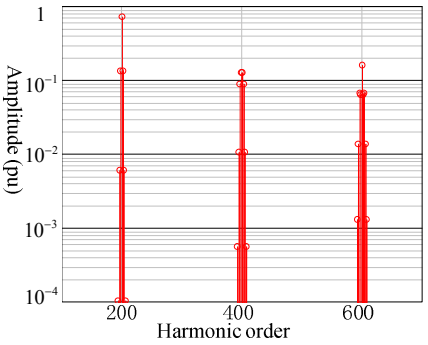

Fig. 7. Inverter output phase voltage spectrum.

the *LLCL*-filter the current control may be destabilized. So it is better to design the L_1, L_f and C_f to make f_{rc} to be chosen to $f_s/6$ in order to obtain the best robustness and passivity.

IV. *LLCL*-Filter Parameters Design Procedure

A. Conventioncal Design Constraints

When designing a power filter, the base impedance of the system should be known. The base values of the impedance, the inductance and the capacitance are referred to as:

$$Z_b = \frac{U_g^{\,2}}{P_o}, C_b = \frac{1}{\omega_0 Z_b}, \; L_b = \frac{Z_b}{\omega_0} \tag{14}$$

where

U_g the line-to-line RMS voltage;

ω_0 the grid frequency;

P_0 rated active power.

The following aspects of the design guideline should be satisfied [3], [21] and [22]:

1) Limit the total inductance (L_1+L_2). The upper limit for the total inductance should be less than 0.1 pu in order to limit the dc-link voltage on operation. A higher dc-link voltage will result in higher switching losses and thereby lower efficiency.

2) The value of the inverter–side inductor (L_1). This inductor deals with high frequency ripple current and it is constrained by the maximum ripple current.

3) Maximum harmonic distortion of the grid current. The lower limit of the filter inductance is determined by the harmonic requirement of the grid-injected current according to IEEE 519-1992[23], as specified in Table II. I_g is the nominal grid-side fundamental current. I_{SC} is the short circuit current of the power system. The harmonic currents can be calculated by the corresponding harmonic voltage amplitudes at different harmonic frequencies.

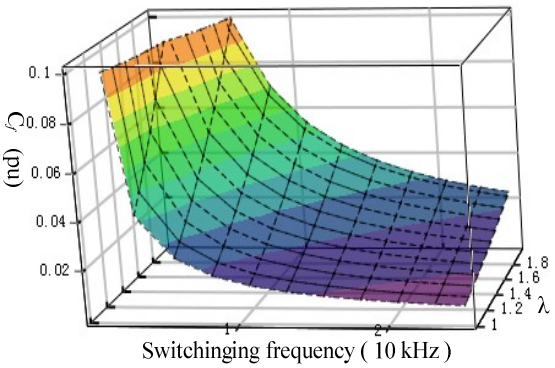

Fig. 8. The relationship between capacitance C_f, switching frequency and delay coefficient λ.

4) Design of the filter capacitance. Large capacitance can provide a better high frequency harmonics attenuation but it consumes more reactive power. For low voltage converter, it is considered that the maximum power factor variation at rated power is less than 5%, as it is expressed by the value of the base impedance of the system $C_f \le 5\%C_b$.

5) Resonance frequency of the filter. The resonance frequency is assumed to be in a range between ten times the line frequency to avoid the major low frequency harmonics and one-half of the switching frequency to avoid resonance problems.

B. Design Procedure

According to the analysis before, the parameter choices of the *LLCL*-filter are very important to the system stability and robustness. The basic design guideline is given as [24] - [26]:

1) Design of inverter-side inductor L_1. Due to the PWM, the output voltage of the inverter has high frequency harmonics as shown Fig. 7. In order to smooth the inverter side current inverter-side inductor L_1 should meet a specific current ripple requirement. The inductance can be calculated from equation $L_1 \ge U_{dc} / 8 f_s (\alpha I_{ref})$, I_{ref} is the rated reference peak current, α is the inverter-side current ripple ratio, which generally is lower than 40% of the rated reference current [4], [6];

2) Design of capacitor C_f. According to the analysis, C_f should be designed by the boundary frequency f_{rc}. It can be seen from (11) the switching frequency L_fC_f is fixed at the switching frequency. When the value of L_1 is fixed C_f can be chosen according to the delay time and sampling frequency. At the same time, the capacitor value should meet the reactive power requirements. Fig. 8 shows the value of the capacitance in pu changes with different switching frequencies and delays. It can be seen from the figure that the capacitance increases with the switching frequency and the delay coefficient λ increasing. The capacitance should statisfied the constain that $C_f \le 5\%C_b$.

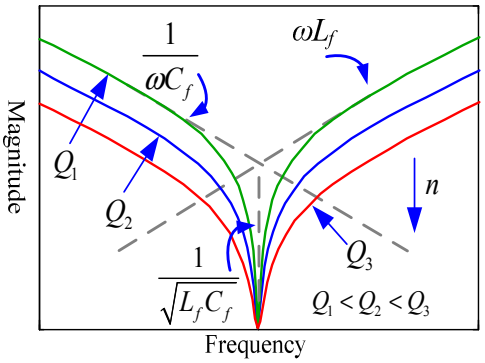

Fig. 9. Characteristic impedance of the *LC* trap filter with different L_f/C_f.

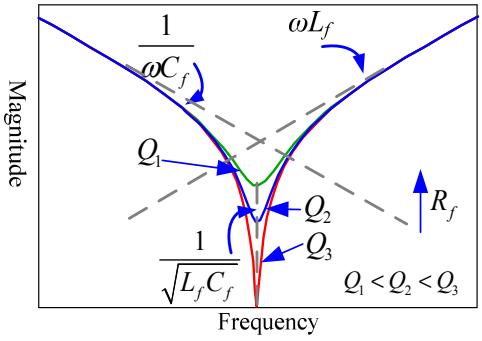

Fig. 10. Characteristic impedance of the *LC* trap filter with different R_f.

3) Design of inductor L_f of L_f-C_f circuit. If C_f is selected L_f can be chosen based on the switching frequency to attenuate the dominant harmonics. The attenuation characteristics are influenced by the L_f-C_f circuit quality. The L_f-C_f series resonant circuit quality factor can be taken as:

$$Q = \frac{1}{R_f}\sqrt{\frac{L_f}{C_f}} \tag{15}$$

$$n = \sqrt{\frac{L_f}{C_f}} \tag{16}$$

where R_f means the sum of the equivalent series inductor resistance and the equivalent series capacitor resistance. It is a parasitic resistance and no external resistance is added to the circuit. Fig. 9 shows the characteristic impedance of the *LC* trap filter with different L_f/C_f. It can be seen from Fig. 9 that the trap range is wider with the Q-factor increasing. When the range of side-band harmonics around the specific frequency is relatively wide, it should be considered to obtain a larger Q-factor of the *LC* trap filter branch to get better harmonic attenuation. Fig. 10 shows that characteristic impedance of the *LC* trap filter with different R_f. R_f will reduce the depth of the *LC* trap filter. These factors tend to lower the quality factor. Normally, the Q-factor can be $10 \le Q \le 50$ [27].

4) Selection of the grid-side inductor L_2. When L_1 and C_f are designed, L_2 should be designed to reduce the harmonic

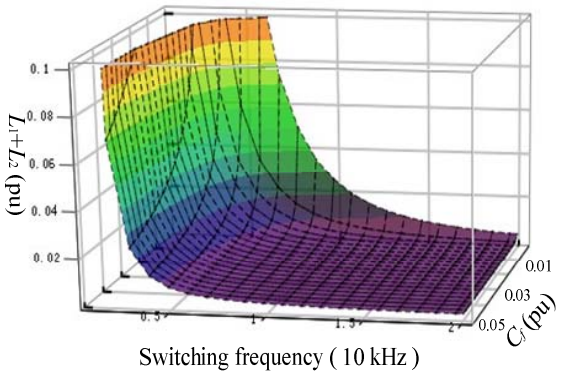

Fig. 11. The relationship between capacitance, switching frequency and total inductance.

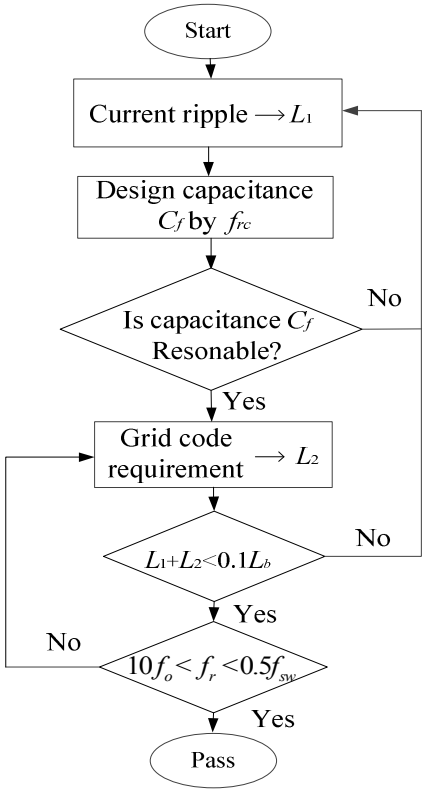

Fig. 12. Flow chart of the parameter design procedure of *LLCL*-filter.

around the double of the switching frequencies down to 0.3% [6], as shown in (5).

$$\frac{\frac{4U_{dc}}{3\sqrt{3}\pi}\times\max\left(\left|J_1(\pi M)\right|,\left|J_5(\pi M)\right|\right)\times\left|G_1(j2\omega_s)\right|}{I_{ref}} \le 0.3\% \tag{17}$$

where J_1 (πM) and J_5 (πM) are the Bessel functions corresponding to the 1st and 5th sideband harmonics at the double of the switching frequency. Because the dominant harmonics around the switching frequency are already attenuated by the *LC* trap circuit, the value of L_2 can be selected relatively low. The resonance frequency will be higher than $f_s/6$.

5) Check of the total inductance (L_1+L_2). Fig. 11 shows the value of the total inductance increases with the switching frequency and the capacitance decreasing. It can be seen from the Fig. 11 that the total inductance increases with the switching frequency and the capacitance is reduced. The value of the total inductance should be less than 0.1pu in order to limit the ac voltage drop during operation and also lower the high dc-link voltage.

6) Component tolerance. The influence of the variation of inductance and capacitance of the *LLCL*-filter will be discussed. The parameter drift of L_1, L_f or C_f may result in the resonance frequency f_{rc} variation. Generally, for industrial filters the tolerances are: Capacitors: 5% and no negative tolerance; Inductors: 2% [28]. Considering the variation of the capacitor and inductor, f'_{rc} is between [96.9%f_{rc}-103%f_{rc}].

C. Design Example

A step-by-step procedure has been proposed to obtain the parameter values of the *LLCL*-filter. The system is specified in Table I. The rated power is 5 kW. Hence, the base impedance Z_b is 29.0 Ω , the base capacitance C_b is 109.6 μF and the base inductance is L_b 92.5 mH. A design example is shown in Table III with following steps:

TABLE III
PARAMETERS OF THE FILTER

Symbol	Definition	Value
L_1	Inverter-side inductor	2.2 mH
L_2	Grid-side inductor	1.8 mH
L_f	Resonant inductor	64 μH
C_f	Capacitor	4 μF
f_r	Resonant frequency	2.45 kHz
f_{rc}	Frequency	1670 Hz

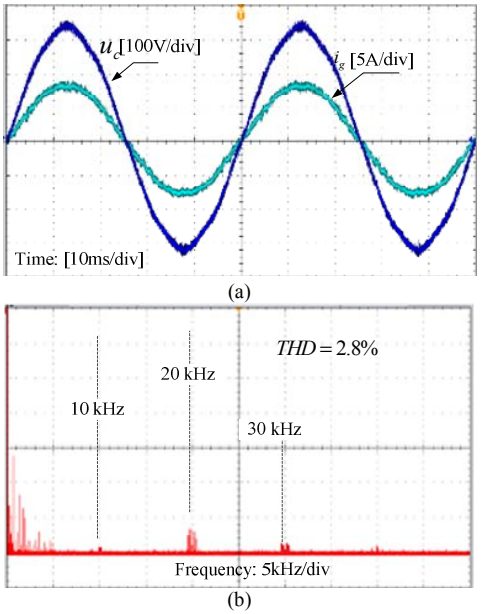

Fig. 13. Experimental results of the designed *LLCL*-filter parameters. (a) Grid current waveform (b) Grid current spectrum.

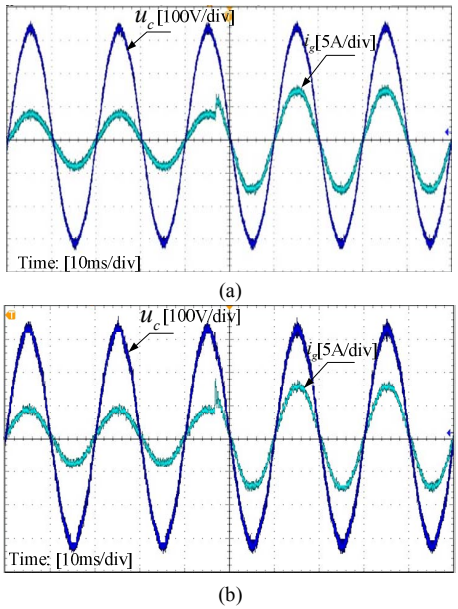

Fig. 14. Transient experimental results when the grid current reference is changed. (a) L_g = 0. (b) L_g = 4.8mH.

1) Based on the constraint of the total inductor and inverter-side current ripple, a 30% current ripple can be obtained to design the inverter inductor L_1. Then the inverter-side inductor is selected to be 2.2 mH.

2) Considering $1.5T_d$ delay and 10 kHz switching frequency the capacitor value is designed as 4 μF in order to make the frequency f_{rc} is f_s/6 and meet the constraint of 5% reactive power.

3) For the L_f-C_f resonant circuit, L_f can be chosen based on the chosen C_f and the switching frequency. It is calculated to be 64 μH.

4) The grid-side inductor value of L_2 can be calculated by the injected grid current harmonics standard. L_2 is selected to be 1.8 mH.

5) Check the total inductance and the possible variation of real value of f_{rc}.

V. EXPERIMENTAL RESULTS

The experimental setup consists of a 5 kW Danfoss FC302 converter connected to the grid through an isolating transformer and the DC-link supplied by Delta Elektronika power sources. The control algorithm has been implemented in a dSPACE DS1103 real time system. TABLE I shows the experimental parameters.

Fig. 13(a) shows the steady state waveforms of the grid current and the L_f-C_f trap voltage for the designed parameters when the grid impedance is neglected, L_g=0 mH. Fig. 13(b) shows the grid current spectrum. It can be seen from the spectrum that the dominant harmonics occur around the double of the switching frequency because the switching harmonics have been attenuated by the trap circuit.

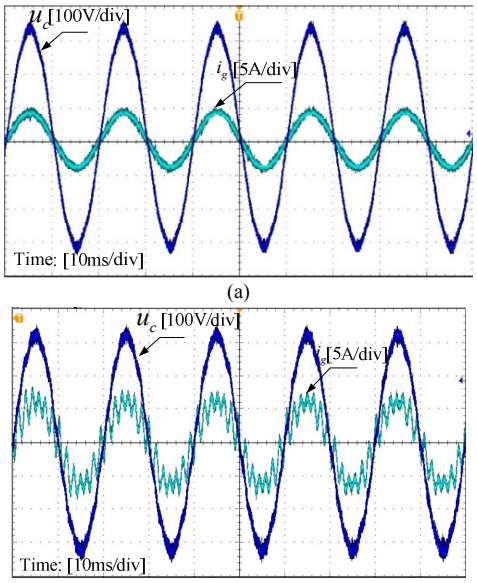

Fig. 15. Experimental waveforms with L_g = 2 mH, C_g = 6.7 μF when (a) follow the design method (b) design method is not followed (C_f = 8 μF).

Fig. 14 shows the transient experimental results when the grid current reference steps in the middle. Fig. 14(b) shows dynamic transition only considering the variation of grid inductance, L_g=4.8 mH. The system has a good robustness in the weak grid.

Fig. 15 shows the experimental results when grid impedance has the values: L_g = 2 mH, C_g =6.7 μF. Fig. 15(a) shows the experimental waveforms when the design method is followed. f_{rc} is designed very close to f_s/6. Fig. 15(b) shows the experimental waveforms, when the design method is not followed and the capacitor C_f is changed to 8 μF. The *LLCL*-filter interacts with the L_g-C_g impedance and make the unstable point to fall into the period the phase of the output admittance is out of the period [-90□, 90□] as discussed in Fig. 6. In that case the system cannot get the passivity.

VI. CONCLUSION

This paper proposed a new design method for the *LLCL*-filter to improve the stability and robustness of a grid-connected system. It can be seen that:

1. The robustness of the *LLCL*-filter based grid-connected system is mainly influenced by the inverter-side inductor and the capacitor.
2. When L_1, C_f, L_f are designed to make f_{rc} to be close to the one-sixth of the sampling frequency, the sensitive frequency period can be disappeared or minimized. The resonance frequency of the *LLCL*-filter is always larger than one-sixth of the sampling frequency no matter how the grid impedance varies. The current control also has the passivity and good robustness to the grid impedance and cable capacitance.
3. A step by step filter design method is proposed based on the analysis. Parameters variation also influences the system robustness and accuracy of the design.
4. A 5 kW grid-connected converter system is implemented to verify the theoretical analysis on the *LLCL*-filter. It can be found that the experimental results match the theoretical analysis results well.

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